OPTIREG™ switcher TLS412x PCB layout and routing guidelines

About this document

Scope and purpose

The scope of this Application Note is limited to the OPTIREG™ Switcher TLS412x family of synchronous buck DCDC converters. The purpose of this Application Note is to provide printed circuit board layout and routing guidelines for the TLS412x converter.

Intended audience

This Application Note is intended for users of Infineon's TLS412x family of synchronous buck DC/DC converters.

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1 Definitions

EMC– Electromagnetic Compatibility is the ability of a device to function in its specified environment while not disturbing other devices in the same environment.

EMI – Electromagnetic Interference that effects the performance of a device.

Goal – A non-critical requirement that must be addressed and is not subject to verification.

IC – Integrated Circuit

I/O – input/output

PCB – Printed Circuit Board

Recommend/Recommended – Identifies a critical requirement (highlighted with bold font). Implementation and verification are advised.

Should –Used to indicate a non-critical provision that must be addressed in the design (highlighted with italic font).

SMD - Surface Mount Devices

THM - Through Hole Mounted devices

Will – Used to indicate a statement of fact and is not subject to verification.

2 General guidelines

The General Guidelines of paragraph 2 describes basic layout topics and principles that are applicable to TLS412x and other general non-isolated power supply applications. Paragraphs **4** and **5** describes specific layout guidelines for the TLS412x which rely on the general guidelines of paragraph 2.

The TLS412x synchronous buck DC to DC converter is usually included on a system board with a microcontroller, and other analog and digital circuits. Therefore, similar layout guidelines *should* apply to the entire system board were applicable.

A good reference for a detailed discussion and explanation of some of the concepts presented in this application note can be found in the book by Henry W. Ott, Electromagnetic Compatibility Engineering [**5**].

2.1 Power supply layout background

Power supply printed circuit board (PCB) layout and routing are extremely critical to proper and reliable circuit function. Compared to analog and digital circuits, power supplies usually have much higher currents and voltages. This makes trace width and clearance (spacing) more important. Also, modern switching power supplies operate at high frequency (>400 kHz) and require fast switching times (<50ns) to achieve high efficiency. This combination of high current, high voltage and high speed make some trace lengths very critical – they must be kept very short.

EMI is an undesirable side effect of fast switching and has the potential to disrupt operation of the power supply, nearby analog and digital circuits, other PCBs and cause the power supply to exceed allowable EMC limits. Completely eliminating power supply noise is not possible. The approach which must be taken is to localize or “contain” the noise. Techniques used include isolation (separation) of noisy and sensitive circuits, shielding by means of ground planes and decoupling through use of strategically placed ceramic capacitors and ferrite beads.

Power supply PCB design is not simple. Auto-routing will not be successful. Hand routing is required. Also, it is nearly impossible to define all layout requirements at the outset. The design is an interactive process involving the PCB designer, mechanical engineer and the electrical engineer. Also, it may take several iterations or sub-iterations of the layout to obtain a workable design.

2.2 Power path loops

The power stage placement and power path routing is critical to a successful PCB design. A simplified schematic of a synchronous buck converter with four different power path loops is shown in Figure 1. The high main power stage components are C_{in}, SW1, SW2, L_{out} and C_{out}. The TLS412x has integrated power switches (SW1 and SW2).

The four power path loops are:

1. Input Loop (DC) – This is the current loop of the unregulated input source. This is a DC loop because the current is continuous (not pulsing).
2. Power Switch Loop (AC) – This is the current loop formed when the power switch (SW1) is ON and the synchronous rectifier (SW2) is OFF. Current flows from the input capacitor (C_{in}) through SW1, output

inductor (L_{out}), output capacitor (C_{out}) and back to C_{in}. This is an AC loop because the current is pulsing with high $\Delta i/\Delta t$.

3. Synchronous Rectifier Loop (AC) – This is the current loop formed when SW2 is ON and SW1 is OFF. Current flows through SW2, L_{out}, C_{out} and back to SW2. This is an AC loop because the current is pulsing with high $\Delta i/\Delta t$.

4. Output Loop (DC) – This is the current loop of the regulated output voltage and load. This is a DC loop because the current is continuous (not pulsing).

Power paths and loops *should* be free of vias (paragraph **2.12**) and thermal relief (paragraph **2.13**). AC loops 2 and 3 above are the most critical in the PCB layout and it is **recommended** that they be given high priority. All layout decisions and compromises *should* consider the effect on the AC power path loops. However, the DC loops must not be ignored as they do effect efficiency, regulation and stability because long, high current DC traces are lossy and have inductance.

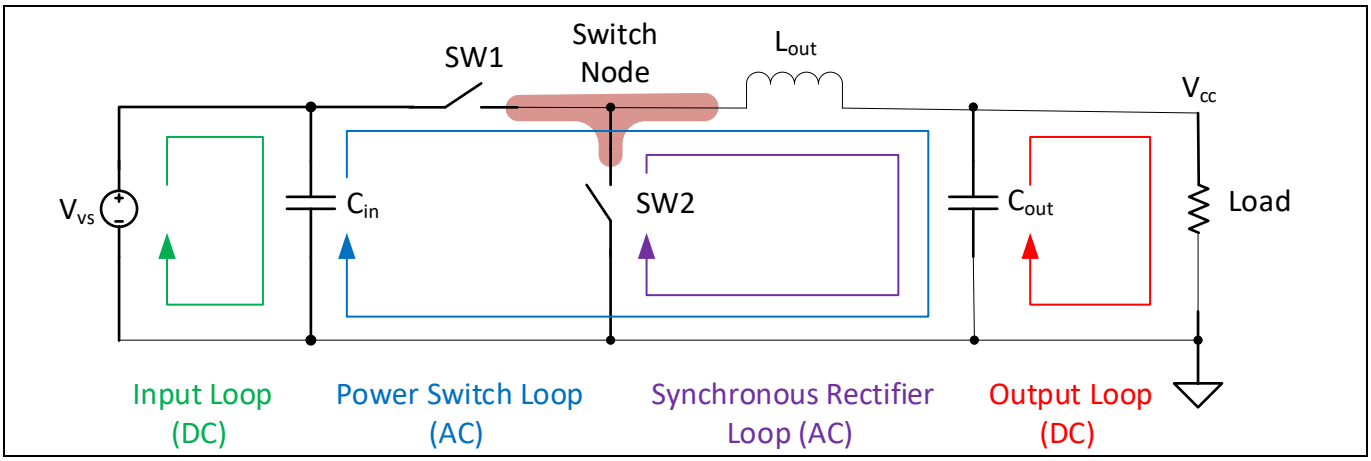

Figure 1 Buck Converter Power Path Loops

2.3 Switch node

The switch node is the output of a power switch in a switching power supply. In a buck converter, this is the common half bridge connection of the high side and low side switches (highlighted area in Figure 1). It is one of the biggest noise generators in the power supply (paragraph **2.4.4.2**) and therefore is a critical signal (paragraph **2.6**). Attention must be given to minimizing its PCB area to limit EMI while also sizing its traces properly for current and temperature rise considerations (paragraph **2.9**). Ground plane placement under the switch node for shielding is important while at the same time controlling the capacitive ground plane coupling (paragraph **2.11**).

It is **recommended** that the switch node be given a high priority in the PCB layout. All layout decisions and compromises *should* consider the effect on the switch node.

2.4 Component placement

Components *should* be placed initially in accordance with paragraphs **2.4.1**, **2.4.2**, **2.4.3** and **2.4.4**. The layout *should* then be adjusted or “iterated” to meet all the concerns of paragraph 2.4. The result will be a

compromise. It will not be possible to optimally satisfy all criteria. However, each concern must be addressed until an acceptable compromise is reached.

2.4.1 Preliminary parts placement

A preliminary parts placement *should* be used for initial PCB planning and area assessment. For a successful layout, it must start early in the PCB design process. Waiting until the end when all other circuits on the system board are placed will most likely impact reliability, efficiency and EMC/EMI.

Preliminary Placement Objectives:

1. **Recommend** that power stage components be given a priority in the preliminary parts placement while thinking about the power path loops (paragraph **2.2**).
2. Power stage components *should* be placed on the same side of the PCB to minimize the need for vias (paragraph **2.12**).
3. A design goal is to place the power supply near its load.
4. **Recommend** that EMI filters for off board input sources be placed adjacent to PCB entry connector. The EMI filter output *should* connect to the power supply input with a short and direct trace. This may conflict with 3 above, but 4 *should* be a higher priority. Consideration *should* also be given to minimizing radiated emissions from this trace by keeping it short and placing local decoupling capacitors (paragraph **2.4.6**) at the power supply input.
5. **Recommend** that noise generators (paragraph **2.4.4.2**) not be placed near EMI filters.

The initial parts placement will usually be a provided to the PCB designer in the form of a sketch or computer aided design (CAD) drawing. This drawing *should* show the PCB outline, keep out zones, large electrical components (magnetics, thru-hole parts, etc.), mechanical components (heatsinks, mounting holes/screws, etc.) and other critical component placement.

2.4.2 Partitioning

The components *should* be partitioned (or grouped) in accordance with circuit function. In the addition to the Preliminary Parts Placement (paragraph **2.4.1**), a sketch (or CAD drawing) *should* be provided to the PCB designer indicating where these additional components and circuit functions are to be located on the board.

2.4.3 Circuit flow

Components *should* be placed to allow ease of circuit flow, to facilitate hookup, and minimize crossovers, long traces and optimize power paths loops (paragraph **2.2**). Placement *should* allow for short traces when required (paragraph **2.10**). Additional PCB area *should* be allotted for heavy traces and PCB heatsinks (paragraph **2.9**), electrical clearance (paragraph **2.14**) and heavy traffic flow.

2.4.4 Sensitive and noisy circuits

Sensitive circuits are circuits which are especially vulnerable to electrical noise. Noisy circuits are noise generators. In most power supplies (or PCB assemblies which include power supplies), there are noisy circuits and usually some sensitive circuits. These circuits must be kept separate from each other. Preferably, they

should be separated a minimum of one inch. Sensitive and noisy circuits will need be to be identified on the schematic**.**

2.4.4.1 Sensitive circuits

Common sensitive signals include:

1. Power Supply Feedback Signal – Noise coupled onto the feedback signal will be injected into the regulation control loop which may cause erratic and unpredictable behavior. This noise can originate directly from the power supply output and/or other radiated noise sources in the system.
2. Error Amplifier Compensation Circuits – For power supplies with external loop compensation, noise in the error amplifier compensation circuit will be very disruptive to the regulation loop as described in 1 above. This concern is not applicable to the TLS412x because it has an integrated (internal) error amplifier and loop compensation.
3. Switching Frequency Clock – It is well known that clocks are noise generators. However, a clock oscillator based upon a discrete capacitor being charged from an IC current source is also vulnerable to misbehavior due to noise.
4. High Gain & Bandwidth Analog Circuits – These circuits have the gain and bandwidth to significantly amplify noise. Both gain and bandwidth *should* be limited to what is necessary to meet system requirements.
5. High Impedance Circuits – A low level noise current coupled onto a high impedance circuit will produce a large noise voltage. Of course, the magnitude is also dependent upon the noise source impedance. Examples include open drain signals with a high impedance pull up resistor, floating signals and analog voltage divider circuits. Lowering circuit impedance as much as practical is a good design goal to reduce noise problems.

2.4.4.2 Noise generators

Common noise generators include:

1. Power Supply Switch Node – The switch node (paragraph **2.3**) has high $\Delta v/\Delta t$ and $\Delta i/\Delta t$ characteristics due to fast power switch turn on/off times resulting in significant radiated emissions. It is one of the biggest noise generators in the power supply and must be given significant attention. Properly designed snubbers and power switch gate drivers can be effective in controlling switch node noise.
2. Clocks and Oscillators – See paragraph **2.7**
3. High $\Delta i/\Delta t$ loops – Switching power supplies have pulsating current loops with high $\Delta i/\Delta t$ (**2** and **3** of paragraph **2.2**). It is not possible to eliminate them. However, the goal will be to reduce the radiated noise by minimizing the loop areas. Thoughtful parts placement is critical in achieving this goal.
4. High $\Delta v/\Delta t$ Circuits – In addition to the switch node, gate drivers and synchronization signals have high $\Delta v/\Delta t$ with fast rise and fall times. A series resistor at the source can be helpful in controlling rise/fall times in low power/current circuits.

2.4.5 Keep out zones

Noisy circuits such as those described in paragraph **2.4.4.2** or other high frequency circuits are **recommended** to be kept away from any I/O connector areas on the PCB. These circuits can couple high frequency electromagnetic fields onto I/O cables, connectors and circuitry. These circuits are **recommended** to be kept at least 0.5 inches away from the I/O area to minimize coupling.

2.4.6 Decoupling capacitors

2.4.6.1 High frequency decoupling

Power supply decoupling capacitors in high frequency circuits are critical for EMC/EMI performance. Therefore, decoupling capacitor placement and routing *should* be given a high priority early in the PCB design. It is desirable to place and route these capacitors first before routing the other signals on the board. If effective decoupling is required above approximately 50 MHz, more than one capacitor is required. This is because the parasitic inductance (not the capacitance) dominates the impedance of ceramic capacitors above 50MHz. Paralleling multiple capacitors effectively lowers the impedance above 50MHz. This is because the equivalent inductance of a parallel capacitor network is lower because the inductances are in parallel.

The requirements for effective decoupling using multiple capacitors are:

1. Make all capacitors the same value. This equalizes the current in each capacitor. It also eliminates parallel resonance (or anti-resonance) with unequal capacitor values. Anti-resonance produces impedance spikes degrading decoupling effectiveness.

   Use the smallest practical package size. This minimizes the capacitor parasitic inductance. The parasitic inductance of a ceramic capacitor increases as the package size is increased. Keep in mind that smaller packages usually have lower voltage ratings compared to larger packages. Capacitance derating due the ceramic capacitor voltage coefficient is therefore more significant with smaller (lower voltage) packages.

2. Connect these capacitors directly to the IC power pins with short/wide traces. Connection directly to the power and ground plane is allowed. However, the goal is to minimize the loop in which the current flows.

3. Avoid using vias if possible due to the added inductance. However, if vias are needed then try to parallel multiple vias for reduced impedance.

4. Each capacitor *should* be connected to the IC through a different trace in order to minimize the mutual inductance.

5. If vias are used, locate the vias on the side of the capacitor package. Each via (power and ground) *should* be on the same side of the package. This minimizes the loop area and reduces the impedance.

The high frequency decoupling capacitors will need to be identified on the schematic. Judgements are needed to determine if the requirements have been satisfied. Where conflict exists, priorities must be set in order to make compromises.

2.4.6.2 Low frequency decoupling

Analog circuits generally operate at low frequencies and therefore have less severe decoupling requirements. The requirements as described in paragraph **2.4.6.1** apply except – only one decoupling capacitor is required and requirements **1** and **4** do not apply.

2.4.7 Thermal and structural considerations

Thermal and structural issues are very important. Where appropriate, specific guidelines will need to be given to the PCB designer. Proper review of layouts/heatsinks are needed to insure design integrity. Often these issues are addressed first. However, in power supplies where layout and routing are extremely critical for proper circuit function, it is best to tend to circuit concerns first and then make the best of thermal and structural concerns.

2.5 Multilayer board objectives for EMC

There are six design objectives that *should* be considered:

1. A signal layer *should* always be adjacent to its power or ground plane.
2. Signal layers *should* be tightly coupled (close) to their adjacent planes.
3. Power and ground planes *should* be closely coupled together.
4. High-speed signals *should* be routed on buried layers located between planes. The planes can act as shields and contain the radiation from the high-speed traces. Also, the effective impedance (inductance) of the trace is reduced by placing it adjacent to ground plane. Objectives 3 and 4 cannot be satisfied simultaneously on a PCB with less than eight layers.
5. Multiple ground planes are very advantageous because they will lower the ground (reference plane) impedance of the board and reduce the common mode radiation.
6. When critical signals are routed on more than one layer, they *should* be confined to two layers adjacent to the same plane.

2.6 Critical signals

Most of the EMI issues associated with PCBs are caused by a relatively few critical signals. These signals are generally repetitive high frequency signals with fast rise and fall times. Examples include digital circuits, clocks, gate drivers, power switching MOSFETs, switch node (paragraph **2.3**) and AC power path loops (paragraph **2.4.4.2**).

These signals will need to be identified on the schematic for the PCB designer. Routing these signals *should* be given high priority in PCB layout.

2.7 System clocks

High frequency clock traces *should* be kept as short as possible. Clock circuits *should* be given high priority in component placement and routing in order to minimize trace length. A ground plane is **recommended** to be placed under the crystal, oscillator or driver on the component side of the board. This ground is **recommended** to be connected to the main ground plane with multiple vias.

2.8 PCB and layer definition

To minimize PCB warpage, a proper copper balance *should* be maintained between layers. Also, any special constraints *should* be identified such as separation of power and signal traces, separation of noisy and sensitive traces, partitioning of ground planes, etc. EMC considerations should be addressed as described in paragraph **2.5**.

2.9 Trace widths

The minimum (default) trace width to be used will need to be specified. This is usually based upon PCB manufacturing limitations. It is **recommended** that all signals needing traces wider than the minimum (default) be indicated on a schematic that specifies either the desired width and/or a maximum current rating. Trace width criteria is fundamentally based upon determining the acceptable temperature rise above the local board ambient. Minimizing the temperature rise *should* be a design criteria whenever possible. An acceptable temperature rise must be agreed upon at the beginning of the PCB design. A reasonable goal is less than 10°C temperature rise above the local board ambient. However, it is understood that this will not be 100% achievable. Therefore, agreed upon deviations are acceptable. It is permissible to neck down to narrower widths in tight areas.

It is **recommended** that the conductor trace width comply with IPC-2152 [**1**]. With the temperature rise defined, the required cross sectional area for the given current can be determined from the IPC-2152 [**1**] Conservative Chart or the Universal Chart. The Conservative Chart can be used as without any modifications for all PCB sizes and does not require any de-rating (safety margin). However, as its name implies it is more conservative than the Universal Chart. The Universal Chart can only be used for PCBs greater than 3 inch by 3 inch. Also, the Universal Chart requires modifications based upon design parameters – copper thickness, plane multiplier, board material, board thickness, altitude, de-rating or safety margin and other environmental factors. Using these multipliers with the Universal Chart allow the designer to adapt the IPC-2152 [**1**] trace width requirements more closely to the actual application.

In addition to sizing traces for current and temperature rise criteria, components needing heatsinking must have sufficient PCB copper area to keep their temperature rise acceptable. Component power dissipation and system thermal resistance are needed to determine the required PCB copper area. For noisy signals like the converter switch node (paragraph **2.3**), minimizing this area to limit EMI is desired. As a result, heatsink and EMI concerns could be in conflict. When this occurs, priorities must be set in order to reach an acceptable compromise.

2.10 Short paths

As mentioned in paragraph **2.4.3**, some traces must be kept as short as possible. In general, these are paths with high current and/or switched current ($\Delta i/\Delta t$). Significant attention must be given to high current and power path loops keeping them short, direct and free of vias (paragraphs **2.2** and **2.12**) and thermal relief (paragraph **2.13**). These traces *should* be identified on the schematic. Determining if the traces are short enough is a judgement call. Priorities will need to be set where conflict exists.

2.11 Ground and power planes

Ground planes *should* not be mixed with other signal or power traces and fill up the entire layer.

General guidelines

When a signal trace crosses a slot in an adjacent reference plane (power or ground), the return current must detour from directly under the trace to flow around the slot. This increases the loop area causing EMI problems. Therefore, slots *should* be avoided in all power and ground planes. If slots are unavoidable, do not route traces above the slot. Where there are overlapping holes/vias in a plane, it is preferred to reposition the holes so the plane can be routed through the holes. In plane areas around connectors, do not remove the plane fill between the connector pins (leave some copper between the holes).

The reference plane current distribution is greatly influenced by the distance the signal trace is from the reference plane. The reference plane return current spreads out beyond the width of the trace providing many parallel paths for the return current to flow. EMI problems can be avoided if reference planes extend sufficiently beyond the width of the signal trace. The design goal is to have the plane extend beyond the signal trace a distance that is at least 20 times the height of the trace above the reference plane. Because this may not be achievable in all instances, the minimum **recommended** requirement is 3 times the height of the trace above the reference plane.

Ground planes can be used to shield sensitive signals from noisy power signals. However, some areas need special attention:

1. Common Mode Inductors – **Recommend** that the grounds beneath the inductor be removed (all layers) to minimize input to output capacitive coupling. Otherwise, the effectiveness of the inductor will be compromised as a result of the increased capacitance. Avoid routing signals in this area.

2. Differential Inductors – **Recommend** that the signal connections to the inductor do not extend beyond the pads under the inductor. Little current flows in this area, but the input to output capacitance is increased compromising the inductor effectiveness. **Recommend** a shield ground under the inductor. However, in high $\Delta v/\Delta t$ areas, it may be desireable to minimize capacitive coupling to the ground plane. This can be accomplished by removing the ground on the layers directly below and add the shield ground to the ground plane furthest away from the high $\Delta v/\Delta t$ source. Avoid routing signals under the inductor.

3. Power Supply Switch Node – The switch node (paragraph **2.3**) has a differential inductor with a high $\Delta v/\Delta t$ characteristic connected to it. The discussion in 2 above applies directly to the switch node and is repeated here to signify its importance. The switch node is most likely the biggest noise source in the power supply and must be given significant attention. This includes using a ground plane for shielding, avoid routing signals under or near it, and minimizing the switch node area.

2.12 Through vias

Through vias are plated holes drilled through the PCB used to connect traces on different layers together. Blind and buried vias will not be discussed in this Application Note. Vias have resistance and must be designed correctly for reliable power supply operation. Vias will not have thermal relief (paragraph **2.13**).

2.12.1 Through via current capability

It is **recommended** that vias be sized in accordance with IPC-2152 [**1**]. Vias *should* have the same cross sectional area (X_{area}) as the trace connected to it. Where this is not possible, use multiple vias in parallel to achieve the needed cross sectional area. If connected to oversized traces or planes, first determine the current in the vias. Then, size the vias like a PCB trace as described in paragraph **2.9**.

General guidelines

$$X_{area} = \pi \cdot D \cdot T$$

D = unplated via hole diameter

T = via plated copper wall thickness

2.12.2 Through via resistance

The resistance of a through via is:

$$R_{via} = \frac{L \cdot \rho}{\pi \cdot [D^2 - (D - T)^2]} \cdot \Omega$$

L = PCB thickness

ρ = resistivity of plated copper

Via resistance will decrease as the hole diameter increases. Resistance will be minimized if multiple vias are used in parallel. Vias *should* be sized for minimal resistance and power loss.

2.12.3 Through via inductance

As the hole diameter decreases, the via's inductance increases. Vias in high frequency signal and power paths *should* be avoided. Inductance will be minimized if multiple vias are used in parallel. Vias *should* be sized for minimal inductance if must be used in high frequency signal traces.

2.12.4 Thermal vias

Power surface mount devices generally have an exposed pad for heatsinking purposes. Figure 2 shows the exposed pad for the TLS412x. This component (top) side pad is connected to an inner layer or bottom side ground plane with thermal vias to improve heat flow. Via size and quantity determine the heatsinking effectiveness. To minimize solder wicking, via drill diameter *should* be less than 13 mil with 1 ounce copper. The number of vias is dependent on the desired thermal resistance. An example of the thermal vias used on the TLS412x demoboard is shown in **Figure 17**.

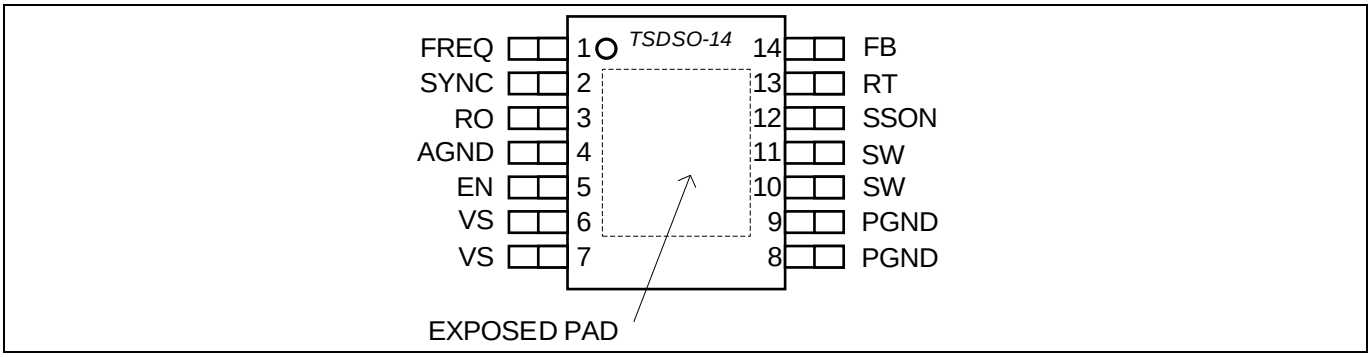

Figure 2 TLS412X Pin Configuration

2.13 Thermal relief

It is **recommended** that pads that connect to large area fills or planes have thermal relief where applicable as defined in IPC-2222 [2] to facilitate soldering. However, thermal relief creates a conflict because it affects electrical performance by increasing the circuit resistance and inductance. Thermal relief *should* be avoided for decoupling capacitors (paragraph **2.4.6**), power path components (paragraph **2.2**) and low equivalent series resistance (ESR) capacitors. No thermal relief is needed for vias (paragraph **2.12**). Where conflict occurs, priorities must be set in order to reach an acceptable compromise.

Thermal relief is used for both surface mount devices (SMD) and through hole mounted (THM) devices.

2.13.1 Through hole mounted devices

Cold solder joints may result when soldering THM component pins into large planes. Also, once soldered into these large planes unsoldering them may be difficult or impossible without damaging the PCB. Thermal relief is intended to solve these issues.

Thermal relief is sometimes described as a wagon wheel. For THM devices, the hub of the wagon wheel is the component lead barrel, the rim is the large copper area fill and the spokes are ties between them. The spokes provide the thermal relief. The spokes must be long enough, skinny enough and limited in number to provide adequate thermal relief. Therefore, it is necessary to closely control both the size of the spokes and the total number of spokes that connect between large area fills and any one barrel. This means adding up all spokes on all layers into a common barrel. Traces that do not go to large area fills do not count as spokes.

The thermal relief spokes must also reliably carry the circuit current. The resultant spokes will need to be evaluated to insure that they can carry the circuit's current without fusing or otherwise jeopardize the circuit performance. As a minimum, the sum total width of all the spokes must meet the trace width requirements of paragraph **2.9**. The maximum sum total width must be defined for solderability concerns and is dependent on the PCB copper thickness. The maximum sum total is 4mm for 35µm copper thickness and 2mm for 70µm copper thickness as defined in IPC-2222 [2].

The length of the spoke (or clearance from the pad to the plane rim) is defined in IPC-2222 [2].

2.13.2 Surface mount devices

Soldering SMDs directly onto large planes may also present problems such as misalignment, cold solder joints and/part damage. Thermal relief is intended to solve these issues.

Similar to THM devices, SMD thermal relief can be described as a wagon wheel. However, the hub is the device surface mount pad. With this distinction, the SMD thermal relief guidelines are identical to the THM devices described in paragraph **2.13.1**.

2.14 Electrical clearance

Whenever possible, the clearance (or spacing) between traces *should* be maximized. The required clearance is a function of the trace peak voltage (V_{peak}). Signal peak voltages *should* be indicated on a schematic and provided to the layout designer. It is **recommended** that the minimum spacing between the respective copper traces, pads, and planes comply with IPC-9592B [3] as summarized in Table 1. Electrical clearance across high voltage safety isolation boundaries are not considered in these guidelines or this Application Note.

General guidelines

Table 1 IPC-9592B Conductor Trace Clearance

Minimum Spacing (mm)	Voltage Range
0.13	$V_{peak} < 15 \cdot volt$
0.25	$15 \cdot volt \leq V_{peak} < 30 \cdot volt$
$0.1 + (V_{peak} \cdot 0.01)$	$30 \cdot volt \leq V_{peak} < 100 \cdot volt$
$0.6 + (V_{peak} \cdot 0.005)$	$V_{peak} \geq 100 \cdot volt$

3 TLS412x datasheet application schematic

3.1 Application schematic for fixed output devices

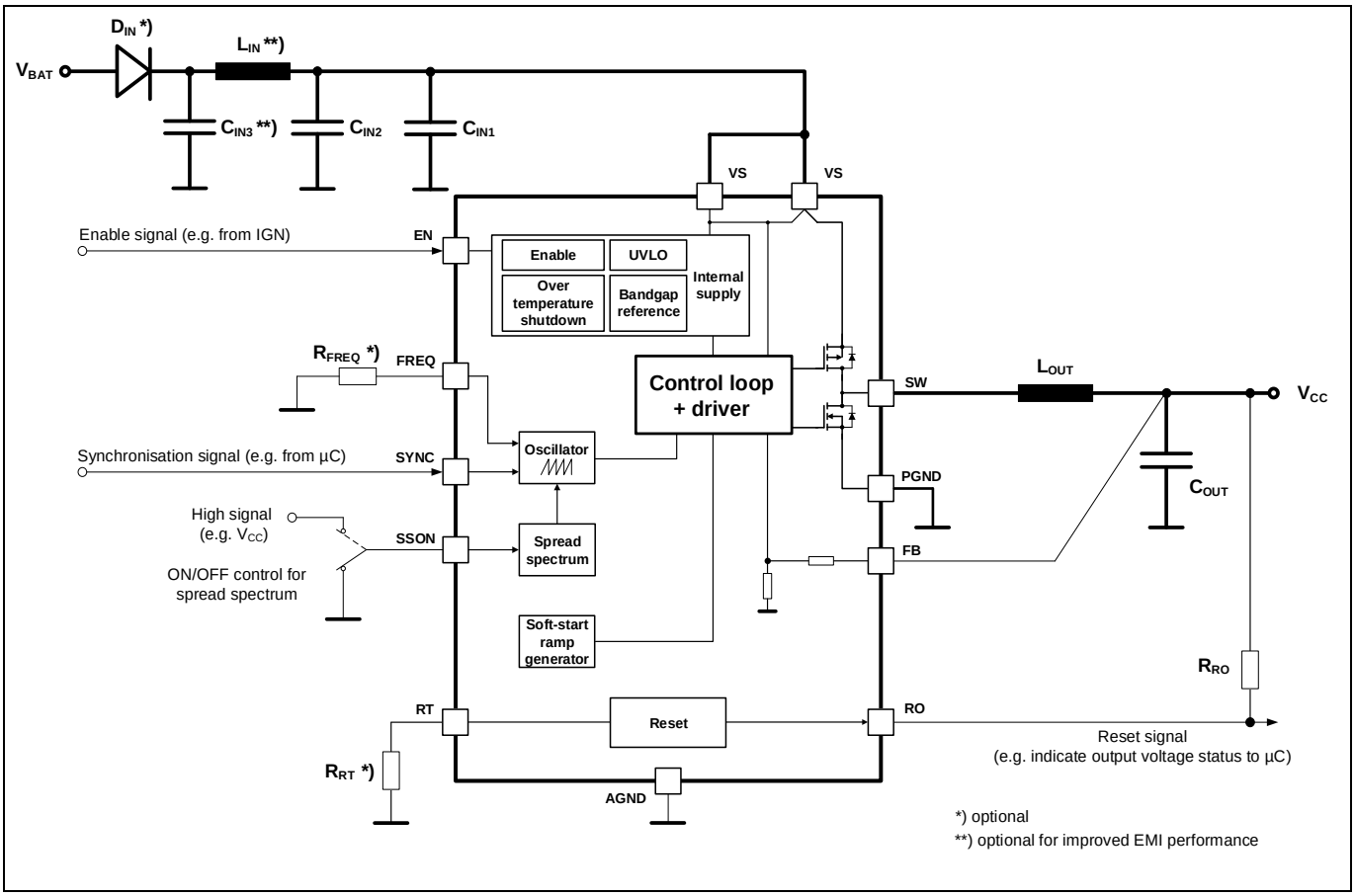

Figure 3 Application Schematic for Fixed Output Devices

3.2 Application schematic for adjustable devices

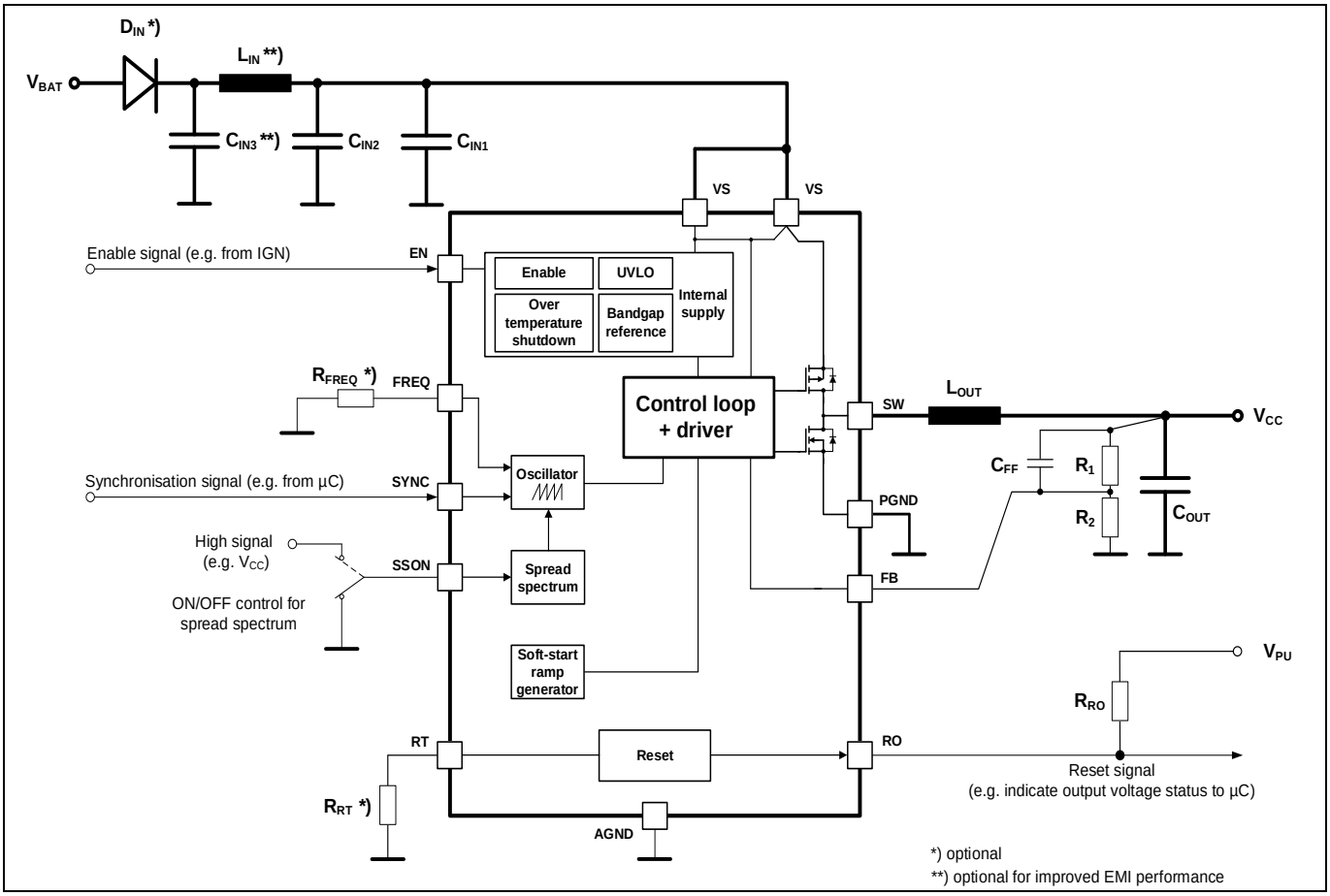

Figure 4 Application Schematic for Adjustable Devices

4 TLS412x layout guidelines

The TLS412x is a synchronous buck converter with integrated power switches. It is available in multiple variants with six different part numbers as shown in Table 2.

Application schematics are shown in **Figure 3** and **Figure 4**.

The TLS412x layout guidelines are presented in the form of an actual PCB layout. The TLS412x demoboard is used as the layout example.

Table 2 TLS412x Part Numbers

Part Number	Output Current	Output Voltage
TLS4120D0EPV33	2 A	3.3 V
TLS4120D0EPV50	2 A	5 V
TLS4120D0EPV	2 A	Adjustable
TLS4125D0EPV33	2.5 A	3.3 V
TLS4125D0EPV50	2.5 A	5 V
TLS4125D0EPV	2.5 A	Adjustable

4.1 TLS412x demoboard example

4.1.1 Demoboard description

A description of the demoboard can be found in the Infineon application note Z8F68163134, OPTIREG™ switcher TLS412xD0EPVxx demoboard [4].

4.1.2 Demoboard schematic

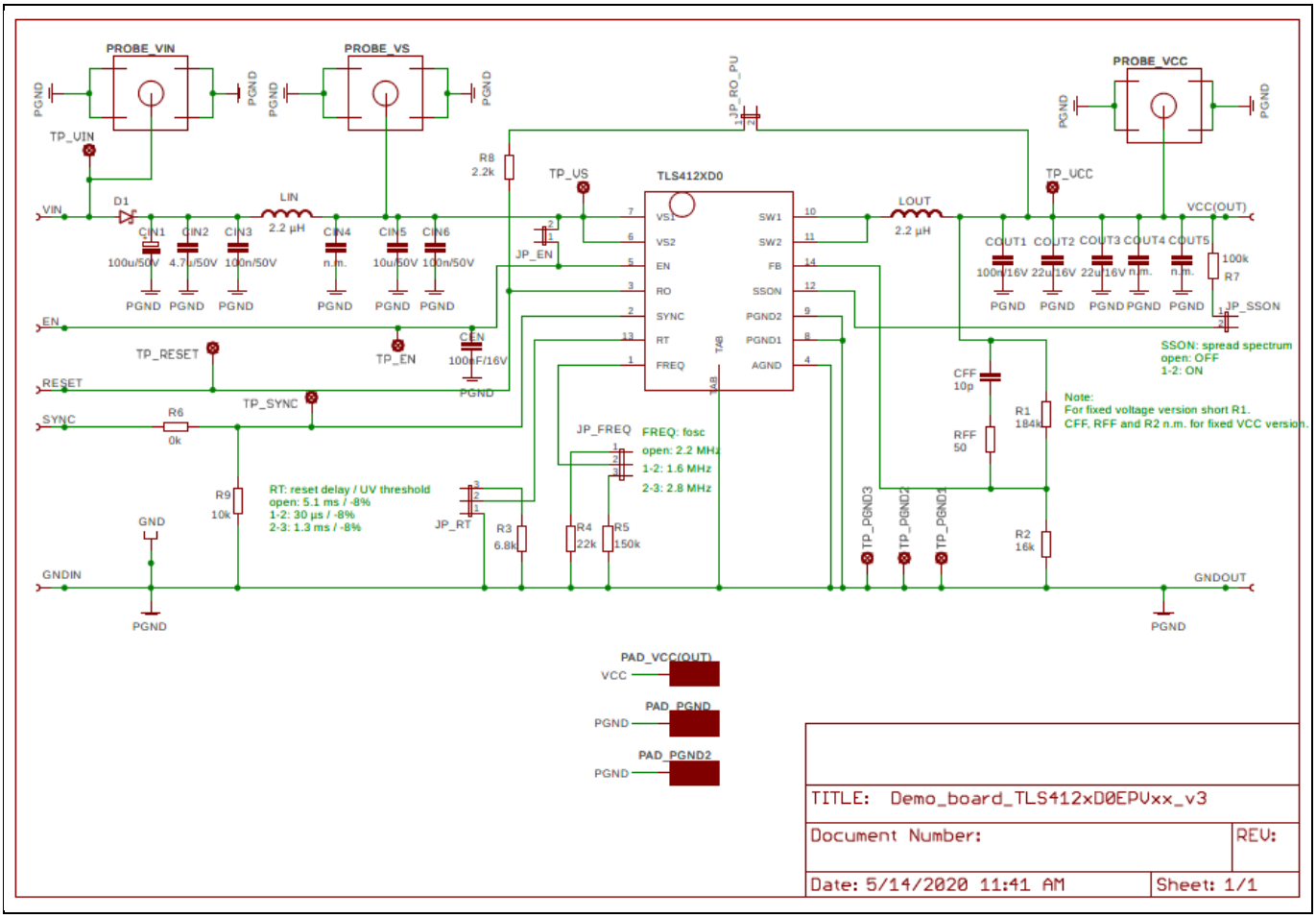

Figure 5 Demoboard Schematic

4.1.3 Demoboard PCB layer definition

The demoboard PCB has four layers. All layers have 70µm copper thickness. The PCB size is 100mm x 72mm (3.94 inch x 2.83 inch).

- Top (Layer 1) – All components are placed on the top layer minimizing the need for vias. The top layer has nearly all of the signal and power traces. A ground pour area fill is used to fill in the unused open areas to improve circuit integrity and EMI. The component placement and routing is shown in Figure 6.

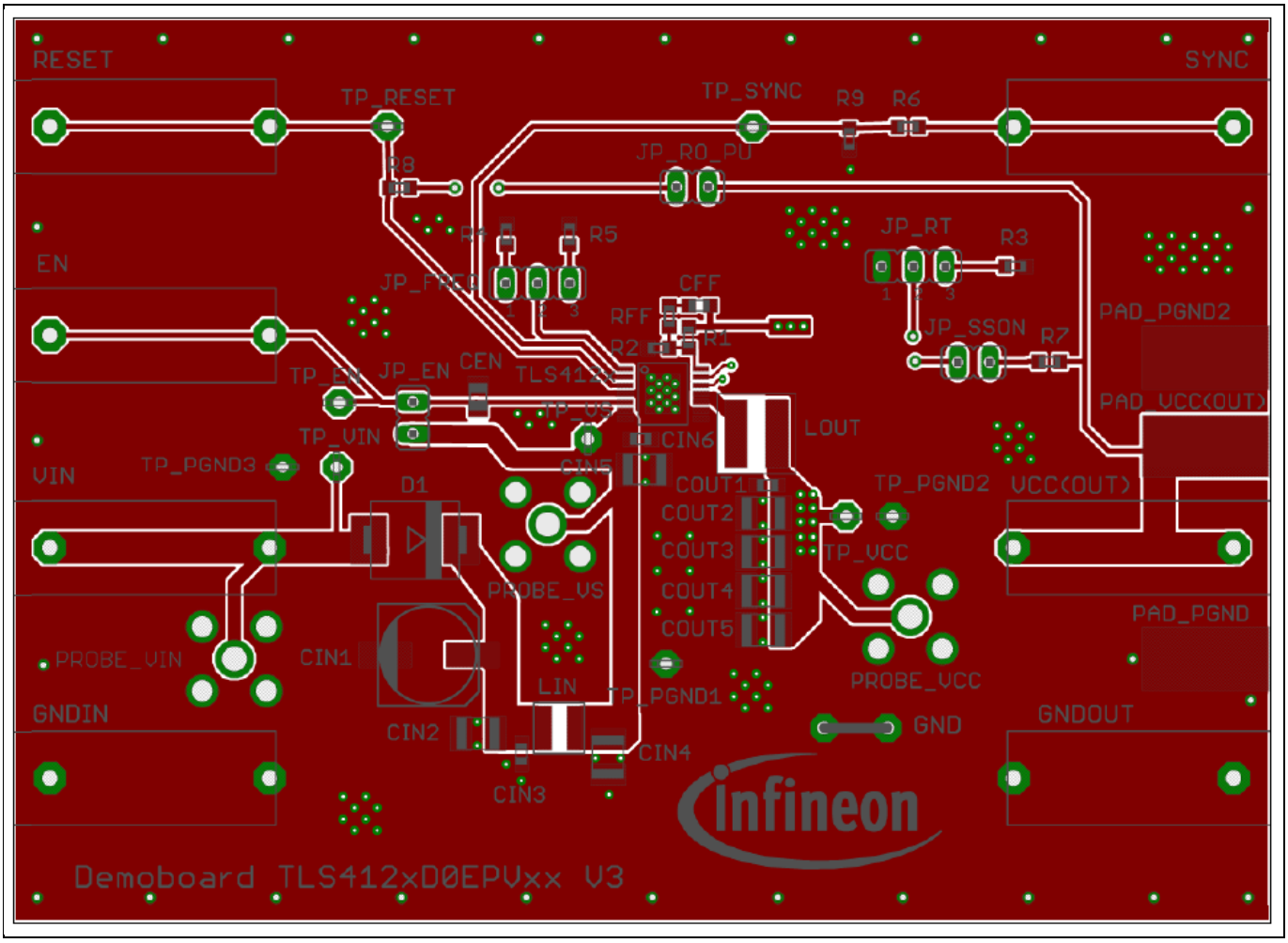

Figure 6 Top (Layer 1)

- Inner Layer 2 – Layer 2 is primarily a ground plane with three PCB signal connections as shown in Figure 7.

  The ground under LIN and the switch node have been removed as described in paragraph **2.11**.

  Two sensitive signal traces (RT and SSON as shown on the Figure 8 schematic) are included on layer 2 to shield them from the switch node noise on layer 1. There are ground planes above and below these signals on layers 1 and 3 which providing shielding.

  The load connection from the output capacitors on layer 1 to the VCC (OUT) connector is included on layer 2. This connection could have been done on layer 1, but this would have compromised the continuous layer 1 ground pour. Also, on layer 2 it has ground above and below it on layers 1 and 3 which provides for some EMI shielding. This is discussed further in paragraph **4.1.4.1**.

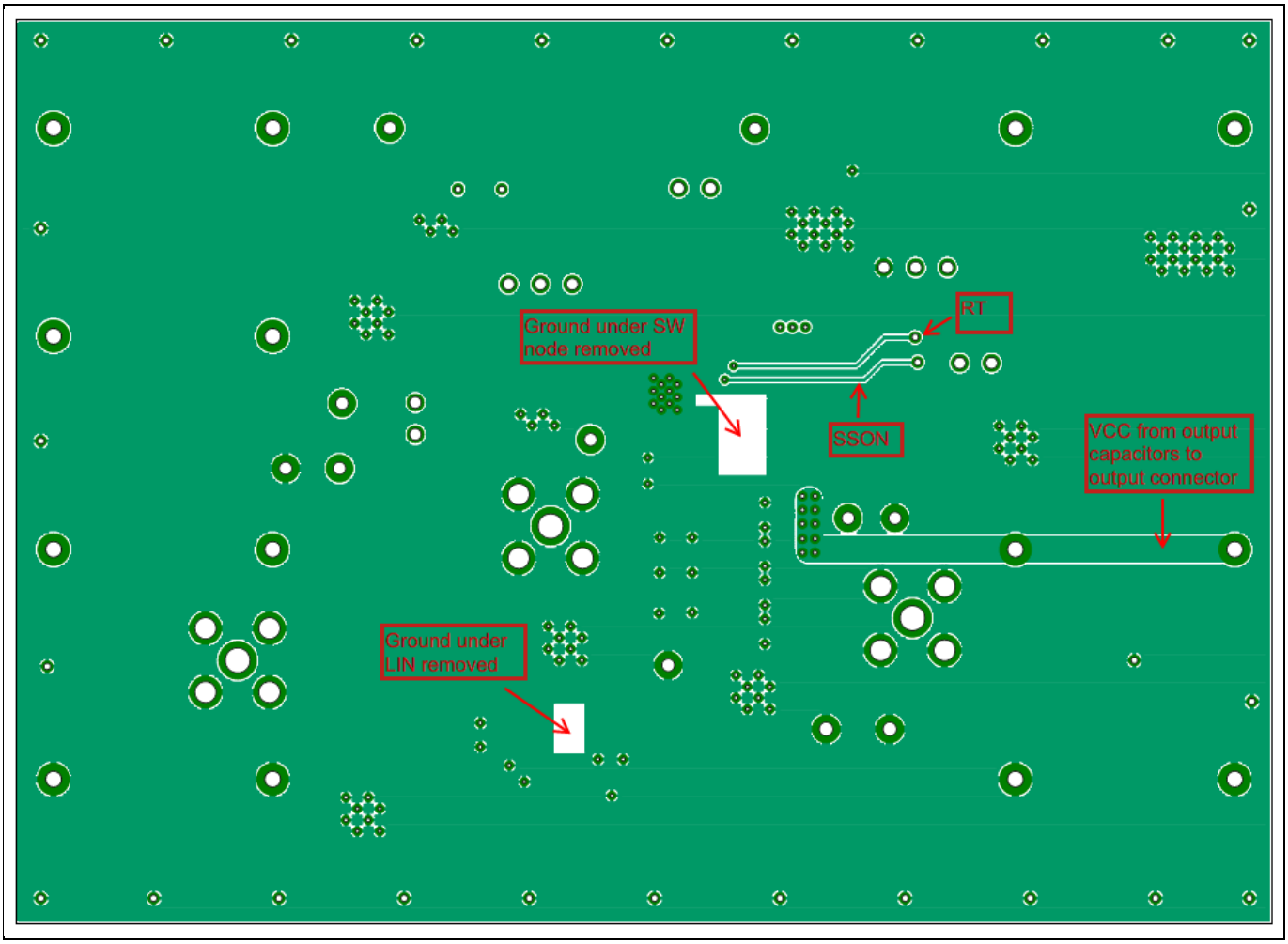

Figure 7 Layer 2

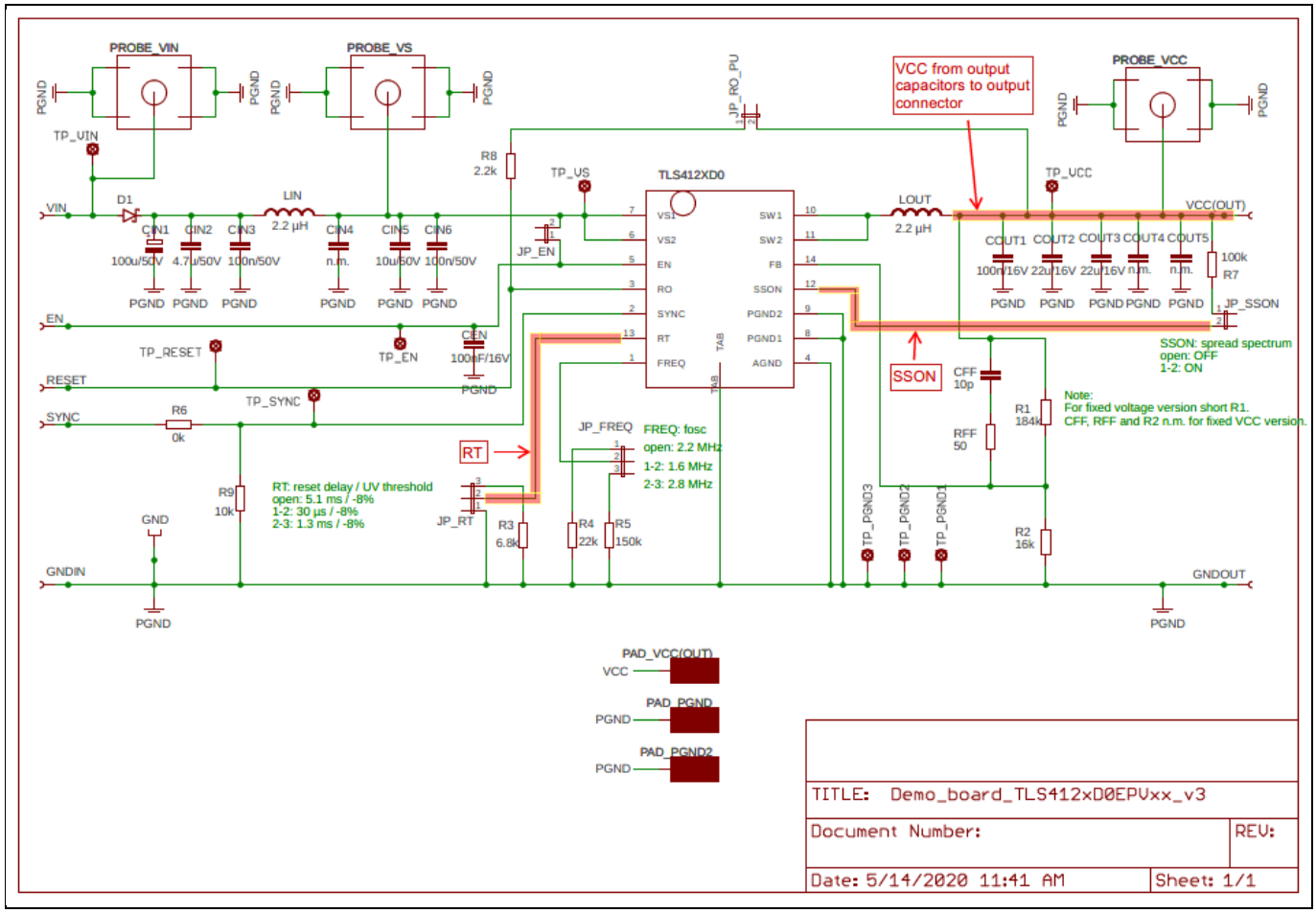

Figure 8 RT, SSON and VCC Signals on Layer 2

- Inner Layer 3 – Layer 3 is primarily a ground plane as shown in Figure 9.

  The ground under LIN and the switch node have been removed as described in paragraph **2.11**.

  A signal trace has also been included on layer 3. This the VCC output voltage signal used in the regulation feedback loop (see Figure 10 schematic). This is a sensitive signal and if corrupted by noise it would disrupt the output VCC regulation function. Including it on layer 3 provides some shielding from the switch node noise on layer 1. There are ground planes above and below it on layers 3 and 4 which provides an effective shield for this sensitive trace.

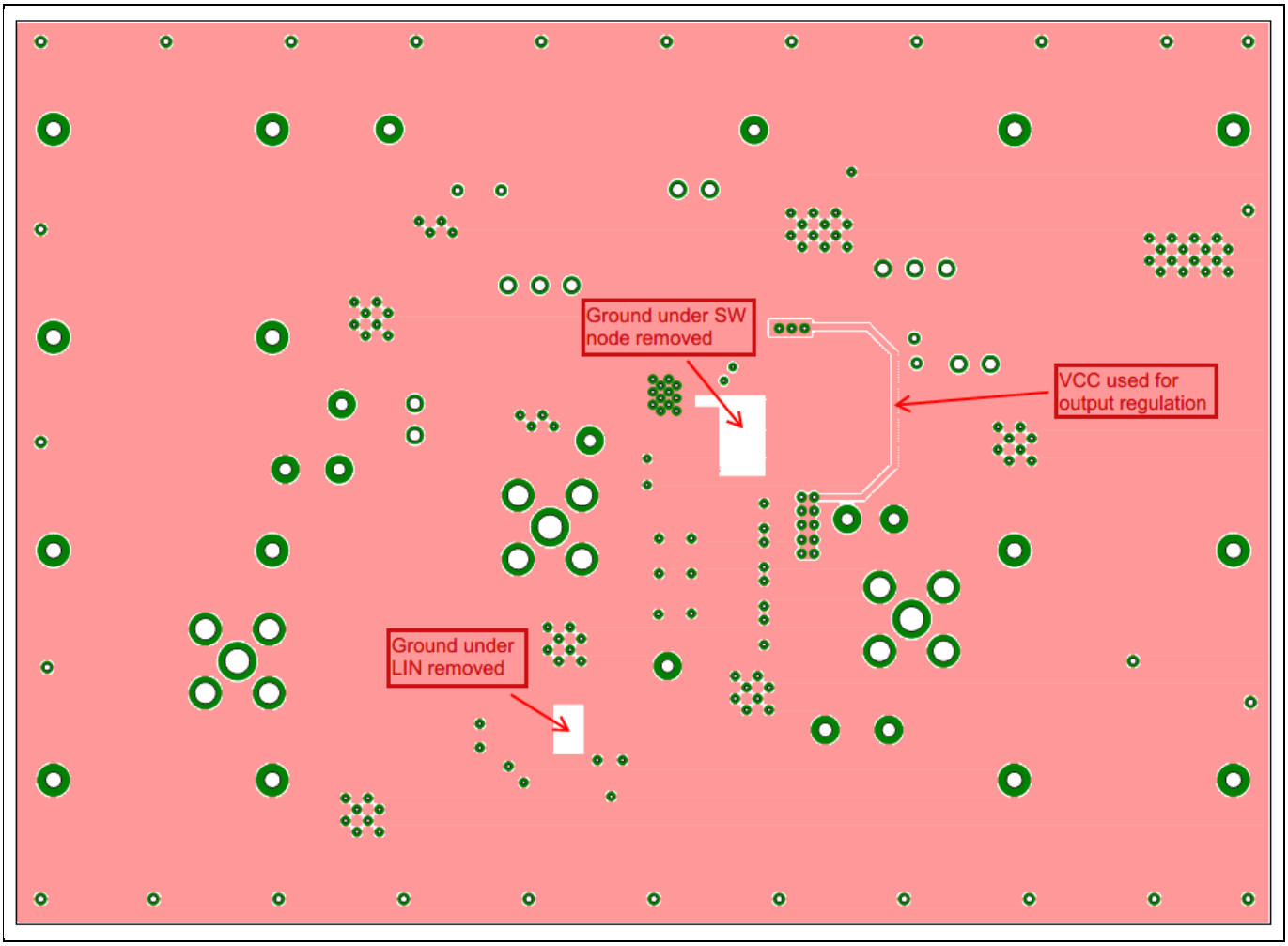

Figure 9 Layer 3

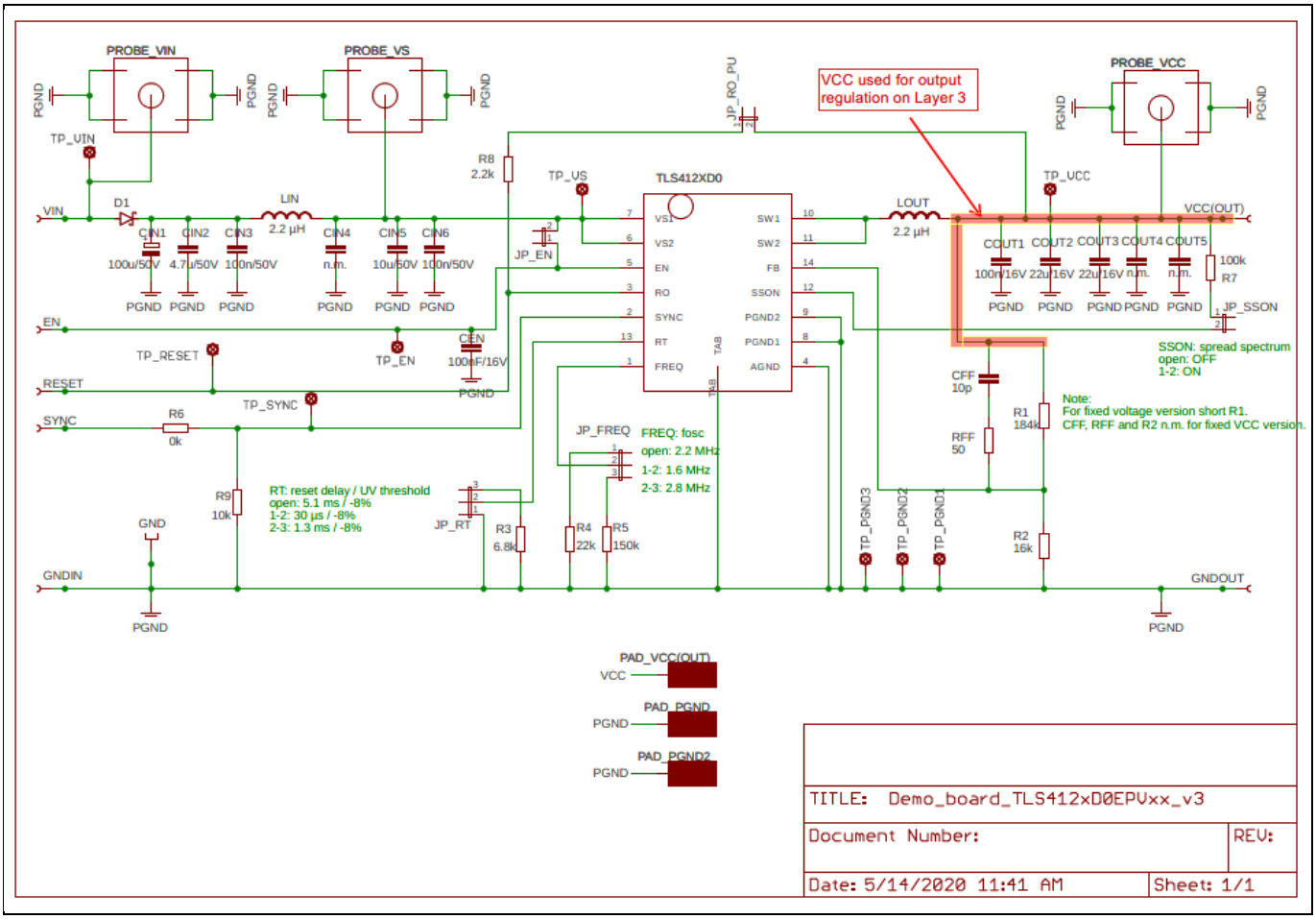

Figure 10 VCC Regulation Signal on Layer 3

- Bottom Layer 4) – The bottom layer is a ground plan with no PCB circuit traces as shown in Figure 11. The ground plane extends completely beneath LIN and the switch node for shielding (paragraph **2.11**)

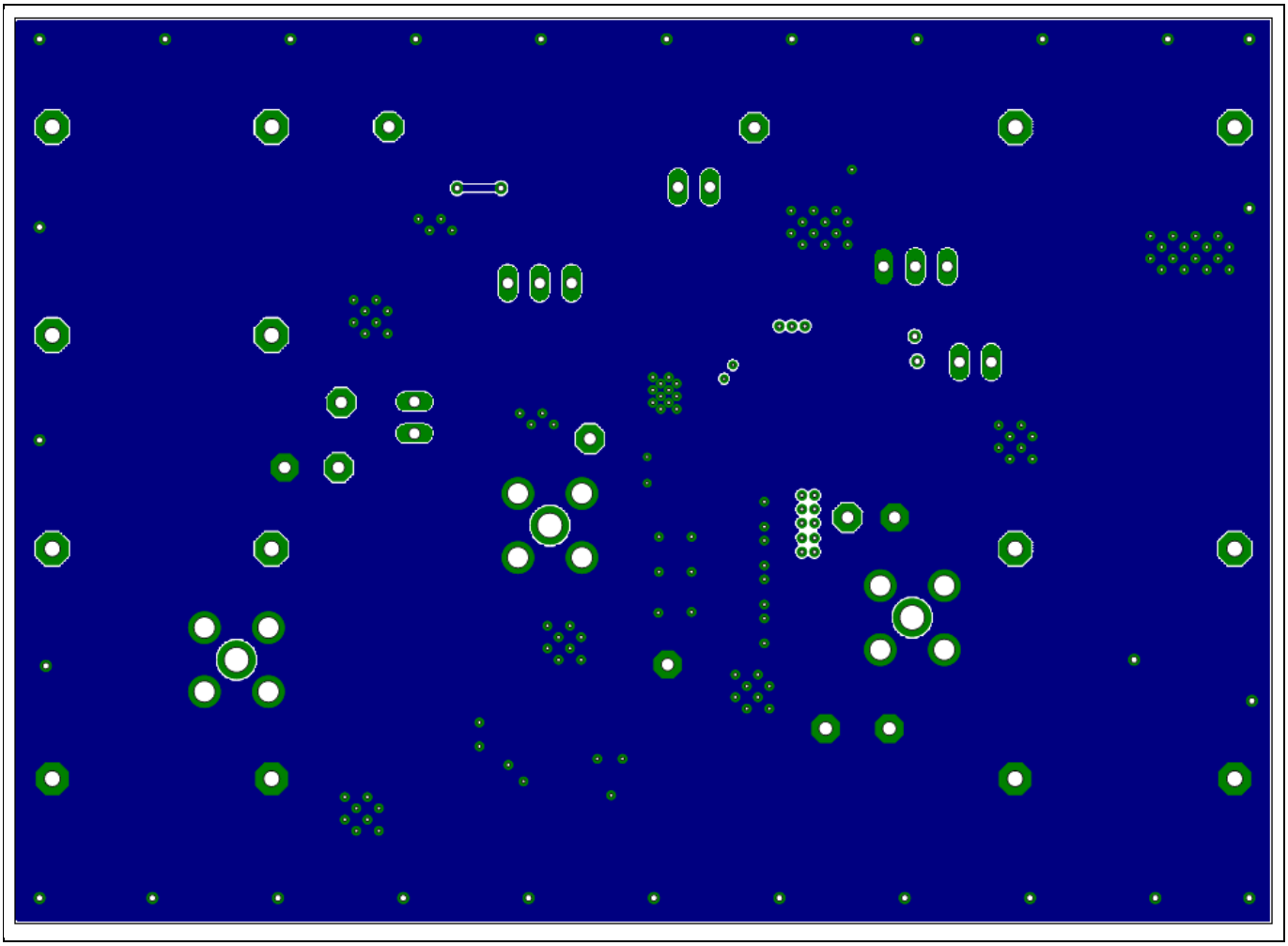

Figure 11 Bottom (Layer 4)

4.1.4 Demoboard power path loops

The demoboard power path loops (see paragraph **2.2** for a description of power path loops) are shown in Figure 12.

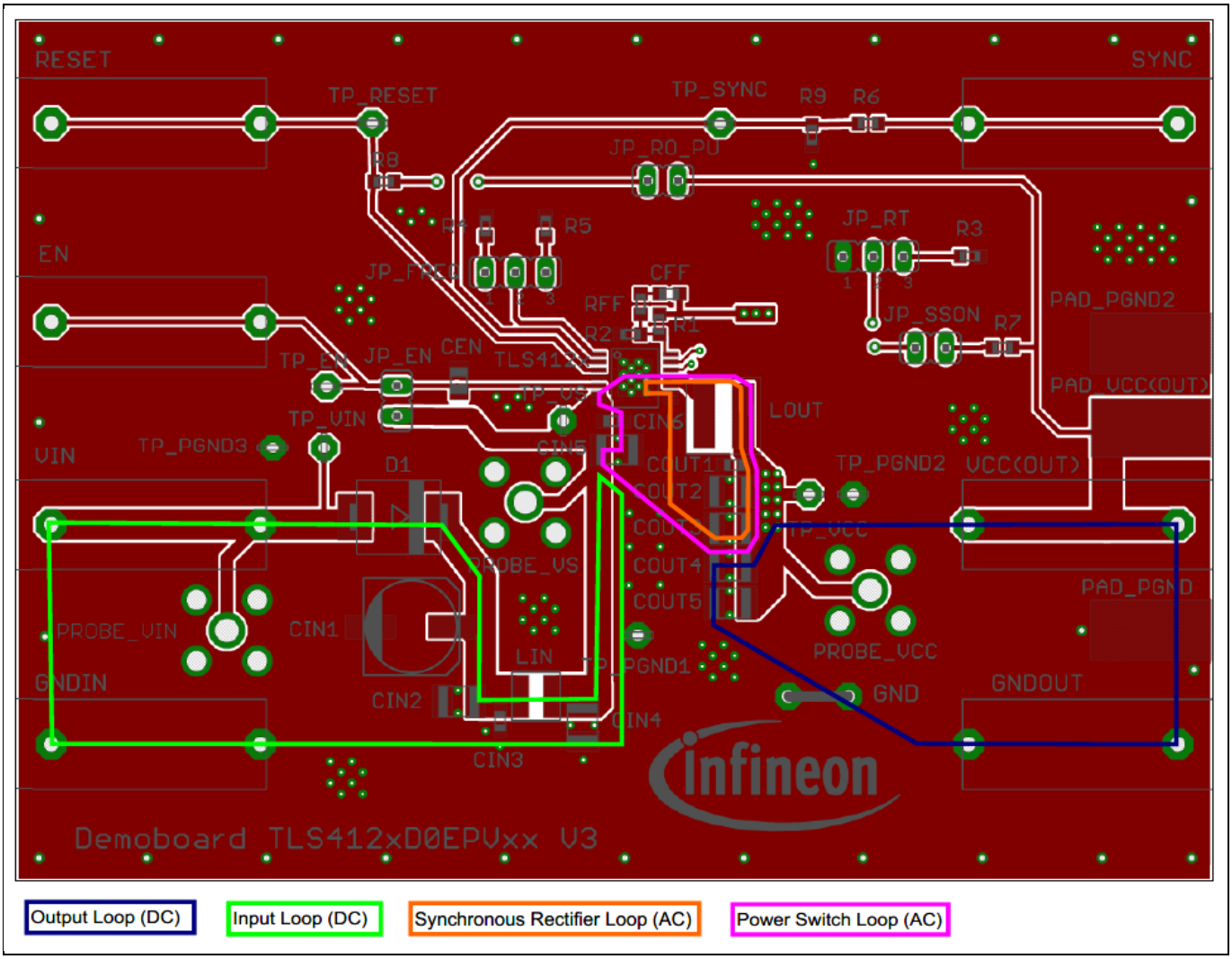

Figure 12 TLS412x Demoboard Power Path Loops

4.1.4.1 Demoboard output loop

The output loop is also relatively small and compact which minimize losses and improve efficiency as shown in Figure 12. The top layer ground area fill and ground planes on layers 2- 4 efficiently carry the DC output loop return current.

The output loop is also free of thermal relief, but does use vias to connect the output capacitors to the VCC (OUT) connector (Figure 13). This was a compromise of a non-critical provision that is inevitable in any PCB design.

As described paragraph **2.13**, thermal relief is not needed for vias. However, as shown in Figure 13 some vias have thermal relief. In order to facilitate rework and soldering components connected to ground, thermal relief was added to vias which did not affect noise and/or thermal performance. For production applications, this normally would not be necessary or advised.

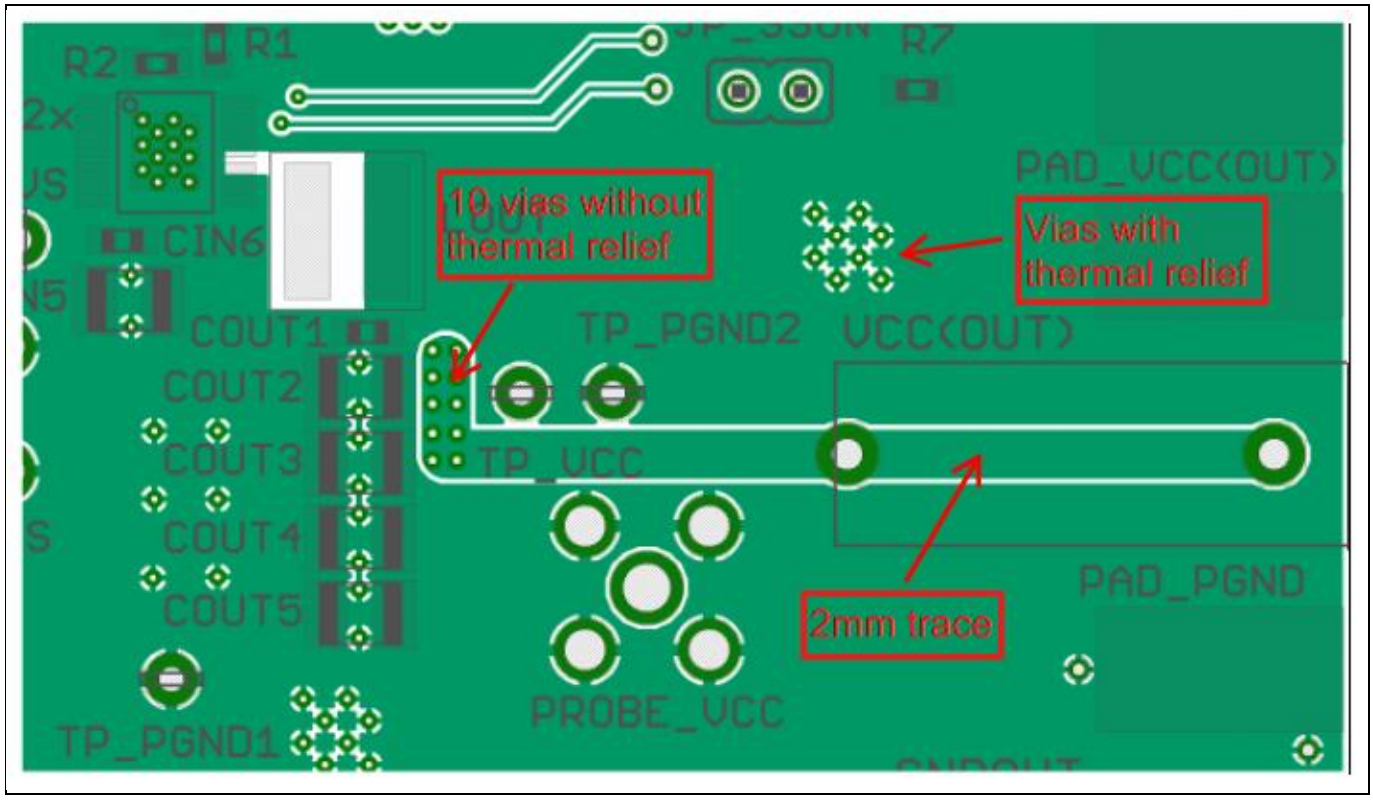

Figure 13 Second Layer VCC (OUT) Connection

There are ten 0.35mm diameter vias connecting the output capacitors on the top layer to the two VCC (OUT) connector pins using a 2mm wide trace (Figure 13).

- The equivalent resistance (R_{via_equiv}) of the ten paralleled vias (paragraph **2.12.2**) is:

  $T = 70 \cdot \mu m$ PCB copper thickness

  $L = 1.71 \cdot mm$ PCB thickness

  $\rho = 1.72 \cdot \mu\Omega \cdot cm$ Resistivity of copper at 20°C

  $D = 0.35 \cdot mm$ Unplated via hole diameter

  $N_{via} = 10$ Total number of vias

  $$R_{via\_equiv} = \frac{L \cdot \rho}{N_{via} \cdot \pi \cdot [D^2 - (D - T)^2]} \cdot \Omega = \frac{1.71 \cdot 10^{-3} \cdot m \cdot 1.72 \cdot 10^{-8} \cdot \Omega \cdot m}{10 \cdot \pi \cdot [(0.35 \cdot 10^{-3} \cdot m)^2 - (0.35 \cdot 10^{-3} \cdot m - 70 \cdot 10^{-6} \cdot m)^2]}$$

  $R_{via\_equiv} = 21.23 \cdot \mu\Omega$

- The worst case equivalent via voltage drop and power dissipation is with maximum load (2.5A):

  $V_{drop\_vias} = 21.23 \cdot \mu\Omega \cdot 2.5 \cdot A = 53.08 \cdot \mu V$

  $P_{loss\_vias} = (2.5 \cdot A)^2 \cdot 21.23 \cdot \mu\Omega = 136.69 \cdot \mu W$

The voltage drop is insignificant and does not adversely affect the regulation loop. Also, the power dissipation is very low and does not affect the PCB temperature.

- The equivalent conductor cross sectional area of the ten paralleled vias (paragraph **2.12.1**) is:

$$X_{area\_via\_equiv} = N_{via} \cdot \pi \cdot D \cdot T = 10 \cdot \pi \cdot 0.35 \cdot 10^{-3} \cdot m \cdot 70 \cdot 10^{-6} \cdot m = 769.7 \cdot 10^{-9} \cdot m^2$$

Because the IPC-2152 [**1**] conductor cross sectional area requirements are in square mils (mil^2), so we need to convert square meters (m^2) to square mils:

$$1 \cdot m^2 = 1.55 \cdot 10^9 \cdot mil^2$$

$$X_{area\_via\_equiv} = 769.7 \cdot 10^{-9} \cdot m^2 \cdot \frac{1.55 \cdot 10^9 \cdot mil^2}{1 \cdot m^2} = 1193 \cdot mil^2$$

- The current carrying capability of the ten paralleled vias is described in paragraph **2.12.1**. Using the Conservative Chart in IPC-2152 [**1**], the required conductor cross sectional area for a 10°C temperature rise at 2.5A is 160 mil^2. The demoboard has nearly 7.5x that amount. This means that the actual temperature rise due to current flowing through the vias is much less than 10°C. The number and size of the vias is more than sufficient for this application.

- The current carrying capability of the second layer trace connecting output capacitor vias to the VCC (OUT) connector is dependent on the cross sectional area of the conductor (paragraph **2.9**). The width of the trace is 2mm.

$W = 2 \cdot mm$ Width of the VCC trace connecting the output caps to the VCC (OUT) connector

$$X_{area\_trace} = W \cdot T = 2 \cdot 10^{-3} \cdot m \cdot 70 \cdot 10^{-6} \cdot m \cdot \frac{1.55 \cdot 10^9 \cdot mil^2}{1 \cdot m^2} = 217.0 \cdot mil^2$$

- As described above the required cross sectional area for a 10°C temperature rise at 2.5A is 160 mil^2. The demoboard has nearly 2x that amount. This means that the actual temperature rise due to current flowing through the trace connecting the VCC output caps to the VCC (OUT) connector is less than 10°C. The trace width is more than sufficient for this application.

- The remainder of the connections of the DC output loop is done with plane or traces larger than 2mm. Therefore, conductor trace widths in the DC output loop is more than sufficient for the application.

4.1.4.2 Demoboard input loop

The input loop is relatively small and compact which minimize losses and improve efficiency as shown in **Figure 12.** The input loop is free of vias and thermal relief. The top layer ground area fill and ground planes on layers 2- 4 efficiently carry the DC input loop return current.

There are 2.54mm and 2mm traces used in the input DC loop as shown in Figure 14. The current carrying capability is function of the conductor cross sectional area (paragraph **2.9**).

- Current carrying capability of the 2.5mm traces:

$$X_{area\_2.5mm\_trace} = W \cdot T = 2.54 \cdot 10^{-3} \cdot m \cdot 70 \cdot 10^{-6} \cdot m \cdot \frac{1.55 \cdot 10^9 \cdot mil^2}{1 \cdot m^2} = 275.6 \cdot mil^2$$

TLS412x layout guidelines

Using the Conservative Chart in IPC-2152 [1], a conductor with a cross sectional area of 275 mil^2 will experience a 10°C temperature rise at approximately 3.75A.

The maximum input current for the TLS4125D0EPV50 will be at the minimum functional input voltage of 6V. Conservatively assuming an efficiency (η) of 85%, the current (I_{in}) in this race is:

$$I_{in} = \frac{V_{cc} \cdot I_{cc}}{\eta \cdot V_{in}} = \frac{5 \cdot V \cdot 2.5 \cdot A}{0.85 \cdot 6 \cdot V} = 2.45 \cdot A$$

The input DC loop traces are capable of approximately 1.5x the worst case application input current. The actual trace temperature rise will be less than 10°C. The trace width is more than sufficient for this application.

- Current carrying capability of the 2mm trace:

In paragraph **4.1.4.1**, a 2mm trace was shown to have a cross sectional area of 217 mil^2. Using the Conservative Chart in IPC-2152 [1], a conductor with a cross sectional area of 200 mil^2 will experience a 10°C temperature rise at 3A. Therefore, the trace width is more than sufficient for this application.

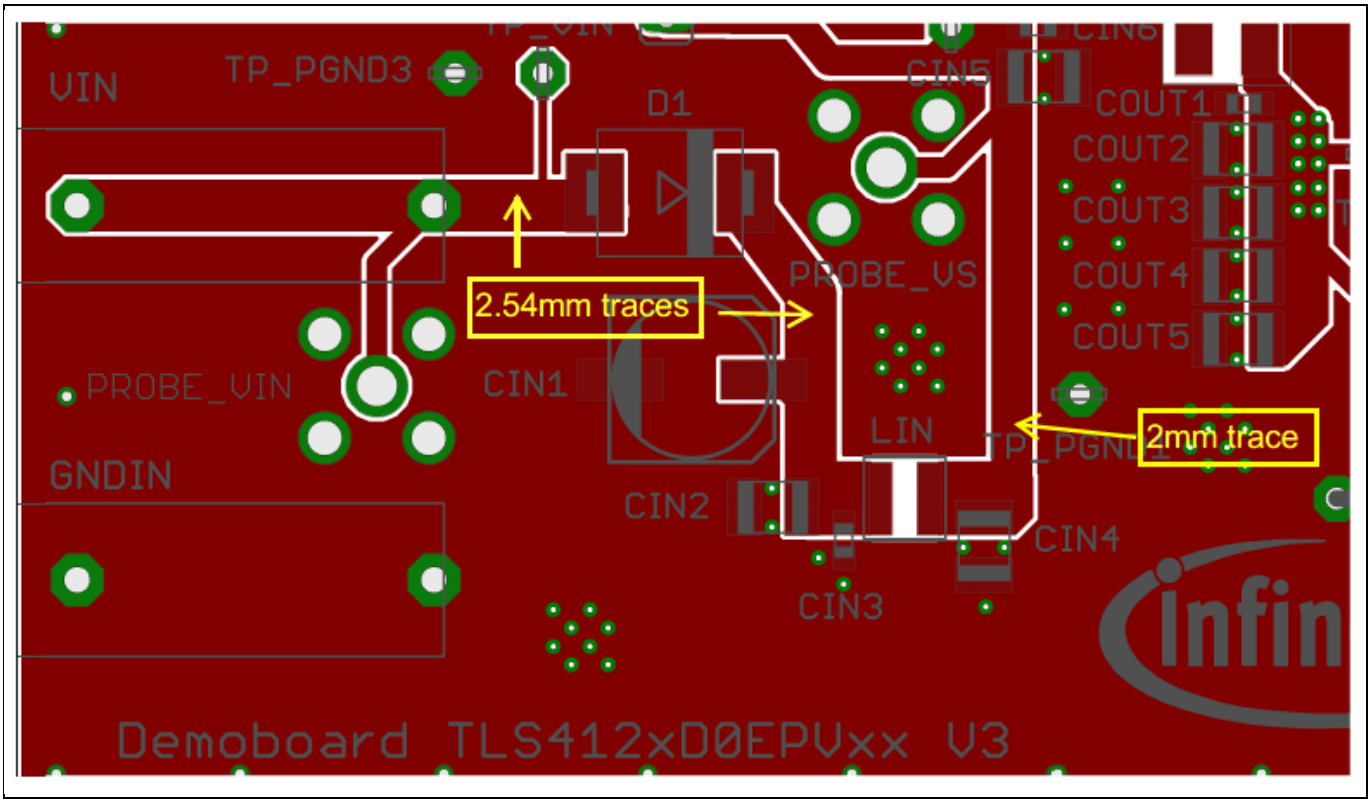

Figure 14 Top Layer Input loop Traces

4.1.4.3 Demoboard synchronous rectifier loop

The synchronous rectifier loop is also relatively small and compact which minimize losses and improve efficiency as shown in **Figure 12**. Placing the output capacitors (COUT1 – COUT5) ground pads close to the TLS412x PGND (pins 8 and 9) helps reduce the loop area. The top layer ground area fill and ground planes on layers 2- 4 efficiently carry the synchronous rectifier loop return current. The synchronous rectifier loop is also free of thermal relief and vias.

4.1.4.4 Demoboard power switch loop

The power switch loop is also relatively small and compact which minimize losses and improve efficiency as shown in **Figure 12**. Placing the output capacitors (COUT1 – COUT5) ground pads close to the input capacitors (CIN5 and CIN6) ground pads helps reduce this area. The top layer ground area fill and ground planes on layers 2- 4 efficiently carry the power switch loop return current. The power switch loop is also free of thermal relief and vias.

4.1.5 Demoboard switch node

The demoboard switch node is shown in the highlighted area of Figure 15. It is probably not realistic to make it any smaller as the majority of the area is occupied by the LOUT inductor pad. The trace connecting TLS412x SW pins 10 and 11 to the inductors is very small (approximately 1.60mm). As discussed in paragraph **2.3**, ground directly below the switch node on layers 2 and 3 has been removed to minimize capacitive coupling. A ground on the bottom (layer 4) is providing shielding. Also, there are no traces routed under the switch node.

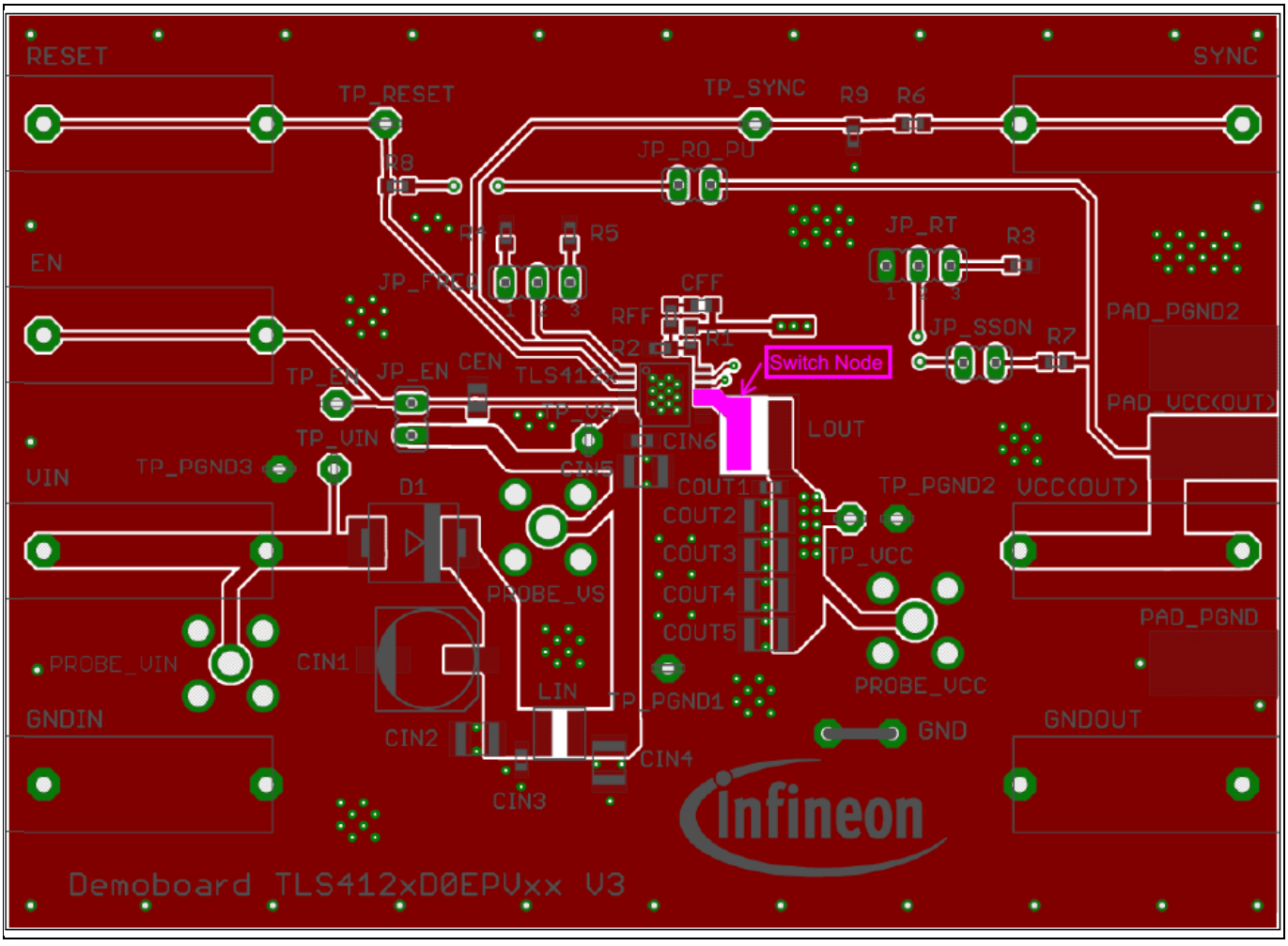

Figure 15 Switch Node

4.1.6 Demoboard sensitive feedback circuit

The power supply feedback circuit is a very sensitive signal as described in paragraph **2.4.4.1**. The demoboard feedback circuit includes CFF, RFF, R1 and R2 as shown in **Figure 5**.

Careful attention to the placement and routing of the feedback circuit is needed and is shown in Figure 16 for the demoboard. The guidelines to minimize radiated noise pickup onto the feedback circuit are:

- Place the feedback circuit parts close to the FB pin of the TLS412x (pin 14) and away from the switch node and buck inductor (LOUT).
- Place resistor R2 close to the FB pin and orient it so that its ground pad is close as possible to the AGND pin of the TLS412x (pin 4).
- Reduced the area of the parts connected to the FB pin as much as possible by keeping all connections short and direct. Using small footprint components also helps reduce this area.
- Position the trace from the FB pin to R1 and R2 at the left side of the pad furthest away from the buck inductor (LOUT).
- Orient the switch node area and LOUT so they are as far away as possible from the FB pin.
- As discussed in paragraph **4.1.3**, the layer 3 connection from the output (VCC) was shielded between ground planes.

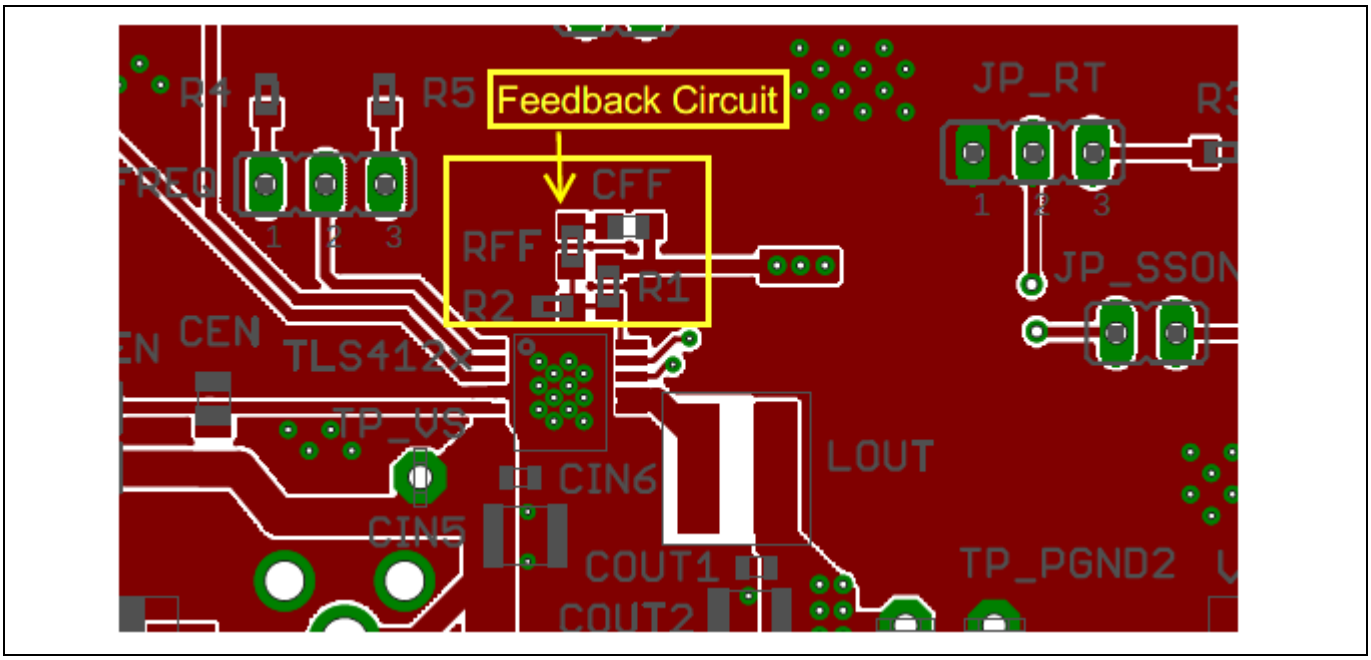

Figure 16 Feedback Circuit

4.1.7 Demoboard input decoupling capacitors

Input voltage decoupling capacitors are required on the VS pin of the TLS412x (pins 6 and 7). The demoboard decoupling capacitors are CIN4, CIN5 and CIN6 are shown in schematic **Figure 5**. The decoupling capacitor placement and routing is shown in **Figure 6**. The input decoupling capacitors were based on the low frequency requirements of paragraph **2.4.6.2**.

CIN4 is provisional and can be used for EMI filtering if needed.

CIN6 is a small 100nF ceramic capacitor and is placed closest to the VS input (pins 6 and 7) of the TLS412x. CIN5 is a larger 10uF ceramic capacitor and placed directly below and in parallel to CIN5. The positive pads of both capacitors are connected to the VS input copper trace without vias. The ground pads are connected to the layer 1 ground pour area fill that also connects directly to PGND (pins 8 and 9) of the TLS412x without vias. The CIN5 ground pad is also connected with two vias to the ground planes on layers 2 – 4. This helps to lower the overall ground impedance.

4.1.8 TLS412x power pad thermal vias

As described in paragraph **2.12.4**, the power pad of the TLS412x can be connected to a ground plane with thermal vias for heatsinking. The demoboard uses 12 vias with a diameter of 0.3mm (11.8 mils) to connect the power pad to the ground planes on all four layers as shown in Figure 17. This a suggestion only. The number of the thermal vias is application specific. Customer manufacturing and producability requirements may also dictate thermal via implementation. Each application must be evaluated at specific board and ambient temperatures, TLS412x power losses and actual PCB thermal resistance to insure desired the performance.

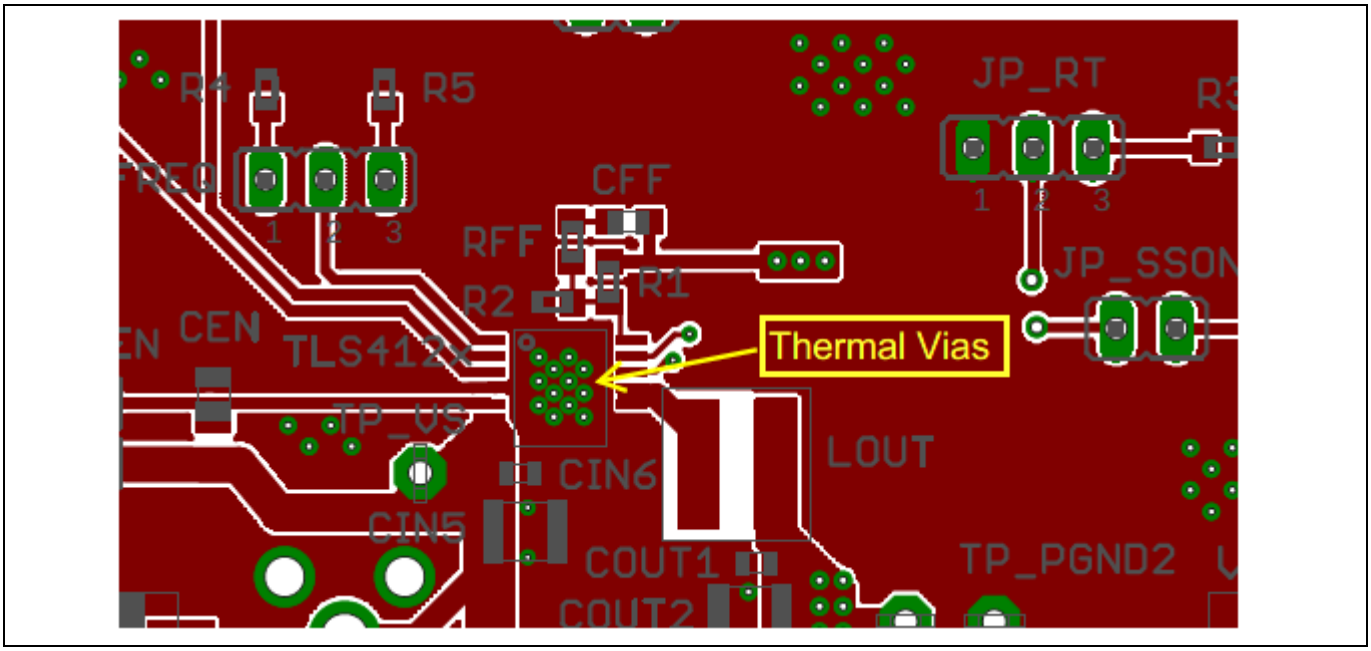

Figure 17 Thermal Vias

4.1.9 Demoboard electrical clearance

The TLS412x VS input voltage functional range is 3.7V to 35V. A PCB design compromise was to consider input voltages greater than 30V to be transient in nature and only define electrical clearance requirements for voltages less than 30V. Therefore, at 30V the electrical clearance requirement as described in paragraph **2.14** is 0.25mm. This is the clearance between conductor traces and ground on the demoboard. However, each application is different and requires evaluation in order to determine the needed PCB electrical clearance.

5 TLS412x layout and routing summary

For a successful TLS412x layout, these are the most significant guidelines to follow:

1. Minimize the synchronous rectifier loop area. Placing the output capacitors (COUT1 – COUT5) ground pads close to the TLS412x PGND (pins 8 and 9) helps reduce the loop area. Use ground planes and/or ground fill areas to efficiently carry the current.
2. Minimize the power switch loop area. Placing the output capacitors (COUT1 – COUT5) ground pads close to the input capacitors (CIN5 and CIN6) ground pads helps reduce this area. Use ground planes and/or ground fill areas to efficiently carry the current.
3. Minimize the switch node area by placing the buck inductor (LOUT) as close as possible to the TLS412x SW pins 10 and 11. If possible, try to make the rest of the switch node no larger than the inductor pad. Have a ground plane under the switch node for shielding only on the last layer (furthest away). Do not route any signals under the switch node.
4. Feedback circuit
   - Place the feedback circuit parts close to the FB pin of the TLS412x (pin 14) and away from the switch node and buck inductor (LOUT).
   - Place resistor R2 close to the FB pin and orient it so that its ground pad is close as possible to the AGND pin of the TLS412x (pin 4).
   - Reduced the area of the parts connected to the FB pin as much as possible by keeping all connections short and direct. Using small footprint components also helps reduce this area.
   - Position the trace from the FB pin to R1 and R2 at the left side of the pad furthest away from the buck inductor (LOUT).
   - Orient the switch node area and LOUT so they are as far away as possible from the FB pin.
   - If possible, shield the output (VCC) trace to the feedback circuit between ground planes.
5. Place the input decoupling capacitors (CIN5 and CIN6) as close as possible to the VS pins of the TLS412x (pins 6 and 7). Orient the capacitors so their ground pads are close to the TLS412x PGND (pins 8 and 9) and the output capacitors (COUT1 – COUT5) ground pads.
6. Insure that a ground plane is directly adjacent to every signal trace. Avoid gaps and slots in the planes.
7. Size conductors and vias for acceptable temperature rise.
8. Insure conductor spacing is appropriate for the expected voltage.

6 References

[1] IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design

[2] IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

[3] IPC-9592B Requirements for Power Conversion Devices for the Computer and Telecommunications Industries

[4] Infineon application note Z8F68163134 OPTIREG™ switcher TLS412xD0EPVxx demoboard

[5] Ott, Henry W. (2000). *Electromagnetic Compatibility Engineering*. John Wiley & Sons, Inc.

Revision history

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