Infineon

Thermal behavior of PROFET™+2 12V in PG-TSDSO-14 package

About this document

Scope and purpose

This document shows how to design an optimal printed circuit board (PCB) using PROFET™+2 12V family in PG-TSDSO-14 package.

Intended audience

Engineers, hobbyists and students who want to add powerful protected high-side switches for heating or power distribution projects.

Table of contents

1   Introduction

This chapter will provide a brief introduction to the PROFET™ (protected FET)+2 12V family.

1.1   PROFET™+2 12V overview

The PROFET™ +2 12V family was developed to replace relays, fuses and discrete circuits. Due to a selection of protection and diagnostic features in combination with a very low ohmic DMOS this family is particularly suitable for applications such as glow plugs, heating loads, DC motors and for power distribution.

1.2   Key features

The PROFET™+2 12V family supports the following features:

1.2.1   Basic features

- High-side switch with diagnostic and embedded protection
- ReverSave™ for low power dissipation in reverse polarity
- Green product (RoHS compliant)
- Complies with AEC Q100 grade 1

1.2.2   Protection features

- Absolute and dynamic temperature limitation with intelligent latch
- Overcurrent protection (tripping) with intelligent latch
- Undervoltage shutdown
- Overvoltage protection with external components

1.2.3   Diagnostic features

- Proportional load current sense signal
- Open load in ON and OFF state
- Short circuit to ground and battery

1.3 Block diagram of the single channel PROFET™+2 12V

Figure 1 shows a block diagram illustrating how a single-channel high-current high-side switch operates. For more information, see the datasheet.
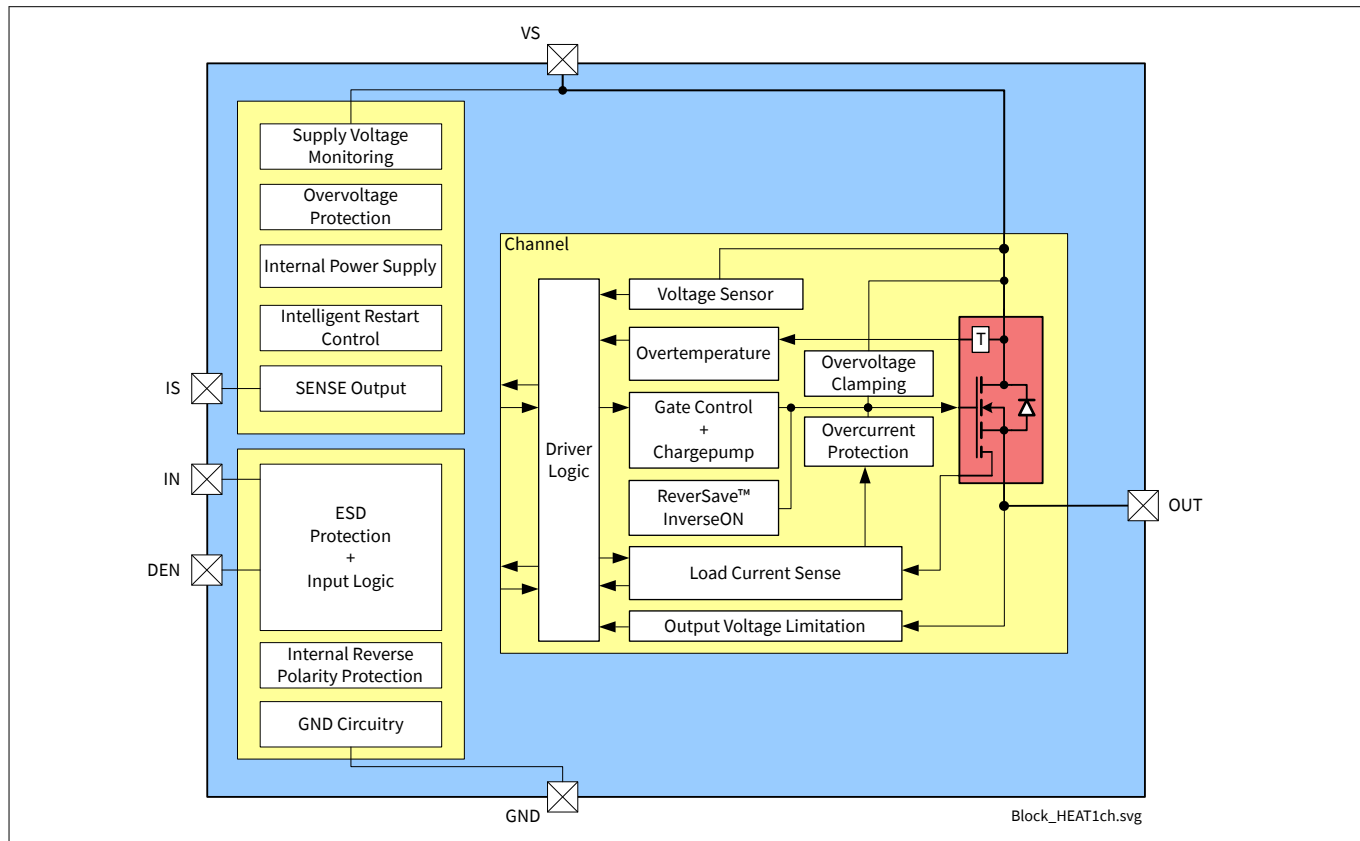

Figure 1 Block diagram of single channel PROFET™+2 12V

1.4 Overall family product summary

Table 1 shows the common feature set for the PROFET™+2 12V family.

Table 1 Product summary, whole family

Minimum operating voltage	$V_{S(OP)}$	4.1 V
Minimum operating voltage (cranking)	$V_{S(UV)}$	3.1 V
Maximum operating voltage	V_S	28 V
Minimum overvoltage protection @ 25°C	$V_{DS(CLAMP)}$	35 V
Maximum operating current	$I_{GND(ON\_D)}$	3 mA
Package	PG-TSDSO-14	

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1.5 Explanation of parameters, names and symbols

A key parameter, $R_{DS(ON)}$, represents the internal resistance of the devices. It is responsible for power loss and is part of the device name, e.g. BTS7002-1EPP for a 0.002 Ω device.

The thermal equilibrium is used to calculate the nominal current of each device, please see the following equations.

$$\left(I^2_{L(NOM)} \times R_{DS(ON)} + V_{S\_max} \times I_{GND\_max}\right) \times R_{thJA\_1s0p} + T_{A\_ECU\_max} < T_{J\_max}$$

$$I_{L(NOM)} < \sqrt{\frac{T_{J\_max} - T_{A\_ECU\_max} - V_{S\_max} \times I_{GND\_max} \times R_{thJA\_1s0p}}{R_{DS(ON)} \times R_{thJA\_1s0p}}}$$

Definitions:

$I_{L(NOM)}$ [A]	Nominal current (drain source)	(depending on temperature)
$R_{DS(ON)}$ [Ω]	Resistor (drain source)	(depending on temperature)
R_{jhJA_1s0p} [K/W]	Thermal resistance at given PCB area	(depending on temperature)
$T_{A\_ECU\_max}$ [K]	Ambient temperature close to the PCB, ECU = Electronic Control Unit	
V_{S_max} [V]	Supply voltage	
I_{GND_max} [A]	Maximum operating current	
T_{J_max} [K]	Maximum junction temperature (e.g.BTS7004-1EPP: T_{J_max} = 150°C)	

The parameters R_{thJA} (thermal resistance junction to ambient) and Rt_{hJC} (thermal resistance junction to case) are important for the package, see **Figure 2**. The necessary cooling area can be estimated based on these values, which is important for the design. In order to ensure comparability, these values are specified assuming a setup according to JEDEC JESD51-2,-5,-7 placing the device on FR4 1s0p or 2s2p board (please see **Figure 5** or **Figure 7**) at natural convection, with an ambient temperature T_A = 25°C and a given power P = 1 W. The products (chip + package) are simulated or measured on 76.2 × 114.3 × 1.5 mm size boards using setups as shown in **Figure 5** or **Figure 7**. Where applicable, a thermal via array under the exposed pad establishes contact between the first inner copper layer and the top- and bottom-layer, please see also **Figure 6**.

1.6 Package

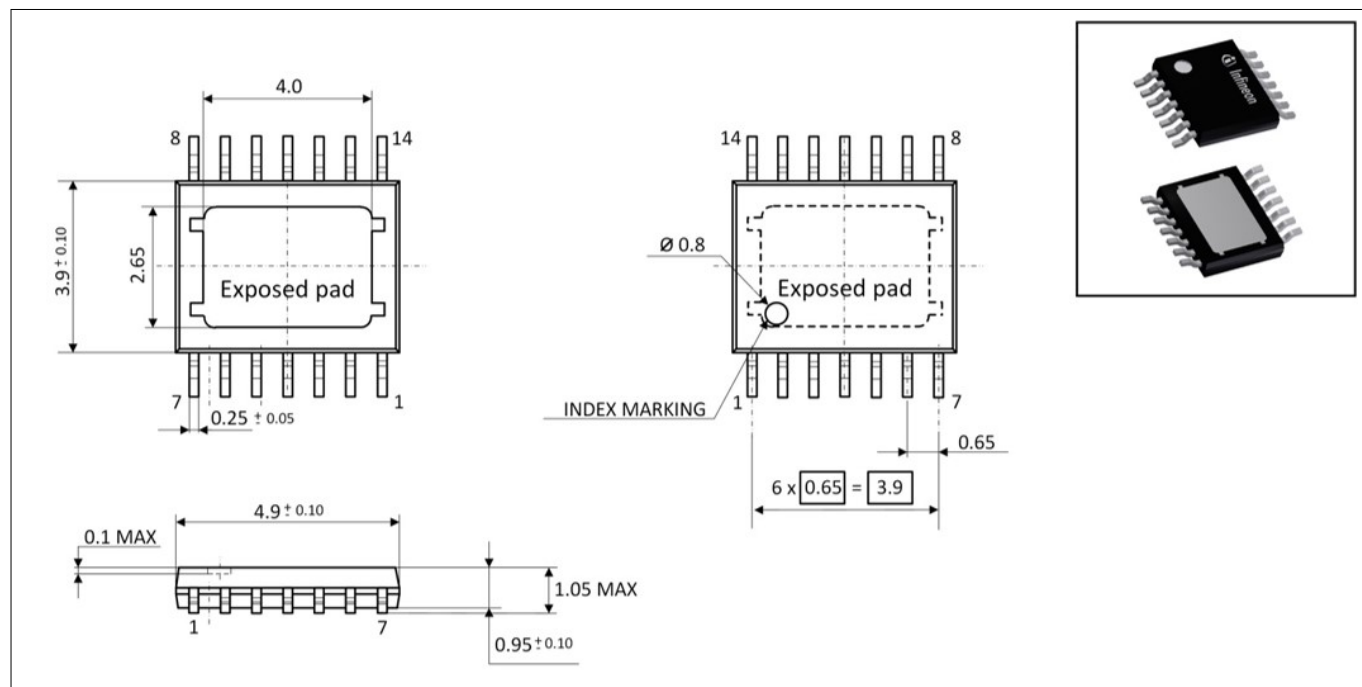*Figure 2* shows the PG-TSDSO-14 package of the PROFET™+2 12V product family.

Figure 2　　　　**Package PG-TSDSO-14**

2 Thermal layout recommendation

A properly designed printed circuit board (PCB) based on PROFET™+2 12V requires that the device junction temperature remains within absolute maximum ratings. Protection functions such as overtemperature shutdown are not designed for continuous or repetitive operation. Operation outside maximum ratings is not considered normal. For this reason, thermal PCB design should be optimized to ensure sufficient cooling of a PROFET™+2 12V. This means that the cooling area around the PCB should be designed in such a way as to ensure that maximum thermal energy can be dissipated into the environment. This means that the R_{thJA} should be as small as possible. This is very important because the areVa where the heat energy can be dissipated is rather small (approximately 11 mm^2; exposed pad).

In this document, we have used thermal resistance values based on the definitions provided below (JEDEC JESD51-13, page 4):

R_{th} (thermal resistance): a measure of steady-state heat flow from point of high temperature to a point of lower temperature, calculated by dividing the temperature difference by the heat flow between the two points.

R_{thJA} (thermal resistance, junction-to-ambient): the thermal resistance from the operating portion of a semiconductor device to a natural convection (still-air) environment surrounding the device.

R_{thJC} (thermal resistance, junction-to-case): the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across; the package interface surface can be on either the top or bottom of the package.

$$R_{thJA} = \frac{(T_J - T_A)}{P} \quad \left[\frac{K}{W}\right]$$

T_J = junction temperature $[K]$
T_A = ambient temperature $[K]$
P = powerdissipation affecting change in junction temperature $[W]$

Figure 3   **Formula for calculating R_{thJA} according to JEDEC JESD51-2A**

2.1 Standard layouts for simulation and measurements

Depending on the technical requirements and application different approaches for dissipating the thermal energy from a PCB exist. A very common solution for applications using smart high-side switches is a PCB with natural convection, i.e. without any cooling devices and non-blown air. In this case only the surface of the copper area, where the chips are mounted, can be used to dissipate the heat into the air. In order to achieve comparable measurement- or simulation results for the thermal behavior of the design two major standards are used:

1. $R_{thJA1s0p}$ – PCB JEDEC 1s0p board: footprint only or with cooling Cu (300 mm^2, 600 mm^2 or 1000 mm^2)
2. $R_{thJA2s2p}$ – PCB JEDEC 2s2p board

70µm modelled (traces, cooling area)

1.5 mm

70µm; 5% metalization*

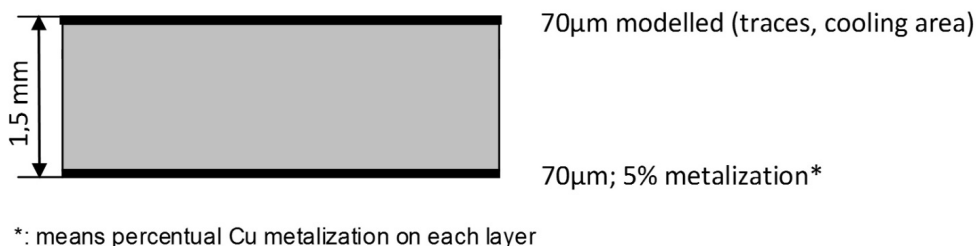*: means percentual Cu metalization on each layer

Figure 4   **Cross section of JEDEC 1s0p board**

2 Thermal layout recommendation

On the 1s0p board, the cooling area of the cooling surface is located at the top. Additional wires (traces) are located at the bottom of the board (see *Figure 4*). *Figure 5* shows a standardized 1s0p PCB board with 600 mm^2 cooling area which will be used for measurements or simulations.
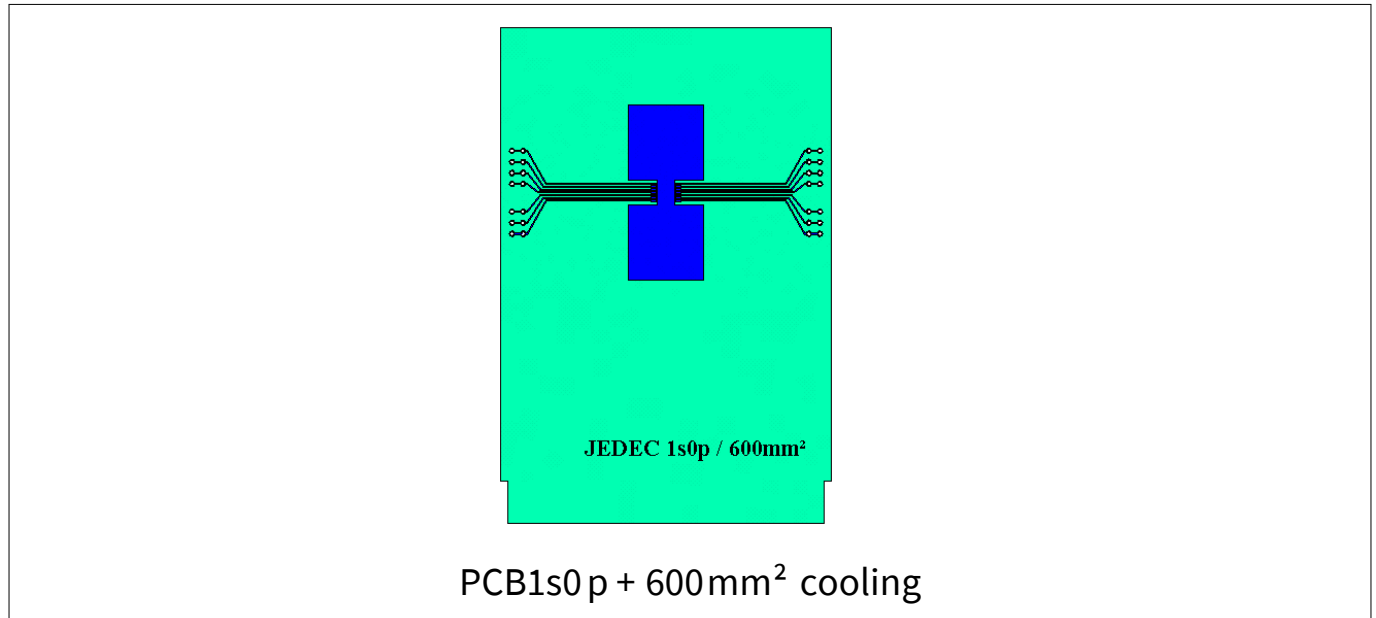

PCB1s0 p + 600 mm² cooling

Figure 5   Standardized JEDEC 1s0p PCB board

The blue areas represent the entire cooling surface; the connecting leads in this example are on the same layer.

Figure 6 shows a cross-section of a JEDEC 2s2p PCB board used for simulations and measurements. The upper, the first internal and the lower layer are connected by means of thermal vias. This increases the surface of the copper area significantly.
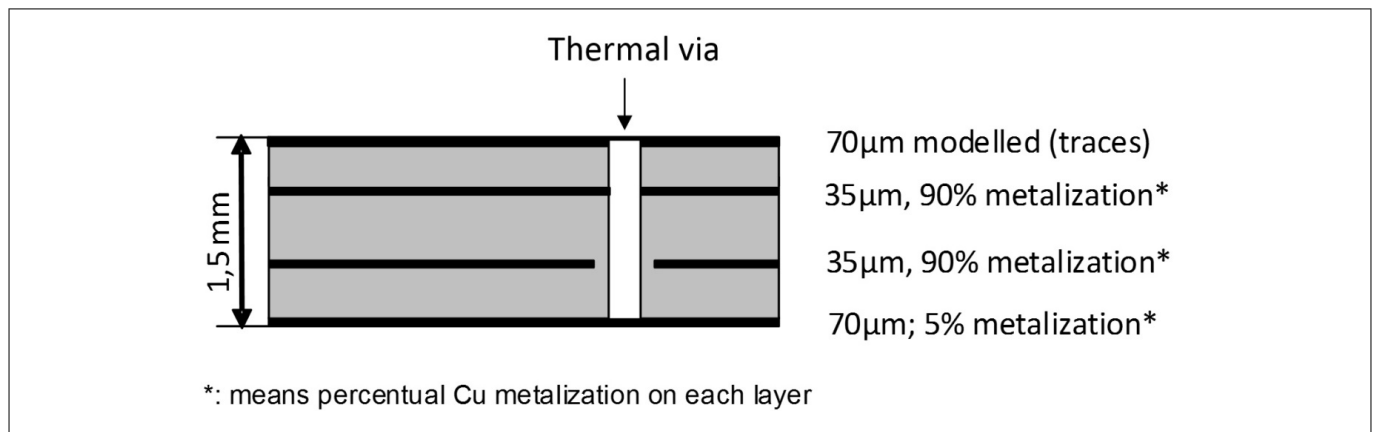

Figure 6   Cross section of JEDEC 2s2p board
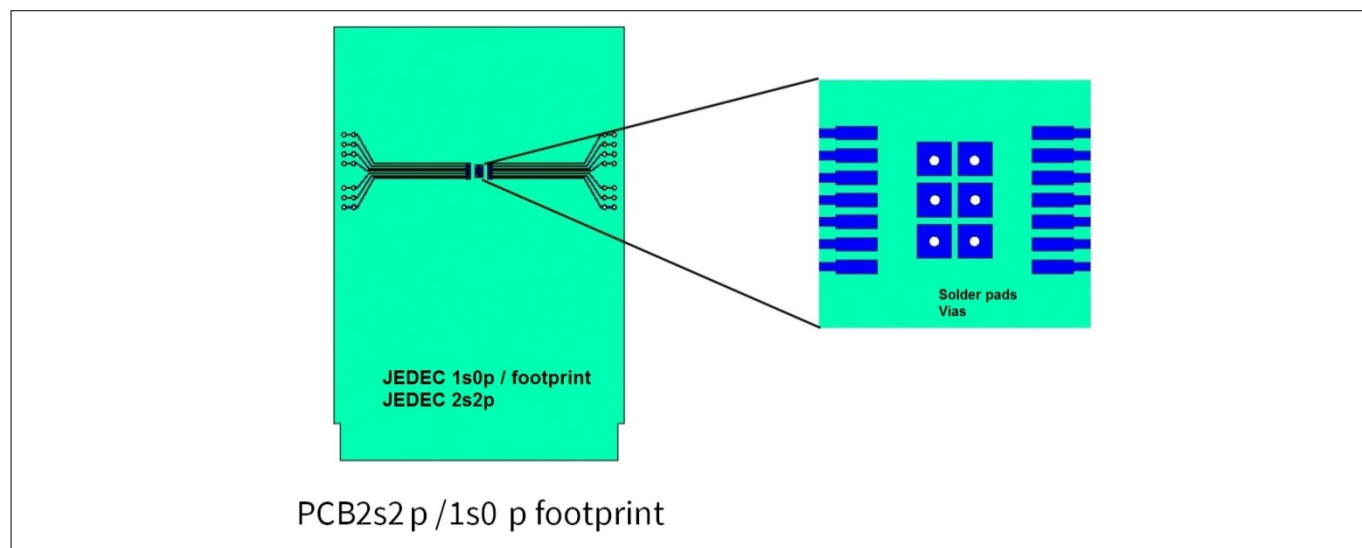
2 Thermal layout recommendation

Figure 7   **Standardized JEDEC 2s2p PCB board with vias at the solder pad PG-TSDSO-14**

The internal layer should of course not be as highly loaded, because that would make it more difficult to dissipate the heat. However, it acts as a small capacitor and can quickly absorb a certain amount of heat. Depending on available space it is also possible to provide a larger copper area for extra cooling at the top layer as well.

2.2 Thermal performance

Figure 8 and *Figure 10* shows as example the thermal properties of the BTS7004-1EPP mounted in the basic layouts just presented. For the data of the rest of the PROFET™+2 12V family please refer to the corresponding datasheets.
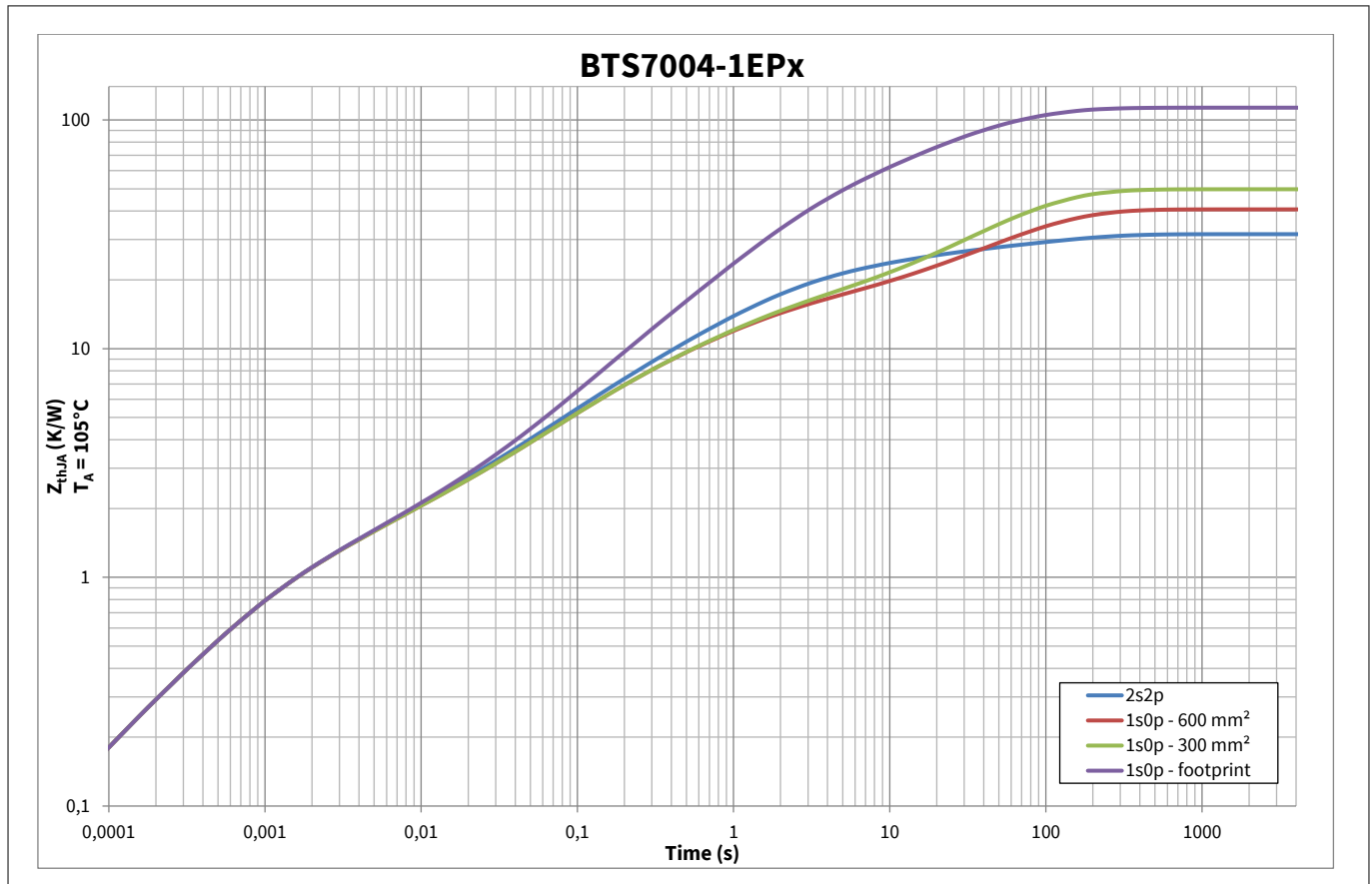

Figure 8   Typical thermal impedance

The difference in the thermal resistance (thermal impedance with t-> ∞) between JEDEC 2s2p and JEDEC 1s0p with 600 mm^2 cooling area is approximately 10 K/W (see *Figure 8*).

Figure 9 is similar to *Figure 8* but provides additional information.
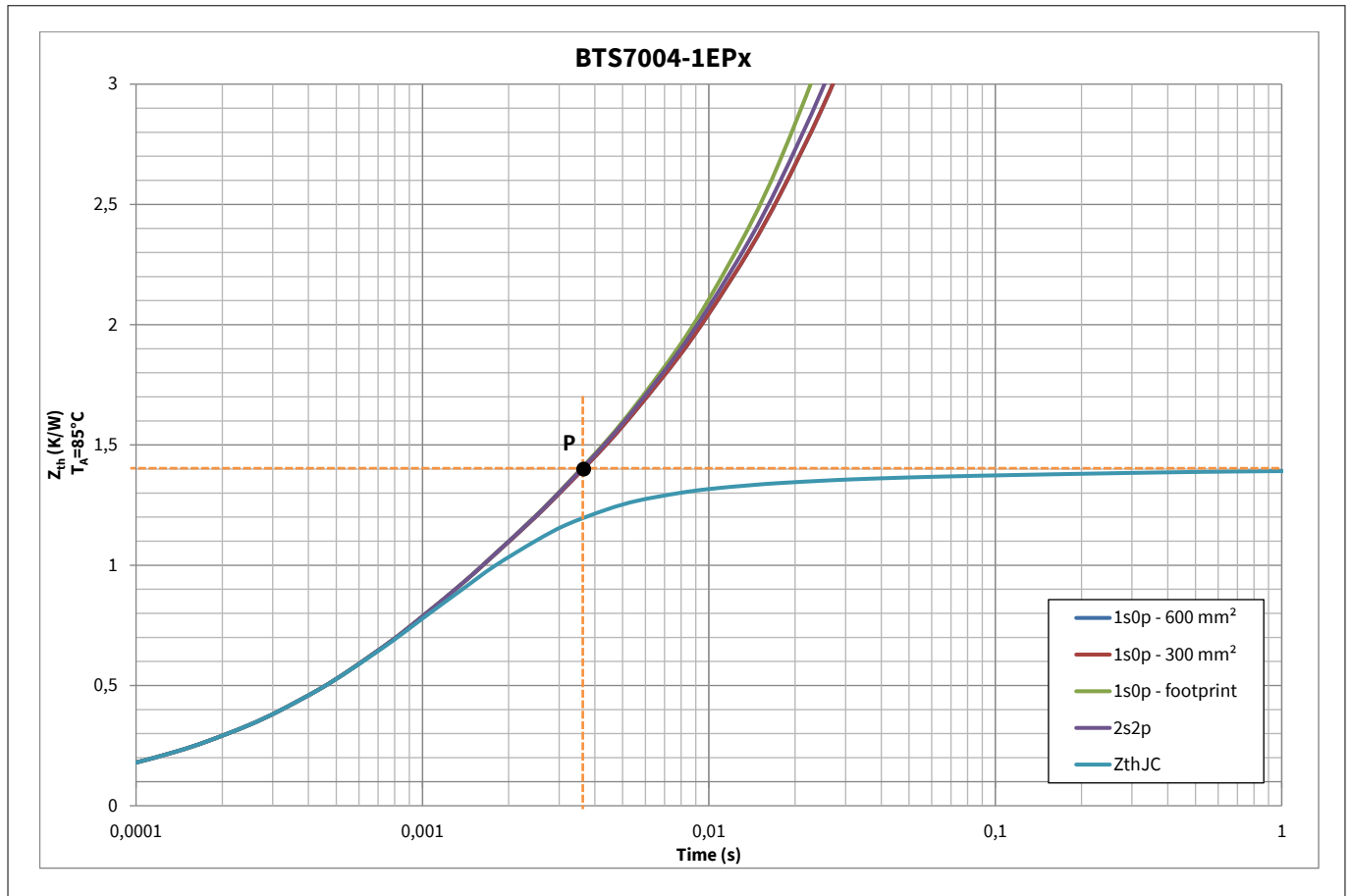
2 Thermal layout recommendation

Figure 9   Typical thermal impedance – zoom in

For short-time (approximately 4 ms), the chip is able to dissipate the heat. This point "P" matches to the parameter R_{thJC}. At this point "P" the value of Z_{thJA} is equal to the parameter R_{thJC} (see **Chapter 1.5**). After this point (t > 4 ms) the curves drift apart. This means, that the PCB design is now the main factor for a maximum flow of thermal energy into the environment.

The next graph shows the dependency of the thermal resistance R_{thJA} on the used cooling surface, based on design 1s0p.

BTS7004-1EPx

Figure 10 — 1s0p - Ta = 105°C

Y-axis: R_{thJA} (K/W) — ranging from 30 to 120
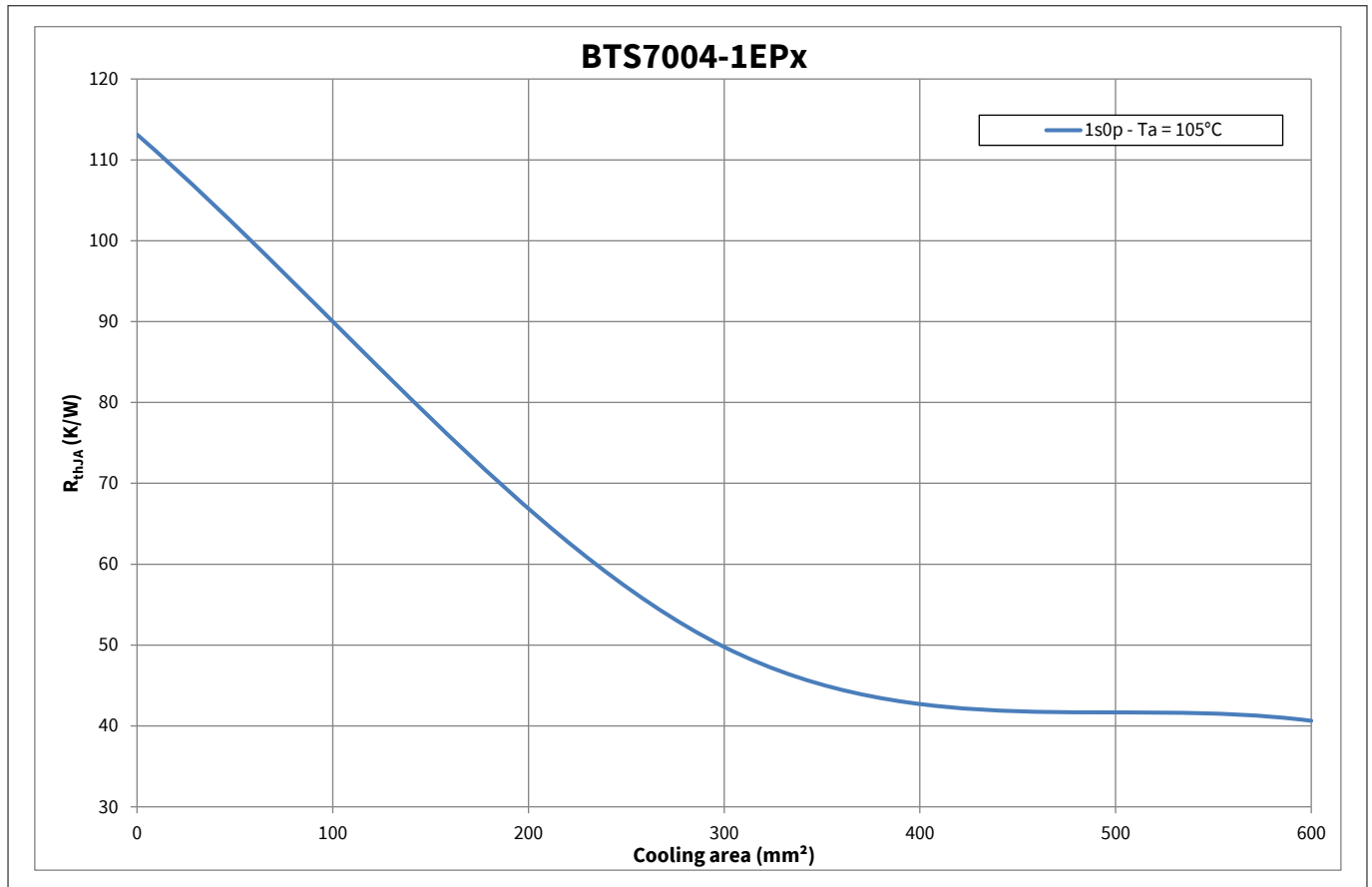X-axis: Cooling area (mm²) — ranging from 0 to 600

Figure 10   **Thermal Resistance on 1s0p PCB with various cooling surfaces**

Figure 10 shows the limits of expanding the cooling surface area of the standard 1s0p device. A decrease in the thermal resistance can be observed up to an enlargement of the cooling surface to 400 mm². A further enlargement does not significantly improve the cooling behavior.

2.3   Placement of thermal vias

This section shows the relationship between area size, number of cooling areas (example 2s2p) and thermal resistance. *Figure 8* shows that the lowest thermal resistance is achieved with a 2s2p PCB arrangement. Here, PCBs are compared according to the JEDEC standard in order to obtain meaningful results.

When using PCBs with JEDEC 2s2p, thermal vias are needed to ensure the thermal flow to the different layers.

Figure 11 shows a recommended arrangement of vias for the PG-TSDSO-14 package according to the standard JEDEC 51-5. The blue areas are only shown in the layout system; on the PCB only copper is visible. This is to show the locations where vias are located or where the pins can be soldered.
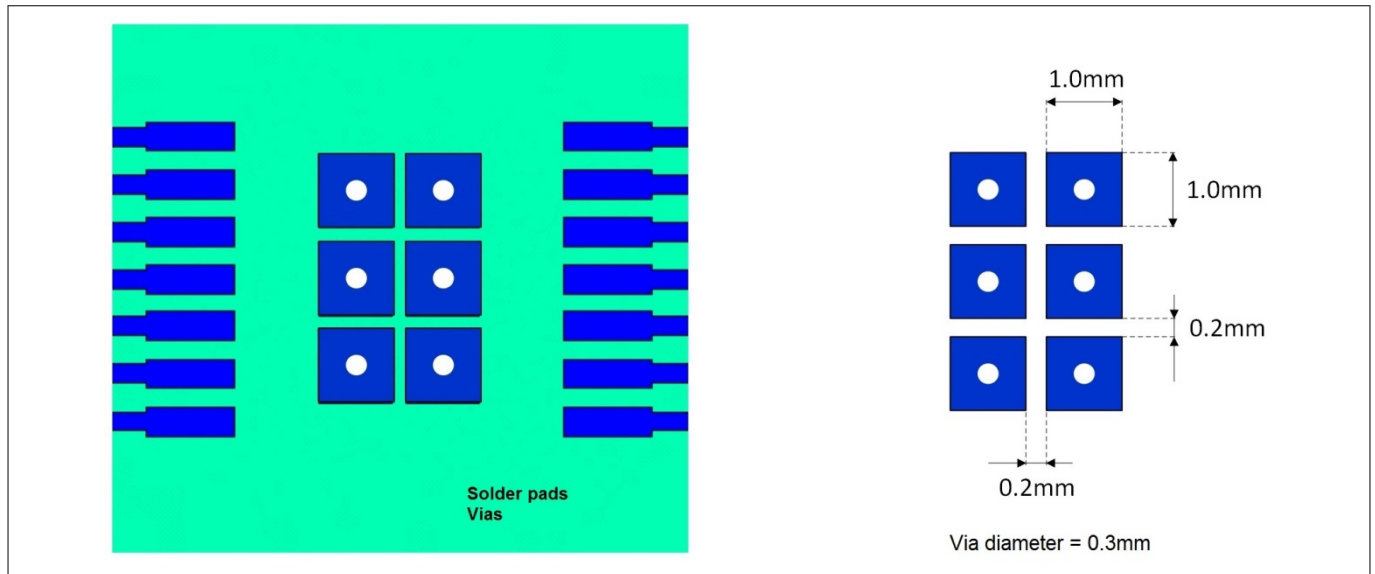
2 Thermal layout recommendation

Figure 11   **Specification of thermal via layout and array pattern for PG-TSDSO-14 related to JEDEC 51-5**

When comparing the package PG-TSDSO-14 with the layout (not to scale), a number of possibilities for optimization are revealed because the area of the vias does not completely cover the area of the exposed pad on the chip (see *Figure 12*). For example, it is possible to implement more vias.

Of course, a minimum distance between pattern and PINs must be maintained in order to ensure a corresponding insulation resistance.
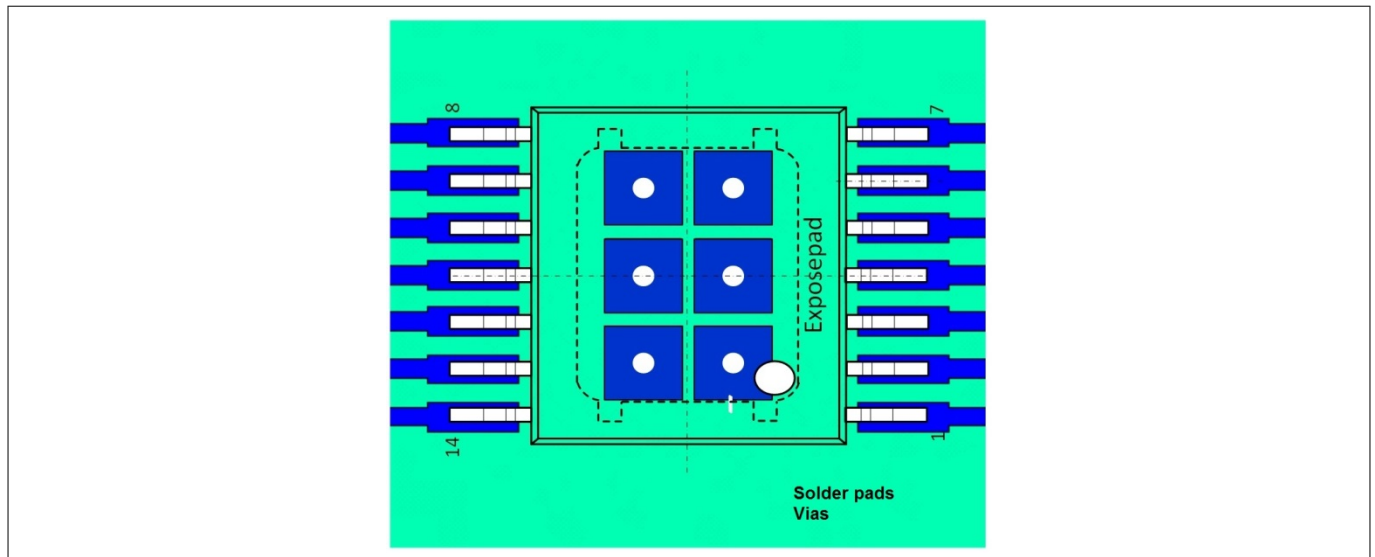

Figure 12   **Via Layout versus package PG-TSDSO-14**

Another problem arises from the fact that some assembly companies are unable to process this type of via connections (vias directly under the package) due to soldering problems. In this case other ways of implementing thermal vias must be developed and tested (see also *Chapter 3*).

3 Practical designs and comparisons

The following chapter discusses some differences with respect to thermal coupling. Two different evaluation boards with the BTS7004-1EPP are used as reference designs. These are two-layer boards with enough copper to cool the switch down. The thickness of the two copper layers are 70 µm.

3.1 PCB design with ring-shaped arrangement of vias

In the following design, an attempt was made to place the vias not directly on the copper surface under the exposed pad in order to prevent possible production problems. *Figure 13* shows the top layer design Rev2.0, *Figure 14* shows the bottom layer.
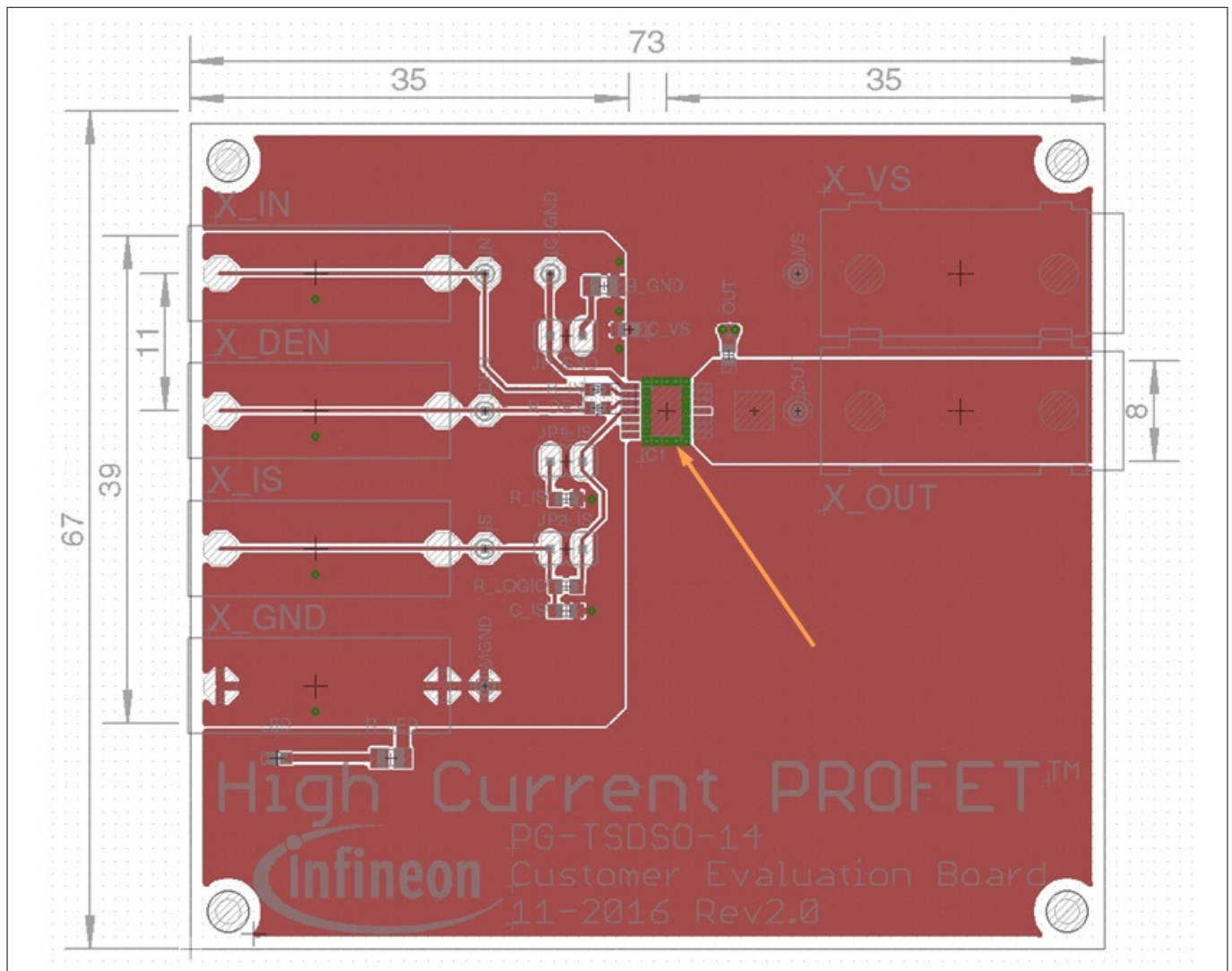

Figure 13 **Top layer with a ring-shaped via arrangement**

The green squares indicate the area where the vias are placed. The vias are directly connected with a part of the red copper area on the top layer and with a part of the blue copper area on the bottom layer (see *Figure 14*).

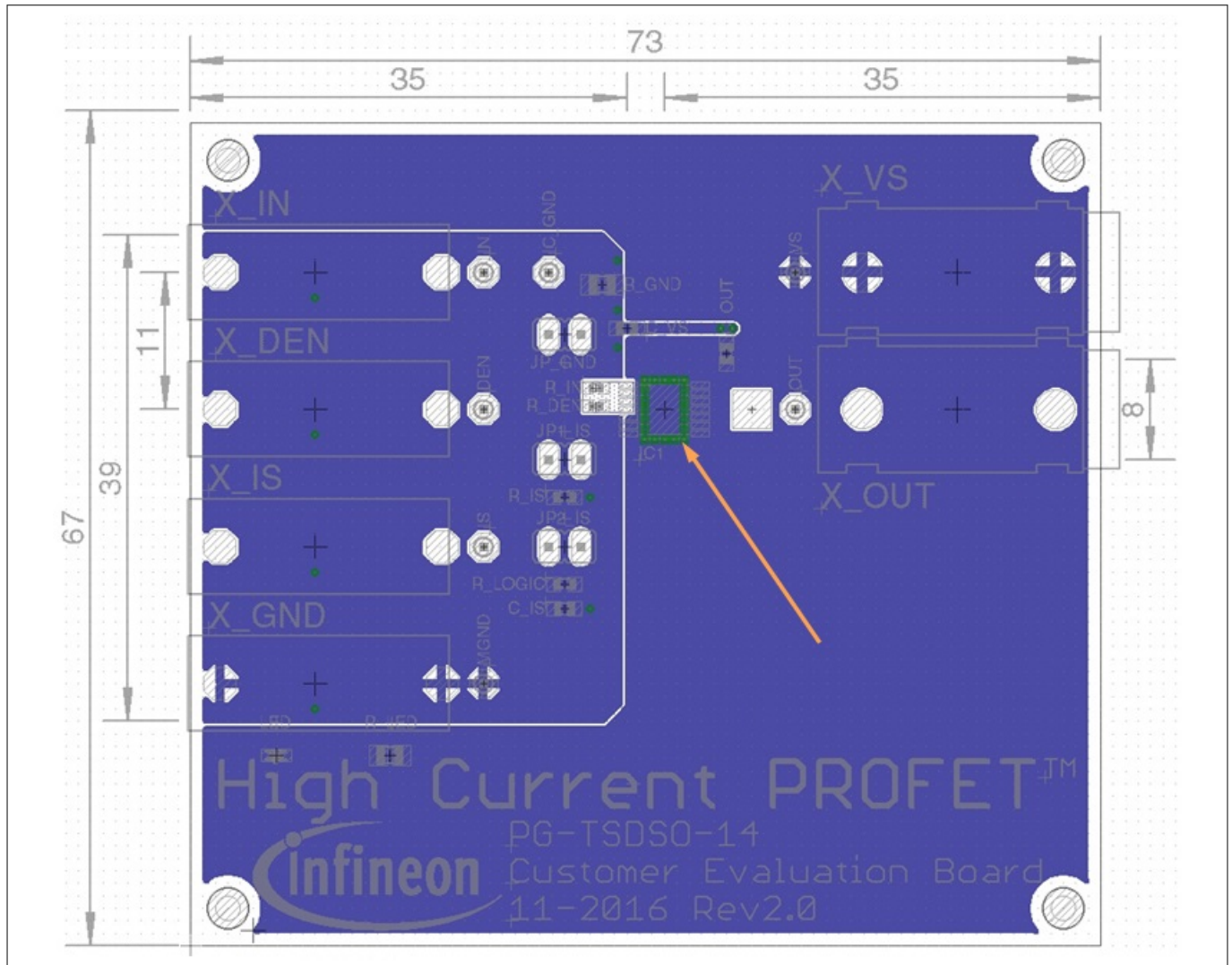## 3 Practical designs and comparisons

Figure 14   Bottom layer with a ring-shaped via arrangement

On the bottom layer, the area of the BTS7004-1EPP is only shown schematically. The green rectangle shows the points where the vias are connected with the top layer.

Figure 15 shows more details. Again, the green pads are of copper; the color is determined by the layout tool (Eagle).

3 Practical designs and comparisons

Figure 15   **Zoom into the ring-shaped arrangement of the vias (top layer, Rev2.0)**

In this case 20 vias are placed around the area above the exposed pad to distribute the heat energy to the second layer. The white area is where the device will be soldered, i.e., there is no solder resist here. Solder resist is applied to the rest of the PCB, including directly above the vias. Since the chip is soldered onto the top layer and fully covered by solder material in the area inside the frame and at the PINs to the left and to the right, the heat energy must first move laterally to the vias on the top layer and to the remaining copper surface of the top layer, in order to move thereafter through the vias to the copper surface on the bottom layer.

3.2 PCB design with vias related to standard JEDEC 2s2p

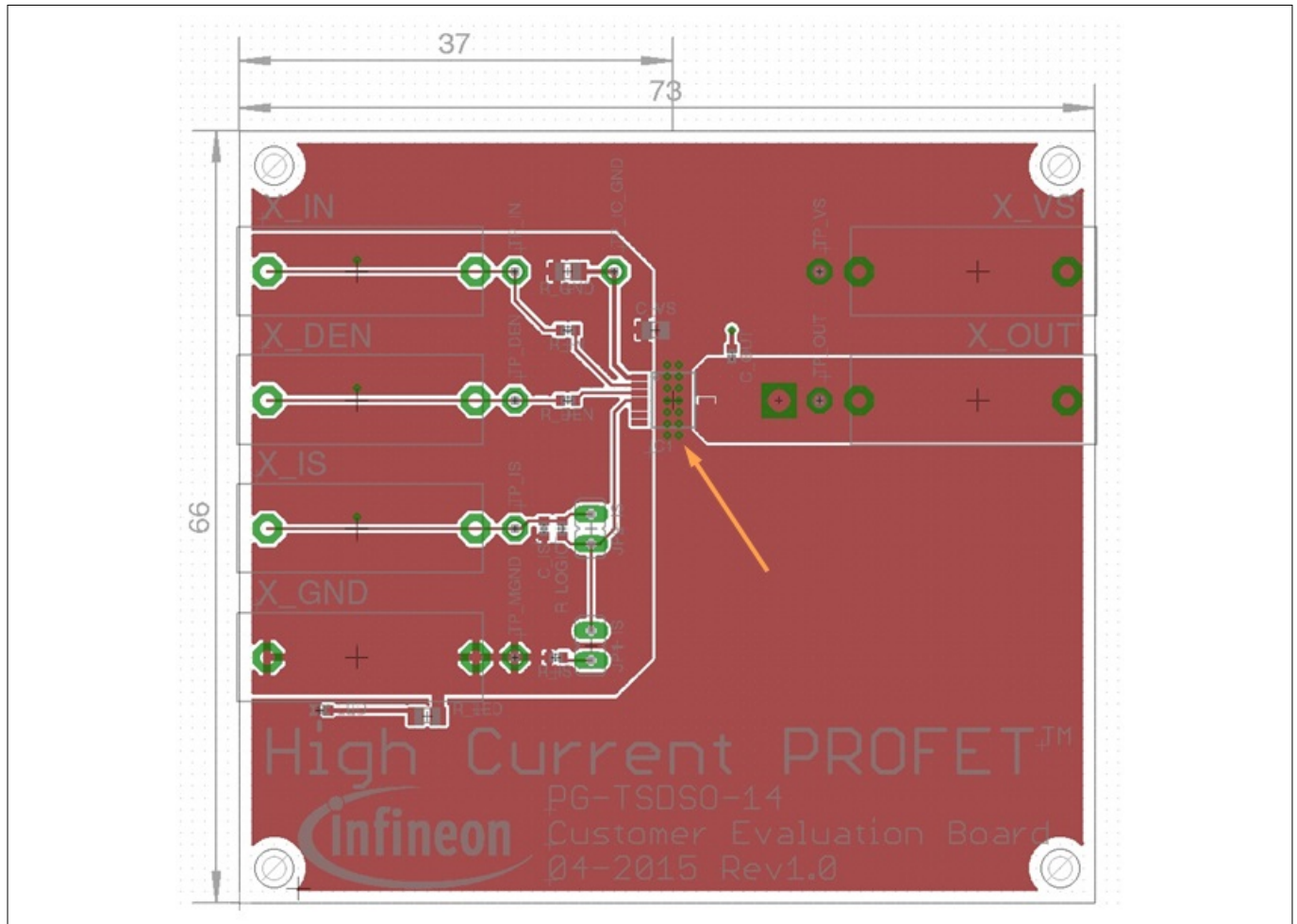*Figure 16* shows a PCB design corresponding to JEDEC 2s2p as discussed in *Chapter 2.3*.

Figure 16 **Top layer with via arrangement according to the JEDEC 2s2p standard (14 centered vias)**

In order to achieve a better cooling effect by improving the heat flow, eight more vias were added (see also *Figure 18*). The thickness of the copper of each of the two layers is 70 µm. The area (approximately 2,890 mm^2) to which the vias and the battery voltage (X_VS) are connected can be used for cooling. Since this applies to the second layer as well, the total cooling area is approximately 5,780 mm^2. The copper area for X_OUT with approximately 231 mm^2 was excluded from this calculation. This area is connected to the output of the switch. Since the thermal flow via the bond wire from the chip to the pins of the chip is not so effective, the cooling effect is limited.

The area specification is roughly the same for both board designs.
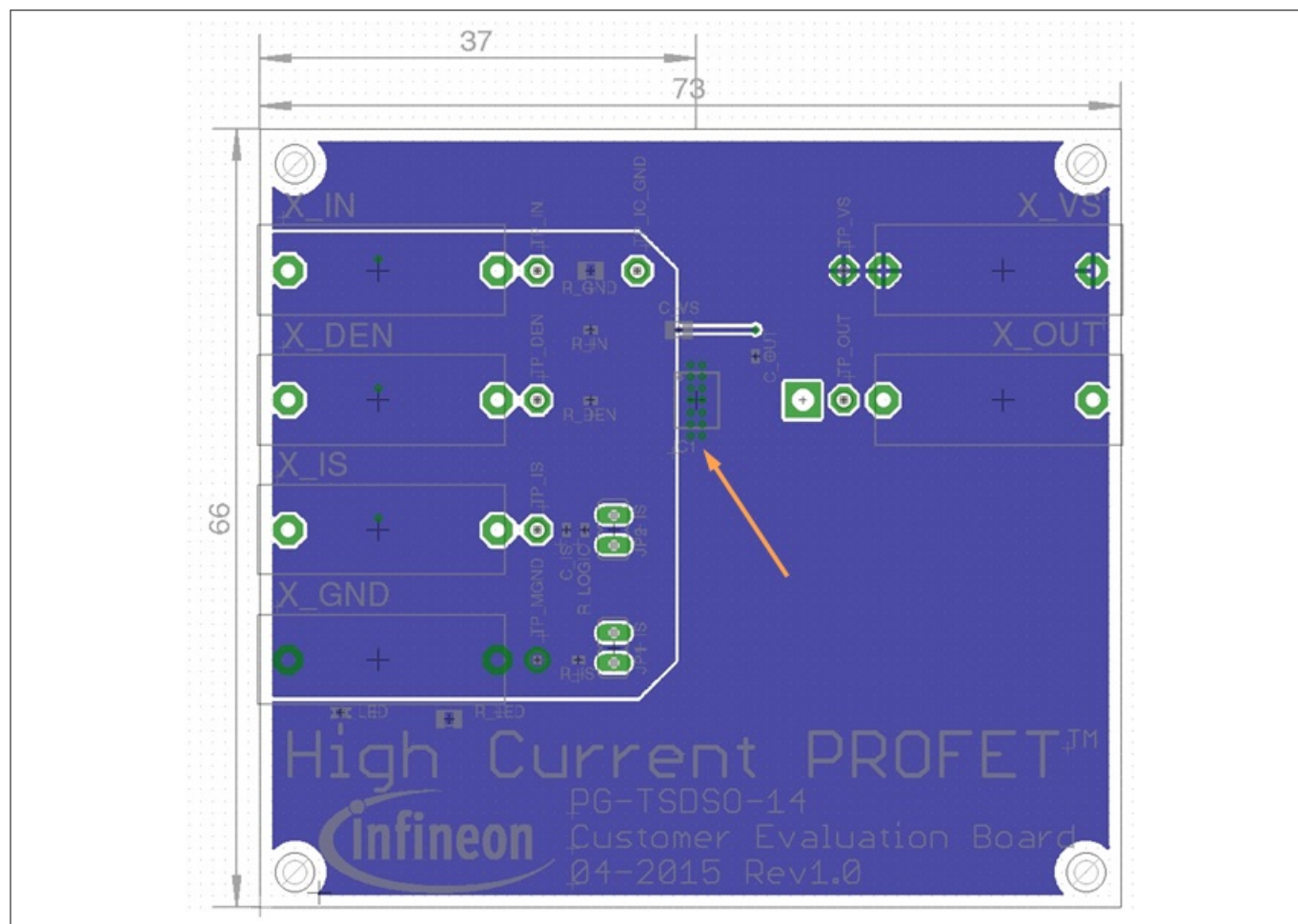
3 Practical designs and comparisons

Figure 17   **Bottom layer with via arrangement according to the JEDEC 2s2p standard**

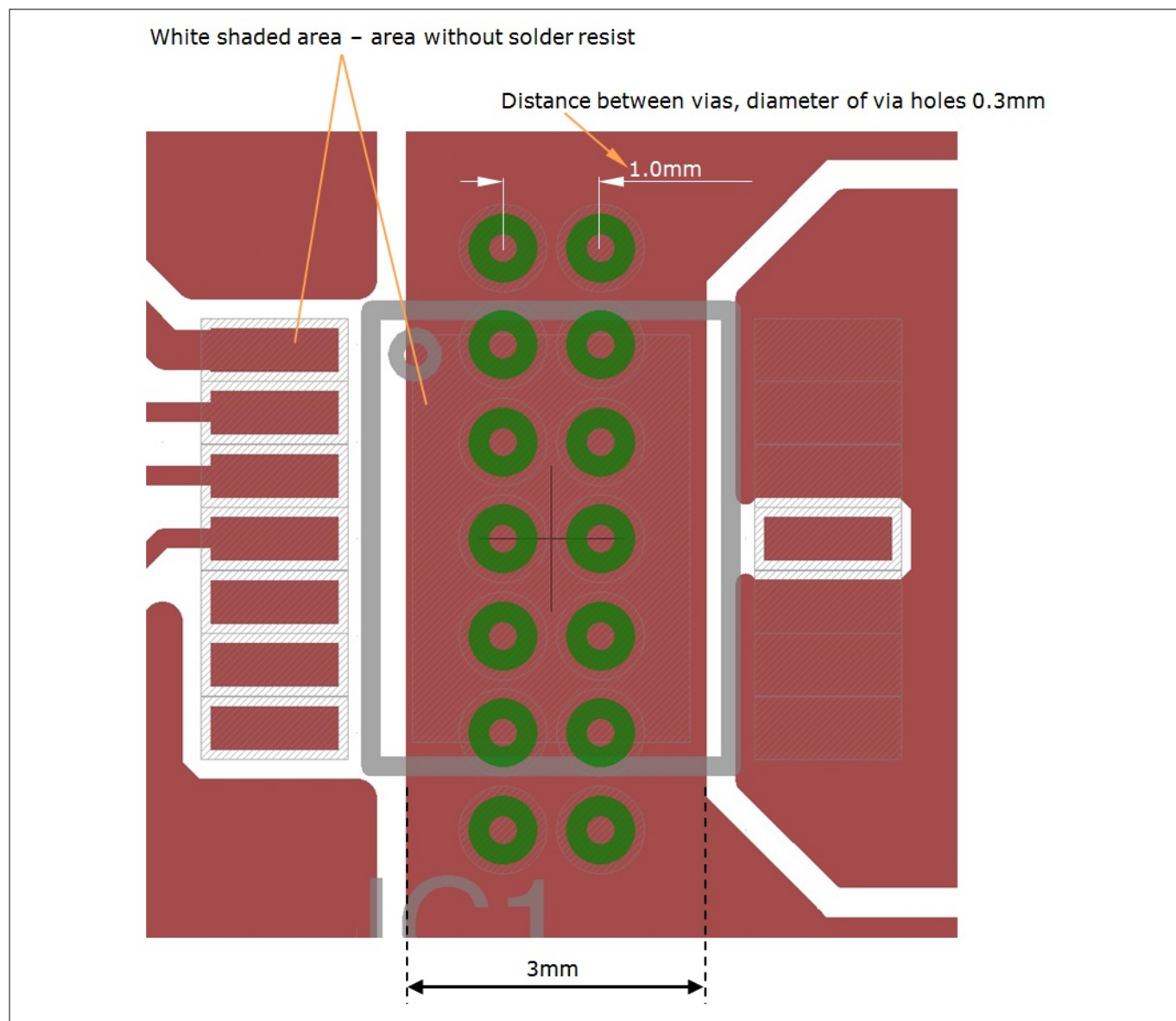## 3 Practical designs and comparisons

Figure 18   **Detail view of thermal via layout related to JEDEC 2s2p (top layer, Rev1.0)**

A total number of 14 vias distribute the heat energy to the second layer. There are 10 vias directly under the exposed pad; four more vias are located next to it. It is assumed that in this case the heat energy will be distributed from the center of the exposed pad to the second layer and there will be a thermal flow along the top layer.

3.3 Further improvements

The results of the **Chapter 3.2** led to the idea of using the area under the exposed pad more effectively. Again, the evaluation board is used as the basis, only more vias are placed under the exposed pad and the width of the trace under the package was increased, see **Figure 19**.
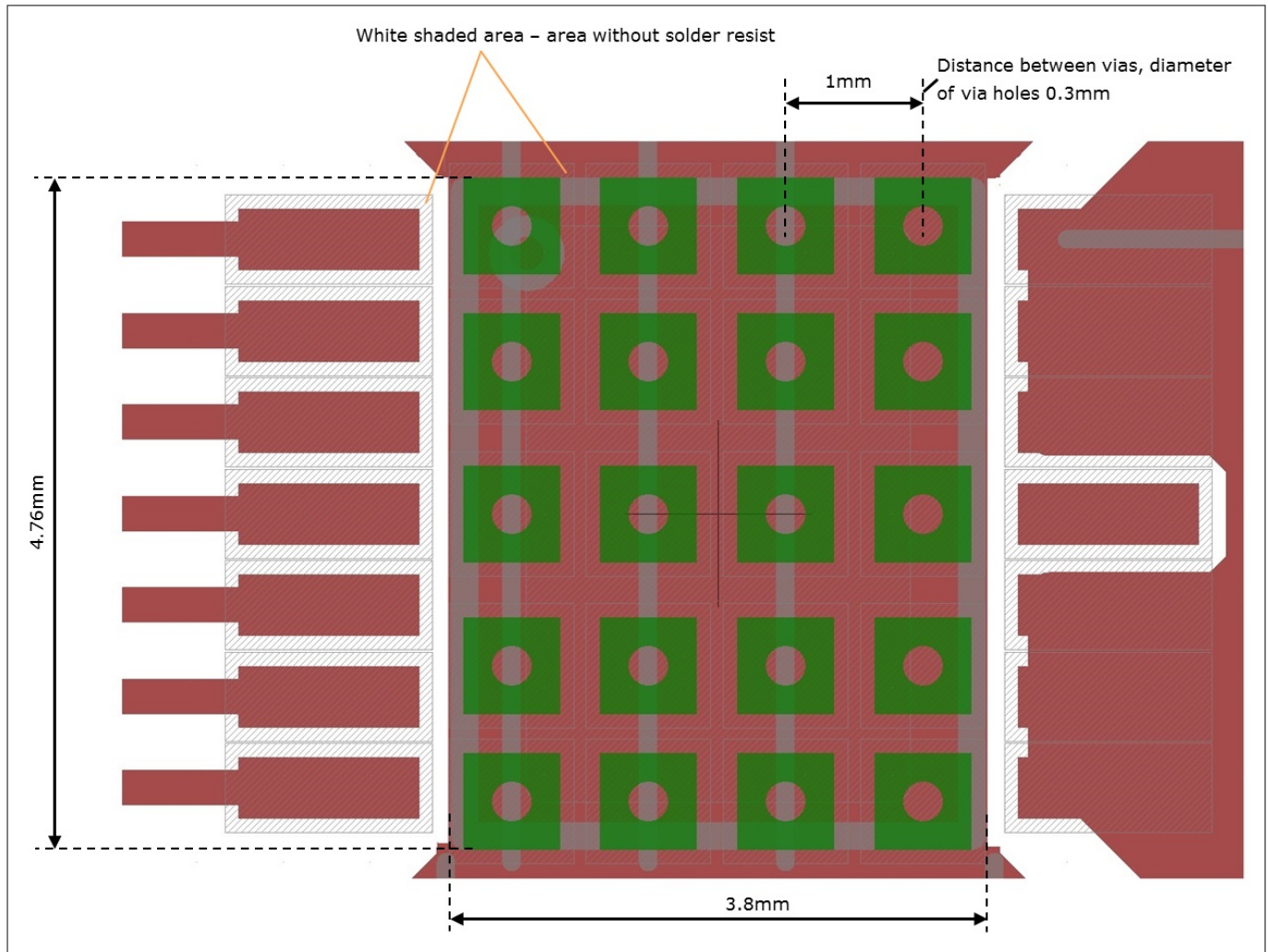

Figure 19   **Centered via design with 20 vias**

3.4 Comparison of different layouts

In the comparison of the different designs, different copper thicknesses were also considered at the same time in order to observe their influence on the thermal behavior. The comparison between the various via designs is shown in **Figure 20**, whereby the copper thicknesses of the individual copper layers are the same (70 µm). Also for the simulation of 2s2p design, all 4 copper layers were assumed with a thickness of 70 µm. With an R_{thJA} of 22 K/W has the centered design with 20 vias under the package the smallest value followed by the 2s2p design with about 25 K/W. Something surprising is the 2s2p design better than the designs with the two outer surfaces (10 vias under package and 20 vias around the package). The reason for this is the very big single copper area with approximately 5476 mm^2 at the 2s2p design in opposite of two times 2890 mm^2 of the evaluation boards. For longer times (t > 1 s) the large single area can absorb and spread the heating energy over the whole PCB area much better as the two smaller areas as designed at the evaluation board. Just the design with 20 vias under the package and the same design as the evaluation board show better results since the area under the package could be maximized. This fact along with the fact that much more vias were placed under the chip explains the result with the lowest value of R_{thJA}.
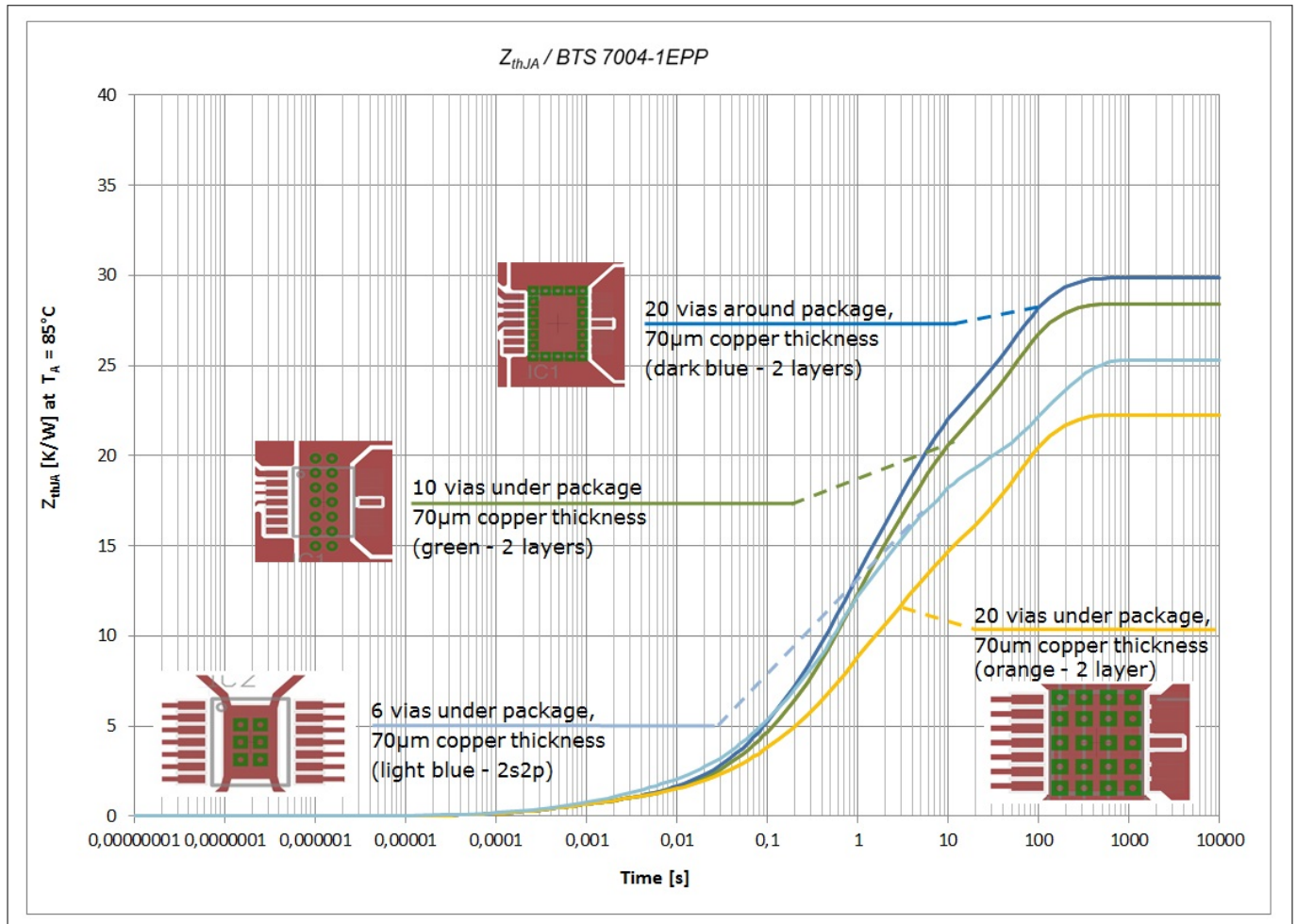
3 Practical designs and comparisons

Figure 20   **Summary of thermal impedances for different via placements**

A second interesting fact is the comparison of the same designs, but with different thicknesses of the respective copper layer. The results are shown in **_Figure 21_**.

Till to the point of approximately t = 1 s, the design with 20 vias under the package and 35 µm copper thickness has a better result as the design with 6 vias and 70 µm copper thickness. After a time of about 2 s, the thickness of the copper layers playing a dominant role in terms of the thermal impedance.
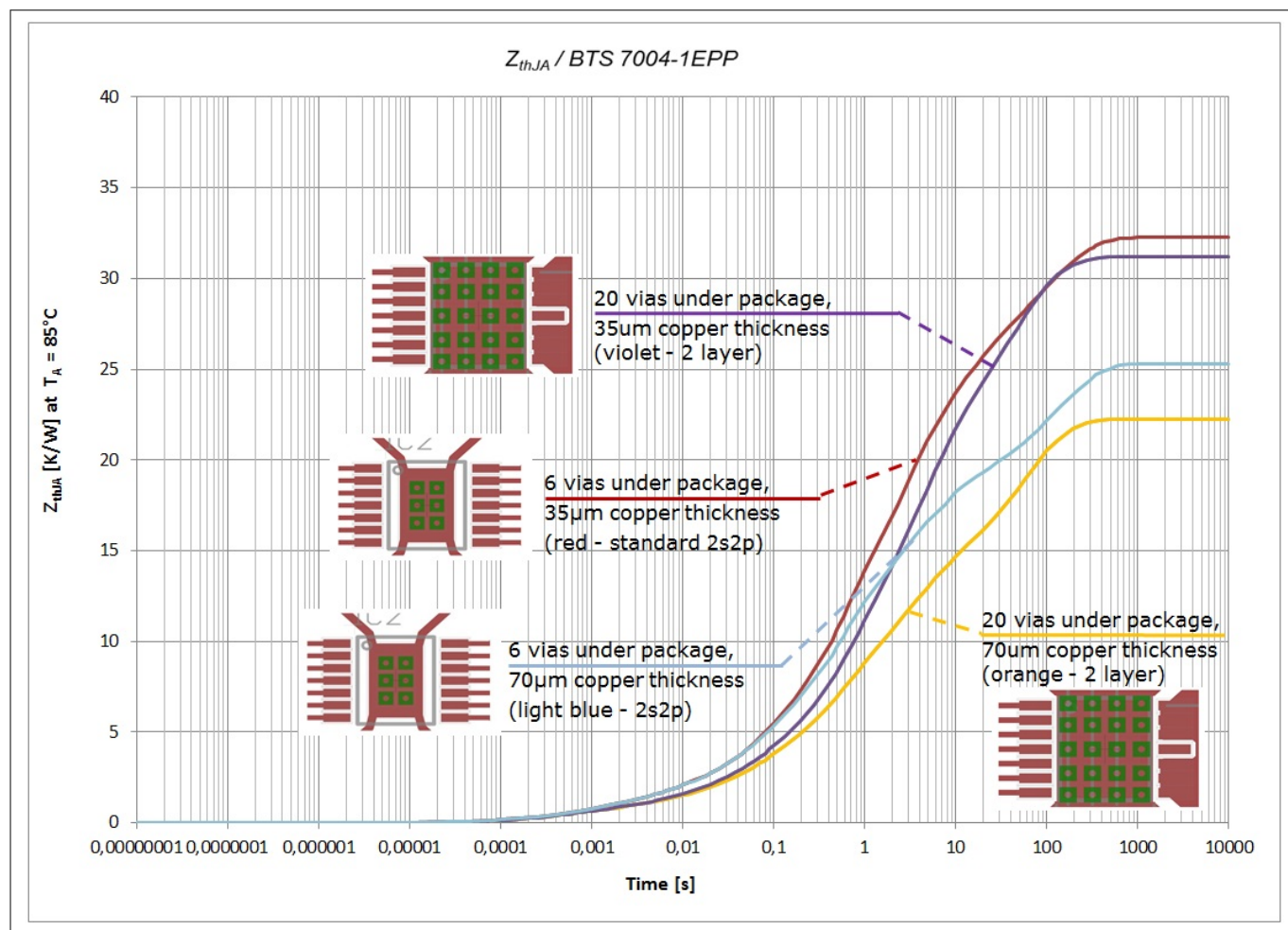
3 Practical designs and comparisons

Figure 21   **Summary of thermal impedances for boards with different copper thicknesses**

4 Summary of results

The PROFET™+2 12V family comes in an extraordinary small package PG-TSDSO-14, offering a very small footprint and a further shrink compared to existing products in DPAK or similar packages. The small size of the package required additional thoughts on PCB design, for optimized heat management.

By optimally utilizing the area on the exposed pad as well as the simultaneous provision of sufficient copper area for cooling, good results with regard to thermal resistance and thermal impedance can be achieved. In case of large-lasting thermal stress, the thickness of the copper layer has to be taken into account.

For production-critical designs (no vias possible on the exposed pad), it was shown that it is possible to place the vias around the exposed pad. However, this increases the thermal resistance. This effect can be reduced by increasing the thickness of the copper layer.

Revision history

Document version	Date of release	Description of changes
1.10	2019-05-20	Changed "*new high-current PROFET™ family*" and "*high-current PROFET™ family*" with "*PROFET™+2 12V*". Typos corrected. **Figure 2**, **Figure 8**, **Figure 9**, **Figure 10** updated. Package name changed: TSDSO-14-22 → PG-TSDSO-14
1.0	2018-01-26	Initial release.

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