TLE7268SK, TLE7268LC Application Note

Dual LIN Transceiver

About this document

Scope and purpose

This document provides application information for the transceiver TLE7268 from Infineon Technologies AG as Physical Medium Attachment within a LIN:

- Introduction to Locla Interconnect Network (LIN) (see **Chapter 1**)
- Modularity for Infineon Single and Dual LIN transceivers (see **Chapter 2.2**)
- Pin description (see **Chapter 3**)
- PCB recommendations (see **Chapter 4**)
- PIN FMEA (see **Chapter 5**)

This document refers to the data sheet of this transceiver **[1]**.

Intended audience

This document is intended for engineers who develop applications.

Table of Contents

1 Introduction to Local Interconnect Network (LIN)

The Local Interconnect Network (LIN) is a low speed class A serial bus system with a maximum baudrate of 20 kbit/s. Typical LIN bus system applications are

- Window lifters
- Rain sensors
- Light sensors
- Sun roofs
- Wiper modules

As the TLE7268 has two independant LIN transceivers integrated in one package it is suitable for applications with higher amount of LIN networks as:

- Body Control Module (BCM)
- Gateway application

The LIN bus system connects modules, actuators and sensors in a sub-bus system. A LIN network consists of a master LIN node and several slave LIN nodes (maximum 15 slave nodes). The master node controls the communication and access to the LIN bus.

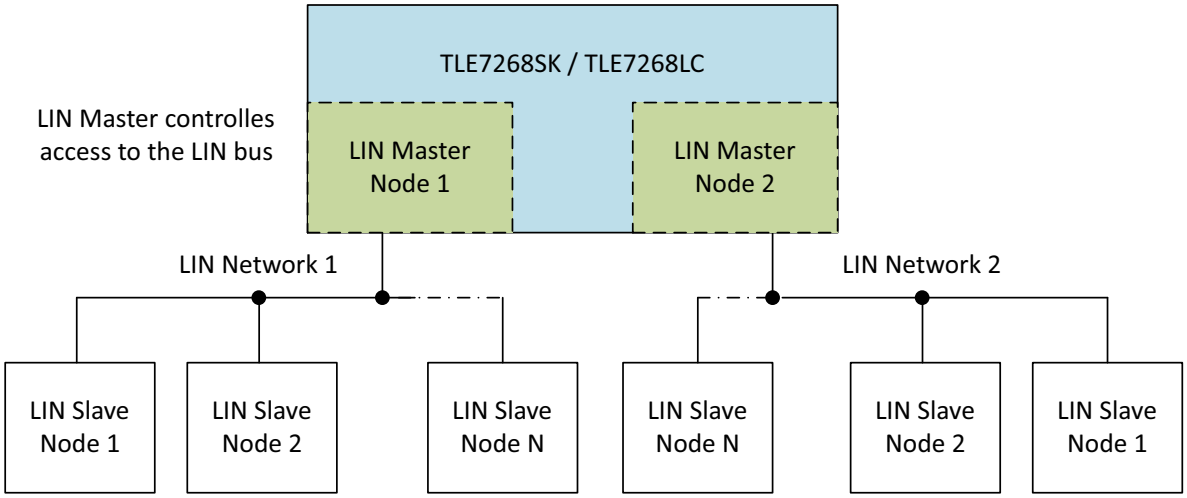

Figure 1 Master-slave LIN bus example

The LIN bus is a single wire, wired AND-bus with a 12 V battery related recessive level. The LIN Specification Package [2] defines the thresholds for the dominant level and the recessive level of the transmitting node and of the receiving node.

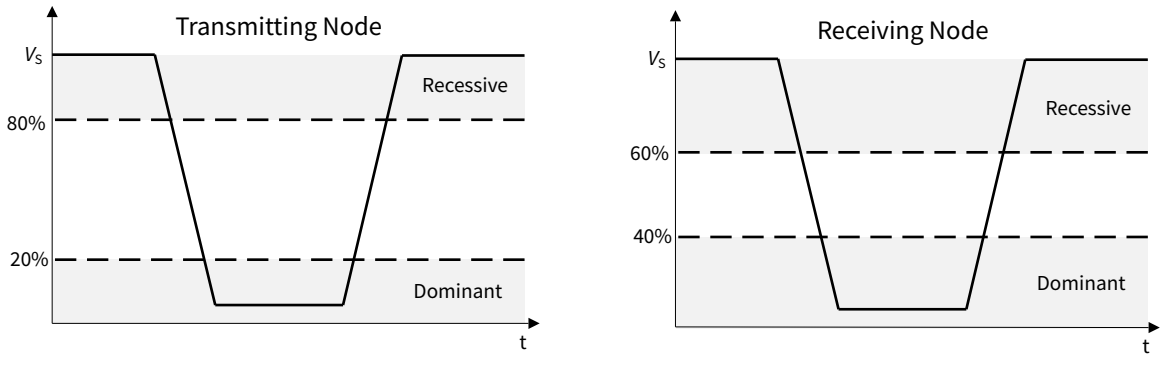

Figure 2 LIN voltage thresholds

TLE7268 is mostly suited for Body Control Modules or Gateway Applications. In these applications the TLE7268 will be used as LIN bus master node. For LIN master nodes an extra master termination resistor R_{MASTER} is required. The capacitance load C_{MASTER} is recommended in order to improve EME as well as EMI. This master application uses a reverse current diode in series with the resistor R_{MASTER} connected between LIN and (see **Figure 3**).

R_{MASTER} = 1 kΩ according to the LIN 2.x specification and to ISO 17987. The OEM specifies the capacitance value of C_{MASTER}.

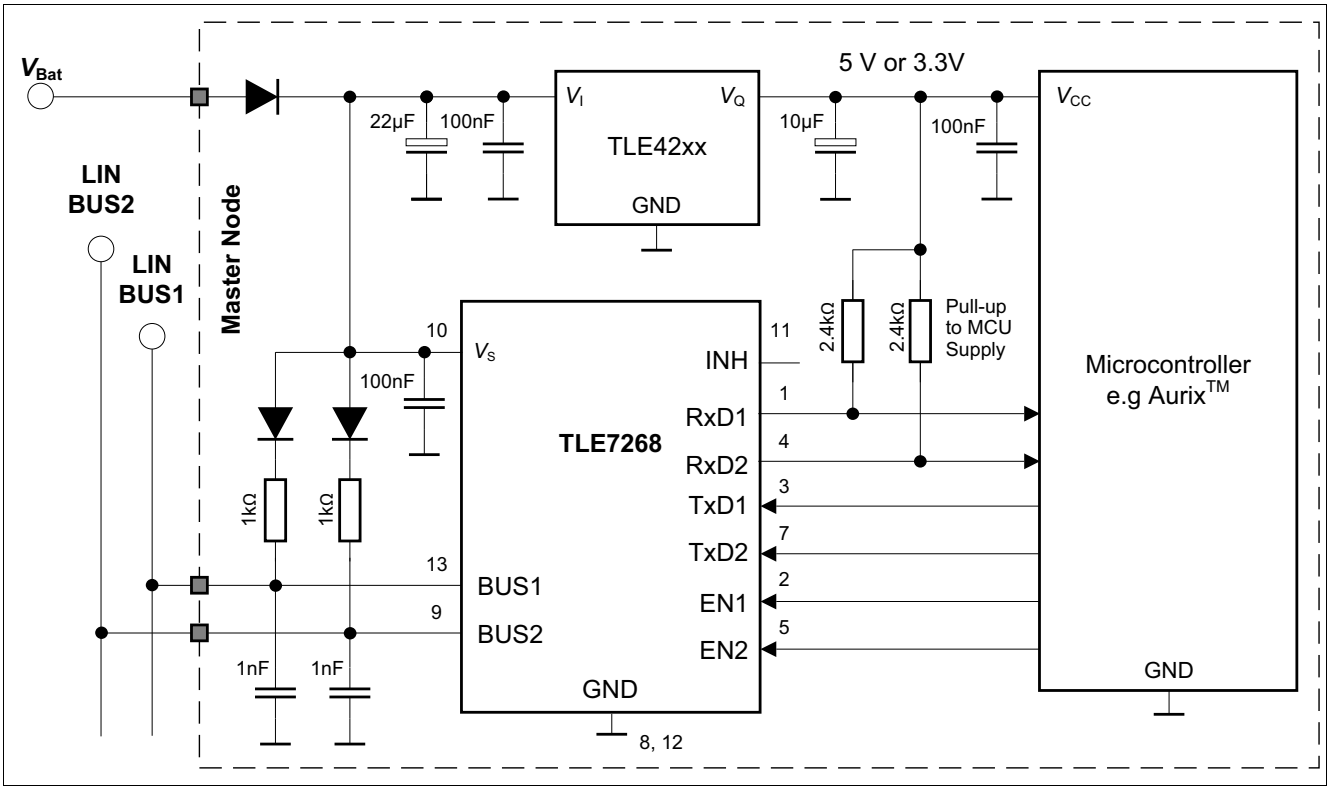

Figure 3 Master node application example with TLE7268

2 General description

The transceiver TLE7268 represents the Physical Medium Attachment, interfacing the LIN master protocol controller and the LIN slave protocol controllers to the LIN transmission medium. The LIN transceiver converts the transmit data stream of the protocol controller at the TxD input to a bus signal with controlled slew rate to minimize Electromagnetic Emission (EME). The receiver of the TLE7268 detects the data stream on the LIN bus line and transmits the data stream to the protocol controller via the RxD pin.

The TLE7268 provides low-power management modes with minimized current consumption for both integrated LIN channels:

- Sleep Mode
- Stand-by Mode

2.1 Features

The main features of the TLE7268 are:

- Two LIN transceivers in one package
- Single-wire LIN transceiver for transmission rates up to 20 kbit/s
- Very low current consumption in Sleep Mode: maximum 15 µA (typical 8 µA)
- Very low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Excellent ESD performance according to HBM (+/-8 kV) and IEC 61000-4-2 (+/-10 kV)
- TxD dominant time-out function
- Available in standard PG-DSO-14 package and tiny PG-TSON-14 package

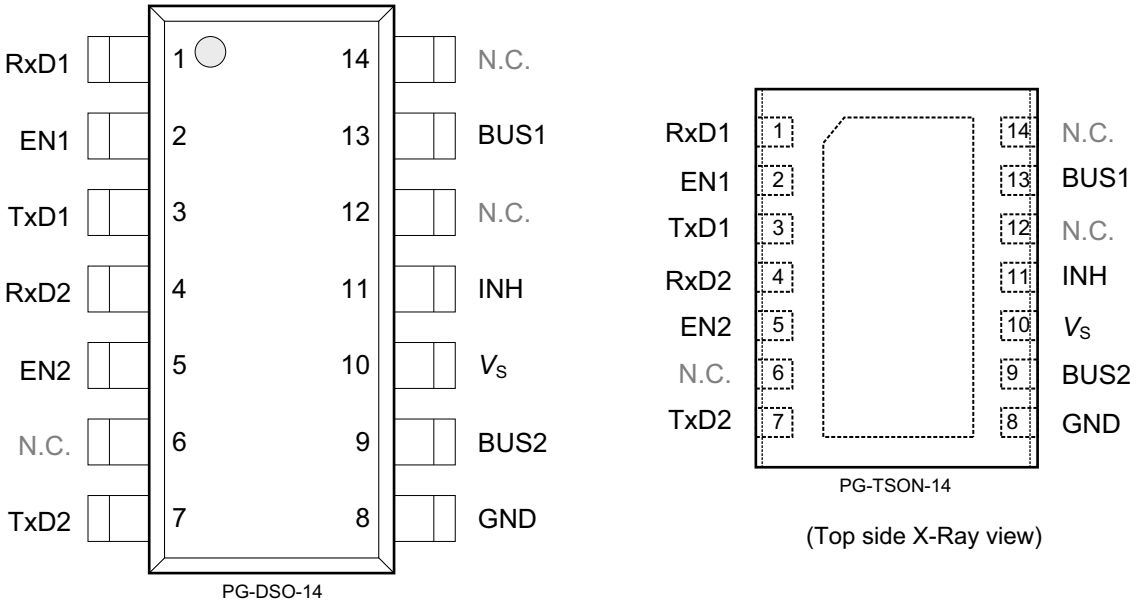

Figure 4 Pinout of TLE7268

2.2 Modularity with Infineon Single LIN Transceivers

Infineon TLE7268 offers the pin-out compatibility and modularity to single Infineon LIN transceivers. This reduces layout efforts for placement options if either a single LIN or Dual LIN transceiver is required depending on the application.

Infineon offers a complete LIN transceiver family consisting of devices in PG-DSO-8 package (TLE7257SJ, TLE7258SJ and TLE7259-3GE) and PG-TSON-8 package (TLE7257LE, TLE7258D, TLE7258LE and TLE7259-3LE). All these devices are pin-to-pin compatible, with the only differences at the pins named N.C. (= Not Connected).

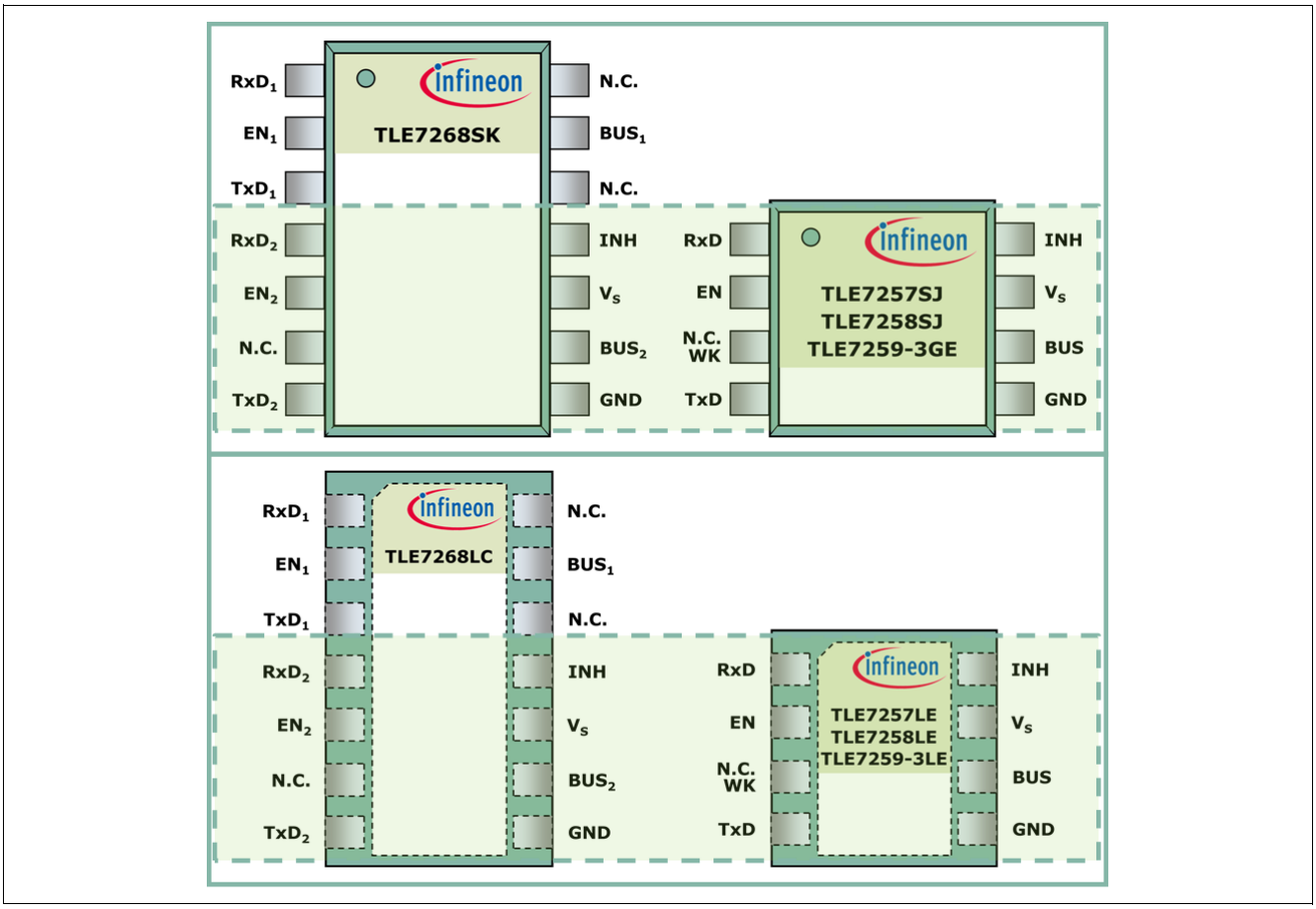

Figure 5 Pinout compatibility between Dual LIN TLE7268SK and Single LIN TLE7257SJ, TLE7258SJ and TLE7259-3GE

Table 1 Functionality of LIN transceiver family

Device	TLE7268SK/LC	TLE7257SJ/LE	TLE7258SJ/LE	TLE7259-3GE/-3LE
Features				
Fast Programming mode	-	–	–	✓
Local Wake input	-	–	–	✓
Inhibit output	VREG control	VREG control	VREG control	VREG control
TxD Time-out	✓	✓	✓	✓
Power-Up mode	Sleep mode	Sleep mode	Standby mode	Standby mode

The functional difference between the devices in the Infineon LIN transceiver family is summarized in **Table 1**. For mode details on the functional and parametric differences, please refer to the respective part's datasheet.

3 Pin description

TLE7268 is an 14-pin Dual LIN transceiver according to the LIN Specification Package [2] with two independant LIN transceivers integrated in on package.

3.1 V_S pin

The V_S pin is the supply pin of TLE7268. It is recommended to place a reverse polarity protection diode between the battery voltage V_{BAT} and the V_S supply pin, in order to protect the device in case of reversed polarity of GND and V_S voltage. In order to dampen noise coupling through battery supply it is recommended to place external capacitors close to the V_S pin. The external capacitors should be dimensioned both for high and low frequency transients.

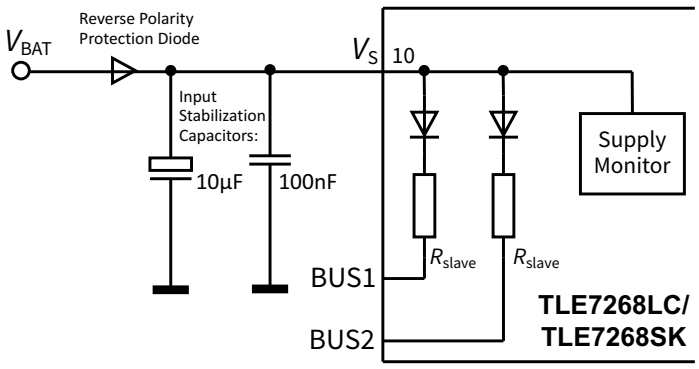

Figure 6 Typical V_S supply voltage output application

3.2 GND pin

The GND pin must be connected as close as possible directly to module ground in order to reduce ground shift. GND level must be identical for transceiver, microcontroller and LIN bus system.

3.3 EN1 & EN2 pin

The EN1 and EN2 input pins sets the mode of the dedicated LIN channel of TLE7268. The EN input is usually connected to output ports of a microcontroller. The internal pull-down resistor R_{EN} of the EN input pin provides a defined input level in case of open circuit failure. If the EN pin is unconnected, due to the internal pull-down resistor the EN input signal is set to “low”. If the TLE7268 is supplied by V_S, the device will go to Sleep Mode in order to save battery current. In Sleep Mode the current consumption is reduced to a minimum. The range of the EN input threshold supports devices supplied at 5 V as well as devices supplied at 3.3 V.

3.4 TxD1 & TxD2 pin

The TxD input pin receives the data stream from the microcontroller. In Normal-operating mode the transceiver transmits the data stream, which the microcontroller sends to the TxD pin, to the LIN bus. In any other mode the TxD input pin is blocked.

In Normal Operation Mode, in Init Mode and in Stand-by Mode the TxD pin provides an internal weak pull-up current source I_{TxD} to ensure a defined input level in case of open circuit failure. In case of permanent dominant TxD input level, the TxD dominant time-out function disables the transmitter to prevent the LIN bus from being clamped to a dominant level. If the TxD input pin is not connected, for example due to a PCB crack, then the internal pull-up resistor on TxD to V_{ref} forces the LIN output stage to a recessive signal. Because of the recessive signal the communication on the LIN bus is undisturbed.

3.5 RxD1 & RxD2 pin

RxD1 & RxD2 are output pins. In Normal-operating mode the RxD output pin displays the data stream that is received from dedicated LIN channel. Because of the open drain output stage of RxD an external pull-up resistor to the microcontroller voltage is needed. A pull-up resistor of 2.4k is recommended. In Sleep Mode the RxD output pin is floating. **Figure 7** shows a typical RxD application.

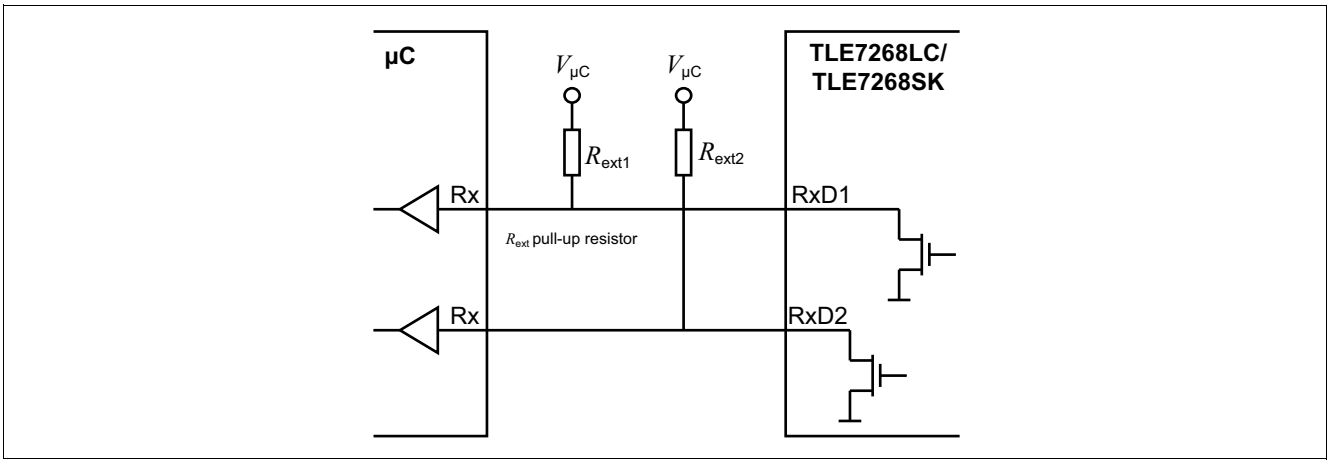

Figure 7 Typical RxD pin application

3.6 BUS1 & BUS2 pin

The BUS pin transmits and receives data on the LIN bus line. Internally a low side switch with controlled wave shaping transmits data, and the receiver receives data. The voltage threshold of the receiver V_{th} is battery related and has a hysteresis of V_{HYS}. The receiver thresholds, range and hysteresis fulfill the LIN 2.2A specification.

The BUS pin has a slave termination resistor R_{SLAVE}. The slave termination resistor as well as the low side switch use a reverse current diode. Thus no external components are required.

The BUS pin can withstand static voltage in the range of -27 V < V_{Bus} < 40 V for safe application usage. The BUS pin has a high ESD robustness and withstands voltage transients of +/- 10 kV according to IEC61000-4-2.

3.7 INH Pin

The INH pin can be used to indicate a wake-up to an external component or to control one or more external components as e.g. voltage regulator. The pin INH provides a V_S related open drain output. If TLE7268 enters Sleep Mode INH is High-Z. Common voltage regulators do have a pull-down resistor on the Inhibit input pin, which results in a “low” signal and switches off the voltage regulator. In case the voltage regulator does not have an internal pull-down resistor, an external pull-down at the INH pin of TLE7268 can be placed. In Normal Operation Mode and Stand-by Mode the pin INH is actively pulled to battery voltage V_S. The maximum current capability of INH pin is specified as 5mA.

4 Schematic and Layout recommendations

The following layout rules should be considered to achieve best performance of the transceiver and the ECU:

- keep TxD and RxD connections to microcontroller as short as possible.
- Place a 100 nF capacitor close from V_S to GND close to these pins for local decoupling. It is recommended to use a ceramic capacitor due to low ESR and low inductance.
- Do not route the LIN bus line in parallel to fast-switching lines or off-board signals in order to reduce noise injection to the LIN bus.
- It is recommended to place the master capacitor, slave capacitor and master termination resistor (only in master node) and the transceiver as close as possible together and close to the ECU connector in order to minimize track length of bus lines.
- Place the GND connector as close as possible to the transceiver in order to avoid ground shift and minimize impedance from ECU GND connector to TLE7268 GND.

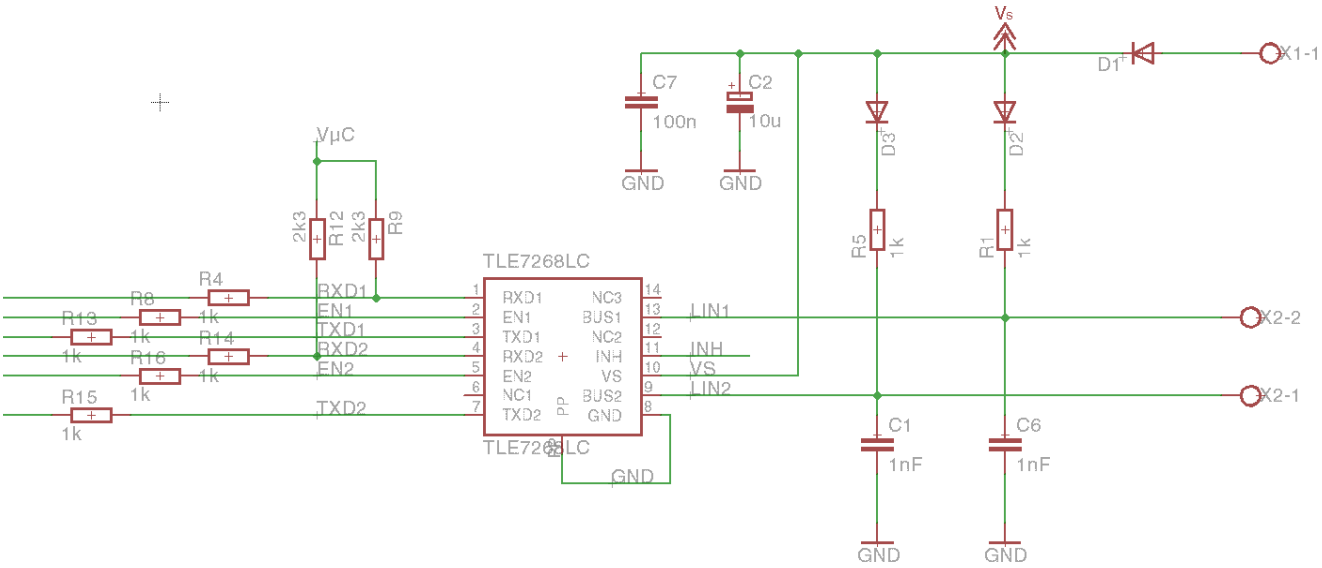

Figure 8 Example of TLE7268LC schematic

- R4, R8, R13, R14, R16, R15: Current limiting series resistors (optional)
- R12, R9: pull-up resistor for RxD1, RxD2 open drain output stages (recommended: 2.4k)
- R1, R5: LIN bus master pull-up termination (required only for LIN Bus Master)
- D2, D3: LIN bus master pull-up diodes (required only for LIN Bus Master)
- D1: Reverse battery protection diode
- C2, C7: V_S input stabilization capacitors (recommended)
- C1, C6: LIN bus capacitor (required for Master (1nF) and Slave (220 pF) applications)

5 Pin FMEA

This chapter provides a pin FMEA (Failure Mode and Effect Analysis) for typical failure situations. Typical failure scenarios for dedicated pins of TLE7268 are:

- short circuit to battery voltageV_S
- short circuit to PCB ground GND
- short circuit between neighboring pins
- unconnected pin

The potential failures are classified according to possible failure effects (see **Table 2**)

Table 2 Classification of failure effects

Class	Possible effects
A	- Transceiver damaged - LIN bus affected
B	- No damage to transceiver - No LIN bus communication on respective channel possible
C	- No damage to the transceiver - LIN Bus communication on respective channel possible - Affected node excluded from communication
D	- No damage to the transceiver - LIN bus communication on respective channel possible - Reduced functionality of transceiver

Table 3 Pin FMEA overview

Pin	Potential Failure	Potential Effects of Failure	Class
RxD1	open	No damage to the transceiver.	C
RxD1	Short Circuit to GND	No damage to the transceiver.	C
RxD1	Short Circuit to V_S	Violation of absolute maximum ratings. Device gets damaged.	A
RxD1	Short Circuit to EN1	Degradation RxD remains recessive.	C
EN1	open	No damage to the transceiver. Due to pull-down resistor LIN channel 1 will enter Sleep Mode.	C
EN1	Short Circuit to GND	No damage to the transceiver. LIN channel 1 will enter Sleep Mode.	C
EN1	Short Circuit to V_S	Violation of absolute maximum ratings. Device gets damaged.	A
EN1	Short Circuit to TxD1	No damage to the transceiver.	C
TxD1	open	No damage to the transceiver. Due to the internal pull-up resistor the TxD1 stays recessive.	C
TxD1	Short Circuit to GND	No damage to the transceiver. Transmitter is disabled after TxD dominant time-out. LIN1 bus communication blocked for t_{TXD_TO}. If failure does not recover transmitter will stay disabled and node cannot transmit data to the LIN1 bus. The receiver works as specified in the datasheet.	C
TxD1	Short Circuit to V_{BAT}	Violation of absolute maximum ratings. Device gets damaged.	A
TxD1	Short Circuit to RxD2	No damage to the transceiver. Both channel get affected.	C
RxD2	open	No damage to the transceiver.	C

Table 3 Pin FMEA overview (cont'd)

Pin	Potential Failure	Potential Effects of Failure	Class
RxD2	Short Circuit to GND	No damage to the transceiver.	C
RxD2	Short Circuit to V_S	Violation of absolute maximum ratings. Device gets damaged.	A
RxD2	Short Circuit to EN2	Degradation RxD remains recessive.	C
EN2	open	No damage to the transceiver. Due to pull-down resistor LIN channel 1 will enter Sleep Mode.	C
EN2	Short Circuit to GND	No damage to the transceiver. LIN channel 1 will enter Sleep Mode.	C
EN2	Short Circuit to V_S	Violation of absolute maximum ratings. Device gets damaged.	A
EN2	Short Circuit to N.C.	No damage to the transceiver.	D
TxD2	open	No damage to the transceiver. Due to the internal pull-up resistor the TxD1 stays recessive.	C
TxD2	Short Circuit to GND	No damage to the transceiver. Transmitter is disabled after TxD dominant time-out. LIN2 bus communication blocked for t_{TXD_TO}. If failure does not recover transmitter will stay disabled and node cannot transmit data to the LIN2 bus. The receiver works as specified in the datasheet.	C
TxD2	Short Circuit to V_{BAT}	Violation of absolute maximum ratings. Device gets damaged.	A
GND	open	No damage to the transceiver. Transceiver stays unsupplied and is passive to the HS CAN Bus.	C
GND	Short Circuit to V_{BAT}	No damage to the transceiver. Transceiver stays unsupplied and is passive to the HS CAN Bus.	C
GND	Short Circuit to BUS2	BUS2 is permanently dominant, no data transfer possible	B
BUS2 (LIN2)	open	No damage to the transceiver. LIN 2 channel excluded from communication.	C
BUS2 (LIN2)	Short Circuit to GND	Degradation of BUS2 output stage as if driven "recessive". BUS2 output stage may be damaged. No bus communication possible.	A
BUS2 (LIN2)	Short Circuit to V_{BAT}	No bus communication possibleDegradation of BUS2 output stage as if driven "recessive". BUS2 output stage may be damaged.	B
V_S	open	No damage to the transceiver. Transceiver stays unsupplied and is passive to the HS CAN Bus.	C
V_S	Short Circuit to INH	No damage of the transceiver	D
INH	open	No damage of the transceiver	D
INH	Short Circuit to GND	Violation of absolute maximum ratings. Device gets damaged.	A
INH	Short Circuit to V_S	INH functionality is not available.	C
BUS1 (LIN1)	open	No damage to the transceiver. LIN 2 channel excluded from communication.	C
BUS1 (LIN1))	Short Circuit to GND	Degradation of BUS1 output stage as if driven "recessive". BUS1 output stage may be damaged. No bus communication possible.	A
BUS1 (LIN1)	Short Circuit to V_{BAT}	No bus communication possibleDegradation of BUS1 output stage as if driven "recessive". BUS1 output stage may be damaged.	B

Terminology

LIN	Local Interconnect Network
OEM	Original Equipment Manufacturer
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
PCB	Printed Circuit Board

6 References

[1] Data Sheet TLE7268, LIN Transceiver, Infineon Technologies AG

[2] LIN Specification Package, LIN Protocol Specification - Revision 2.2a,
LIN Consortium; ISO 17987-4

[3] International Standard ISO 9141, Road Vehicles - Diagnostic Systems - Requirement for Interchange of Digital Information, International Standardization Organization, 1989

[4] **Infineon Automotive Transceiver Homepage**

7 Revision History

Revision	Date	Changes
1.0	2017-07-26	Application Note created

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