

# Recommendations for HS CAN Transceivers

Electrostatic Discharge (ESD)

Electromagnetic Compatibility (EMC)

PCB Layout

## HS CAN Transceiver

Z8F54492107

## Application Note

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Automotive Power



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## Summary

# 1 Summary

This document provides application information for the HS CAN transceivers from Infineon Technologies AG for Electrostatic Discharge (ESD) and Electromagnetic Compatibility (EMC).

### Electrostatic Discharge

Among all the disturbances a CAN transceiver can encounter in a vehicle, the ESD discharge is one of the most critical. In case of an ESD event a very high current flows into the CAN-transceiver. ESD tests on system level can lead a lot of confusion because the results are not always unique and reproducible. For a better understanding of this phenomenon, this document provides technical information and hints for Electrostatic Discharge (ESD). Infineon HS CAN transceivers have a very high ESD robustness, which allows to use the transceiver in most applications.

### Electromagnetic Compatibility

Electromagnetic compatibility becomes more and more important for vehicle manufacturers. There are defined emission limits which have to be fulfilled to pass OEM requirements. The Electromagnetic Emission (EME) mainly depends on the falling and rising edge of the CANH and CANL waveforms. Infineon HS CAN transceivers are developed to achieve the smoothest possible waveform on the market and fulfill or exceed OEM EMC requirements.

### PCB Recommendations

In order to achieve best performance of a HS CAN transceivers and also applications, this document provides major PCB layout recommendations.

This document refers to all HS CAN transceivers of Infineon Technologies AG, especially to:

- TLE7250SJ and TLE7250LE
- TLE7250VSJ and TLE7250VLE
- TLE7250XSJ and TLE7250XLE
- TLE7251VSJ and TLE7251VLE

*Note: The following information is given as a hint for the implementation of our devices only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

## 2 ESD Hints

There are several test standards to prove that semiconductor devices can overcome the always present challenge of electrostatic discharge (ESD). But ESD tests on system level can generate a lot of confusion because the results are not always unique and reproducible. This comes from big deviations in the resulting current waveform from one ESD test to another because of many influencing factors (e.g. ESD tester, discharge network, ambient temperature, air humidity, angle between GUN and PCB, position of discharge return cable...) [1] [2]. To get as much reproducibility as possible into your measurements you have to keep these factors constant during your measurements. You can try to reproduce ESD test results afterwards but it is not necessarily possible even if the specific parameters reproduced as detailed as possible.

### 2.1 ESD test targets

ESD tests divide the world into component level and system level. Component level tests should assure that semiconductor devices survive handling during manufacturing, testing and assembly. By contrast system level tests are designed to prove that systems can withstand ESD in the real operational world. Because of these very different requirements the two tests strongly vary in the discharge current waveform. As you can see in the chart below according to the variations of the current waveform the requirements of component- and system-level ESD test are very different.

Don't be confused if there is talk of currents on the y-axes in case of ESD test and you expected voltages because a certain ESD test voltage is linked to a certain peak current of the discharge.

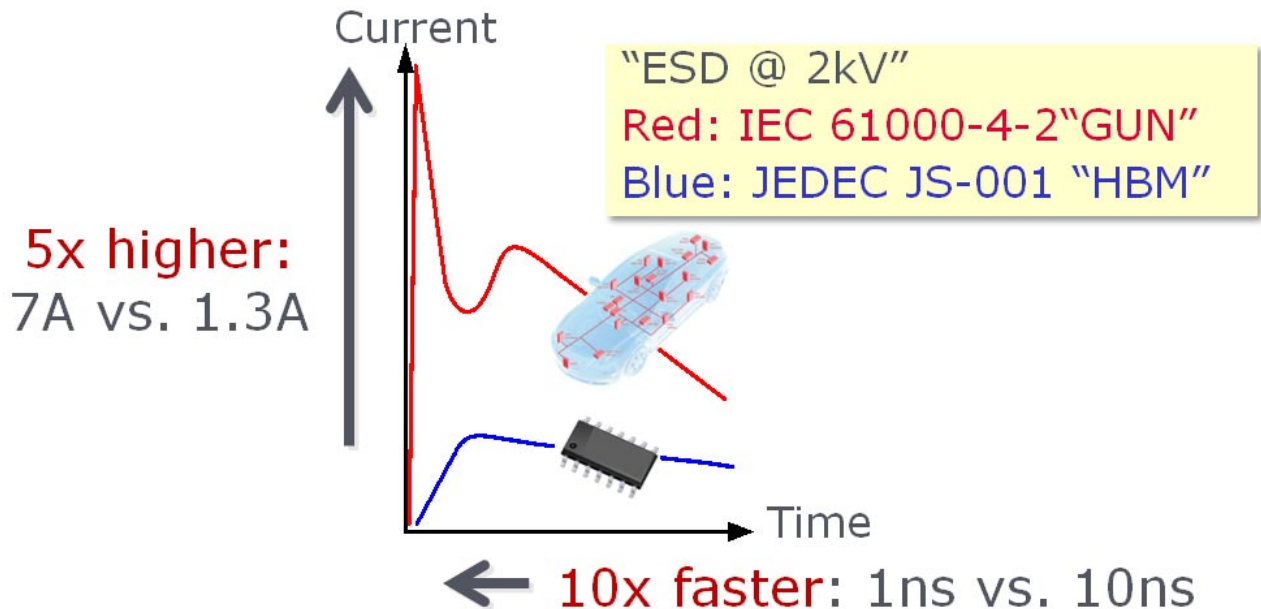


Figure 1 Difference between component-level (HBM) and system level (GUN) test standards

### 2.1.1 Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001

The most accepted component level test within electronics industry is the HBM test (Human Body Model) according to ANSI/ESDA/JEDEC JS-001. This standard simulates a charged human body by a 100 pF capacitor and discharging it into a device under test (DUT) through a 1500  $\Omega$  resistor which emulates skin.

For electronic systems HBM robustness level is not crucial because this model is just valid for handling in an electrostatic protected area (EPA) where relatively low ESD pass values are required. But systems consisting of components are handled in real world outside of EPA. Furthermore high HBM robustness does not necessarily result in high system-level robustness as several studies have proven, e.g. of the Industry Council on ESD target levels [4].

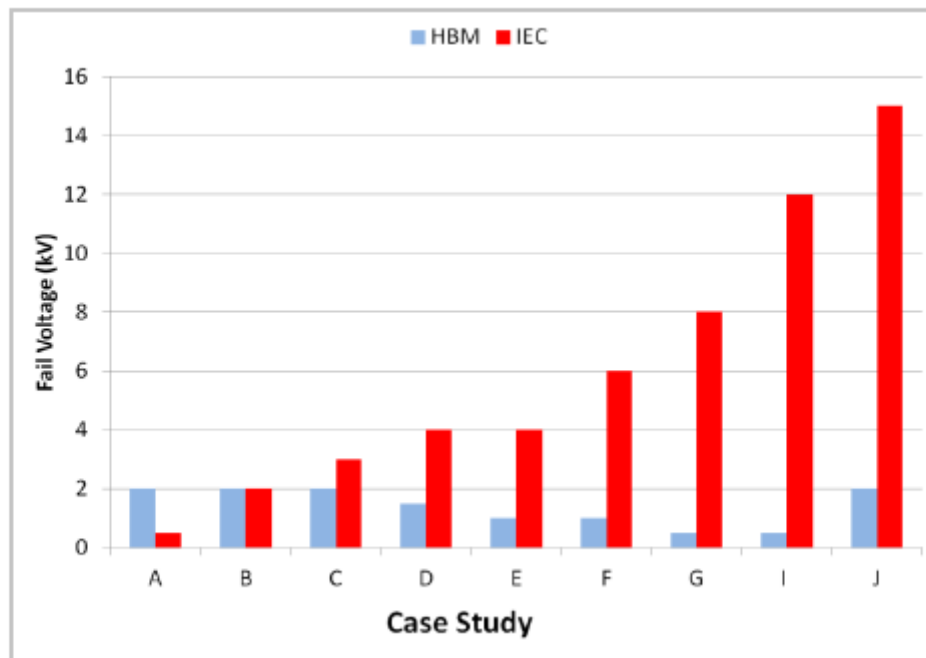


Figure 2 Comparison of component-level and system-level ESD robustness of various system (A-J) [4]

### 2.1.2 Gun Test according to IEC 61000-4-2 or ISO 10605

For system level ESD tests there are two quite similar standards, which are widely accepted IEC 61000-4-2 and ISO 10605. These tests should simulate a charged human touching an electronic system through a metallic object by a 150 pF capacitor discharged via a 330  $\Omega$  resistor into the equipment under test (EUT). Special focus is on detection of system disturbances due to ESD. This test method is called GUN test because the ESD tester usually has the shape of a gun. The test is performed on pins which leave the board via a connector and is tested vs. GND. Those pins are called global pins. Typically transceiver pins (CANH, CANL), supply pins (VBAT) or other control pins (WAKE) are global pins. A pin which does not leave the board is called local pin.

At GUN tests there is by contrast to HBM not only direct discharge into the device under test (DUT) but also indirect discharge into an object near the EUT or cable harness. In case of direct discharge the DUT is tested for destruction in contrast to the disturbance test of a system in case of indirect discharge. Air discharge is additionally a direct discharge to the DUT with the possibility of an electric arc between GUN and DUT.

## ESD Hints

### 2.2 ESD protection

There are two basic concepts of ESD protection. Quite often seen is a breakdown behavior of ESD protection structures. Another solution is a so called snap-back behavior. Both have their benefits and drawbacks and both are being used in the industry. ESD protection in general is a high-ohmic device up to the trigger-voltage. Above this voltage the device provides a low-ohmic path to GND and can carry a few amperes for a short period of time (typically 100-200ns).

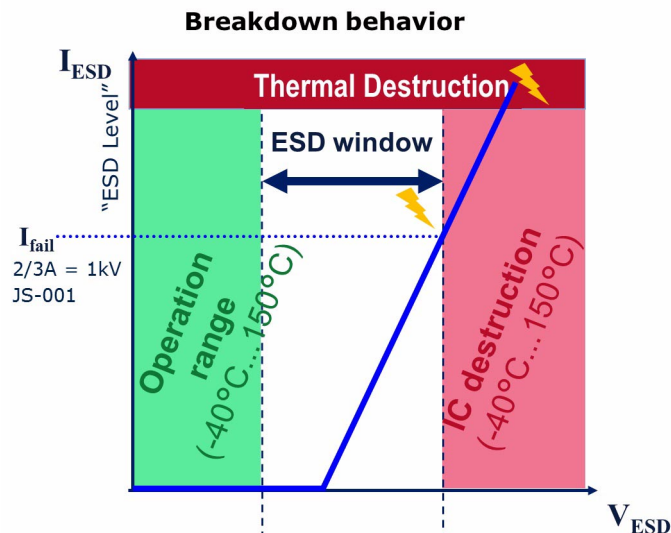


Figure 3 Breakdown ESD structure

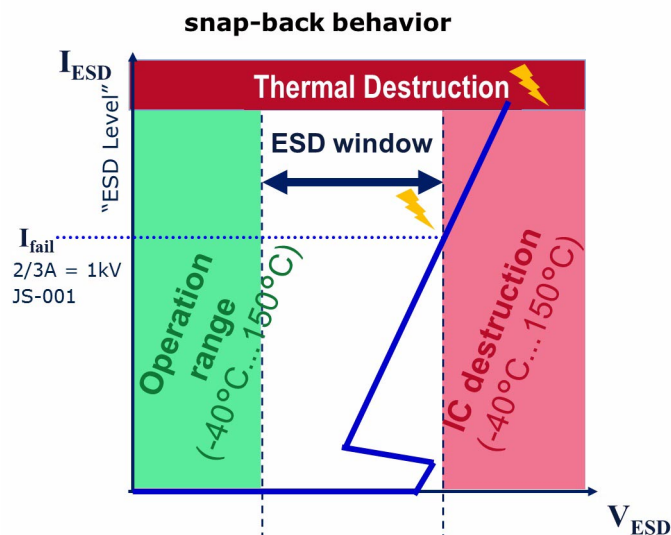


Figure 4 Snapback ESD structure

To avoid accidental triggering of the ESD protection during normal operation it is necessary not to exceed AMR (Absolute Maximum Rating) in the application. Otherwise the ESD device tries to shunt the current with a very low-ohmic path to ground and can be destroyed if the energy is too high.

## ESD Hints

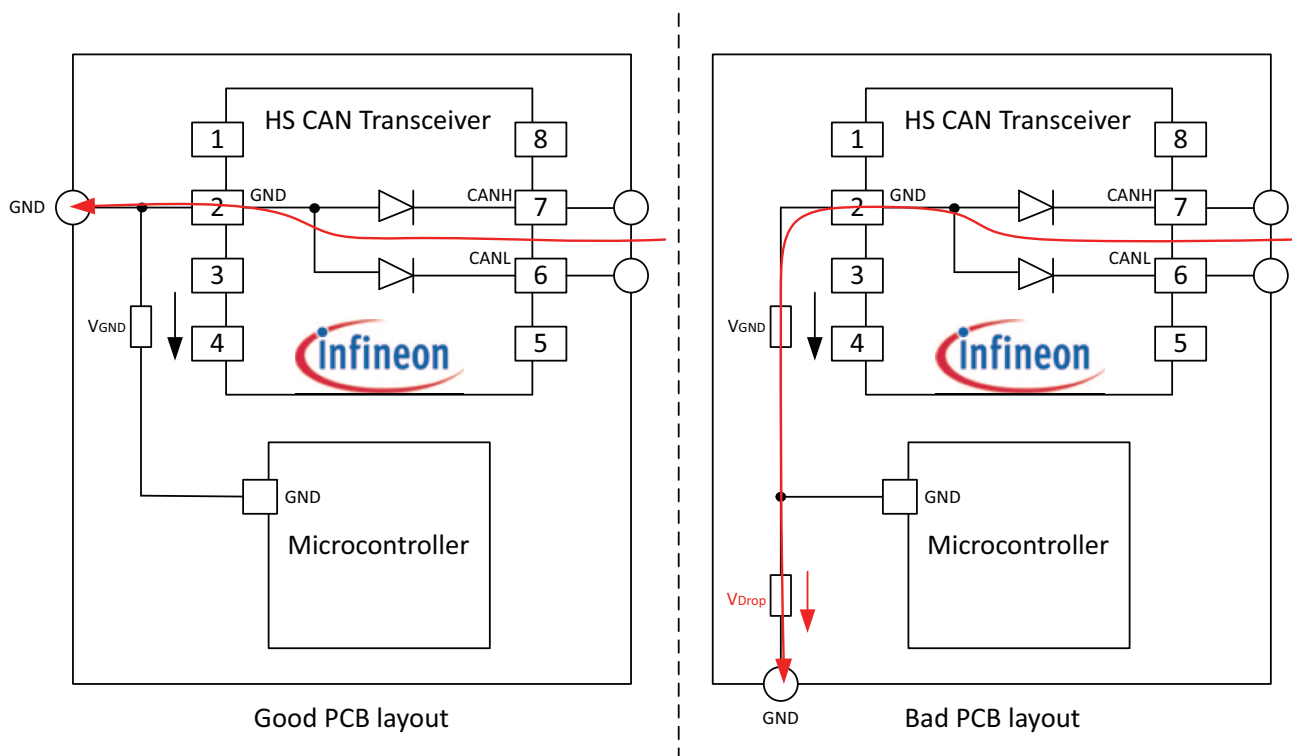
### 2.3 PCB layout

At first sight PCB layout might have nothing to do with ESD but system-level ESD addresses the whole system. This includes not only the single devices but also the connection between the devices.

First of all this chapter shows some grounding recommendations. The ground of the device is not necessarily at the same potential as GND connector of the board. In case of ESD a high current up to several amperes is flowing which leads to a voltage drop of a few volts even across resistances below  $1\ \Omega$ . This can cause different voltage potentials at different GND points on the PCB.

In order to pass the ESD tests it is also very important to create an appropriate, well-evaluated PCB layout. [Figure 5](#) shows a typical case where ESD discharge becomes an issue for the module.

In this case the GND connector is situated far away from the transceiver and with the digital components as microcontroller in between, the GND line resistance cannot be neglected. ESD discharge on CANH or CANL can cause voltage shift on the GND pin of the microcontroller and easily destroy the device. Therefore it is important to place the GND connector as close as possible to the transceiver.



**Figure 5** Good and bad PCB layout example

## ESD Hints

### 2.4 On-Chip vs. Off-Chip Protection

Although Infineon HS CAN transceivers have implemented system level ESD protection up to  $\pm 8$  kV according to 03/02/IEC TS62228 (DIN EN61000-4-2), it is often a system requirement to withstand  $\pm 15$  kV or even more. To reach this goal an additional external ESD protection structure is necessary. Interactions between the protection elements is sometimes difficult to predict. All parasitic resistances and inductances of the PCB traces and all components in the ESD current path have to be taken into account, e.g. as a via only can have an inductance of 0.5 nH.

Attention should be paid on the trigger characteristics of internal and external protection devices. Both trigger voltages have to be higher than the maximum operating voltage  $V_{op,max}$  of the application to avoid accidental triggering during normal operation. Furthermore the clamping voltage  $V_{clamp}$  at the demanded ESD current  $I_{IEC-Pulse}$  has to be below the destructive voltage of the on-chip protection  $V_{t2,IC}$ . Otherwise the IC can be destroyed during ESD.

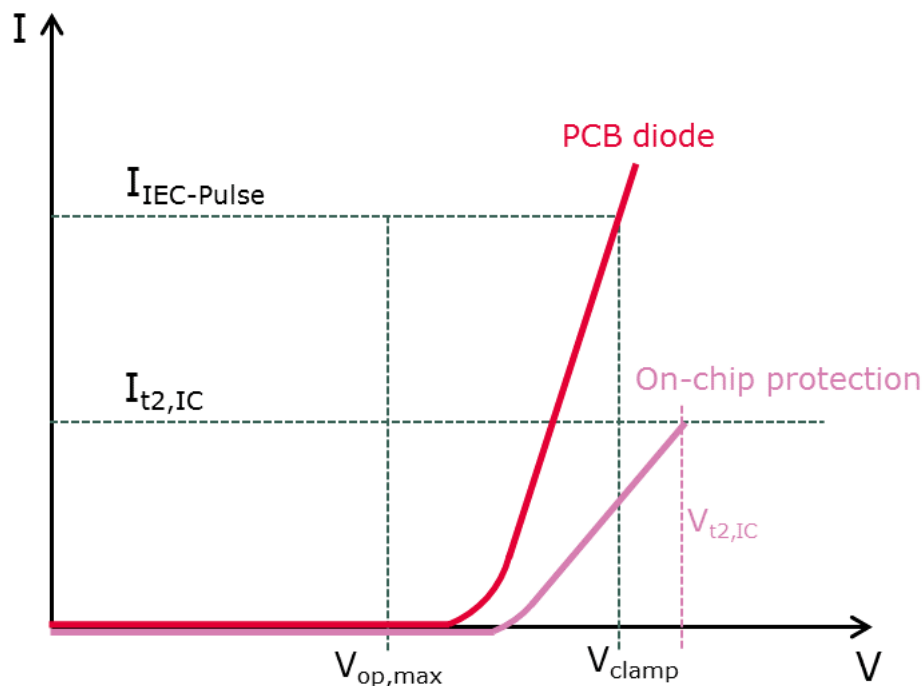


Figure 6 Internal and external ESD protection



### 3 EMC Aspects

The CAN physical layer is a dual-wire bus with a  $V_{CC}/2$  related recessive level. Smooth output wave shaping is very important. Electromagnetic Emission (EME) mainly depends on the falling and rising edge of the CAN bus waveforms. Smooth edges reduce the EME reduction. For the PCB layout it is recommended to keep the same dimensions and lengths for all bus wire connections from the transceiver to Common Mode Choke (CMC) and/or termination. Usage of Common Mode Choke and type of termination depend on the application and OEM requirements.

#### 3.1 Common Mode Choke

The Common Mode Choke (CMC) is the first interference suppression in CAN networks in order to reduce EME. It attenuates noise which is common to CANH and CANL. A CMC increases Common Mode Rejection Ratio (CMRR) and provides high impedance for common signals, when the bus is in recessive state. Additionally the CMC provides low impedance for differential signals, when the bus is in dominant state. The CMC dampens differential mode interference, which may be injected by split termination. The inductance of the common mode choke should be as low as possible in order to avoid high shutdown peaks.

#### 3.2 Split Termination

Split termination reduces EME and improves EMI. The split termination circuit is a modified standard termination and consists of two equal value split resistors ( $R_{Split} = 60 \Omega$ ) and a bypass capacitor ( $C_{Split} = 4.7 \text{ nF}$ ) tied between the resistors and GND. The two resistors and the capacitor work as a low-pass filter with a cut off frequency of  $f = 1/(2 \times \pi \times R_{Split} \times C_{Split})$ . A common mode signal is terminated to GND through the  $C_{Split}$ . In result high frequency noise will be directly shunted to ground. The two resistors should match as closely as possible.

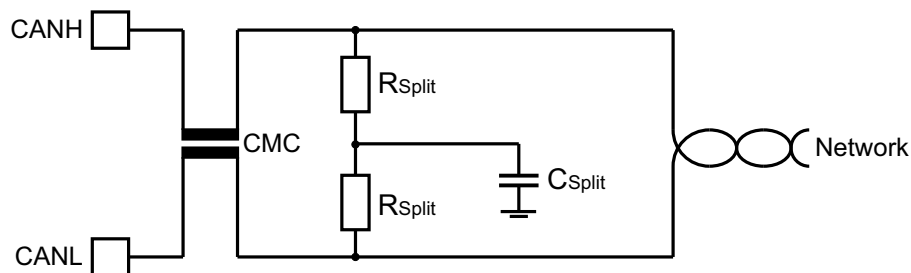


Figure 7 Split termination

## EMC Aspects

### 3.3 Biased Split Termination

A split biased termination is recommended to reduce EME. The best performance can be achieved by connecting  $V_{CC}/2$  between the two split resistors. This method is used to maintain the common mode recessive voltage at a almost constant level in order to improve EMC performance. The biased split termination circuit is the same as the standard split termination with the addition of a voltage divider of  $V_{CC}/2$  between the two split termination resistors. Recommended value of  $R_K = 1.3 \text{ k}\Omega$ . The two resistors  $R_K$  should match as closely as possible.

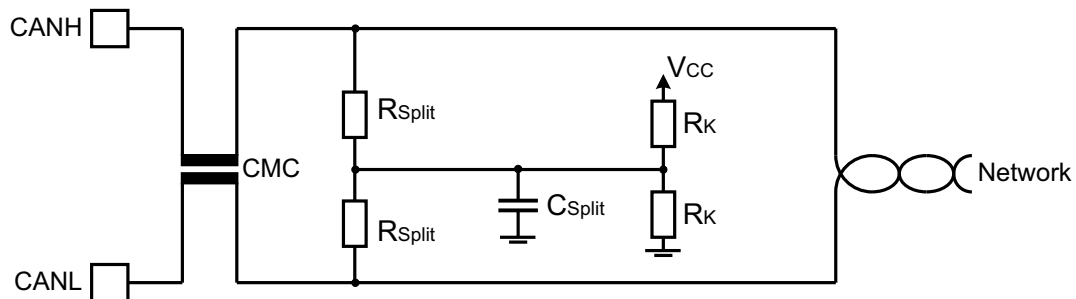


Figure 8 Biased Split termination

### 3.4 Stabilization Capacitors

For HS CAN applications it is recommended to use stabilization capacitors at  $V_{CC}$  voltage supply input and  $V_{IO}$  reference supply input in order to support the robust performance of the CAN transceiver. It is important to place the stabilization capacitor  $C_1$  and  $C_2$  as close as possible to the  $V_{CC}$  and  $V_{IO}$  pins. The recommended value for the stabilization capacitor of the voltage supply  $V_{CC}$  is in the range of 47 nF to 100 nF. The recommended value for the stabilization capacitor of the reference supply  $V_{IO}$  is in the range of 47 nF to 100 nF. Due to their low resistance and lower inductance compared to other capacitor types, it is recommended to use ceramic capacitors.

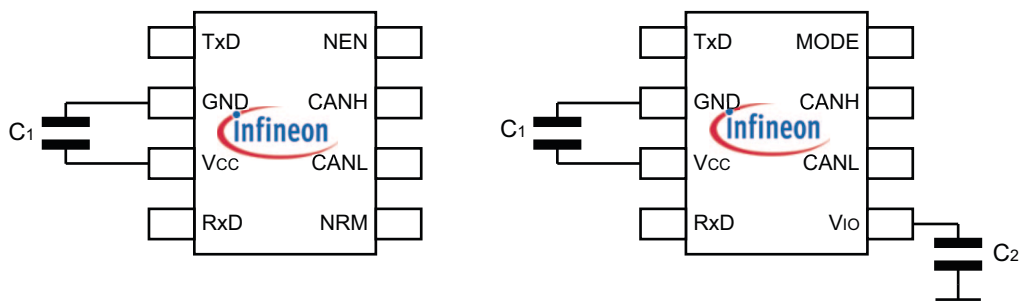


Figure 9 Stabilization Capacitors

## 4 PCB Layout Recommendations

The following rules should be considered to achieve best performance of the transceiver and the ECU:

- It is recommended to place the transceiver as close as possible to the ECU connector in order to minimize track length of bus lines.
- TxD and RxD connections to microcontroller should be as short as possible.
- Place two individual 100nF capacitors close to  $V_{CC}$  and  $V_{IO}$  pins. Due to their low resistance and lower inductance compared to other capacitor types, it is recommended to use ceramic capacitors.
- In case a CMC (common mode choke) is used, it has to be placed as close as possible to the transceiver bus pin CANH and CANL.
- Avoid routing CANH and CANL in parallel to fast-switching or off-board signals in order to reduce noise injection to the bus.
- Avoid routing digital signals in parallel to CANH and CANL.
- CANH and CANL tracks should have the same length. They should be routed symmetrically close together with smooth edges.
- For high current applications the current should not flow through the GND line of transceiver and microcontroller in serial.
- Same dimensions and lengths for all wire connections from the transceiver to CMC and/or termination.
- Avoid routing transceiver GND and microcontroller GND in serial. GND connector should be placed as close as possible to the transceiver.

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References

## 5 References

- [1] F. zur Nieden, B. Arndt, J. Edenhofer, S.Frei: Vergleich von ESD-System-Level Testmethoden für Packaging und Handling, ESD Forum 2009
- [2] Jayong Koo, Qing Cai, David Pommerenke, Kai Wang, John Mass, Masayuki Hirata, Andrew Martwick: The repeatability of system level ESD test and relevant ESD generator parameters, 2008, Faculty Research & Creative Works - Paper 1509
- [3] Industry Council on ESD Target Levels: White Paper 3 - System Level ESD - Part I: Common Misconceptions and Recommended Basic Approaches, 2010
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## 6 Revision History

Revision	Date	Changes
1.0	2015-10-26	Application Note created

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