XMC1302

32-bit Microcontroller Series for Industrial Applications

Server Fan Control Reference Design

AP32294

Application Note

About this document

This document is designed for the low voltage server fan motor drive application and based on XMC1302. This application is designed to implement sensorless FOC drive to minize the server fan motor vibration effect.

Scope and purpose

To show how to implement the control with XMC1302 microcontroller to drive BLDC and PMSM server fan motor with Sensorless Field Oriented Control.

Intended audience

Server Fan motor manufacturers and design engineers who intend to reduce the system cost, improve efficiency, and shorten the application development cycle.

Applicable Products

- XMC1302
- BSL308C
- BC848W
- IFX20001MB
- DAVE ™

References

The User's Manual can be downloaded from http://www.infineon.com/XMC.

DAVE™ and its resources can be downloaded from http://www.infineon.com/DAVE

Table of Contents

1 Introduction

The Infineon 'Server Fan Reference Design' is a complete solution for a low-voltage fan motor drive application (a BLDC and PMSM server fan motor), with low noise, minimal motor virbration, and a very low external component count. This application is typically used to supply cooling air to electronic equipments.

The compact design is based around the Infineon 32-bit ARM® Cortex ™ XMC1302 microcontroller with ready-to-use sensorless Field Oriented Control (FOC) firmware to support fast implemention into exisiting development platforms. The XMC1302 is a low-cost, high-performance microcontroller, and has flexible ADC features, Capture Compare Units (CCU4/8), and a Math Co-processor.

The PCB layout has a unique 'coin concept'. The spacing on the PCB board is ultilized with surface mount components which results in lower BOM costs:

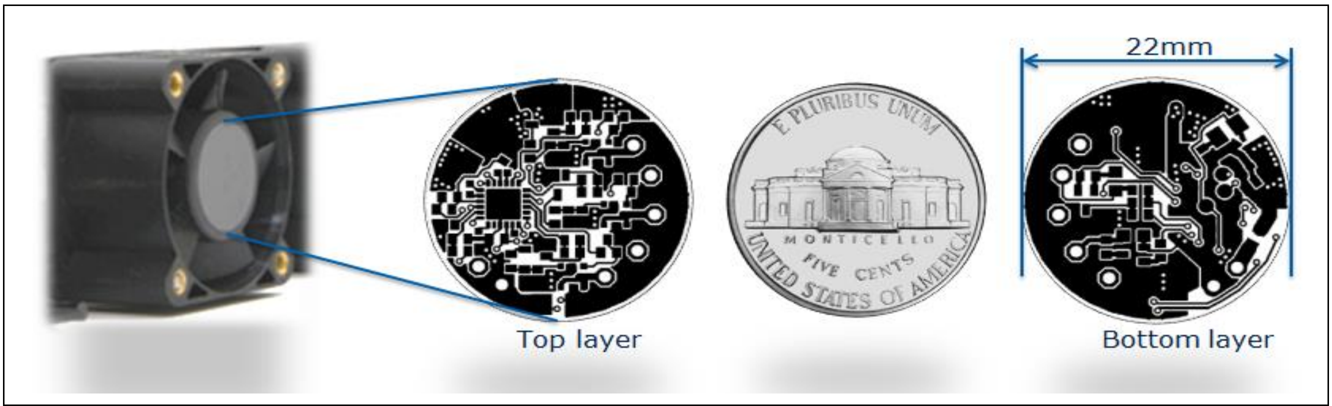


Figure 1 Server Fan PCB layout Coin Concept

1.1 XMC1302 Key Features

The XMC1302 is a low-cost microcontroller, optimized for motor control applications.

Package types

- TSSOP-16
- VQFN-24
- TSSOP-28
- TSSOP-38
- VQFN-40

XMC1302 as a controller for various types of motor

- Permanent Magnet Synchronous Motors (PMSM)
- Brushless DC Motors
- AC Induction Motors (ACIM)
- Servo Motors
- Brushed DC Motors

Key features

- High performance 32-bit Cortex-M0 CPU
- MATH Co-processor (MATH), consists of a CORDIC unit for trigonometric calculation and a division unit
- On-Chip Memories, 16 kbytes on-chip high-speed SRAM, up to 200 kbytes on-chip Flash program and data memory
- 12 channels 12-bit ADCs with hardware trigger
- Built-in Temperature Sensor
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Capture/Compare Units 8 (CCU8) for motor control PWM generation
- Watchdog Timer (WDT) for safety sensitive applications

2 Reference Design Target Requirements

The reference design is intended to meet common server fan application specifications:

Table 1 Reference Design Requirements

Item	Requirement
Motor Type	3 Phase PMSM motor
Motor Pole Pair	2 pp
Motor Resistance (per phase)	1.1 ~ 1.2 Ω
Motor Inductance (per phase)	293 ~ 302 uH (10 kHz)
PCB Layout Diameter	22 mm
Operating Voltage	12 V
Current Rating	1.00 A
Power Rating	12 W
Speed	0 to 25000 rpm
Fault Detection	Lock, reverse polarity
Over Current	Yes
Control Interface	POT / PWM input / FG Output
Control Algorithm	Field Oriented Control
Microcontroller	XMC1302 TSSOP16/VQFN24

Note: All test waveforms are captured and shown later in this document.

3 System Block Diagram

The hardware can be dvided into four parts:

- Microcontroll (MCU)
  - The MCU consists of an XMC1302 ARM® Cortex ™ with single-shunt Field Oriented Control (FOC) algorithm. It is used to control high-side and low-side transistors with adjustable dead-time.
- MOSFET stage
- Control interface
- Voltage regulator

This reference design uses ADC for current measurement with integrated gain in the XMC1302 microcontroller.

A two-wire SWD or single-wire SPD debugging interface is supported.

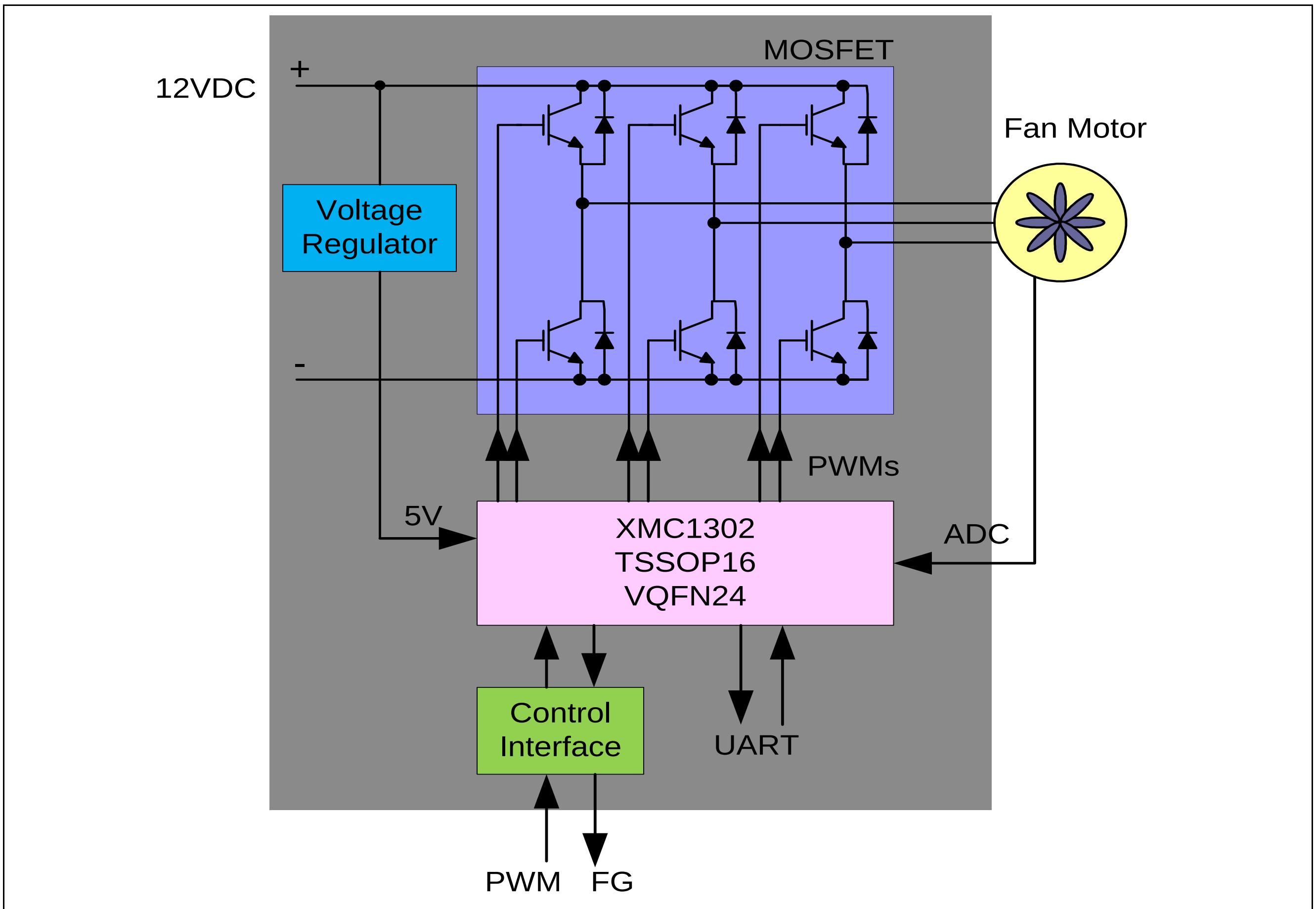


Figure 2 System Block Diagram

4 Motor Drive Features

The major requirements of server fan applications are for low audible noise and high efficiency. To boost the efficiency, design engineers need a means to offset the higher cost of a 3-phase fan motor compared to a single or dual-phase fan motor.

Most server fan motors are based on a 3-phase Brushless DC (BLDC) motor and Permanent Magnet Synchronous Motor (PMSM). While BLDC and PMSM motors have always been preferred for performance (efficiency, noise, starting torque), a complex and robust sensorless motor control algorithm is required.

4.1 Infineon Sensorless FOC algorithm with XMC1302

- Fast execution with hardware Math co-processor
- Optimized FOC block, without Inverse Park Transform
- Optimized Space Vector Modulation (SVM) using internal amplifier for single-shunt current sensing
- One single CORDIC calculation for Space Vector Modulation (SVM)
- Smooth and low-power start-up

5 Hardware Design

This reference design hardware includes single-shunt current measurement. The operating supply voltage of the hardware is 10V to 30V. It supports up to 25 kHz PWM switching frequency.

5.1 Form Factors

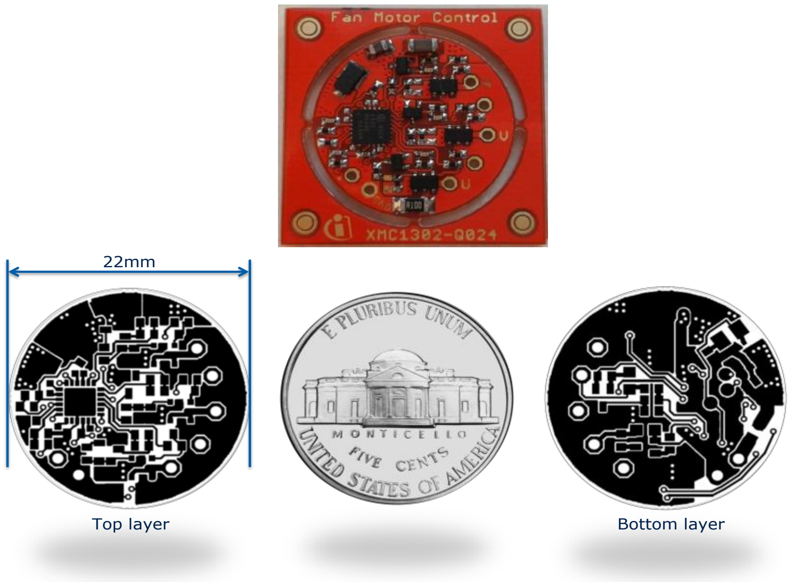


Figure 3 Diameter 22 mm with 2 layer Circular PCB layout

5.2 Pin Mapping

			XMC1302-VQFN24
S/N	**Signal**	**Description**	**1-Shunt, CoinInverter**
1	HO1	High side drive for Phase U MOSFET	P0.0 (CCU80.OUT00)
2	LO1	Low side drive for Phase U MOSFET	P0.5 (CCU80.OUT01)
3	HO2	High side drive for Phase V MOSFET	P0.7 (CCU80.OUT10)
4	LO2	Low side drive for Phase V MOSFET	P0.6 (CCU80.OUT11)
5	HO3	High side drive for Phase W MOSFET	P0.8 (CCU80.OUT20)
6	LO3	Low side drive for Phase W MOSFET	P0.9 (CCU80.OUT21)
7	IDC+	ADC for DC link current sensing	P2.7 (G1.CH1)
8	DC_LINK_DIV	Voltage of DC link (with voltage divider)	P2.2 (G0.CH7)
9	IN (PWM)	PWM duty cycle for speed adjustment	P1.1 (CCU40.IN1L)
10	OUT (FG/RD)	Voltage of DC link (with voltage divider)	P1.2 (CCU40.OUT2)
11	Debug	SWDIO_0 / SPD_0 / RX	P0.14
12	Debug	SWDCLK_0 / TX	P0.15

Figure 4 XMC1302 VQFN Pin assignment

5.3 Microcontroller Motor Control Ports

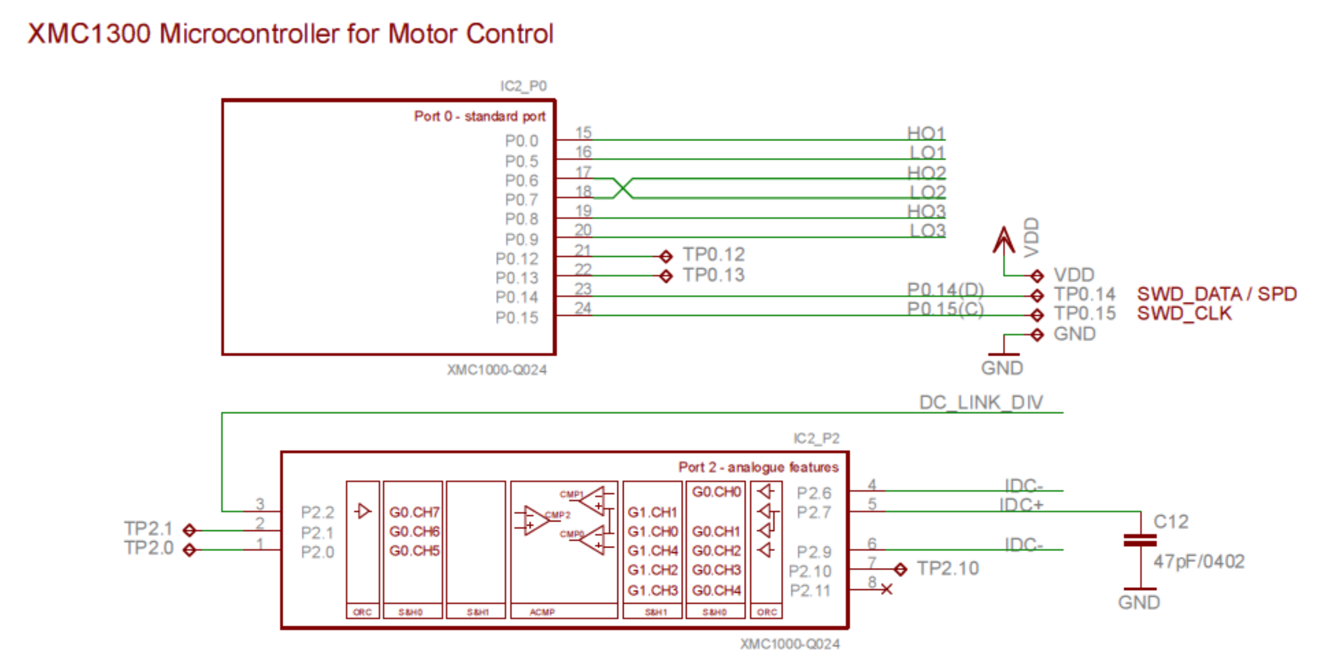


Figure 5 XMC1302 Motor Control Ports

Highlights

- XMC1302 ARM® Cortex ™ - M0 32-bit microcontroller for motor control.
- Control of High-side and Low-side transistors with dead-time.
- ADC current measurement with adjustable gain.
- Support debug interface which includes two wire SWD or 1 wire SPD.
  - The non-isolated debug interface pins are connected directly to the controller.
- No external crystal or resonator is required. This helps for small size PCB layout.

5.4 MOSFET Stage

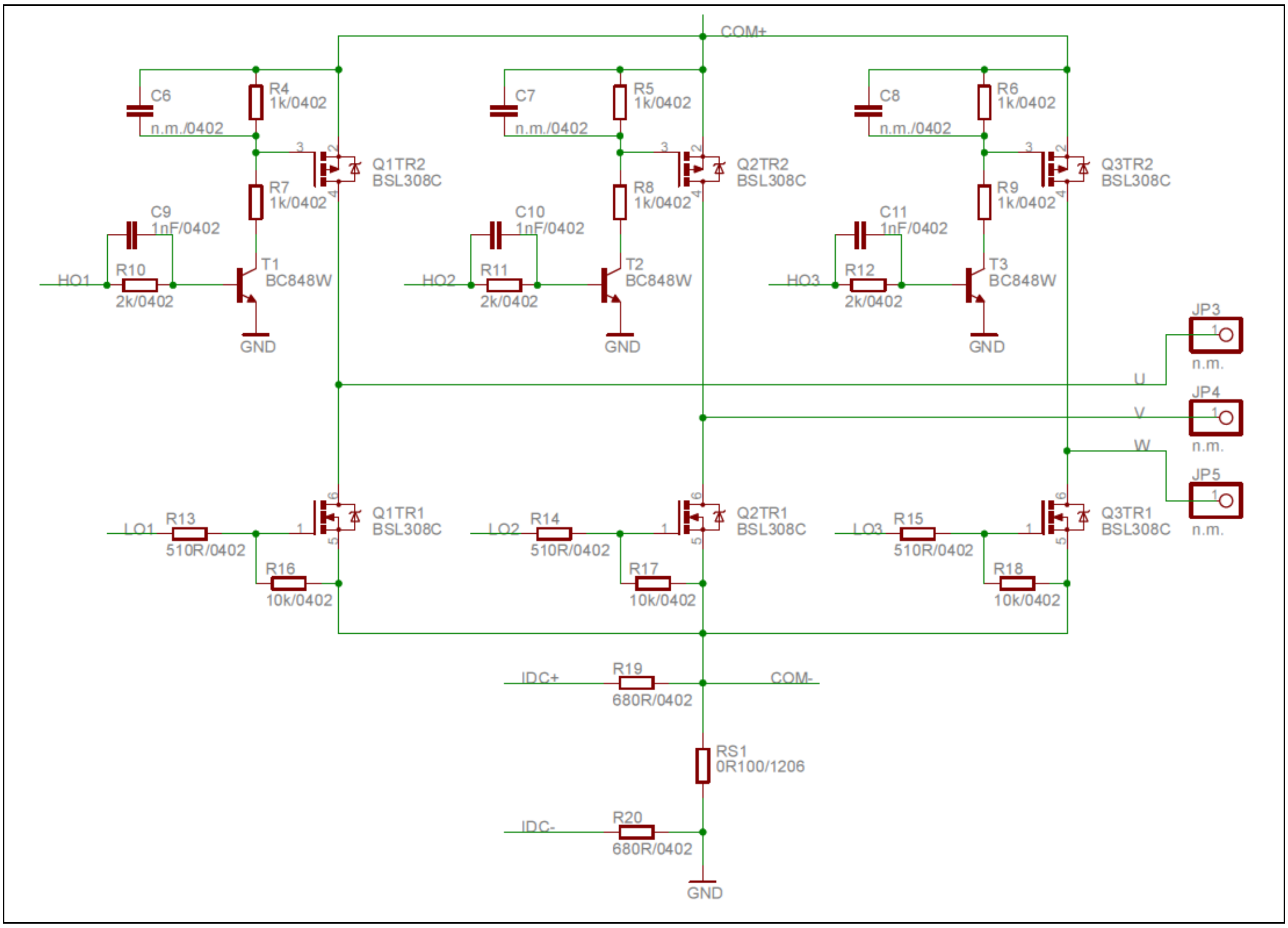


Figure 6 High Side and Low Side MOSFET circuitry

Highlights

- Dual MOSFET switching with enhanced High-side driver circuitry.
- Direct drive of Low-side MOSFET.
- Single Shunt current sensing measurement.

5.5 Microcontroller Control Interface

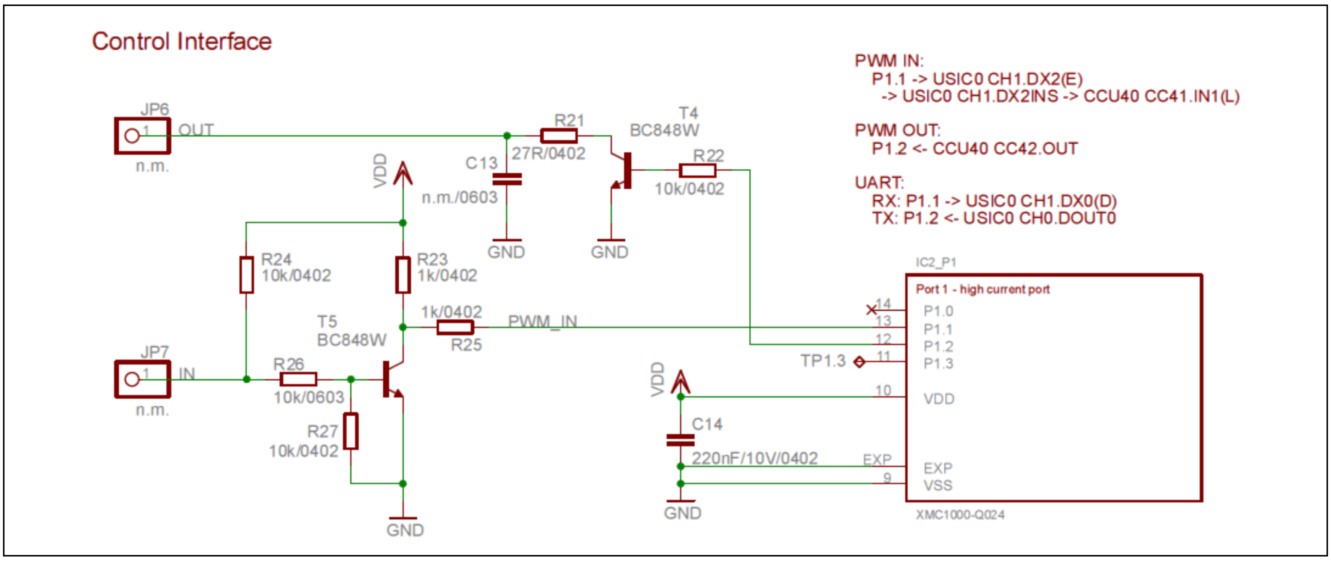


Figure 7 Interface circuitry with XMC1302

Highlights

- Speed control with PWM input including 12V level shifter.
- FG output with open collector circuitry for use in 12V domain.
- Two independent UART channels (RXD/TXD) with 12V level shifter (optional).

5.6 Power Supply

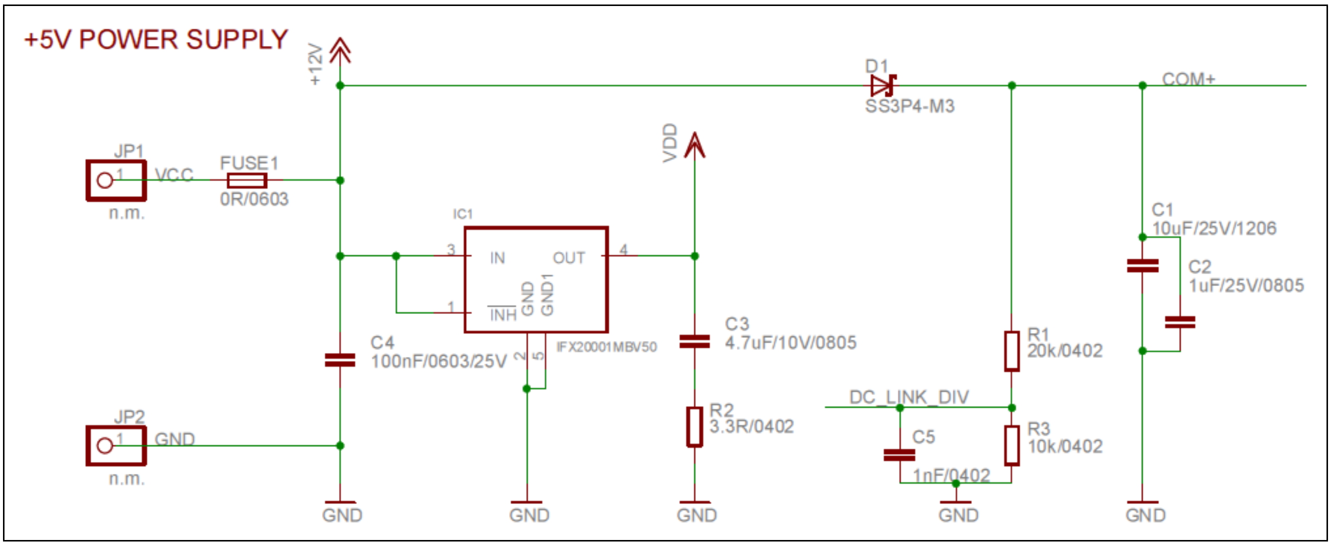


Figure 8 Low Dropout Power Supply

Highlights

- IFX20001MBV5 in small package SCT-595.
- Input voltage range up to 45V.
- Output voltage 5V, output current 30mA.
- Protection functions include over-temperature protection, and reverse polarity protection.
- Wide temperature range -40 ˚C ≤ Tj ≤ 125 ° C.

6 Software State Machine

The Infineon Server Fan Control Reference Design software provides the following life-cycle states:

- Brake
  - When the board is powered on, braking is applied for position alignment.
- Start-up
  - The motor will start based on the voltage applied.
- Ramping
  - It performs speed adjustment (ramp-up or ramp-down).
- Transition
  - Maximum Efficiency Tracking (MET) is applied to increase transition from open loop to closed loop stability.
- Stop/Trip Protection
  - If any over-current protection is triggered, the motor will stop or stop-restart the operation.
- FOC PLL Observer
  - Closed loop algorithm to estimate the rotor position based on single shunt current feedback measurement.

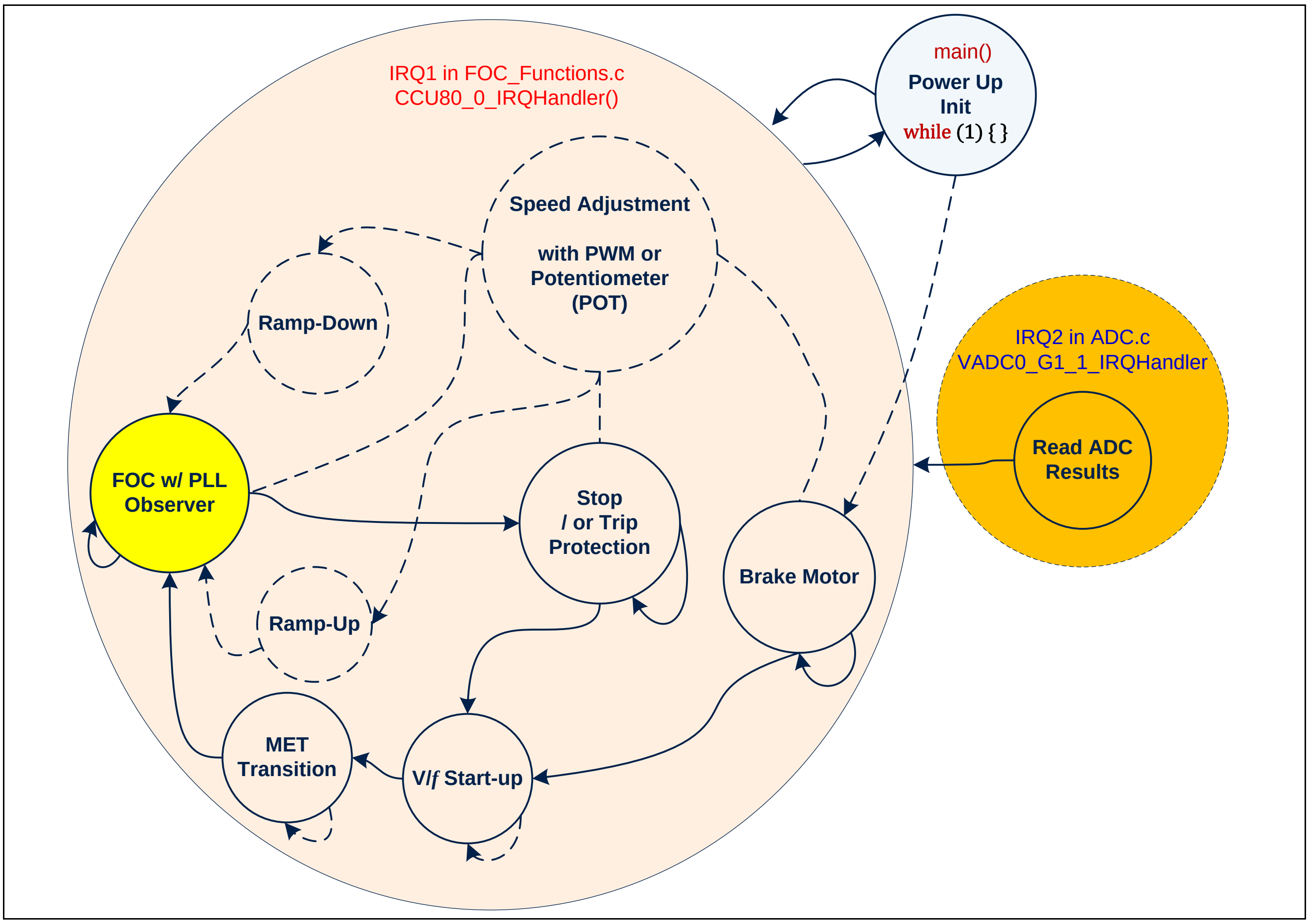
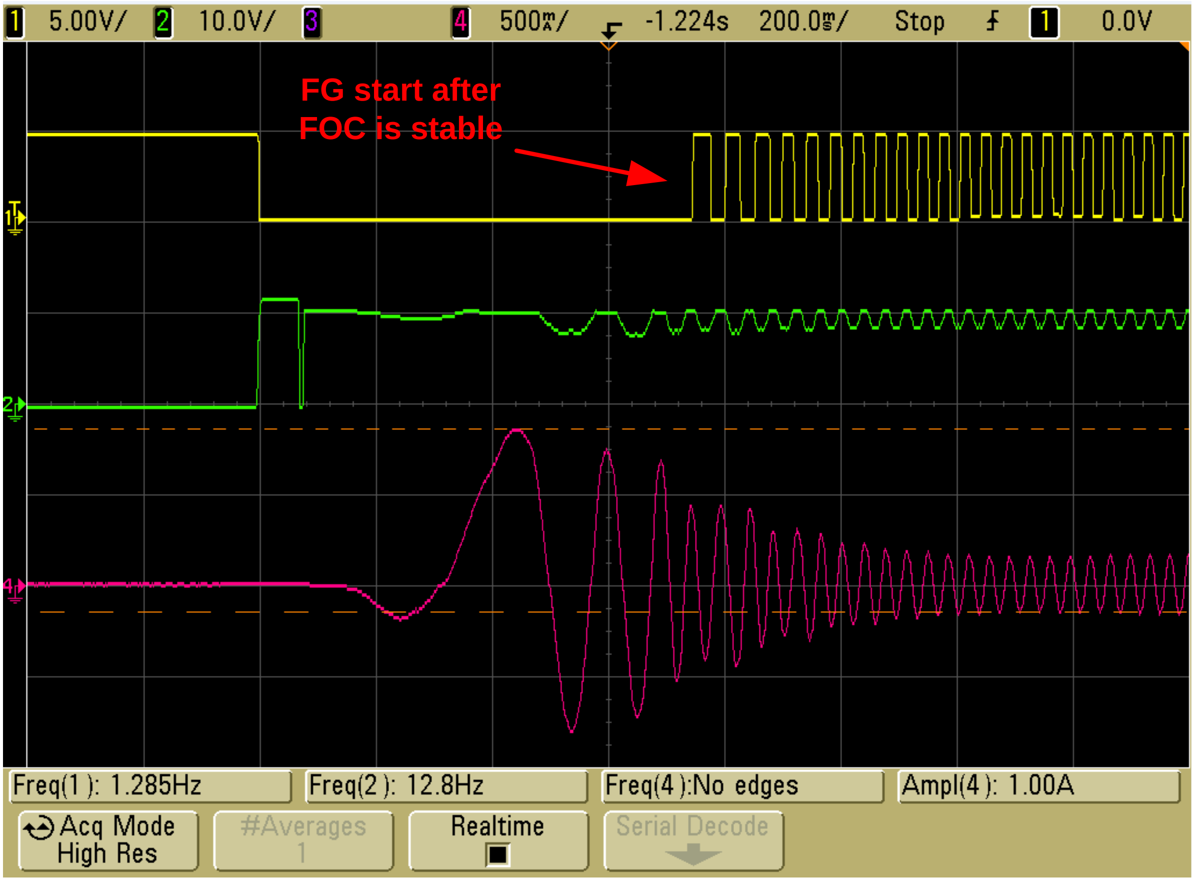


Figure 9 Software State Machine

7 Motor Control Test Data

7.1 Start-up Current Waveform

When the fan motor is at a standstill, it is impossible to sense positional information from motor back-EMF. Infineon server fan reference design provides FOC direct start-up control to achieve better efficiency.



CH 1 (Y): P2.10 (for FG)

CH 2 (G): P0.0 (UH) – Inverter phase U high-side control signal

CH 3 (B): -

CH 4 (P): Current of Fan Motor Phase U (100mV/A)

Figure 10 Direct FOC Start-up

7.2 Power Stage Inverter Dead-Time

To minimize the unwanted ripple in torque that may affect motor motion smoothness, the XMC1302 Capture Compare Unit (CCU4/8) provides flexible dead-time generation. This is used to generate a blanking time period (high-side and low-side transistor in off-state simultaneously). Both transistors are switched off for a short period of time to prevent the transistors conducting simulatenously and causing a short circuit from DC link voltage to ground. The CCU8 supports assymetric dead-time which is required in this application for efficient switching.

CH 1 (Y): P0.0 (UH) – Inverter phase U high-side control signal

CH 2 (G): P0.1 (UL) – Inverter phase U low-side control signal

CH 3 (B): Gate of inverter high-side switch (PMOSFET), for phase U

CH 4 (P): Phase U output of inverter

Figure 11 Phase U Rising Edge Output

CH 1 (Y): P0.0 (UH) – Inverter phase U high-side control signal

CH 2 (G): P0.1 (UL) – Inverter phase U low-side control signal

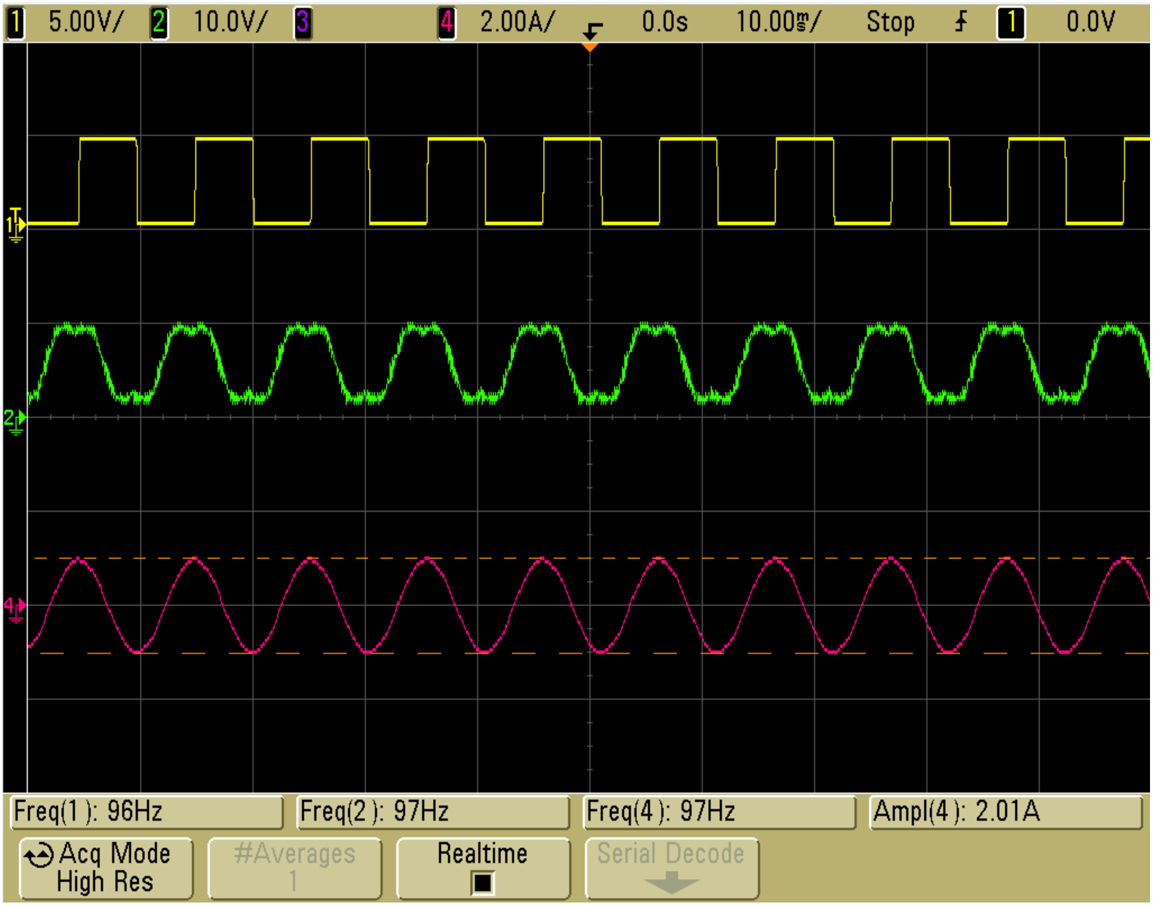
CH 3 (B): Gate of inverter high-side switch (PMOSFET), for phase U

CH 4 (P): Phase U output of inverter

Figure 12 Phase U Failing Edge Output

To minimize the unwanted ripple in torque that may affect motor motion smoothness, XMC1302 Capture Compare Unit (CCU4/8) provides flexible dead-time generation. It is used to generate blanking time period (high-side and low-side transistor in off-state simultaneously). Both transistors are switched off for short period of time to prevent both transistors conducting simulatenously thus causing a short circuit from DC link voltage to ground. The CCU8 supports assymetric dead-time which is required in this application for efficient switching.

7.3 Motor Steady-State Current Waveform



CH 1 (Y): P2.10 (for FG)

CH 2 (G): P0.0 (UH) – Inverter phase U high-side control signal

CH 3 (B): -

CH 4 (P): Current of Fan Motor Phase U (100mV/A)

Figure 13 At steady state stage (FOC Closed Loop)

The Frequency Generator (FG) output is an important feature for server system. It is used as important feedback for the system to monitor the speed behavior of the Server Fan. For example, if the FG output is about 96Hz,

$$\omega = \frac{60 \ x \ FG_{freq}}{n} = \frac{60 \ x \ 96 \ Hz}{2}$$

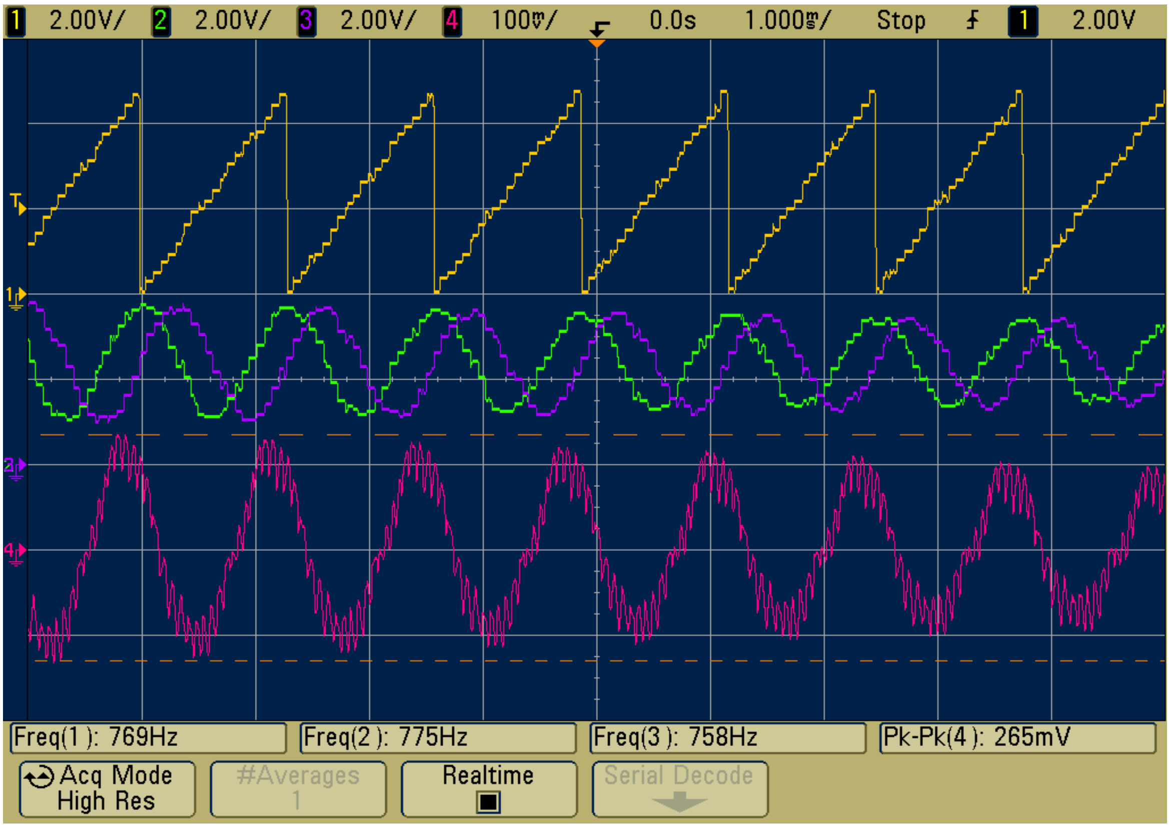
$$\omega = \ 2880$$

Where,

ω = Motor Speed (in rpm)

n = No. of pole pairs

7.4 Motor High Speed Current Waveform



CH 1 (Y): Angle γ =arctan(Iβ/Iα) of fan motor phase current I

CH 2 (G): Iα

CH 3 (B): Iβ (where Iα/Iβ are from single-shunt current reconstruction)

CH 4 (P): Current of fan motor Phase U (100mV/A)

Figure 14 Motor Phase Current with constant high speed

The motor phase current waveform has a harmonic of PWM frequency of 15 kHz. The harmonic distortion is mainly due to the small phase inductance of the fan motor. By increasing the PWM frequency, the harmonic distortion could be reduced.

$$\omega = \frac{60 \;\; x \;\; \gamma}{n} = \frac{60 \;\; x \; 769 \; Hz}{2}$$

$$\omega = \;\; 23{,}070$$

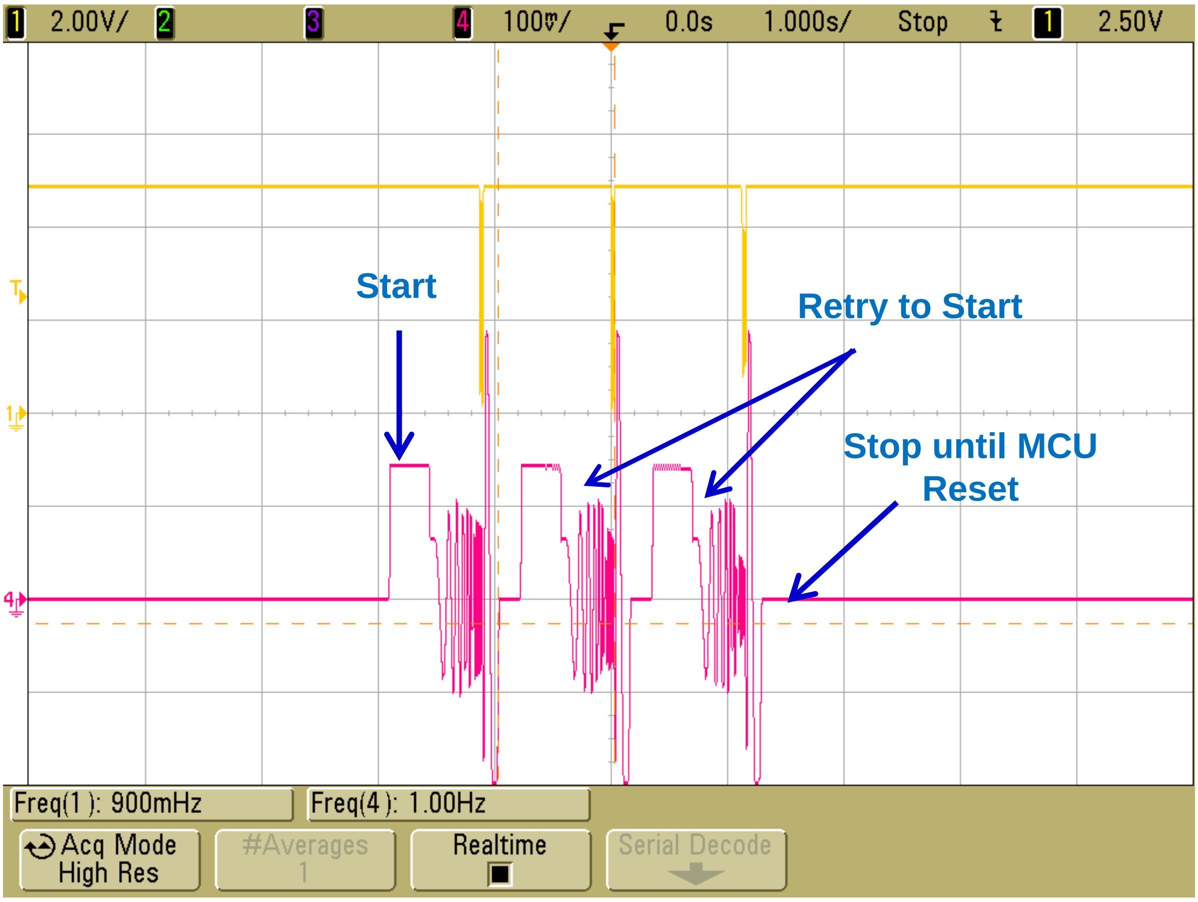
Where,

ω = Motor Speed (in rpm)

n = No. of pole pairs

γ = Angle (in Hz)

7.5 Start-up Lock Detection



CH 1 (Y): P2.10 (for FG)

CH 2 (G): -

CH 3 (B): -

CH 4 (P): Current of Fan Motor Phase U (100mV/A)

Figure 15 Phase Current Waveform during Start-up

The FG pin outputs a PWM waveform in the normal operation condition. During the start-up lock protection, FG output remains high until the motor restart. The retry process will only be stopped when the microcontroller power is reset.

8 Revision History

Current Version is V1.0, 2015-05

Page or Reference	Description of change
V1.0, 2015-03	
	Initial Version

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