Whitepaper
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Driving performance in GaN-based USB-C adapters and chargers with EPR

An innovative, highly integrated combo controller for the joint control of the PFC and the hybrid flyback stage

Abstract

With the announcement of the USB PD 3.1 standard [1], higher power levels of up to 240 W are enabled. Still, the wide output voltage range from 5 V to 48 V raises new challenges for the converter topologies currently in use. In this white paper, the combination of an AC-DC PFC boost and a DC-DC hybrid flyback (HFB) stage [2], also well known as asymmetrical half-bridge flyback topology, is proposed as the most suitable combination for USB-PD chargers and adapters with wide input and output voltage range.

A novel, highly integrated XDP™ controller XDPS2221 is used as a combo controller for the joint control of the PFC and the hybrid flyback stage. This integration offers optimal control of both stages to deliver class-leading performance. The shown 140 W AC-DC reference design achieves a full load peak efficiency of up to 95 percent and a high-power density of 22.67 W/in^3 (uncased) while delivering an output voltage from 5 V to 28 V with input voltage range from 90 V_{AC} to 264 V_{AC}.

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Table of contents

1 Introduction

The new USB-PD Extended Power Range (EPR) standard [1] offers a universal AC-DC adapter for many different purposes, charging a whole range of end devices, from smartphones to gaming laptops, up to power tools, and even e-bikes. Nevertheless, the typical requirements for electromagnetic compatibility, power factor correction, standby power, and average efficiency raise a new challenge for the converter topologies used up to now. Additionally, the size (and, consequently, the power density) becomes a more important factor for the customers.

State-of-the-art mid-power range circuit topologies for wide output voltage range are:

1. **PFC+Flyback topology [4] – [7]:**
   It is extremely flexible in terms of input and output voltage range but very bulky due to its transformer size. The switch requires higher dielectric strength. Furthermore, it is limited in switching frequency since the leakage energy cannot be recycled. This can be solved in the active clamp version. However, transformer size is still a limiting factor for small form factor design.
2. **PFC+LLC+Buck topology:**
   The PFC+LLC [8], [9] can be very small and efficient, but it is very limited in terms of the output voltage range. Therefore, a buck converter would be required additionally for a wide output voltage range, resulting in a bulky and expensive system solution.
3. **PFC+Hybrid flyback topology [11], [12]:**
   With the proposed innovative control, this architecture enables a high-power density with high power efficiency to meet international regulatory standards, such as EU CoC Version 5 Tier 2 and DoE Level VI. Furthermore, it supports an effective control of the wide output voltage for the latest USB PD extended power range (ERP) standard V3.1. Compared to conventional flyback variants, the transformer size can be considerably reduced.

2 Proposed architecture

In order to achieve the highest power density, the proposed two-stage solution consists of an AC-DC PFC boost stage and the DC-DC hybrid flyback in combination with synchronous rectification at the output [12] – [14]. Figure 1 shows the details of the converter architecture.

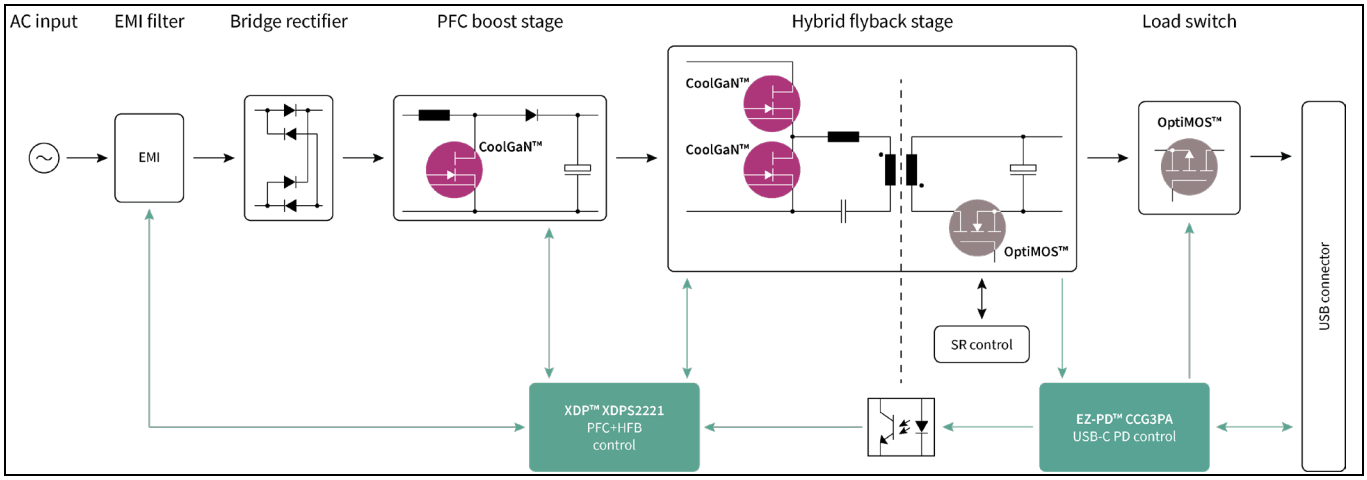

Figure 1 Proposed converter power architecture for USB-PD EPR

XDP™ XDPS2221 integrates an AC-DC power factor correction (PFC) controller with a DC-DC hybrid flyback controller (HFB), also known as asymmetrical half-bridge (AHB), in one single package. Regulatory efficiency requirements can easily be met through the harmonized operation of the two stages. In addition, the further integration of all gate drivers and a 600 V high voltage start-up cell for the initial IC voltage supply enable a low external bill of material (BOM) and component count. Based on a novel zero-voltage switching (ZVS) HFB topology in conjunction with GaN-based devices, it brings class-leading efficiency across various line/load conditions. Thanks to these features and inherent topology advantages, such as zero voltage switching and resonant energy transfer for transformer size reduction, system designs using XDP™ XDPS2221 can achieve very high power densities.

Moreover, the new combo IC features a synchronous PFC and HFB burst mode operation for the lowest possible no-load input standby power performance. The quasi-resonant multimode PFC stage is enhanced with automatic PFC enable/disable functionality and adaptive PFC bus voltage control to maximize average and light load efficiency. Optionally, the integrated PFC function can also be disabled to support the use case with any kind of external PFC controller.

The hybrid flyback stage uses peak current control operation for robust regulation and fast dynamic load response. To ensure ZVS operation under all conditions, the hybrid flyback features ZVS pulse insertion, including body diode cross-conduction prevention in discontinuous conduction mode. Additionally, XDP™ XDPS2221 also provides easy-to-configure parameters via a graphical user interface to optimize system performance.

The embedded digital core of the XDP™ XDPS2221 allows a sophisticated control algorithm to optimize the performance of both power stages. For optimum system efficiency and reduced standby power, the PFC stage will only be enabled depending on input and output voltage conditions as well as load

conditions. In addition, a bus voltage target modulation, depending on the operation point of the HFB, helps to increase the efficiency further.

To reach the highest power density, it is desired to maximize the efficiency at the maximum load, typically the worst case in terms of power losses. With the newly implemented PFC modulation, it is possible to improve the efficiency for the lower output voltage levels. Figure 2 shows the four-point average efficiency with PFC modulation and fixed PFC output voltage.

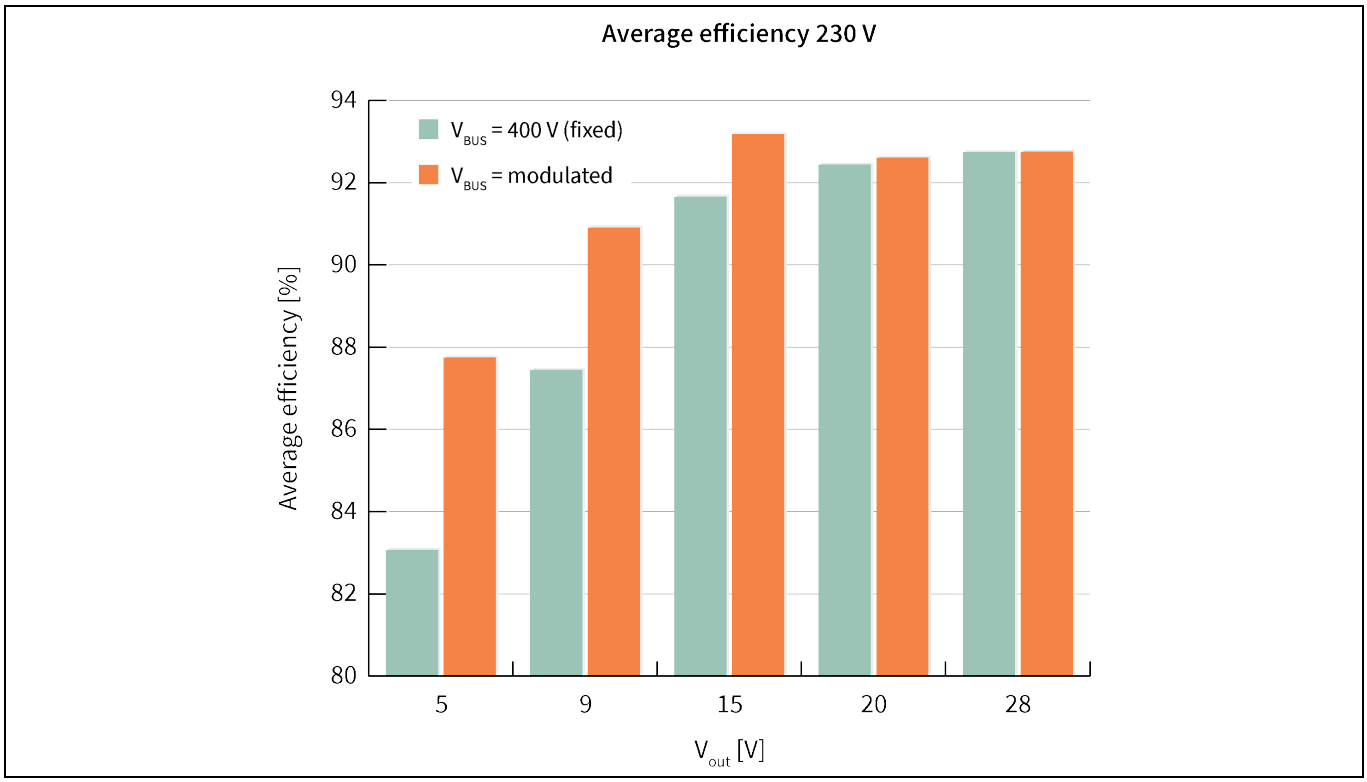

Figure 2 Four-point average efficiency with and without modulation at 230 V

Due to the modulation, the efficiency can be improved by nearly five percent for the lowest output voltage. Besides the high-performance multimode PFC working in critical conduction mode with valley switching and the high-efficiency multimode HFB topology, the controller offers a 600 V start-up cell to start the system before the auxiliary supply takes over.

The embedded digital core supports system fine-tuning by configurable parameters. This gives a lot of flexibility to designers to adapt to different power levels and application requirements. Additionally, very high-frequency switching applications can be supported and enable the usage of a planar transformer due to zero voltage switching (ZVS) and zero current switching (ZCS).

3 Practical prototype

To demonstrate the described advantages, a 140 W (28 V/5 A) prototype has been developed (Figure 3). In this case, two-layer PCBs and standard magnetic cores are utilized to achieve low system cost.

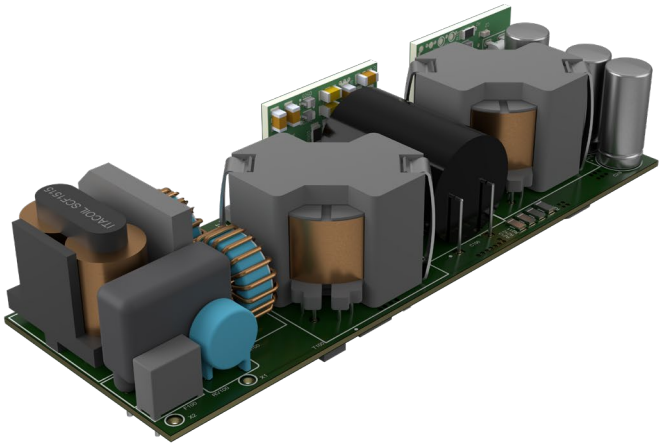

Figure 3 140 W prototype USB-PD EPR 5 V – 28 V with a power density of 22.67 W/inch³

The efficiency results are shown in Figure 4 (Low line) and Figure 5 (High line). The results cover the output voltage range from 5 V – 28 V with load variation from 10 – 100 percent. The circuit reaches a peak efficiency of 95 percent at maximum load but also stays above 80 percent efficiency at minimum load.

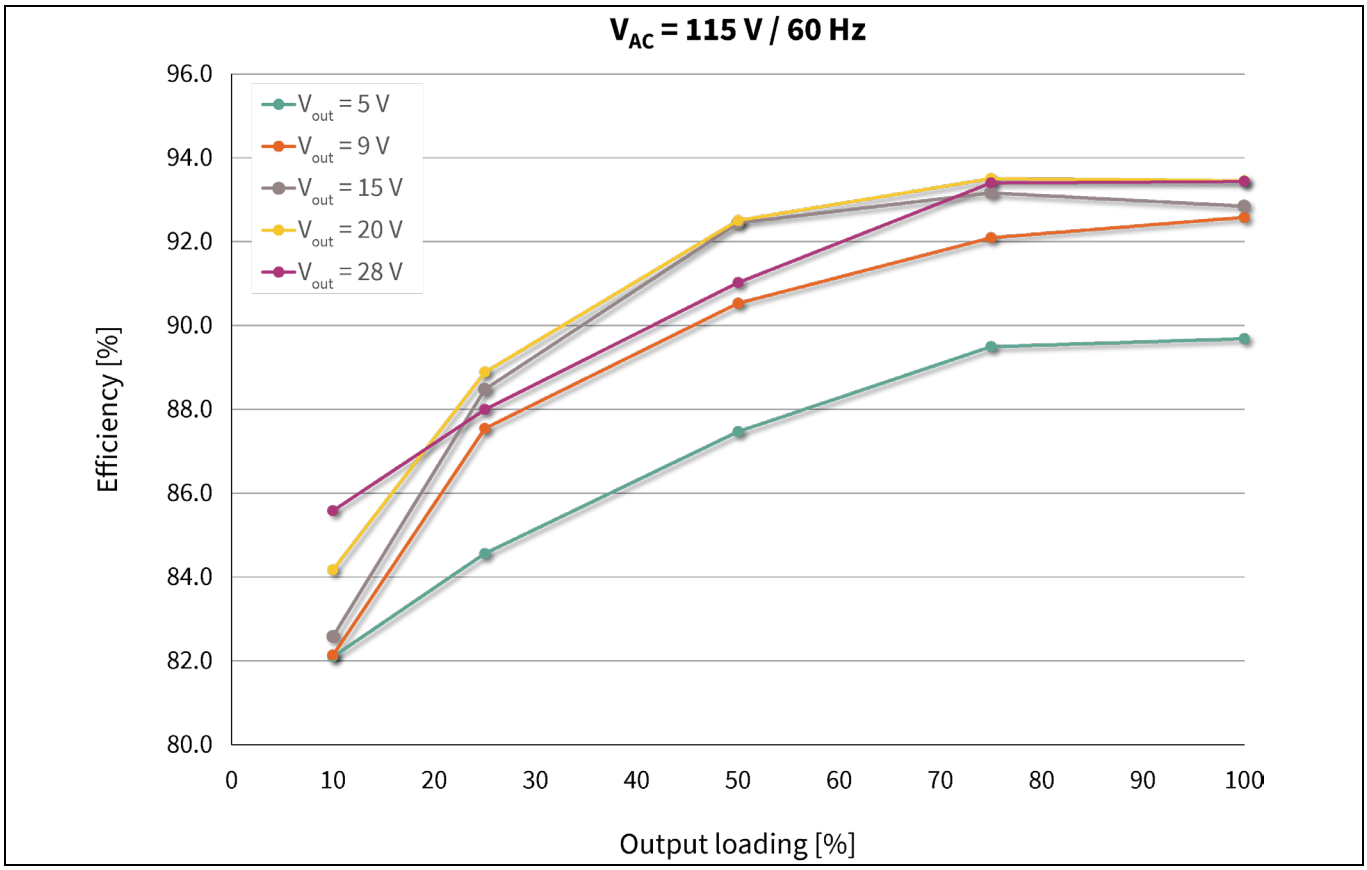

Figure 4 Low line efficiency vs. output loading for a voltage range of 5 – 28 V

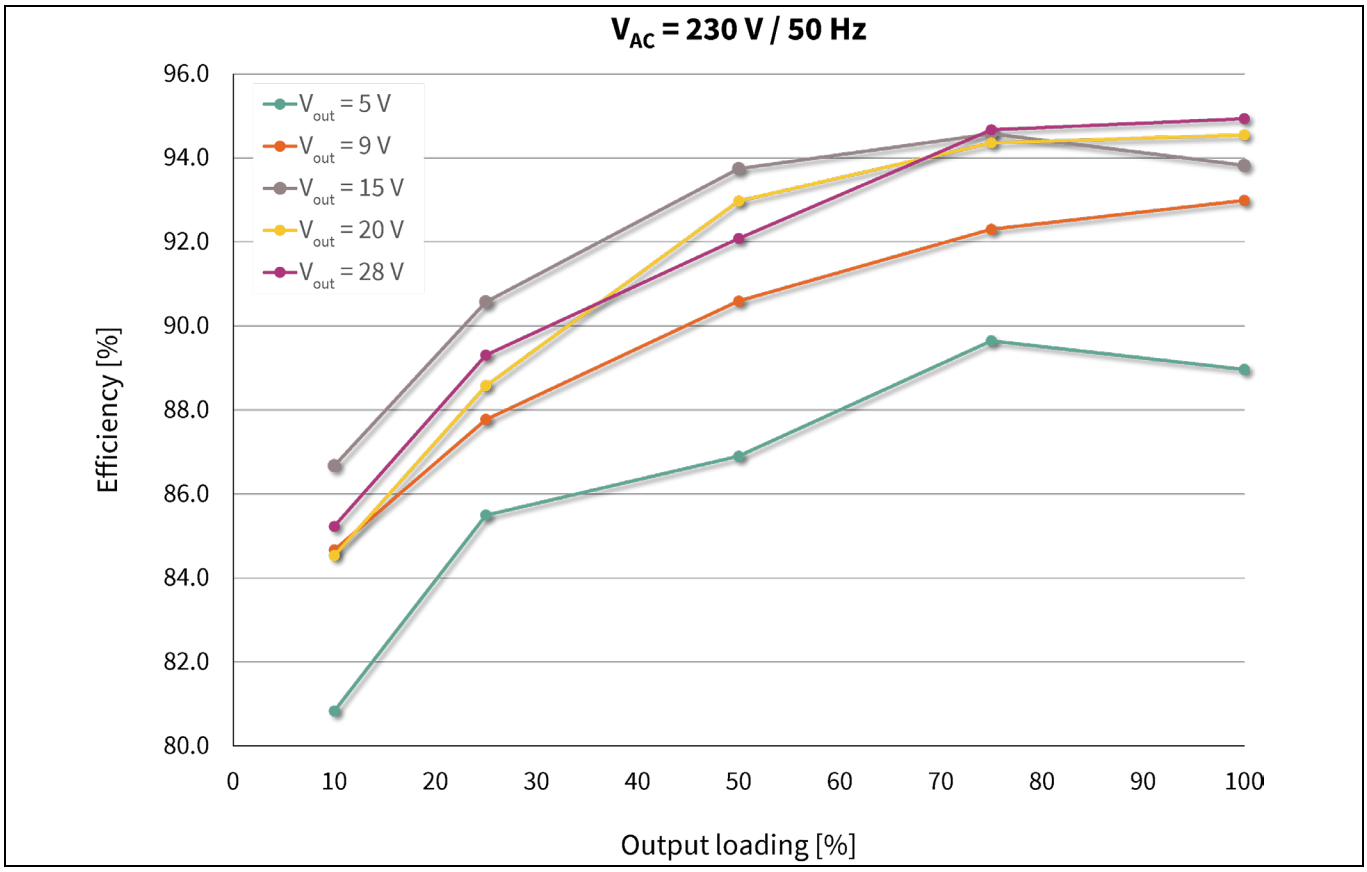

Figure 5 High line efficiency vs. output loading for a voltage range of 5 – 28 V

This results in the following four-point average efficiency (Figure 6). With the integrated sophisticated control algorithm between PFC and HFB, the CoC Tier 2 limits can be easily achieved.

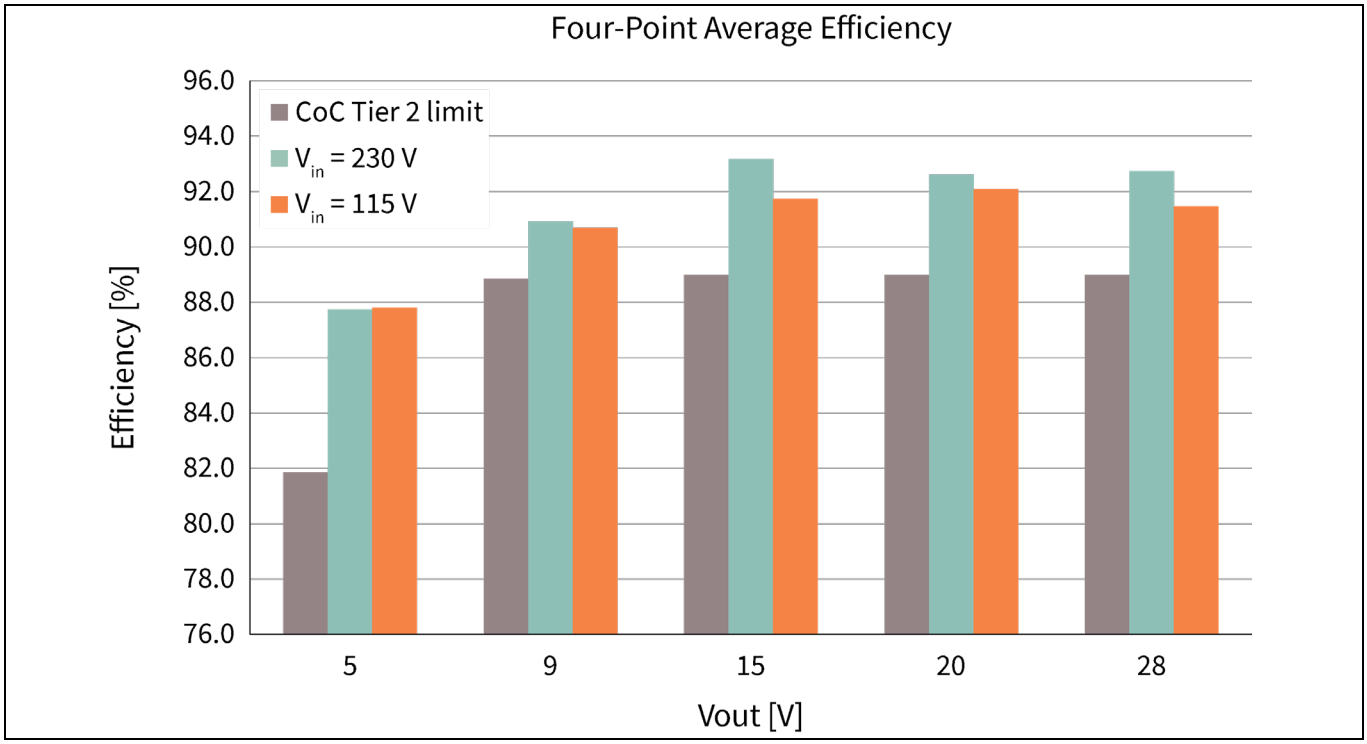

Figure 6 Four-point average efficiency, indicating that the CoC Tier 2 limits can be easily achieved

Figure 7 shows the standby losses in the input voltage range from 90 V up to 264 V. Due to the synchronous PFC and HFB burst mode operation, the standby losses could be decreased below 70 mW in the entire input voltage range.

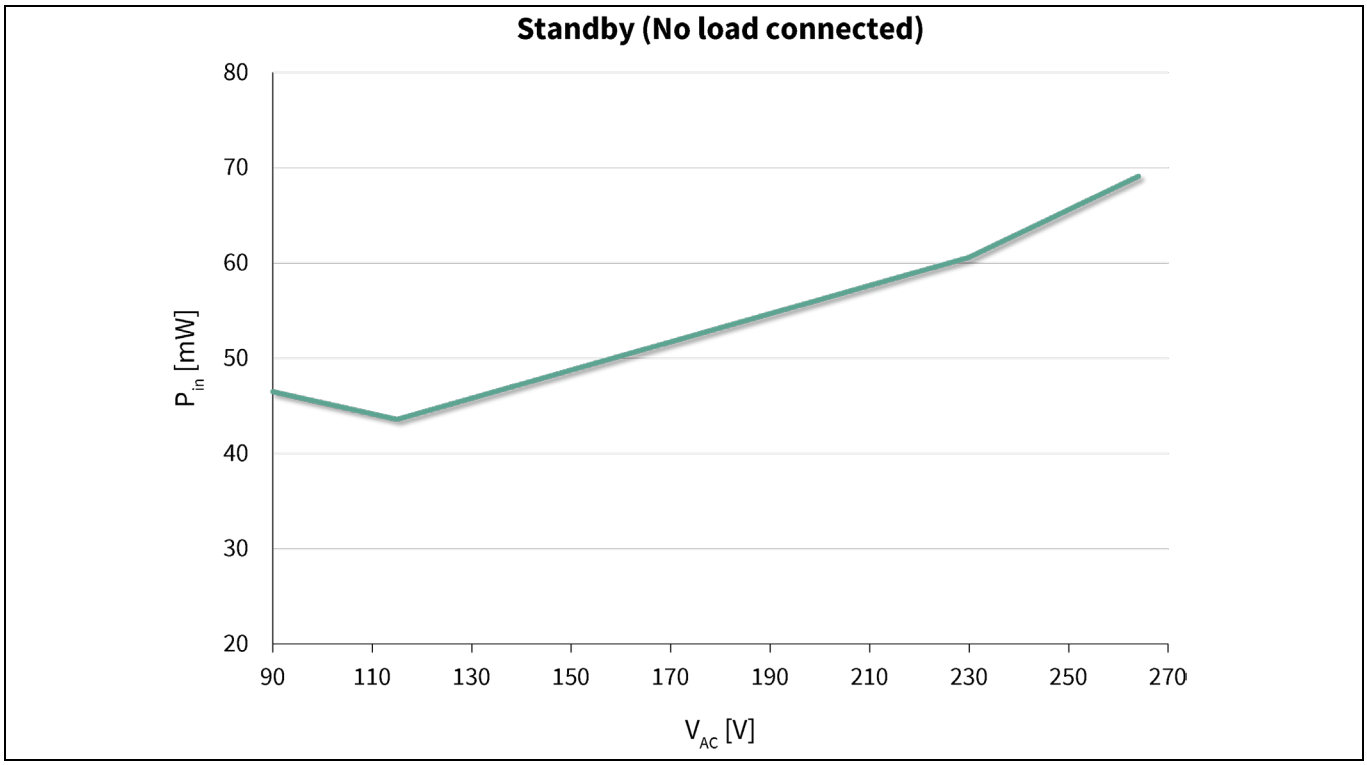

Figure 7 Standby losses in the input voltage range

4 Conclusions and future work

Combining the HFB and the PFC-boost with the new sophisticated control strategy demonstrates the potential for USB-PD EPR adapters to reach high efficiencies from light load to maximum load. The highly integrated controller with combined PFC and HFB operation enables a simple design in small size to get also a high-power density. The benefits of the proposed solution have been demonstrated with a 140 W USB-PD EPR prototype achieving high peak efficiency of 95 percent and a power density of 22.67 W/inch^3 with a low-cost two-layer PCB.

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