Dimming Control using a PWM Signal

XDP™ Digital Power

White Paper
Revision 1.0

About this document

Scope and Purpose

This White Paper explains how a ***Pulse Width Modulation (PWM)*** signal can be used for analog dimming of the output current of a ***Light Emitting Diode (LED)*** lighting controller. An example for such a controller is XDPL8220. This White Paper provides information about how the ***PWM*** duty cycle maps to the output current and how the ***PWM*** duty cycle is measured in a digital controller. Possible faults are discussed which can cause flicker in light and solutions to these faults are provided.

Intended Audience

The intended audience are engineers who design power converters for lighting applications using ***PWM*** control for dimming.

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1 Introduction

To save energy, extend system life and enhance flexibility, the dimming of light has become a regular requirement. The stability of light output is important as ***LED***s react very fast to any change of their driving current. Thus, any instability can cause visual flicker.

The usage of a ***PWM*** signal to control the light output of a power converter has several advantages compared to usage of an analog voltage level:

- The information of the ***PWM*** signal can easily be transferred over an isolation barrier using a simple optocoupler. As the dimming information is coded in the timing of the edges of the signal, any tolerances as well as aging of the optocoupler causing a change in its gain has only minimal influence on the dimming information.
- A digital controller can typically capture the timing of the ***PWM*** signal more accurately and with less effort than capturing a voltage level. For example, if the ***PWM*** signal uses a frequency of 1 kHz and is detected using a clock of 50 MHz, the granularity is 50 MHz / 1 kHz = 50000. To achieve the same granularity for sensing of a voltage signal, a 16 bit ***Analog-to-Digital Converter (ADC)*** is required (2^16 > 50000).
- Any circuitry for voltage levels can easily be affected by temperature. A temperature dependency of the circuitry is especially present if semiconductors are involved. E.g. diodes typically change their forward voltage by -2.5 mV/K. For them, a temperature change of 60°C can cause a voltage shift of 150 mV. If the dimming signal is coded by a signal between 0 V and 2 V, the temperature dependency causes an absolute error of 7.5%. The relative error (especially for low dimming voltages) will be even much higher.

This White Paper provides information about different topics related to usage of a ***PWM*** signal for dimming control. First, the mapping of the ***PWM*** signal to an output current is discussed. Second, the sensing of the ***PWM*** signal by a digital controller is described. Finally, possible faults of the sensing and processing of the ***PWM*** signal are described and solutions are presented to avoid any impact on the performance of the lighting application.

2 Mapping of PWM duty cycle to output current

If a ***PWM*** signal is applied to the output current directly, the ***PWM*** duty cycle relates proportional to the resulting current, e.g. a 30% duty cycle maps to 30% current and a 60% duty cycle maps to 60% current as shown in ***Figure 1*** .

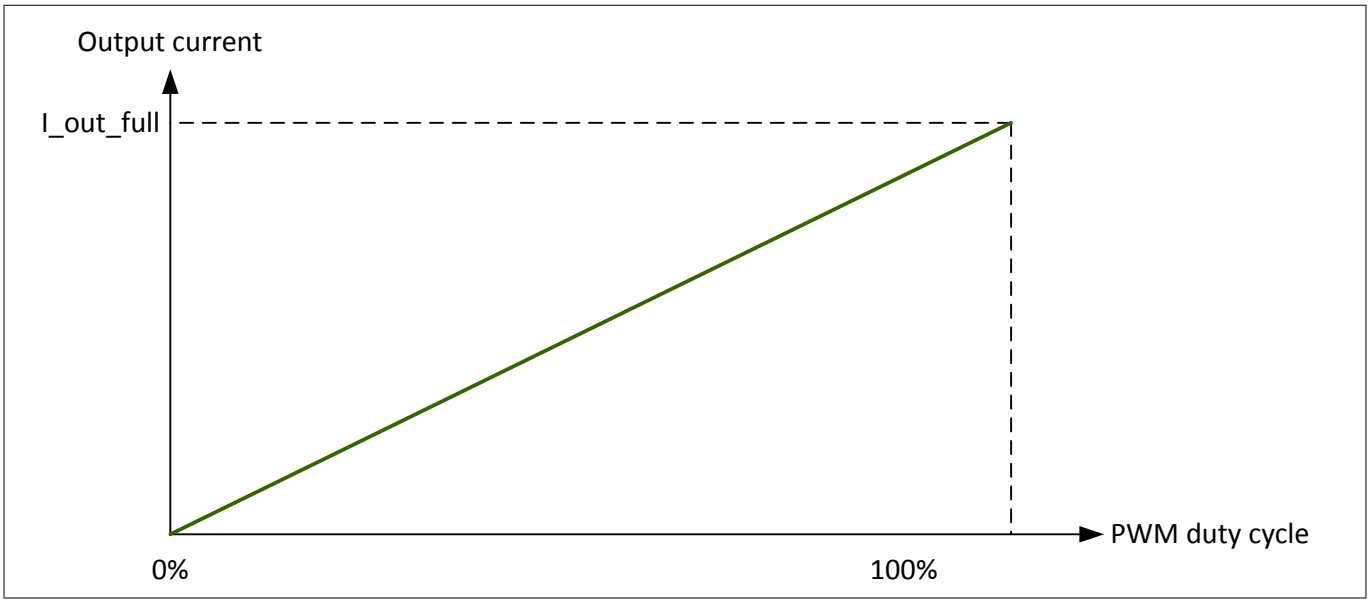

Figure 1 Direct Mapping of a PWM Signal to the Output Current

Mapping of PWM duty cycle to output current

While this is the easiest mapping of a ***PWM*** signal to the output current , it has some disadvantages:

- ***PWM*** signals with extreme duty cycles (e.g. 1% or 99%) can easily be affected by noise. Relative errors can become large and easily visible to the human eye, especially for low output currents.
- Tolerances of components can easily cause part-to-part deviations. This can result in not all parts being able to reach extreme duty cycles. As a consequence, not all power converters may be able to reach lowest and full light output.
- The human eye is sensitive to relative changes in light intensity. The direct mapping allows no adaptation of the light output to this property of the human eye. As a consequence, when the ***PWM*** duty cycle is changed with a fixed rate in time, the relative changes in light will seem small at higher output currents and large for smaller output currents.
- Measurements of ***PWM*** duty cycles by digital controllers are limited by the sampling frequency of the digital signal processing.

Due to these disadvantages, a different mapping of the ***PWM*** duty cycle to an output current is usually preferred. This mapping of the ***PWM*** duty cycle to an output current is called "Dimming curve". Some possible dimming curves are shown in ***Figure 2*** .

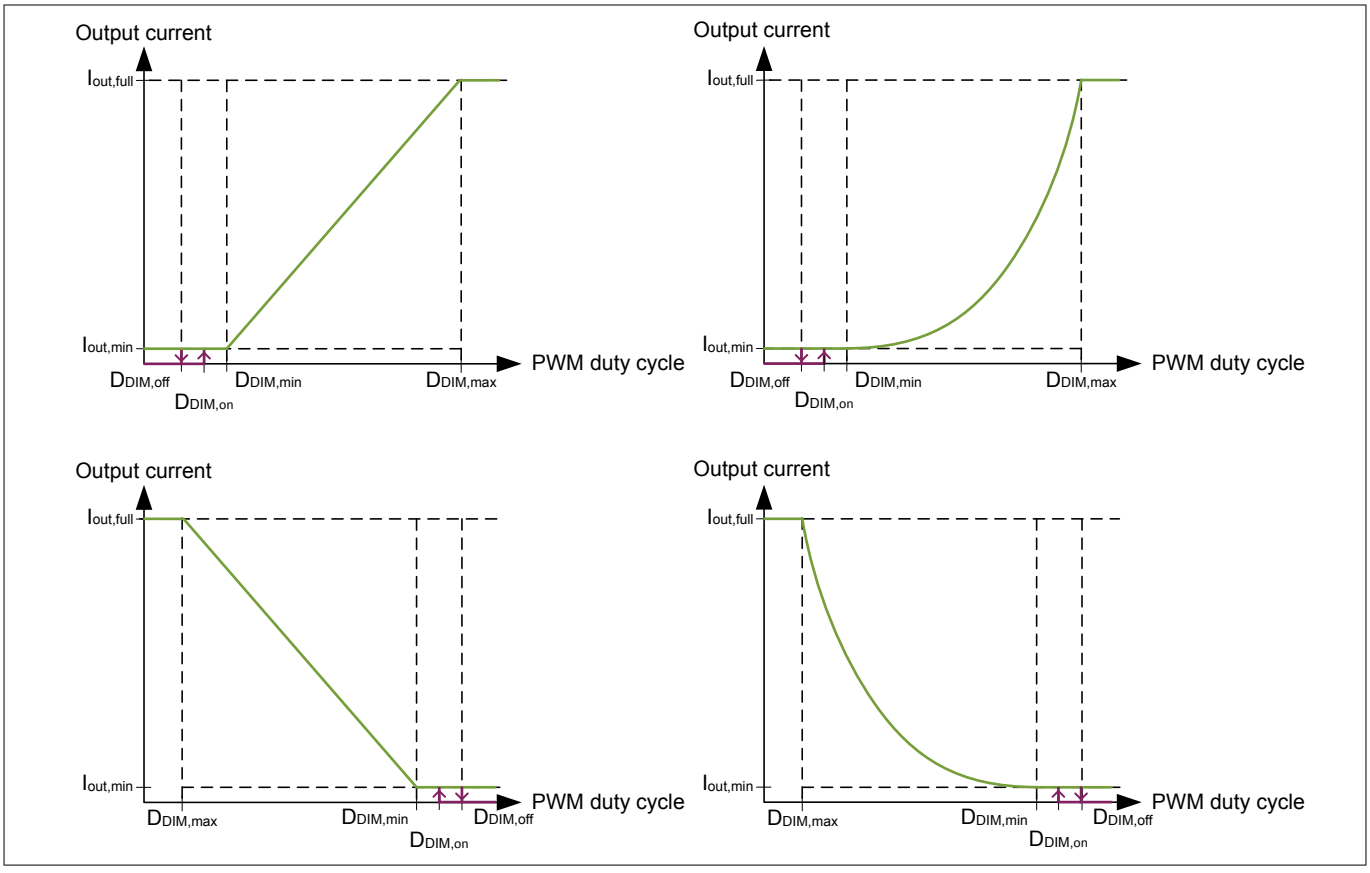

Figure 2 Dimming curves

A dimming curve may have different properties:

- Dead bands:

  Lower ***PWM*** duty cycles below a certain threshold $D_{DIM,min}$ are mapped to the lowest current. Higher duty cycles above another threshold $D_{DIM,max}$ are mapped to the full current. These dead bands ensure that lowest and full current can be reached independently from any tolerances. In between the thresholds, the current is interpolated. This causes a steeper curve compared to the direct mapping without dead bands: The relative change of current of a dimming curve with dead bands is higher than the relative change of the ***PWM*** duty cycle of a direct mapping.
- Shape:

  The dimming curve between the dead bands can be either linear or eye-adapted:

- The linear dimming curve ensures a proportional change of current with respect to the ***PWM*** duty cycle. This is the closest approximation of the direct mapping of the ***PWM*** duty cycle. In the special case of no dead bands, this maps exactly to the direct mapping.
- As the human eye is sensitive to relative changes in light, the eye-adapted dimming curve ensures a constant relative change of output current with respect to ***PWM*** duty cycle. This requires an exponential dimming curve. To minimize the technical effort, the exponential curve can typically be approximated by a quadratic curve.

- Direction:

  The direction of the dimming curve defines the sign of the slope of the dimming curve:
  - Normal: A low ***PWM*** duty cycle maps to a low current and a high ***PWM*** duty cycle maps to a high current.
  - Inverted: A high ***PWM*** duty cycle maps to a low current and a low ***PWM*** duty cycle maps to a high current.

  A change of the direction of a dimming curve may be beneficial in circuits which use an optocoupler as the optocoupler may invert the polarity of the ***PWM*** signal.

3 Sensing the PWM duty cycle

The ***PWM*** duty cycle can be detected in two ways:

1. Measuring the positive pulse width (time between rising and falling edge) and negative pulse width (time between falling and rising edge) and calculating:

$$\text{duty\_cycle} = \frac{\text{positive\_pulse\_width}}{\text{positive\_pulse\_width} + \text{negative\_pulse\_width}}$$

Equation 1

2. Measuring the positive pulse width (time between rising and falling edge) and the period (time between rising edges and caluclating:

$$\text{duty\_cycle} = \frac{\text{positive\_pulse\_width}}{\text{period}}$$

Equation 2

The first way is preferred with respect to implementation as the XDP hardware easily supports these measurements. Also, the equation is always valid while the second way may cause a division by zero and require case handling if the period is measured incorrectly or has not been measured at all.

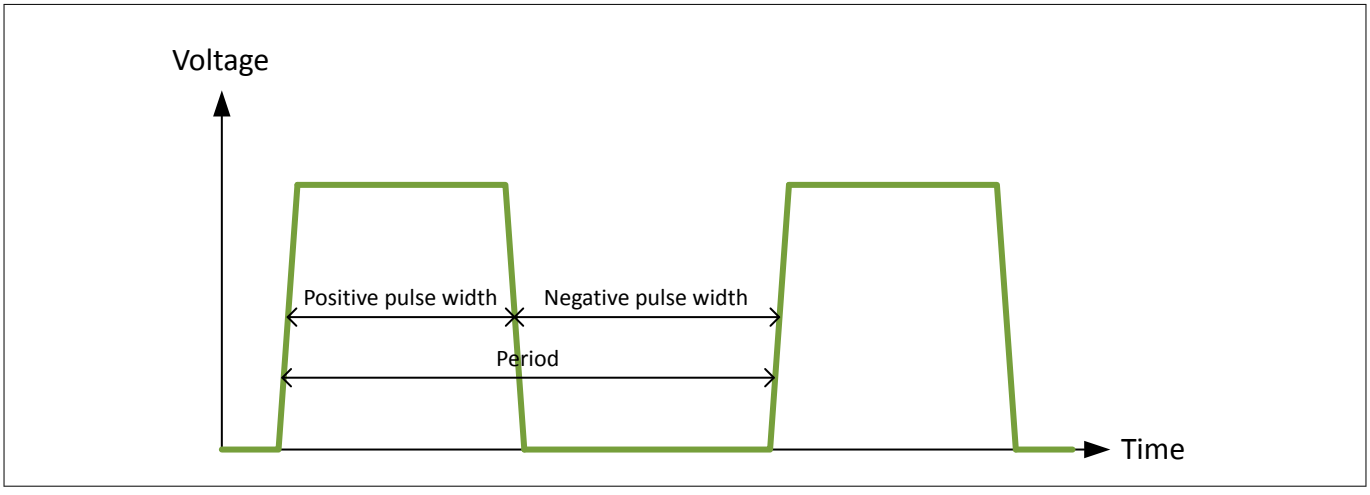

Figure 3 PWM signal

Due to limitations of the used XDP hardware and the scheduling of firmware tasks, a positive or negative pulse-width below a limit cannot be measured. For XDPL8220, the firmware tasks are scheduled in intervals of typical 32 µs which limits the minimum pulse width to this duration. Depending on the frequency of the ***PWM*** signal, the minimum pulse width limits the usable ***PWM*** duty cycle to e.g.[1)]:

- For 2 kHz ***PWM*** signal: 32 µs * 2000 Hz = 6.4% to 100%-6.4% = 93.6%
- For 1.5 kHz ***PWM*** signal: 32 µs * 1500 Hz = 4.8% to 100%-4.8% = 95.2%
- For 1 kHz ***PWM*** signal: 32 µs * 1000 Hz = 3.2% to 100%-3.2% = 96.8%
- For 500 Hz ***PWM*** signal: 32 µs * 500 Hz = 1.6% to 100%-1.6% = 98.4%

Special handling has to be implemented if constant low or constant high signals need to be detected. These cases can be detected based on the level of the signal if no edges occur within a timeout period. The duration of the timeout period depends on the maximum ***PWM*** period plus an additional ***PWM*** period (***PWM*** signal and sensing are asynchronous) plus some margin for tolerances.

Depending on the used clock frequency of the digital signal processing, the ***PWM*** frequency range and the digital number format has to be defined: For a clock oscillator of 50 MHz, any ***PWM*** frequency below 50 MHz / 2^16 = 763 Hz[2)] does not fit into a 16 bit number format, but require 32 bit processing (or at least 17 bit processing using a right shift of the measured pulse-width combined with special 16-bit overflow handling).

4 Errors in the usage of a PWM signal

The sensing and processing of the ***PWM*** signal can be disturbed by different effects. If periodic or random noise is present in the ***PWM*** signal itself or in the sensed duty cycle, the noise can propagate to the output current. Visible flicker can occur. Digital signal processing can reduce and avoid these effects.

Spikes or Glitches

Spikes or glitches caused by e.g. switching gate drivers can easily create false edges of the ***PWM*** signal and cause a wrong measurement of a pulse width. As the digital signal processing cannot recognize any pulse width below a certain limit (e.g. for XDPL8220 this is 32 µs), it is recommended to use a spike filter with the same filter duration (e.g. 32 µs) to blank out any shorter spikes.

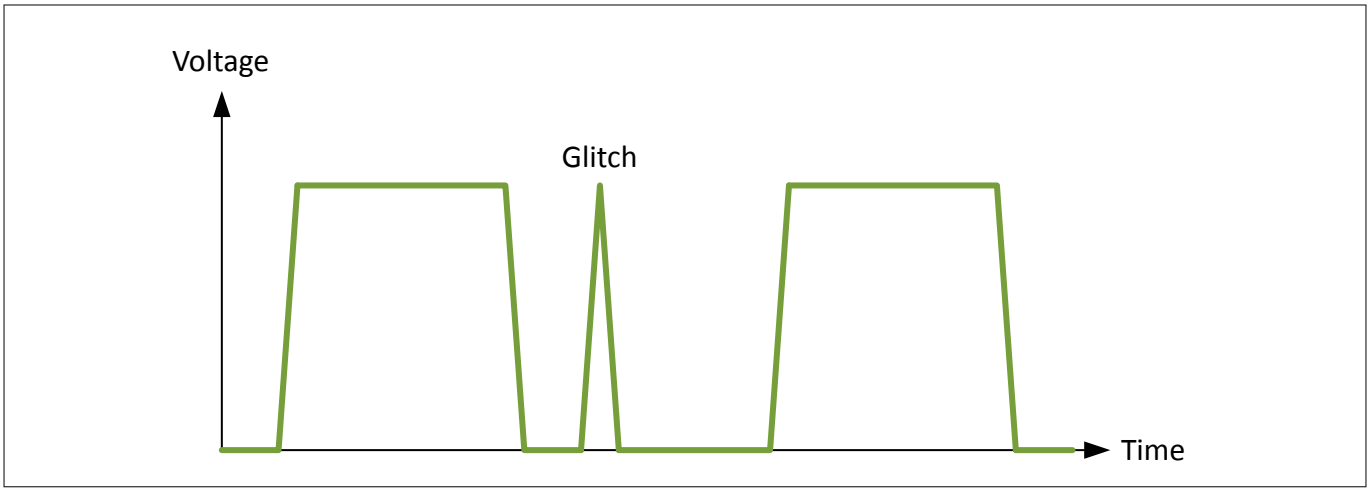

Figure 4 PWM signal with a glitch

Quantization noise

The duty cycle of the ***PWM*** signal is sensed with an asynchronous clock and is internally processed as a digital variable. Due to this, random quantization noise occurs as the duty cycle of the ***PWM*** signal does usually not

1 Tolerances of the clock oscillator reduce these limits further.
2 Tolerances of the clock oscillator increase the frequency limit to more than 763 Hz.

Errors in the usage of a PWM signal

map exactly to a digital representation (see ***Figure 5***). The amplitude of the quantization noise depends on the granularity of the digital representation. Depending on the dimming curve, the quantization noise can be visible in light. To avoid flicker caused by quantization noise, a hysteresis can be used to suppress any change in duty cycle of only 1 bit.

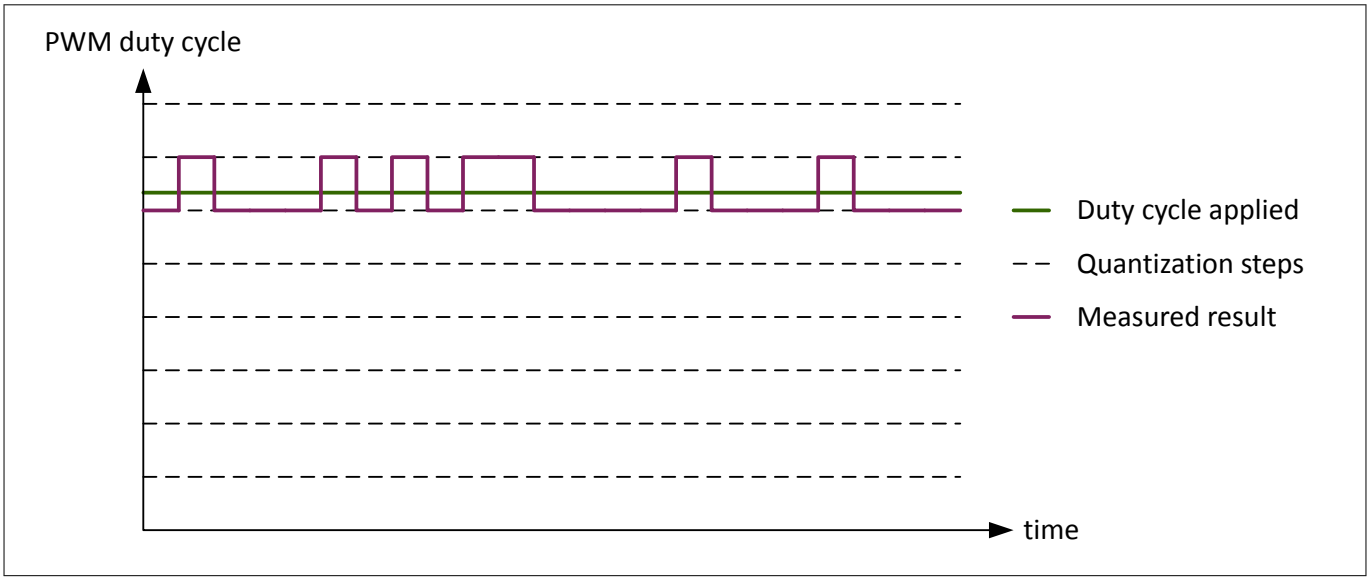

Figure 5 Effect of Quantization Noise on the PWM Duty Cycle

Example: XDPL8220 processes the ***PWM*** duty cycle in 2^11 = 2048 steps. Therefore, a quantization noise of 1/2048 = 0.05% is expected for the duty cycle. If the system operates at e.g. 5% duty cycle and uses a linear dimming curve, the quantization noise causes a relative fluctuation of 0.05%/5% = 1%. Depending on the dimming curve, this can map to a higher fluctuation in light, especially if a steep linear dimming curve is used.[1)]

Jitter of the PWM signal

The ***PWM*** signal may not be stable over time. Two typical sources of instability are temporal changes of the duty cycle (duty cycle jitter) or temporal changes of frequency (frequency jitter), as shown in ***Figure 6*** . Both types of jitter can create visible flicker in light, especially at low output currents if a linear dimming curve is used.

Example: Assume a ***PWM*** signal with a frequency of 1 kHz, a duty cycle of 10% and a duty jitter of 4 µs. This results in a variation of duty cycle of 0.4% which may seem rather small. However, the human eye is sensitive to the relative change in light. Assuming a liner dimming curve without dead bands[2)], this jitter creates a relative change in light output of 0.4% / 10% = 4% which is visible in light[3)].

1 As the human eye can only sense relative differences in light of more than 1.5%, no flicker is expected for XDPL8220 due to quantization noise.
2 Dead bands cause a steeper dimming curve, so the effect gets worse for larger dead bands.
3 The human eye can typically sense relative differences in light of more than 1.5%

Errors in the usage of a PWM signal

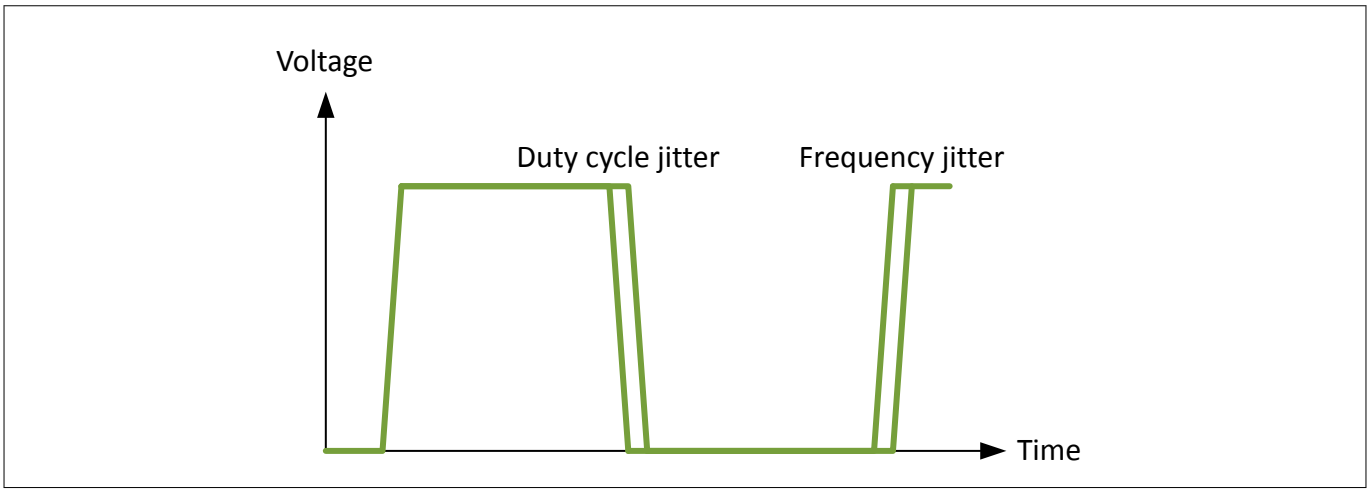

Figure 6 Multiple periods of a PWM signal with jitter overlayed

To suppress fluctuations in duty cycle, different methods can be used:

- The sensed duty cycle can be filtered (e.g. using a finite or infinite impulse response filter). This will remove any fast reactions of the controller to jitter of a ***PWM*** signal. A disadvantage is that any signal processing for the filter introduces a delay. As a consequence, a too strong filter is not desired as it can create a noticeable lag in the transient response (e.g. if the dimming level is changed by intention). Also, a filter should not be applied to the ***PWM*** signal during the start of the controller as it can significantly delay the time-to-light.
- A hysteresis can be applied to the sensed signal to ignore any smaller deviations below a certain threshold. This still allows to react immediately to larger transients. A disadvantage of a hysteresis is that the controller will show no reaction to slow transients of a clean ***PWM*** signal for a limited time if the dimming direction is changed (dimming up after previously dimming down or vice versa).
- The methods above can be combined to trade off the advantages and disadvantages of both methods.

Impact of other Features on the Dimming Curve

Some feature of a lighting controller can cause deviations of output current measured from the ideal dimming curve, as shown in ***Figure 7*** . The following explanations refer to a normal dimming curve (low current at low ***PWM*** duty cycle):

- If the controller features a limited power mode and the full output current would be above the power limit at some output voltages (V_out*I_out_full > P_out_set), the output current will not reach the full output current for these cases. The controller will limit the high dead band to a lower current level of I_out = P_out_set / V_out. As the level of the high dead band is lower than the full current, the controller will enter this dead band already at a lower ***PWM*** duty cycle than the D_DIM_max configured.
- If the dimming curve is configured to a minimum current which cannot be achieved at all output voltages due to a minimum power limit[4)] (V_out*I_out_min < P_out_min), the output current will not reach the minimum output current for these cases. The controller will be limited to higher low dead band at I_out_min = P_out_min/V_out. As the level of the low dead band is higher than the minimum current, the controller will enter this dead band already at a higher ***PWM*** duty cycle than the D_DIM_min configured.
- A hysteresis for the sensing of the ***PWM*** duty cycle can cause an offset of the dimming curves from the ideal curve. This effect is strongest for a clean ***PWM*** signal without any jitter. If the ***PWM*** signal has random jitter, the noise will reduce the visible hysteresis between dimming curves.

[4] Please note that a minimum power level may not be a fixed value, but may depends on other parameters, especially on bus voltage.

Errors in the usage of a PWM signal

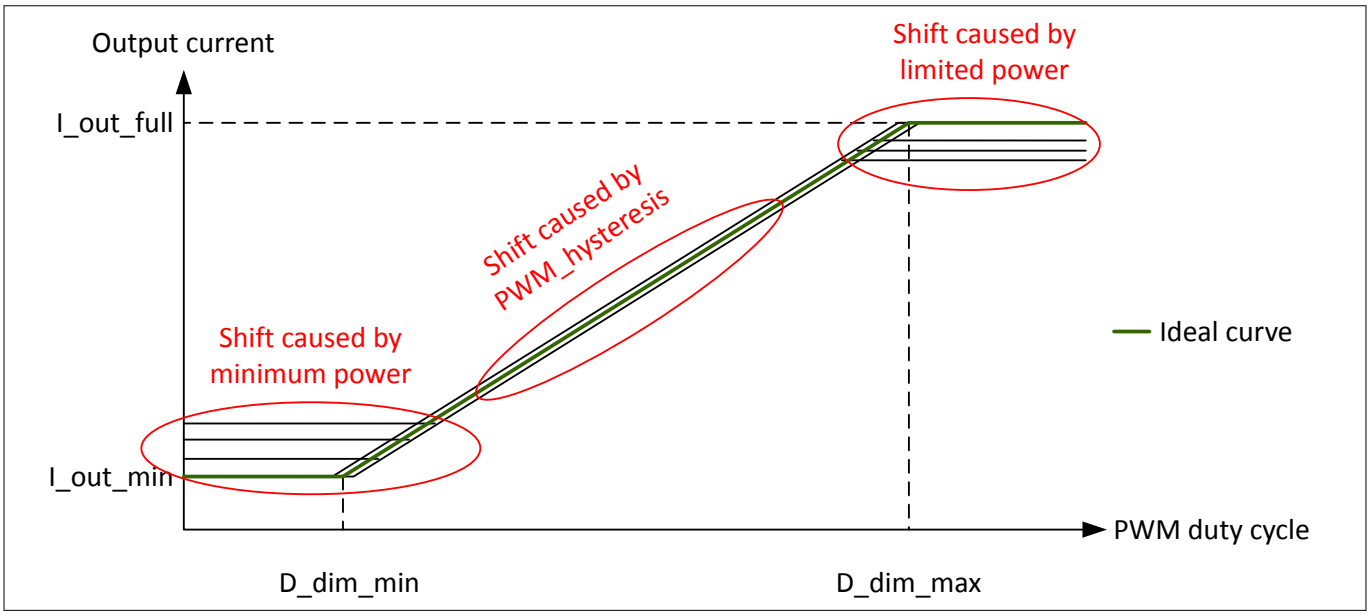

Figure 7 Deviations of the Dimming Curve from the Ideal Case

Abbreviations

ADC
Analog-to-Digital Converter (ADC)

An analog-to-digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

LED
Light Emitting Diode (LED)

A light-emitting diode is a two-lead semiconductor light source which emits light when activated.

PWM
Pulse Width Modulation (PWM)

Pulse-width modulation is a technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

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