VQFN48
Layout Hints

VQFN48-29, -31

Application Note
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1 Abstract

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide a specific information what to consider when creating a Printed Circuit Board (PCB) Layout containing an integrated circuit in a VQFN48 package. This Application Note applies to the following package variants:

VQFN48-29, -31
2 Introduction

Besides designing rules and layout requirements originating from electromagnetic compliance also package related issues should be accounted for. This Application Notes gives an indication and suggestion what has to be considered when designing a layout of a PCB with an integrated circuit using specific VQFN48 packages with tie bars.
3 Layout Suggestion for VQFN48 Packages

3.1 Packages with Tie Bars
The P(G)-VQFN, Plastic (Green) Very Thin Profile Quad Flat Non Leaded Package (see Figure 1) is a near chip-scale plastic encapsulated package. It provides on the package bottom side perimeter pads and also a large die exposed pad, which is typically also soldered to the printed circuit board to get an optimum of electrical and thermal performance and board level reliability. “G” denotes “green” VQFN packages, which means lead-free package material set (RoHS compliant).

Features

- Optimized electrical performance with short leads
- Enhanced thermal performance through exposed die pad structure
- Leads and exposed die pad with solder plating
- Small footprint, thin package
- Package outline according to JEDEC MO-220

For further recommendations for Printed Circuit Board (PCB) assembly of VQFN packages see the Infineon Additional Information: “Recommendations for Printed Circuit Board Assembly of Infineon P(G)-VQFN Packages, DS7, May 2012”.

This Applications Note focuses on the PCB Layout with specific attention to the tie bars. The packages VQFN48-15, -19, -20, -22, -24, -48, -51, -52, -53, -54, -55, -56, -57 and VQFN48-29, -31 have visible tie bars on each corner which are connected to the lead frame (see Figure 1 red circles). In Figure 3 (Source: “Recommendations for Printed Circuit Board Assembly of Infineon P(G)-VQFN Packages, DS7, May 2012”) it can be seen that the lead frame is connected to the exposed pad and thus most likely connected to GND.

Figure 1 Engineering drawing of the VQFN48 package outline.
3.2 Recommendation for a Layout with Respect to Tie Bars

The layout and routing of trace pitches on a PCB close to tie bars has to be evaluated accurately with respect to the corresponding application and requirements. To prevent the tie bars from establishing shorts to any elements on the PCB it is required to ensure the isolation of any conducting elements (i.e. vias, resistors, circuits with no solder resist, ...). It needs to be ensured that no shorts are possible on the PCB to any conducting element.
4 Conclusion

The not masked tie bars are originating from the production process and have no specific functionality. The tie bars are not pins and are located in the corners of the package. It needs to be ensured in the application that there is no short between the tie bars and vias, wires or other conducting elements.
5 Additional Information

- For further information you may contact http://www.infineon.com/
## 6 Revision History

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