Using a capacitance-diode-lossless turn-off snubber circuit in telecom bricks

A new non-dissipative turn-off snubber circuit for secondary synchronous rectifier increases efficiency in center-tap PWM topologies

About this document

Scope and purpose

This document describes the design and performance advantages of using a **c**apacitance-**d**iode-**l**ossless **(CDL) snubber** to damp the high-frequency ringing due to the **reverse recovery body diode current** of the synchronous rectifiers (SRs), while increasing efficiency as well. The reverse recovery charge of the SRs is **recycled to the output in a non-lossy way**. The CDL snubber is used in Infineons 600 W FB-FB and FB-CT quarter and eight brick demo units using many of are mosfets, gate drivers and DHPx0x0N10N5 is a 100 V half-bridge Intelligent Power Modules.

The main Infineon components used for reference in the 600 W isolated quarter brick demos are:

- **Intelligent HB Power Stage** DHP1050N10N5, OptiMOS™ 100 V
- **OptiMOS™ 5 100 V** BSC050N10NS5, 100 V 5 mΩ, SuperSO8 power transistors
- **OptiMOS™ 6 40 V** BSC010N04LS6, 40 V 1 mΩ, SuperSO8 power transistors
- **EiceDriver™ 2EDL8114G** Infineon's isolated dual gate drivers
- **EiceDRIVER™ 2EDN7524G** fast dual-channel 5 A gate driver

Intended audience

This document is intended for power supply design engineers.

Table of contents

1 Background and CDL description

Full-bridge (FB) primary and center-tap secondary, or half-bridge (HB) primary and center-tap secondary are very popular topologies in telecom DC-DC bricks. They have the advantage that the secondary sync FETs are in parallel and driven from low-side drivers. However, the disadvantage is a split transformer, which causes a large leakage. This leakage necessitates the use of higher voltage FETs and an R-C snubber network, **Figure 1,** to damp the high-frequency ringing due to the **reverse recovery body diode current** of the SRs. All this results in loss of efficiency. A new **CDL** (all **SMD** devices), non-dissipative snubber circuit is shown in **Figure 6**. It recycles the **reverse recovery current** to the output capacitors, while enabling the use of lower-voltage SR FETs and the elimination of the dissipative R-C snubber network. A power loss, due to turn-off, of $\mathbf{P}_{loss\_toff}$ equals:

$$\mathbf{P}_{loss\_toff} = 1/2*(\mathbf{Q}_{ossvpk}*\mathbf{V}_{pk} - \mathbf{Q}_{ossvin}*\mathbf{V}_{in})*\mathbf{F}_s$$

where F_s is the switching frequency.

In addition, the ringing will necessitate the use of higher voltage, higher $R_{DS(on)}$ and slower secondary sync FETs. All this will reduce the efficiency and will cause larger EMI. One solution is to use an R_s, C_s R-C snubber to damp the ringing, see **Figure 1**. This is quite dissipative, and the value of C_s cannot be too large (excessive power loss). A solution that is not dissipative yet recycles the I_{rr} energy and is shown in **Figure 2**. The $\mathbf{C}_s$-$\mathbf{D}_s$-$\mathbf{L}_s$ network is a non-dissipative network that recycles the Q_{rr} charge back to the output capacitor. The large leakage, as shown in **Figure 2**, causes a lot of ringing when the body diode turns off, and the reverse recovery current, I_{rr}, resonates in the $L_{leakage}$ in series with the C_{oss} of the sync FET.

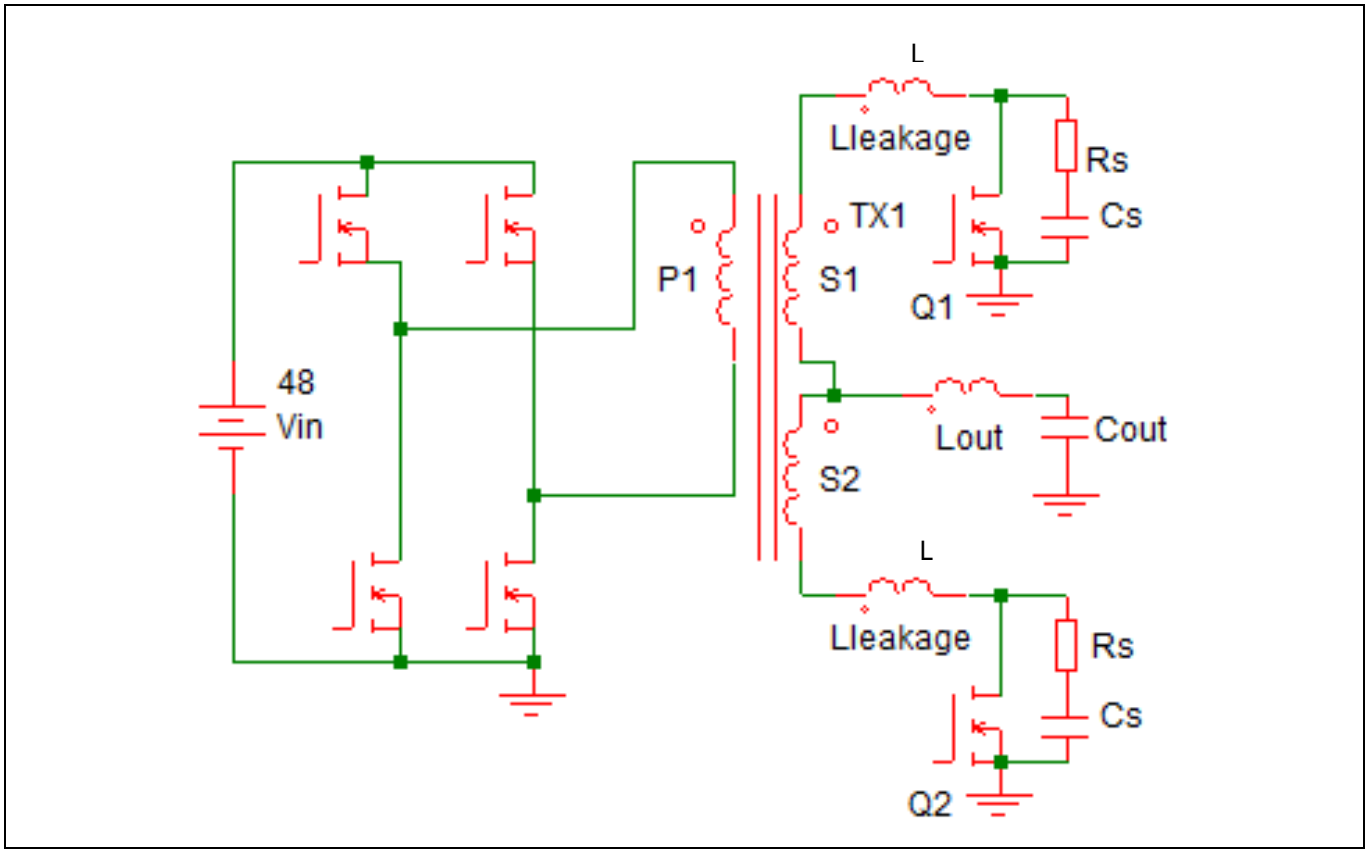

Figure 1 FB center-tap schematic

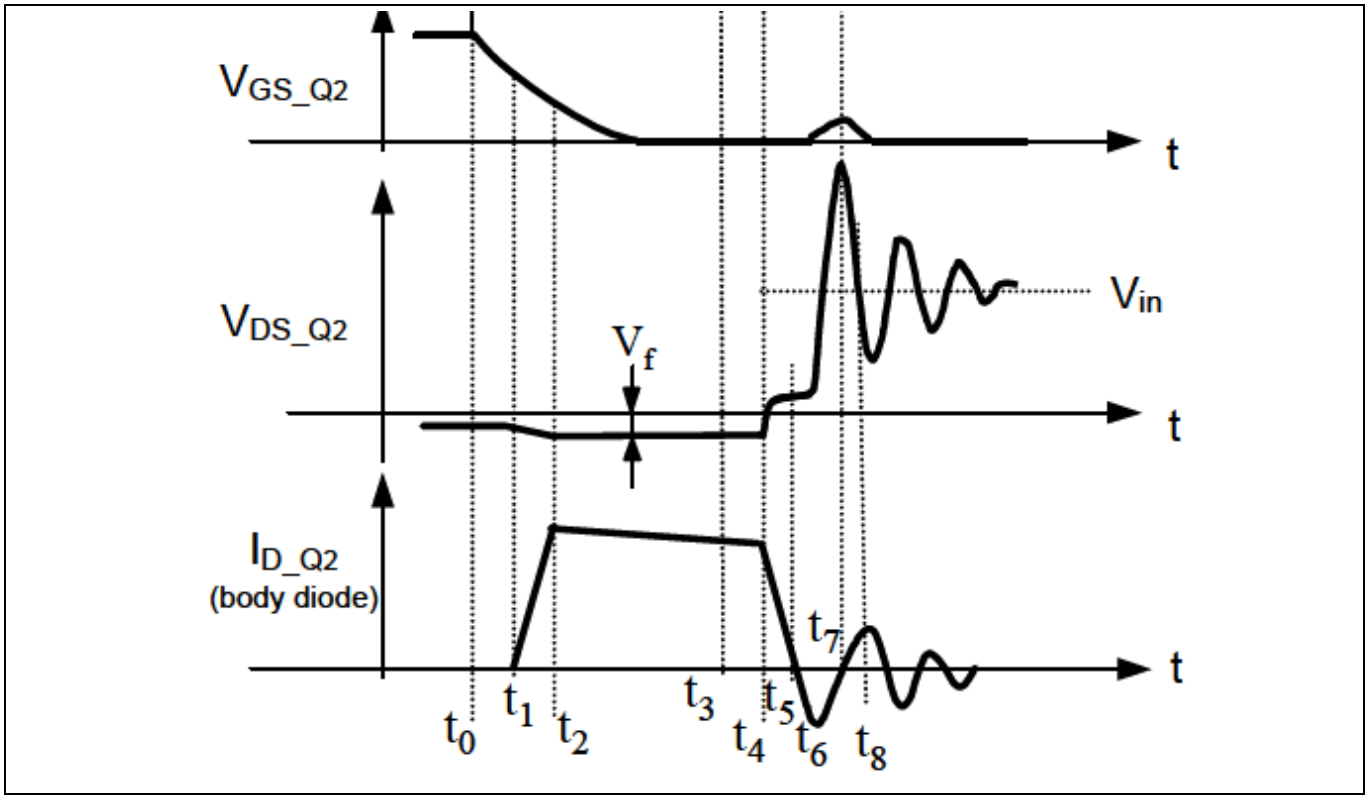

Figure 2 **FB center-tap turn-off timing**

Attention: ***The block diagram of the CDL snubber used on Infineon's quarter brick demo units is shown in Figure 3, Figure 4 and Figure 5. They are both FB-FB and FB-CT designs. Many of the Infineon componets used are highlighted in block diagram.***

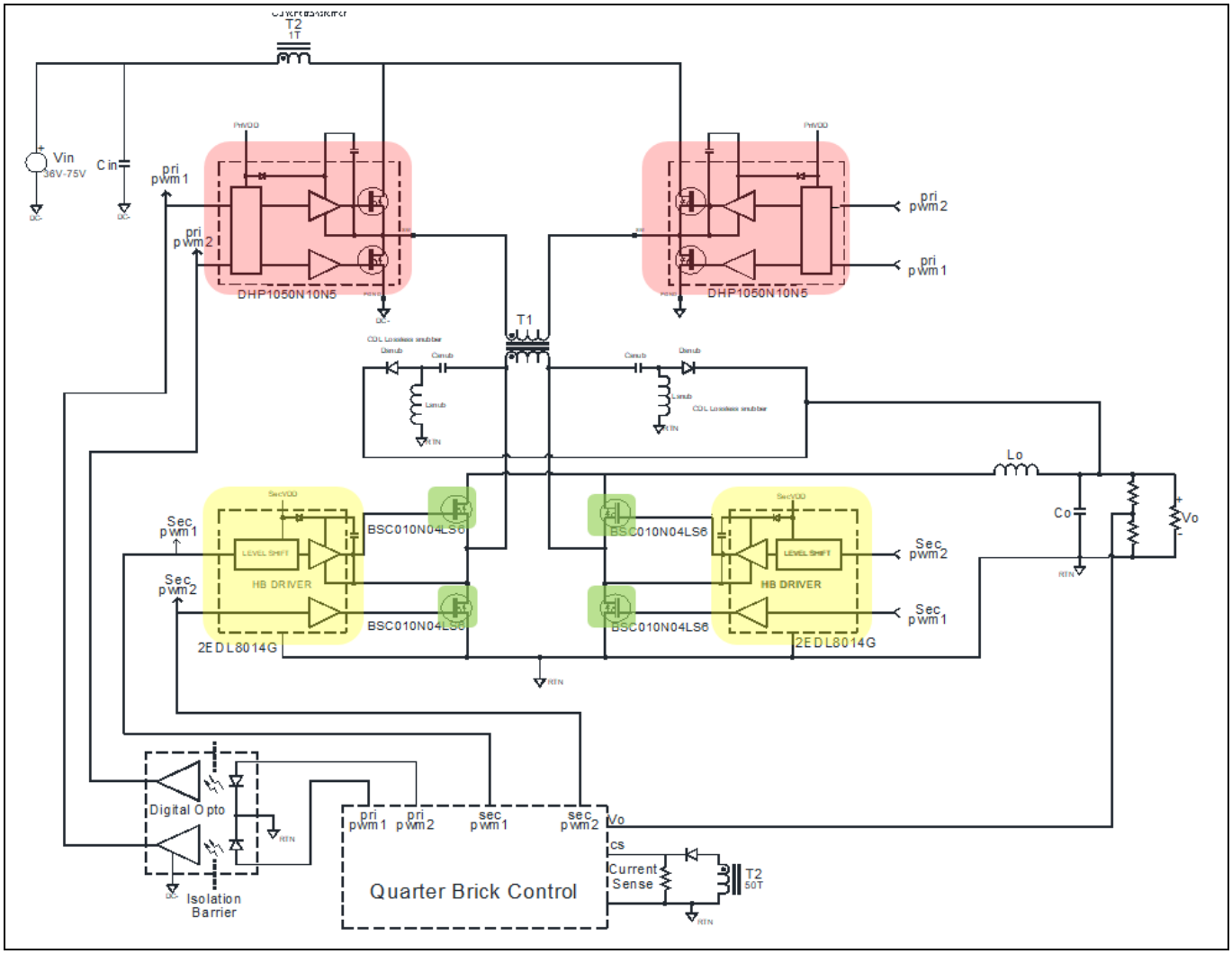

Figure 3 **Block diagram of CDL snubber used on Infineon 600W quarter brick demo using DHP1050N10N5 in primary side**

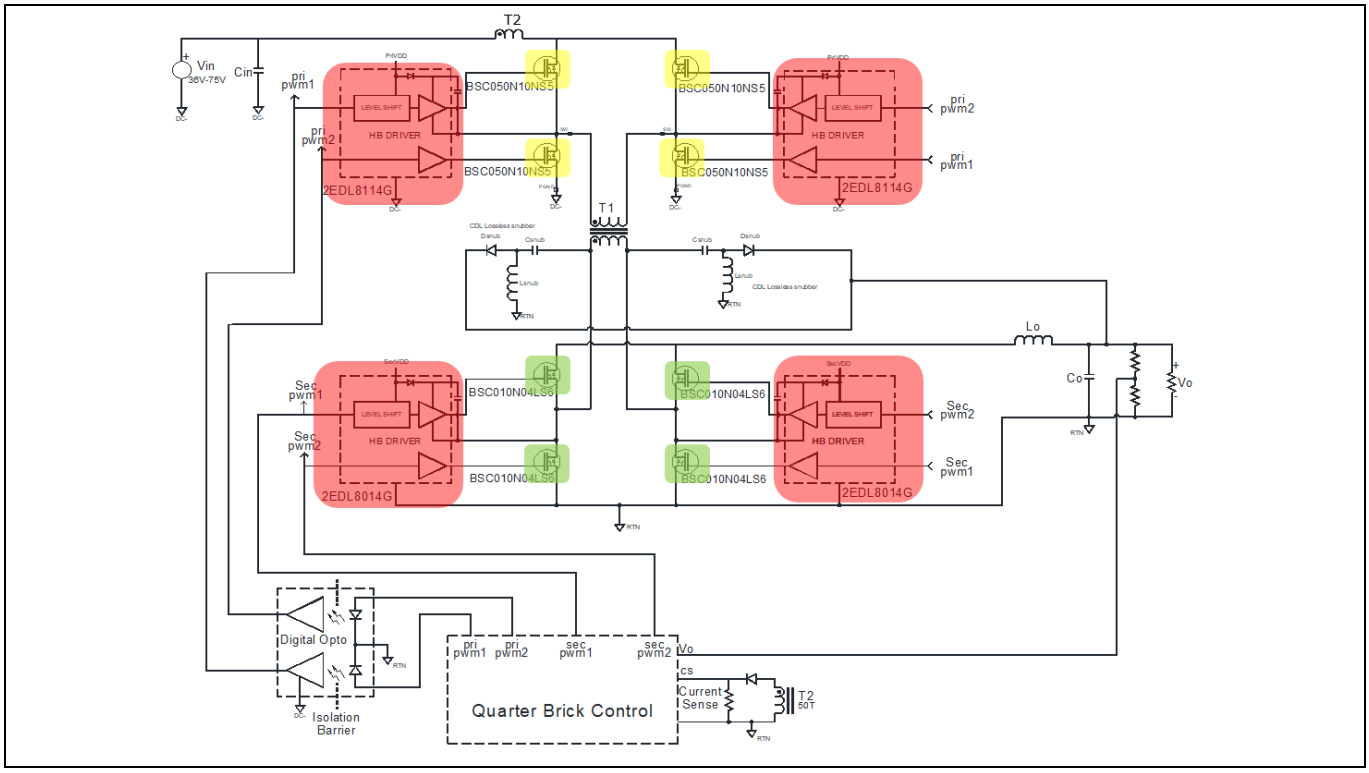

Figure 4 Block diagram of Infineon 600 W quarter brick using BSC050N10NS5 in primary side

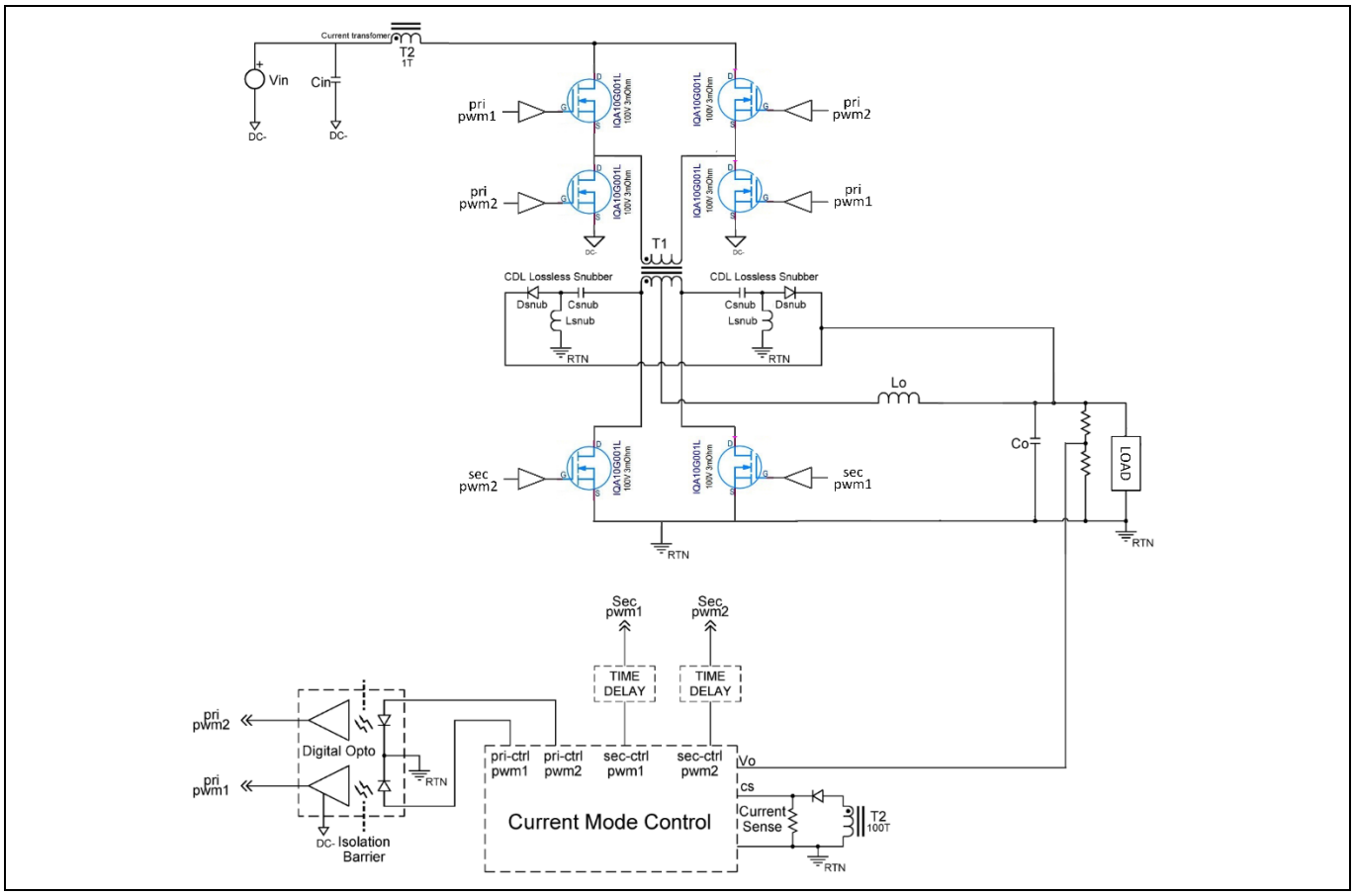

Figure 5 Block diagram of Infineon 840 W FB-CT quarter brick

2 The four operation modes with the CDL snubber

There are four modes of operation for the non-dissipative C_s-D_s-L_s circuit in **Figure 6**. We will use a FB center-tap design for evaluation, but the results could be applied to all switching topologies. The turns ratio of the transformer is n = 3:1 for this example.

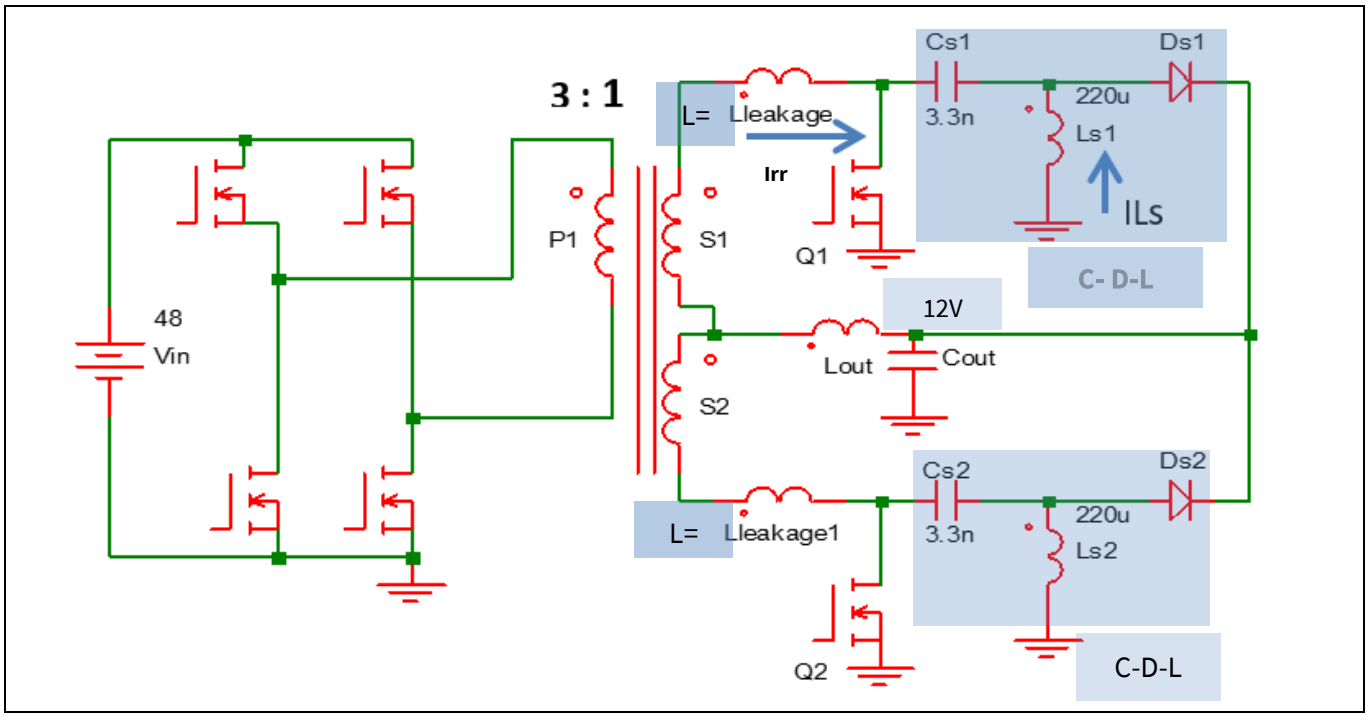

Figure 6 FB center tap with CDL snubber network on each phase

2.1 Mode 1_Fig.4.

Here the reverse recovery current of Q1, I_{rr}, charges C_s and C_{out}. C_s charges to a peak negative value of:

$$Vcspk = (Vsec - Vout) - \sqrt{(Vsec - Vout)^2 + Irr^2 * \frac{L}{Cs}} \qquad \text{Equation (1)}$$

Where V_{sec} = (V_{in}/n) x 2 in FB_ CT, n = xtfr, turns ratio = 3.

See derivation of equation (1) in paragraph **5.1**.

See simulated and measured waveforms in **Figure 10** and **Figure 11**.

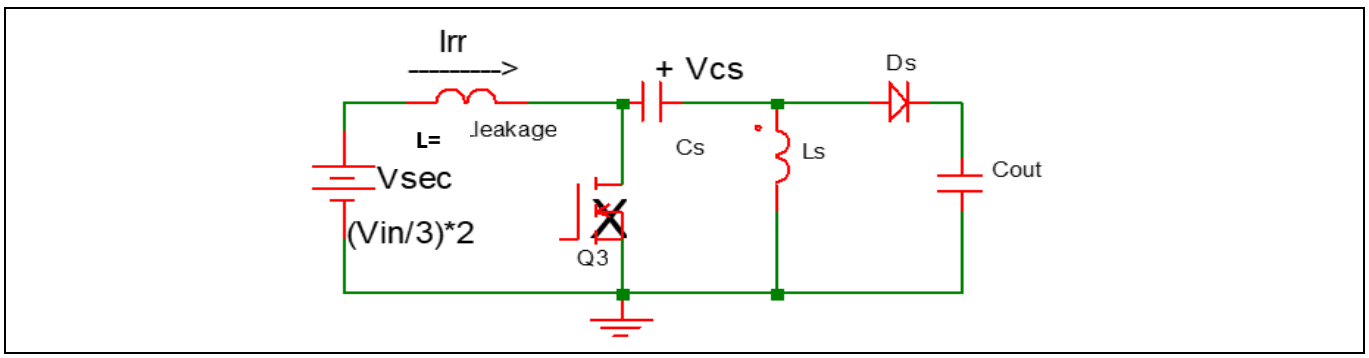

Figure 7 Mode 1 where C_s charged by I_{rr}

2.2 Mode 2_Fig. 5.

Here the current in L_s discharges C_s. Diode D_s is off. Assume 0 A in L_s, and V_{cs} (t = 0) is given by equation (1). The input source, V_{sec}, is the secondary D-S voltage during "off" state, namely:

$$V_{sec} = (V_{in}/3) \times 2 = 32\ V \qquad \text{Equation (1a)}$$

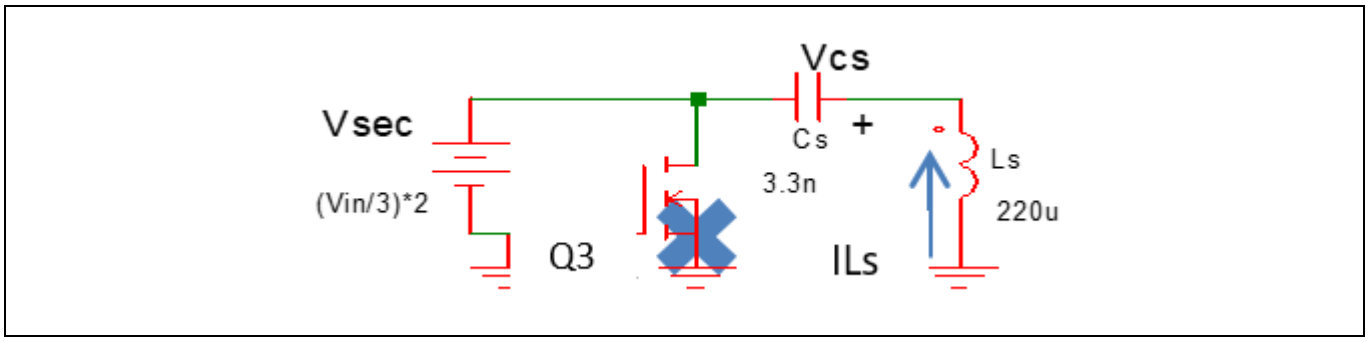

Figure 8 Mode 2 where C_s is charged by L_s

2.3 Mode 3_Fig. 6

Here the secondary FET Q3 is on again (during the "dead-time" all secondary FETs are on for better efficiency). Here the IL_s current charges the capacitor C_s to a positive voltage. When V_{cs} charges to V_{out}, diode D_s clamps the voltage across C_s to V_{out}.

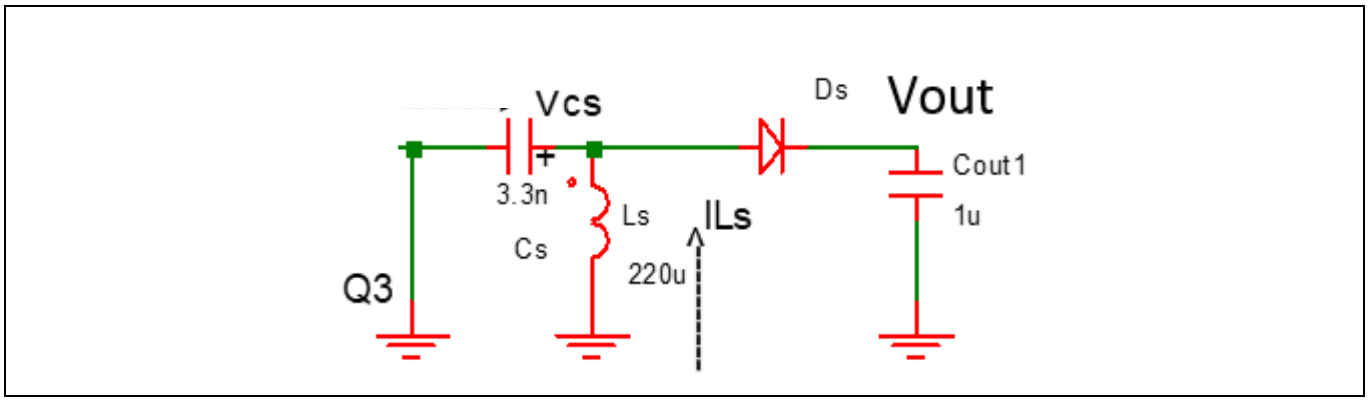

Figure 9 Modes 3 and 4, where C_s is charged by IL_s

2.4 Mode 4_Fig. 6

Mode 4 is the same as mode 3, except V_{cs} is clamped to V_{out}. It is waiting for the next FET turn-off cycle with the current stored in L_s holding D_s on and clamped to the output voltage. This will allow the next cycle turn-off clamp energy to be transferred to output.

3 Switching waveforms using the CDL snubber

The waveforms below were recorded from both simulation and actual measured switching waveforms. The voltage across C_s is given as shown below (also see the derivation in paragraph **5.1**):

$$Vcs(t) = (Vsec - Vout) - \sqrt{(Vsec - Vout)^2 + Irr^2 * \frac{L}{Cs}} * \sin(\omega * t + \rho) \qquad \text{Equation (2)}$$

$$\tan(\rho) = \frac{(Vsec - Vout)}{Irr} * \sqrt{\frac{L}{Cs}} \quad \text{Where } \omega = \sqrt{\frac{1}{L * Cs}}$$

Equation (2) is valid for mode 1, where in mode 1, C_s is being charged to V_{cspk} by I_{rr} of the secondary FETs.

A simulation of the circuit in **Figure 6** was done using SIMetrix and BSC014N060 secondary FETs. The input voltage was 48 V, load current 50 A. C_s = 3.3 nF, L_s = 220 µH (SMD 1210 parts), D_s = 2 A, 100 V Schottky diode. The simulation results show the four operation modes in **Figure 10**. **Figure 10** shows the complete switching cycle, along with a zoomed-in view of the secondary FET turn-off rising edge.

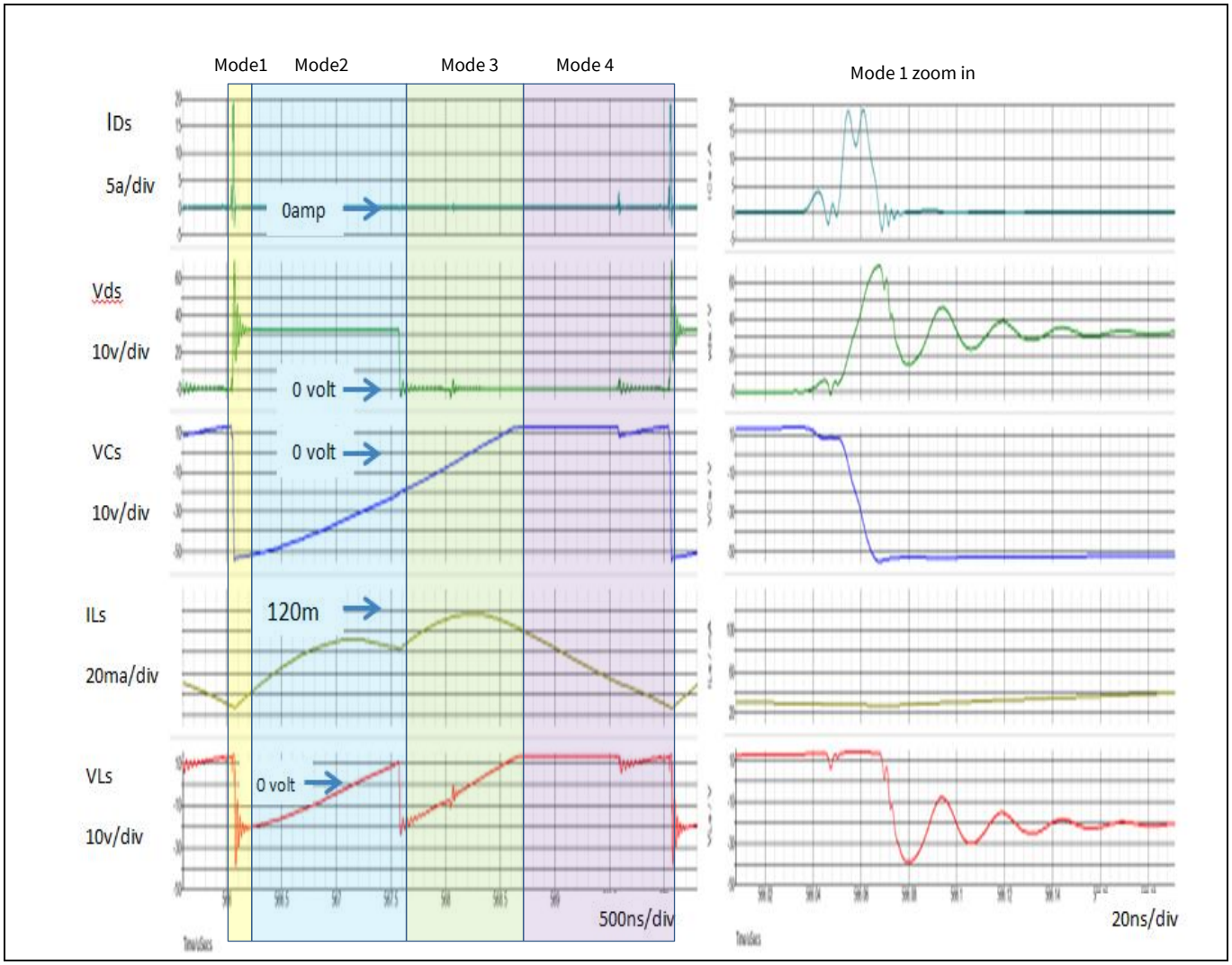

Figure 10 Simulated waveforms of CDL snubber using SIMetrix

3.1 Switching waveforms from actual circuit used on 600 W quarter-brick

The waveforms in **Figure 11** show the same switching waveforms as shown in the simulation taken on a 600 W quarter-brick using the CDL snubber. **Figure 11** depicts the V_{ds}, V_{cs}, IL_s and VL_s at V_{in} = 48 V, V_{out} = 12 V, C_s = 3.3 nF, L_s = 220 µF and D_s is a 2 A 100 V Schottky diode used in the CDL snubber. **Figure 11** shows the complete switching cycle along with a zoomed-in view of the FET turn-off rising edge taken on the 600 W quarter-brick.

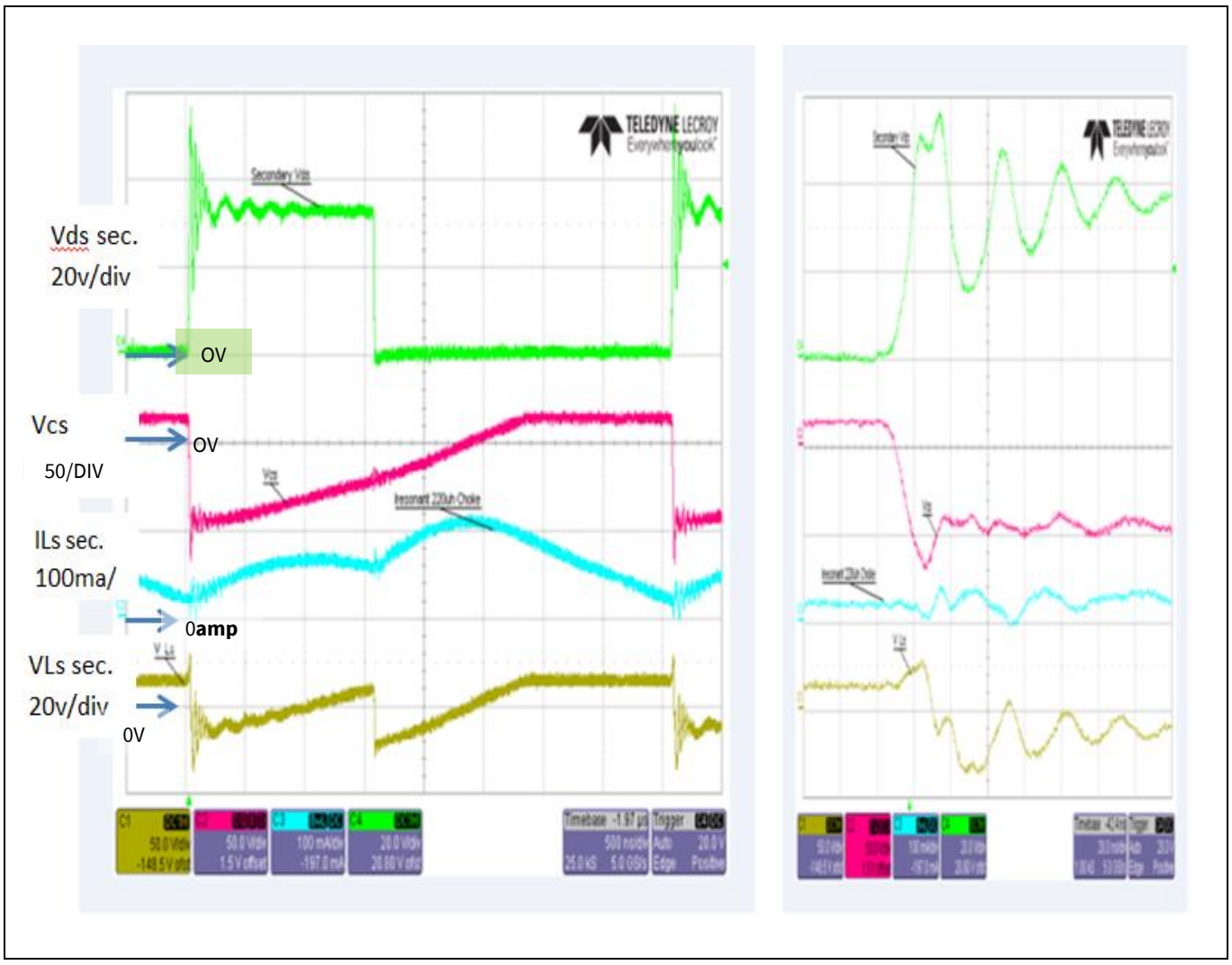

Figure 11 Measured waveforms taken on CDL snubber in 600 W quarter-brick

It can be seen in **Figure 11** that the simulated and measured waveforms are very similar.

4 Efficiency with and without CDL snubber

The efficiency was recorded at nominal input line, 48 V DC, with and without a CDL snubber installed on a 600 W FB center-tap quarter-brick test unit. When the CDL snubber was not used, an R-C snubber was used to damp the turn-off energy in secondary FETs. **Figure 12** shows the efficiency over output load range with and without the CDL snubber. It can be seen that we increase the efficiency over the entire load range when using the CDL snubber.

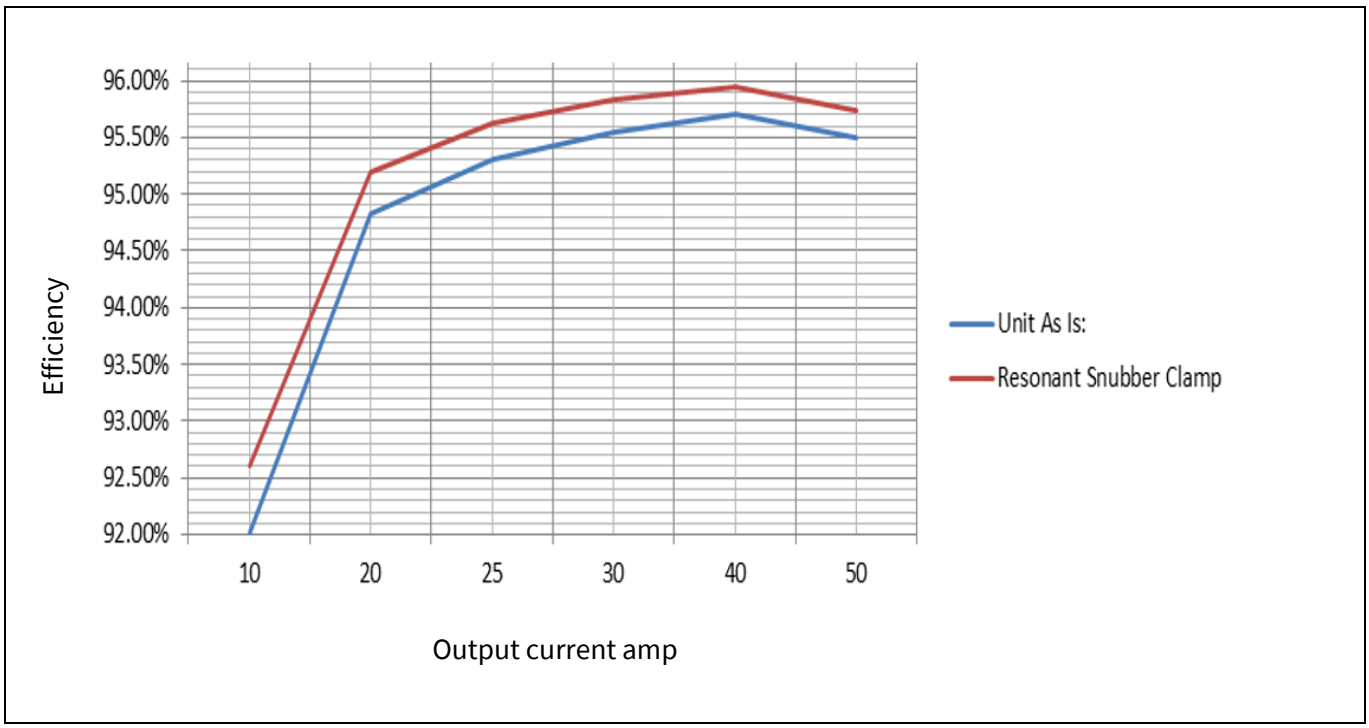

Figure 12 Efficiency with and without CDL snubber installed on 600 W quarter-brick

5 Equations for CDL snubber and numerical example

The equations for the CDL snubber values are shown below.

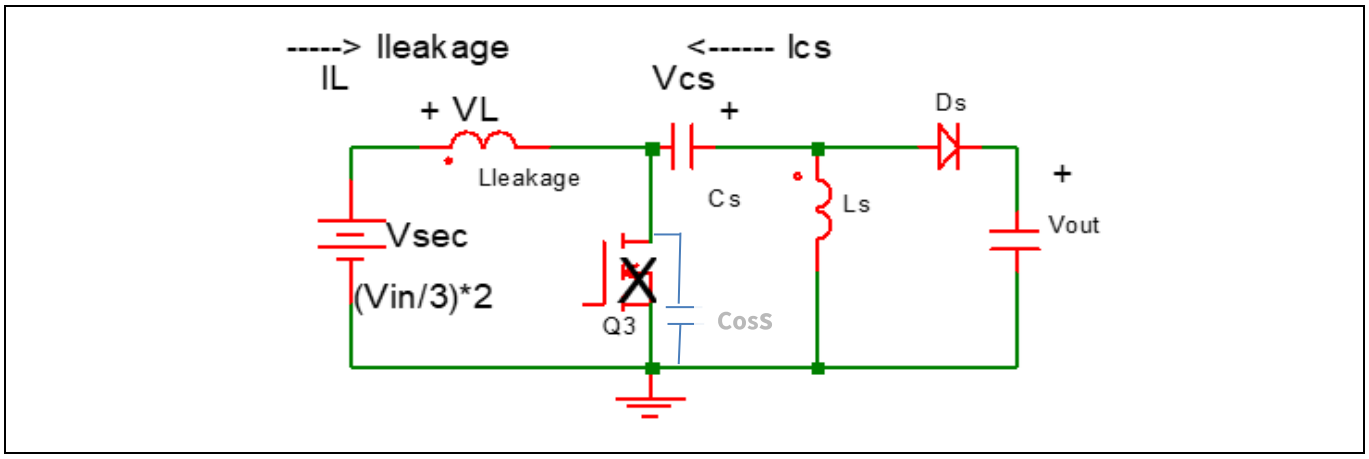

Figure 13 C_s charged by I_{rr} from FET turn-off

5.1 CDL equations

From **Figure 13** we have $Vsec - Vl = Vcs = Vout$ Equation (3)

$$Vl = L * \left(\frac{d}{dt} * I_L\right)$$ Equation (4)

$$I_L = -I_{cs} \qquad (I_c(\tau = 0) = -I_{rr}$$ Equation (5)

$$I_{cs=}C_s * \left(\frac{d}{dt} * V_{cs}\right)$$ Equation (6)

Substituting equations (4), (5) and (6) in equation (3) we get:

$$L * C_s * \left(\frac{d^2}{dt^2} * V_{cs}\right) + V_{cs} = Vout - Vsec$$ Equation (7)

Where L is equal to leakage inductance, and $\omega = \sqrt{\frac{1}{L*C_s}}$

The solution to equation (7), (with the initial conditions V_{cs} (t = 0) = V_{out}, and dV_{cs}/dt (t = 0) = $-I_{rr}/C_s$), is:

$$V_{cs}(t) = (Vsec - Vout) - \sqrt{(Vsec - Vout)^2 + {I_{rr}}^2 * \frac{L}{C_s}} * \sin(\omega * \tau + \rho) \qquad \text{Equation (8)}$$

$$\tan(\rho) = \frac{(Vsec - Vout)}{I_{rr}} * \sqrt{\frac{L}{C_s}}$$

This **assumes** the D-S capacitance of Q3, C_{oss}, is small, and C_{oss} charges from 0 V to V_{out} very fast.

When C_{oss} charges to V_{out}, then $\mathbf{V_{cs}}$ **= 0 V**, and diode D_s starts conducting.

5.2 Numerical example

As an example: V_{in} = 48 V, V_{sec} = (V_{in}/n) x 2, n = 3 = transformer turns ratio in center tapped secondary side:

$$V_{sec} = 36\ Volts \quad V_{out} = 12\ Volts \quad I_{rr} = 25\ Amps \quad L = 18\eta H \quad C_s = 4.7\eta F$$

Which results in a spike of:

$$V_{cspk} = (V_{sec} - V_{out}) - \sqrt{(V_{sec} - V_{out})^2 + {I_{rr}}^2 * \frac{L}{C_s}} = 43.6\ V$$

6 Summary

This document describes the Infineon-designed CDL non-dissipative snubber circuit and its advantages. You gain in efficiency while reducing the voltage stress on the secondary switching devices. We have implemented this snubber design into Infineon's demonstration designs. We have presented the schematic implementation of the CDL non-dissipative snubber into the secondary switching FETs. We have also presented the simulated and measured switching waveforms of the CDL snubber. We have finally given the equations for calculating the values of the Infineon-designed CDL non-dissipative snubber. This design proves that Infineon's CDL non-dissipative snubber has outstanding performance on DC-DC brick converters. The parts can be all SMD and do not require much space on your PCB.

7 References

[1] The **intelligent power module** (IPM) DHP1050N10N5, 100 V OptiMOS™ 5 family. Infineon offers a variety of IPMs, with different semiconductors in different packages and different voltage and current classes. These IPMs are separated into Compact, Standard and Performance families. Part of the IPMs is divided into the **CIPOS™ Nano**, **CIPOS™ Micro**, **CIPOS™ Tiny**, **CIPOS™ Mini** and **CIPOS™ Maxi** families. These energy-efficient intelligent power modules integrate the latest power semiconductor and ICs technology.

[2] **OptiMOS™ 5 100 V power MOSFETs** are especially designed for synchronous rectification in **telecom** and **server** power supplies. In addition, these devices can also be utilized in other industrial applications such as **solar**, **low-voltage drives** and **adapters**. Within seven different packages, the new OptiMOS™ 5 100 V MOSFETs offer the industry's lowest $R_{DS(on).}$ OptiMOS™ 5 100 V has a lower $R_{DS(on)}$ of up to 22 percentwhen compared to other similar devices. Additionally, compared to the previous generation, OptiMOS™ 5 80V has an $R_{DS(on)}$ reduction of up to 43 percent.

[3] The **OptiMOS™ 6 power MOSFET 40 V family** is optimized for a variety of applications and circuits, such as synchronous rectification in switched mode power supplies (SMPS) in servers, desktop PCs, wireless chargers, quick chargers and ORing circuits. Improvements in on-state resistance ($R_{DS(on)}$) and figure of merits (FOM – $R_{DS(on)}$ x Q_g and Q_{gd}) enable designers to increase efficiency, allowing easier thermal design and less paralleling, leading to system cost reduction.

[4] **2EDL8x1x** is a high-side low-side driver designed for advanced switching converters such as in telecom, low voltage drive and solar applications. 2EDL801x takes in independent inputs with built-in hysteresis for enhanced noise immunity, whereas 2EDL811x takes in differential input with built-in hysteresis for enhanced noise immunity. 2EDL811x's inherent shoot-through protection ensures the robustness of the system. 4ns maximum delay matching ensures volt-second balance and avoids magnetic core saturation.

[5] CoolGaN™ 100 V MV e-mode power transistor IQA10G001L datasheet.

[6] EiceDRIVER™ **2EDN7524G datasheet**. **2EDN7524G** is a fast dual-channel 5 A gate driver optimized for driving both standard and Superjunction MOSFETs, as well as GaN power switching devices.

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-05-31	Initial release

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