Q-DPAK Full Bridge V2.1 Evaluation Board user guide

About this document

Scope and purpose

This document is the user guide for the Q-DPAK Full Bridge V2.1 Evaluation Board (ISPN: EVAL_QDPAK_FB_V2_1). It provides an overview of the eval board hardware, describes its main functionality, and provides step-by-step instructions for operating the board and performing experiments in a lab environment.

Intended audience

This document is intended for developers, researchers, and professionals in power electronics who are interested in evaluating the latest silicon carbide (SiC) power technology from Infineon Technologies. The intended users must be trained in working with high-voltage equipment.

Evaluation Board

This board demonstrates the optimal usage of generation two CoolSiC™ 750 V G2 SiC power MOSFETs (“AIMDQ75R016M2H”) in top-side-cooled “Q-DPAK” packages [1] in a full-bridge topology. Electrical experiments (such as single- or double-pulse measurements) can be performed and the voltages of the SiC MOSFETs can be observed. Moreover, the eval board itself serves as a demonstrator of an optimal PCB design showing the correct usage of latest-generation wide-bandgap semiconductors in top-side-cooled packages. The complete design resources (such as the schematic, BOM, and layout) are available as complete Altium-project via www.infineon.com.

Figure 1 Picture of the Q-DPAK Full Bridge V2.1 Evaluation Board

About this document

Note: *This is an application-oriented eval board with an optimized layout for fast switching. This eval board is not a switching-loss evaluation platform because it does not contain a current sensor within the commutation loop. For switching-loss evaluation boards, refer to Infineon's complementary eval boards on www.infineon.com.*

Note: *This eval board is built for single pulses, rather than continuous switching because it comes without an assembled heatsink. A heatsink can be mounted additionally to enable continuous high-power operations.*

Note: *This eval board does not comply with all safety, EMI, and quality standards (such as UL and CE) required for commercial applications.*

Ordering information

Use the following information on www.infineon.com to order this eval board:

ISPN	EVAL_QDPAK_FB_V2_1
OPN	EVALQDPAKFBV21TOBO1
SP No.	SP00612907
SA No.	SA006129076

Additional support and assistance

For additional support and assistance, see Infineon Developer Community [2] or use our MyCases support system [3] to get in contact with the Infineon experts.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 500 V_{DC}. When measuring voltage waveforms by oscilloscope, high voltage probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the system, wait at least five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in injury or death.*
	**Warning:** *Remove or disconnect power before you disconnect or reconnect wires or perform maintenance work. Wait at least five minutes after removing power to discharge the bus capacitors. Failure to do so may result in injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assembly's sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 Overview

The Q-DPAK Full Bridge V2.1 Evaluation Board is a platform to evaluate the switching performance of Infineon's CoolSiC™ 750 V G2 silicon carbide MOSFETs in Q-DPAK packages.

The board uses four 750 V CoolSiC™ switches in a full-bridge assembly, corresponding Infineon gate drivers, small DC-DC converters providing the isolated voltage for each domain, and passives to support the DC link and to terminate power loops.

The EVAL board is designed to be as flexible as possible, showcasing the optimum usage of high-speed switching devices in Q-DPAK packages. Therefore, the placement and design of the power loop was optimized towards high-speed switching performance.

Each MOSFET can be controlled by external PWM signals provided via SMA terminals. You need to provide external load inductors (e.g., the main inductor for a PFC) via high-voltage (HV) terminals.

	**Caution:** *This eval board does not contain overtemperature, overcurrent, overvoltage protection circuits . Please safeguard the electronics with external measures.*
	**Caution:** *The eval board does not contain any control logic. These features must be realized externally according to your requirements.*
	**Caution:** *Always operate the boards only within the limits specified in this document.*
	**Caution:** *This eval board is built for single pulses, rather than continuous switching because it comes without an assembled heatsink. A heatsink can be mounted additionally to enable continuous high-power operations.*
	**Caution:** *This eval board does not comply with all safety, EMI, and quality standards (e.g. UL, CE) required for commercial applications.*

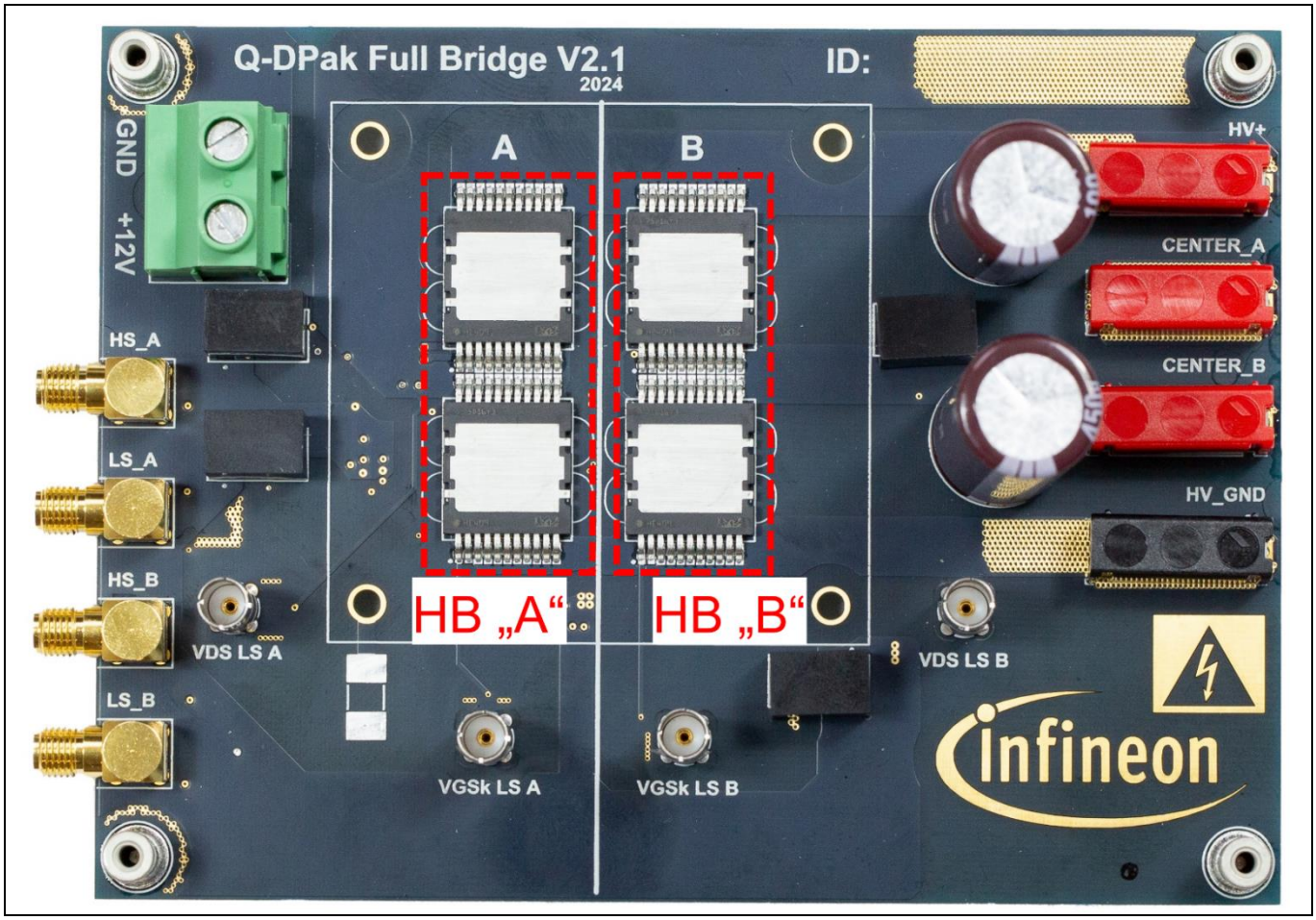

Figure 2 Top view of the eval board with indication of half-bridge (HB) “A” and HB “B”

1.1 Scope of supply

The evaluation board provides a fully tested PCB to evaluate Infineon’s latest high-voltage discrete silicon carbide MOSFETs. The eval board utilizes following Infineon products:

- AIMDQ75R016M2H: Infineon CoolSiC™ G2 Automotive Power MOSFET 750 V
- 2EDB9259Y: Infineon EiceDRIVER™ dual-channel isolated gate driver IC in 150 mil DSO package
- BAT165: Infineon medium power AF Schottky diode

The eval board is fully tested for electrical testing with limited energy (such as double-pulse test). You can mount a heatsink for thermal management, but it does not come with the heatsink mounted. The drillings on the PCB are compatible with the ATS-61600W-C2-R0 heatsink from Advanced Thermal Solutions, Inc. [4] or similar heatsinks from other vendors.

To optimize the thermal interface for devices in Q-DPAK package, follow the guidelines provided in the application note: Innovative top-side cooled package solution for high-voltage applications [5].

1.2 Block diagram

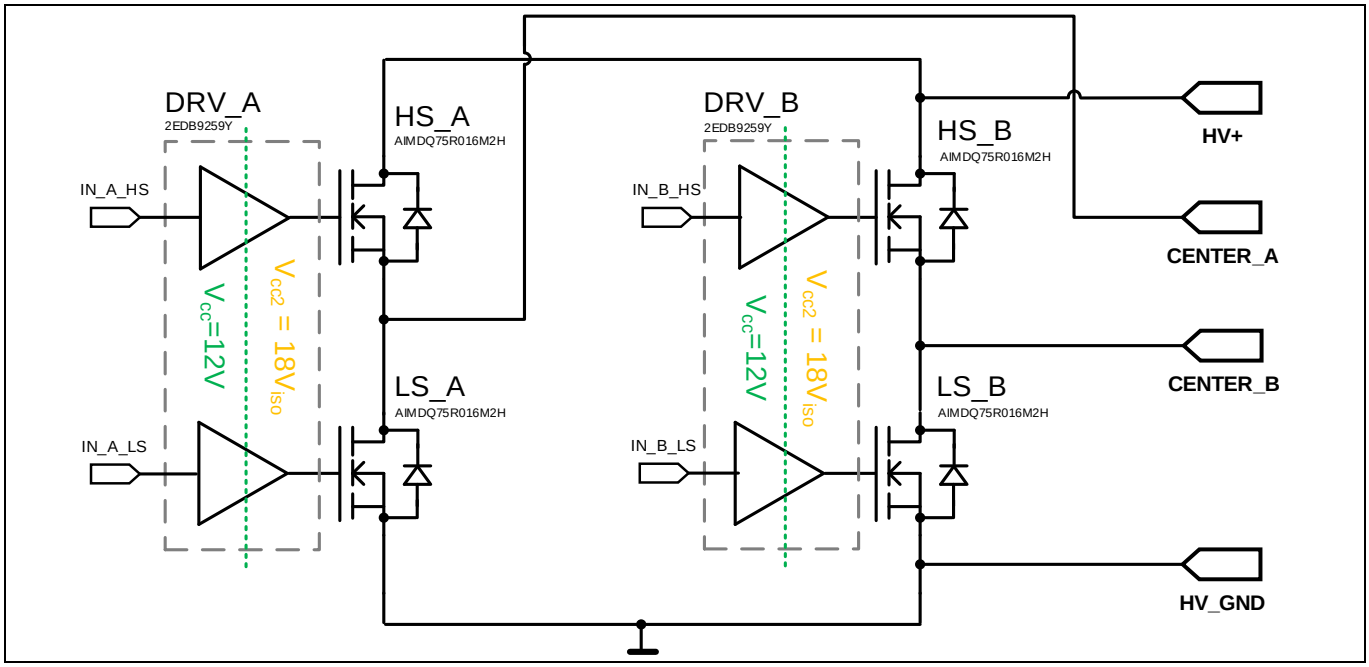

Figure 3 Block diagram of eval board, showing the full-bridge topology consisting of four 16 mΩ SiC G2 power MOSFETs (AIMDQ75R016M2H) with their respective MOSFET drivers (2EDB9259Y)

1.3 Main features

- Simple eval board comprising a full-bridge topology to enable highest flexibility for lab evaluation
- Building block for lab evaluation of different applications such as PFC and soft-switching DC-DC converters
- Optimal PCB layout enabling fastest switching
- Operation of board in single- and continuous PWM operation possible
- 2.6 mm clearance between high-voltage potentials on the top and bottom layers
- 0.6 mm clearance for inner layers
- Optimized gate-loop design for high-speed driving
- Probing ports for drain-to-source voltage (V_{ds}) and gate-to-Kelvin source voltage (V_{gsk}) for both half-bridges

1.4 Board parameters and technical data

The following table specifies the main parameters for the eval board. Operate the eval board within these limits to ensure a safe and correct operation.

Table 2 Parameter

Parameter	Symbol	Conditions	Value	Unit
Maximum input voltage	$V_{HV,max}$	DC voltage applied between HV+ and HV_GND	500	V
Maximum commutation current on HB “A”	$I_{L,max@500V,A}$	Maximum allowed inductor current on HB “A” at Vin = 500 V	100	A
Maximum commutation current on HB “B”	$I_{L,max@500V,B}$	Maximum allowed inductor current on HB “A” at Vin = 500 V	90	A

Overview

Parameter	Symbol	Conditions	Value	Unit
Nominal LV input voltage	$V_{cc,LV}$	Regulated DC voltage supply with at least 500 mA current capability	12	V
PWM input “ON level”	$V_{PWM,ON}$	PWM signal on IN_A_LS, IN_A_HS, IN_B_LS, and IN_B_HS terminals. Driving signal at high-impedance	3.3	V
PWM input “OFF level”	$V_{PWM,OFF}$	PWM signal on IN_A_LS, IN_A_HS, IN_B_LS, and IN_B_HS terminals. Driving signal at high-impedance	0	V
Absolut maximum drain-to-source voltage	$V_{DS,MAX}$	Absolute maximum allowed transient voltage, measured across drain and source for this EVAL board. For end applications using 750 V SiC G2, refer to product datasheets	650	V

2 System and functional description

2.1 Getting started

1. Unpack the eval board and check it for visible damages
2. Prepare a lab bench with the following equipment:
   - A low-voltage DC source
   - A PWM generator
   - A high-voltage DC source
   - A power inductor (see Figure 11)

2.2 Basic operation: double-pulse switching

This section describes how to operate the eval board in double-pulse mode. This basic setup can be used to evaluate the turn-on and turn-off voltage transients of Infineon's G2 silicon carbide MOSFETs. The basic operation has the following sequence:

1. One MOSFET is turned on to magnetize an external inductor with the intended current
2. The MOSFET is turned off and the current is taken over by the body diode of the second MOSFET
3. A subsequent short pulse turns on the MOSFET again before it turns off again
4. The total energy stored in the inductors is dissipated over the body diode

The turn-on and turn-off behavior of the MOSFETs can be investigated.

Figure 4 shows one method of how the double-pulse setup can be realized with the eval board. The proposed setup shows the inductor being connected in parallel to the high-side MOSFET of HB "A". The MOSFET is labelled "HS_A", which indicates the high-side transistor in half-bridge "A". Like this, passive probes on the oscilloscope can be used to measure the voltages in reference to the HV_GND voltage directly via the probe holders (see Figure 9 and Figure 10).

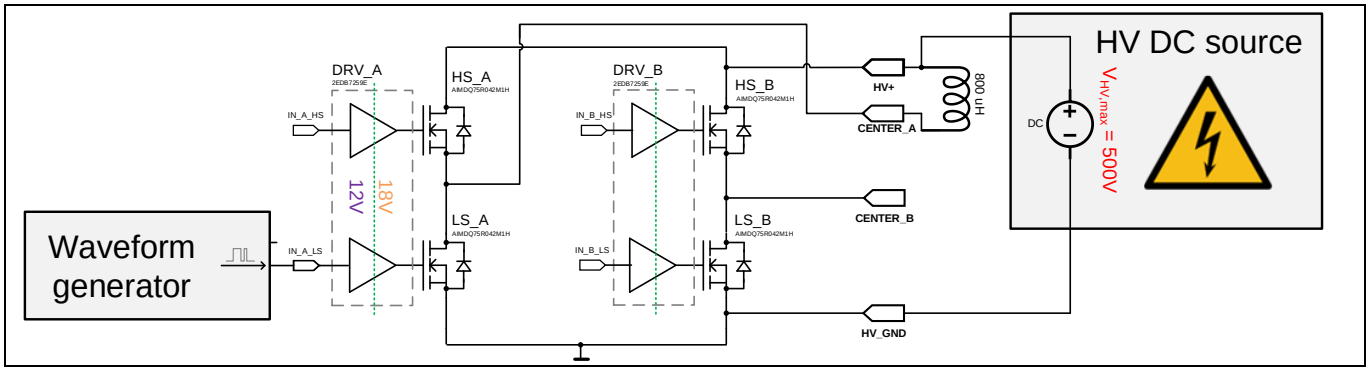

Figure 4 Schematic for double-pulse setup (simplified)

Note: The inductance value (800 µH) shown in this document (Figure 3) is only an example. The eval board can be used together with different inductor values if the timing of the PWM input signal is adapted accordingly.

2.2.1 Cabling setup

1. Supply the 12 V DC (low voltage; LV) on the X0 terminal. Ensure the correct polarity as shown in Figure 5

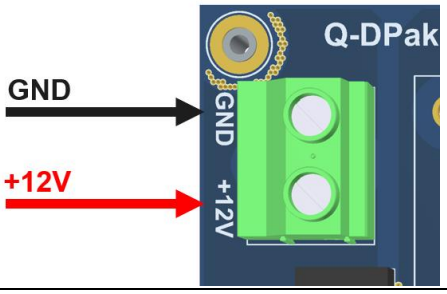

Figure 5 Supply 12 V on connector "X0" as shown above

2. Connect the PWM input signal. For the basic operation, only one MOSFET (the low-side MOSFET of Leg "A", called "LS_A") is supplied with a PWM signal. Figure 6 shows the correct cabling to operate the low-side MOSFET of HB "A"

Note: The ground connection of the PWM signals is the same ground as the low-voltage ground.

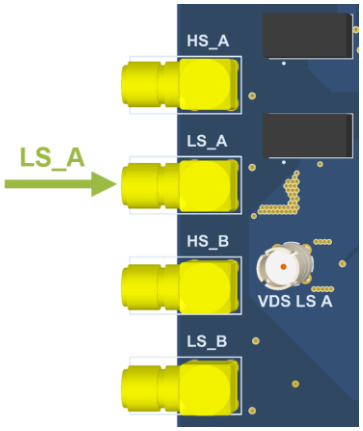

Figure 6 Connection of PWM input signal for "LS_A" MOSFET for single/double pulse switching

3. Connect the load inductor and the HV voltage supply to the PCB via the banana jacks as shown in Figure 7

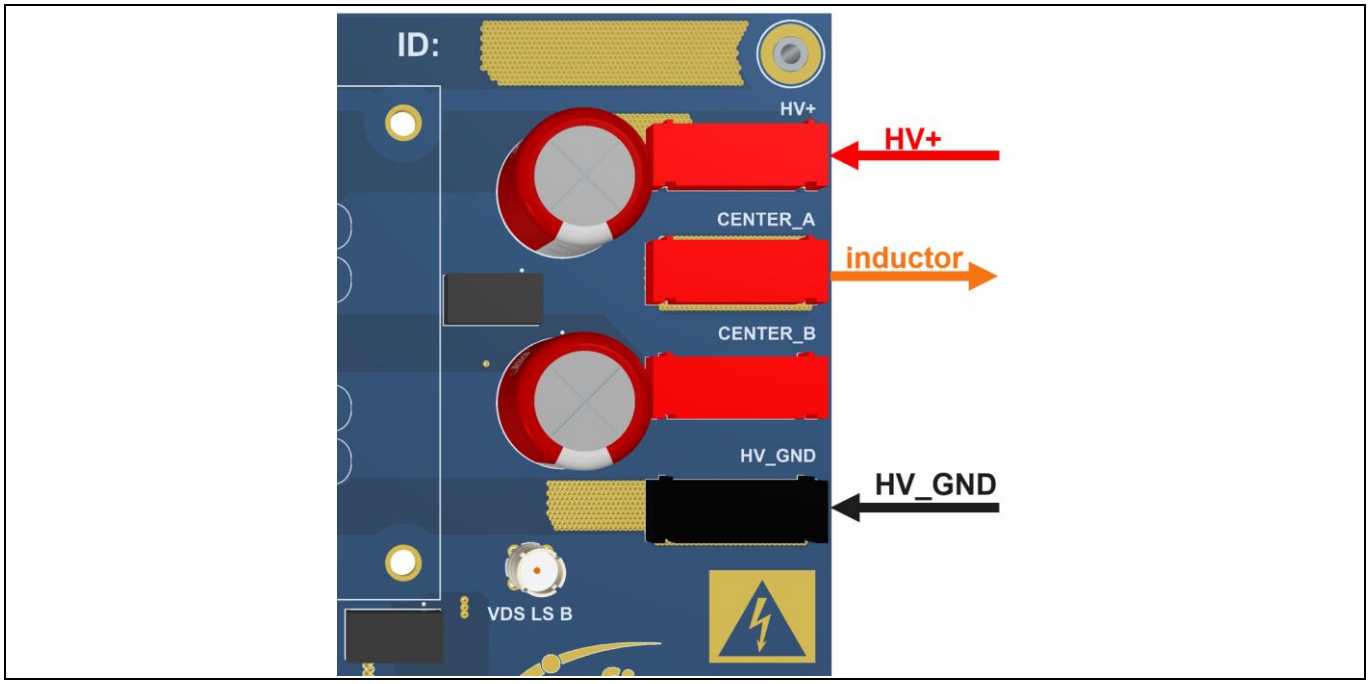

Figure 7 Cabling on HV terminals for single-/double-pulse testing utilizing half-bridge “A”

The board is ready for double-pulse operation. Figure 8 shows an overview of the complete cabling setup.

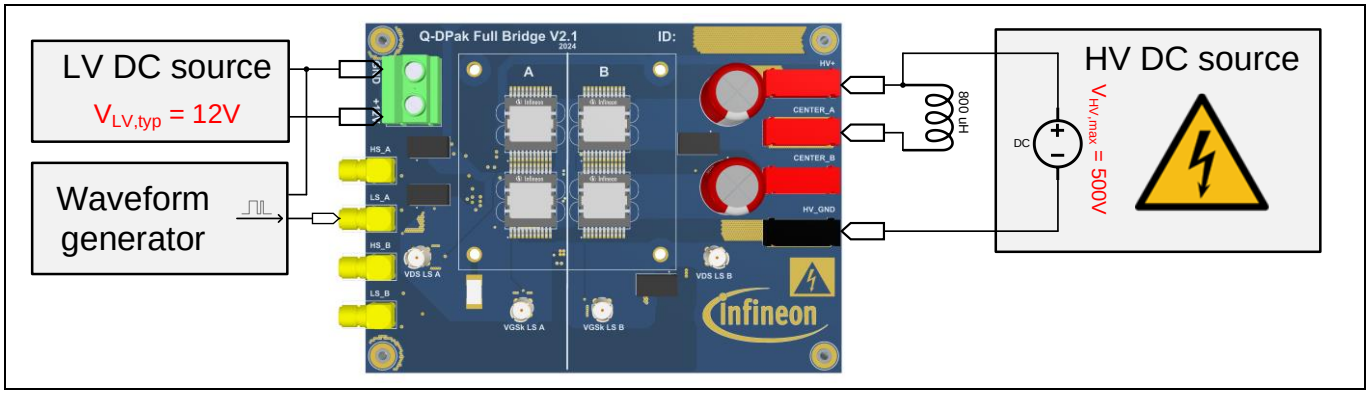

Figure 8 Complete cabling arrangement for double-pulse testing (utilizing half-bridge “A”)

4. Connect the passive probe for the drain-to-source voltage measurement as shown in Figure 9

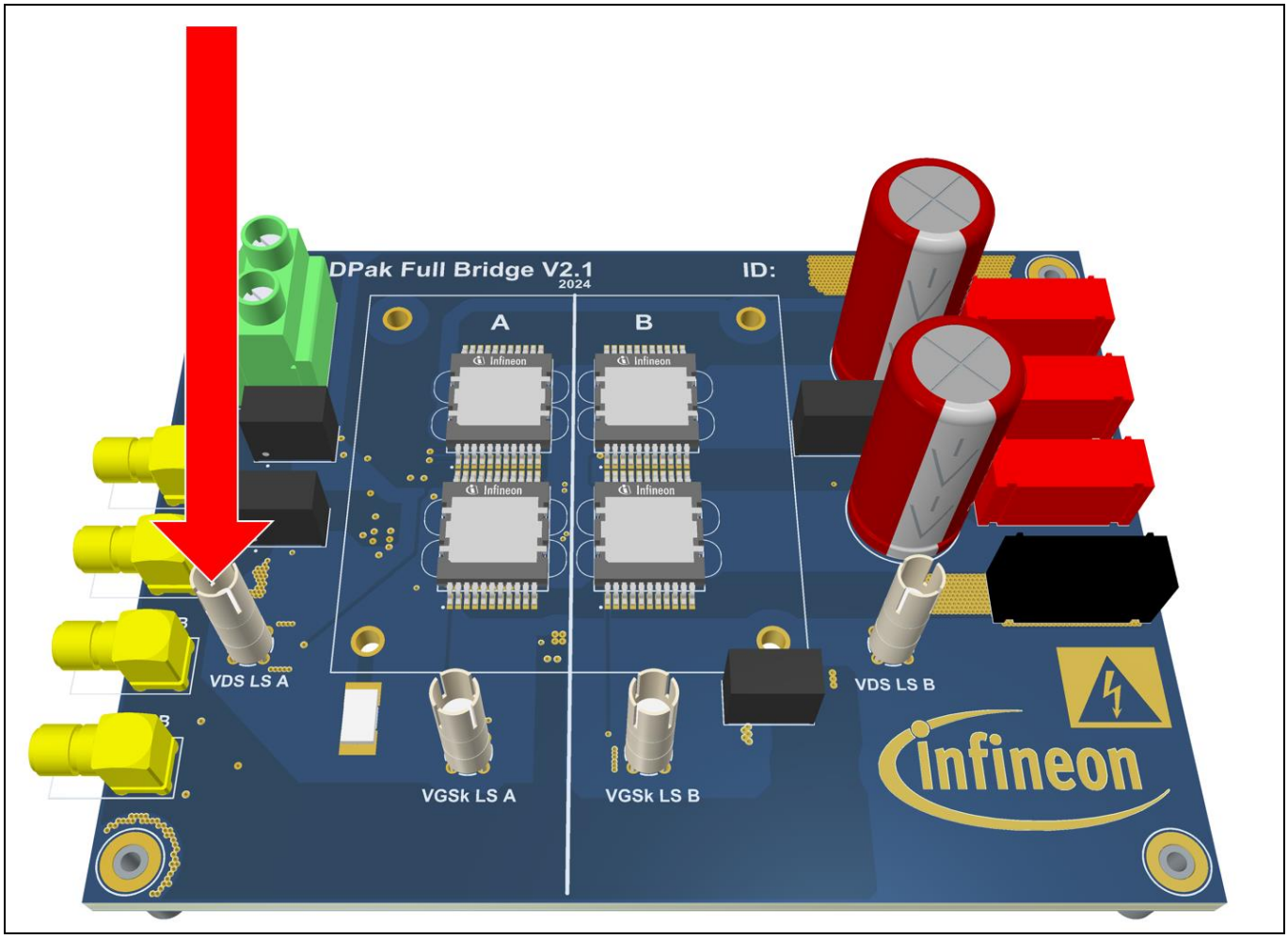

Figure 9 Connection for passive probe to measure the drain-source voltage of MOSFET “LS_A”

To measure the gate-to-Kelvin source voltage (V_{gsk}), refer to Figure 10.

Note: The ground connection of the probe refers to the Kelvin source pin of MOSFET “LS_A”. This is different from the ground to V_{DS} probe holders, which refers to their respective power grounds (source connection of the MOSFET “LS_A”, resp. “LS_B”).

Note: If the V_{gsk} voltage is measured together with the V_{ds} voltage, use a differential probe to avoid shorting signals via the oscilloscope.

Note: To measure multiple signals, use the sequence. Infineon recommends using only one passive probe at a time to get the best measurement results. Disconnect all other probes to avoid short-circuits or common-mode issues, unless you are using only different probes.

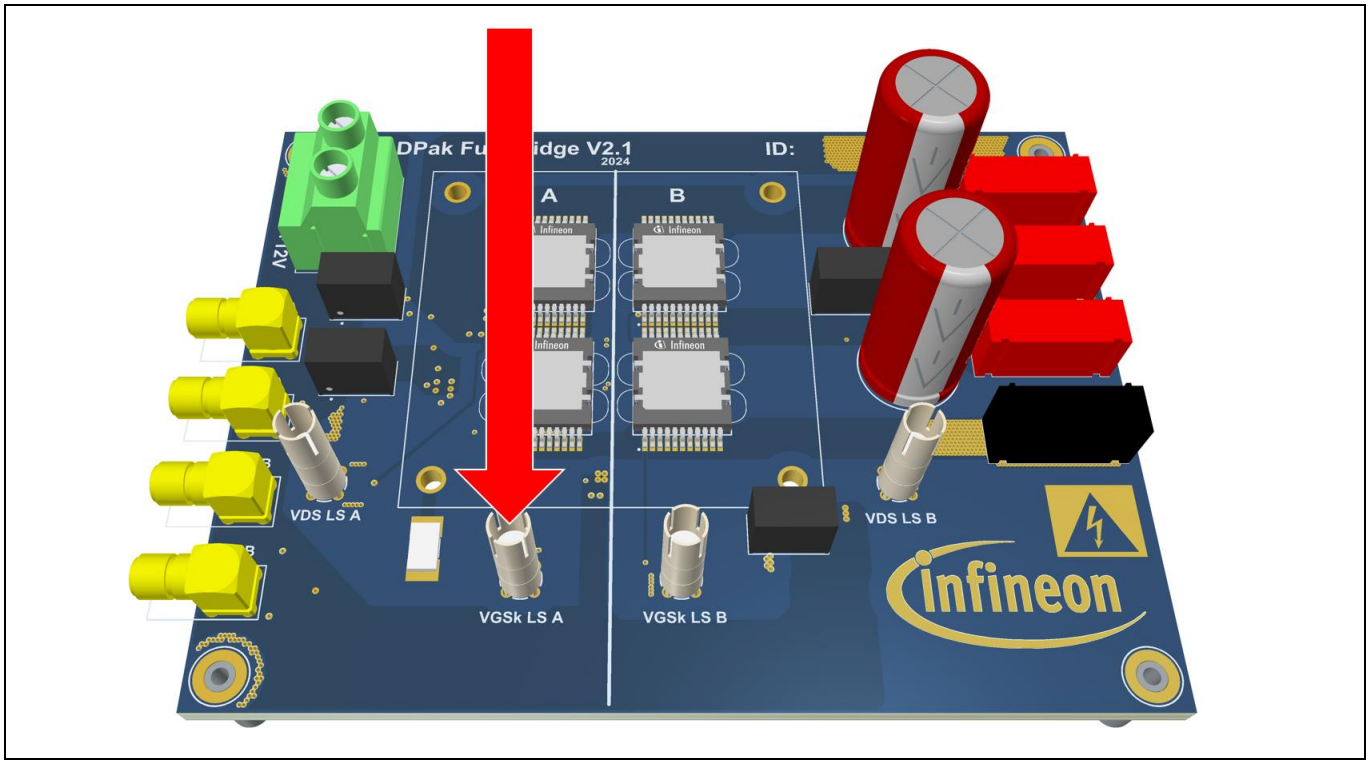

Figure 10 Probe holder for measuring the gate-to-Kelvin source voltage (V_{gsk}) of MOSFET "LS_A"

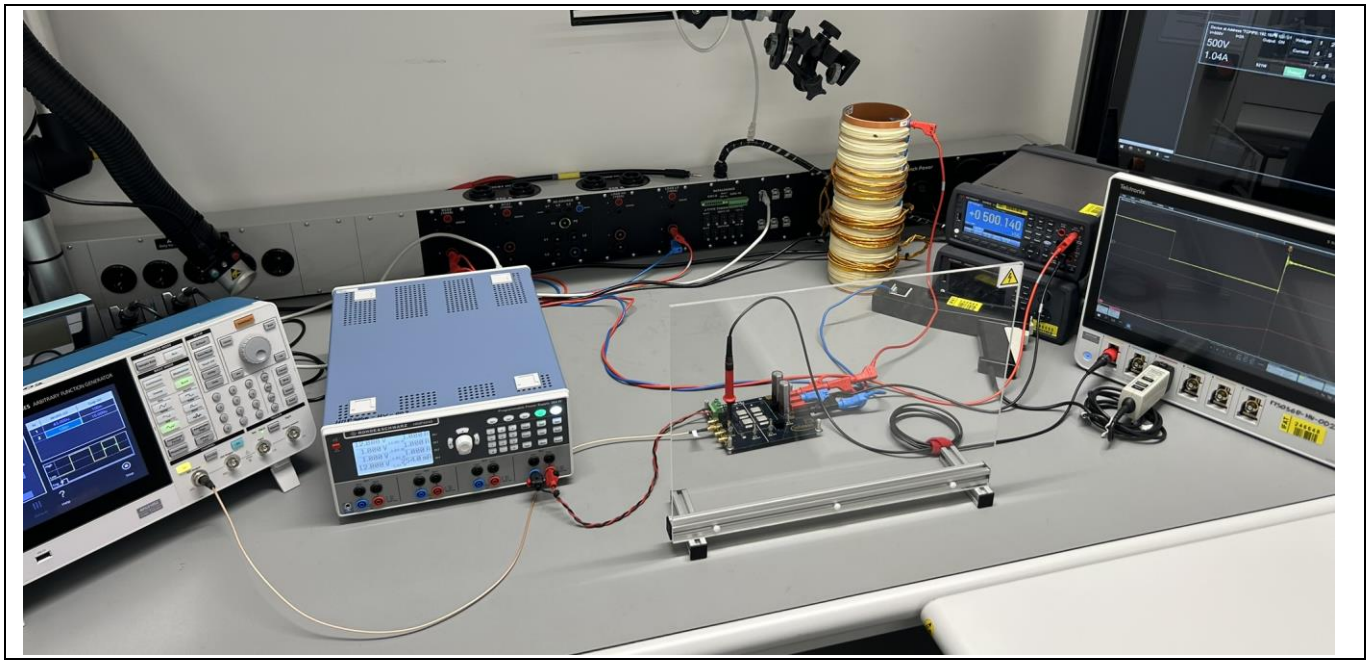

Figure 11 Lab setup for double-pulse testing while measuring the drain-to-source voltage (V_{DS}) via the corresponding probe holder

2.2.2 Measurement results

This section shows example waveforms acquired with the double-pulse setup on HB "A" (see Section 2.1). The same results can be acquired using HB "B", but with a lower limit of the maximum commutation current (see Table 2).

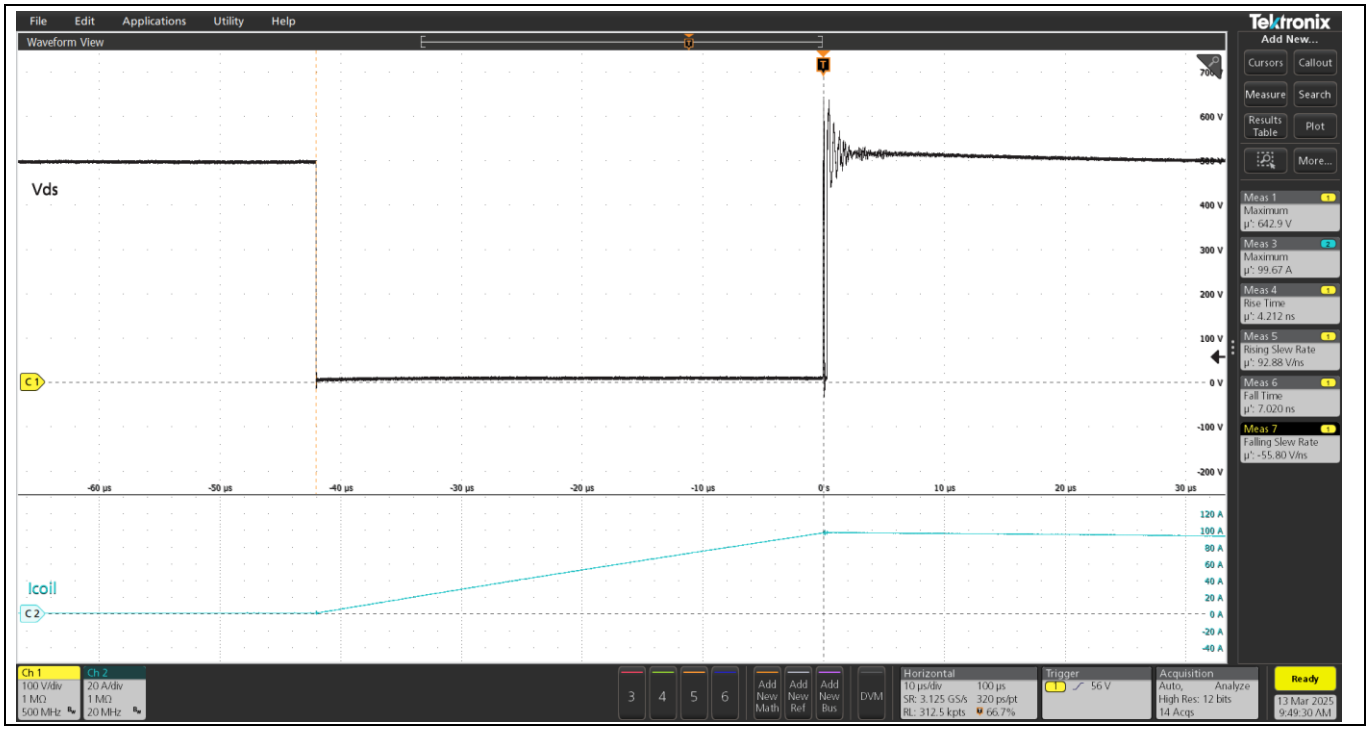

Figure 12 **Double-pulse waveform: The black waveform shows the V_{ds} voltage on MOSFET "LS_A". The turquoise curve shows the current through the inductor. This measurement also shows the absolute maximum conditions (limited by the transient overshoot of ~ 150 V on LS_A): Vin = 500 V, maximum commutation current I_L = ~ 100 A**

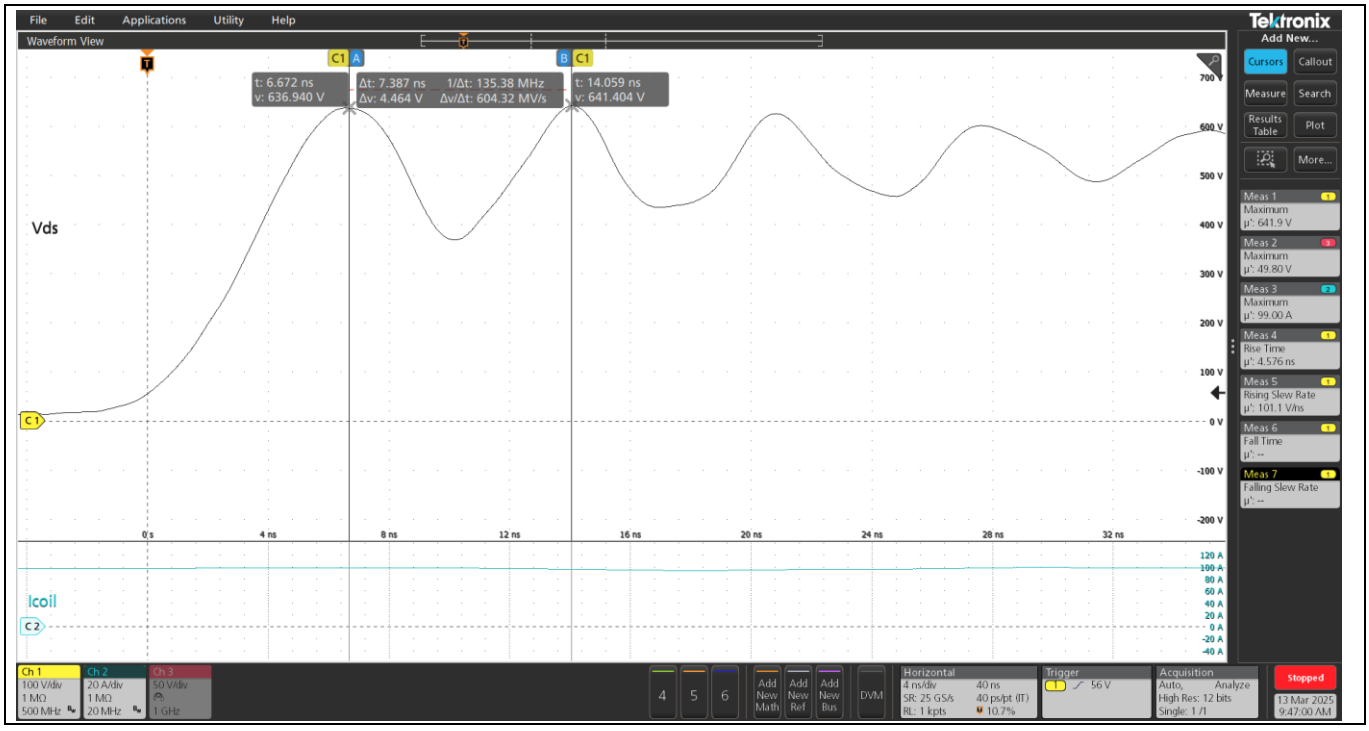

Figure 13 **Zoomed in: Overshoot of the maximal V_{ds} voltage during turn-off of MOSFET "LS_A" (V_{in} = 500 V). The turquoise curve shows the current in the inductor (I_L = ~ 100 A)**

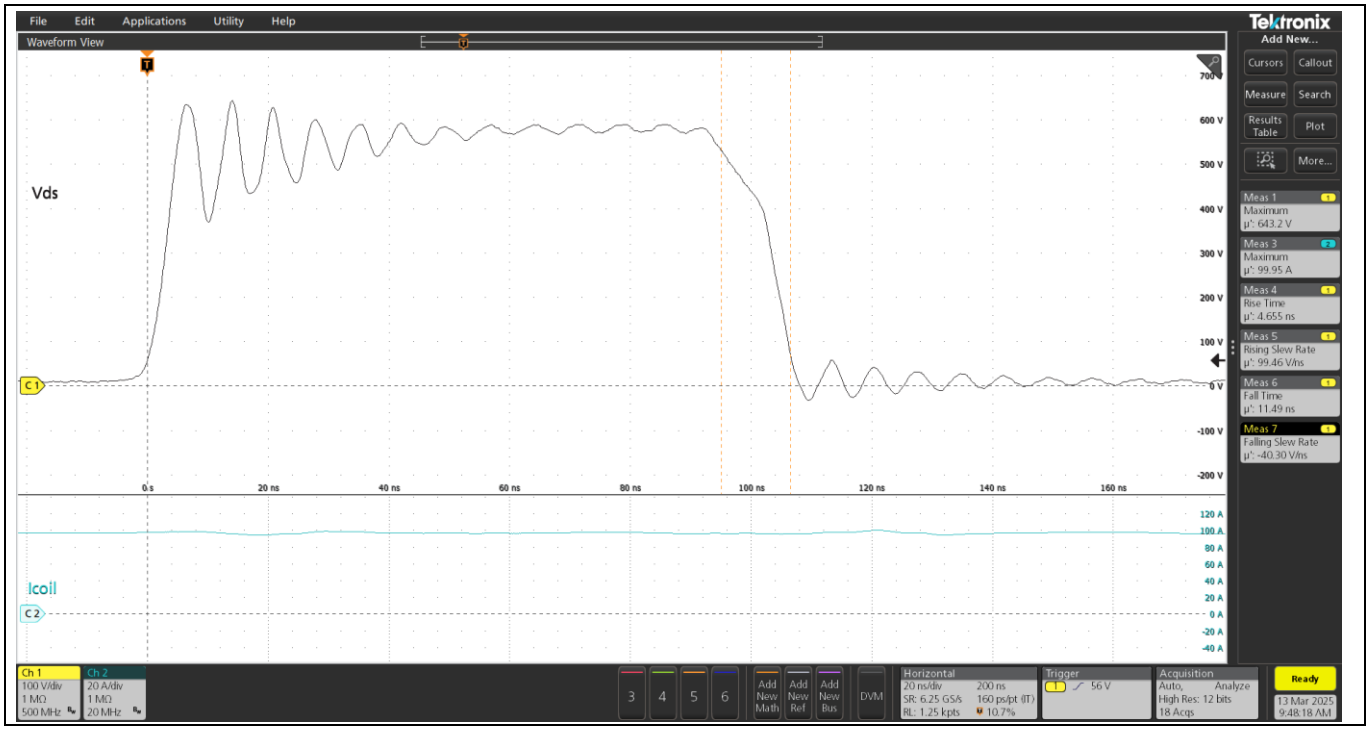

Figure 14 **V_{ds} waveform showing the turn-off and a subsequent turn-on of MOSFET "LS_A" (black curve) according to the setup above (at V_{in} = 500 V). The inductor current (I_L) is ~ 100 A**

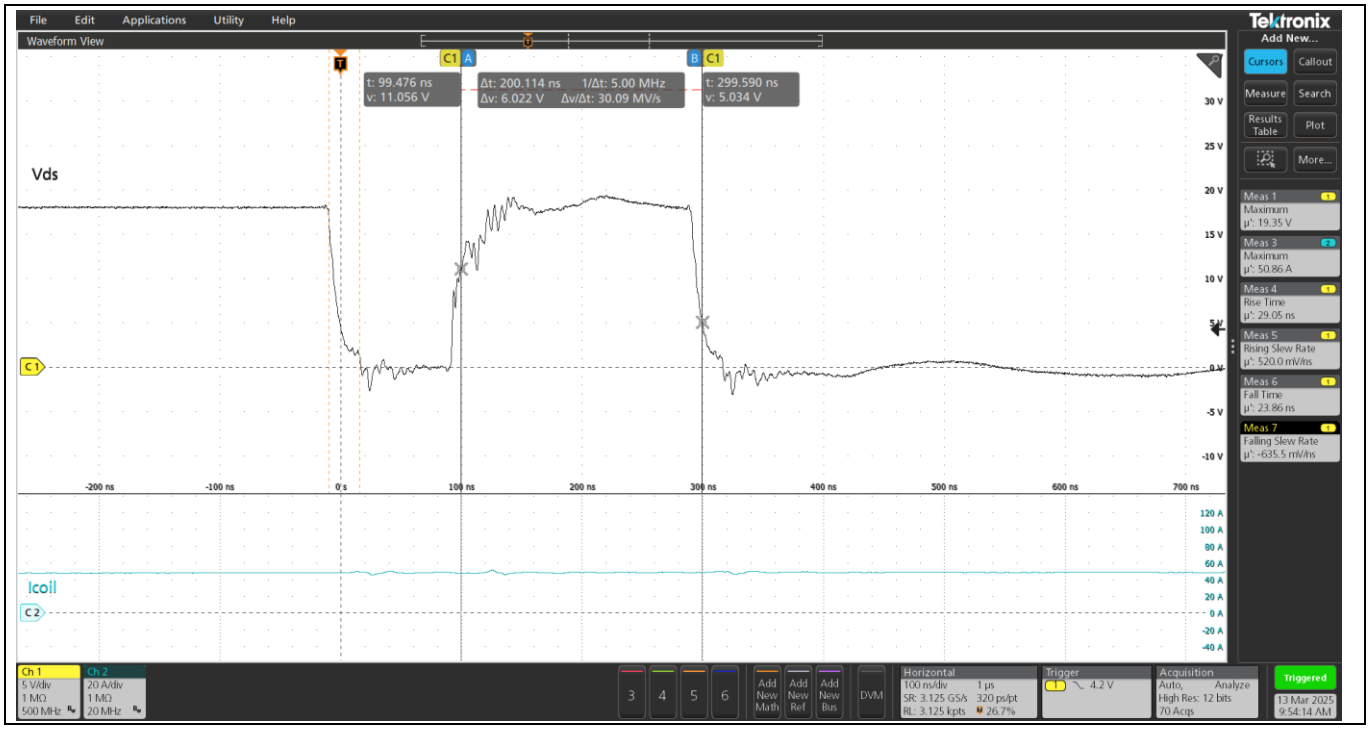

Figure 15 **Zoomed in: Gate-to-Kelvin source voltage (V_{gsk}) on MOSFET "LS_A" (at Vin = 500 V, maximum commutation current I_L = ~ 100 A)**

2.3 Example: Special operation modes

2.3.1 Diode testing

This section shows how to acquire waveforms on the “passive” MOSFET. The idea is to drive the high-side MOSFET actively with a PWM signal and measure the V_{ds} waveform on the opposite, low-side MOSFET. The low-side MOSFET does not get any PWM signal and therefore, the low-side MOSFET will act like a diode.

Figure 16 shows this concept in detail; Figure 17 shows the setup and cabling for evaluation of the MOSFET “LS_A” acting as a diode in Leg A.

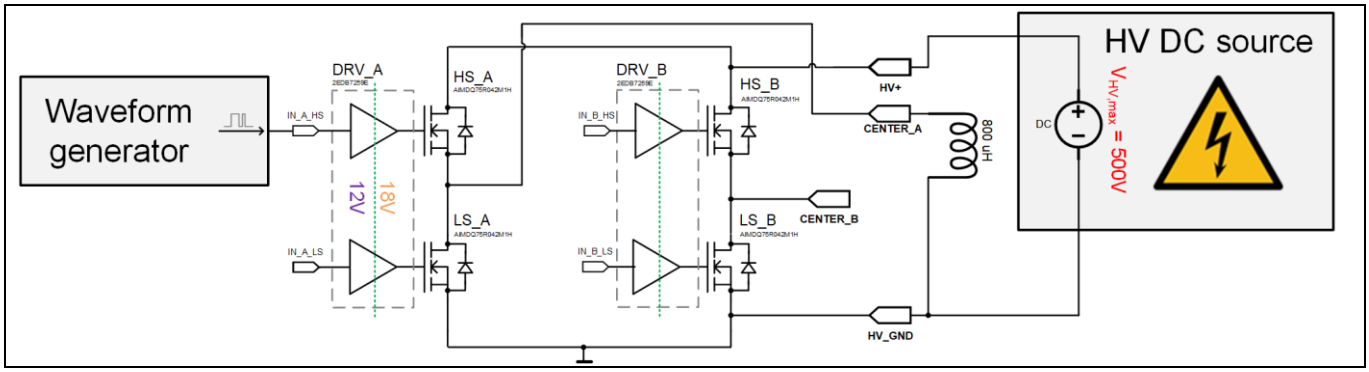

Figure 16 Schematic showing the concept of measuring MOSFET “LS_A” acting as a diode (in HB “A”)

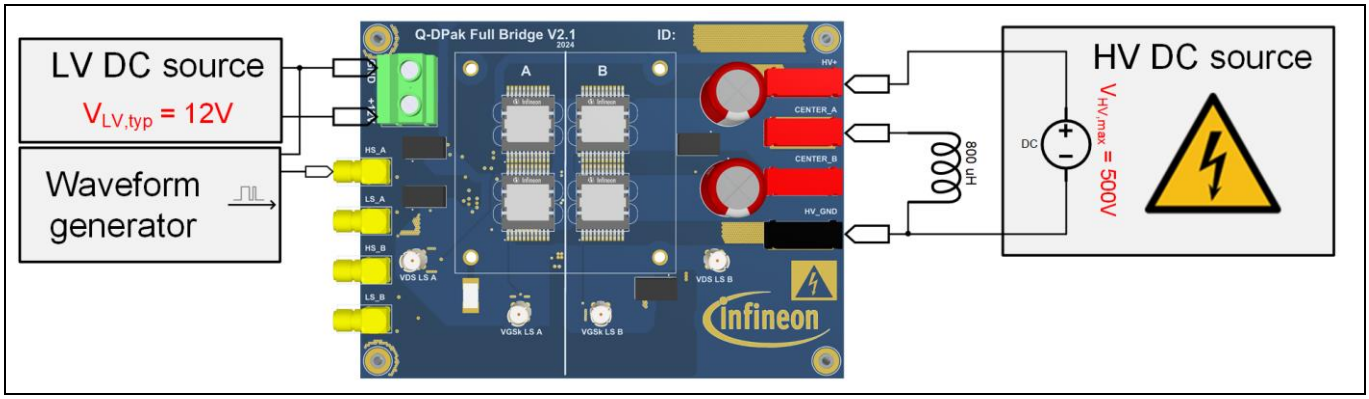

Figure 17 Setup and cabling for evaluation of the MOSFET “LS_A” acting as a diode in Leg A

2.3.2 Fully synchronous operation

This eval board can also be used as a building block for more complex testing. It is possible to provide independent PWM signals to each MOSFET to drive the board as a synchronous full-bridge.

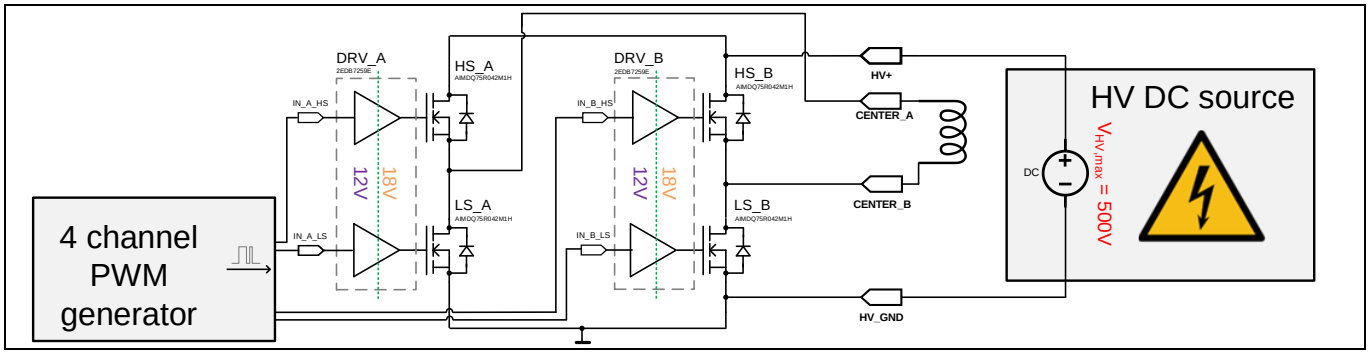

Figure 18 Schematic of eval board working in fully synchronous operation of the full-bridge (e.g., DC-AC inverter)

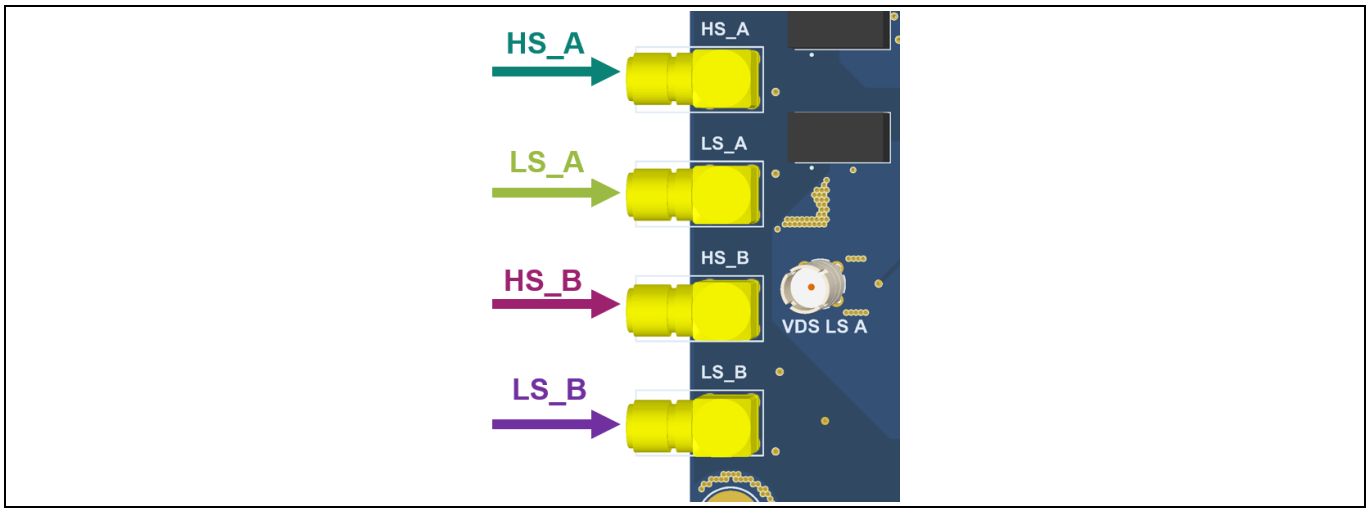

Figure 19 PWM input signals on SMA terminals for fully synchronous full-bridge operation

Similarly, an AC-DC converter can be realized by following the concept shown in Figure 20.

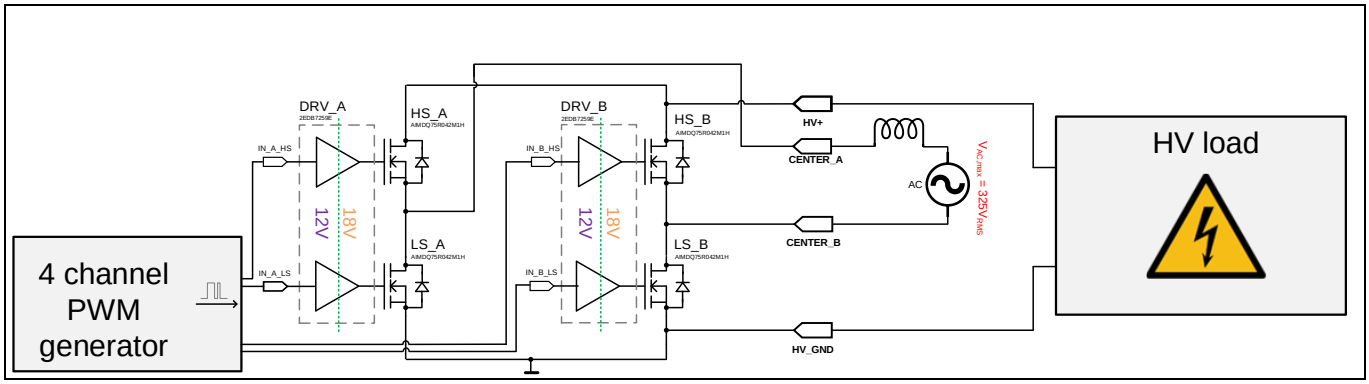

Figure 20 Concept of using this eval board as AC-DC rectifier (totem-pole PFC)

Note: Sensing, control, and protection features are not part of this eval board and must be realized externally.

3 System design

The complete system design resources, such as the bill of materials, the complete schematics, and all PCB design resources and the complete Altium project are available via www.infineon.com.

3.1 Connector details

Table 3 Connectors

Terminal	Label in schematic	Voltage domain	Function
X0	GND +12V	LV	LV supply for DC-DC converter primary side and gate drivers primary side *Note: Ensure the correct polarity.*
X1_U_HB_A	HS_A	LV	PWM input for MOSFET “HS_A”
X2_U_HB_A	LS_A	LV	PWM input for MOSFET “LS_A”
X1_U_HB_B	HS_B	LV	PWM input for MOSFET “HS_B”
X2_U_HB_B	LS_B	LV	PWM input for MOSFET “LS_B”
X_VDS_U_HB_A	VDS LS A		Oscilloscope probing port to probe the drain-to-source voltage of MOSFET “LS_A” (against the power-source: HV_GND)
X_VGS_U_HB_A	VGSk LS A	LS	Oscilloscope probing port to probe the Gate-to-Kelvin source voltage of MOSFET “LS_A”
X_VDS_U_HB_B	VDS LS B		Oscilloscope probing port to probe the drain-to-source voltage of MOSFET “LS_B” (against the power-source: HV_GND)
X_VGS_U_HB_B	VGSk LS B	LS	Oscilloscope probing port to probe the Gate-to-Kelvin source voltage of MOSFET “LS_B”
X_HV+	HV+		HV+ port for high-voltage DC voltage
X_CTR_U_HB_A	CENTER_A		Center-point connection of half-bridge “A”
X_CTR_U_HB_B	CENTER_B		Center-point connection of half-bridge “B”
X_HV_GND	HV_GND		Reference for HV+ voltage

Appendices

A Appendix 1

Figure 21 **Settings for LV power supply providing 12 V (in operation, a current of approximately 300 mA is drawn)**

Figure 22 **Settings for PWM generator (adapt the timing to the inductor you are using)**

References

[1] Infineon Technologies AG: *Q-DPAK package details*; Available online

[2] Infineon Technologies AG: *Infineon Developer Community*; Available online

[3] Infineon Technologies AG: *MyCases Support System*; Available online

[4] Advanced Thermal Solutions, Inc.: *ATS-61600W-C2-R0*; Datasheet; Available online

[5] Infineon Technologies AG: *Innovative top-side cooled package solution for high-voltage applications*; Available online

Revision history

Document revision	Date	Description of changes
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