User guide for IRDC38263 evaluation board

For Intel PVNN rail

About this document

Scope and purpose

The IR38263 **IPOL** is an easy-to-use, fully integrated and highly efficient DC/DC regulator with Intel SVID and I2C/SMBus interface. The onboard PWM controller and low duty cycle optimized MOSFETs make IR38263 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications such as PVNN.

IR38263 is a versatile regulator which offers programmability of switching frequency, output voltage, and fault/warning thresholds and fault responses while operating over a wide input and output voltage range. Thus, it offers flexibility as well as system level security in event of fault conditions.

The switching frequency is programmable from 166 kHz to 1.5 MHz for an optimum solution. The on-chip sensors and ADC along with the PVID and PMBus interfaces make it easy to monitor and report input voltage, output voltage, output current and temperature.

This user guide contains the schematic and bill of materials for the IRDC38263 evaluation board, designed for Intel PVNN rail. The guide describes the use of the evaluation board itself. Detailed application information for IR38263 is available in the IR38263 data sheet.

Intended audience

This user guide is intended as a reference for for designer's evaluating the IRDC38263 board, Intel PVNN rail.

Table of Contents

1 Board features

- V_{in} = +12 V
- V_{out} = +1.0 V
- Idc = 18 A, Ipk = 20.5 A
- F_s = 978 kHz
- L = 100 nH (12.4 mm X 8.3 mm X 8.0 mm, DCR=0.15 mΩ)
- C_{in} = 4x22 µF (16 V, ceramic 0805) + 1X270 µF (16 V, electrolytic, *Note*1)
- C_{out} = 2x470 µF (SP-Cap/2.5 V/3 mΩ) + 3x47 µF(X5R/6.3 V/0805)
  + 4x22 µF (X6S/6.3 V/0805) + 15x10 µF (X6S/6.3 V/0603)

Note 1: The electrolytic input capacitor is used to damp the parasitic inductance of input supply cables. It can be eliminated if the input is from nearby power planes.

2 Connections and operating instructions

IR38263 VCCIO demo board requires a single +12 V for the input power and +5 V for Vcc bias voltage. It can deliver up to 20.5A load current. Table 1 lists the connectors, jumpers and test points on the board.

Table 1 Connections

Label		Descriptions
Power Connectors	12V_Source	Connect input power (+12 V) to this connector
	GND	Return of input power
Power Connectors	VOUT	Vout (+1.0 V), connect a load (not to exceed 30 A) to this connect
	GND	Return of Vout
Vcc inputs	Vcc, GND	Apply an external 5 V supply for the bias voltage
SW1	1, 2	Enabled: 1=On, Disabled: 1=Off
J1	Mini Slammer	An Intel mini slammer could be connected to this connector
J2	ALERT	SM Bus Line
	GND	
	DATA	
	CLK	
J3	VCCIO_SKT	Test points to sense VCCIO output
J4	SVID_CLK	Can be used to apply a logic signal to VIDSEL0; if used, populate R44 with 4.99 K and depopulate R25
J5	SVID_DIO	Can be used to apply a logic signal to VIDSEL1; if used, populate R45 with 4.99 K and depopulate R24
J6	SVID_ALERT	Can be used to apply a logic signal to VIDSEL2; if used, populate R46 with 4.99 K and depopulate R27
Test Points	1.8 V, GND	Test points for the internal 1.8 V supply for the digital circuitry
	Pgood	Test point for Power Good
	VSENSE	Test point for Vsns pin
	ADDR	Test point for Address pin
	Enable	Test point for Enable pin
Jumpers	SV_CLK	Open to pull up VIDSELx lines high, short to pull them low
	SV_DIO	
	SV_ALERT	
SW4	1, 2	Keep 1(Vcc switch) = ON, 2 =OFF
Test Points	VPVID, GND	Not Used
Power Connectors	12 V_Source	Connect input power (+12 V) to this connector

The SV_CLK, SV_DIO and SV_ALERT jumpers should be left open to pull the VIDSELx lines high.

They should be shorted to pull the VIDSELx lines low.

Table 2 PVID to output voltage mapping

VIDSEL2	VIDSEL1	VIDSEL0	Vout (V)
0	0	0	0.85
0	0	1	0.90
0	1	0	0.95
0	1	1	1
1	0	0	0.85
1	0	1	0.90
1	1	0	0.95
1	1	1	1

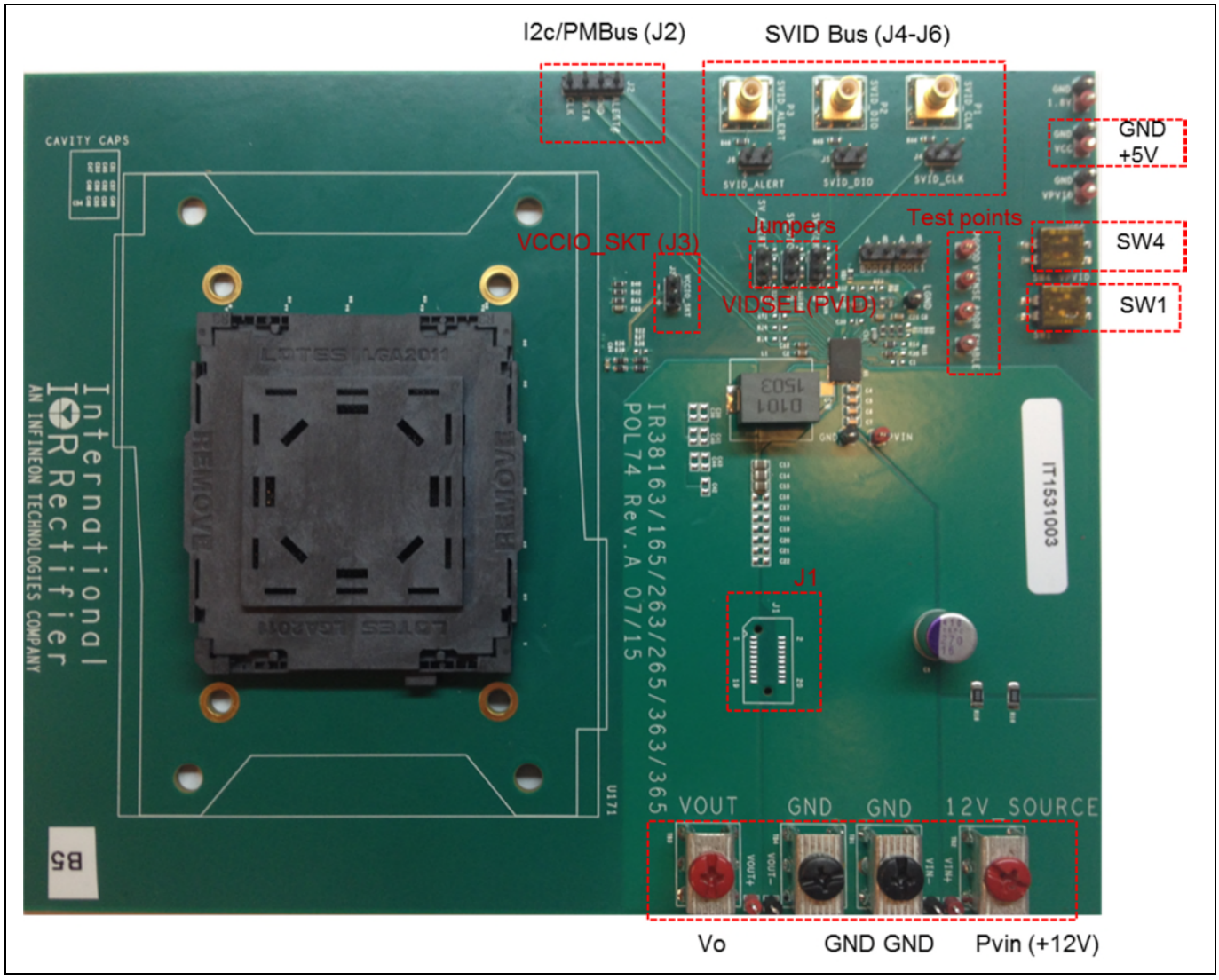

Figure 1 Top view of IR38263 PVNN evaluation board with R socket

The PCB of IR38263 demo board is a 5.5”x 7” 10-layer board using FR4 material. All layers use 2 Oz. copper. The PCB thickness is 0.062”.

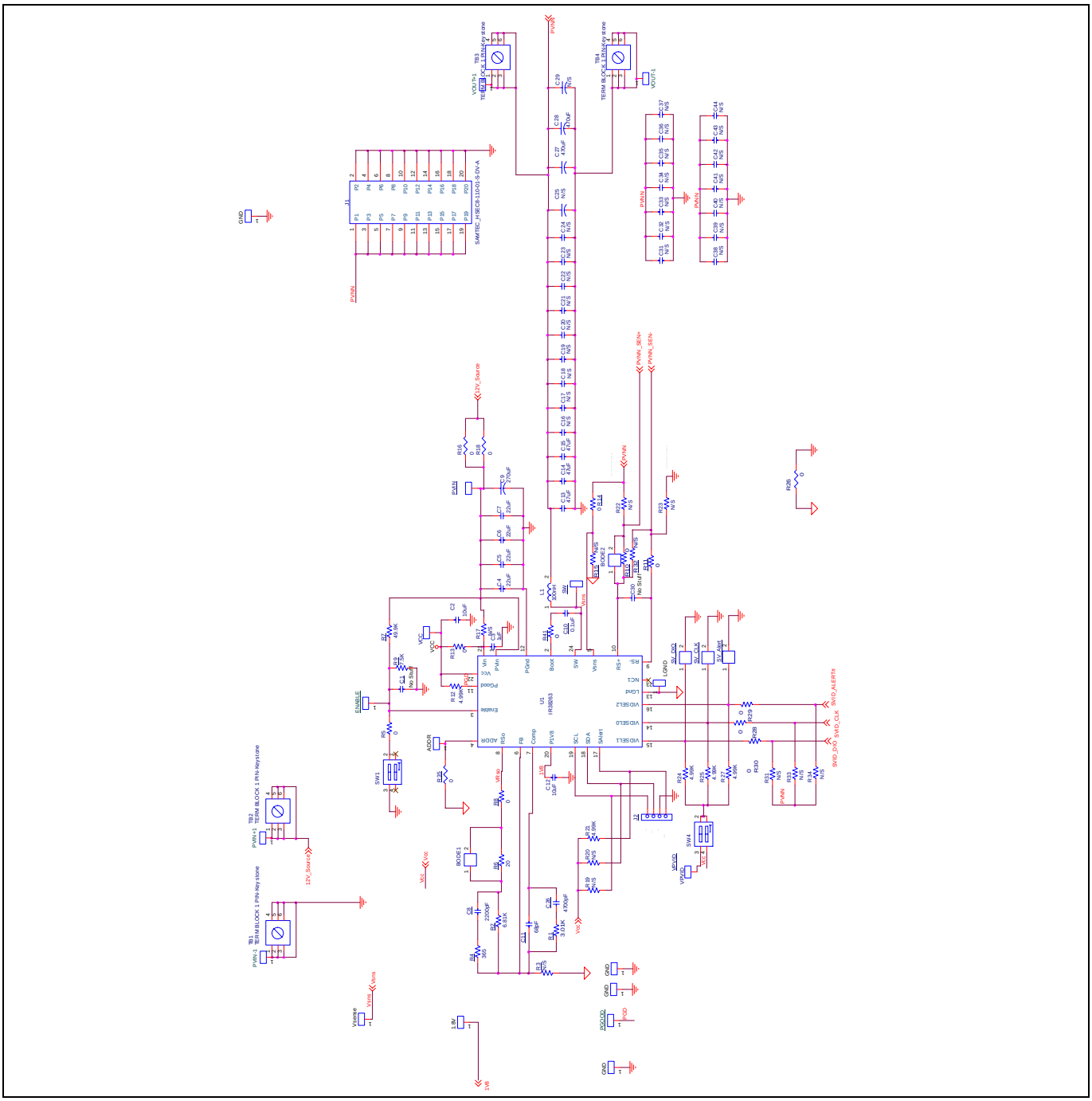

Figure 2 Schematic of the IRDC38263 PVNN evaluation board

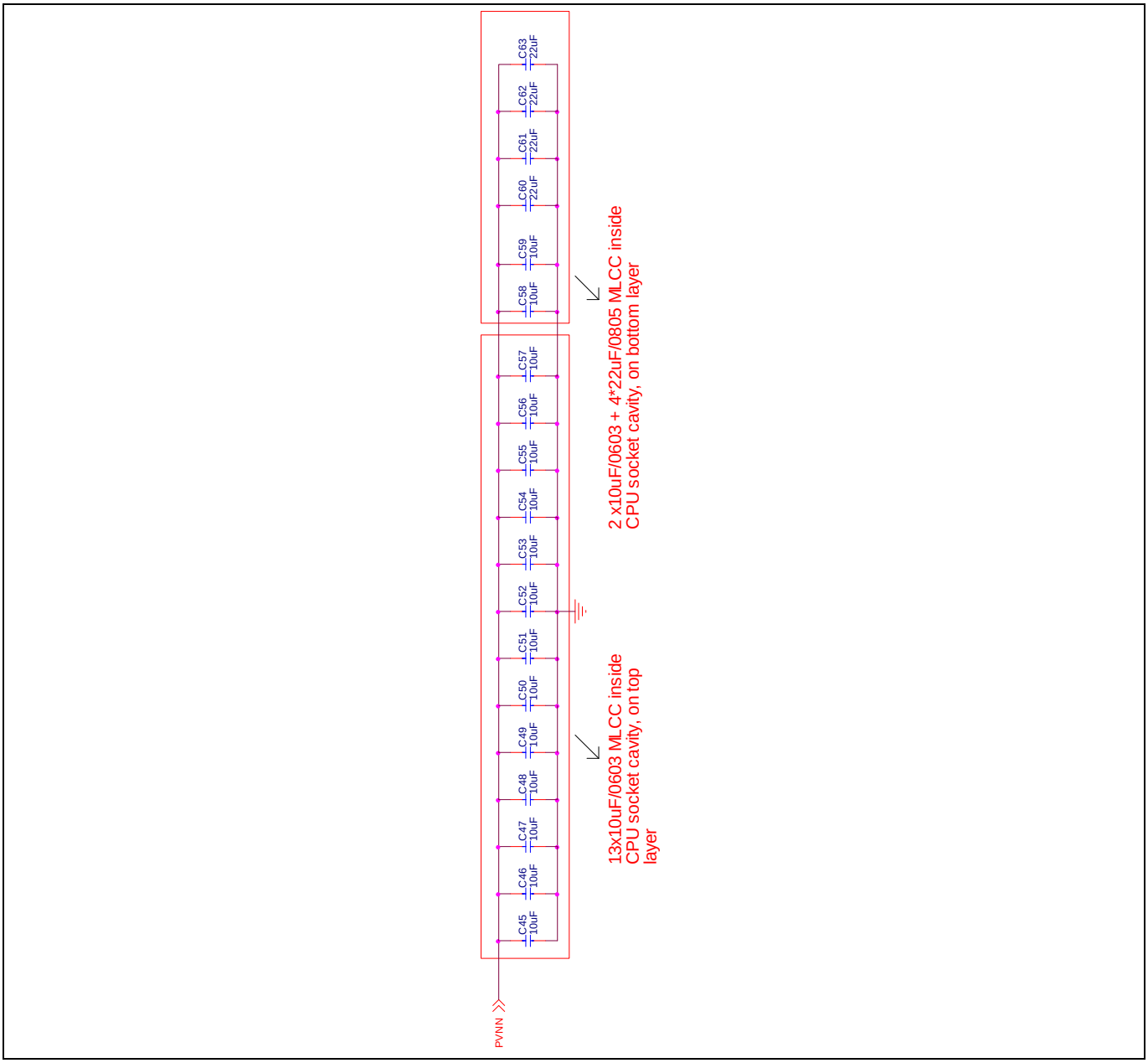

Figure 3 Schematic of the IRDC38263 PVNN evaluation board

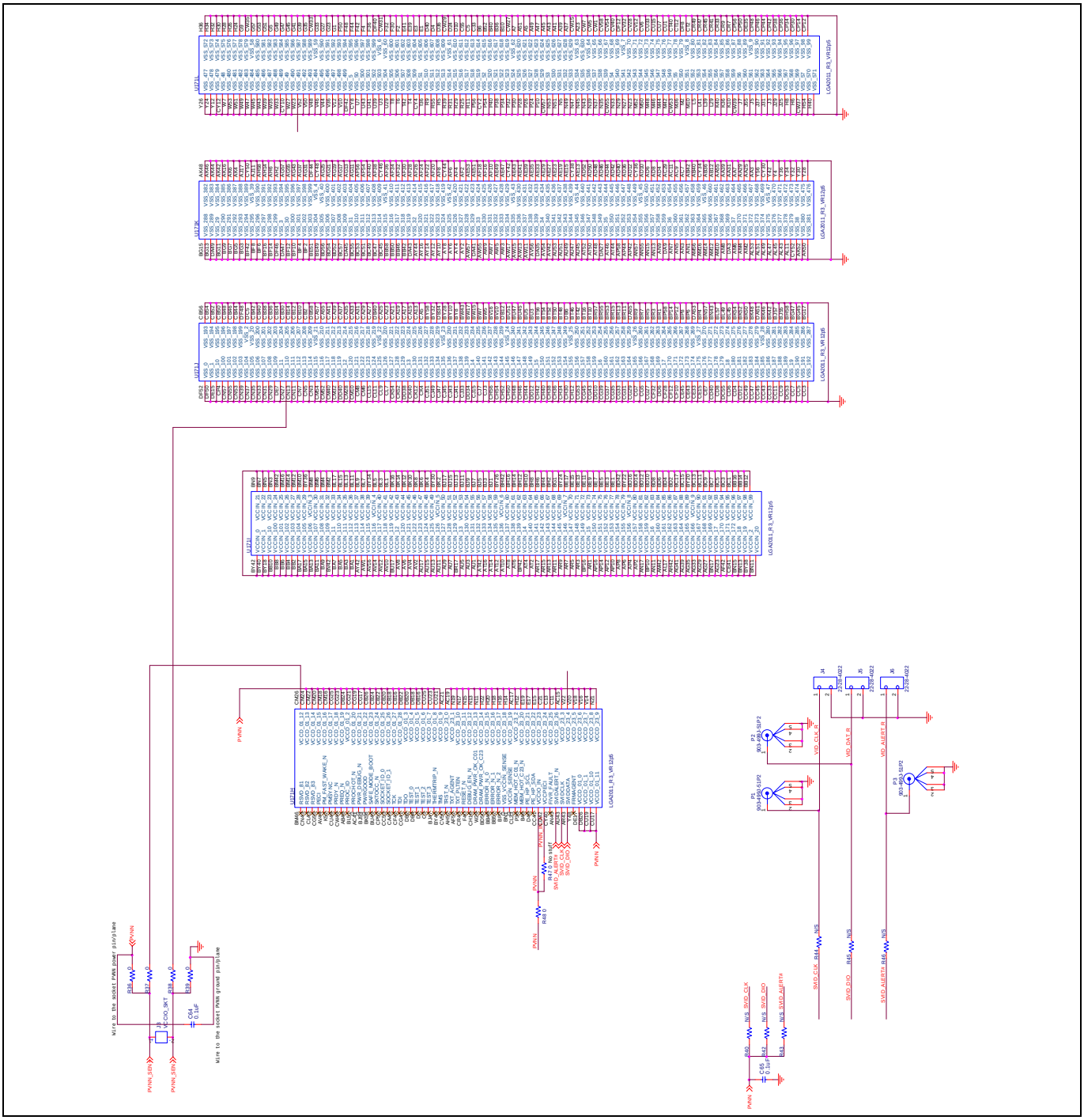

Figure 4 Schematic of the IRDC38263 PVNN evaluation board

3 Bill of materials

Table 3 Bill of materials

Item Number	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	10	1.8 ADDR ENABLE PGOOD PVIN+1 PVIN VOUT+1 VSENSE VPVID VCC	0.075" SQ_SMT_TestPoint (red)		Keystone Electronics	5000
2	7	GND1 GND2 GND3 GND4 LGND VOUT -1 PVIN-1	0.075" SQ_SMT_TestPoint (black)		Keystone Electronics	5006
3	8	BODE1 BODE2 SV_ALERT SV_CLK SV_DIO J4 J5 J6	2 pin header			M20-9990246
4	3	C10 C64 C65	0.1 µF	CAP CER 0.1µF 25 V 10% X7R 0603	Murata	GRM188R71E104KA01D
5	17	C2, C12, C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59	10 µF	CAP CER 10 µF 6.3 V 20% X6S 0603	TDK	C1608X6S0J106M080AC
6	1	C3	1 µF	0603, X5R, 25 V, 20%	TDK	C1608X5R1E105M
7	4	C4 C5 C6 C7	22 µF	0805, X5R, 16 V, 20%	TDK	C2012X5R1C226M085AC
8	4	C60 C61 C62 C63	22 µF	0805, 4 V, X6S, 20%	Murata	GRM21BC80G226ME39L
9	1	C8	2200pF	2200 pF, 0603, 50 V, NPO	TDK	C1608C0G1H222J
10	1	C9	270 µF	Electrolytic 16 V	Panasonic	16SEPC270M
11	1	C11	68pF	50 V, 0603, NP0, 5%	Murata	GRM1885C1H680JA01D
12	3	C13 C14 C15	47 µF	0805, 6.3 V, X5R, 20%	TDK	C2012X5R0J476M
13	2	C27, C28	470 µF	SP-Cap, SMD, 2.5 V, 3 m Ohm	Panasonic	EEFGX0E471R
14	1	C26	4700pF	4700 pF, 0603, 50 V, NPO	TDK	C1608C0G1H472J
15	1	J1	SAMTEC_HSEC8-110-01-S-DV-A		SAMTEC	HSEC8-110-01-S-DV-A
16	1	J2	Header	4X1 header	Sullins Connector Solutions	PEC36SAAN
17	1	J3	VCCIO_SKT			M20-9990246
18	1	L1	100nH	DCR=0.15 mohm	Delta	HCB138380D-101
19	3	P1 P2 P3	903-499J-51P2	CONN SMB JACK STR 50 OHM PCB	Amphenol-RF Division	903-499J-51P2
20	1	R1	3.01K	RES SMD 3.01 KOHM 1% 1/10 W 0603	Rohm	MCR03EZPFX3011
21	1	R2	6.81K	RES SMD 6.81 KOHM 1% 1/10 W 0603	Rohm	MCR03EZPFX6801
22	1	R4	365	0603,1/10 W,1%	Rohm	MCR03EZPFX3650
23	21	R5 R8 R10 R11 R14 R13 R26 R35 R37 R38 R41 R44 R45 R46 R28 R29 R30 R47 R48 R36 R39	0	RES SMD 0.0 OHM JUMPER 1/10 W	Panasonic	ERJ-3GEY0R00V
24	2	R16 R18	0	RES SMD 0.0 OHM JUMPER ¼ W 1206	Panasonic	ERJ-8GEY0R00V
25	1	R6	20	0603,1/10 W,1%	Vishay	CRCW060320R0FKEA
26	1	R7	49.9K	0603,1/10 W,1%	Rohm	MCR03EZPFX4992
27	1	R9	7.5K	0603,1/10 W,1%	Rohm	MCR03EZPFX7501
28	5	R12, R21, R24, R25, R27	4.99K	0603,1/10 W,1%	Rohm	MCR03EZPFX4991
29	2	SW1 SW4	SW_DIP_2POS			
30	4	TB1 TB2 TB3 TB4	TERM BLOCK 1 PIN-Keystone			8199
31	1	U1	IR38263	30 A Integrated Buck Regulator with PMBus and SVID	Infineon	IR38263MTRBPF
32	1	U171	Intel Socket-R 3_LGA2011-R3		Intel	Intel

4 Typical operating waveforms

PVin=12.0 V, Vout=1.0 V, Iout=0-20.5 A, Fs=978 kHz, Room Temperature, no airflow

4.1 Waveforms

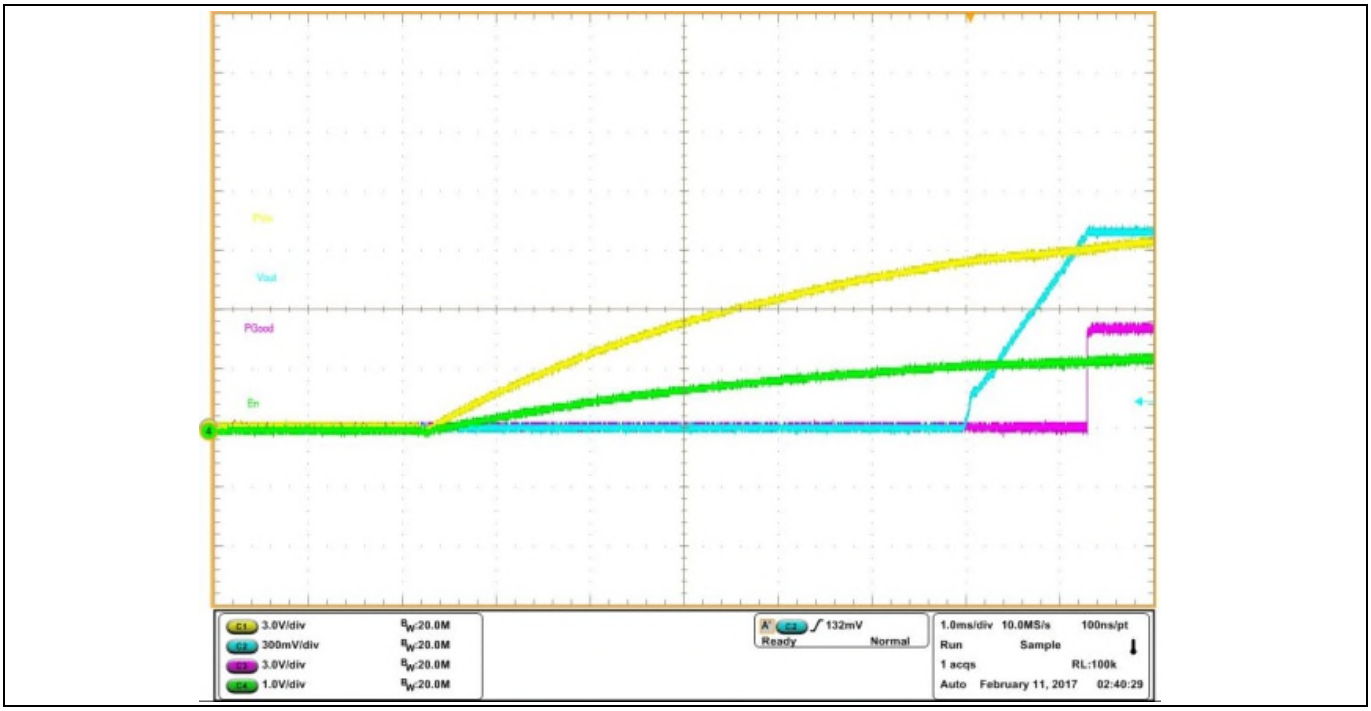

Figure 5 P_{Vin} start-up at 20.5 A load, Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

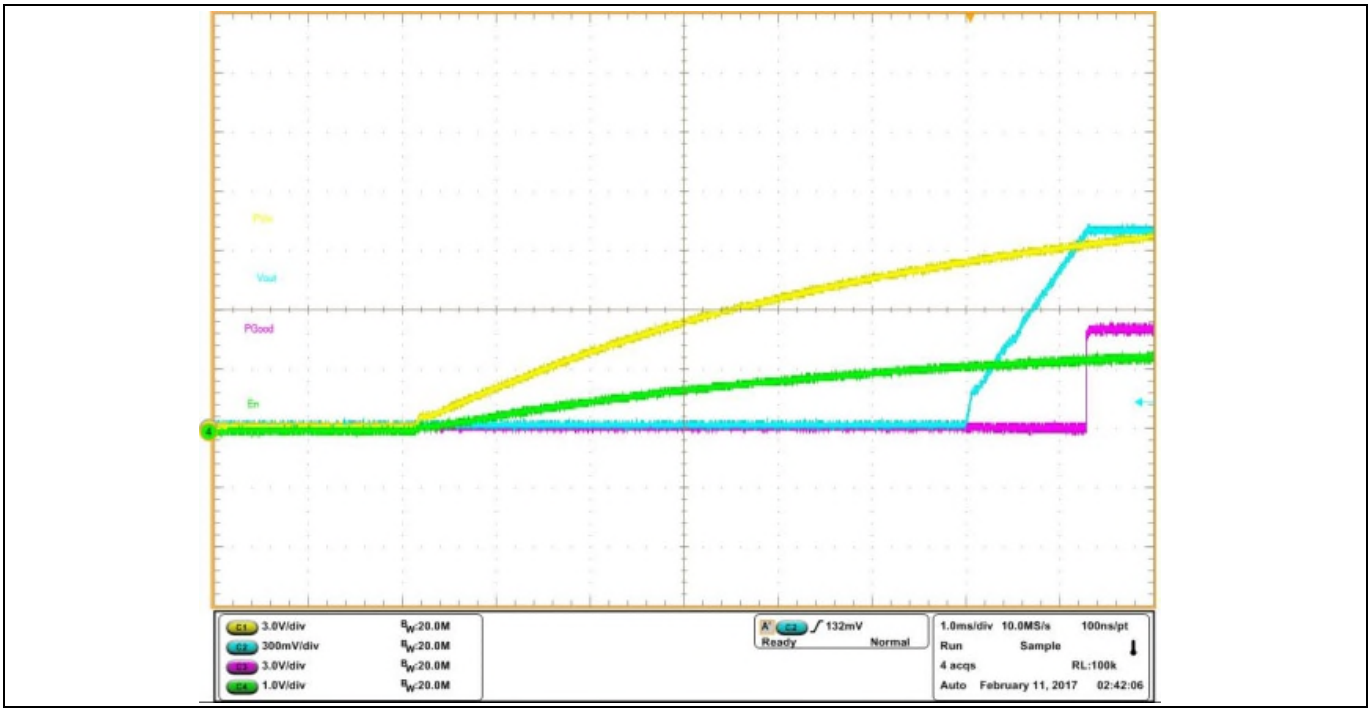

Figure 6 P_{Vin} start-up at 20.5 A load, Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

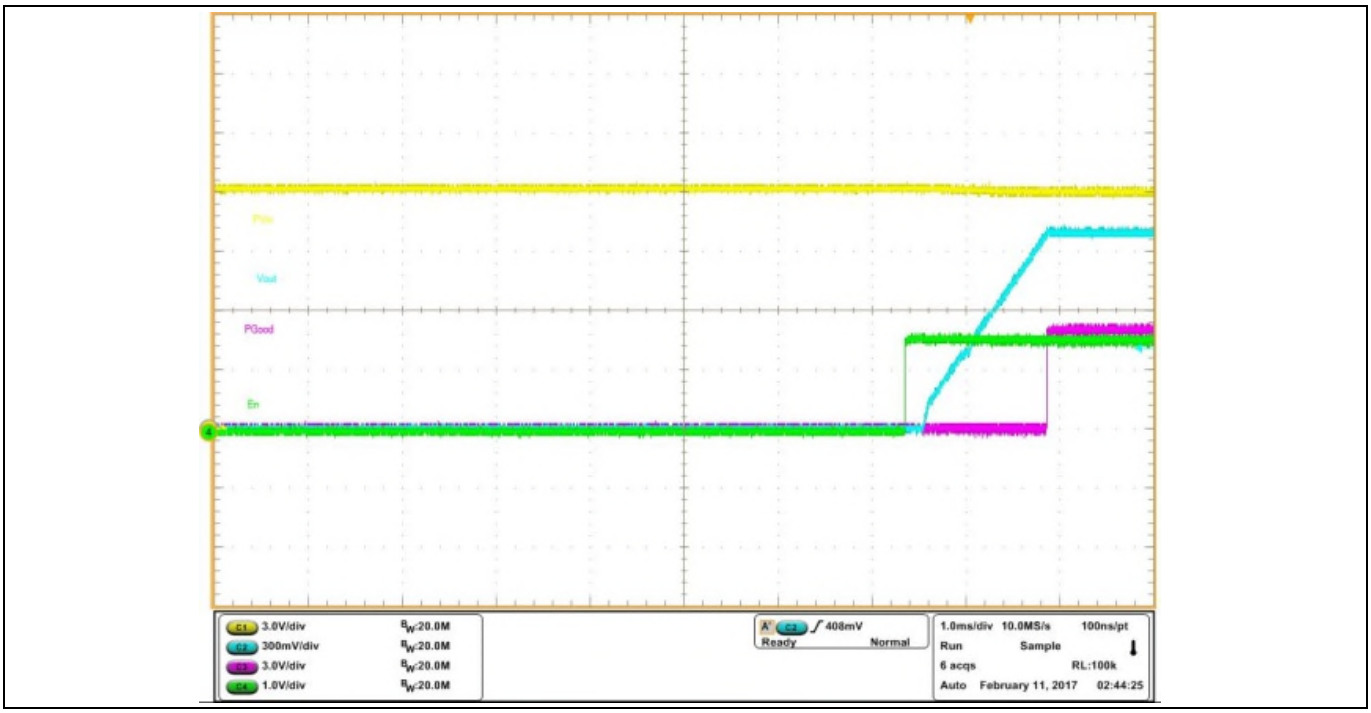

Figure 7 En startup at 20.5 A load, Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

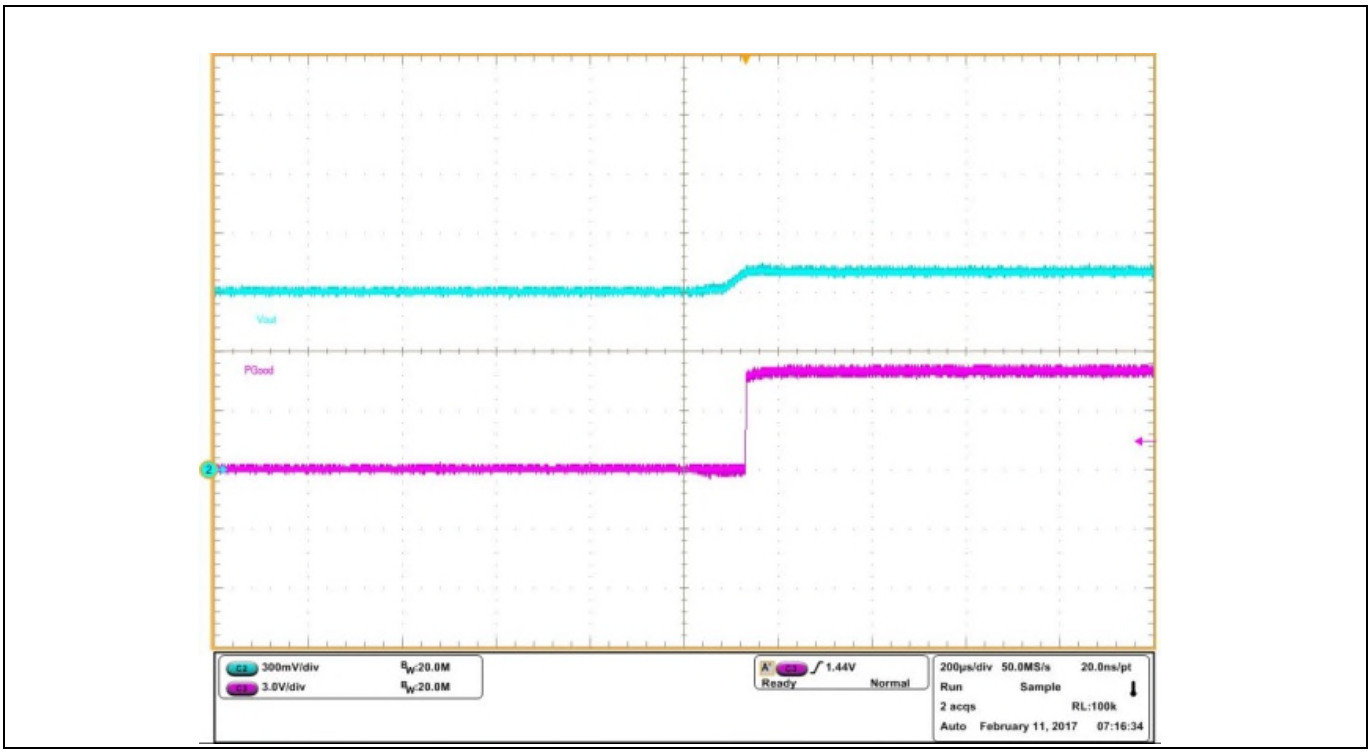

Figure 8 Prebias startup at 0.9 V, Ch_2:V_{out}, Ch_3:P_{Good}

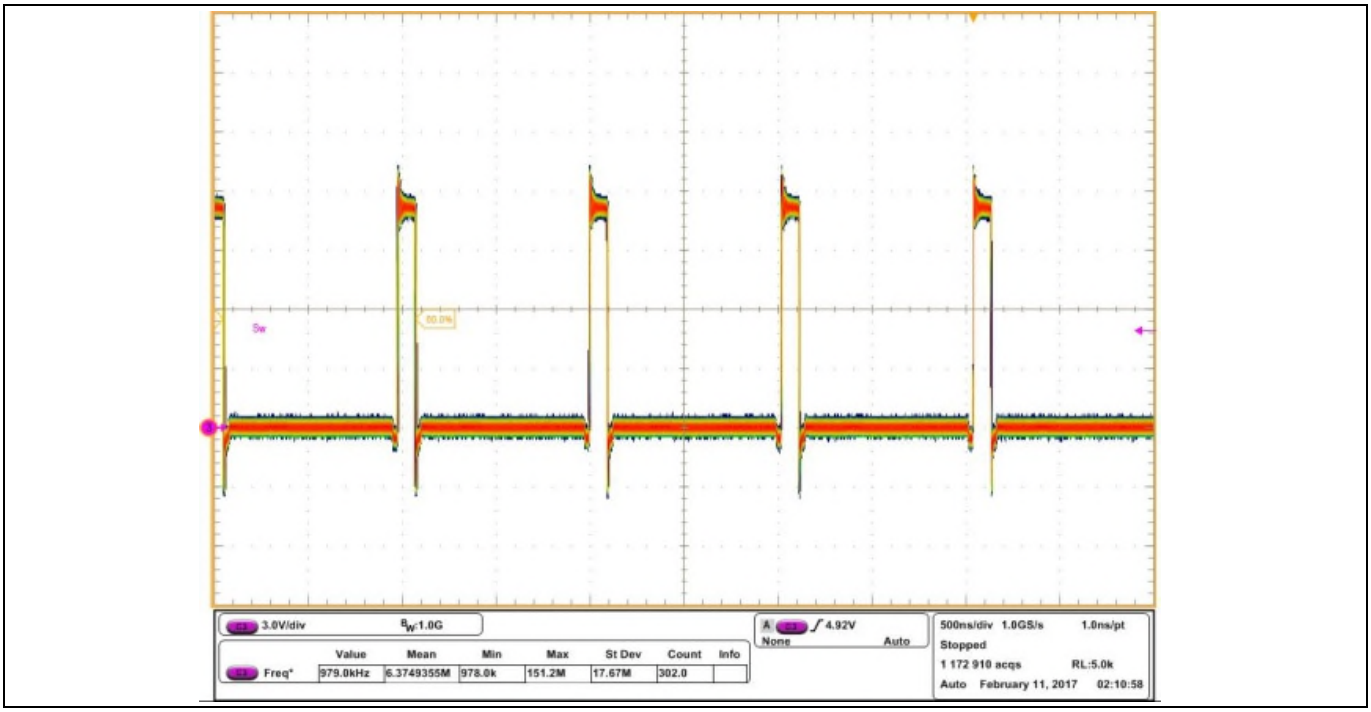

Figure 9 Inductor node at 20.5 A load, Ch_3:SW node

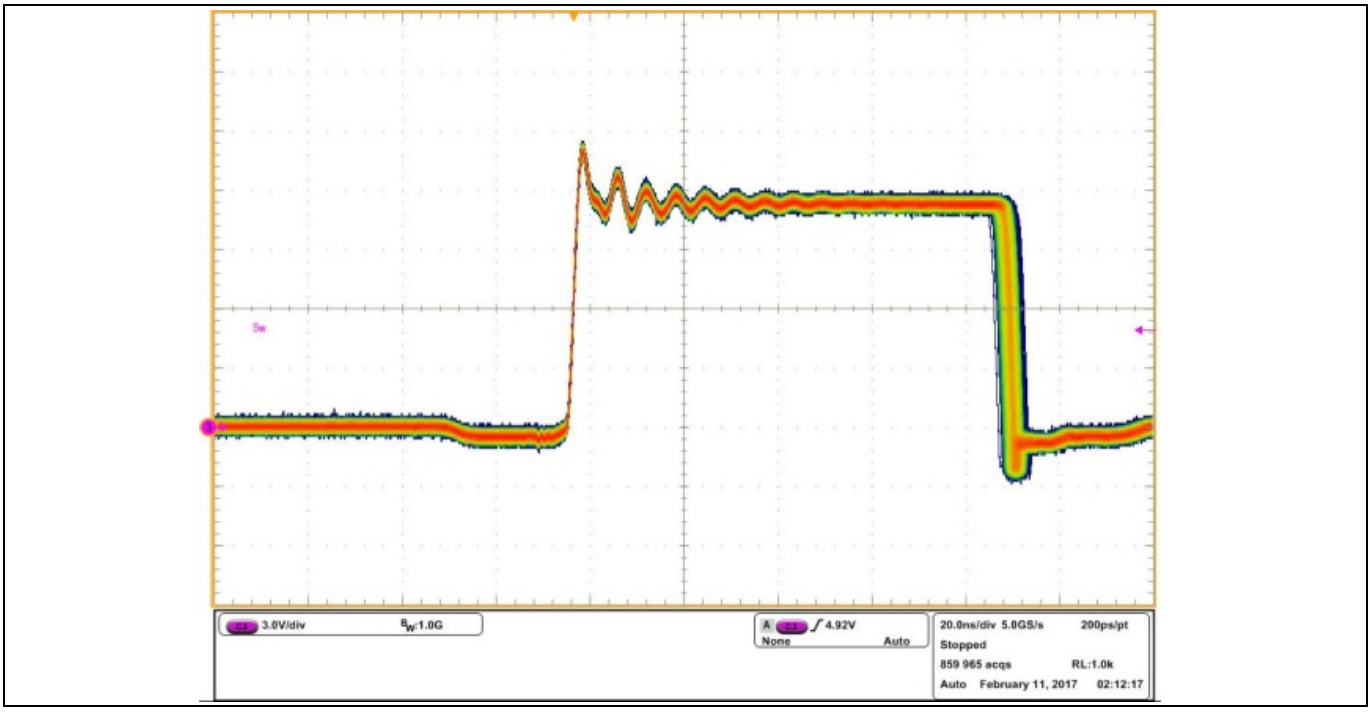

Figure 10 Sw node jitter at 20.5 A load, Ch_2:V_{out}

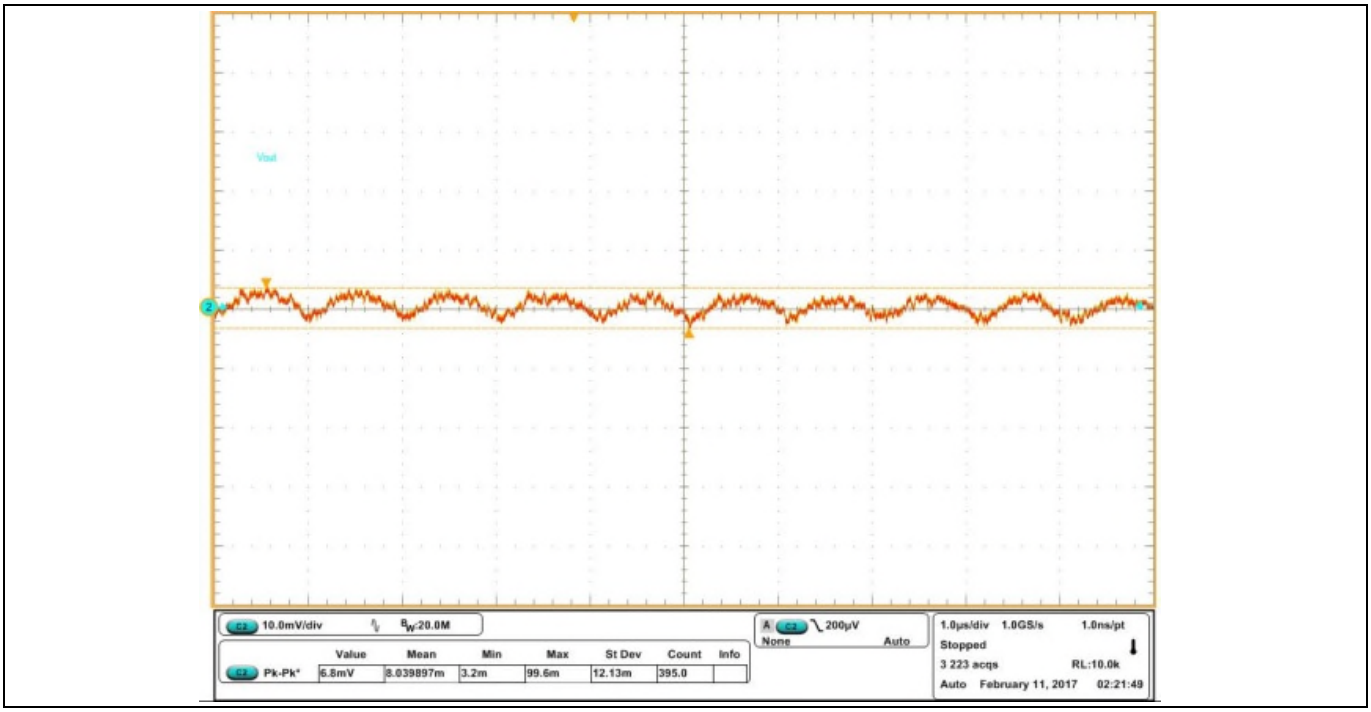

Figure 11 Vo ripple at 20.5 A load, Ch_2:V_{out}

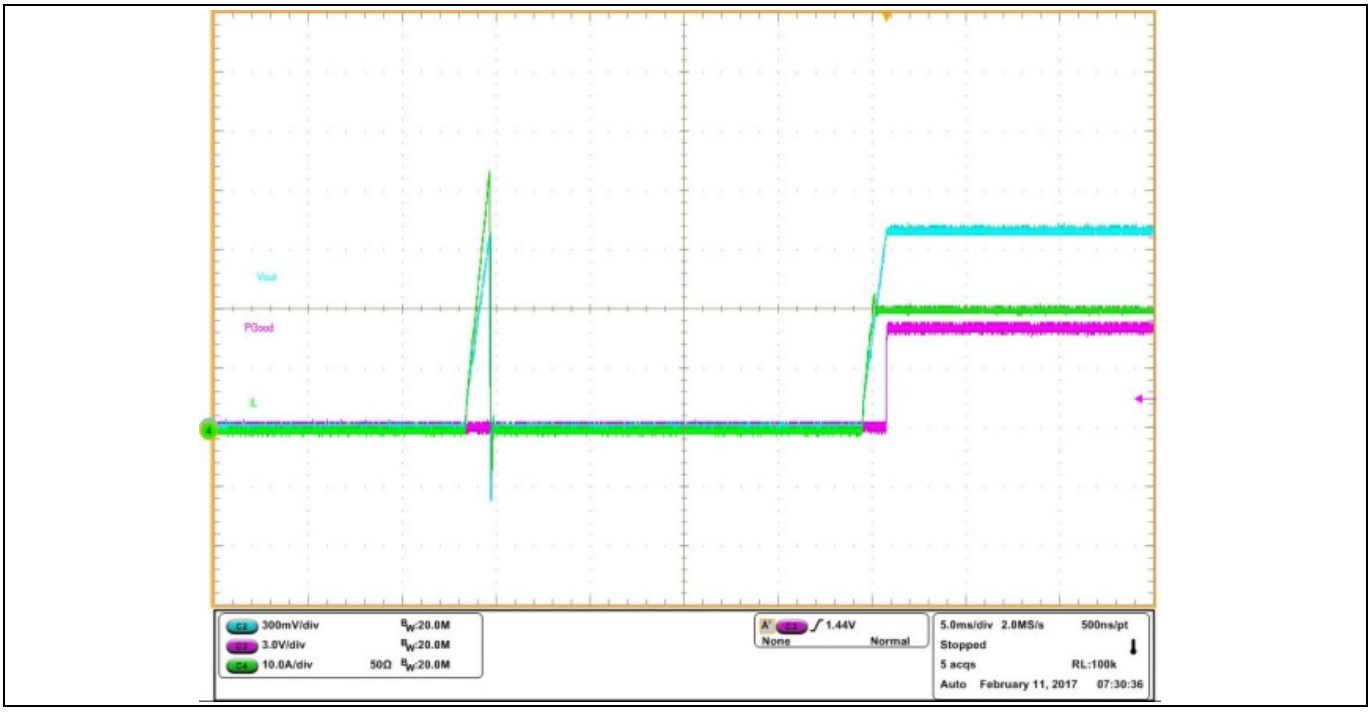

Figure 12 Hiccup recovery at 20.5 A Load, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:I_{out}

4.2 Bode plots

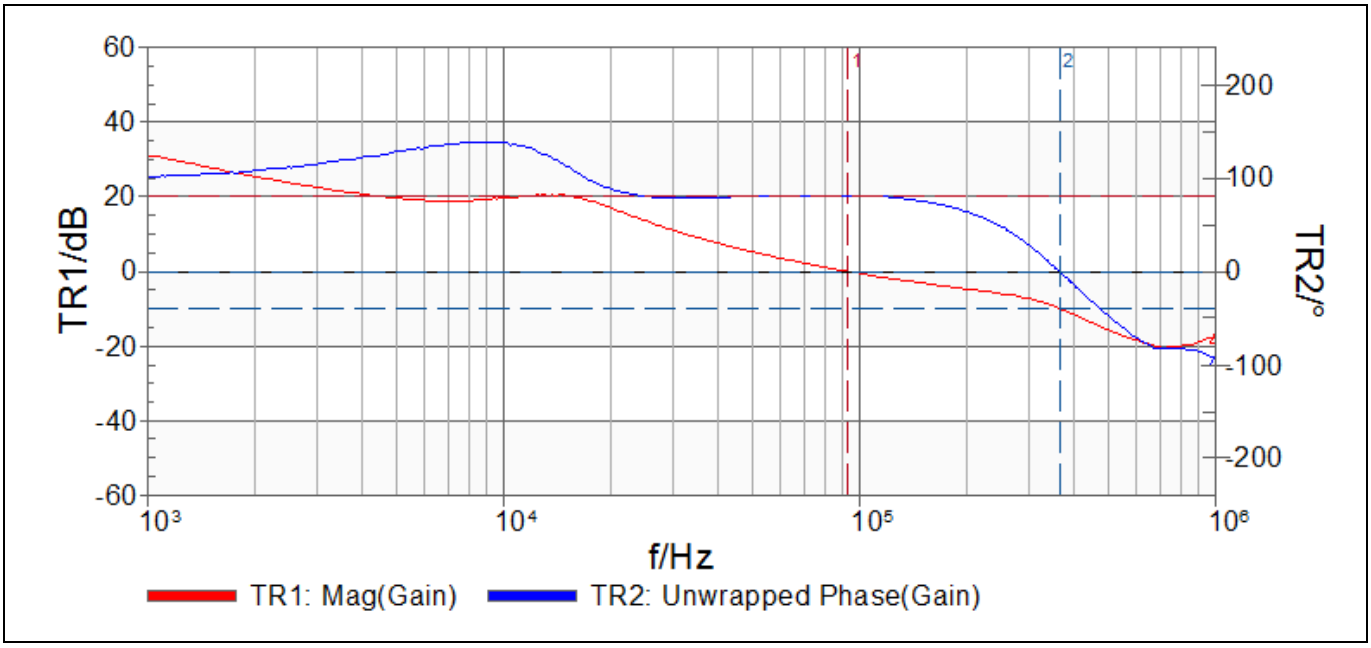

Figure 13 Bode plot at 20.5 A load, bandwidth = 93.1 kHz, phase margin = 82° , gain margin = 9.8 dB

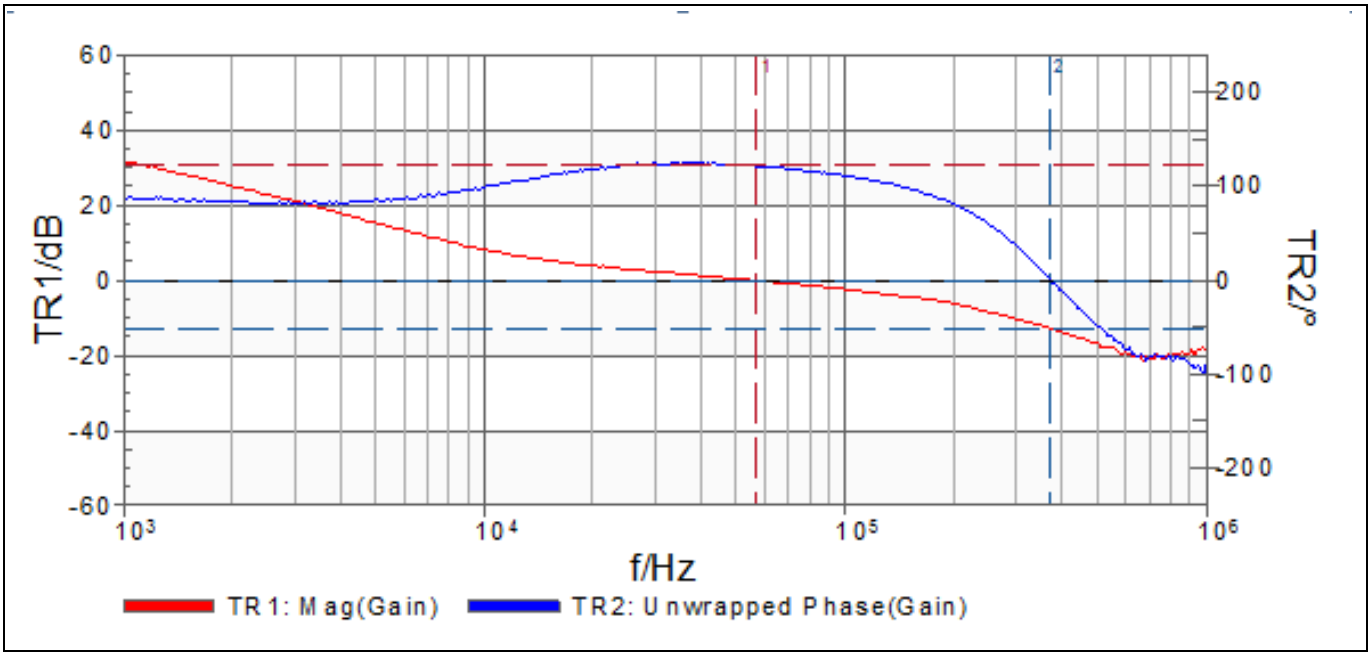

Figure 14 Bode plot at 0 A load, bandwidth = 56.2 kHz, phase margin = 121° , gain margin = 12.9 dB

4.3 Thermal image

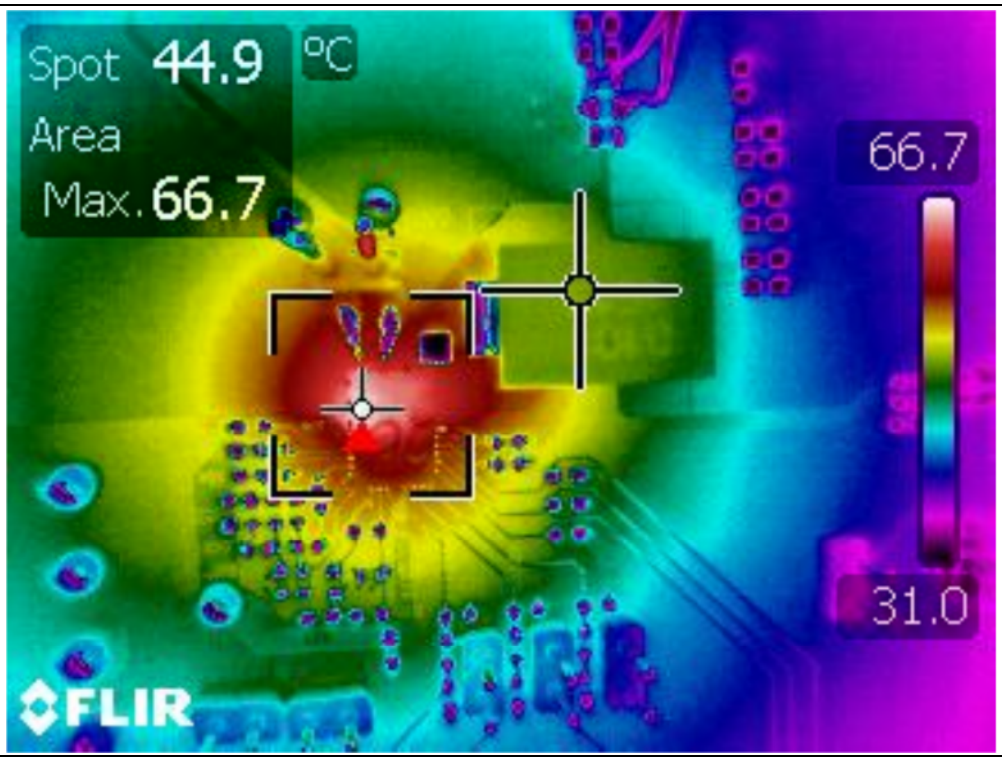

Figure 15 Thermal image of the board at 30 A load, IR38263: 66.7°C, inductor: 44.9°C

4.4 Efficiency and power loss

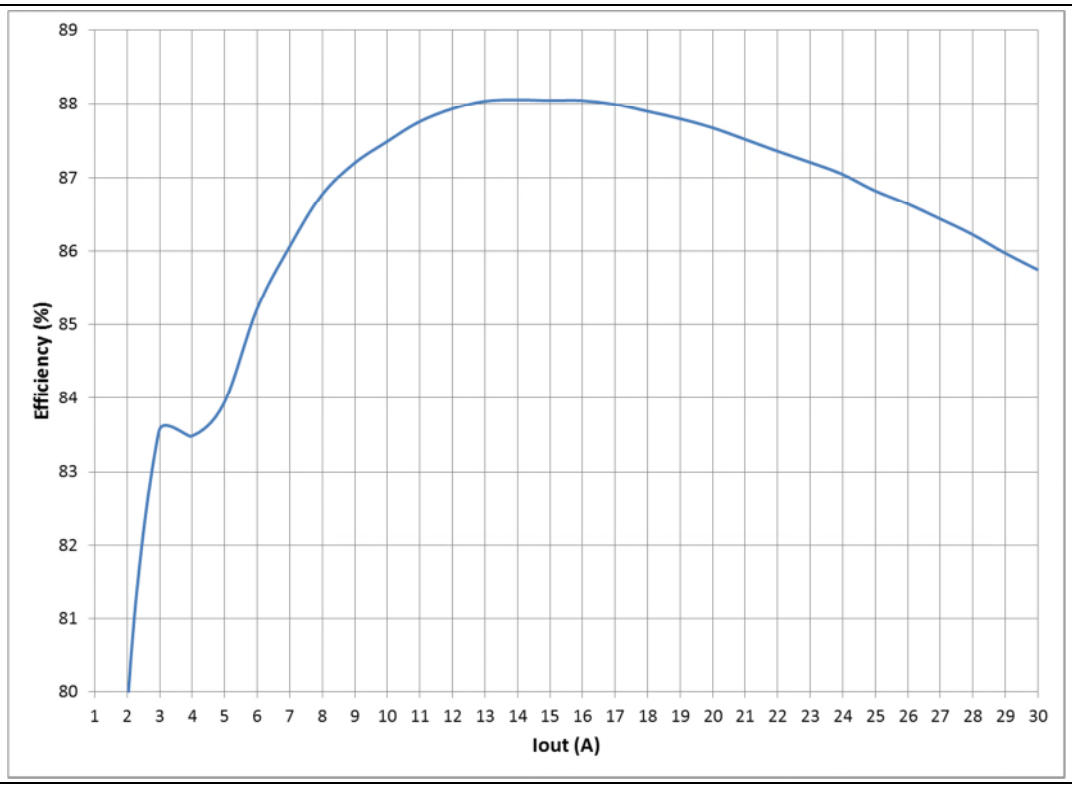

Figure 16 Efficiency vs. load current

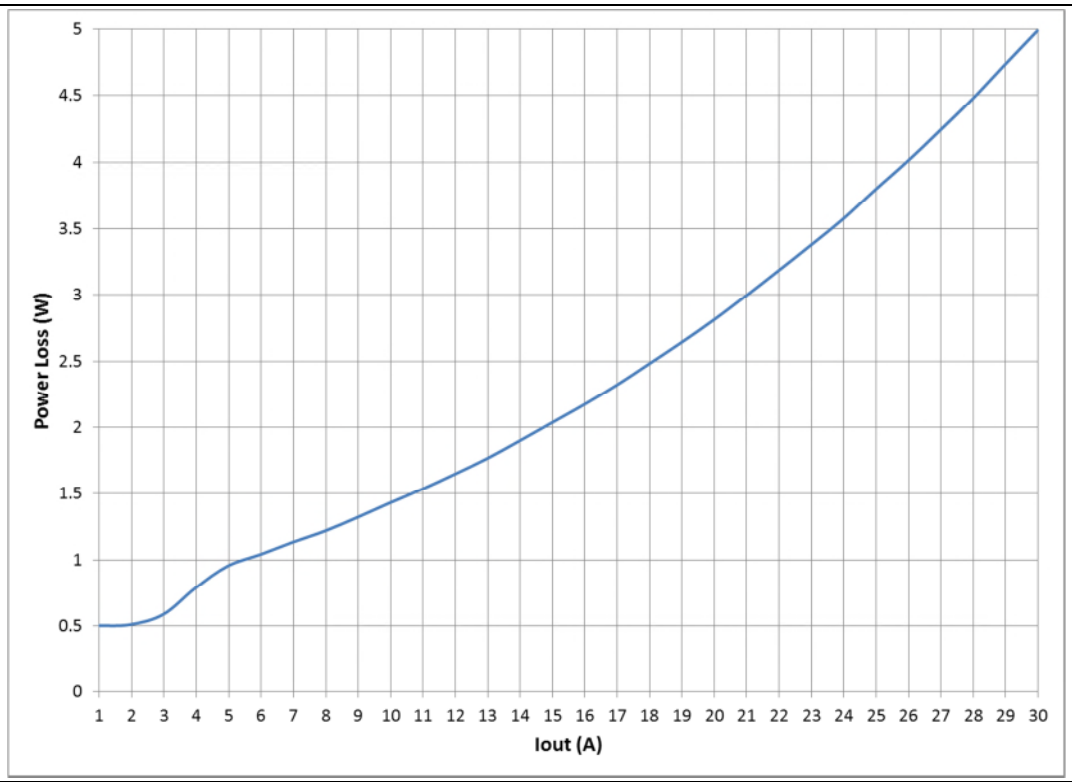

Figure 17 Power loss vs. load current

Revision History

Major changes since the last revision

Page or Reference	Description of change
Figure 1	Added annotations to indentify labels on table 1 on the actual demo board.
Page 5 & 8	Updated C12 capacitor from 2.2uF to 10uF, on schematic and BOM
	Updated general typo's on document.

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