USB PD DRP (dual-role power) schematics using EZ-PD™ PMG1 MCUs

About this document

Scope and purpose

This application note provides the reference schematics for USB power delivery (PD) dual-role power (DRP) applications using the EZ-PD™ PMG1 MCU family.

Intended audience

This application note is intended for users who want to use EZ-PD™ PMG1 microcontrollers to design a DRP application. This application note includes DRP reference design schematics using PMG1-S1, PMG1-S2 and PMG1-S3.

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1 EZ-PD™ PMG1 introduction

Infineon's EZ-PD™ PMG1 (first-generation PD microcontroller) is a family of high-voltage USB-C PD MCUs. These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with the analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides or consumes power to or from a high-voltage USB-C PD port and leverages the MCU to provide additional control capability.

The PMG1 MCU family is fully compliant with the USB PD and Type-C standards. **Table 1** compares the features of different MCUs in the EZ-PD™ PMG1 family.

Table 1 Comparison of features of different EZ-PD™ PMG1 family MCUs

Subsystem or range	Item	PMG1-S0*	PMG1-S1	PMG1-S2	PMG1-S3
CPU and memory subsystem	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Maximum frequency (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power delivery	PD ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	Sink	DRP	DRP	DRP
	MOSFET gate drivers	1× PFET	2× PFET	2× NFET	Flexible 2× NFET
	Fault protections	VBUS OVP and UVP	VBUS OVP, UVP and OCP SCP and RCP (for source configuration only)	VBUS OVP, UVP and OCP	VBUS OVP, UVP and OCP SCP and RCP (for source configuration only)
USB	Integrated full-speed USB 2.0 device with billboard class support	No	No	Yes	Yes
Voltage range	Supply (V)	VDDD (2.7 to 5.5) VBUS (4 to 21.5)	VSYS (2.75 to 5.5) VBUS (4 to 21.5)	VSYS (2.7 to 5.5) VBUS (4 to 21.5)	VSYS (2.8 to 5.5) VBUS (4 to 28)
	I/O (V)	1.71 to 5.5	1.71 to 5.5	1.71 to 5.5	1.71 to 5.5
	SCB (configurable as I^2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM block (configurable as timer, counter	4	2	4	7 for 48-QFN 8 for 97-BGA

EZ-PD™ PMG1 introduction

Subsystem or range	Item	PMG1-S0*	PMG1-S1	PMG1-S2	PMG1-S3
	or pulse width modulator)				
	Hardware authentication block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG, CRC)	Yes (AES-128, SHA2-256, TRNG, vector unit)
Analog	ADC	2× 8-bit SAR	1× 8-bit SAR	2× 8-bit SAR	2× 8-bit SAR 1× 12-bit SAR
	On-chip temperature sensor	Yes	Yes	Yes	Yes
Direct memory access (DMA)	DMA	No	No	No	Yes
GPIO	Maximum number of I/Os	12 (10+2 OVT)	17 (15+2 OVT)	20 (18+2 OVT)	26 (24+2 OVT) for 48-QFN 50 (48+2 OVT) for 97-BGA
Charging standard	Charging source	–	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC, and Quick Charge 3.0
	Charging sink	BC 1.2, Apple charging (AC)	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC
ESD protection	ESD protection	Yes (up to ±8 kV contact discharge, up to ±15 kV air discharge, human body model and charged device model)	Yes (human body model and charged device model)	Yes (up to ±8 kV contact discharge, up to ±15 kV air discharge, human body model and charged device model)	Yes (human body model and charged device model)
Packages	Package options	24-QFN (4 × 4 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch) 42-CSP (2.63 × 3.18 mm, 0.4 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch)	48-QFN (6 × 6 mm, 0.5 mm pitch) 97-BGA (6 × 6 mm, 0.5 mm and 0.65 mm pitch)

*PMG1-S0 is a USB PD sink-only device, and therefore does not support DRP applications.

2 USB PD specifications

This section reviews the basics of USB PD. The **USB PD specification** defines how a PD-enabled USB Type-C port can get the required power from VBUS by negotiating with a USB PD-compliant power source.

A USB-C port providing power is known as a “source”, and a USB-C port consuming power is known as a “sink”. There is only one source port and one sink port in each PD connection. In the legacy USB specification, the USB port on the host computer (such as a notebook or a PC) was always a source and the USB peripheral device was always a sink. The USB PD specification allows the source and sink to interchange their roles so that a USB peripheral device (such as an external self-powered hard disk, dock or monitor) can supply power to a USB host. These new power roles are independent of the USB data transfer roles between the USB host and USB device. An example is a self-powered USB peripheral such as a monitor that can charge the battery of a notebook or PC, which is a USB host.

2.1 Type-C and USB PD architecture of a DRP port

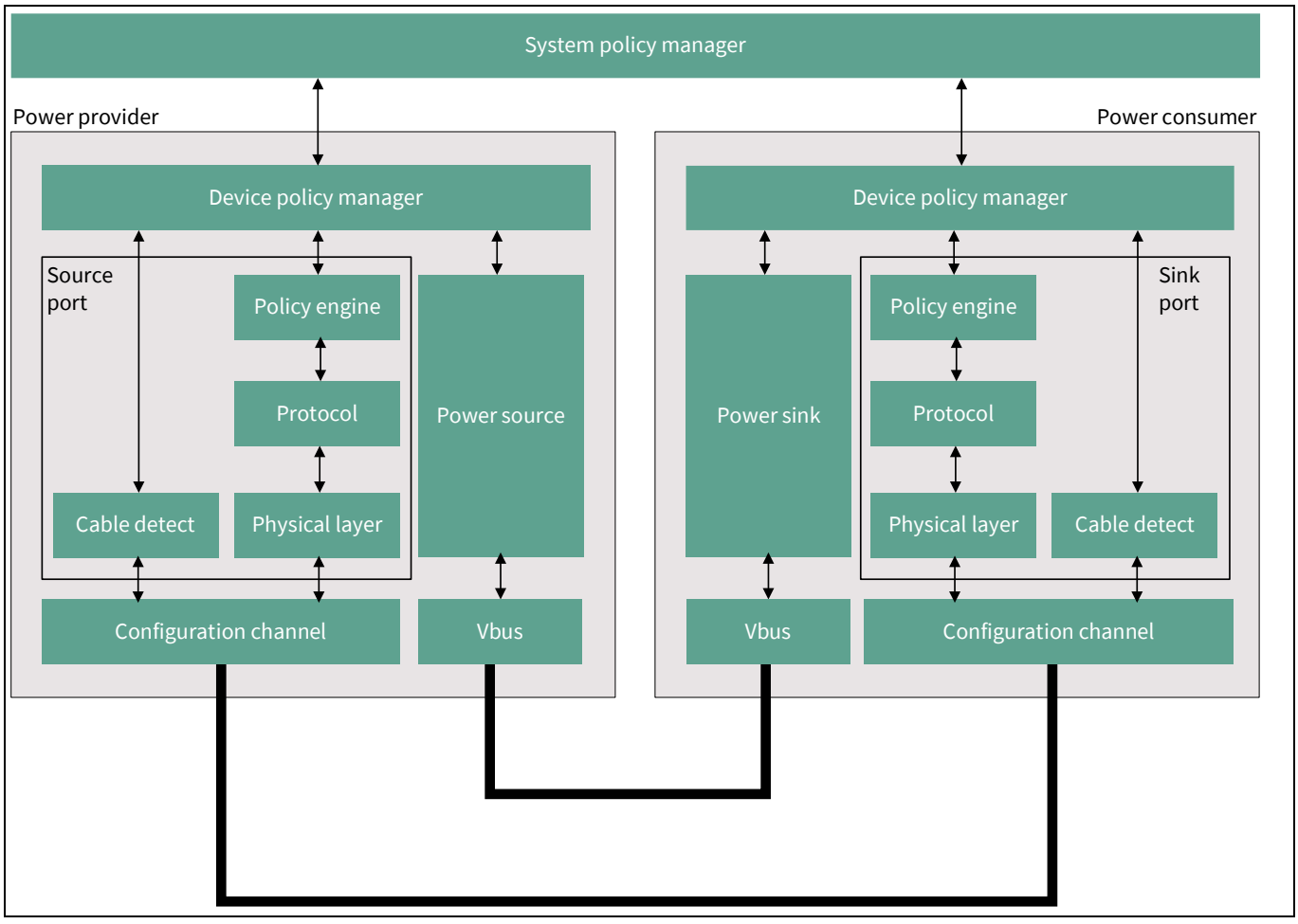

Figure 1 Type-C and PD architecture for DRP applications

System policy manager: The PD specification defines a system policy manager that is implemented on the USB host running as an operating system stack. For more details, see the **USB PD specification**.

Device policy manager: The device policy manager is the module running in the power provider or power consumer, which applies a local policy to each port in the device via the policy engine.

USB PD specifications

Source port: The source port is the power provider port, which supplies power over VBUS. It is, by default, a USB port on the host or hub.

Sink port: The sink port is the USB power consumer port, which consumes power over VBUS. It is, by default, a USB port on a device.

Policy engine: The policy engine interprets the device policy manager's input to implement the policy for the port. It also directs the protocol layer to send messages.

Protocol: The protocol layer creates the messages for communication between port partners.

Physical layer: The physical layer sends and receives messages over either VBUS or the configuration channel (CC) between port pairs.

Power source: The ability of a PD port to source power over VBUS. This refers to a Type-C port with Rp asserted on CC.

Power sink: The ability of a PD port to sink power from VBUS. This refers to a Type-C port with Rd asserted on CC.

Cable detection module: The cable detection module detects the presence of an electronically marked cable assembly (EMCA) cable attached to a Type-C port.

Dual-role devices can be developed by combining both provider and consumer elements in a single device.

When a USB host and USB device are interconnected, they form a USB link pair, and each link partner has a CC controller. Messages are then logically exchanged among device policy managers within each PD controller. These messages are physically transferred over the CC, and a PD contract is set up between the link pair, and then the power is delivered over VBUS. The CC is a new signal pair in the Type-C signal definition (see the **Type-C signal definitions** section for more details).

2.2 Type-C signal definitions

Figure 2 shows the USB Type-C receptacle, plug and flipped-plug signals. The USB Type-C receptacle has USB 3.1 (TX and RX pairs) and USB 2.0 (Dp and Dn) data buses, USB power (VBUS), ground (GND), CC signals (CC1 and CC2), and two sideband use (SBU) signal pins.

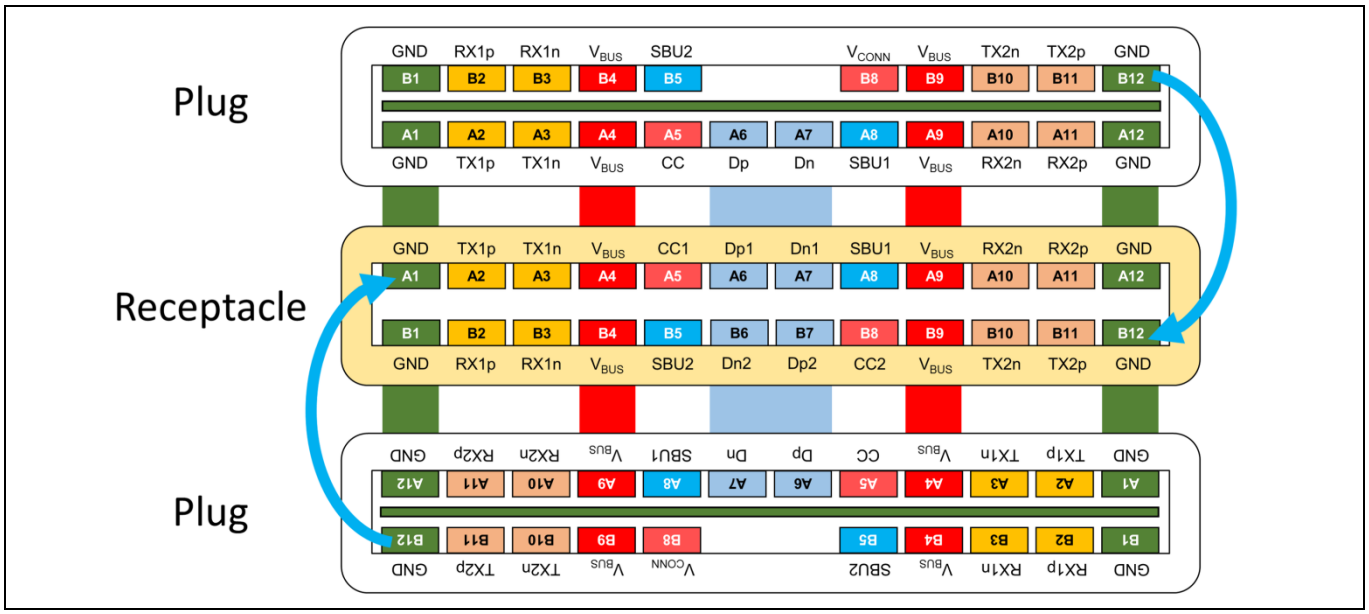

Figure 2 USB Type-C plug, receptacle and flipped-plug signals (source USB Type-C Specification)

USB PD specifications

As listed in **Table 2** and **Table 3**, the descriptions of the USB Type-C plug and receptacle signals are the same, except for the CC and VCONN signals. The two sets of USB 2.0 and USB 3.1 signal locations in this layout facilitate the mapping of the USB signals independent of the plug orientation in the receptacle.

Table 2 USB Type-C receptacle signals

Signal group	Signal	Description
USB 3.1	TX1p, TX1n, RX1p, RX1n, TX2p, TX2n, RX2p, RX2n	The SuperSpeed USB serial data interface defines a differential transmit pair and a differential receive pair. On a USB Type-C receptacle, two pairs of SuperSpeed USB signal pins are defined to enable the plug-flipping feature.
USB 2.0	Dp1, Dn1 Dp2, Dn2	The USB 2.0 serial data interface defines a differential pair. On a USB Type-C receptacle, two sets of USB 2.0 signal pins are defined to enable plug flipping.
Configuration channel	CC1, CC2	The CC in the receptacle detects the signal orientation and channel configuration.
Auxiliary signals	SBU1, SBU2	Sideband use. See the **USB Type-C Cable and Connector Specification Revision 2.1** for more details.
Power	VBUS	USB cable bus power.
	GND	USB cable return current path.

Table 3 USB Type-C plug signals

Signal group	Signal	Description
USB 3.1	TX1p, TX1n RX1p, RX1n TX2p, TX2n RX2p, RX2n	The SuperSpeed USB serial data interface defines a differential transmit pair and a differential receive pair. On a USB Type-C plug, two pairs of SuperSpeed USB signal pins are defined to enable the plug-flipping feature.
USB 2.0	Dp, Dn	On a USB Type-C plug, the USB 2.0 serial data interface defines a differential pair.
Configuration channel	CC	The CC in the plug is used for connection detection and interface configuration.
Auxiliary signals	SBU1, SBU2	Sideband use. See the **USB Type-C Cable and Connector Specification Revision 2.1** for more details.
Power	VBUS	USB cable bus power.
	VCONN	Type-C cable plug power.
	GND	USB cable return current path.

When a cable with the Type-C plug is inserted into the receptacle, one CC pin is used to establish signal orientation, and the other CC pin is repurposed as VCONN for powering the electronics in the USB Type-C cable (plug).

2.3 Type-C ports

2.3.1 Downstream-facing port and upstream-facing port

A Type-C downstream-facing port (DFP) is, by default, a USB host and a power source, whereas a Type-C upstream-facing port (UFP) is, by default, a USB device and a power sink. A DFP exposes Rp terminations on its CC pins (CC1 and CC2), while a UFP exposes Rd terminations on its CC pin, as shown in **Figure 3**.

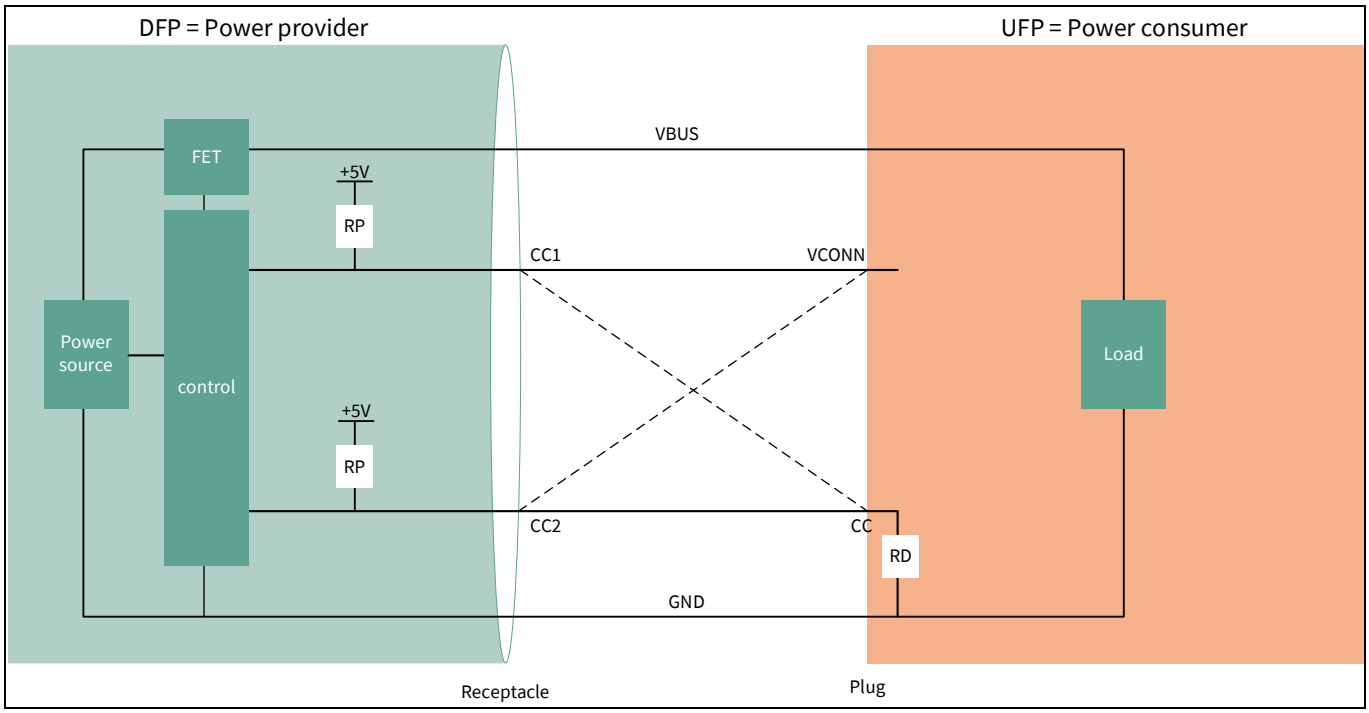

Figure 3 Direct connection of a DFP and UFP

2.4 USB PD dual-role power

A USB-C port configured as DRP can operate as either a power provider or power consumer, or may alternate between these two states. Initially, when operating as a power provider, the port takes the data role of a DFP and, when operating as a sink, the port takes the data role of a UFP. However, the port's power role can be dynamically changed using the USB PD message (power role swap). For example, a laptop, when connected to a dock, can initially become a power provider and a DFP. The dock or the laptop can later issue a power role swap to become a power provider or consumer, respectively.

The DRP devices have the capability to detect the presence of the Rp and Rd resistors on the CC lines. A typical DRP device can perform the roles listed in **Table 4**.

Table 4 Roles of DRP device

No.	Data port role (USB host or device)	Power port role (power provider or power consumer)
1	DFP	Source (power provider; connect Rp and disconnect Rd)
2	DFP	Sink (power consumer; disconnect Rp and connect Rd)
3	UFP	Source (power provider; connect Rp and disconnect Rd)
4	UFP	Sink (power consumer; disconnect Rp and connect Rd)

2.5 USB Type-C alternate mode

The USB Type-C supports alternate modes on some of the pins in the USB-C 3.1 cable for alternate data protocols, such as Thunderbolt, DisplayPort and HDMI. The four high-speed lanes, two SBU pins and one configuration pin can be used for alternate mode transmission. The modes are configured using vendor-defined messages (VDMs) through the CC.

In DRP applications, such as docks, the Type-C port needs to switch between USB SuperSpeed and alternate mode (such as DisplayPort). PMG1 MCUs support alternate mode protocol required for reconfiguring the Type-C port via CC line. To enable switching between USB SS and DisplayPort mode, a high-speed mux/switch is used along with the PMG1 MCU. **Figure 4** shows the basic implementation of a DisplayPort alternate mode with PMG1 MCUs.

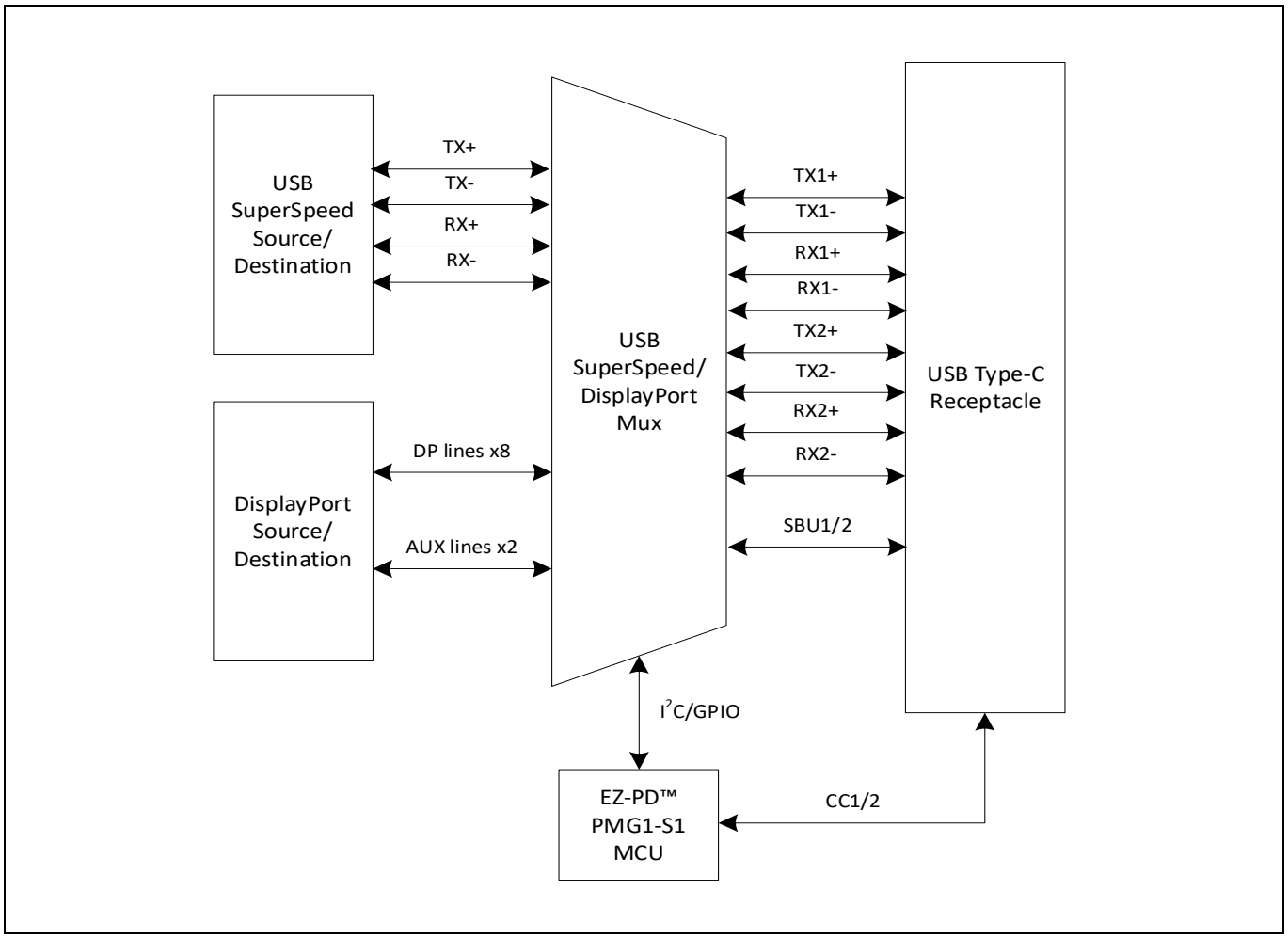

Figure 4 USB Type-C DisplayPort alternate mode

The DRP schematic designs provided with this application note include the DisplayPort alternate mode mux in the design files. The design in PMG1-S1 and PMG1-S3 uses PI3DPX1205A Type-C mux from Pericom, and the design in PMG1-S2 uses PS8740 Type-C mux from Parade Technologies. The alternate mode implementation is application-specific, and the users can decide to not include the DisplayPort mux schematics in the end application.

3 PMG1-S1 DRP hardware design

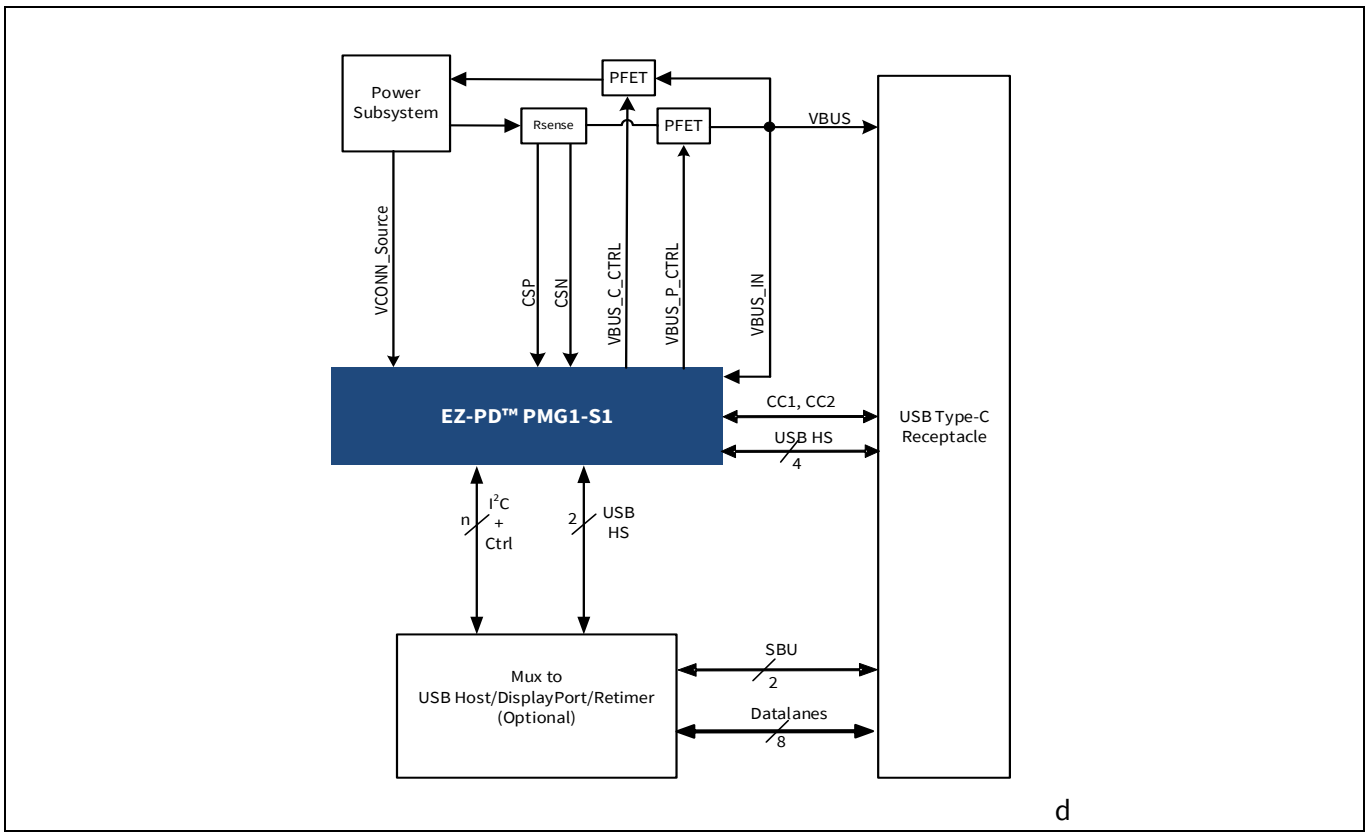

Figure 5 Single-port Type-C DRP design using EZ-PD™ PMG1-S1

For the full reference schematic and design files, see the **EZ-PD™ PMG1 S1 DRP reference schematic** in the **EZ-PD™ PMG1-Sx DRP reference schematics.zip** file.

3.1 System power supply design

The PMG1-S1 DRP design reference schematic design uses the NCP81239 buck-boost DC-DC converter from onsemi as a variable-output VBUS source. The voltage output of the regulator can be controlled using the I^2C interface.

The design reference also consists of two step-down regulators to generate the 5 V and 3.3 V outputs to provide for VCONN and PMG1-S1 system power.

The PMG1-S1 MCU operates with two possible external supply voltages, VBUS or VSYS. The VDDIO supply powers the device I/Os as shown in **Table 5**. VDDD generates 3.3 V from an internal regulator, and this can be shorted to VDDIO. VCCD is the output voltage from the core regulator, and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. PMG1-S1 has power supply inputs at the VCONN_Source pin for providing power to EMCA cables through integrated VCONN FETs.

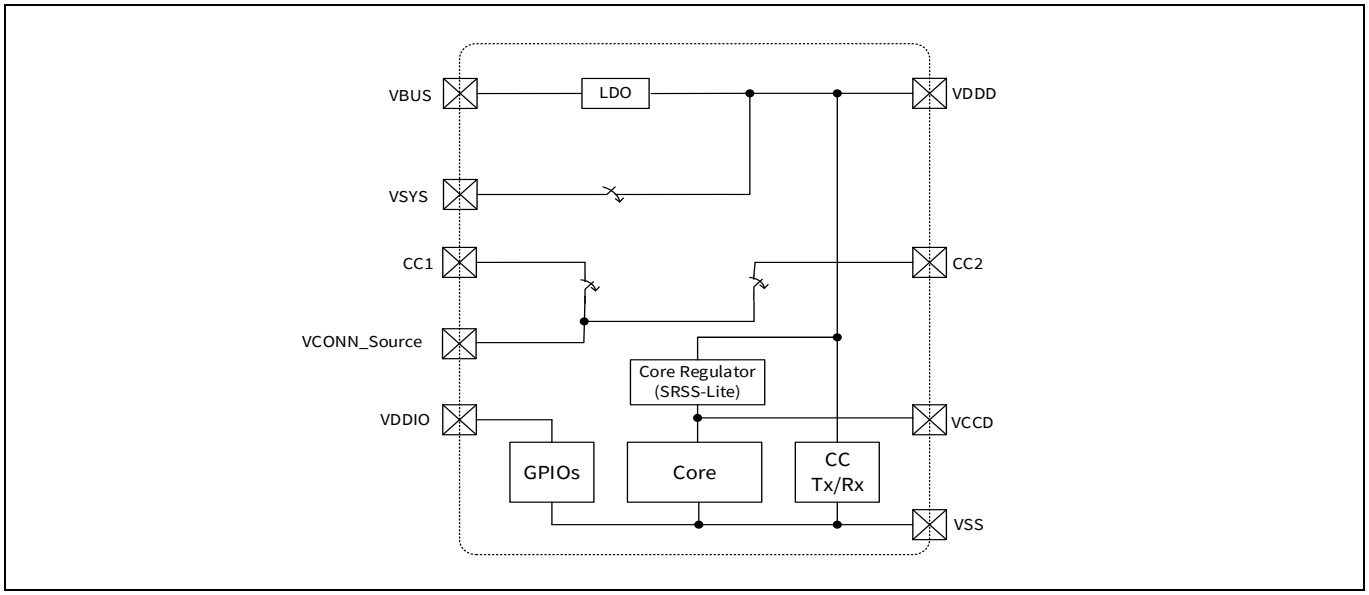

Figure 6 PMG1-S1 power supply system design

Table 5 PMG1-S1 operating voltage

Parameter	Minimum (V)	Maximum (V)
VBUS	4.0	21.5
VSYS	2.75	5.5
VDDD	VSYS-0.05	VSYS
VDDIO	VDDD	VDDD
VCONN_Source	4.85	5.5

3.2 Power provider and consumer circuits

This section explains the recommended external hardware circuitry for VBUS control, overvoltage (OV), overcurrent (OC), reverse current (RC) and short-circuit (SC) protection in a DRP design. A DRP design, such as a portable speaker, using a PMG1-S1 device can be a power provider when running from its internal battery and a power consumer when being charged from the connected power sources, such as power adapters and monitors.

3.2.1 Control of the VBUS provider path and VBUS consumer path

The PMG1-S1 device consists of two I/Os with integrated PFET gate drivers, namely VBUS_P_CTRL and VBUS_C_CTRL, to control the VBUS provider (sourcing of power) and consumer (sinking of power) path connecting the Type-C port to the power source and consumer.

Figure 7 shows the recommended implementation to control this VBUS path.

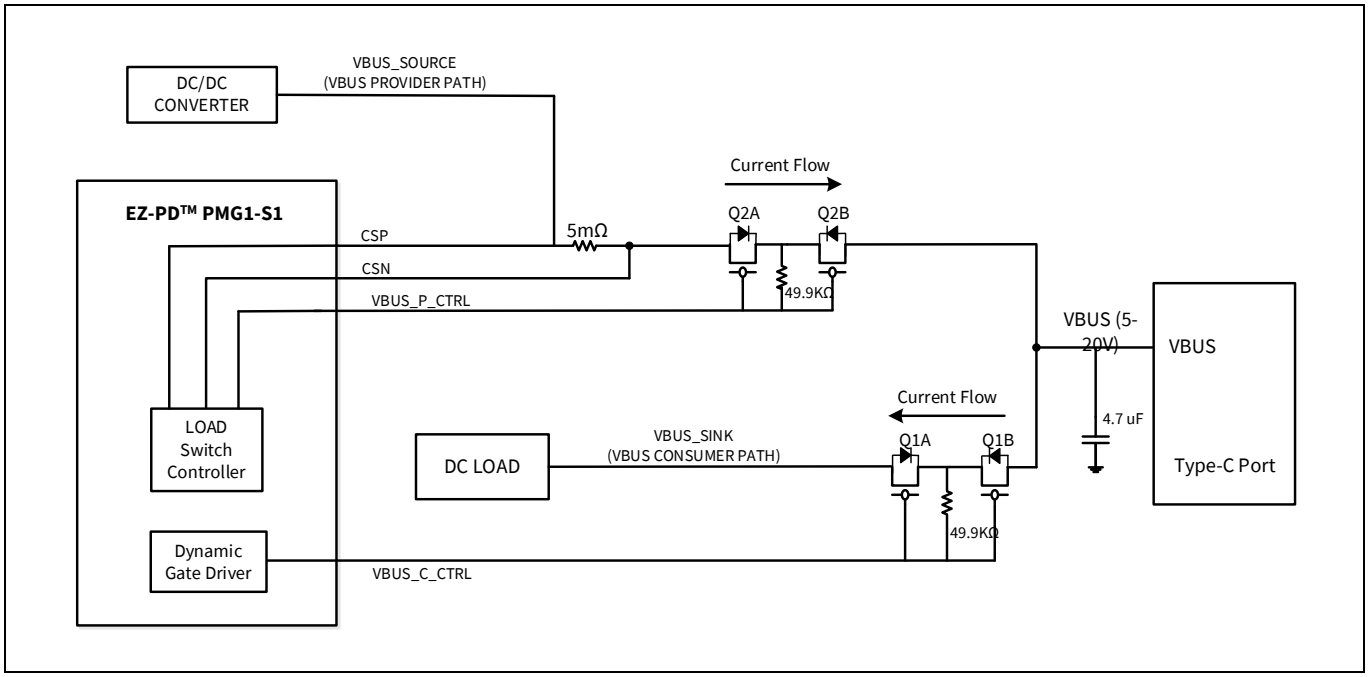

Figure 7 PMG1-S1 VBUS provider and consumer path control

3.2.2 Control of VBUS discharge path

Depending on the connected downstream device, the VBUS voltage varies as illustrated by the following example scenarios:

- **Example scenario 1:** A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from a Type-C port, and immediately another UFP device sinking 15 W of power (5 V, 3 A) is connected to the same Type-C port.
- **Example scenario 2:** An externally powered dock, changing its power role from provider (sourcing 100 W of power) to consumer (sinking 15 W of power) due to a power role swap.

In both the scenarios, the VBUS capacitor shown in **Figure 8** may not have discharged fully from the original 20 V.

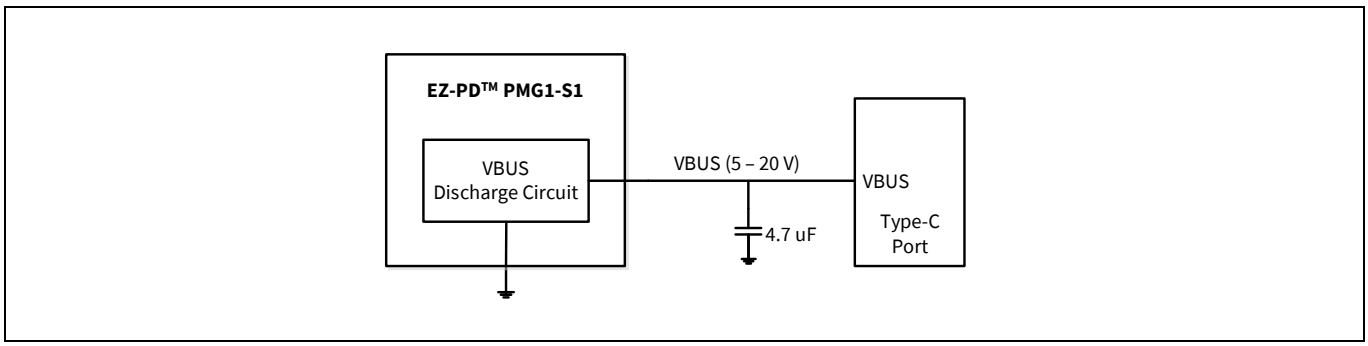

Figure 8 VBUS discharge control circuitry

To prevent this OV on VBUS, the PMG1-S1 device provides a built-in VBUS discharge circuit that provides a discharge path for the VBUS capacitor as shown in **Figure 8**. This avoids OV scenarios as in examples 1 and 2. The discharge strength can be controlled by the firmware.

3.2.3 Undervoltage and overvoltage protection (UVP/OVP) for VBUS

PMG1-S1 implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detectors have programmable thresholds that can be controlled by the firmware. The inputs to the UV and OV comparators are a division (8 percent or 10 percent) of VBUS supply voltage and a reference voltage. The reference voltage is configurable in the range of 200 mV to 2190 mV in steps of 10 mV.

Figure 9 shows the built-in UVP/OVP circuit for PMG1-S1 MCU. The inputs to the comparator are a reference voltage (vref_out) from the REFGEN module and either 8 percent or 10 percent of the VBUS. The vref_out[3] and vref_out[2] voltages in the reference generator must be programmed through the firmware to adjust the UVP and OVP levels.

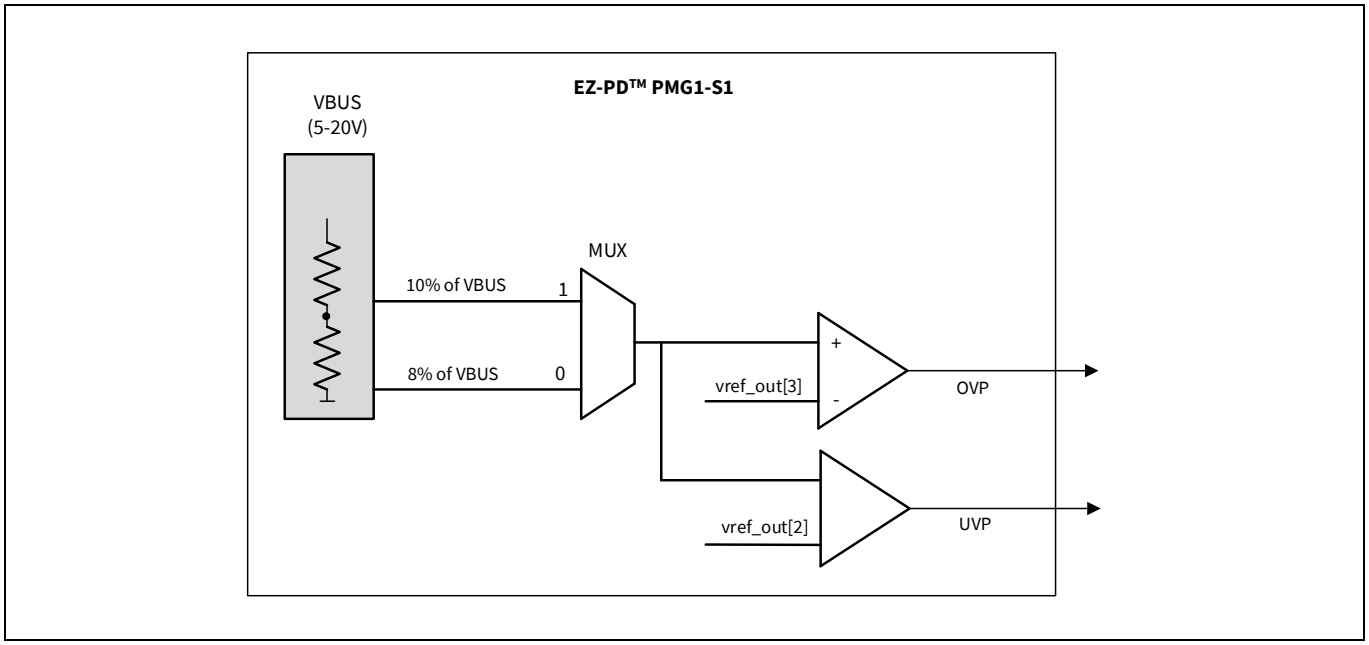

Figure 9 UVP/OVP implementation in PMG1-S1

3.2.4 Overcurrent/short-circuit/reverse-current protection (OCP/SCP/RCP) for VBUS

PMG1-S1 has an integrated high-side current sense amplifier (CSA) that can detect the current in the VBUS provider path via an external 5 mΩ resistor. The CSA is coupled with comparators for detecting the OC, SC and RC, which can be used to detect the OC, SC and RC fault in the VBUS provider path.

Figure 10 shows the implementation of a 5 mΩ CS resistor in the VBUS provider path to detect OC, SC and RC faults. The PMG1-S1 generates interrupt on faults to automatically turn off the power FETs.

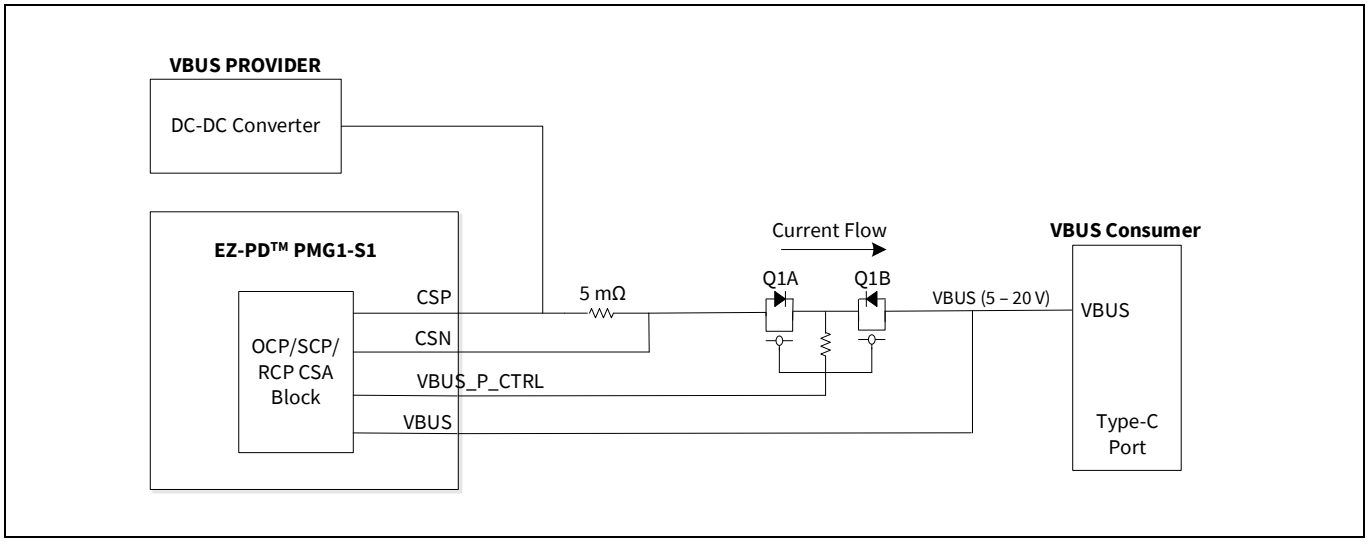

Figure 10 OC, SC and RC detection for PMG1-S1 DRP design

3.2.5 OCP for VCONN

PMG1-S1 has a power supply input, VCONN_Source, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs to supply VCONN on either the CC1 or CC2 pins. These FETs can provide 1.5 W power over VCONN on the CC1 and CC2. As shown in **Figure 11**, PMG1-S1 has a built-in VCONN OCP circuit, and therefore, no external circuitry is required to implement OCP for VCONN in a system using PMG1-S1.

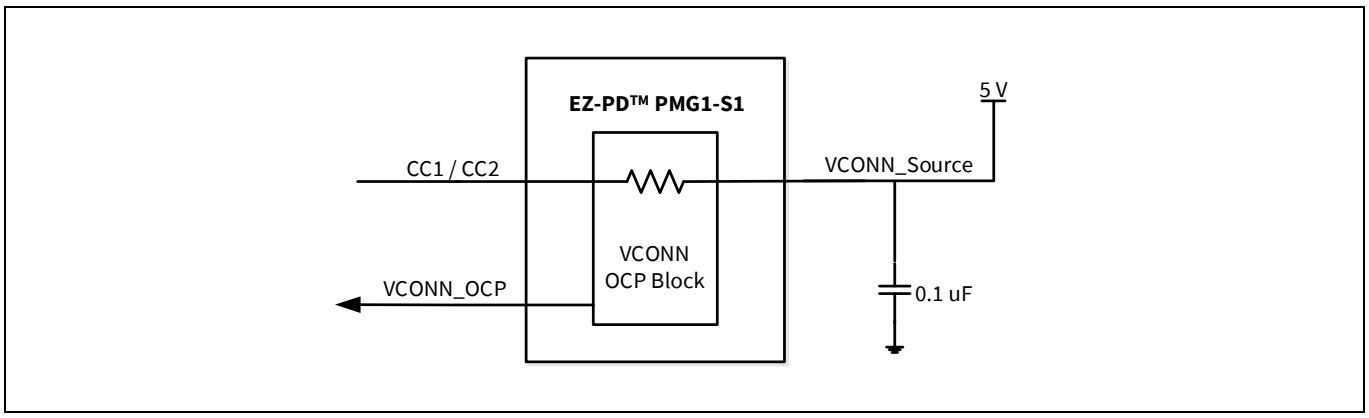

Figure 11 VCONN OCP for PMG1-S1

3.3 Type-C alternate mode implementation

The PMG1-S1 DRP schematic design provided with this application note consists of the DisplayPort alternate mode multiplexer included. The PMG1-S1 design uses PI3DPX1205A from Pericom. The alternate mode implementation is application-specific, and the users can decide to not include the DisplayPort mux schematics in the end application.

PMG1-S1 has a built-in USB high-speed mux to route the system DP and DM lines to the Type-C top or bottom port based on the CC (Type-C plug) orientation. This USB 2.0 mux also contains the charger detection feature for USB BC1.2 legacy charging systems.

PMG1-S1 DRP hardware design

Figure 12 shows the alternate mode implementation for PMG1-S1 design schematics.

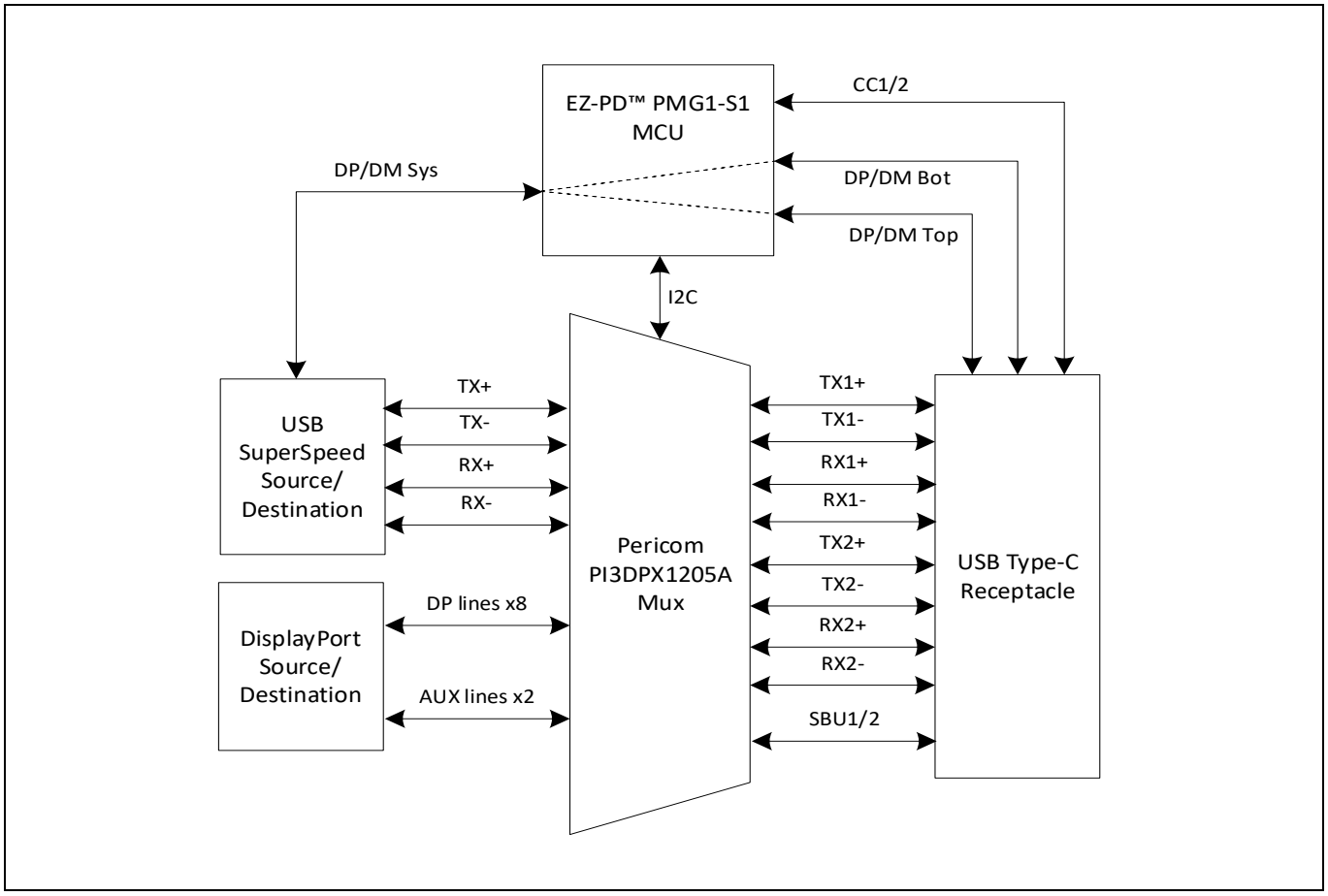

Figure 12 USB Type-C DisplayPort alternate mode for EZ-PD™ PMG1-S1

4 PMG1-S2 DRP hardware design

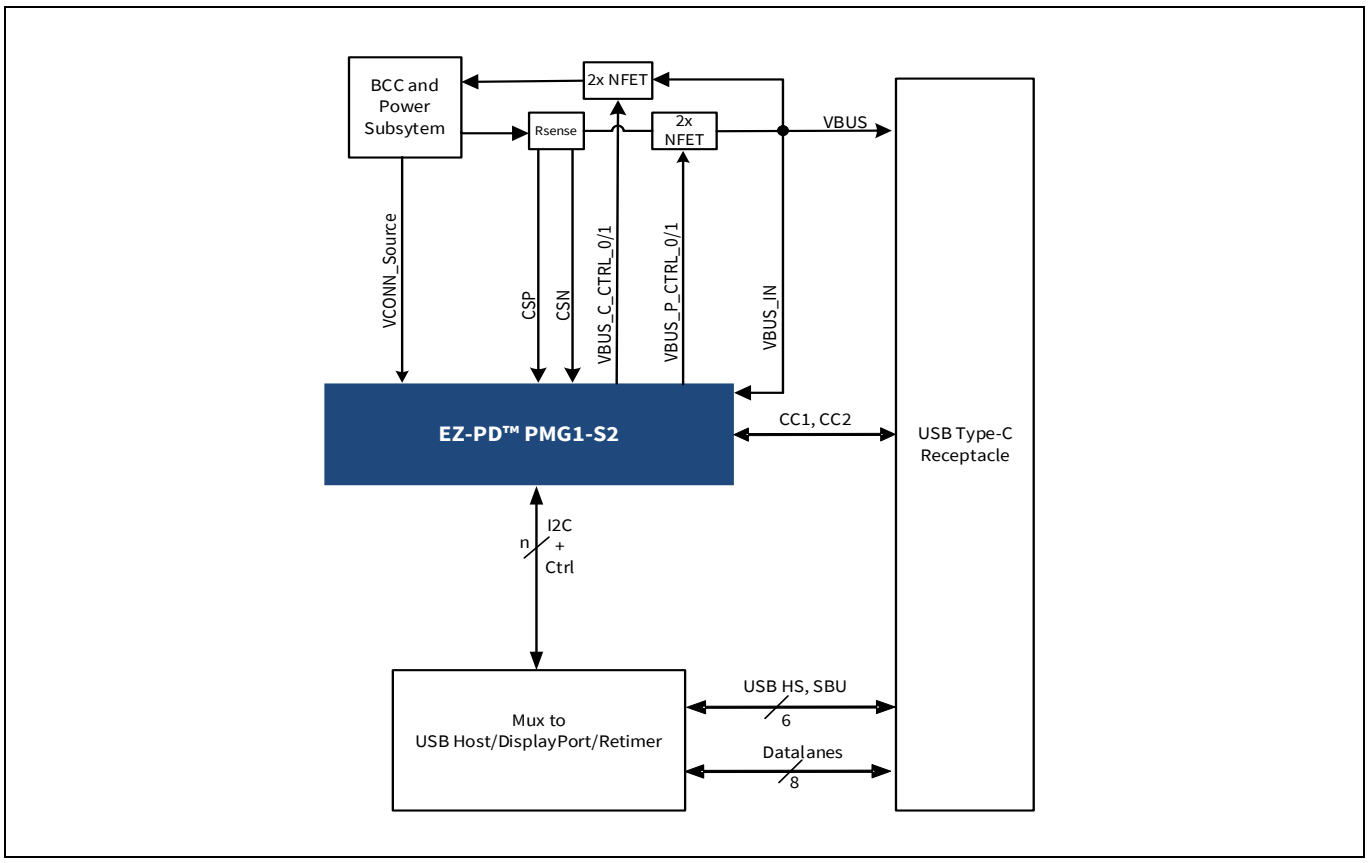

Figure 13 Single-port Type-C design using EZ-PD™ PMG1-S2

For the full reference schematic, see the **EZ-PD™ PMG1-S2 DRP reference schematic** in the **EZ-PD™ PMG1-Sx DRP reference schematics.zip** file.

4.1 System power supply design

The PMG1-S2 DRP design reference schematic design uses the buck converter based on NCP1034 from onsemi as a variable-output VBUS source. The voltage output of the regulator can be controlled using the analog feedback to the internal reference. The PMG1-S2 reference schematic is designed for VBUS output of the 5 V, 9 V, 15 V and 20 V options using GPIO control.

The design reference also consists of two step-down regulators to generate the 5 V and 3.3 V outputs to provide for VCONN and PMG1-S2 system power.

PMG1-S2 MCU operates with two possible external supply voltages, VBUS or VSYS. The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO) down to 3.3 V level. The chip's internal VDDD rail intelligently switches between the output of the VBUS regulator and unregulated VSYS. The VDDD is either used directly inside some analog blocks or further regulated to VCCD. The VCCD pin is intended to connect only to a decoupling capacitor. The VCCD pin cannot be used as a voltage source. A separate power domain VDDIO is provided for the GPIOs. The VDDIO supply powers the device I/Os as shown in **Table 6**. The VDDIO pin can also be shorted to VDDD. PMG1-S2 has power supply inputs at the VCONN_Source pin for providing power to EMCA cables through integrated VCONN FETs.

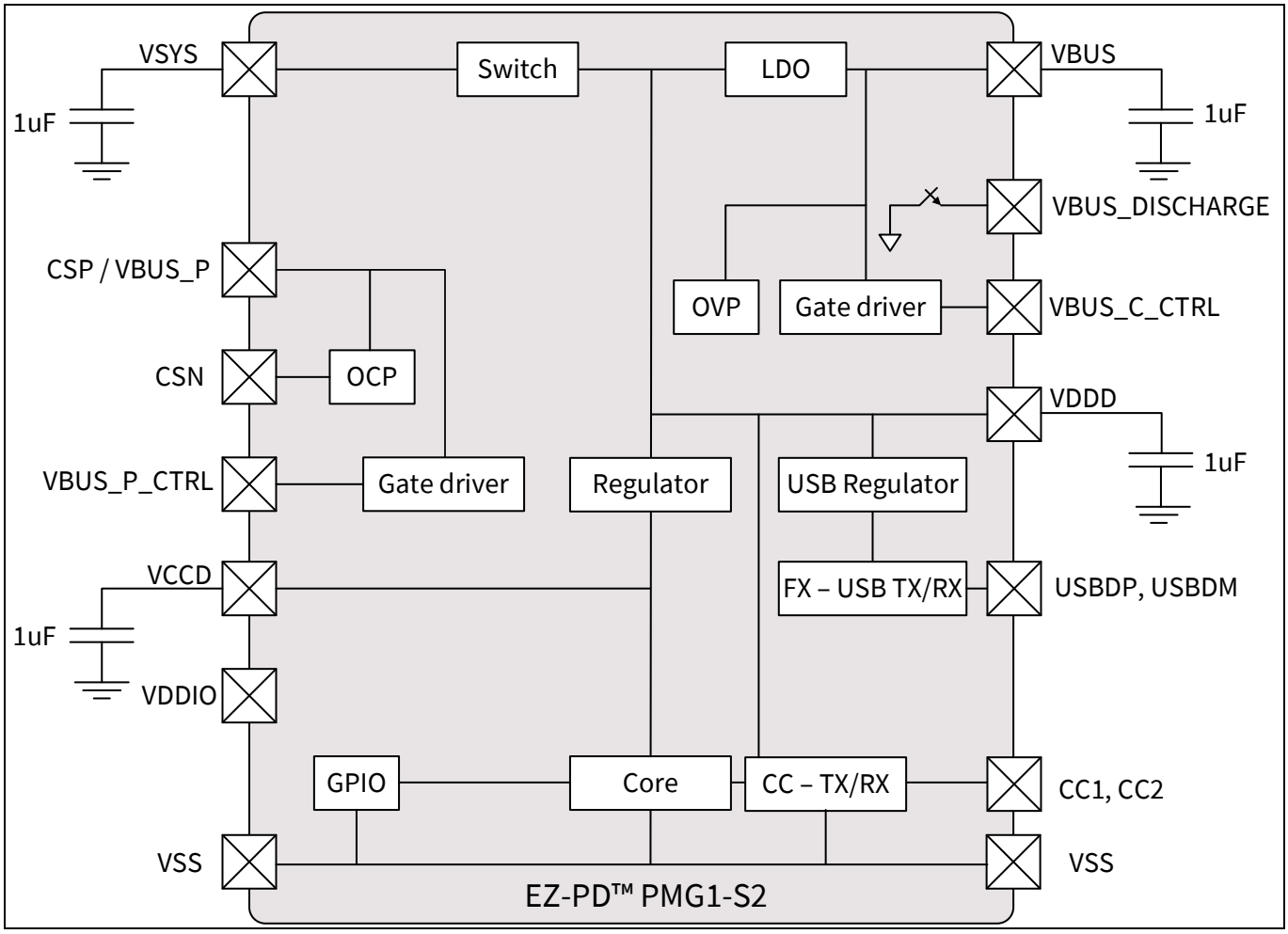

Figure 14 EZ-PD™ PMG1-S2 power supply system design

Table 6 PMG1-S2 operating voltage

Parameter	Minimum (V)	Maximum (V)
VBUS	4.0	21.5
VSYS	4.5	5.5
VDDD	2.7	5.5
VDDIO	1.71	VDDD
VCONN_Source	2.7	5.5

4.2 Power provider and consumer circuits

This section explains the recommended external hardware circuitry for VBUS control, OV and OC in a DRP design. A DRP design using a PMG1-S2 device will be a power provider when running from its internal battery, and a power consumer when being charged from the connected power sources, such as power adapters and monitors.

4.2.1 Control of VBUS provider path and VBUS consumer path

PMG1-S2 consists of four gate drivers, namely VBUS_P_CTRL1, VBUS_P_CTRL0, VBUS_C_CTRL1 and VBUS_C_CTRL0, to control the VBUS provider path (Type-C port to VBUS power source) and VBUS consumer

path (Type-C port to power consumer). **Figure 15** shows the recommended implementation of FETs to control this VBUS path.

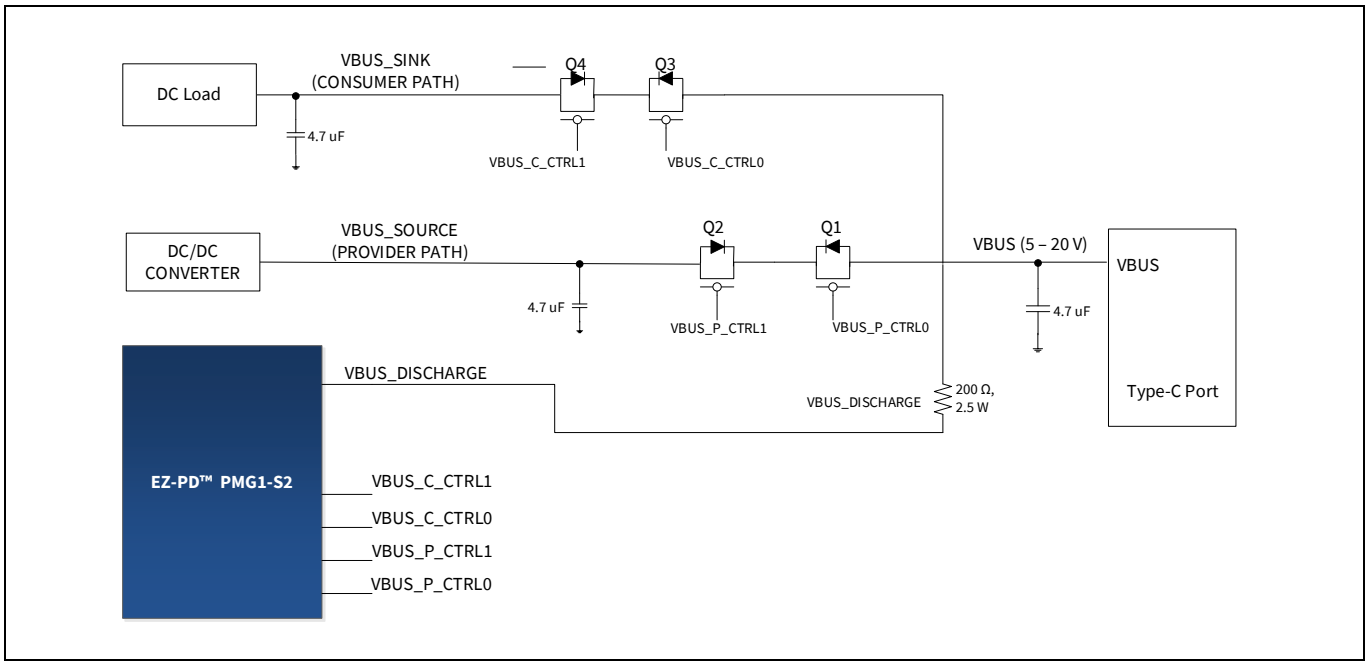

Figure 15 EZ-PD™ PMG1-S2 VBUS provider and consumer path control

VBUS_P_CTRL1 and VBUS_P_CTRL0 are active high pins. FETs Q1 and Q2 turn on when both the pins are high. This turns on the VBUS provider path. Similarly, when VBUS_C_CTRL1 and VBUS_C_CTRL0 are high, FETs Q3 and Q4 turn on, which turns on the VBUS consumer path.

The diodes between the source and drain terminals of FETs Q1 and Q2 turn off the VBUS provider path completely when the VBUS consumer path is active. Similarly, the diodes between the source and drain terminals of FETs Q3 and Q4 turn off the VBUS consumer path completely when the VBUS provider path is active.

4.2.2 Control of VBUS discharge path

Depending on the connected downstream device, the VBUS voltage varies, as illustrated by the following example scenarios:

- **Example scenario 1:** A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from the Type-C port, and immediately another UFP device sinking 15 W of power (5 V, 3 A) is connected to the same Type-C port.
- **Example scenario 2:** An externally powered dock, changing its power role from the provider (sourcing 100 W of power) to consumer (sinking 15 W of power) due to a power role swap.

In both scenarios, the VBUS capacitor shown in **Figure 15** may not have discharged fully from the original 20 V when there is disconnect or a power role change, respectively.

PMG1-S2 provides a discharge path to the VBUS capacitor by triggering the VBUS discharge pin. VBUS discharge is an active high signal, which turns on the integrated VBUS discharge FET in PMG1-S2, causing a discharge of the VBUS capacitor through an external resistor, as shown in **Figure 15**. It is necessary to use the series resistor (200 Ω) with a minimum 2.5 W power rating as the power dissipation during VBUS discharge will be high.

4.2.3 UVP/OVP for VBUS

PMG1-S2 includes integrated UVP/OVP circuits to sense UV and OV conditions on VBUS. PMG1-S2 has a built-in UVP/OVP circuit to detect and protect the system against UV and OV faults, and therefore, no external circuit is required.

The PMG1-S2 UVP/OVP fault detection threshold can be configured in the firmware with respect to the negotiated VBUS voltage. If the VBUS voltage exceeds the UVP/OVP trip voltage, PMG1-S2 detects the UV and OV at VBUS and turns off the VBUS (Q1 and Q2 in **Figure 15**) from the external power supply. PMG1-S2 also turns off power consumer FETs (Q3 and Q4 in **Figure 15**) and disconnects itself from the Type-C port.

4.2.4 OCP for VBUS

PMG1-S2 includes an integrated CSA and comparator to sense OC conditions on VBUS. PMG1-S2 detects the OC condition at VBUS using a CS resistor and turns off the VBUS by turning off the gate drivers to turn off the power provider FETs Q1 and Q2. PMG1-S2 also disconnects itself from the Type-C port.

The CSN pin is the OC sensor input pin to PMG1-S2. This pin should be connected to the VBUS_P/CSP pin of PMG1-S2 through a 10 mΩ sense resistor to sense the input current, as shown in **Figure 16**.

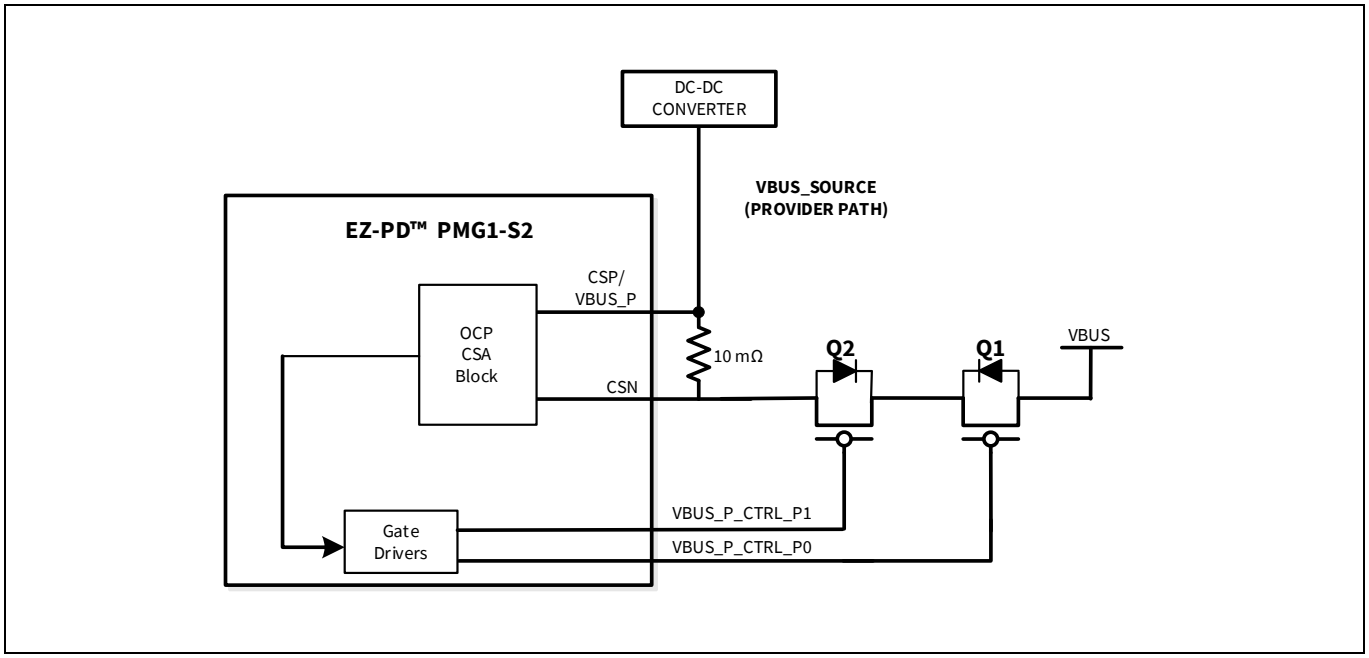

Figure 16 OCP circuitry in PMG1-S2

4.2.5 OCP for VCONN

In a DRP system design, VCONN supplies power to the EMCA attached to it. PMG1-S2 integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the VCONN_Source pin. The FETs on the CC lines can handle a current up to 0.5 A. The OCP circuitry is required on VCONN to prevent damage to the system if VCONN current exceeds 0.5 A. Designs based on PMG1-S2 need an external circuit to detect the VCONN overcurrent condition. The design included with this application note uses the AP2822A power switch from Diodes Inc. to implement VCONN current protection.

Figure 17 shows the circuit based on AP2822A to implement OCP for VCONN in a DRP application design using PMG1-S2.

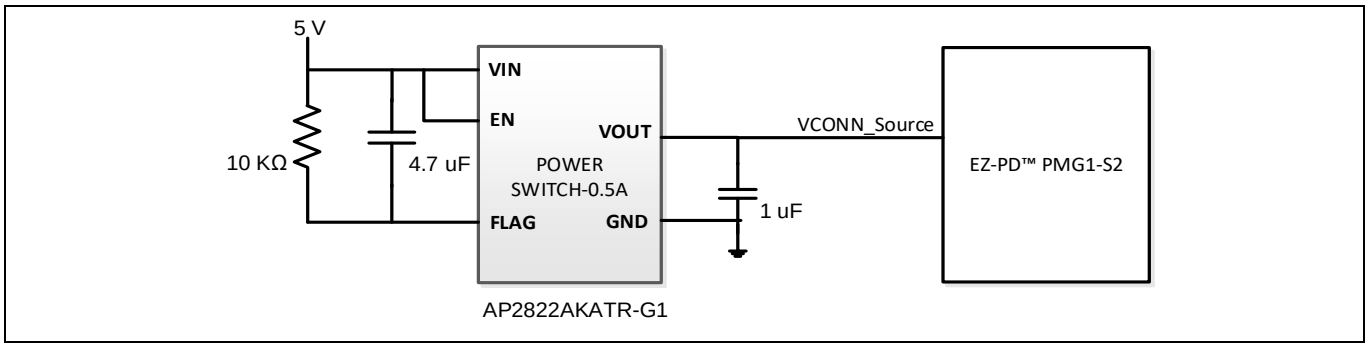

Figure 17 OCP for VCONN

Note: The VCONN power switch (AP2822AKATR-G1) has an OC detection limit of 0.5 A. The output of the switch (V_{OUT}) is connected to the VCONN_Source of PMG1-S2. The 5 V supply (V_{IN}) to the VCONN power switch is an output voltage of the 5 V regulator in a system. If the VCONN current exceeds the OC detection limit of 0.5 A, the V_{OUT} (5 V) power supply is shut down by the power switch, preventing any damage to the system.

4.3 Type-C alternate mode implementation

The PMG1-S2 DRP schematic design provided with this application note consists of the DisplayPort alternate mode multiplexer included. The design in PMG1-S2 uses PS8740 Type-C mux from Parade Technologies. The alternate mode implementation is application-specific, and the users can decide to not include the DisplayPort mux schematics in the end application.

PMG1-S2 has a built-in analog crossbar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins, which can be used to multiplex the AUX signals to the SBU pins of the Type-C port. PMG1-S2 also has a DisplayPort hot-plug detect processor, and HPD from DisplayPort can be directly connected to PMG1-S2.

PMG1-S2 DRP hardware design

Figure 18 shows the alternate mode implementation for PMG1-S2 design schematics.

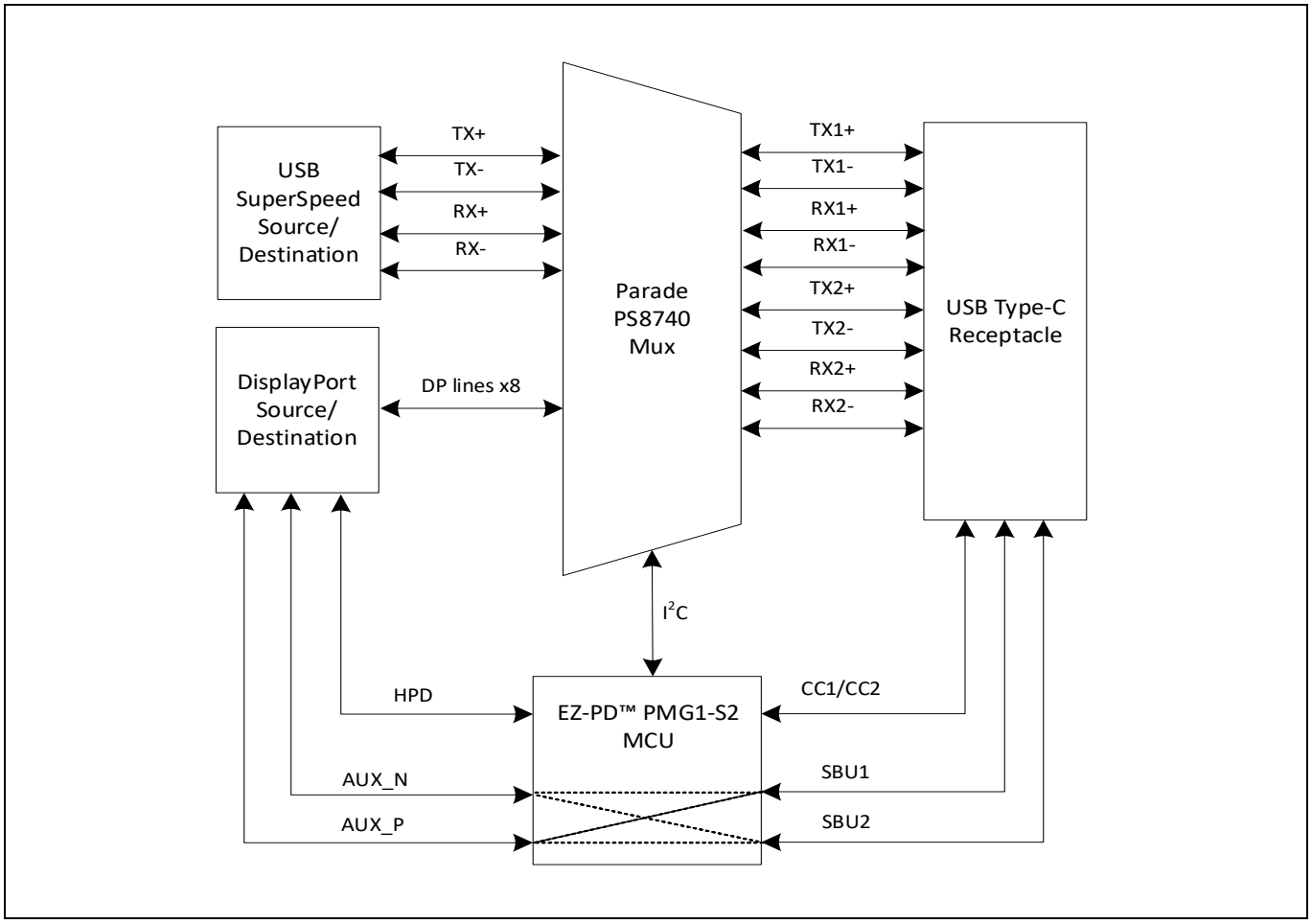

Figure 18 USB Type-C DisplayPort alternate mode for PMG1-S2

5 PMG1-S3 DRP hardware design

PMG1-S3 MCU is available in two device package options: 48-QFN and 97-BGA. The 48-QFN variant is a single-port USB PD device, whereas the 96-BGA variant is a dual-port USB PD device. This application note discusses the single-port (Port-0) DRP design using 48-QFN device variant, in detail. All the subsystems in the dual-port (Port-0 and Port-1) design are duplicates of Port-0.

The schematic designs files for both single-port and dual-port implementations are attached with this application note. See **EZ-PD™ PMG1 S3 DRP single-port reference schematic** and **EZ-PD™ PMG1 S3 DRP dual-port reference schematic** in the **EZ-PD™ PMG1-Sx DRP reference schematics.zip** file for more details.

5.1 USB PD extended power range (EPR)

USB PD revision 3.1 added the EPR mode to the existing USB PD power levels, which allows VBUS to reach higher voltages of 28 V, 36 V and 48 V, providing up to 240 W of power (48 V at 5 A), and the adjustable voltage supply (AVS) protocol, which allows specifying the voltage from a range of 15 V to 48 V in 100 mV steps. The existing USB PD power modes are retroactively renamed as standard power range (SPR).

PMG1-S3 MCU is EPR-capable for a VBUS level of up to 28 V. This makes it possible to use the PMG1-S3 device in the EPR applications with reduced BOM count. The PMG1-S3 DRP design-reference schematics are designed with EPR compatibility and, therefore, fully support operations up to 28 V of VBUS (nominal).

The difference between an SPR and EPR hardware design is to select the components with appropriate voltage ratings on the VBUS path. The USB PD revision 3.1 recommends the component voltage rating of 55 V (absolute) for EPR operation, whereas for SPR operation, the recommended voltage rating is 24 V (absolute).

5.1.1 Migrating the PMG1-S3 EPR design to SPR only

If EPR is not required in the DRP design, the VBUS DC-DC buck-boost converter and components on the VBUS path can be replaced with the components to support the operation up to a maximum of 24 V. The **EZ-PD™ PMG1 S3 DRP single-port reference schematic** and BOM in the **EZ-PD™ PMG1-Sx DRP reference schematics.zip** file have EPR components placed. To build an SPR-only design, the PD regulator and FETs on the VBUS provider and consumer path FETs can be changed to a 24 V maximum design to reduce the overall system cost. These components can be picked from the PMG1-S1 or PMG1-S2 reference schematics.

Figure 19 and **Figure 20** show the parts which can be replaced for VBUS regulator and VBUS provider/consumer FETs in the PMG1-S3 schematic.

5.1.1.1 EPR VBUS regulator migration

The EPR reference schematic uses the MP4247 buck-boost converter from Monolithic Power Systems to provide VBUS up to 28 V. To switch to an SPR design, replace the following parts:

1. U2: MP4247
2. Q3 and Q4: BSC059N04LS6ATMA1
3. All capacitors between the provider and consumer voltage to ground

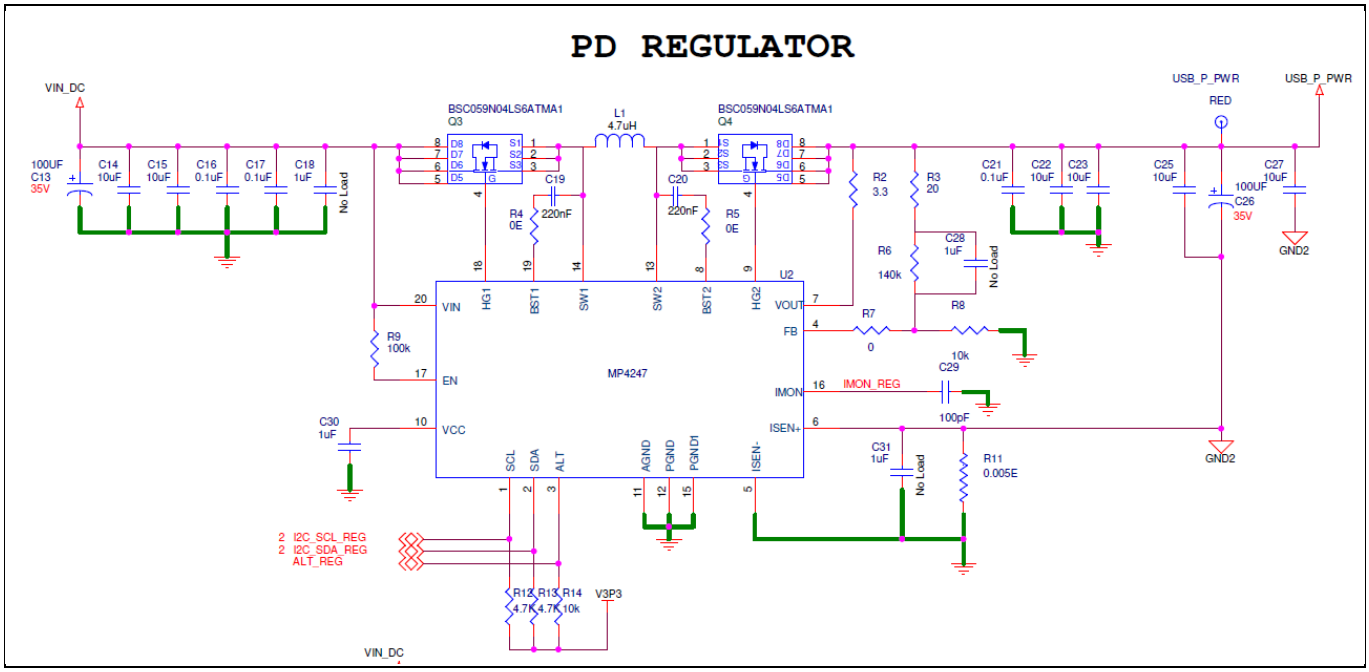

Figure 19 EPR-capable VBUS regulator in PMG1-S3 DRP schematic

5.1.1.2 VBUS provider/consumer path FET migration

Replace the following parts:

1. Q1 and Q2: BSC059N04LS6ATMA1
2. Q5 and Q6: SPP80P06P

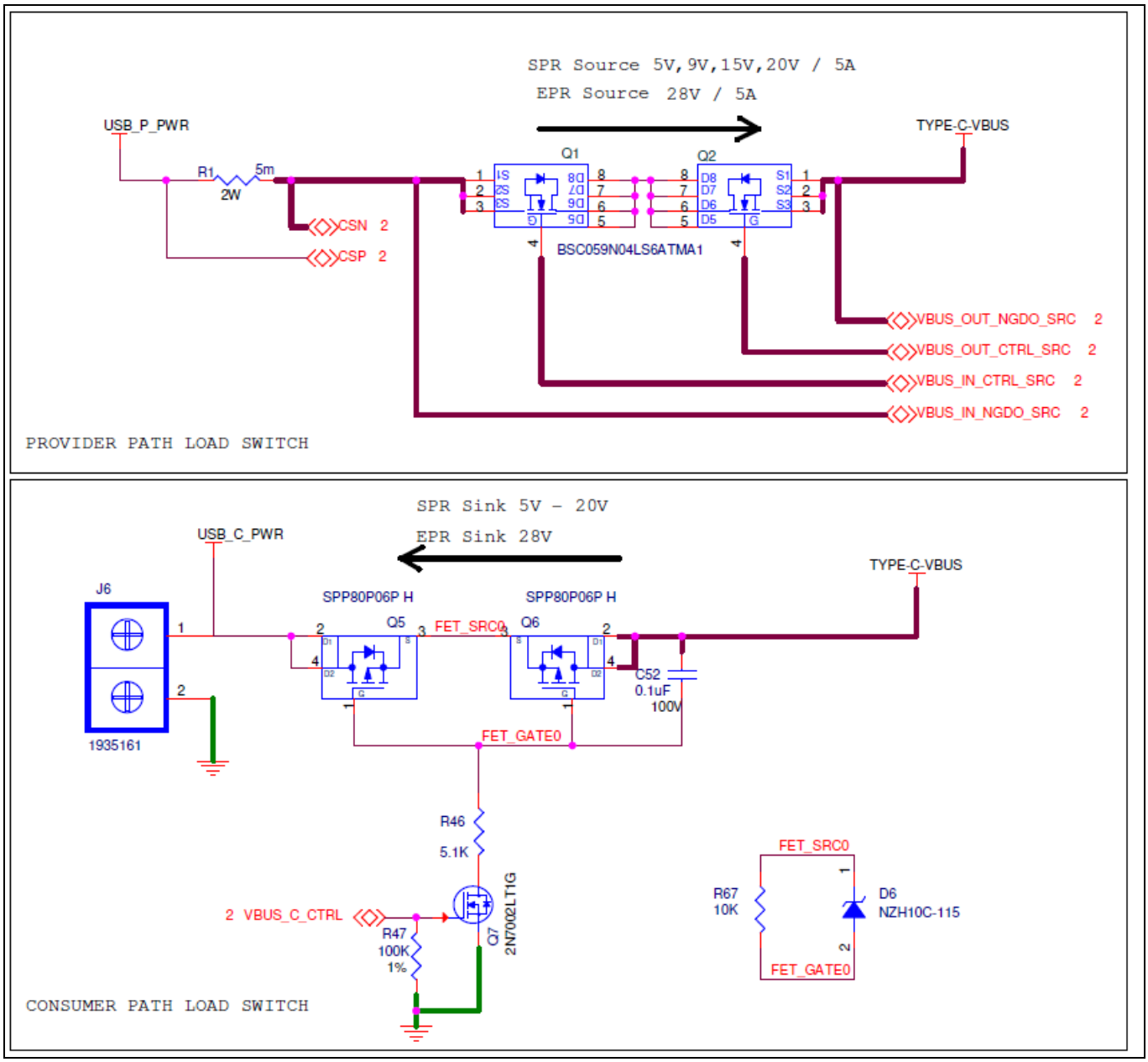

Figure 20 EPR-capable VBUS FET selection in PMG1-S3 DRP schematic

5.2 PMG1-S3 single-port and dual-port DRP implementation

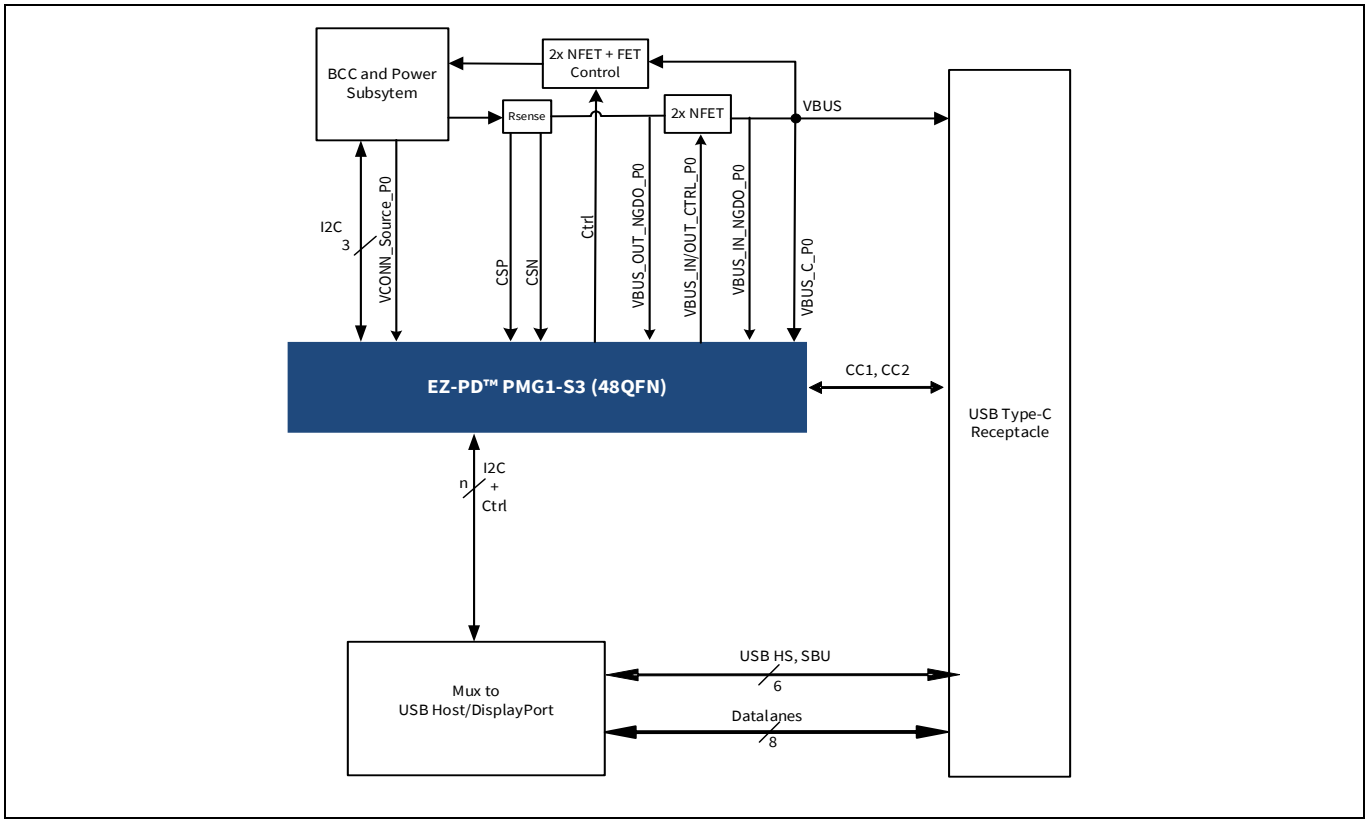

Figure 21 Single-port Type-C design using PMG1-S3 (48-QFN)

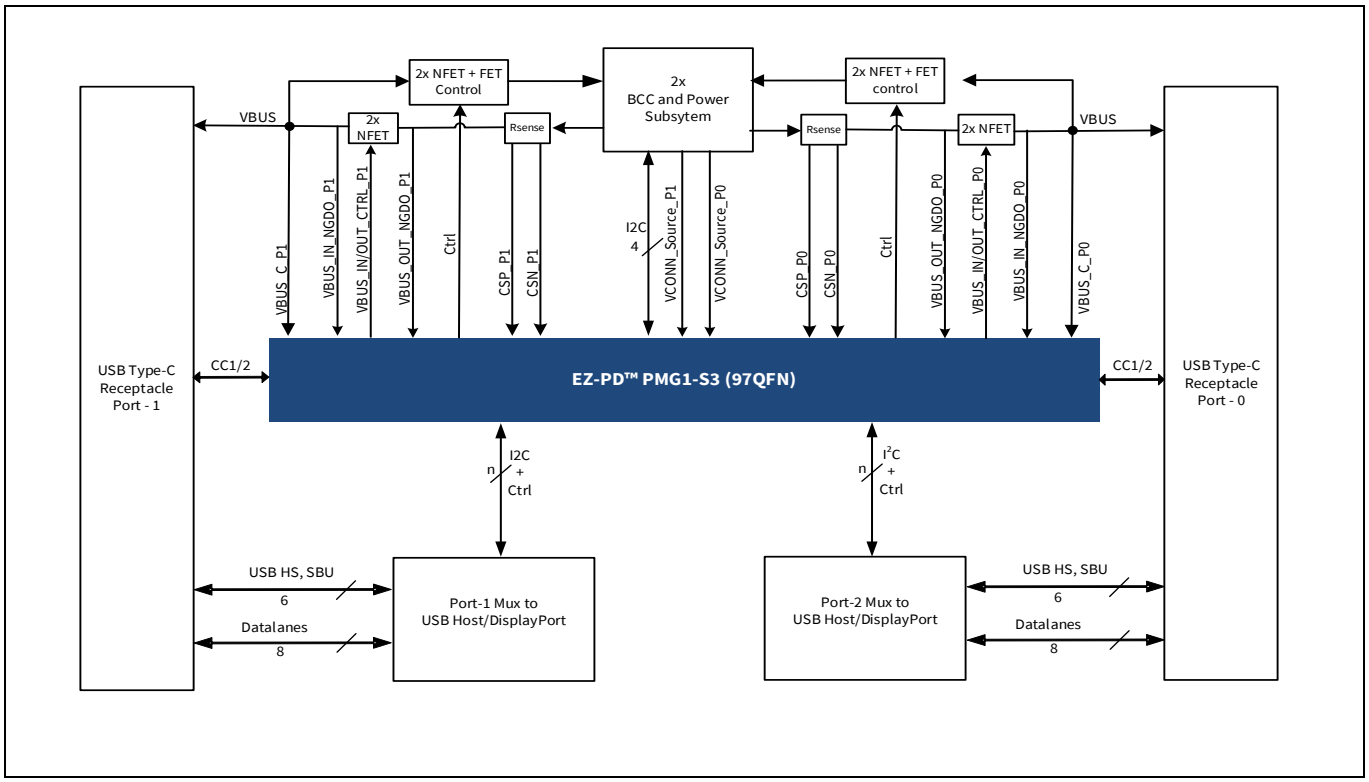

Figure 22 Dual-port Type-C design using PMG1-S3 (97-BGA)

5.3 System power supply design

The PMG1-S3 DRP design reference schematic design uses the MP4247 buck-boost DC-DC converter from Monolithic Power Systems as a variable-output VBUS source of up to 28 V. The voltage output of the regulator can be controlled using the I^2C interface.

The design reference also consists of two step-down regulators to generate the 5 V and 3.3 V outputs to provide for VCONN and PMG1-S3 system power.

The PMG1-S3 MCU operates with two possible external supply voltages: VBUS or VSYS. The VDDIO supply powers the device I/Os as listed in **Table 7**. VDDD generates 3.3 V from an internal regulator, and this can be shorted to VDDIO. VCCD is the output voltage from the core regulator, and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. PMG1-S3 has power supply inputs at the VCONN_Source_P0/P1 pins for providing power to EMCA cables through integrated VCONN FETs.

Table 7 PMG1-S3 operating voltage

Parameter	Minimum (V)	Maximum (V)
VBUS	4.0	30
VSYS	3	5.5
VDDD	2.9	5.5
VDDIO	1.71	VDDD
VCONN_Source	4.85	5.5

5.4 Power provider and consumer circuits

This section explains the recommended external hardware circuitry for VBUS control, OVP, OCP, RCP and SCP in a DRP design.

A DRP design using a PMG1-S3 device will be a power provider when running from its internal battery, and a power consumer when being charged from the connected power sources, such as power adapters and monitors.

5.4.1 Control of VBUS provider path and VBUS consumer path

PMG1-S3 consists of gate drivers and four pins for each port, namely VBUS_IN_CTRL_P0/1, VBUS_OUT_CTRL_P0/1 for NFET control and VBUS_IN_NGDO_P0/1, VBUST_OUT_NGDO_P0/1 with charge pump output to drive the NFET in the provider path.

Figure 23 shows the recommended implementation of FETs to control this VBUS path.

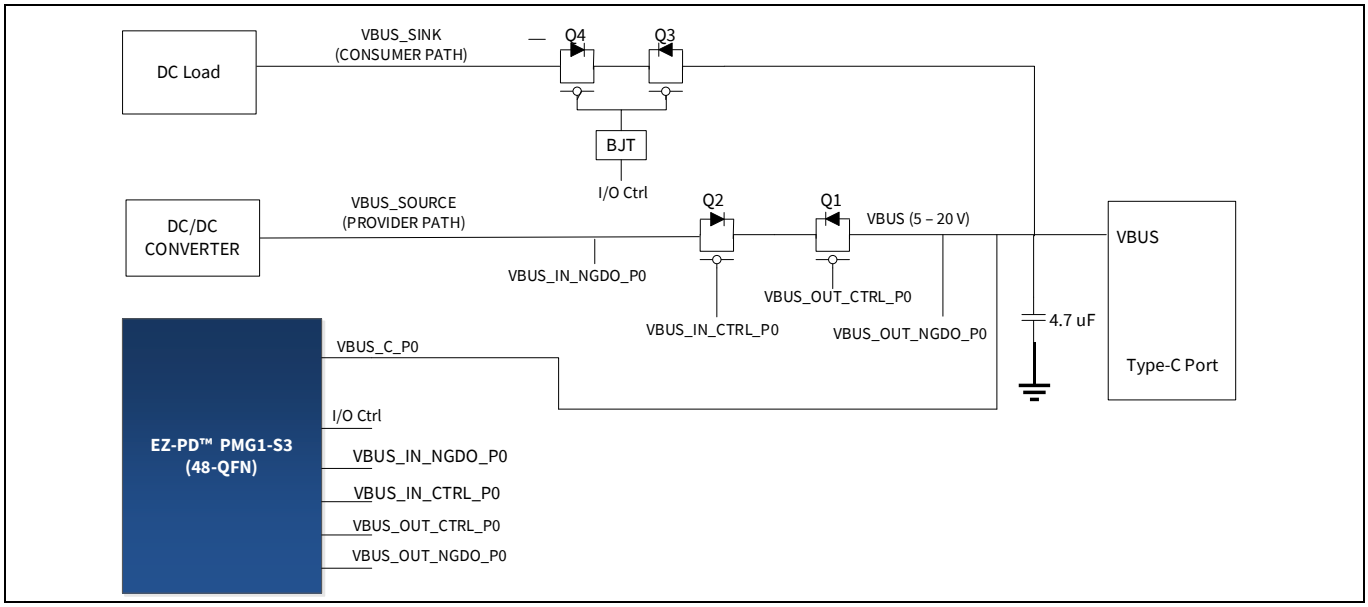

Figure 23 PMG1-S3 VBUS provider and consumer path control

5.4.2 Control of VBUS discharge path

Depending on the connected downstream device, the VBUS voltage varies, as illustrated by the following example scenarios:

- **Example scenario 1:** A UFP device sinking 140 W of power (28 V, 5 A) is disconnected from the Type-C port, and immediately another UFP device sinking 25 W of power (5 V, 5 A) is connected to the same Type-C port.
- **Example scenario 2:** An externally powered dock changes its power role from provider (sourcing 140 W of power) to consumer (sinking 45 W of power).

In both the scenarios, the VBUS capacitor shown in **Figure 23** may not have discharged fully from the original 20 V when the device is disconnected or the power role is changed to a lower voltage.

To prevent these scenarios, PMG1-S3 contains a VBUS discharge block, which has a 40 V drain extended NFET connected from VBUS supply to ground. The discharge strength can be changed by the firmware.

5.4.3 UVP/OVP for VBUS

PMG1-S3 includes integrated UVP/OVP circuits to sense UV and OV conditions on VBUS. Note that in the EZ-PD™ PMG1-S3 MCU 48-QFN package MCU, only Port-0 and, therefore, only one set of UVP/OVP, is available. The threshold levels for UV and OV detection can be programmed independently in 10 mV steps within the range of 200 mV to 2.1 V.

The UV and OV conditions are detected with the help of comparators placed on the VBUS divided by a series of resistors and the threshold level from the reference generator block. The resistor divider network can be set to select the VBUS level of 100 percent, 20 percent, 10 percent or 8 percent using the firmware control.

5.4.4 OCP/SCP/RCP for VBUS

PMG1-S3 includes integrated OCP/SCP/RCP circuits to sense the current fault conditions on VBUS. Consider a scenario in which the USB dock and the UFP device connected to its Type-C port establish the power contract, and the dock starts providing 5 A of VBUS current to the UFP. Once the power contract is established for 5 A of VBUS, the PMG1-S3 device's firmware configures the OCP trip current, which can be set by the firmware on the basis of negotiated VBUS current. If the VBUS current exceeds the OCP trip current (for example, due to a hardware fault in the UFP device), PMG1-S3 detects the OC condition at VBUS and turns off VBUS by turning off the gate drivers to turn off the power provider FETs Q1 and Q2. Similarly, the protection is activated if a SC condition arises or RC is detected on the VBUS path.

The CSN and CSP pins are the OC sensor input pins to PMG1-S3. These pins are connected to the CS resistor in series with the VBUS provider path, as shown in **Figure 24**.

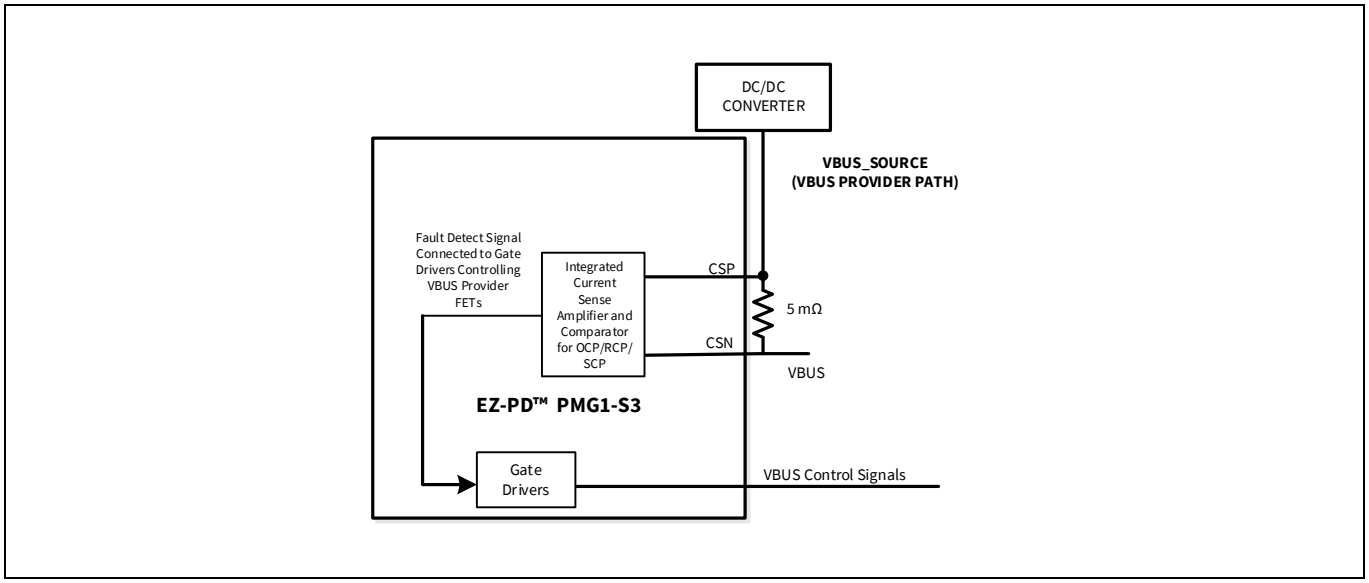

Figure 24 OCP/RCP/SCP circuitry in PMG1-S3

5.4.5 OCP for VCONN

In a DRP system design, VCONN supplies power to the EMCA attached to it. An OCP circuit is required on VCONN to prevent damage to the system when the VCONN power exceeds 1.5 W. As shown in **Figure 25**, PMG1-S3 has a built-in VCONN OCP circuit, and therefore, no external circuitry is required to implement OCP for VCONN in a DRP design using PMG1-S3.

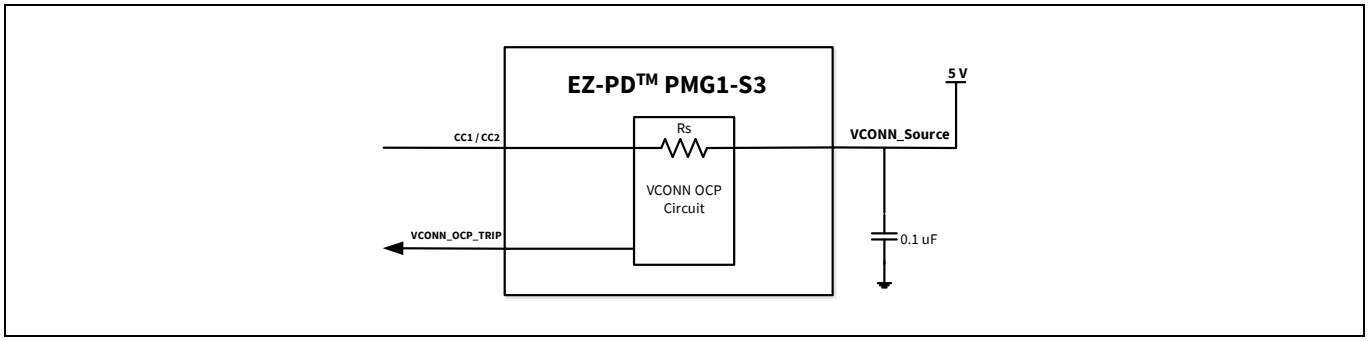

Figure 25 VCONN OCP for PMG1-S3

5.5 Type-C alternate mode implementation

The PMG1-S3 DRP schematic design provided with this application note consists of the DisplayPort alternate mode multiplexer included. The design in PMG1-S3 uses PI3DPX1205A from Pericom. The alternate mode implementation is application-specific, and the users can decide to not include the DisplayPort mux schematics in the end application.

Figure 26 shows the alternate mode implementation for PMG1-S3 single-port DRP design schematics.

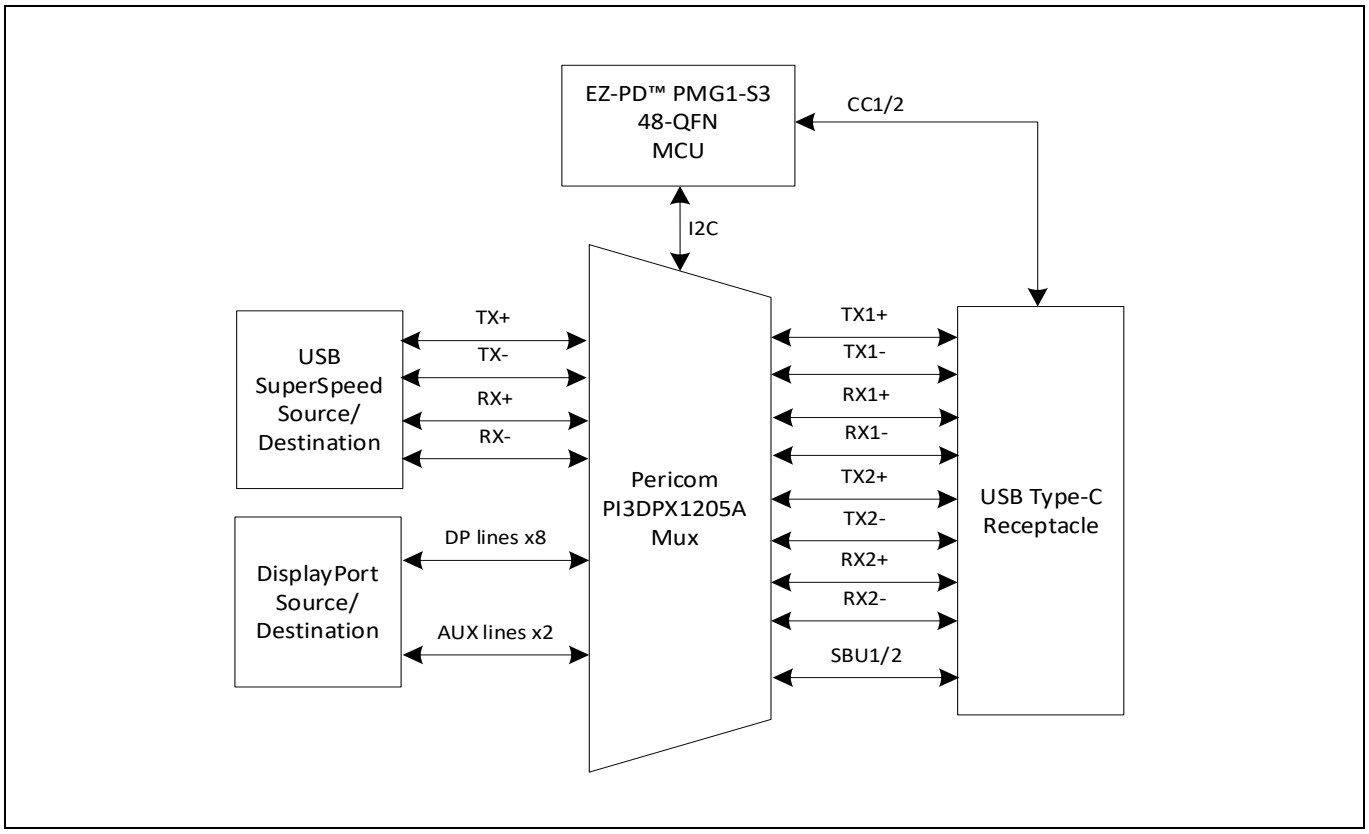

Figure 26 USB Type-C DisplayPort alternate mode for PMG1-S3 48-QFN

Note: PMG1-S3 97-BGA contains a set of analog switches to connect the SBU1 and SBU2 pins of the Type-C connector to AUX of a DisplayPort or LSx of Thunderbolt and UART debug pins. AUX pins are provided with switchable pull-up and pull-down resistors as required by their respective specifications. The LSTX/RX debug ports are muxed digitally, and no analog mux is required for these inputs. For more details on SBU mux on PMG1-S3 97-BGA, refer to the device datasheet.

Attachments

- PMG1-S1 DRP design reference schematics (DSN and PDF)
- PMG1-S1 DRP design reference bill of materials
- PMG1-S2 DRP design reference schematics (DSN and PDF)
- PMG1-S2 DRP design reference bill of materials
- PMG1-S3 single-port DRP design reference schematics (DSN and PDF)
- PMG1-S3 single-port DRP design reference bill of materials
- PMG1-S3 dual-port DRP design reference schematics (DSN and PDF)
- PMG1-S3 dual-port DRP design reference bill of materials

Revision history

Document revision	Date	Description of changes
**	2022-06-21	Initial release.
*A	2022-09-12	Template update. Updated Figure 1, Figure 3, and Figure 14.

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