DMA
Direct Memory Access
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**Key Features**
- Flexible DMA channels requests
- DMA double buffering
- DMA linked list

**Highlights**
- The DMA moves data from source locations to destination locations without the intervention of the CPU or other on chip devices.
- Up to 128 individually programmable DMA channels

**Customer Benefits**
- Possible configuration of the request type (SW, HW, Auto, ..) per DMA channel
- Transfer continuous data stream to two destination buffers
- Perform multi DMA transactions from non contiguous Memory regions
The DMA Channel supports the following types of requests:

- **DMA Software Request**: initiated by CPU
- **DMA Hardware Request**: any peripheral that can trigger an interrupt can initiate a DMA transaction through the Interrupt Router
- **DMA Daisy Chain Request**: DMA transaction initiated by the next higher priority DMA channel
- **DMA Auto Start Request**: initiated by the loading of the next Transaction Control Set (TCS) during a DMA Linked List operation
DMA
DMA double buffering

- Double buffering could be selected for source or destination buffering
- The application is able to freeze one of the destination buffers for cyclic software tasks while the other buffer continues to be filled
DMA
DMA linked list

- A linked list operation consists of a series of DMA transactions executed by the same DMA channel. Each DMA transaction has an unique configuration Set

- If the Auto start request is selected, a DMA transaction will be triggered after the end of the previous one in the list → no HW or SW trigger is needed

- DMA linked lists are useful when user wants to transfer data from/to non contiguous memory locations using one DMA channel and/or one service request
The DMA is connected to both SRI and SPB with master interfaces.

This enables the DMA to read and write data from/to any module.
In this example, data is transferred from the ADC output registers to internal memory without any CPU intervention.

1. End of ADC conversion interrupt
2. Trigger a DMA channel transfer
3. Read ADC result register
4. Write data to RAM
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