Triac Dimmable non-isolated Flyback converter using the IRS2982S controller IRXLED06

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About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IRXLED06 dimmable LED driver evaluation board based on the IRS2982S. The scope describes the operation of LED drivers with triac based phase cut dimmers and covers technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases. Test results and waveforms are included.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction

The IRS2982S is a versatile LED driver IC primarily intended for LED drivers in the 5 to 80 W power ranges suitable for Buck, Buck-Boost and Flyback converters operating in critical conduction mode (CrCM) at typical loads and discontinuous mode (DCM) at light loads. Flyback converters will be covered in this application note focusing on a current regulated design with high power factor for driving an LED load.

All of the control and protection required for the converter is integrated in the IRS2982S as well as a high voltage start-up cell to enable rapid illumination at switch on over a wide line input voltage range. The IRS2982S is also able to provide power factor correction in a single stage Flyback converter able to meet class C (lighting) line current harmonic limits of the EN61000-3-2 standard.

A 24W non-isolated current regulated PFC Flyback evaluation board based on the IRS2982S controller is described in detail in this application note and detailed test results are presented.

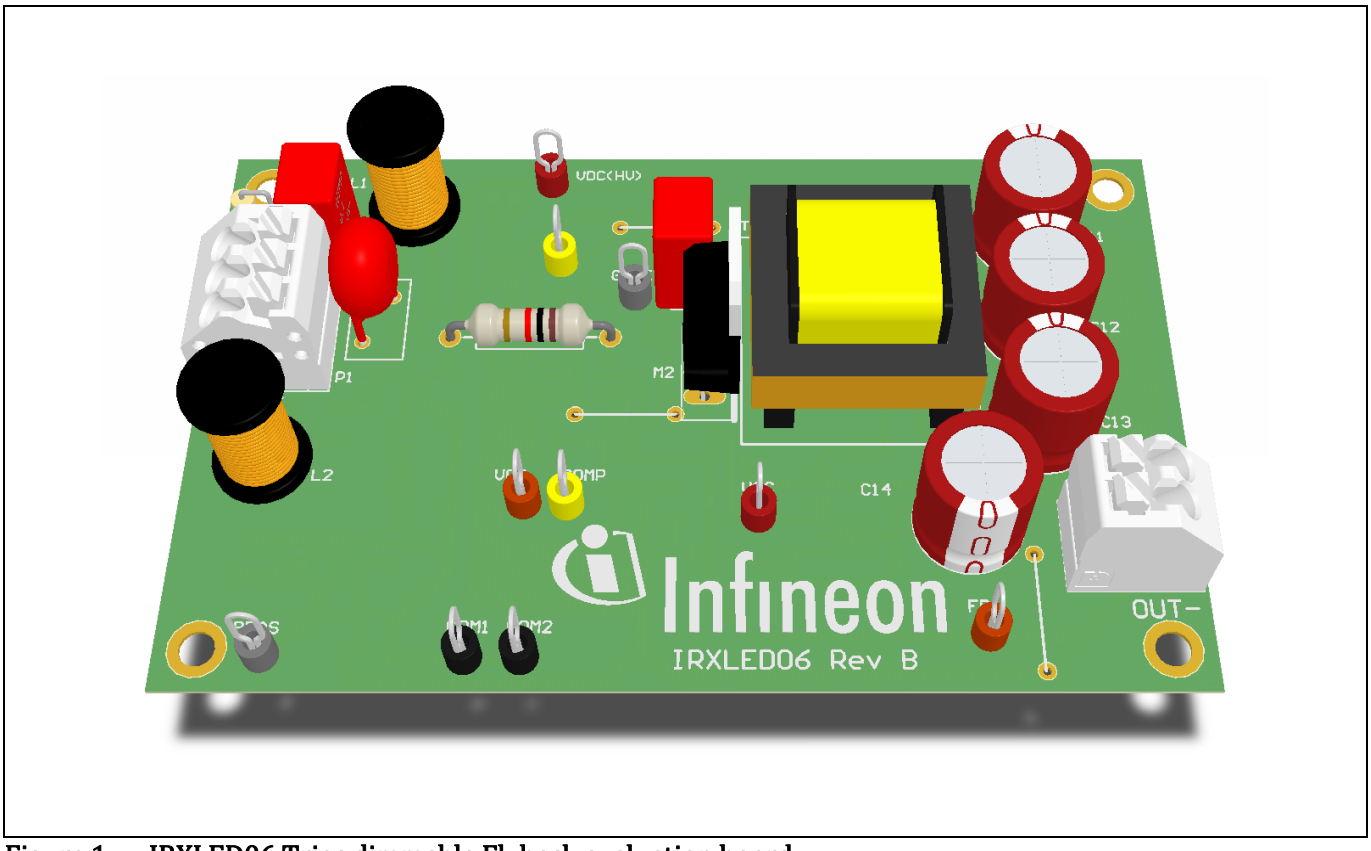


Figure 1 IRXLED06 Triac dimmable Flyback evaluation board

2 IRS2982S functional overview

The IRS2982S is comprised of the following functional blocks:

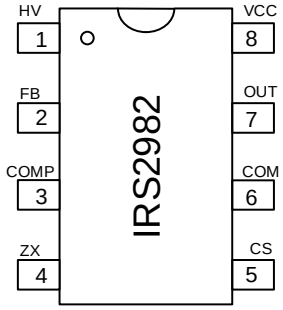
1. *High voltage start-up cell*
   The IC internal functional blocks remain disabled in low power mode until VCC first rises above the V_{CCUV+} under-voltage lock out (UVLO) threshold, continuing to operate while VCC remains above V_{CCUV-}. VCC is initially supplied through the integrated high-voltage start-up cell, which supplies a controlled current from the HV input provided a voltage greater than V_{HVSMIN}, is present. The current supplied is limited to I_{HV_CHARGE} reducing to less than I_{HVS_OFF} when VCC reaches the cut-off threshold V_{HVS_OFF1}. The HV start-up cell switches over from *start-up mode* to *support mode* after the feedback input at FB has exceeded V_{REG} for the first time. In this mode the cut-off threshold becomes V_{HVS_OFF2}. During steady state operation under all line-load conditions VCC is supplied through an auxiliary winding on the Flyback transformer with VCC high enough so that the HV start-up in does not supply current. If the auxiliary supply were unable to maintain VCC, the HV start-up cell operating in support mode would supply current to assist.

2. *PWM controller*
   The SMPS control section operates in voltage mode where the gate drive output on time is proportional to the error amplifier output voltage appearing at the compensation output COMP. An external capacitor CCOMP (shown in figure 3) connected to 0 V (ground) acts with the trans-conductance characteristic of the error amplifier to provide loop compensation and stability. Minimum on time is reached when V_{COMP} falls to $V_{COMPOFF}$ below which the gate drive is disabled. Under very light load conditions V_{COMP} transitions above and below $V_{COMPOFF}$ to produce burst mode operation. Off time is determined by the demagnetization signal received at the ZX input, which is derived from the auxiliary transformer winding that supplies VCC through a resistor divider. Internal logic limits the minimum off time to t_{OFFMIN}, therefore the system transitions from CrCM to DCM at light loads. If the ZX input signal fails to provide triggering the next cycle will start automatically after a re-start period of t_{WD}.

3. *Protection*
   The IRS2982S includes cycle by cycle primary over-current protection, which causes the gate drive to switch off if the voltage detected at the CS exceeds the threshold V_{CSTH}. This prevents the possibility of transformer saturation at low line under heavy load but does not protect against output overload or short circuit.

Over-voltage protection is also provided through the ZX input, which provides a voltage proportional to the output voltage. This disables the gate drive output and pulls the COMP voltage below the $V_{COMPOFF}$ threshold. The error amplifier then starts to charge CCOMP until the gate drive starts up again at minimum on time. Under an open circuit output condition the over voltage protection causes the converter to operate in burst mode preventing the output voltage from rising too high.

The IRS2982S uses an SO-8 package as shown below:



Pin	Name	Description
1	*HV*	High Voltage Start-up Input
2	*FB*	Feedback Input
3	*COMP*	Compensation and averaging capacitor input
4	*ZX*	Zero-Crossing & Over-Voltage Detection input
5	*CS*	Current Sensing Input
6	*COM*	IC Power & Signal Ground
7	*OUT*	Gate Driver Output
8	*VCC*	Logic & Low-Side Gate Driver Supply

Figure 2 IRS2982S pin assignments

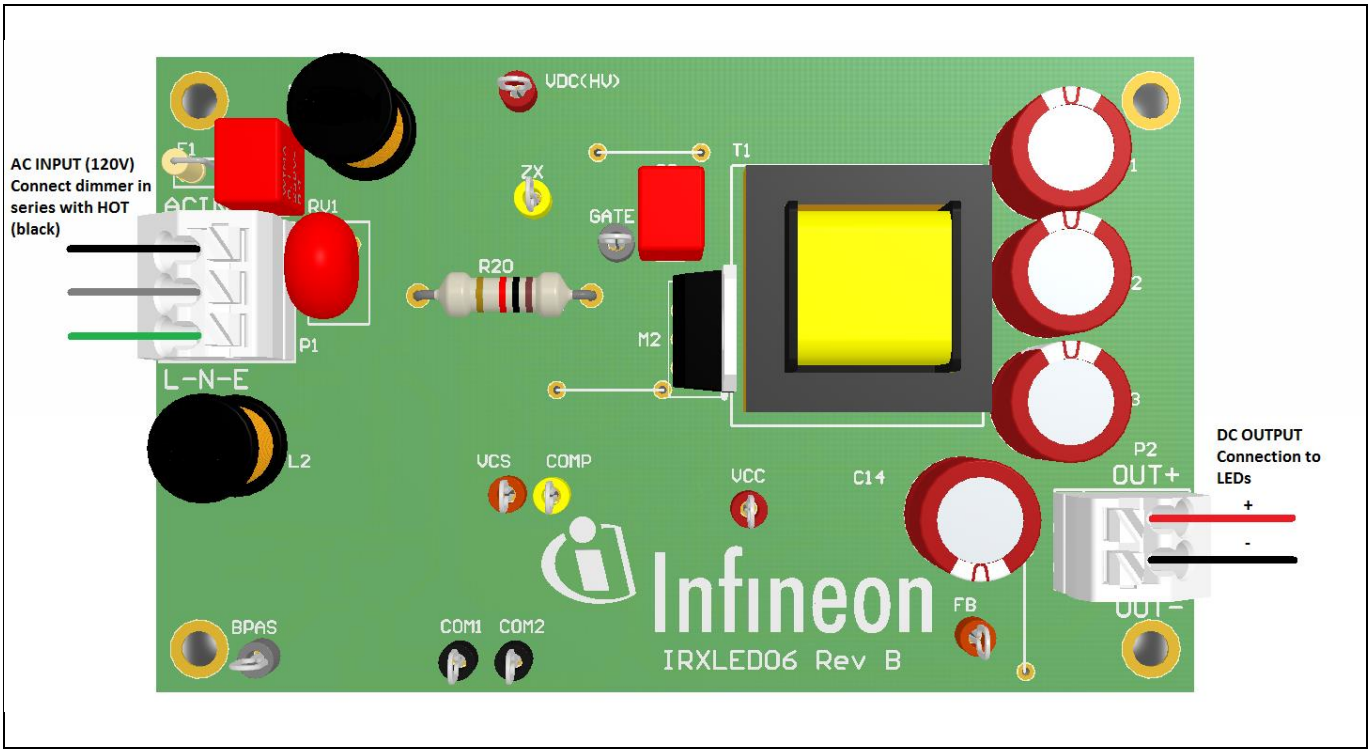


Figure 3 IRXLED06 Connection Diagram

3 Flyback converter

3.1 Flyback converter types

There are several configurations of Flyback converter that may be used with the IRS2982S depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated,
2. Current or voltage regulation,
   In the case of voltage regulation current limiting is needed for protection against overload or short circuit and in the case of current regulation over-voltage protection is necessary for an open-circuit.

The IRS2982S can operate in any of the four combinations of (1) and (2). Extremely accurate current or voltage regulation is achieved in non-isolated converters since direct feedback to the FB input is possible. Isolation is however required in the majority of Flyback converters. For isolated constant current regulation an opto-isolator is necessary; for isolated constant voltage regulation feedback may be taken from an auxiliary winding with a small loss of line and load regulation accuracy. An opto-isolator is also necessary for highly accurate voltage regulation.

The basic circuit in figure 4 shows the main elements of the IRS2982S based non-isolated constant current regulated PFC Flyback converter. In this example the IRS2982S VCC supply is derived from the output of the converter therefore no auxiliary transformer winding is needed. This arrangement may be used providing the LED output voltage always remains above 20V and that it does not exceed 60V where the VCC supply circuit based around QVCC would dissipate excessive power. An auxiliary winding is required for LED voltages outside this range.

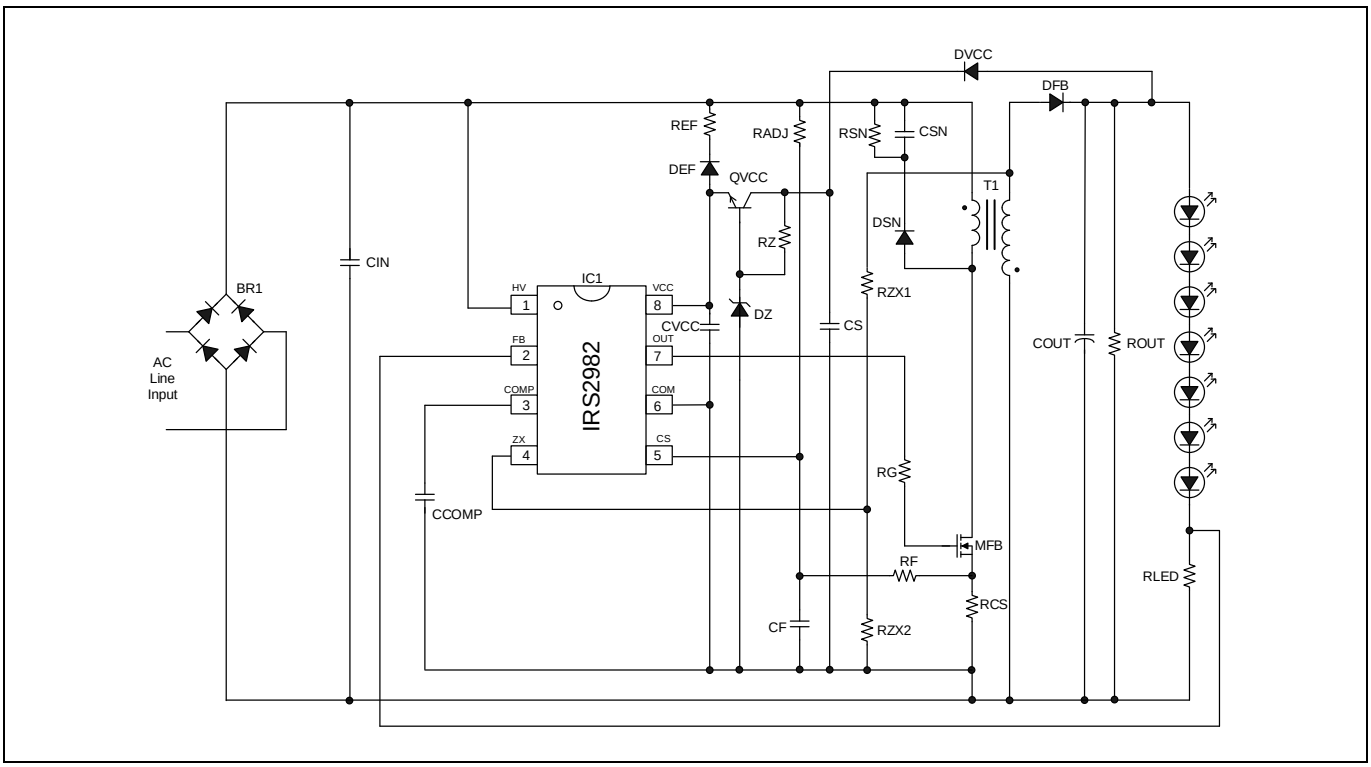


Figure 4 Non-isolated current regulated Flyback converter based on the IRS2982S

A triac dimmable PFC Flyback voltage regulated design as implemented in the IRXLED06 evaluation board will be discussed in detail in the following sections.

3.2 Eval board specifications

Input and output at normal operation:

- AC Input voltage 90 VAC up to 132 VAC (55 to 65 Hz)
- Output voltage 24 to 48 VDC
- Output average current 500mA +/- 1%
- Maximum output current ripple 30%
- Maximum output continuous power 24 W
- PF >0.95 at maximum load, 90 to 132 VAC input voltage
- THD <10% at maximum load, 90 to 132 VAC input voltage
- Efficiency >80% at maximum load at 120 VAC input voltage.
- Startup time to reach the secondary nominal output voltage during full load condition and 120 VAC input voltage <300 ms with no dimmer connected.
- Maximum flicker 30% (including ripple at 2 x line frequency)

Protection features

- Primary output over-voltage protection @ VOUT <= 60 VDC
- Cycle by cycle primary over-current protection

WARNING!
Output is not isolated! Risk of electric shock! Not designed for hot re-connect!

No load operation

- Burst mode during no load condition.
- Max power losses during no load condition must be <500mW @120VAC input voltage

Max component temperature
During worst case scenario (ambient temperature 60 °C) the max allowed component temperature is:

- Resistor < 105 °C
- Ceramic capacity, film capacity and electrolyte capacity <85 °C
- Flyback Transformer and chokes <105 °C
- MOSFET, transistor and diodes <105 °C
- IC <100 °C

Dimensions of evaluation board

- Max width 2.2” (55.9 mm), max length 3.3” (83.8 mm).

WARNING!
Output is not isolated! Risk of electric shock! The board should be used only by qualified engineers and technicians.

4 Schematic

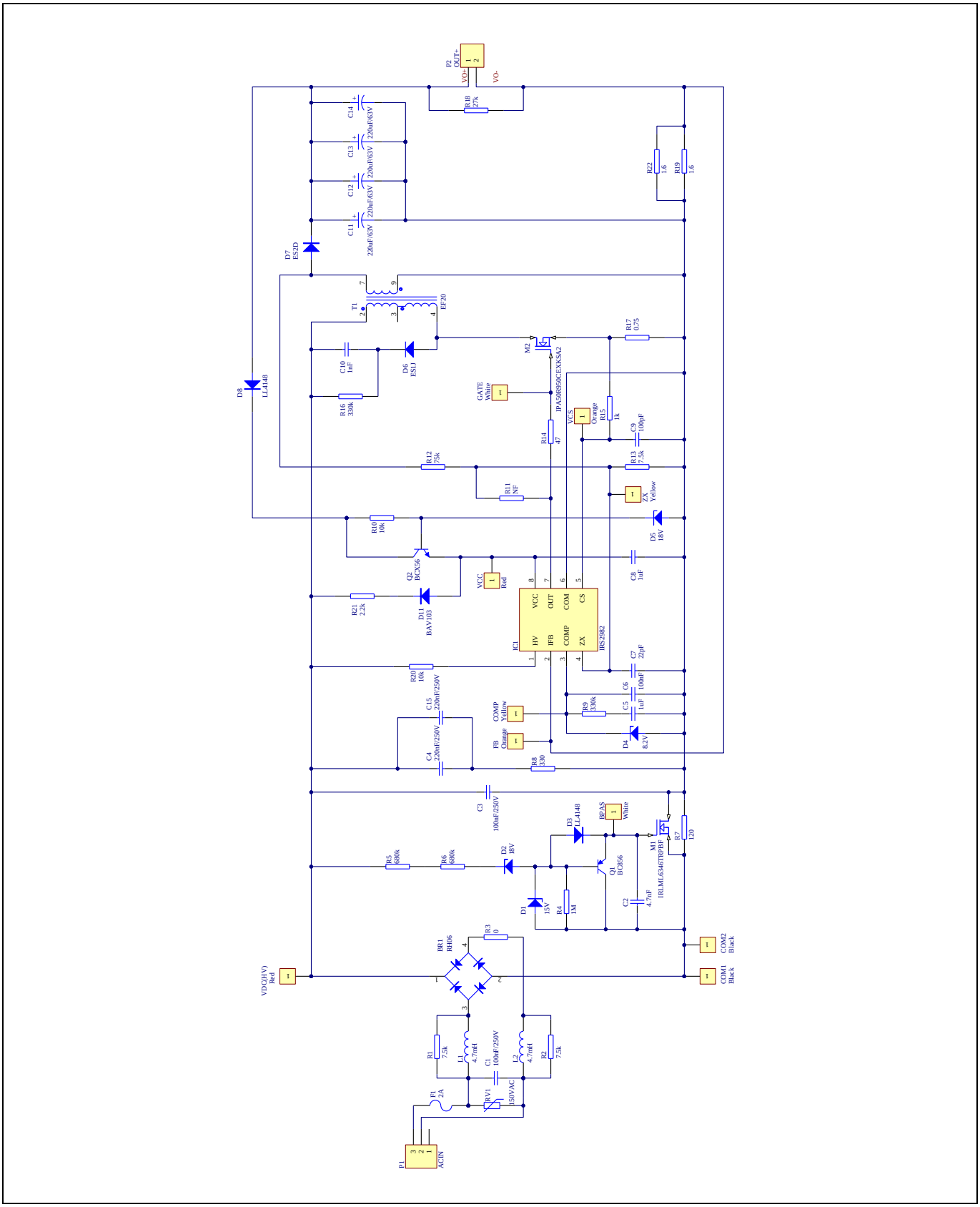


Figure 5 IRXLED06 24 W Triac Dimmable PFC Flyback schematic

5 Dimensioning

The IRXLED06 evaluation board is designed for constant current regulation using direct feedback from shunt resistor RLED (R19 and R22 in parallel) as shown in figures 4 and 5.
The Flyback converter is designed for power factor correction with low AC line current total harmonic distortion (iTHD).

5.1 MOSFET selection

The MOSFET used is an IPA50R950CEXKSA2 500 V rated CoolMOS device with 950 mΩ on resistance, 10.5 nC gate charge and very low parasitic capacitances in an TO-220 FullPAK. A standard TO-220 package may also be used. This device is able to withstand high voltage ringing at switch off for a converter supplied in the 120VAC range only, with minimal added snubber components and has low conduction and switching losses as well low gate drive current.
The TO-220 FullPAK has 80°C per Watt temperature rise with no heatsink connected. Referring to the thermal image in figure 28, it can be seen that the steady state operating temperature of M2 is 57°C in open air at 25°C ambient. This 32°C rise is a result of conduction and switching losses. The selection of this MOSFET would allow for use in a higher ambient inside an enclosure and still maintain the temperature below 105° as stipulated in section 3.2. DPAK or IPAK packaged devices are possible alternatives, however these possess a higher junction to ambient thermal resistance resulting in higher temperature rise with an equivalent device. Such devices are likely to operate at excessive temperature in applications above 15W. At higher power levels lower $R_{DS(ON)}$ values should be used TO-220 standard or FullPAK devices may be used with heat sinks added where necessary.

The output diode ES2D-13-F (SMB package) has typically 25 ns reverse recovery and a forward voltage drop less than 920m V at maximum rated current of 2 A at 25 °C temperature. The blocking voltage is 200 V, necessary to withstand the output voltage under open circuit condition at maximum line input added to the transformer secondary reflected voltage.
The parameters of the MOSFET and output diode contribute to the overall high efficiency of the converter. The Flyback transformer (more accurately described as a coupled inductor) consists of two windings; the primary for energy storage during the on time, the secondary for energy transfer to the output during the off time, which also supplies VCC and provides the required de-magnetization and voltage feedback signals. The IRS2982S (IC1) VCC supply is derived from the output through DVCC (D8) through a series transistor QVCC (Q2), which clamps the voltage according to DZ (D5) to protect IC1 from over-voltage at VCC. Current feedback is provided through RLED (R19 and R22 in parallel), which sets the output current.
Switching cycle peak current limiting is set by shunt resistor RCS (R17), which is set to 1.0 Ω, setting the peak current to 1.2 A according to the threshold VCSTH of 1.2 V. This limits the inrush current during start-up. The maximum peak current at low line and full load, assuming DMAX is 0.4[1] is calculated as:

$$I_{PMAX} = \frac{2\sqrt{2}\cdot POUT}{D_{MAX}.VAC_{MIN}\cdot\eta} = \frac{2\sqrt{2}\cdot 20}{0.4\cdot 100\cdot 0.85} = 1.66 \quad [A] \quad [1]$$

The transformer turns-ratio is calculated as follows:

$$N = \frac{N_P}{N_S} = \frac{\sqrt{2}\cdot VAC_{MIN}}{V_{OUT}+V_F}\cdot\frac{D_{MAX}}{1-D_{MAX}} = \frac{\sqrt{2}\cdot 100}{40+1}\cdot\frac{0.4}{1-0.4} = 2.3 \quad [2]$$

[1] The value of maximum duty cycle was chosen so that an off the shelf Flyback transformer could be used. In practice this value could be up to 0.6, which would reduce the peak current.

Dimensioning

The transformer primary inductance is calculated according to the formula:

$$L_{PRI} = \frac{VAC_{MIN}^2 \cdot \eta \cdot N \cdot (V_{OUT}+V_F)}{2 \cdot P_{OUT} \cdot f_{MIN} \cdot [N \cdot (V_{OUT}+V_F)+\sqrt{2} \cdot VAC_{MIN}]} \quad [H] \quad [3]$$

$$\frac{100^2 \cdot 0.85 \cdot 2.3 \cdot (40+1)}{2 \cdot 20 \cdot 100000 \cdot [2.3 \cdot (40+1)+\sqrt{2} \cdot 100]} = 850 \cdot 10^{-6}\ \text{H} = 850 \quad [\mu H]$$

Where, η is the efficiency assumed to be 0.85 and minimum frequency set to 100 kHz[1] to occur at the peak of the line input voltage at 100 Vrms.
The output current sense resistor RLED is calculated as follows:

$$R_{LED} = \frac{V_{REF}}{I_{LED}} \quad [\Omega] \quad [4]$$

$$\frac{0.4}{0.5} = 0.8 \quad [\Omega]$$

The threshold for over voltage protection through the ZX input is given by the resistor divider consisting of RZX1 and RZX2, where RZX1=68 k and RZX2=8.2 k and V_{OVTH} is 5.1 V:

$$V_{OUTOV} = V_{OVTH} \cdot \frac{RZX1+RZX2}{RZX2} \quad [V] \quad [5]$$

$$5.1 \cdot \frac{68k+8.2k}{8.2k} = 47.4 \quad [V]$$

The maximum reflected voltage appearing at the MOSFET drain is then calculated as follows based on the highest AC line input voltage of 132 Vac:

$$V_{DMAX} = \sqrt{2} \cdot V_{ACMAX} + (V_{OUT(MAX)} + V_F) \cdot N \quad [V] \quad [6]$$

$$\sqrt{2} \cdot 132 + (40+1) \cdot 2.3 = 298 \quad [V]$$

It is recommended to allow 30% headroom on top of the reflected voltage to accommodate the switch off transient and high voltage ringing. This requires a MOSFET with a minimum drain-source maximum rating of 765 V and therefore an 800 V part has been selected.
Four parallel 220 µF output capacitors COUT (C11 to C14) have been used with a total capacitance of 880 µF, combined ripple current rating of 3.4 A and impedance of 30 mΩ at 100 kHz. The maximum low frequency output ripple can be calculated as follows:

$$V_{RIPPLE} = \frac{I_{OUT}}{2 \cdot \pi \cdot f_{ac(\min)} \cdot C_{OUT}} \quad [Vpp] \quad [7]$$

$$\frac{0.5}{2 \cdot \pi \cdot 55 \cdot 880 \cdot 10^{-6}} = 1.64 \quad [Vpp]$$

$$C_{OUT} = \frac{I_{OUT}}{2 \cdot \pi \cdot f_{ac(\min)} \cdot V_{RIPPLE}} \quad [F] \quad [8]$$

[1] The value of minimum frequency has been chosen to minimize transformer cost. A lower frequency could be chosen, which would require a higher primary inductance.

6 Dimming with triac based dimmers

6.1 Triac dimmer basics

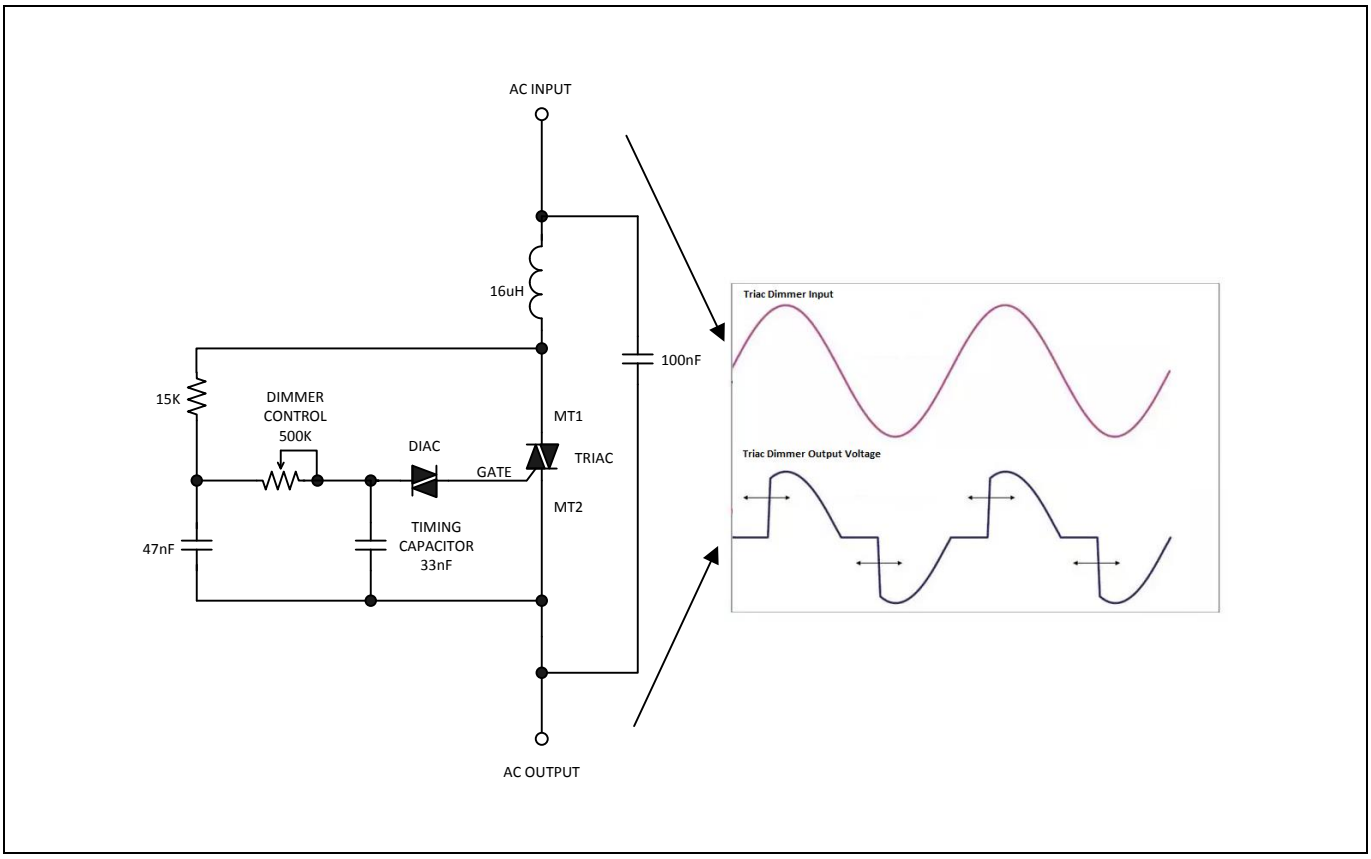


Figure 6 Triac based dimmer basic schematic and waveforms

Before the introduction of LED lighting, virtually all residential and professional dimming systems used *triac* based circuits. The triac is a bi-directional SCR type device that conducts only after having been *fired* by the application of a voltage pulse at the gate terminal. Conduction then continues between the two main terminals (MT1 and MT2) sometimes termed anodes, while the current magnitude remains in excess of the *holding current* of the device. These dimmers were designed in the 1960s to operate with *resistive* loads such as Tungsten filament incandescent light bulbs, which present a low resistance from the AC output terminal back to AC line neutral. During the period when the triac is not conducting almost all of the line voltage appears across the triac main terminals. This allows the voltage at the timing capacitor to rise at a rate depending on the setting of the dimmer control potentiometer until it reaches the threshold voltage of the diac (typically 32V). At this point the diac fires and the timing capacitor discharges through the triac gate causing the triac to fire. The diac is a two terminal break-over device similar to a triac but instead fired by a voltage threshold being exceeded between the terminals. The timing capacitor is discharged to a low voltage during the firing process. Current then flows in either direction depending on the polarity of the AC line cycle until it drops below the holding current, which happens as the line voltage approaches the zero crossing. The delay from the line zero crossing to the triac firing point determines the phase angle at which the triac fires such that the voltage appearing at the load is *phase cut* as shown in the waveform of figure 6. The RMS voltage of the phase cut waveform is reduced the larger the firing angle thereby adjusting the RMS current to provide excellent dimming performance for incandescent light bulbs.
Most dimmers include a series inductor and bypass capacitor to reduce EMI and protect the triac in the event of an inductive load being connected to the dimmer such as an Iron core mains frequency transformer.

6.2 Challenges driving LEDs with triac based dimmers

To obtain acceptable dimming performance, it is necessary to provide a load to the dimmer that will allow smooth and flicker free operation over the full dimming range. However, the standard triac based *leading edge* dimmer is not able to operate in a stable manner if connected to a capacitive load such as the input of an LED driver or other lighting ballast. A power factor corrected (PFC) Flyback LED driver can address the problem as it presents a load that appears effectively resistive with some capacitance due to the input EMI filter. The presence of EMI filtering components in the dimmer and in the LED driver are likely to create high voltage ringing oscillations caused by the high dv/dt that occurs when the triac fires. Such oscillations, if large enough, can cause the current to fall below the holding current of the triac making it switch off prematurely instead of conducting until the end of the line half-cycle. This is often made worse by the dimmer circuit re-firing the triac so that it switches on and off multiple times during a single line half-cycle, which apart from stressing the components and possibly damaging the dimmer or LED driver, creates visible flickering in the LEDs and introduces audible noise.

New generation dimmers are now available designed to operate with LED drivers such as electronic low voltage (ELV) dimmers, which operate with reverse phase control otherwise known as *trailing edge* dimmers. However, these are relatively expensive and so there remains a strong demand for LED lights that are compatible with existing triac based dimmers. For this reason circuitry is added to the LED driver to overcome the miss-firing problem previously described.

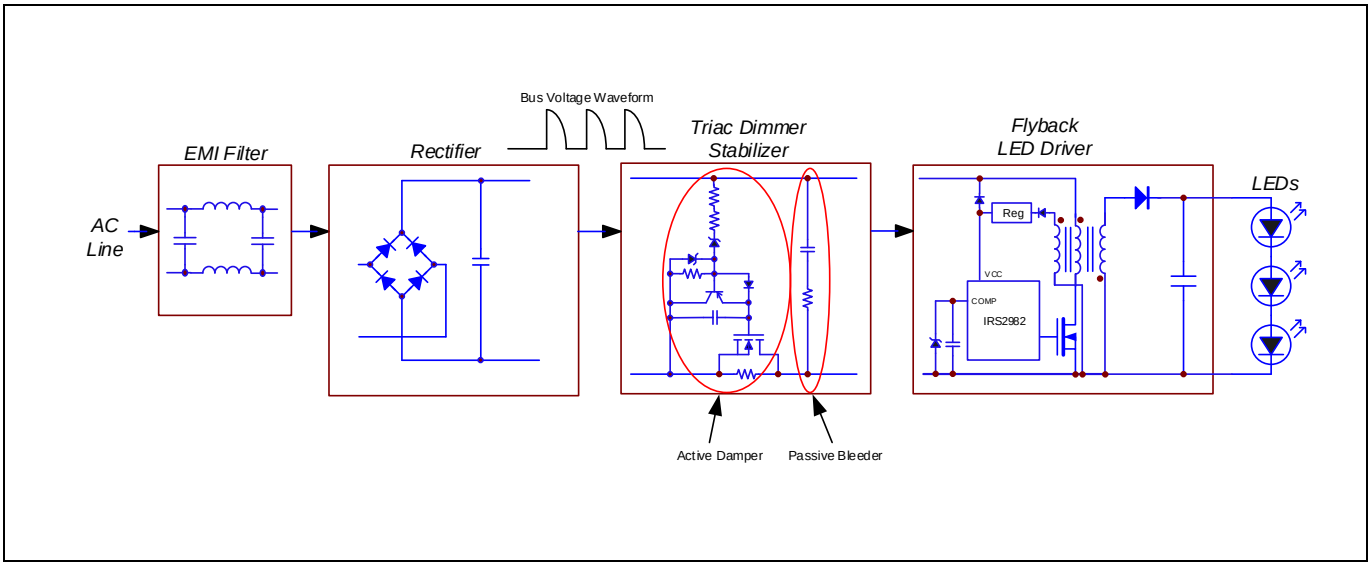


Figure 7 Dimmable PFC Flyback LED driver block diagram

It should be noted that is vital when designing the LED driver input filter to keep the input capacitance to a minimum. This also helps to optimize the power factor and harmonic distortion of the line current (iTHD). For dimmer compatibility, the active damper and passive bleeder circuits are added as shown in figure 7. The *damper* circuit limits the inrush current when the triac fires to reduce ringing and thereby avoid multiple firing and switching off. Shortly after the triac fires and the bus voltage transitions high, the damper resistor is bypassed by a small MOSFET to prevent power loss during the remaining conduction period. The active damper circuit has the added benefit of reducing audible noise, which is a major consideration in phase cut dimming applications.
To minimize cost in low power drivers (< 10W) the bypass MOSFET and its associated drive circuitry may be omitted so that damping relies only on the series resistance of the input filter inductors combined with series the resistor shown in the 0V return bus. Removing the active damper increases heat dissipation in the resistor causing some efficiency loss but this is often acceptable in low power LED lights.

The passive *bleeder* circuit is used to replace the active bleeder used in some dimming solutions, which are relatively expensive since they require high voltage MOSFETs. This series RC network shown in figure 7 conducts current beginning at the triac firing point for long enough to allow the switching converter to start up and begin to draw current. This helps to ensure that the current does not drop below the holding current during the period immediately after triac firing. The IRS2982S based PFC Flyback converter operating with constant on time appears as a predominantly resistive load to the DC bus, allowing conduction to occur through the dimmer's triac from the moment of firing until the next line zero crossing. It is essential that the converter draw sufficient current to remain above the triac holding current throughout the conduction period.
The circuits described do not affect the LED driver's ability to function with a trailing edge (ELV) dimmer.

6.3 Controlling the LED brightness

Operating in voltage mode CrCM the DC voltage level present at the IRS2982S COMP input determines the on time of the switching cycle. To enable high power factor the on time does not change significantly during the AC line half-cycle and requires several cycles to adjust to compensate for line or load changes. Since the IRS2982S is used with output current regulation, it becomes necessary to clamp the COMP voltage by adding a zener diode to this input to set a maximum limit for the on time. This means that during dimming as the firing angle is increased and the DC bus voltage is reduced, the on time is not able to increase to compensate and maintain full output current. The result is that as the dimmer level control is adjusted downwards and the DC bus voltage drops, the output current also reduces. This allows the light level to be smoothly and linearly dimmed to 10% output current or lower by adjusting the dimmer control. The IRS2982S requires no complex circuitry for detecting the dimmer phase angle and converting this to a reference to regulate the output.

6.4 Flicker elimination

When using the IRS2982S in this application is necessary to maintain a residual voltage at CIN during the period when the dimmer is off. With some dimmers this happens due to the current conduction through the triac bypass capacitor though this is not the case with all dimmers. The IRS2982S VCC supply is maintained continuously during dimming, therefore the gate drive continues to operate even during the non-conduction portion of the line half-cycle. This helps to maintain triac conduction by drawing a small current. However, if the bus voltage at CIN (C3) drops too low the ZX input no longer receives a voltage pulse to initiate the next switching cycle and therefore the restart timer is activated for the next switching periods. When this happens, the firing of the dimmer triac for the next line half-cycle can occur at any point during the t_{WD} restart timer interval. The result is an un-synchronized delay between triac firing and the first switching pulse that occurs after it. This delay varies between AC half-cycles introducing a small visible flicker. This is easily overcome by adding a series diode DEF (D11) and resistor REF (R21) so that the VCC voltage is transferred to CIN to maintain enough voltage to trigger ZX every cycle. This causes very short off periods during the dimmer non-conducting time so that there is very little variation in the firing to first switching pulse delay and therefore no flicker.

6.5 Shimmer effect

"Shimmer" refers to the amount of instability that may be seen in the light output while the LED light is operating at some set dimming level under steady state conditions. This is often more noticeable when the light is reflected from a surface. Since it is distracting to end users, LED driver manufacturers typically carry out a series of tests designed to ensure that an acceptable level of stability is achieved. Such tests are carried out using a photo sensor in a dark room, connected to an oscilloscope to measure the light level or more simply by observing the LED current with a DC current probe.

It is very important to be aware that changes in the AC line voltage caused by the switching on and off of heavy loads such as air conditioners and elevators are likely to cause small changes in light output, which are more visible at low dimming levels. This is unavoidable if the peak voltage and firing angle from the dimmer supplying the LED driver circuit that set the output current, change with a step change in the AC line voltage. Shimmer tests are therefore only valid if carried out using a stabilized AC source. A test of light output change as a response to line input voltage disturbances would be a different test.

6.6 Audible noise

End users are often very particular about audible buzzing produced by LED driver electronics while being dimmed with phase cut dimmers. Stringent tests are carried out by driver manufacturers to determine whether excessive audible noise is produced. Typically no buzzing should be heard from a distance of 3 feet or one meter (or metre).

A necessary and important part of the driver design process is therefore to reduce audible noise as much as possible and this must be tackled from an electronic and mechanical design perspective. Sound is mainly produced by the filter inductors and transformer resulting from high dv/dt that occurs at the firing point of the dimmer each AC line half-cycle. It is therefore important that the transformer cores and bobbin be glued together and that the drum core filter inductors be in a housing or covered by shrink rubber. Potting the driver is a widely used solution though some manufacturers prefer to avoid it.

Keeping the peak current I_{PMAX} to a minimum also helps to reduce noise (refer to section 5.1). However RCS must be low enough to prevent clipping of the AC line input current at full load and minimum input voltage.

As a final and very important point, the driver board assembly itself is often located inside a plastic housing where vibrations between hard surfaces can greatly amplify unwanted buzzing. If the product is not potted, sticky pads or glue should be used to create a buffer and damp out any such vibrations.

6.7 Start-up time

The IRS2982Ss integrated high voltage start-up cell enables the LED driver to light up the LED load very rapidly. In the majority of applications the VCC supply is derived from the output through a simple series regulator circuit. However during start up when VCC is supplied by the HV start-up cell, as VCC rises above approximately 5V, emitter to base conduction reverse breakdown occurs in QVCC (Q2) and the base to collector junction becomes forward biased. If the collector were to be connected directly to the converter output the large output capacitance would cause a significant delay in the rise time of VCC to the VCCUV+ threshold to start up the system. To eliminate this delay a series diode DVCC (D8) must be added.

7 Bill of materials

Designator	Manufacturer	Part Number	Quantity	Value/Rating
BPAS, GATE	Keystone	5002	2	0.04" dia white
BR1	Diodes Inc	RH06-T	1	600V/0.5A
C1	Panasonic	ECQ-E2104KB	1	100nF/250V
C2	TDK	C3216X7R2J472K115AA	1	4.7nF/630V/1206
C3	Panasonic	ECQ-E2104JB	1	100nF/250V
C4, C15	TDK	C3216X7T2E224K160AA	2	220nF/250V/1206
C5	TDK	C2012X7R1E105K125AB	1	1uF/25V/10%/0805
C6	TDK	C2012X7R1H104K085AA	1	100nF/50V/10%/0805
C7	Kemet	C0805C220J5GACTU	1	22pF/50V/5%/0805
C8	TDK	C3216X7R1E105K085AA	1	1uF/25V/10%/1206
C9	TDK	CGA4C2C0G2A101J060AA	1	100pF/100V/5%/0805
C10	TDK	C3216X7R2J102K115AA	1	1nF/630V/10%/1206
C11, C12, C13, C14	Nichicon	UPW1J221MPD	4	220uF/63V/105C/20%
COM1, COM2	Keystone	5001	2	0.04" dia black
COMP, ZX	Keystone	5004	2	0.04" dia yellow
D1	Micro Commercial	BZV55C8V2-TP	1	8.2V/500mW/SOD-80C
D2, D5	Micro Commercial	BZV55C18-TP	2	18V/500mW/SOD-80C
D3, D8	Diodes Inc	LL4148-13	2	75V/150mA/MINIMELF
D4	Micro Commercial	BZV55C8V2-TP	1	8.2V/500mW/MiniMelf
D6	Micro Commercial	ES1J-LTP	1	600V/1A/SMA
D7	Diodes Inc	ES2D-13-F	1	200V/2A/SMB

D11	Micro Commercial Co	BAV103-TP	1	200V/200mA/MINIMELF
F1	Littelfuse	0251002.NRT1L	1	FUSE BRD MNT 2A/125VAC/VDC
FB, VCS	Keystone	5003	2	0.04" dia orange
IC1	Infineon	IRS2982S	1	Flyback Controller IC
L1, L2	Murata Power Solutions	13R475C	2	4.7mH/0.16A
M1	Infineon	IRLML6346TRPBF	1	MOSFET N-CH 30V 3.4A SOT23
M2	Infineon	IPA50R950CEXKSA2	1	500V/950mOhms/TO-220 FP
P1	Phoenix Contact	1985205	1	3 Position 3.5mm Green
P2	Phoenix Contact	1985195	1	2 Position 3.5mm Green
Q1	Diodes Inc	BC856B-7-F	1	PNP/65V/0.1A/SOT-23
Q2	Infineon	BCX56E6327HTSA1	1	NPN/80V/1A/SOT-89
R1, R2	Panasonic	ERJ-6GEYJ752V	2	7.5k/0.125W/5%/0805
R3	Panasonic	ERJ-8GEY0R00V	1	0/0.25W/1206
R4	Panasonic	ERJ-8GEYJ105V	1	1M/0.25W/5%/1206
R5, R6	Panasonic	ERJ-6GEYJ684V	2	680K/0.25W/5%/0805
R7	Panasonic	ERJ-8GEYJ121V	1	120/0.25W/5%/1206
R8	Panasonic	ERJ-8GEYJ331V	1	330/0.25W/1206
R9	Panasonic	ERJ-6GEYJ334V	1	680K/0.25W/5%/0805
R10	Panasonic	ERJ-6GEYJ103V	1	10k/0.125W/5%/0805
R11	Panasonic	ERJ-6GEYJ683V	1	68k/0.125W/5%/0805
R12	Panasonic	ERJ-6GEYJ753V	1	75k/0.125W/5%/0805

R13	Panasonic	ERJ-6GEYJ752V	1	7.5k/0.125W/5%/0805
R14	Panasonic	ERJ-8GEYJ470V	1	47/0.125W/5%/1206
R15	Panasonic	ERJ-8GEYJ102V	1	1k/0.125W/5%/1206
R16	Panasonic	ERJ-14YJ334U	1	330k/0.5W/5%/1210
R17	Panasonic	ERJ-8GEYJ0R75V	1	0.75/0.25W/5%/1206
R18	Panasonic	ERJ-8GEYJ273V	1	27k/0.25W/1206
R19, R22	Panasonic	ERJ-8GEYJ1R6V	2	1.6/0.25W/5%/1206
R20	Yageo	CFR-50JB-52-10K	1	10k/0.5W/5%
R21	Panasonic	ERJ-6GEYJ222V	1	2.2k/0.125W/5%/0805
RV1	Epcos	S07K150	1	150VAC/1.2kA/7mm
T1	Wurth	750316266	1	EF20, Horizontal, 10 pin
VCC, VDC(HV)	Keystone	5000	2	0.04" dia red

8 Transformer specification

Transformer type: Wurth 750316266 Rev 00
Primary inductance and leakage inductance:
Lp = 830µH (±10%), measured between pin 2 and pin 4, leakage inductance ≤ 44µH
Saturation current is 1.6A

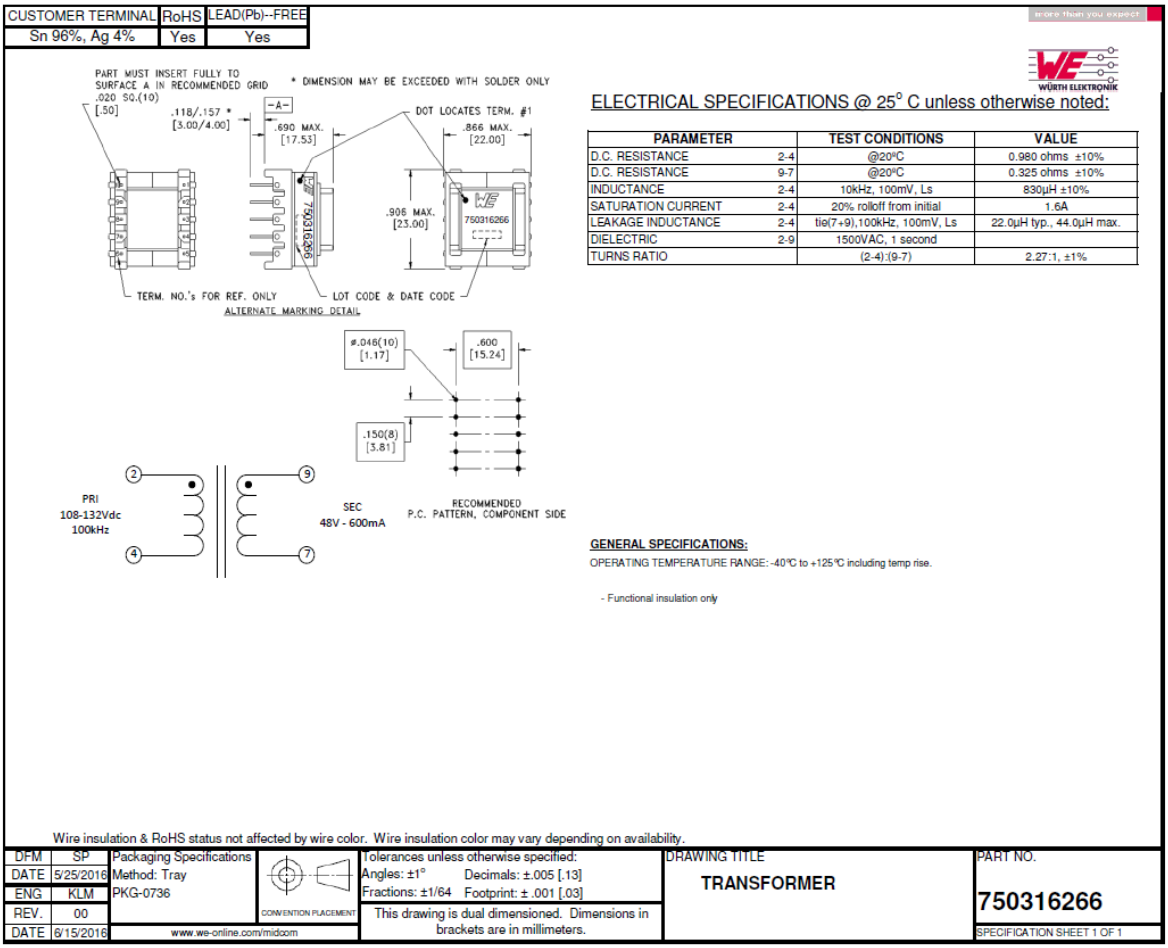


Figure 8 Flyback transformer specification

9 PCB Layout

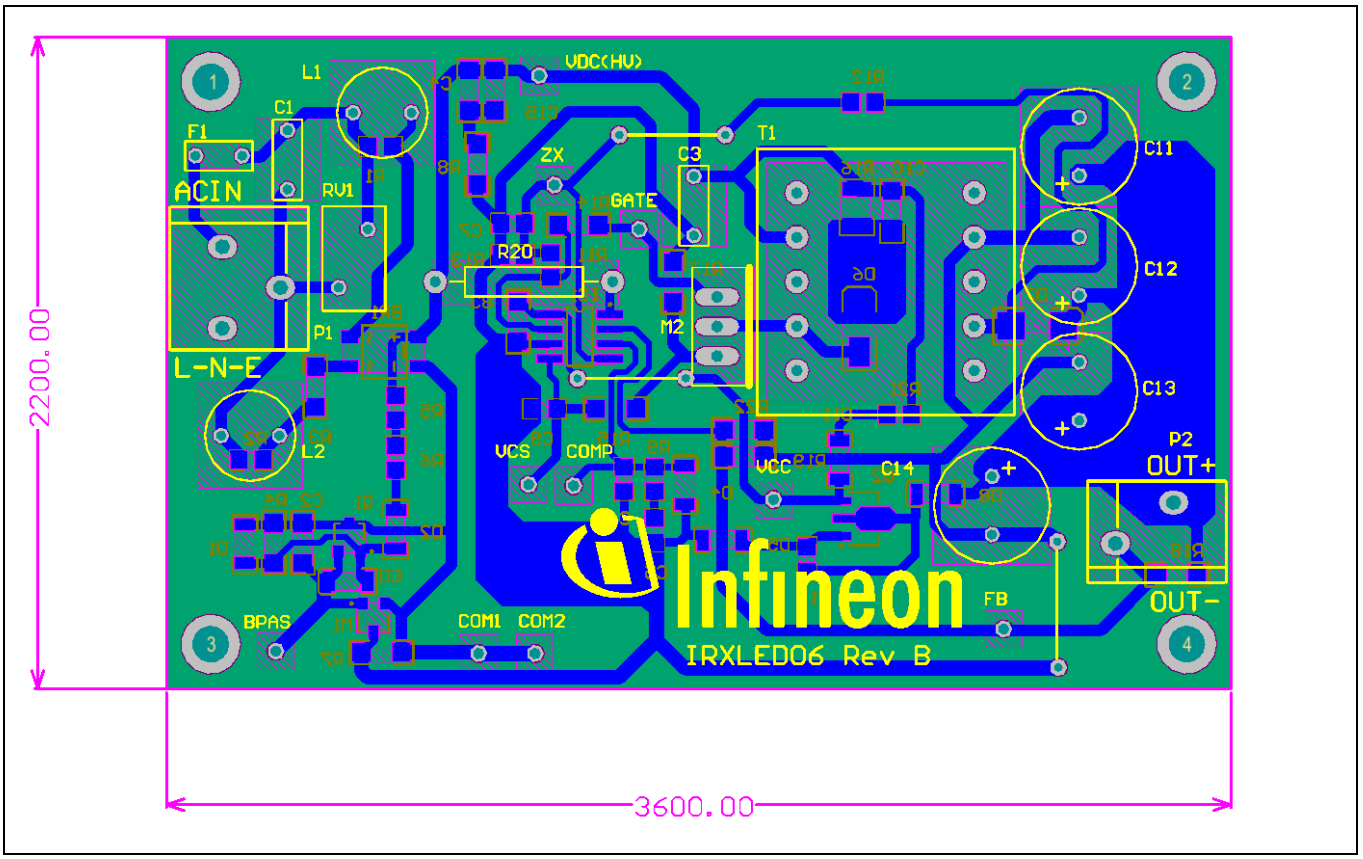


Figure 9 PCB top side components

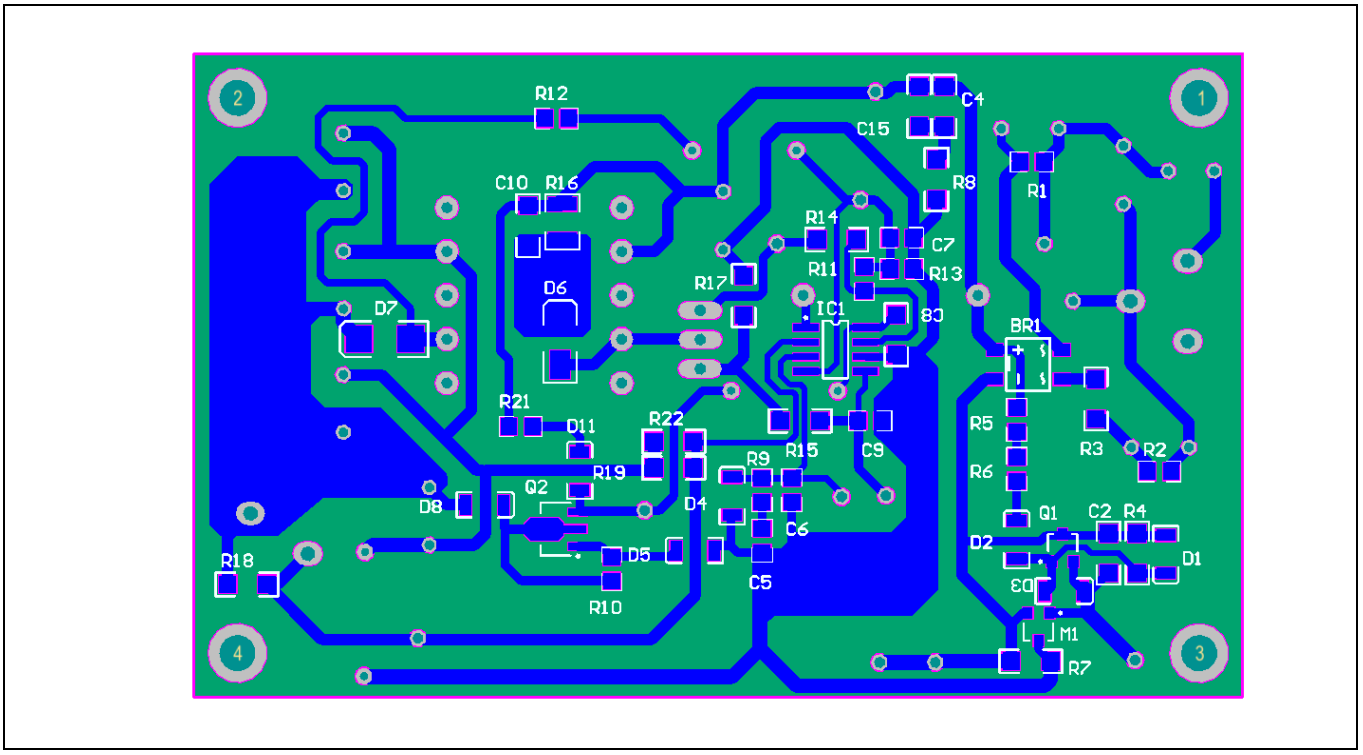


Figure 10 PCB bottom side components and traces

9.1 PCB layout guidelines for system optimization

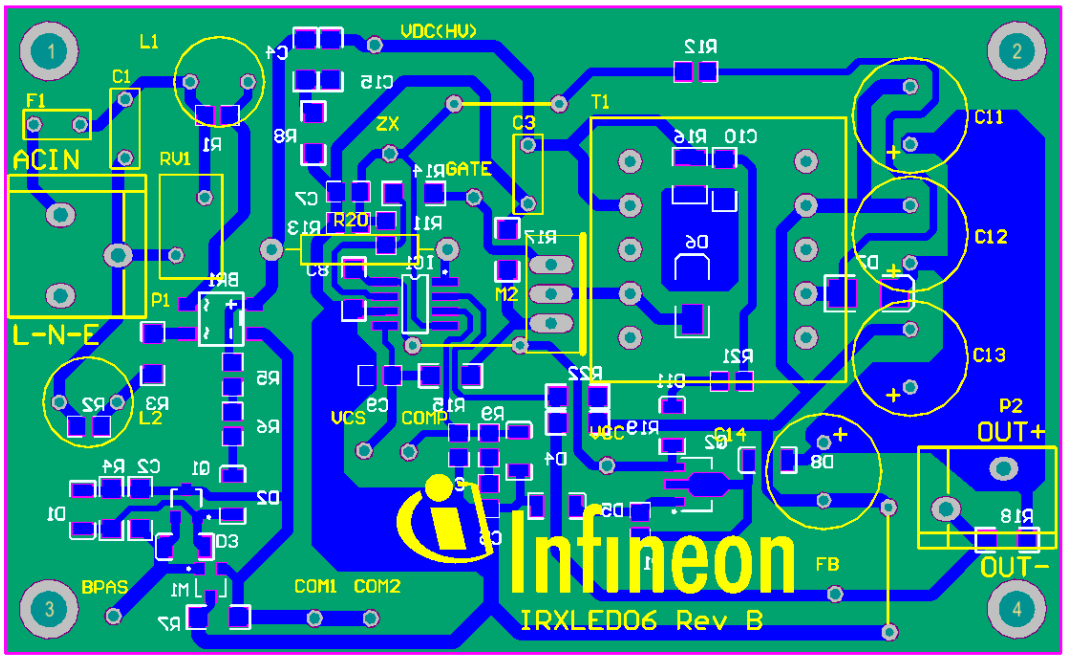


Figure 11 PCB layout

The left side of the above figure shows the primary and secondary high frequency current loops surrounded by a black outline in each case. The primary loop on the left side of the board originates from CIN (C3) connecting first to the transformer (T1) primary (pin 2). The other side of the primary winding (pin 4) is connected to the drain of the MOSFET (M2). To minimize EMI this trace should be kept as short as possible. The current sense resistor RCS (R17) is located such that the connection to the high frequency 0V bus return of CIN (C3) is extremely short with the other end connected to the source of MFB (M2) through another short trace. The secondary high frequency current loop originates from T1 pin 7 connecting through a short trace to DOUT (D7), which then connects through another very short trace to C12. The negative side of C12 returns directly back to T1 pin 9 again through another short trace providing the tightest possible HF current loop. Parallel output capacitors C11-14, are connected to C12 through large Copper traces to provide minimum impedance and best possible HF ripple current sharing between the capacitors. The layout techniques described minimize EMI emitted by the converter as much as possible.

Aside from EMI considerations, it is essential to design the PCB so that the IRS2982S is able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. The picture on the right of the above figure shows the area around IC1. Pin 6 is the 0V (ground) connection, which is returned to the 0V side of CIN (C3) through a direct connection. It is also essential that decoupling capacitor CVCC (C8) be located directly next to IC1 with direct connections to the VCC and COM/0V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star point, which is at the negative side of the high frequency capacitor CIN (C3).

Components associated with IC1 such as CCOMP (C5 and C6), RZX2 (R13), CZX (C7) are connected to the signal ground with the shortest traces possible back to pin 6.

10 Test results

10.1 Operation under different line and load conditions

Table 1 Input 90 VAC

Load(V)	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD
24	12.06	24.37	0.495	14.99	80.47%	0.994	8.11%
32	16.04	32.52	0.493	20.19	79.45%	0.996	6.22%
37	18.31	37.06	0.494	23.06	79.38%	0.997	5.90%
43	21.38	43.37	0.493	27.32	78.26%	0.997	7.43%
48	23.53	47.95	0.491	31.25	75.29%	0.991	13.00%

Table 2 Input 100 VAC

Load(V)	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD
24	11.98	24.20	0.495	14.664	81.69%	0.988	9.83%
32	16.05	32.52	0.494	19.726	81.37%	0.995	7.39%
37	18.30	37.01	0.494	22.491	81.36%	0.996	6.01%
43	21.40	43.32	0.494	26.550	80.60%	0.997	5.56%
48	23.57	47.93	0.492	29.980	78.61%	0.990	7.77%

Table 3 Input 110 VAC

Load(V)	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD
24	11.94	24.13	0.495	14.47	82.55%	0.985	11.37%
32	16.06	32.52	0.494	19.42	82.69%	0.992	8.68%
37	18.26	36.96	0.494	22.10	82.62%	0.994	6.85%
43	21.38	43.27	0.494	26.01	82.18%	0.996	5.90%
48	23.58	47.92	0.492	29.10	81.02%	0.996	6.10%

Table 4 Input 120 VAC

Load(V)	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD
24	11.94	24.13	0.495	14.47	82.55%	0.985	11.37%
32	16.06	32.52	0.494	19.42	82.69%	0.992	8.68%
37	18.26	36.96	0.494	22.10	82.62%	0.994	6.85%
43	21.38	43.27	0.494	26.01	82.18%	0.996	5.90%
48	23.58	47.92	0.492	29.10	81.02%	0.996	6.10%

Table 5 Input 130 VAC

Load(V)	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD
24	11.90	24.04	0.495	14.24	83.57%	0.974	14.00%
32	16.06	32.52	0.494	19.08	84.20%	0.985	11.00%
37	18.25	36.86	0.495	21.62	84.39%	0.992	8.98%
43	21.34	43.20	0.494	25.36	84.15%	0.992	7.55%
48	23.63	47.98	0.493	28.18	83.85%	0.990	7.79%

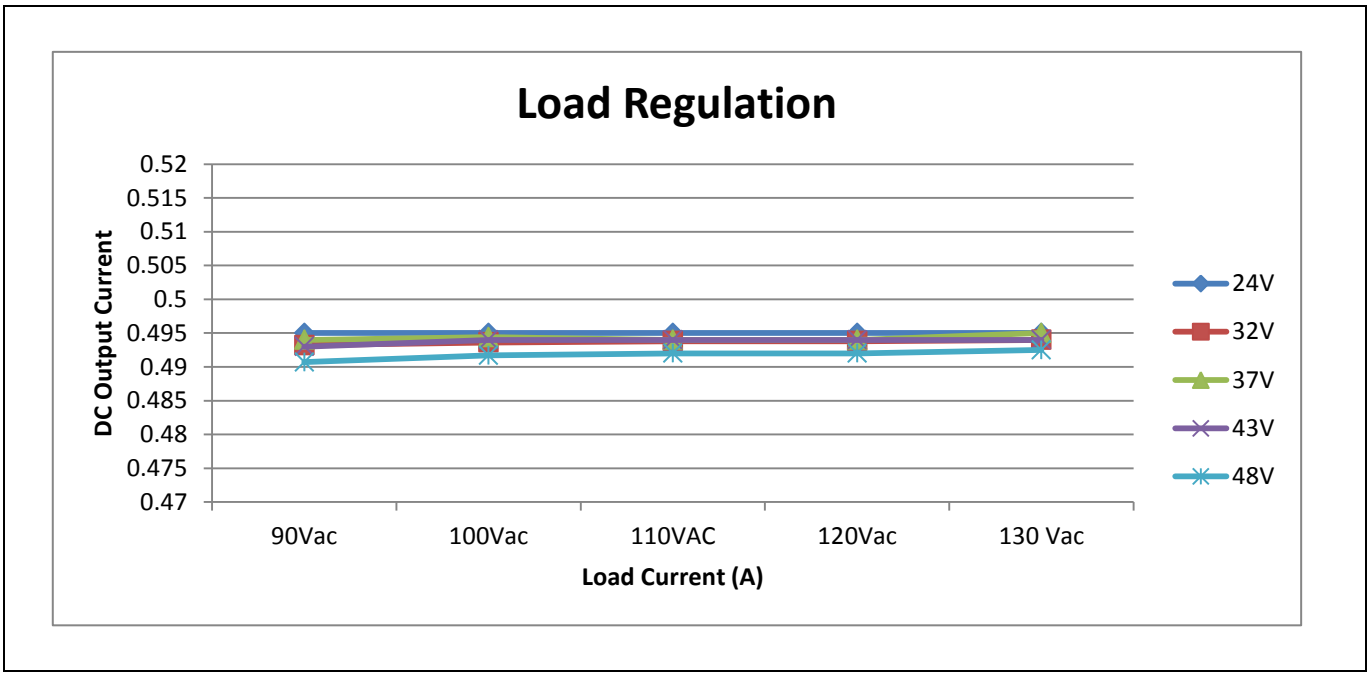


Figure 3 Load regulation at different line input voltages (no dimmer connected)

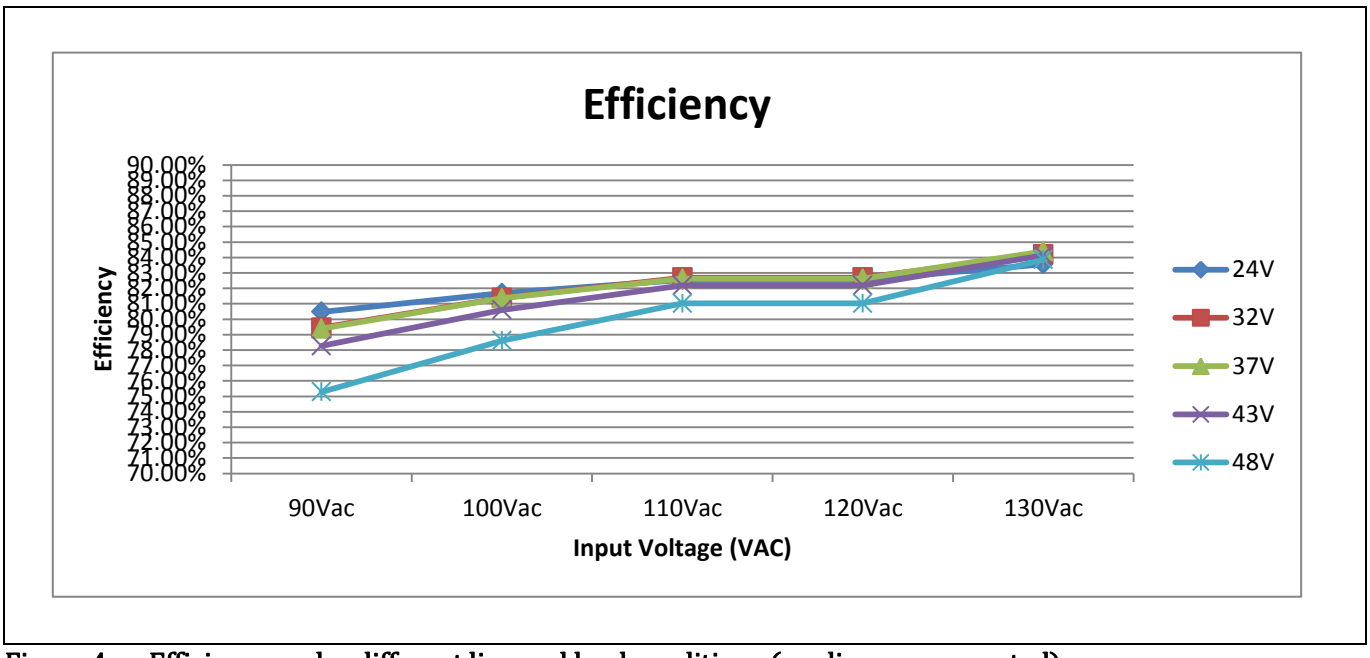


Figure 4 Efficiency under different line and load conditions (no dimmer connected)

10.2 Power factor and current harmonics (iTHD)

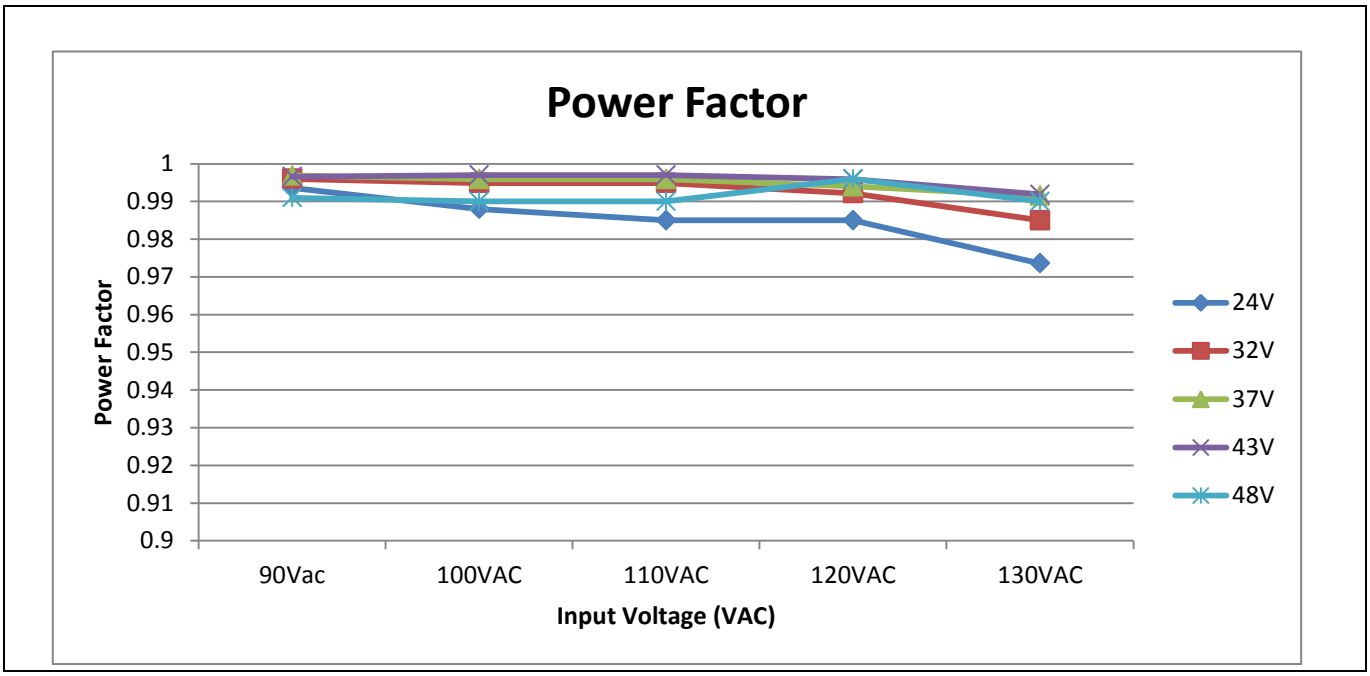


Figure 54 Power factor vs input voltage at different outputs (no dimmer connected)

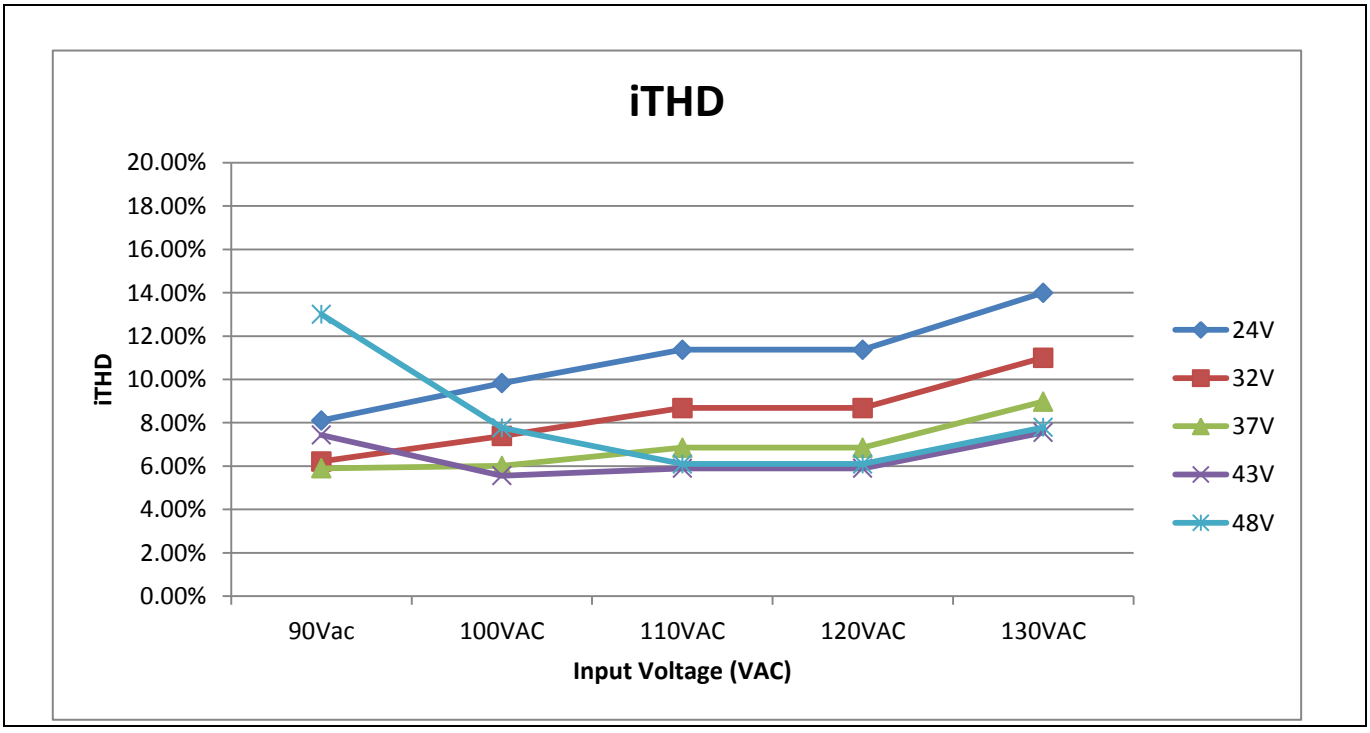


Figure 6 THDi vs input voltage at different outputs (no dimmer connected)

Table 6 EN61000-3-2 Class C limits for system power >25 W

Requirements	Harmonics Limits Class C according EN 61000-3-2 for System Power > 25W	
	Harmonics order n	Maximum value expressed as a percentage of the fundamental input current
	2	<2%
	3	<30 λ %
	5	10%
	7	<7%
	9	<5%
	11 ≤ n ≤ 39	<3%
		λ = power factor

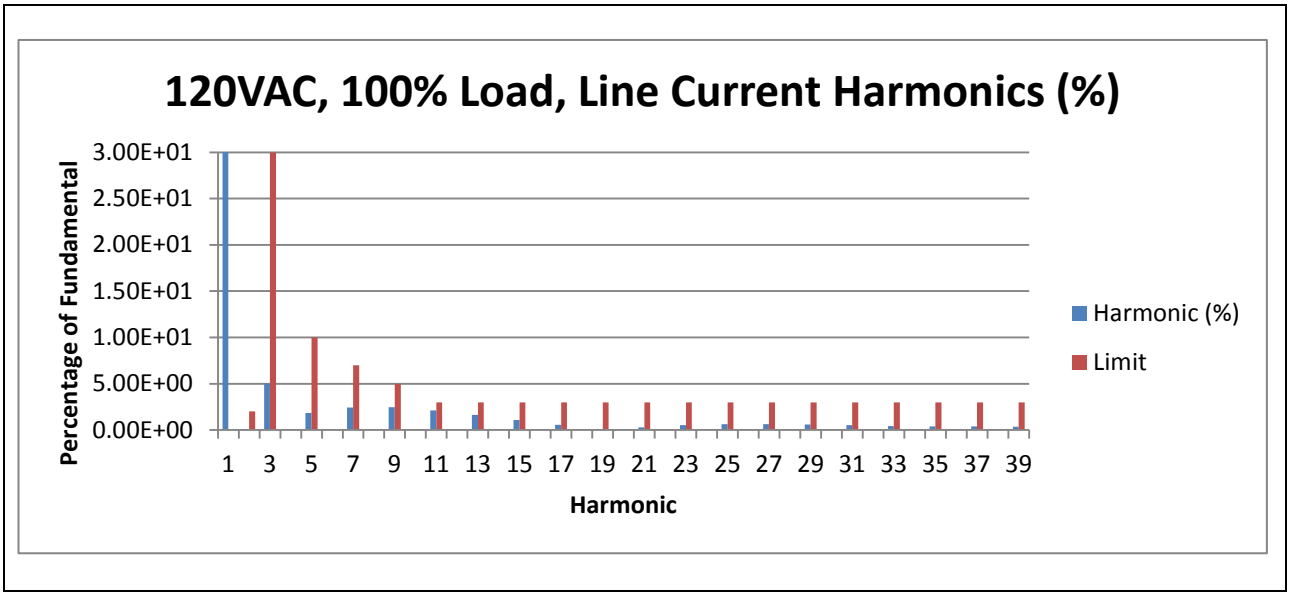


Figure 16 Harmonic test results at 120 VAC and 100% load

Class C limits are met at 100% load.

10.3 Start and steady state operation at maximum load

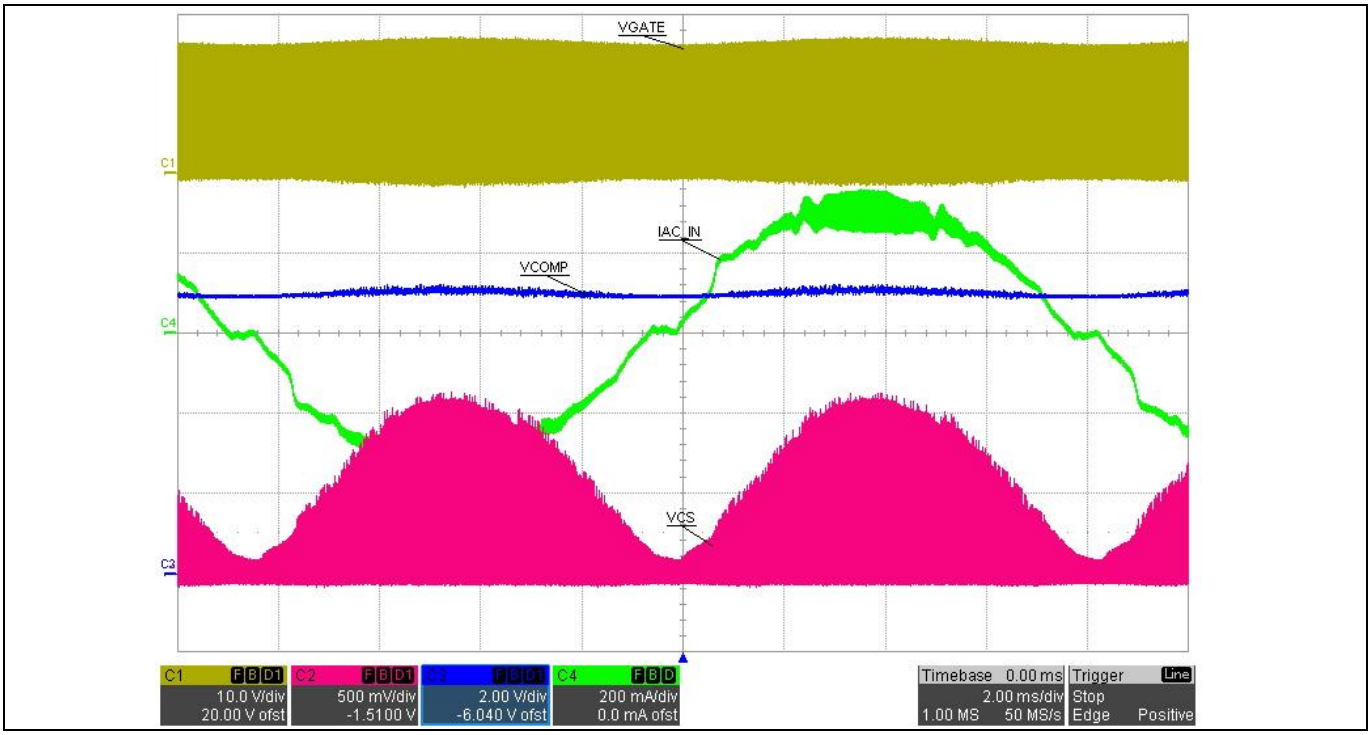


Figure 7 120 VAC steady state operation at 100% load
Input current (green), Gate drive (yellow), CS (red), VCOMP (blue)

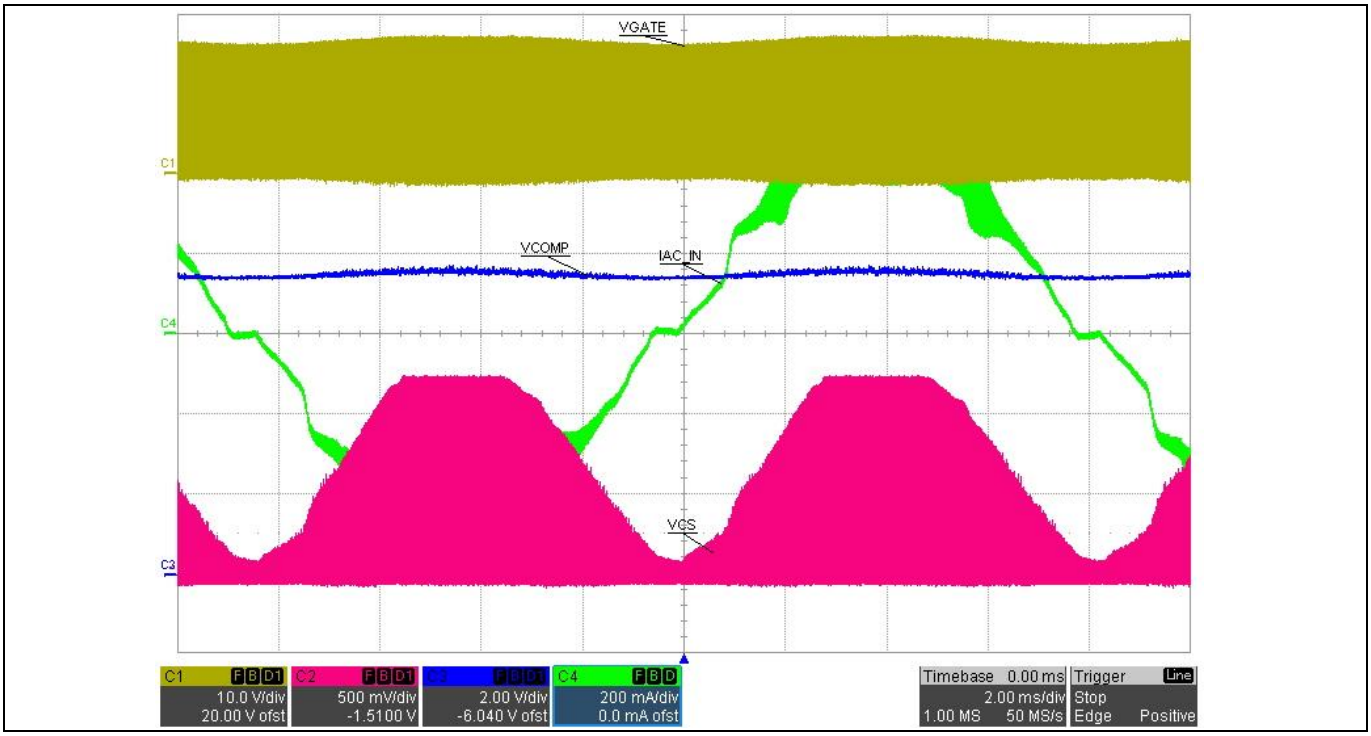


Figure 8 100 VAC start-up at 100% load with current limiting
Input current (green), Gate drive (yellow), CS (red), VCOMP (blue)

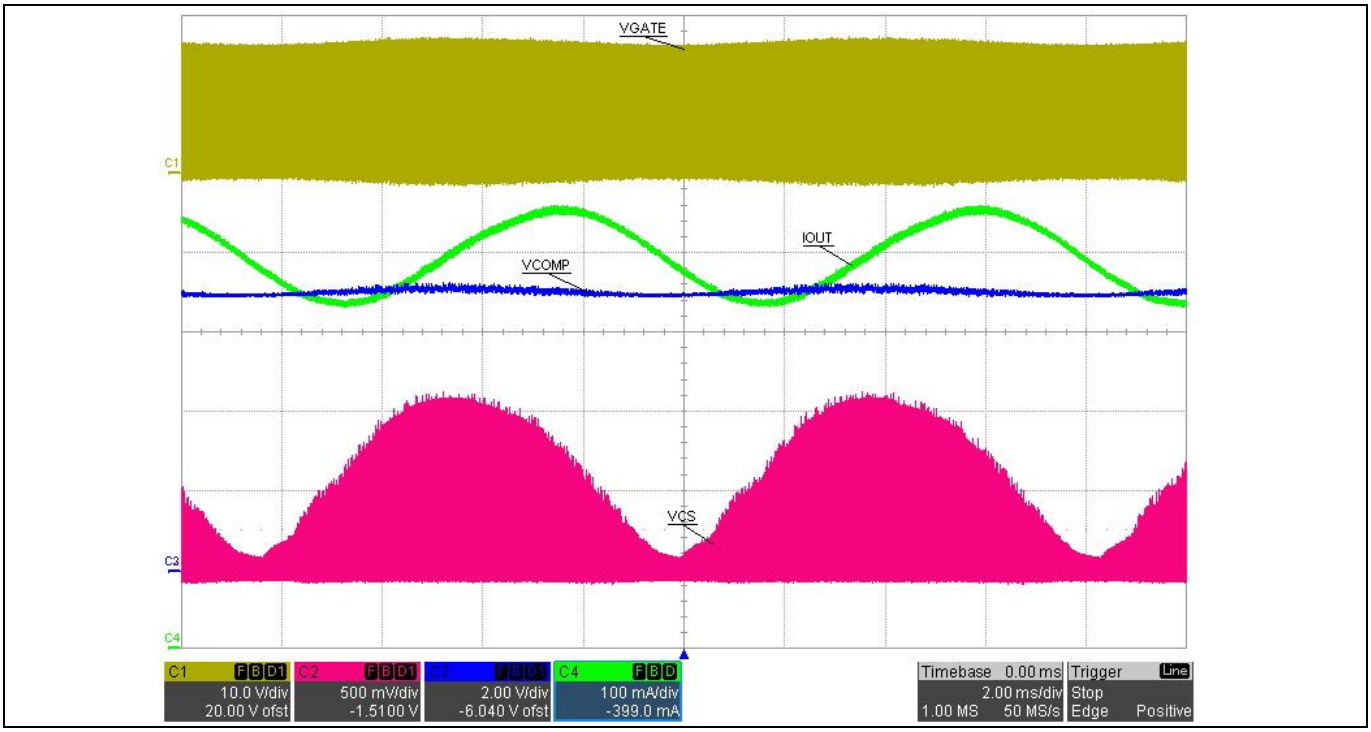


Figure 9 120 VAC steady state operation at 100% load
Gate drive (yellow), CS (red), VCOMP (blue), Output current (green)

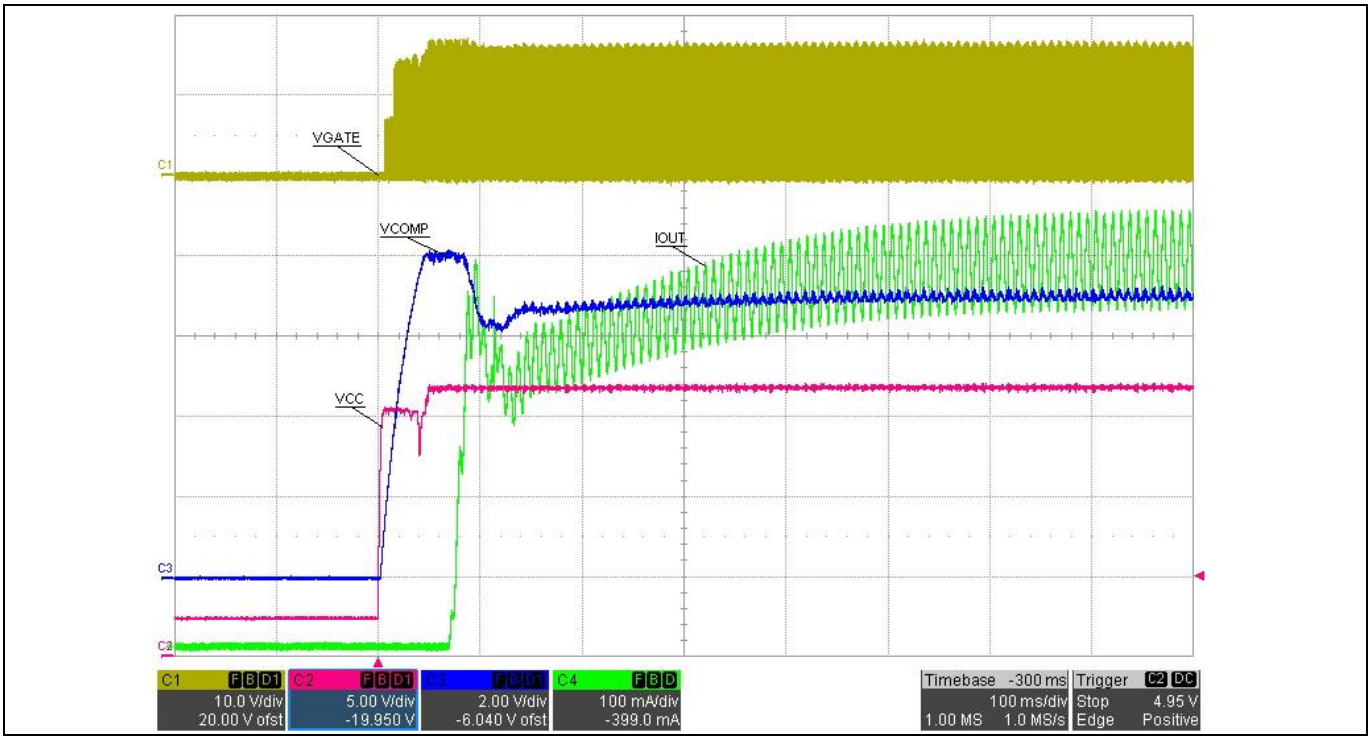


Figure 20 120 VAC start-up at 100% load
Gate drive (yellow), VCC (red), VCOMP (blue), Output current (green)

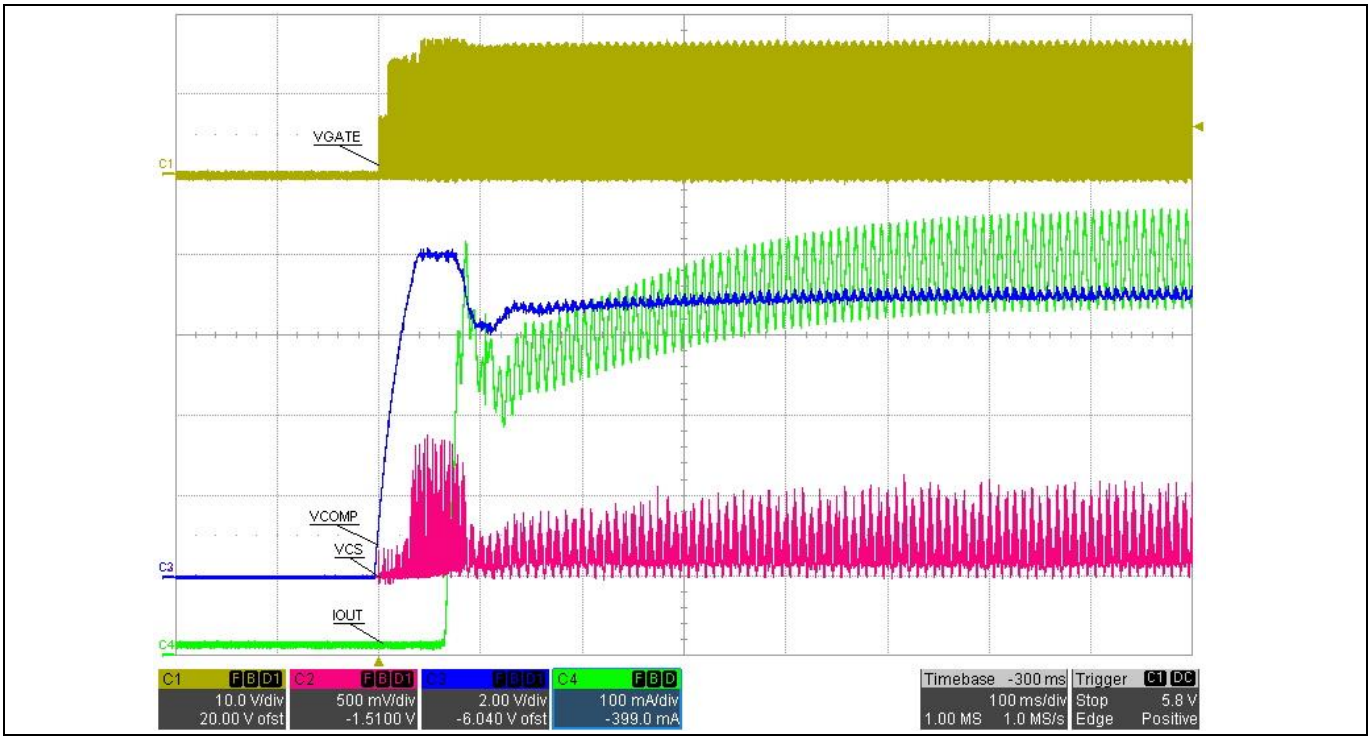


Figure 21 120 VAC start-up at 100% load
Gate drive (yellow), VCS (red), VCOMP (blue), Output current (green)

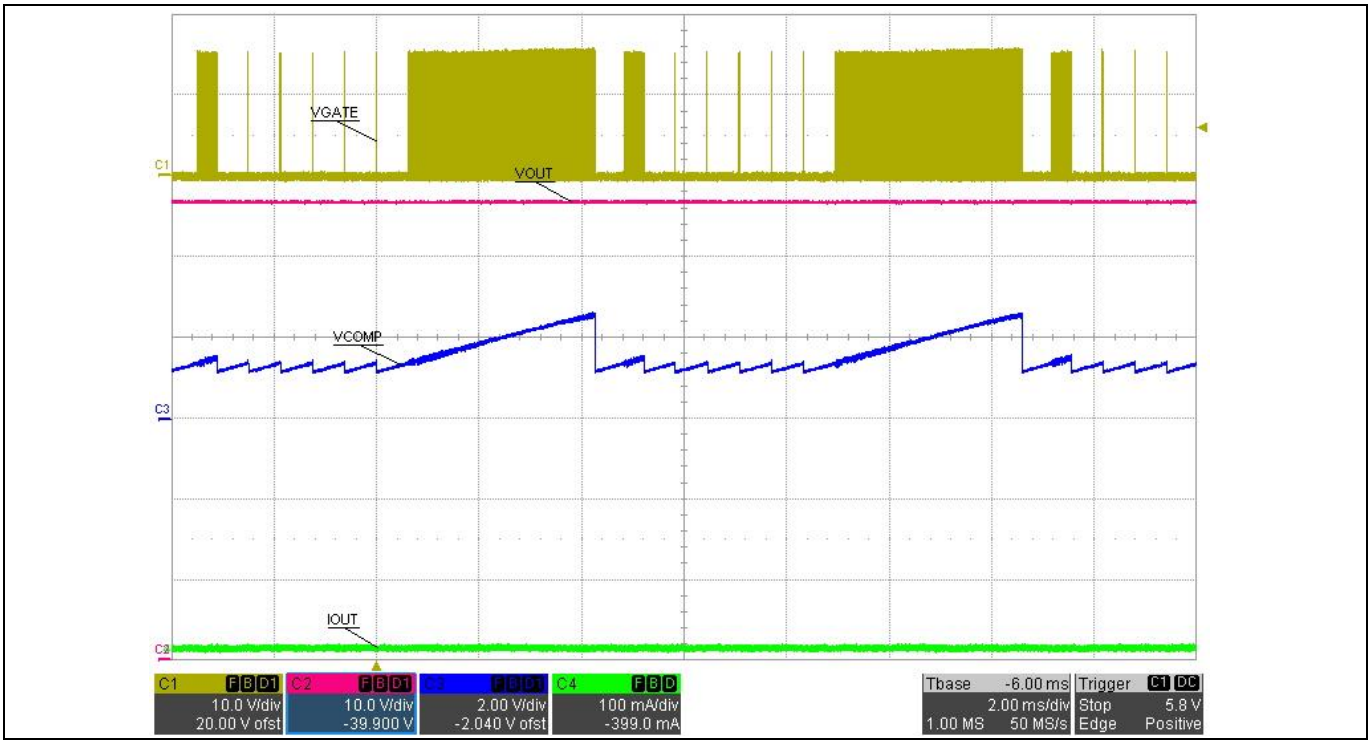


Figure 10 120 VAC open circuit output
Gate drive (yellow), VCOMP (blue), Output voltage (red), Output current (green)

10.4 Operation with a triac based dimmer

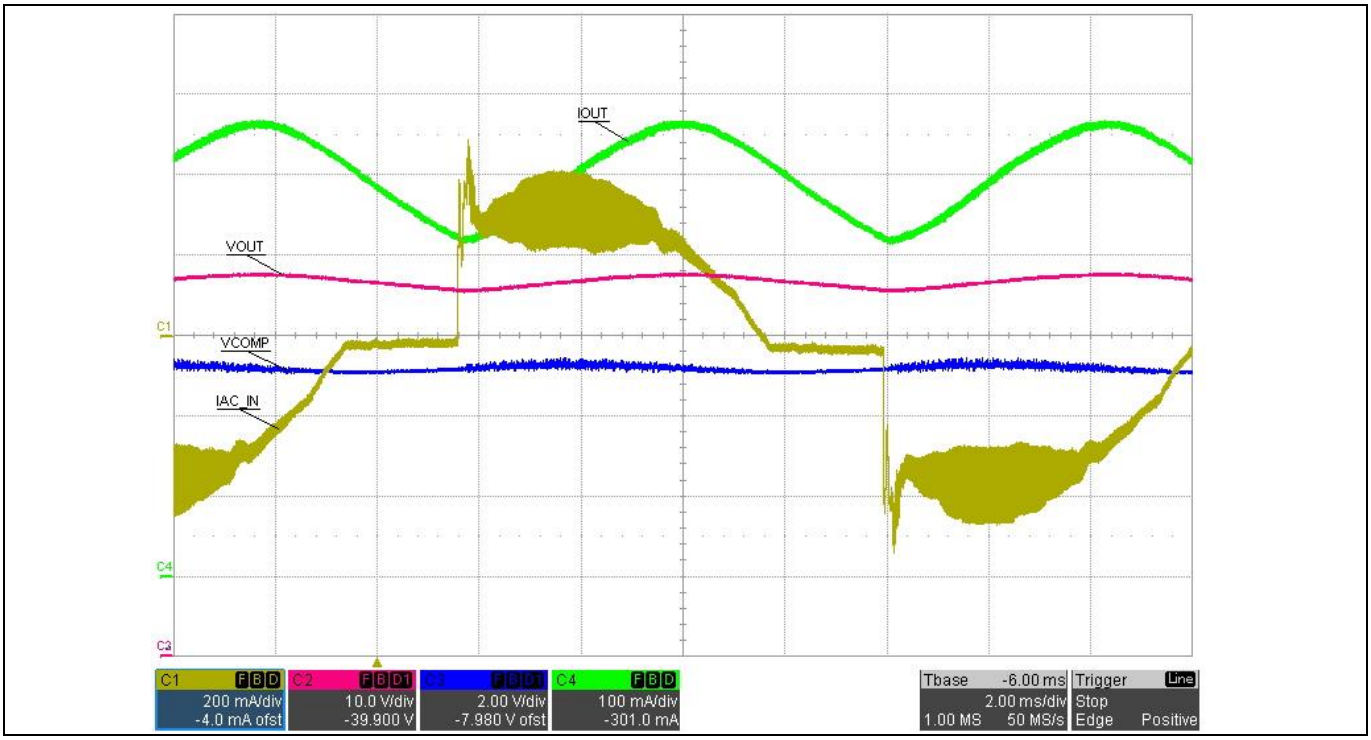


Figure 11 120 VAC steady state operation at 100% load with dimmer set at maximum
Input current (yellow), VCOMP (blue), VCOMP (green), Output voltage (red)

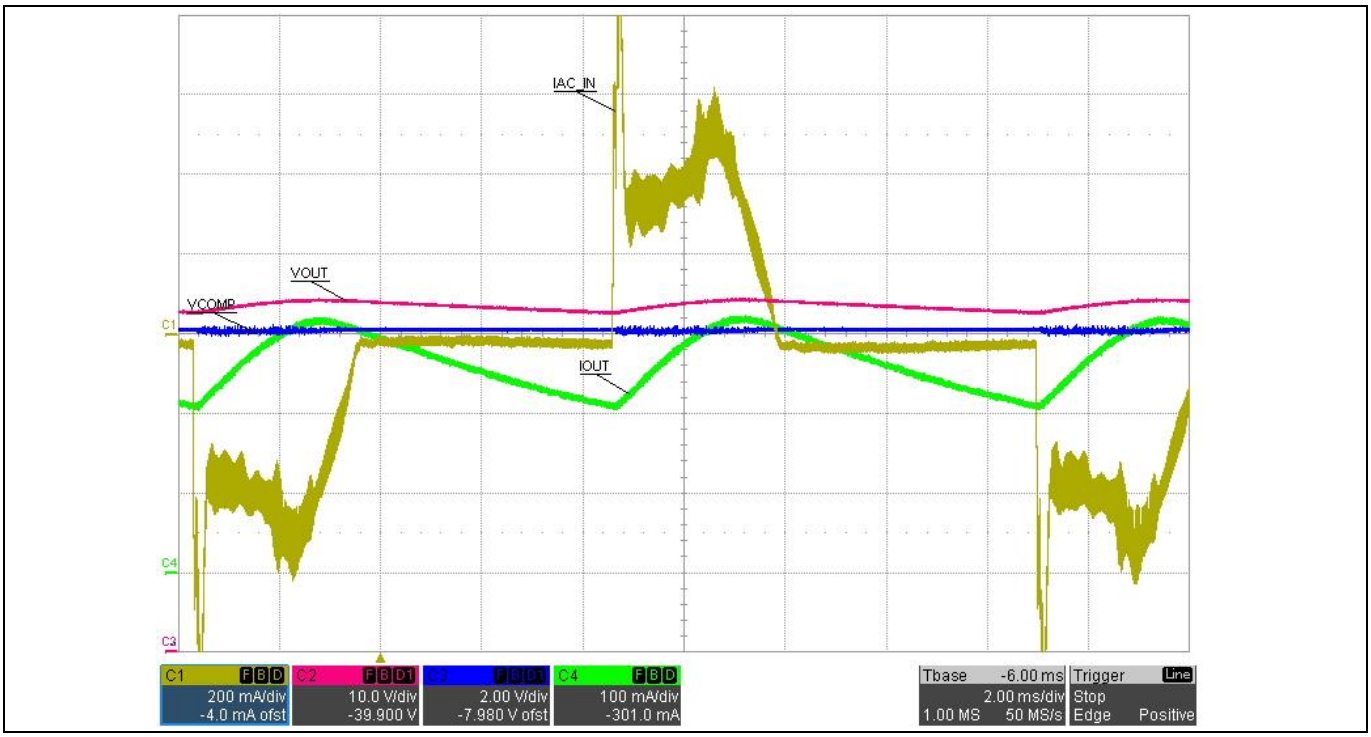


Figure 12 120 VAC steady state operation at 100% load with dimmer set at mid-point
Input current (yellow), VCOMP (blue), VCOMP (blue), Output voltage (red)

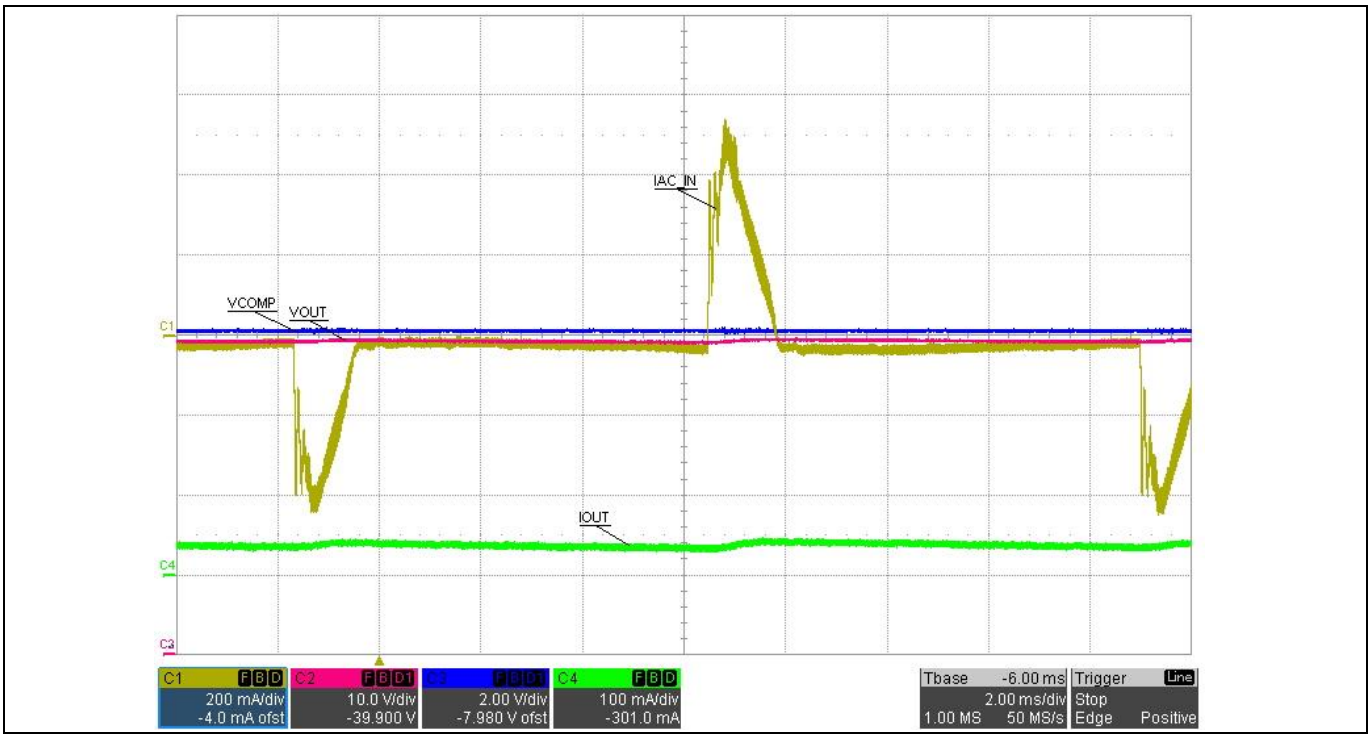


Figure 13 120 VAC steady state operation at 100% load with dimmer set at minimum Input current (yellow), VCOMP (blue), VCOMP (blue), Output voltage (red)

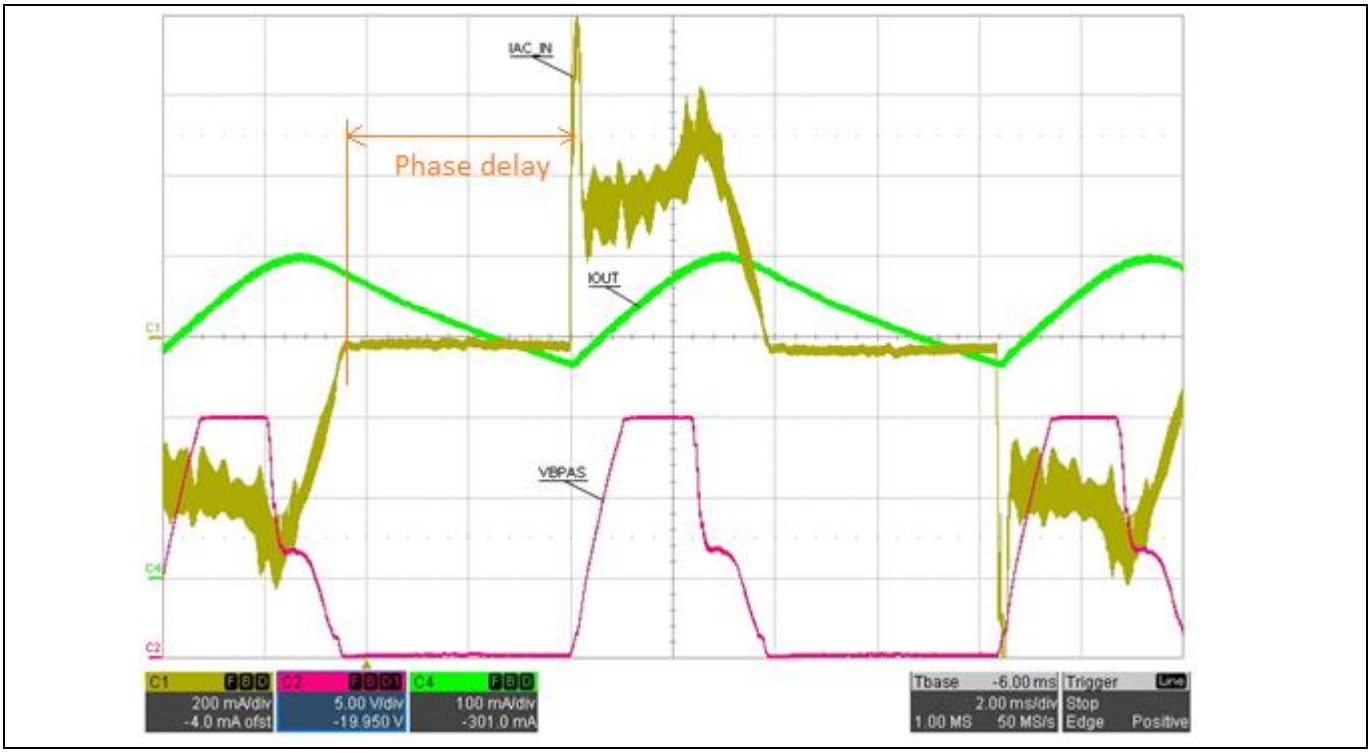


Figure 14 120 VAC steady state operation at 100% load with dimmer set at mid-point Input current (yellow), VCOMP (blue), VCOMP (blue), Bypass MOSFET gate drive (red)

The dimmer phase delay for leading edge (triac based) dimmers is defined as the period from the line zero crossing to the firing point, which increases as the dim level is reduced.

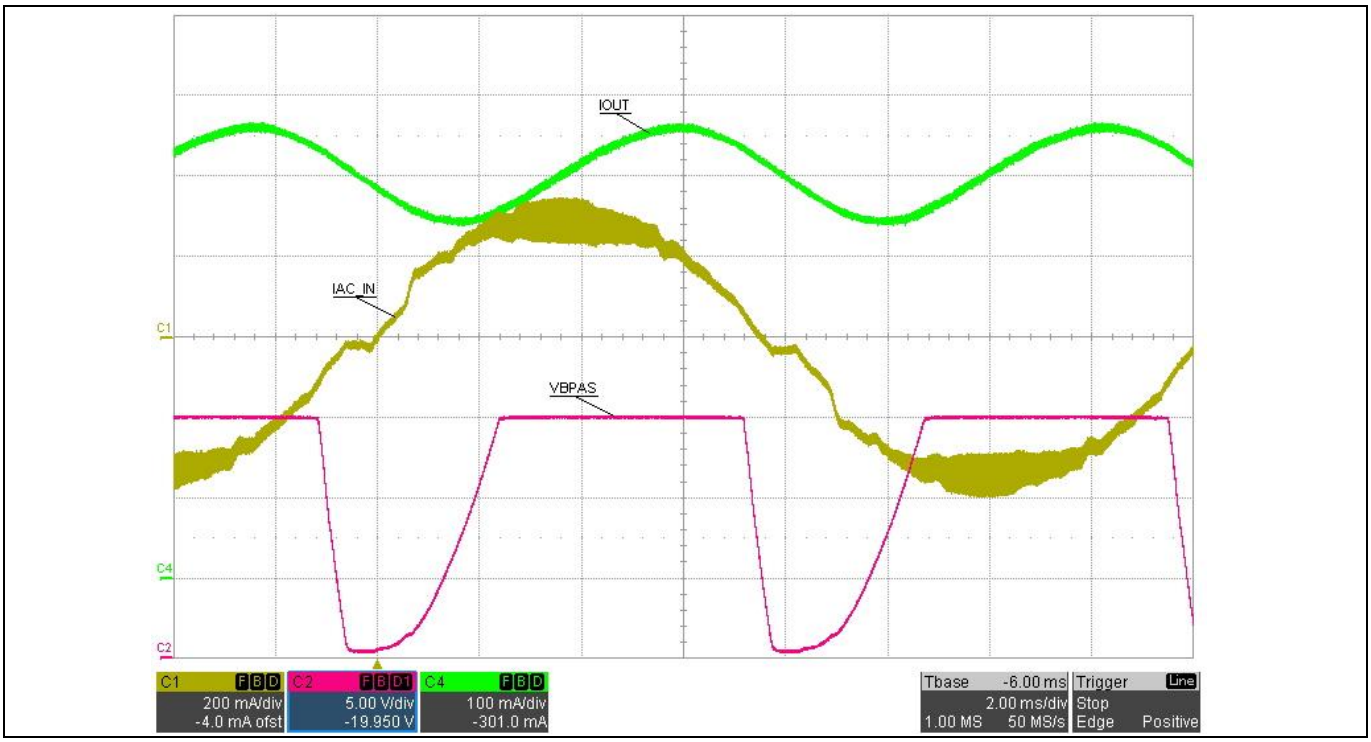


Figure 15 120 VAC steady state operation at 100% load with no dimmer set with no dimmer Input current (yellow), VCOMP (blue), VCOMP (blue), Bypass MOSFET gate drive (red)

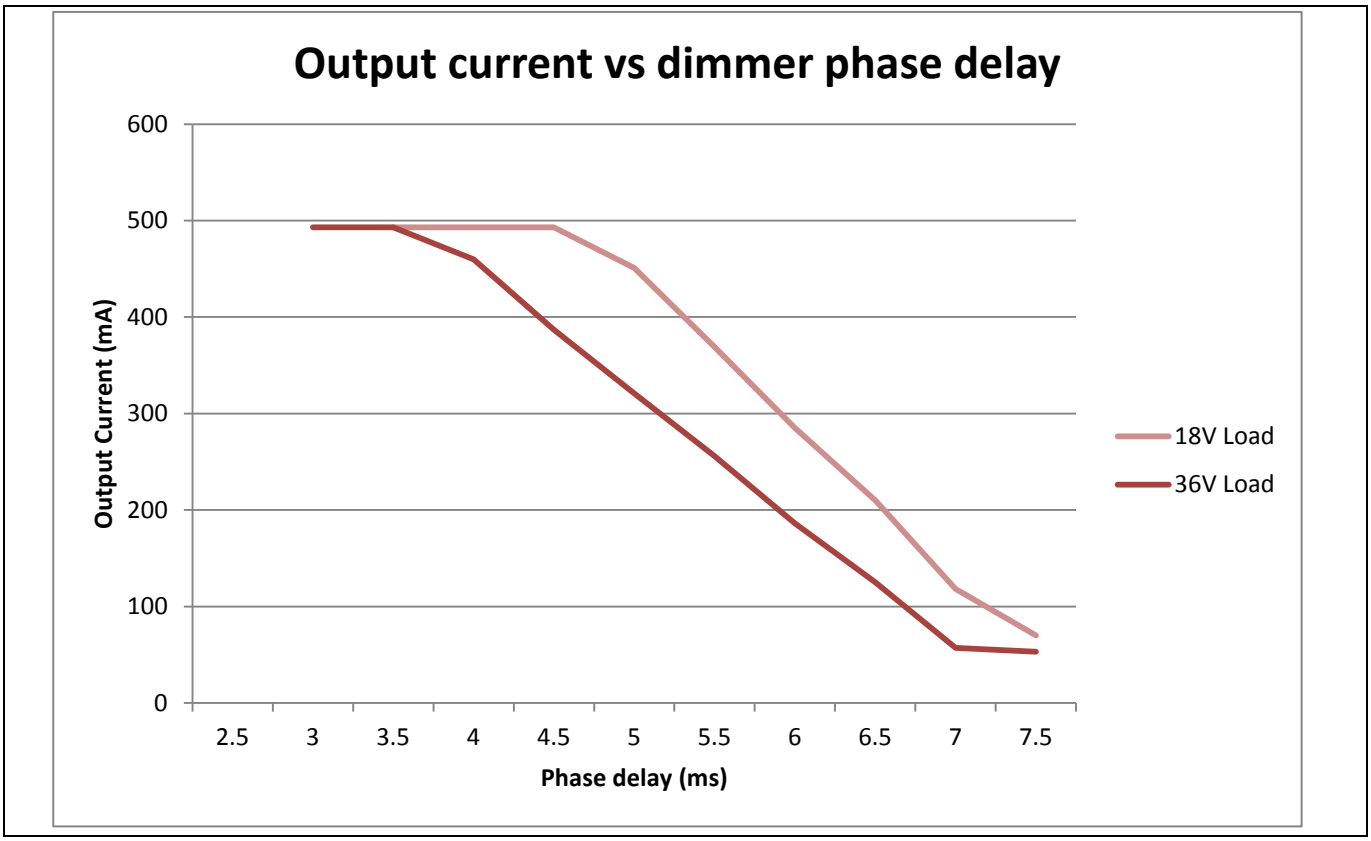


Figure 16 Output current vs dimmer phase for Lutron digital dimmer

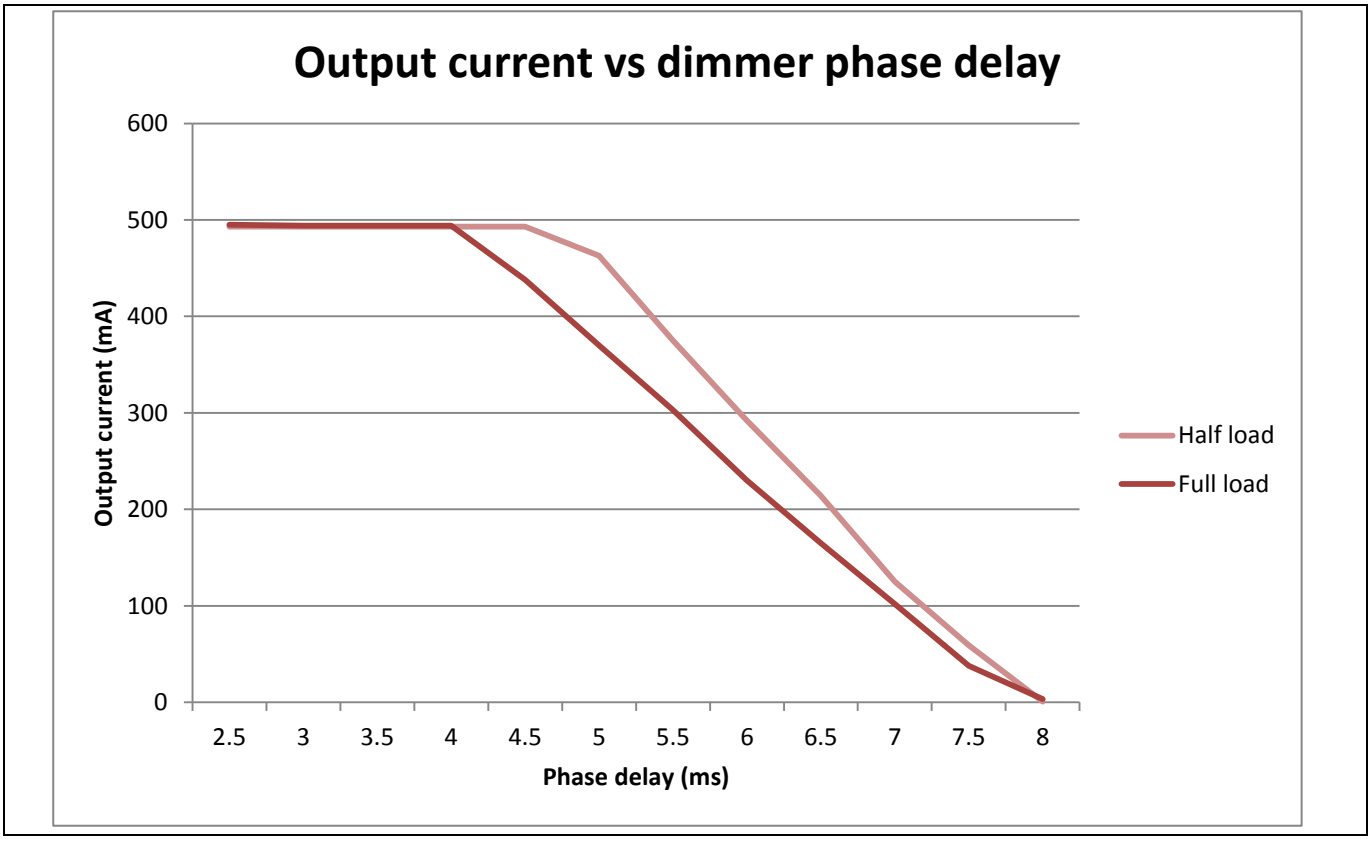


Figure 17 Output current vs dimmer phase for Leviton slider dimmer

10.5 Thermal Performance under normal operating conditions

No dimmer is connected for thermal test.

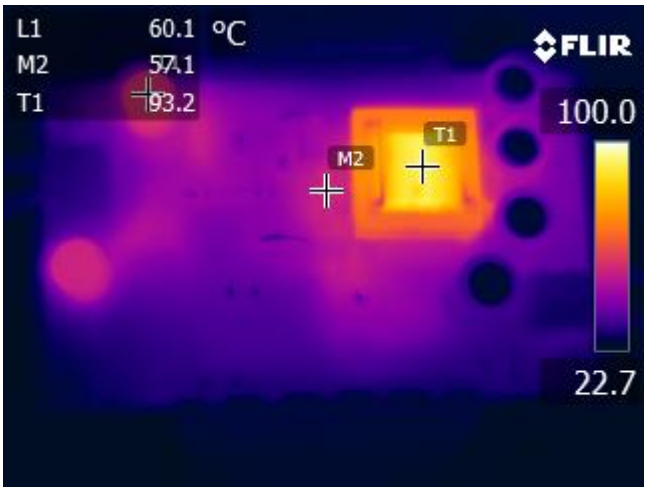


Figure 30 120 VAC at 100% load top side thermal image

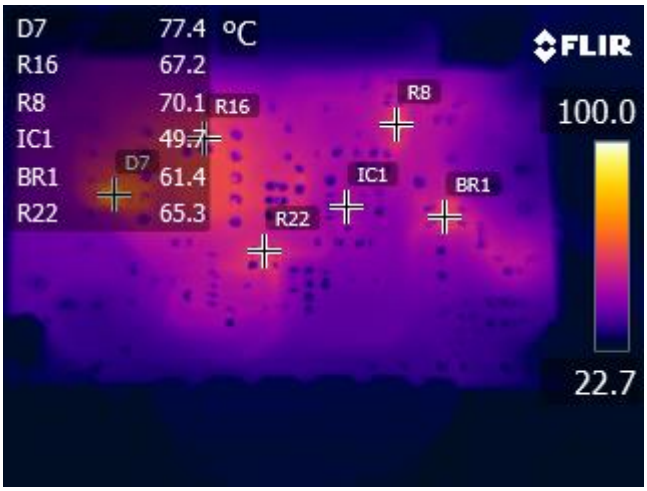


Figure 31 120 VAC at 100% load bottom side thermal image

10.6 Conducted EMI test results

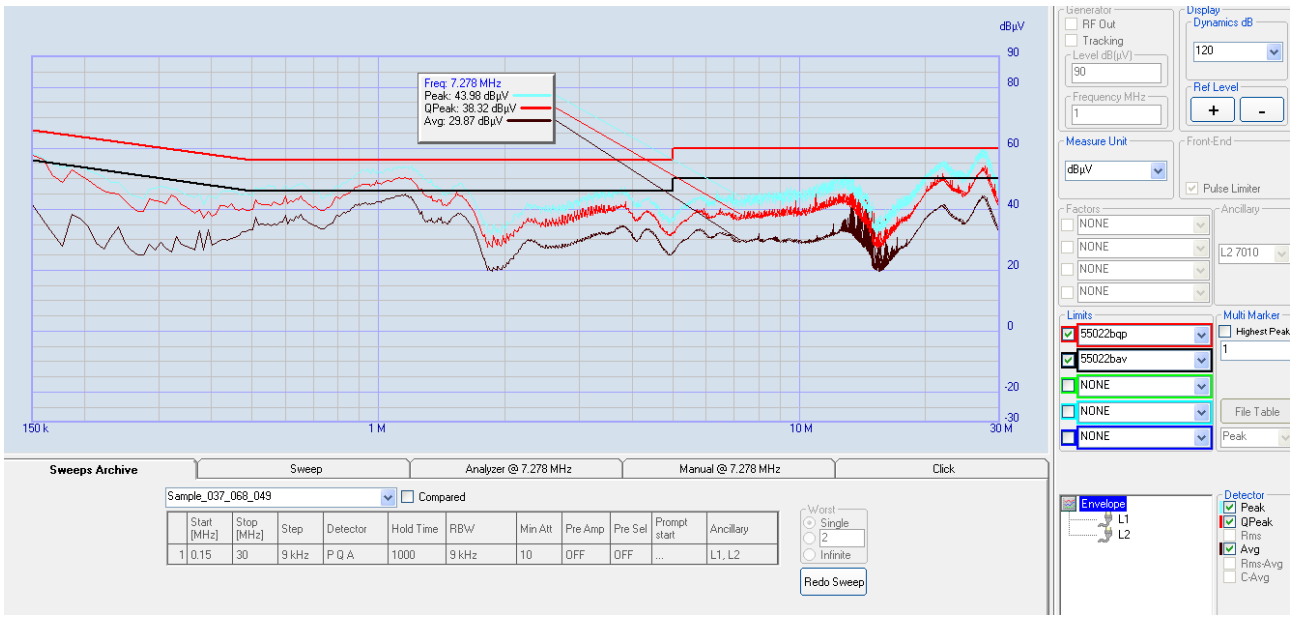


Figure 32 Conducted emissions at 120 VAC and 100% load

The red limit line shows the limit for the quasi-peak measurement, for which the frequency sweep trace is also shown in red. To pass the red trace must to remain below the red limit line and the pink average measurement trace must remain below the yellow average limit line. The orange peak trace may be disregarded.

EMI emissions are very dependent on the board layout, please refer to section 9.1.

Note

Infineon Technologies does not guarantee compliance with any EMI standard.

11 Conclusion

Where galvanic isolation is not required a phase cut dimmable current regulated LED driver can be effectively implemented using a low cost, low component count solution based on the IRS2982S as demonstrated by the IRXLED06 evaluation board. Safety standards in LED bulbs and lamps are now often met by mechanical means, which prevent user access to live parts and therefore non-isolated driver solutions are becoming more popular due to their excellent performance, relative simplicity and low cost.

Compatibility with standard triac based dimmers is achieved by clamping the COMP pin voltage by an external zener diode enabling a linear dimming characteristic down to 10% of output current or lower. The front end circuitry comprises the input filter, passive or active damper and bleeder networks, which allow the triac to fire and maintain conduction until the next line zero crossing. These networks are designed to work in either a 120VAC or 220VAC application and since they need to be optimized to one or other of these ranges, it is not practical to design a triac dimmable LED driver able to cover both.

The IRXLED06 converter is a simple analogue solution and therefore dimming characteristics and minimum dimming level will vary depending on the type of dimmer being used with it. This is illustrated in figures 26 and 27, however stable and linear performance is achievable down to 10% in most cases. Even if the firing angle is equal for two different dimmers the output current depends on the load and characteristics of the dimmer, which shape the voltage applied at the LED driver input. Digital solutions able to self-adjust have been launched in the market but the additional cost has not proven to be acceptable for the majority of applications and these more complex solutions have generally not been adopted.

Output current regulation is very tightly regulated since the current is directly fed back to the IRS2982S as a proportional voltage from a shunt resistor. The 400mV feedback threshold allows direct feedback with 140mW resistor dissipation at 350mA and 280mW dissipation at 700mA making it suitable for such applications where most controller feedback thresholds would be too high. Open and short circuit protection make the design tolerant to external fault conditions.

The IRXLED06 evaluation board achieves a power factor well above 0.9 and line current THD less than 10% at maximum load when no dimmer is connected. It is also able to meet EN61000-3-2 harmonic limits and EN55022 conducted emission limits.

References

[1] IRS2982SPBF IC datasheet, Infineon Technologies.

Attention:

Revision History

Major changes since the last revision

Page or Reference	Description of change
	First Release

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