REF_SiC_D2Pak_MC and REF_SiC_D2Pak_BP User Guide

1200 V CoolSiC™ MOSFET in D2Pak with coreless isolated gate driver reference board

About this document

Scope and purpose

This user guide describes how to operate the reference boards of 1200 V CoolSiC™ MOSFET in D2Pak with coreless isolated gate drivers.

Intended audience

This document is intended for owners and users of the reference boards.

Reference board

There are two types of reference boards described in this guide:

- REF_SiC_D2Pak_MC_V0.1, uses 1EDC20I12MH with Miller clamp function
- REF_SiC_D2Pak_BP_V0.1, uses 1EDI20H12AH with bipolar power supply and separated sink/source output

The two reference boards are designed as daughter boards to fit the 1200 V CoolSiC™ MOSFET in TO-247 3-/4-pin evaluation platform. By installing the reference daughter board (hereafter called ‘daughter board’) on the evaluation platform (hereafter called ‘main board’), the user can do a double pulse test to evaluate the performance of the CoolSiC™ MOSFET and coreless isolated gate drivers.

Note: Boards do not necessarily meet safety, EMI, or quality standards (for example UL, CE) requirements.

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Safety precautions

Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 800 V. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The reference daughter board at a glance

1.1 Block diagram

The gray area in Figure 1 indicates the function blocks of the daughter boards. The gate drivers and CoolSiC™ MOSFETs are all placed on the daughter boards in a half-bridge configuration, and the remaining circuits are located in the main board.

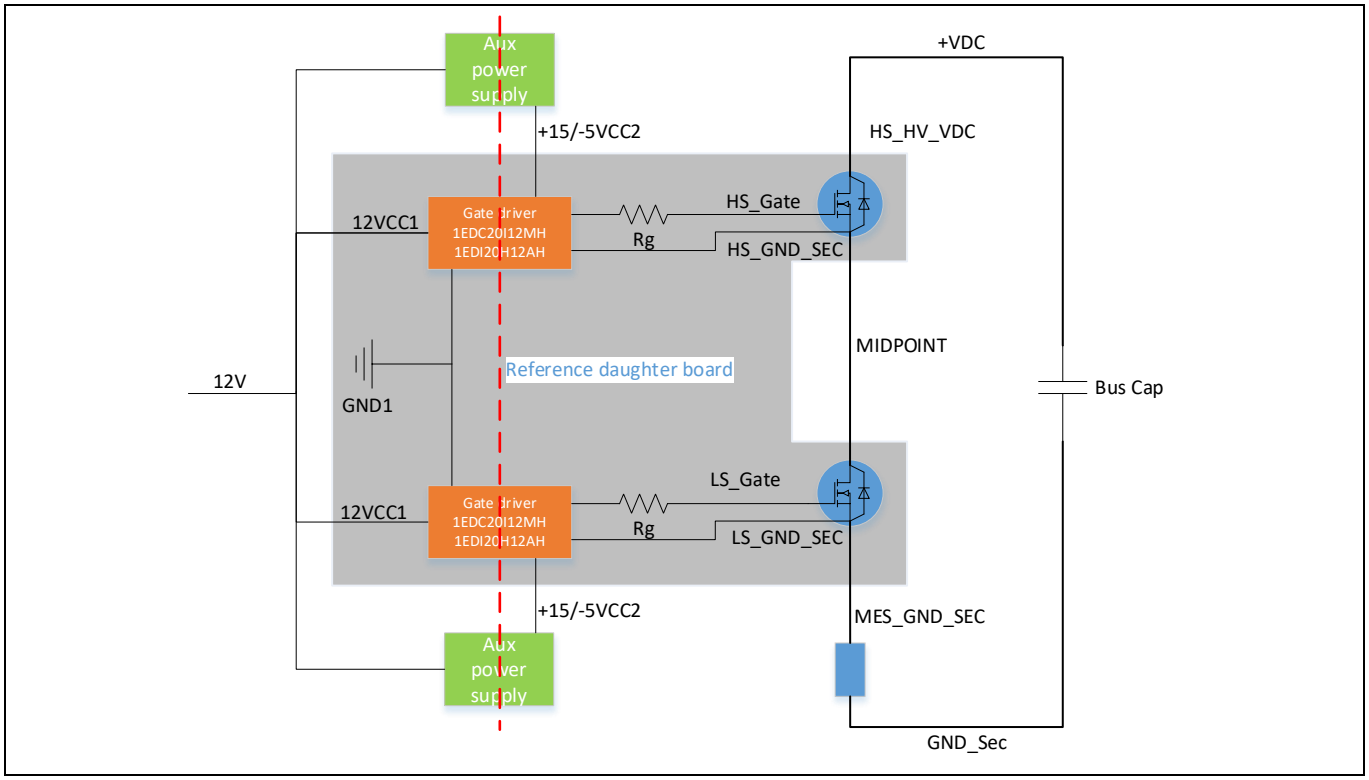


Figure 1 Block diagram of the daughter boards

1.2 Main features of the daughter boards

- Both daughter boards utilize insulated metal substrate (IMS), which provides an excellent thermal conduction capability.
- All the components are surface mounted devices (SMD) due to the IMS board type.
- Creepage is at least 4 mm to ensure the safe operation under 800 V_{DC} bus voltage.

1.3 Main features of the components

The main components on the boards and their features are listed as follows:

- IMBG120R030M1H
  - CoolSiC™ 1200 V silicon carbide (SiC) trench MOSFET
  - 30 mΩ on-state drain-source resistance with threshold-free on-state characteristics
  - Very low switching losses
  - Benchmark gate threshold voltage, $V_{GS(th)}$=4.5 V
  - O V turn-off gate voltage for easy gate drive
  - Fully controllable dV/dt

- Robust body diode for hard commutation
- Temperature-independent turn-off switching losses
- Sense pin for optimized switching performance

- 1EDC20I12MH
  - Single channel galvanically isolated gate driver in wide body package
  - Coreless technology
  - Minimum 2.0 A peak drive current
  - Active Miller clamp function
  - Wide input voltage operating range
  - Suitable for operation at high ambient temperature and in fast switching applications
  - Recognized under UL 1577 with an insulation test voltage of V_{ISO}=3000 V(rms) for 1 S
- 1EDI20H12AH
  - Single channel galvanically isolated gate driver in wide body package
  - Coreless technology
  - Minimum 2.0 A peak drive current
  - Separate source and sink outputs
  - Wide input voltage operating range
  - Suitable for operation at high ambient temperature and in fast switching applications

1.4 Board parameters and technical data

The electrical and mechanical parameters are the same for the two reference daughter boards.

Table 2 Board specification

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Electrical parameter					
Bus voltage	V_{bus}	HS_HV_VDC to MES_GND_SEC		800	V
Supply voltage of gate driver input side	VCC1	VCC1 to GND1	-0.3	18.0	V
Logic input voltages (IN+, IN-)	$V_{LogicIN}$	IN+/IN- to GND1	-0.3	18.0	V
Supply voltage of gate driver output side	VCC2	VCC2 to GND2, for 1EDC20I12MH	-0.3	20	V
		VCC2 to GND2, for 1EDI20H12AH	-0.3	40	V
Current	I_{DS}	25℃ ambient temperature		56	A
Breakdown voltage between the circuit layer and substrate		ASTM D149	1200		V
Operation temperature			0	50	℃
Mechanical parameter					
Dimension		Length*Width	50*40		mm
Metal substrate thickness			2		mm
Copper thickness			1		oz
Material					
Thermal conductivity		ASTM D5470	1.0		W/m.K

The reference daughter board at a glance

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Peel strength		IPC-TM-650 2.4.8	1.5		N/mm
Flammability		UL94	V-0		Class
RoHS compliant					

2 System and functional test description

2.1 Description of the daughter board

All the components are located on the bottom side of the daughter board. The pin headers are SMD headers, which match the pin sockets on the main board. Figure 2 and Figure 3 depict the daughter board details.

*Note: The two daughter boards have the same appearance, thus only the REF_SiC_* D2Pak *_MC_V0.1 is demonstrated herein.*

The test pins seen in Figure 2 are not provided in the board delivery. The users have to solder them in field.

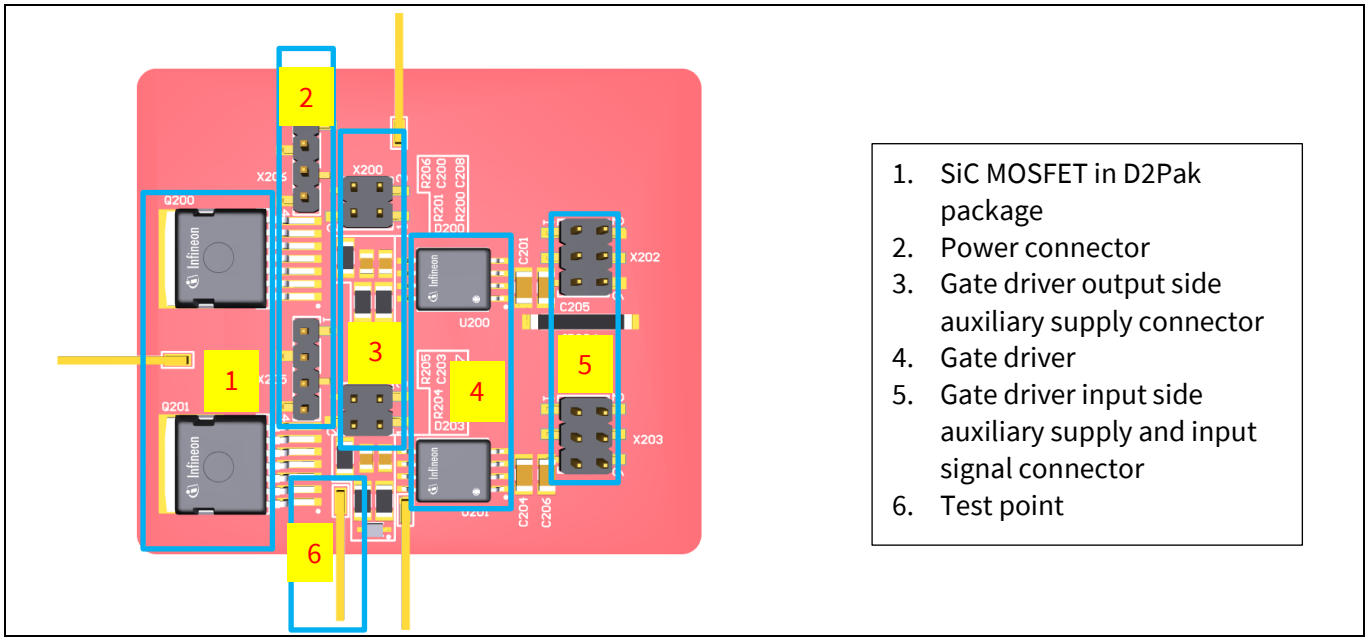


Figure 2 Bottom view of the daughter board

On the top side of the board, there are general descriptions of the SiC MOSFET and gate drivers, as well as indications for the test points from the top view, see Figure 3.

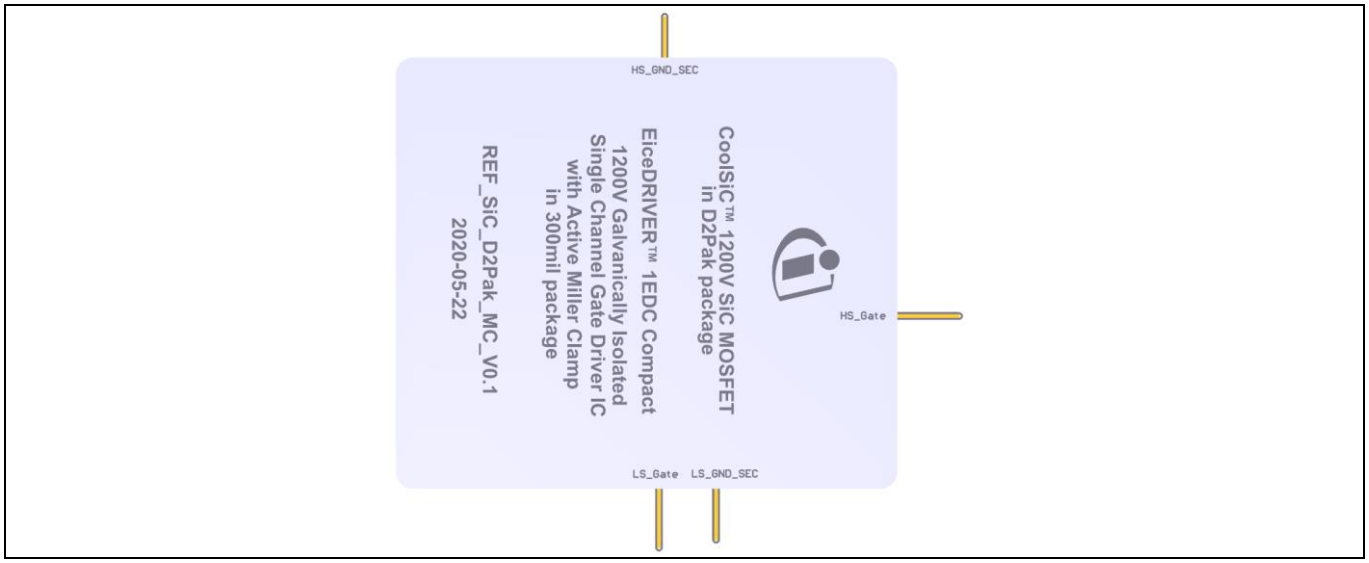
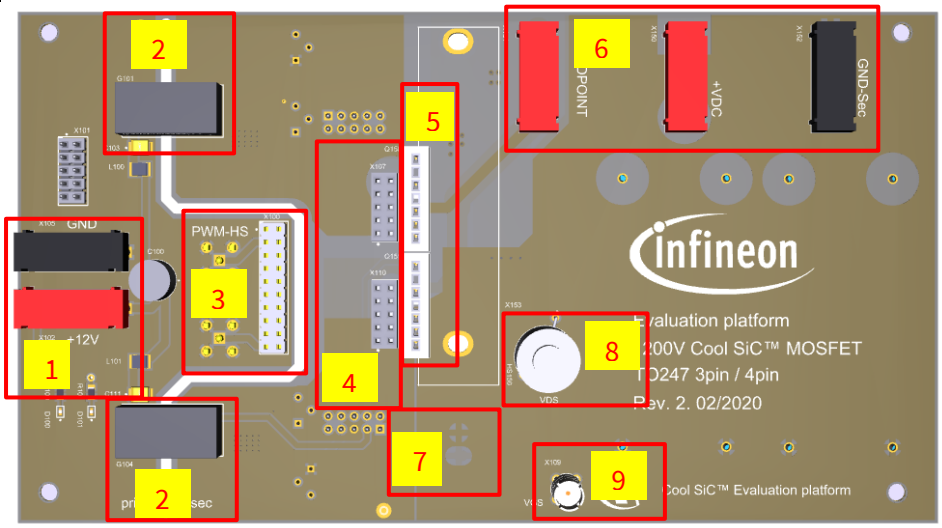


Figure 3 Top view of the daughter board

2.2 Install the daughter board onto the main board

The daughter board is intended for installation on the main board to share its power circuit, such as bus capacitors, power connectors, current sampling, probe sockets, etc.

The main board and its function blocks are displayed in Figure 4.



1. Auxiliary power supply input connector
2. 12 V-20 V isolated power converter
3. Supply and signal connector for input
4. Supply and signal connector for output
5. Socket for TO247 3-/4-pin
6. Power input connector
7. I_{DS} sensing pads
8. V_{DS} sensing probe socket
9. V_{GS} sensing probe socket

Figure 4 Top view of the main board

Insert the daughter board onto the main board until there is a firm contact.

Note: Make sure the pin-6 of X203 (or X303) on the daughter board mates the pin-19 of X100 on the main board, as indicated in Figure 5.

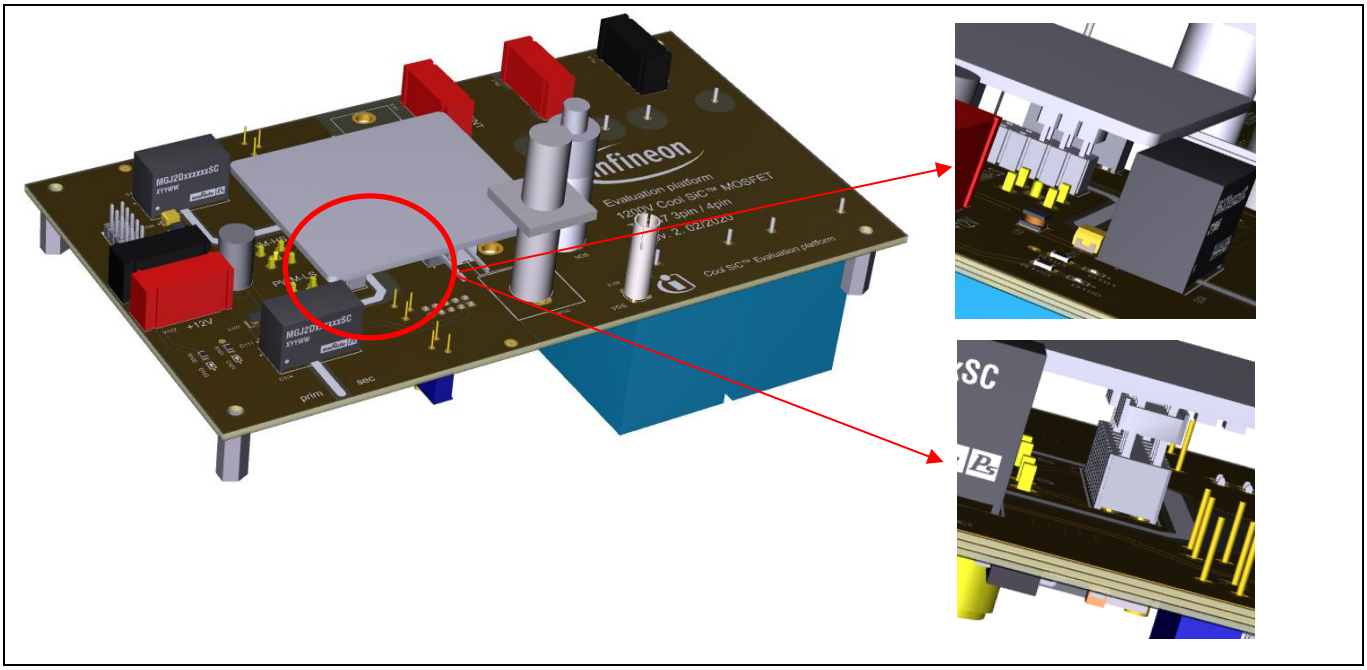


Figure 5 Install the daughter board onto the main board

2.3 Double pulse test setup

The double pulse test is set up as in Figure 6, with the necessary test equipment:

- The +800 V bus voltage is generated by an isolated DC voltage generator with the current limitation of 0.2 A.
- The external inductor value can be selectable, herein is 100 uH.
- The +12 V is powered by another isolated DC voltage generator with the current limitation of 0.2 A.
- When one side SiC MOSFET is in switching, the other side PWM input must be kept in low state. *The users can pull down the PWM input directly on the main board.*

  Note: DO NOT leave the PWM input floating to avoid any noise interferences at the input side.
- The MOSFET gate-source voltage (V_{GS}) is measured by an isolated differential voltage probe.
- The MOSFET drain-source voltage (V_{DS}) is measured by a non-isolated high voltage probe.

  Note: The V_{DS} probe should endure a voltage larger than 1200 V.
- The MOSFET drain-source current (I_{DS}) is measured by a Pearson current probe.

  Note: The I_{DS} can also be sensed by a shunt resistor. A coaxial shunt with BNC connector is preferred.
- The oscillation scope with high band width (BW), at least 1 GHz is preferred.

  Note: The oscillation scope should be well grounded in the test to prevent any electrical shock to the users.

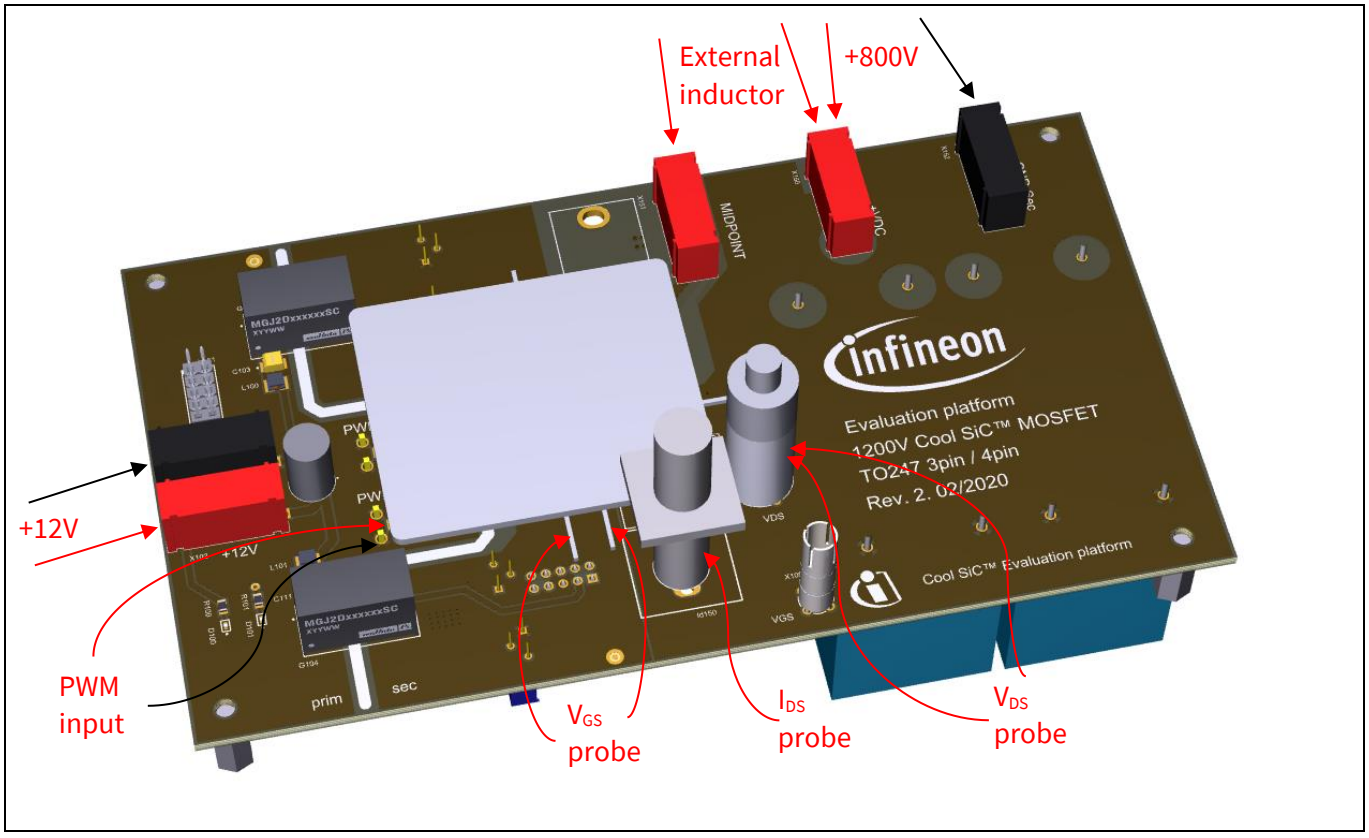


Figure 6 The double pulse test setup

Before power-on, the user has to double check the following items:

- The polarities of the +800 V, +12 V and PWM input signals are correct.
- The daughter board are installed correctly, as illustrated in Figure 5. Any mismatch of the pin headers and pin sockets may cause board damage.
- The double pulse width should be well tuned to make sure the peak I_{DS} is within the SiC MOSFET's specification.

- The DC bus voltage does not exceed 800 V.
- The PWM input is pulled down to low level when the other side SiC MOSFET is in switching.

2.4 Test waveforms of the daughter boards

For REF_SiC_ D2Pak _MC_V0.1, the turn-on gate resistor R_{gon}=10 Ω, whereas the turn-off gate resistor R_{goff}=4.7 Ω.

Figure 7 and Figure 8 illustrate the turn ON/OFF behaviors of the MOSFET. Rings on the waveform are caused by the parasitic inductances in system.

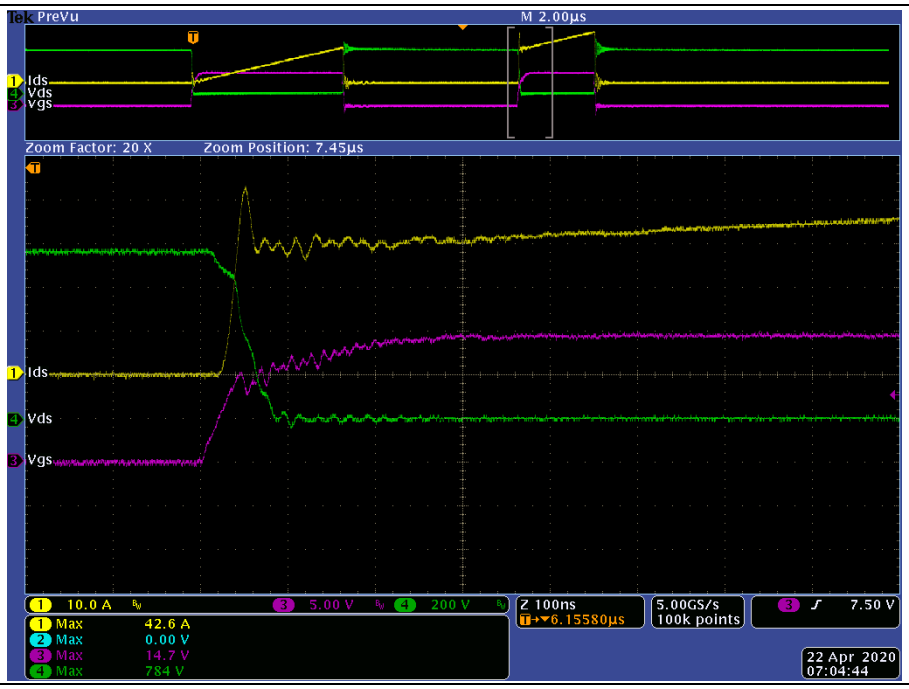


Figure 7 Turn-on of the REF_SiC_ D2Pak _MC_V0.1

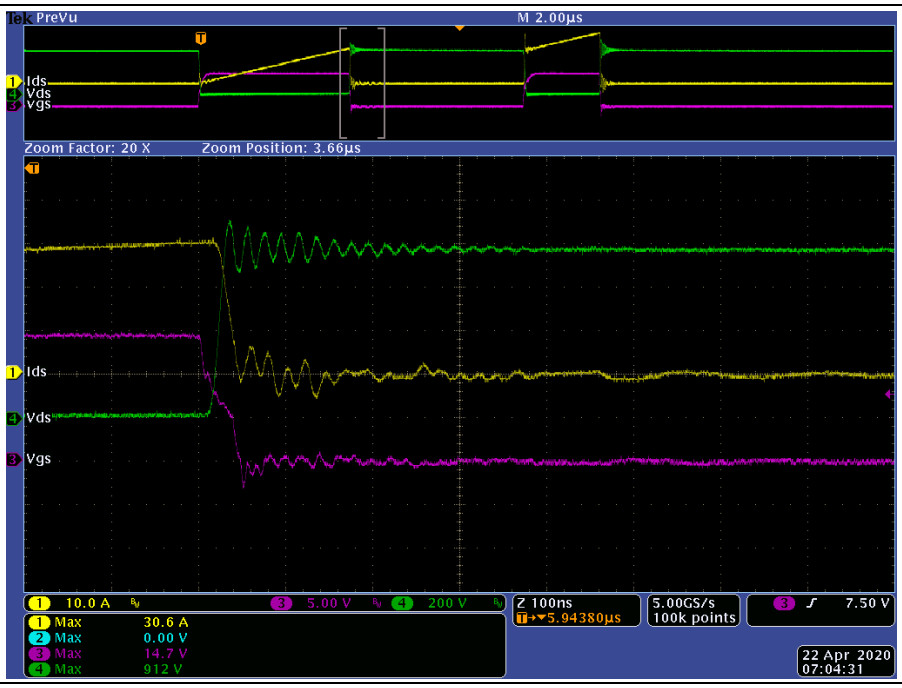


Figure 8 Turn-off of the REF_SiC_ D2Pak _MC_V0.1

The turn ON/OFF waveforms of the REF_SiC_ D2Pak _BP_V0.1 are shown in Figure 9 and Figure 10, with R_{gon}=R_{goff}=10 Ω.

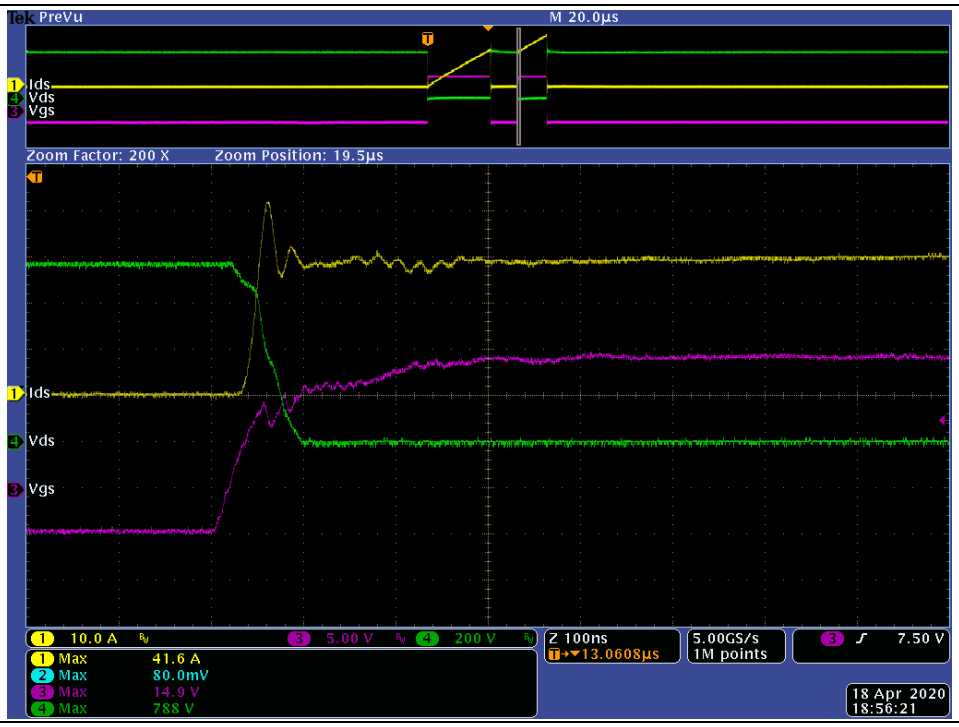


Figure 9 Turn-on waveform of the REF_SiC_ D2Pak _BP_V0.1

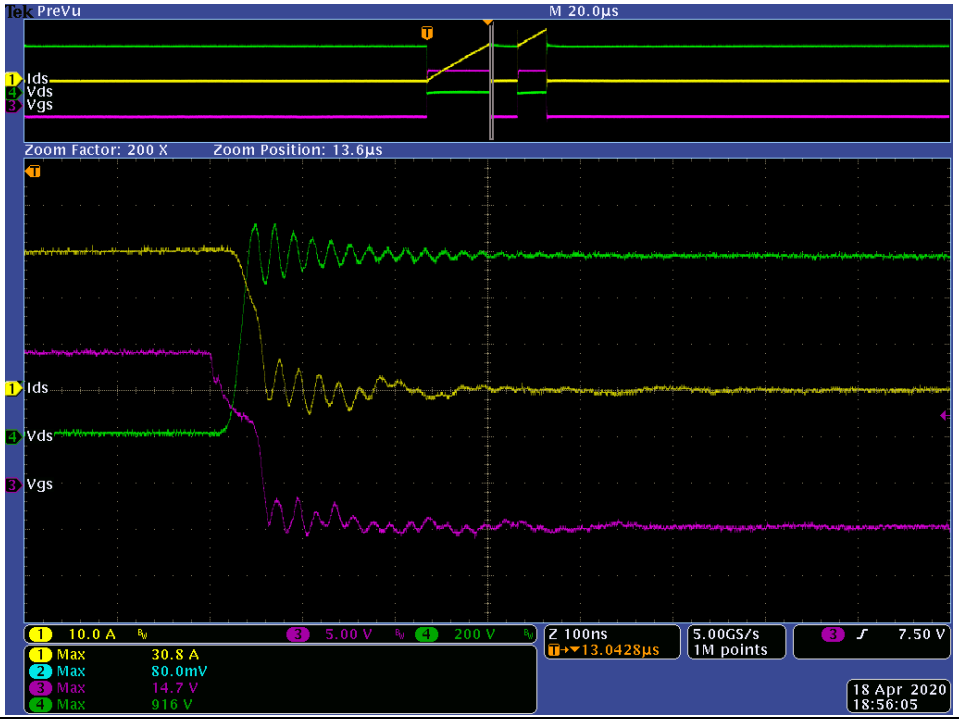


Figure 10 Turn-off waveform of the REF_SiC_ D2Pak _BP_V0.1

3 Details of the schematics, layout and BOM

3.1 Schematic of the daughter boards

The schematics of the REF_SiC_ D2Pak _MC_V0.1 and REF_SiC_ D2Pak _BP_V0.1 are shown in Figure 11 and Figure 12, respectively.

Note: The high-side MOSFET source and low-side MOSFET drain are not connected on the daughter board, and are to be shorted after installation on the main board.

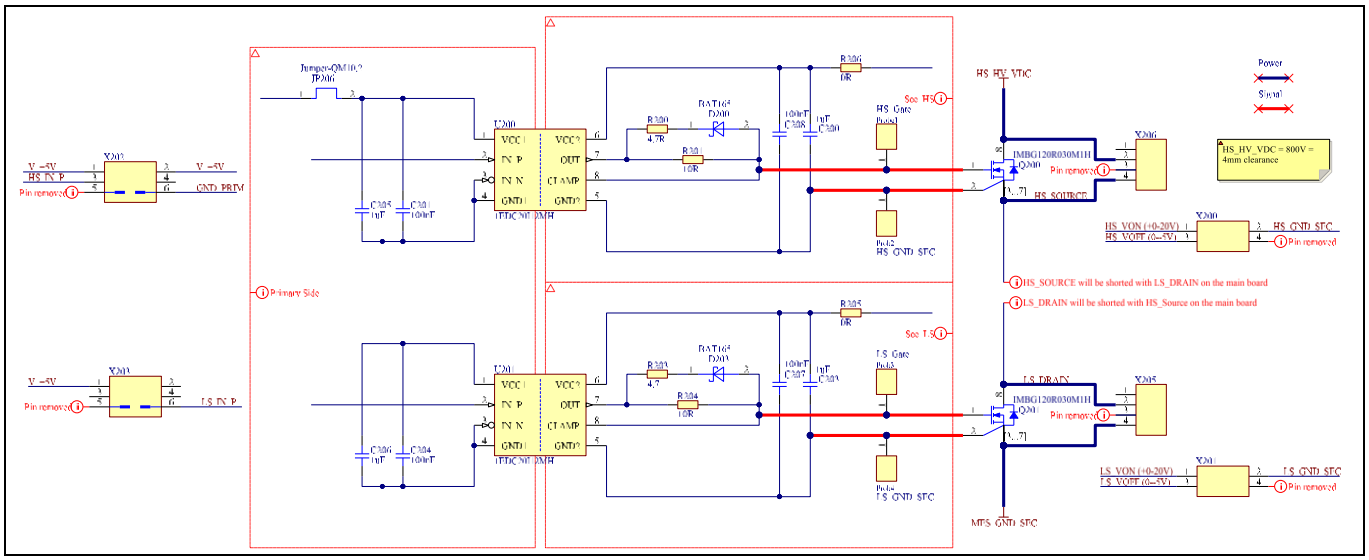


Figure 11 Schematic of the REF_SiC_ D2Pak _MC_V0.1

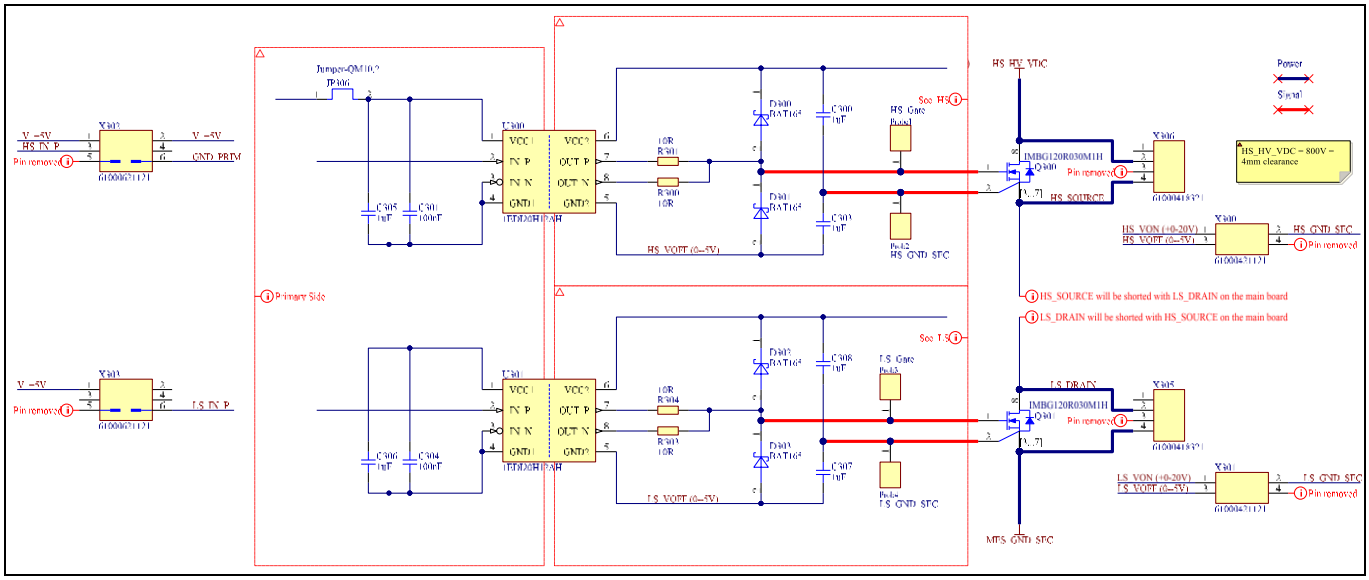


Figure 12 Schematic of the REF_SiC_ D2Pak _BP_V0.1

3.2 Layout of the daughter boards

The layout of the REF_SiC_ D2Pak _MC_V0.1 and REF_SiC_ D2Pak _BP_V0.1 are depicted in Figure 13 and Figure 14, respectively. Only the bottom layer is shown here, since the boards are single-layer.

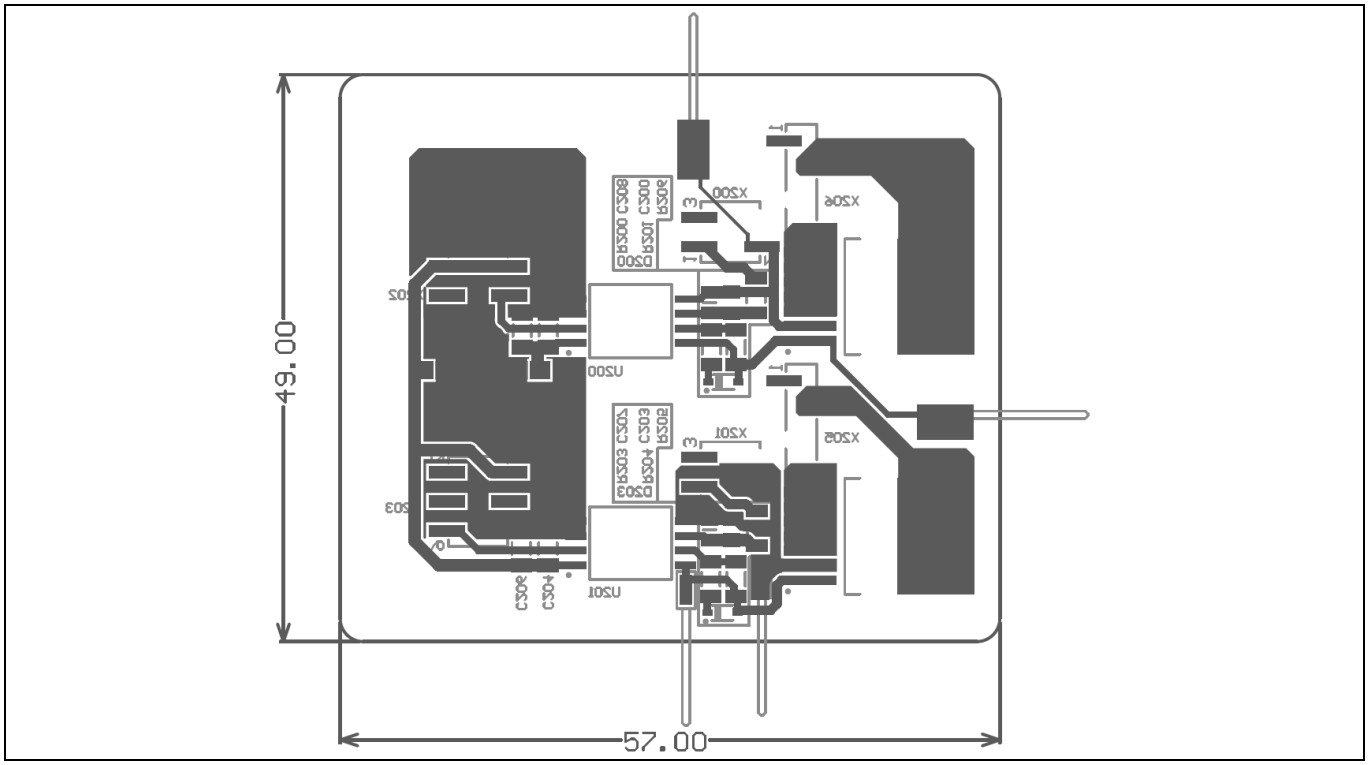


Figure 13 Layout of the REF_SiC_ D2Pak _MC_V0.1

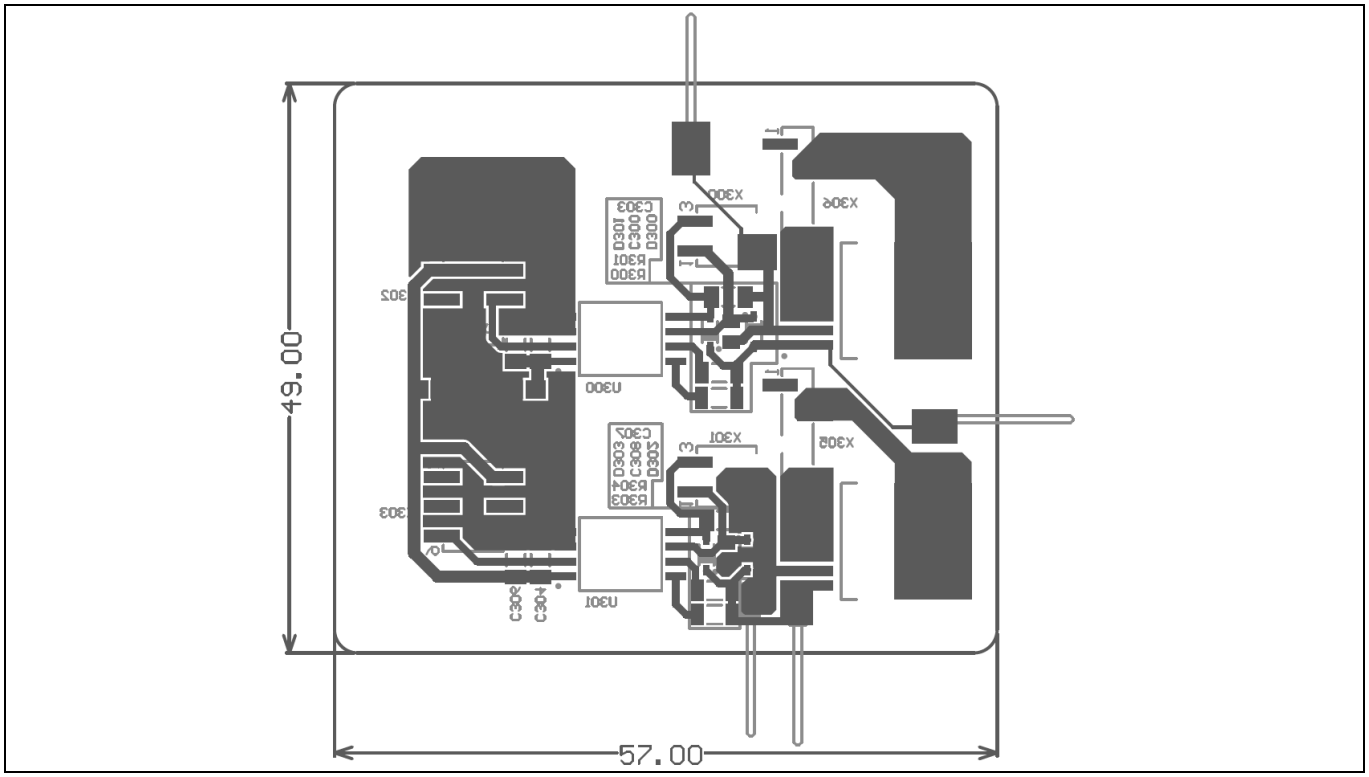


Figure 14 Layout of the REF_SiC_ D2Pak _BP_V0.1

3.3 Layout tips

Here are some layout guidelines that were applied on the daughter boards:

- The gate driver and the MOSFET are placed close together, thus the drive loop is as small as possible.
- The power traces are set as thick as possible.
- The creepage distance of the IMS board is more difficult to achieve than the regular PCB with FR-4 material, since the base of the IMS board is conductive. For these daughter boards, the creepage distance between primary and secondary circuit is at least 7.62 mm (300 mil wide body package of the gate driver), while between the high and low voltage in the secondary circuit it is at least 4.0 mm due to the limitation of the SMD pin-headers. That is why the board is defined to work at the maximum bus voltage of 800 V.
- The pads of the SMD pin-headers are as large as possible to increase the peel strength.

3.4 Bill of material of the daughter boards

The complete bill of material is available on the download section of the Infineon homepage. A log-in is required to download this material.

Table 3 BOM of the REF_SiC_ D2Pak _MC_V0.1

Quantity	Ref designator	Description	Manufacturer	Manufacturer P/N
2	C200, C203	CAP SMD CER 1 µF 50 V X7R 0805	Yageo	CC0805KFX7R9BB105
2	C205, C206	CAP SMD CER 1 µF 50 V X7R 1206	Yageo	CC1206KFX7R9BB105
2	C201, C204	CAP SMD CER 0.1 µF 50 V X7R 1206	Yageo	CC1206KPX7R9BB104
2	C207, C208	CAP SMD CER 0.1 µF 50 V X7R 0805	Yageo	CC0805KPX7R9BB104
2	D202, D203	Schottky diode 40 V 750 mA SOD323	Infineon	BAT165
1	JP206	Jumper SMT	Dongguan Qin Min	QM10.2
2	Q200, Q201	30 mΩ 1200 V SiC MOSFET D2Pak	Infineon	IMBG120R030M1H
2	R205, R206	RES SMD 0 Ω 1% 1206	Yageo	RC1206JR-070RL
2	R201, R204	RES SMD 10 Ω 1% 1206	Yageo	RC1206FR-0710RL
2	R200, R203	RES SMD 4.7 Ω 1% 1206	Yageo	RC1206FR-074R7L
2	U200, U201	Single channel galvanically isolated gate driver IC 2.0 A 1200 V Miller clamp 300 mil DSO-8	Infineon	1EDC20I12MH
2	X200, X201	Pin header 2.54 mm pitch 4-pin vertical double row SMT	Wurth	61000421121
2	X202, X203	Pin header 2.54 mm pitch 10-pin vertical double row SMT	Wurth	61000621121
2	X205, X206	Pin header 2.54 mm pitch 4-pin vertical single row SMT	Wurth	61000418321

Table 4 BOM of the REF_SiC_D2PAK_BP_V0.1

Quantity	Ref Designator	Description	Manufacturer	Manufacturer P/N
2	C300, C308	CAP SMD CER 1 µF 50 V X7R 0805	Yageo	CC0805KFX7R9BB105
4	C303, C307, C305, C306	CAP SMD CER 1 µF 50 V X7R 1206	Yageo	CC1206KFX7R9BB105
2	C301, C304	CAP SMD CER 0.1 µF 50 V X7R 1206	Yageo	CC1206KPX7R9BB104
4	D300, D301, D302, D303	Schottky diode 40 V 750 mA SOD323	Infineon	BAT165
1	JP306	Jumper SMT	Dongguan Qin Min	QM10.2
2	Q300, Q301	30 mΩ 1200 V SiC MOSFET D2Pak	Infineon	IMBG120R030M1H
4	R300, R303, R301, R304	RES SMD 10 Ω 1% 1206	Yageo	RC1206FR-0710RL
2	U300, U301	Single channel galvanically isolated gate driver IC 2.0 A 1200 V bipolar supply 300 mil DSO-8	Infineon	1EDI20H12AH
2	X300, X301	Pin header 2.54 mm pitch 4-pin vertical double row SMT	Wurth	61000421121
2	X302, X303	Pin header 2.54 mm pitch 10-pin vertical double row SMT	Wurth	61000621121
2	X305, X306	Pin header 2.54 mm pitch 4-pin vertical single row SMT	Wurth	61000418321

4 References

[1] Infineon Technologies AG: AN_1801_PL52_1801_132230, PCB layout guidelines for MOSFET gate driver, Online

[2] Infineon Technologies AG: 1EDI20H12AH and 1EDC20I12MH datasheet, Online

[3] Infineon Technologies AG: IMBG120R030M1H datasheet

[4] Infineon Technologies AG: AN2017-04, Advanced Gate Drive Options for Silicon Carbide (SiC) MOSFETs using EiceDRIVER™, Online

[5] Infineon Technologies AG: Application Note AN2019-28 1200 V CoolSiC™ MOSFET in TO-247 3-/4-pin evaluation platform

Table 5 Abbreviations

Abbreviation	Meaning
SiC	Silicon Carbide
IMS	Insulated Metal Substrate
MC	Miller Clamp
BP	Bipolar
DC	Direct Current
EMI	Electromagnetic interference
UL	Underwriters Laboratories
ASTM	American Society of Testing Materials

Revision history

Document version	Date of release	Description of changes
1.0	2020-09-01	First release
2.0	2020-10-15	Add one item on the double pulse setup in section 2.3. Add '*Note: DO NOT leave the PWM input floating to avoid any noise interferences at the input side' in section2.3.*

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