User guide
REF-GPD30KN3T4M5
Infineon Reference Design Kit for drives - power board for 30 kW GPD and CAC applications

About this document

In order to support customers' new applications and new product development, Infineon developed a series of boards under a new platform called the Infineon Reference Design Kit (RDK) for drives. Under this kit, a generic-hardware power board built around a power module, a separate control board and a suitable auxiliary power supply have been developed, tested and can be shared with the customer. The control board and auxiliary power supply interfaces are intended to be common across the platform. Presently, RDK featured functionalities are tailored to the industry applications like general purpose drives (GPD), commercial air conditioners (CAC) and servo drives. Its subsystems and design ideas can be applied elsewhere.

In this kit, Infineon offers the complete design details of the project, which includes the BOM, the schematics, the PCB files and any firmware if applicable.

This particular document specifically describes the details of the power board, which is based on the PIM modules FP150R12KT4 or FP100R12KT4 and the EiceDRIVER™ 2ED020I12-F2 gate-driver IC. Separate documents are available for the control board and auxiliary power supply.

The auxiliary supply board and different power board variants shall provide implementation ideas, giving customers a valuable starting point for their design. By enabling re-use of either one specific functional block or the combination of a multitude of blocks, design efforts and design risks will be reduced on the customer side. The design and layout as well as the selection of passive components on all the boards was performed with a strong focus towards industry oriented design.

Scope and purpose

- To provide a platform for engineers who are looking for implementation ideas in the field of GPD and CAC
- To explain the bootstrap power supply implementation and desaturation circuit implementation for a large power module
- To evaluate proper operation of the pre-charge circuit to protect the input rectifier from damage
- To provide details on safe torque-off protection implementation
- To provide a design guideline for engineers working in GPD and CAC applications
- To provide a generic power board, along with control board and auxiliary power supply, so that customers can start the testing
- To provide a well-defined control interface to the power board. This is useful when other microcontrollers from Infineon or microcontrollers from different suppliers are to be used

Intended audience

Development, design and qualification engineers working on GPD and CAC.

1. Important Notice

The Evaluation Boards and Reference Boards as well as the information in this document are solely intended to support designers of applications in evaluating the use of products from Infineon Technologies for their intended applications.

Environmental conditions have been considered in the design of the Evaluation Boards and Reference Boards provided by Infineon Technologies. The design of the Evaluation Boards and Reference Boards has been tested by Infineon Technologies only as described in this document. The design is not qualified in terms of safety requirements, manufacturing and operation over the entire operating temperature range or lifetime.

The Evaluation Boards and Reference Boards provided by Infineon Technologies are subject to functional testing only under typical load conditions. Evaluation Boards and Reference Boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD).

Evaluation Boards and Reference Boards are not commercialized products, and are solely intended for evaluation and testing purposes. In particular, they shall not be used for reliability testing or production. The Evaluation Boards and Reference Boards may therefore not comply with CE or similar standards (including but not limited to the EMC Directive 2004/EC/108 and the EMC Act) and may not fulfill other requirements of the country in which they are operated by the customer. The customer shall ensure that all Evaluation Boards and Reference Boards will be handled in a way which is compliant with the relevant requirements and standards of the country in which they are operated.

The Evaluation Boards and Reference Boards as well as the information provided in this document are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document and in other related documentation supplied with the respective Evaluation Board or Reference Board.

It is the responsibility of the customer's technical departments to evaluate the suitability of the Evaluation Boards and Reference Boards for the intended application, and to evaluate the completeness and correctness of the information provided in this document with respect to such application.

The customer accepts that the Evaluation Boards and Reference Boards are not intended to be used in life-endangering applications such as medical, nuclear, military, life-critical or other applications, where failure of the Evaluation Boards and Reference Boards, or any results from the use thereof, can reasonably be expected to result in personal injury.

The Evaluation Boards and Reference Boards and any information in this document is provided "as is" and Infineon Technologies disclaims any warranties, express or implied, including but not limited to warranties of non-infringement of third party rights and implied warranties of fitness for any purpose, or for merchantability.

Infineon Technologies shall not be responsible for any damages resulting from the use of the Evaluation Boards and Reference Boards and/or from any information provided in this document. The customer is obliged to defend, indemnify and hold Infineon Technologies harmless from and against any claims or damages arising out of or resulting from any use thereof.

Infineon Technologies reserves the right to modify this document and/or any information provided herein at any time without further notice.

2. Safety precautions

In addition to the precautions listed throughout this manual, please read and understand the following statements regarding hazards associated with development systems.

Table 1 Safety Precautions

	***Attention: Infineon Reference Design Kit for drives - power board for 30 kW GPD and CAC Applications is connected to the grid input during testing. Hence while measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.***
	***Attention: Only personnel familiar with the drive, power electronics and associated machinery should plan or implement the installation, start-up and subsequent maintenance of the system. Failure to comply may result in personal injury and/or equipment damage.***
	***Attention: The heat sink and IGBT module surfaces of the power board may become hot during testing. Hence necessary precautions are required while handling the board, failure to comply may cause injury.***
	***Attention: Infineon Reference Design Kit for drives - power board for 30 kW GPD and CAC Applications contains parts and assemblies sensitive to Electrostatic Discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing this assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to applicable ESD protection handbooks and guidelines.***
	***Attention: A drive, incorrectly applied or installed, can result in component damage or reduction in product lifetime. Wiring or application errors such as under sizing the motor, supplying an incorrect or inadequate AC supply or excessive ambient temperatures may result in system malfunction.***
	***Attention: Infineon Reference Design Kit for drives - power board for 30 kW GPD and CAC Applications is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials which are unnecessary for system installation may result in overheating or abnormal operating condition.***

3. Table of contents

4. The power board at a glance

This kit is targeted to the commercial air conditioners (CAC) and general purpose drives (GPD) market. To enable the customer to use the kit in these applications, the power board is provided with IGBT power module with gate driver, short-circuit protection, voltage and current-sensing circuits, and safe torque-off (STO) protection circuit. In addition, the board includes the necessary input and output power terminations, control board and auxiliary power supply terminations as well as heat-sink mounting terminals.

This section briefly describes key Infineon components used in this board and the specifications, features and benefits of the power board.

4.1 Power module - FP150R12KT4 and FP100R12KT4

Power modules FP150R12KT4 / FP100R12KT4 are EconoPIM™3 modules using Trench-Fieldstop IGBT4 technology. The footprint of FP150R12KT4 is a superset of FP100R12KT4, which means by doing a PCB for a 150 A module, a 100 A module can be accommodated in the same footprint. The footprint in the PCB has been considered for the standard module, however, the component keep-out area is considered for the PressFIT module. Hence, it is easy for the customer to modify the drill-hole dimensions to suit PressFIT modules without disturbing the placement and routing.

4.2 EiceDRIVER™ - 2ED020I12-F2

The Infineon coreless transformer-based IGBT dual-channel driver EiceDRIVER™ - 2ED020I12-F2 is used to drive the IGBT module. The dual channel driver used here is functionally isolated. However the complete logic and the µC – board is connected to DC bus negative, hence the functional isolation of the driver is not utilized i.e. the driver is used like a level shift driver.

The complete details of the IGBT modules and gate driver are available in their respective datasheets. They may be referred to for further information.

4.3 Specifications of the board

Table 2 displays the specifications of this board.

Table 2 Specifications of the board

Parameter	Symbol	Min.	Nominal	Max.	Unit
Input AC voltage phase to phase	V_{in}	360	400	528	V
Phase current FP150R12KT4 module	I_{Load}		60	90	A
Phase current FP100R12KT4 module	I_{Load}		40	60	A
Power dissipation of the module [1]	P_{Loss}			1500	W
DC bus voltage	V_{DC}	520		750	V
Switching frequency	fs		4	10	kHz
Humidity		5		95	%RH
Operating temperature	T_{op}	-25	25	50	°C
Storage temperature	T_s	-25	25	50	°C
Input voltage range in +15 V	V_{+15V}	14.8	15	15.2	V
Input supply current +15 V	I_{+15V}		1		A
Input voltage range -15 V	V_{-15V}	-14.8	-15	-15.2	V
Input supply current -15 V	I_{-15V}		0.5		A
Input voltage range in +5 V	V_{+5V}	4.8	5	5.2	V
Input supply current +5 V	I_{-5V}		0.6		A
Blanking time – short-circuit protection			3.6		µs

[1] Appropriate cooling required. Section 7.6 provides further details of thermal management.

4.3.1 PCB details

Figure 1 shows the power board. The dimensions of the board are 281 mm by 230 mm. The PCB size is not optimized in terms of total required area but in terms necessary PCB space surrounding specific ICs or specific functionalities. This design has been enlarged intentionally to enable easy access of the testing points, and to allow comfortable handling during testing.

The PCB is made of FR4 material with a thickness of 2.1 mm. This platform focusses strongly on typical industry design and applications; hence, FR4 material is used. This PCB is a four-layered PCB. Stack-up details of the PCB are provided in Table 3. Outer and inner layers are of 105 µm copper thickness. Usually 10% tolerance is seen in the overall thickness.

Table 3 Stack up details of the PCB (units in mm)

Solder mask top	0.05
Top copper layer	0.105
Dielectric	0.280
Internal top copper layer	0.105
Core	1.28
Internal bottom copper layer	0.105
Dielectric	0.280
Bottom copper layer	0.105
Solder mask bottom	0.05

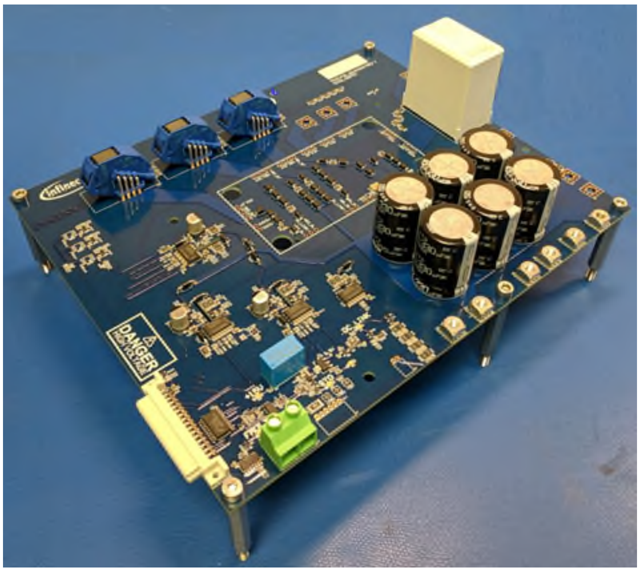

Figure 1 Power board based on FP150R12KT4/FP100R12KT4 and EiceDRIVER™-2ED020I12-F2

4.4 Features and benefits of the board

The features and benefits of this power board are as follows:

- The board is equipped with EiceDRIVER™ drivers, high-side drivers' power supply via bootstrap, short-circuit protection using desaturation detection, and a well-tuned gate resistor suiting both the modules.

This feature provides a compact, low-cost alternative to level-shifter designs using functionally isolated driver ICs.

- DC-link electrolytic capacitors are mounted on-board with the provision to mount additional capacitors via external termination. This enables the user to perform double pulse tests and limited power load tests with well-defined DC-link stray inductance.
- The board is provided with a suitable DC-link, pre-charge circuit that is controlled via microcontroller control interface. This enables a good pre-charge solution, protecting the rectifier during initial DC-link charging as well as in recharging DC link after voltage sags according to IEC 61000-4-11, [7].
- Safe torque-off feature can be used in GPD applications providing redundant channels as well as feedback.
- Conveniently scaled voltage-sensing circuit to interface directly with control board. This enables the control board to be used directly for inverter control and for the control of the pre-charge circuit.
- On-board phase-current sensing via open-loop, Hall-effect sensor provides a cost-effective standard solution as used in many designs in this power range.
- Properly tested heat sink is suggested for this setup. This will help the engineer when using continuous loading operation.
- LED indication provided in the board will help during lab testing.
- All the signals to the microcontroller are suitably scaled and clamped to +3.3 V logic level so that the board is compatible with modern microcontrollers.
- Exclusive connector for auxiliary power supply. This allows adaption for several different devices used in the auxiliary supply, or to implement the alternate sources for auxiliary power, e.g. auxiliary power from 24 V via isolated DC/DC.
- Suitable provision to enable testing of brake control is provided in the board for connecting braking resistor.

4.5 A note on the control board and auxiliary power supply

Infineon provides a control board that matches the functional requirements of this power board. The control board is based on XMC4400, see Reference no. [4] for further information. The power board termination is designed to match the control board termination.

Regarding the Auxiliary Power Supply (APS), customers may approach Infineon Technologies for additional information. The auxiliary power supply is based on CoolSiC™ IMBF170R1K0M1 and is a common power supply across Infineon RDK. The power board termination is designed to match the APS termination.

5. Architecture of the power board

This section briefly provides the details of the architecture of the board. Figure 2 provides the signal flow of the power board, and components of the IGBT module are marked.

In Figure 2, the three-phase input to rectifier is marked as L1, L2 and L3. Rectified three-phase voltage is sensed through a resistor divider network to provide the signal AC SNS, which is used to sense the voltage before the relay. A relay with a pre-charge PTC isolates the rectifier output from the DC link of the system. The input relay is controlled by RLY_IP with a suitable driver circuit.

A DC-filter inductor is not part of the power board as its use is optional, but proper terminals are provided for the customer to decide appropriately. The capacitor bank is a series-parallel combination of electrolytic capacitors to meet voltage and capacitance requirements. The power board is also provided with voltage-balancing resistors for the capacitor bank. In addition to the on-board capacitors, the customer can still connect additional capacitors.

The dynamic braking resistor RB dissipates the regenerated energy when the chopper IGBT is controlled. Although the dynamic braking resistor is not part of the PCB, suitable terminals are provided to enable the customer to connect externally.

Each inverter half bridge uses an EiceDRIVER™ 2ED020I12-F2 and each channel of the driver has a reset signal (RST), fault signal (FLT), ready signal (RDY) and gate pulse signal. Reset signals for all the driver ICs are merged together to form a common RST signal, likewise with the RDY and /FLT signals.

Phase currents IU+, IV+ and IW+ are sensed via the Hall-effect current sensor.

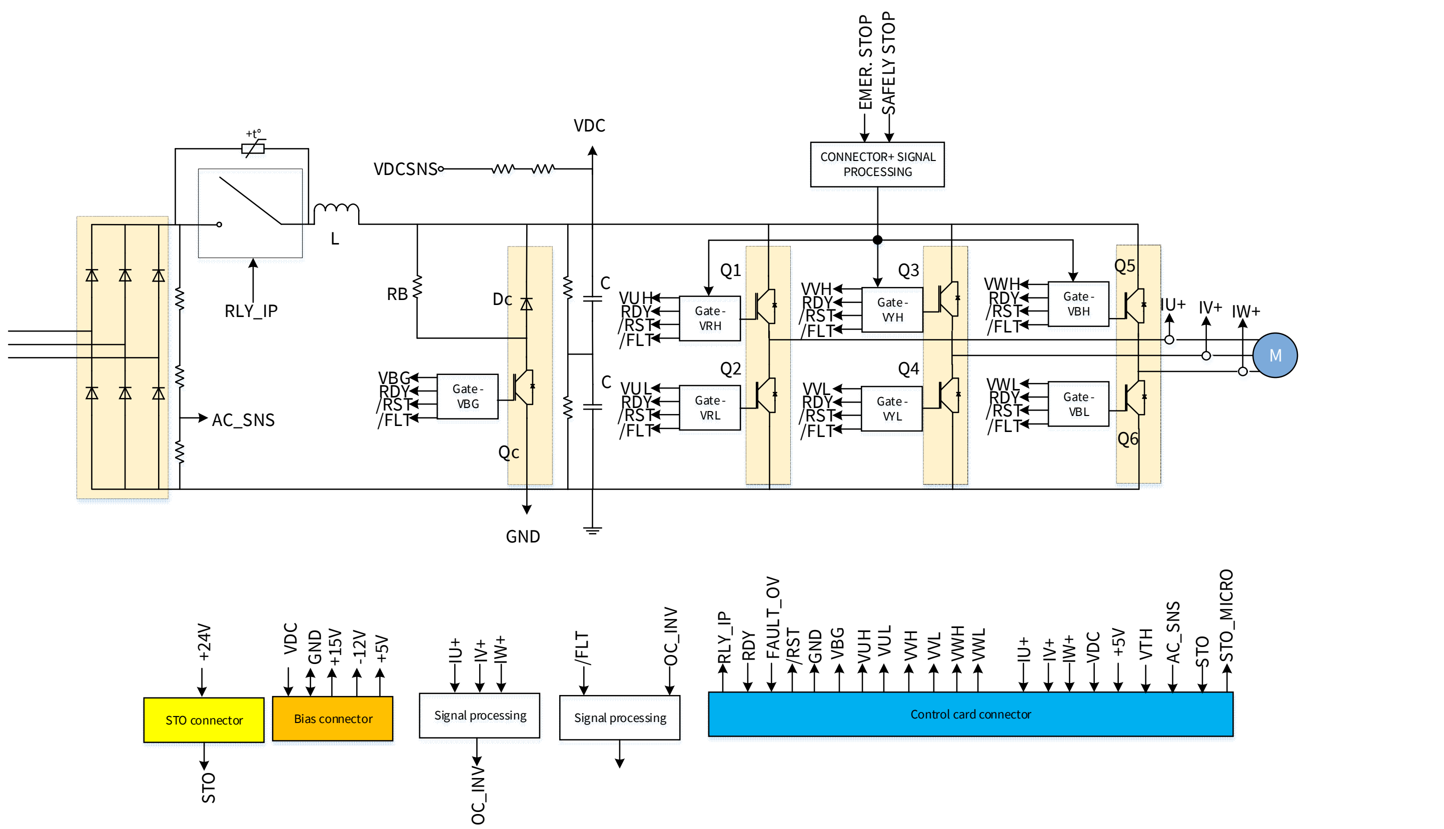

Figure 2 Architecture of the power board

5.1 Safe torque-off

Safe torque-off (STO) is an important feature provided with this power board. STO can be related to general safety of the operator during starting, operation, shut down, and during servicing the mechanical part of the system. Modern GPDs are required to provide STO, as detailed in IEC 61800-5-2. The implemented circuit demonstrates a STO circuit with feedback of status from the disabled drivers. However for a certification based on IEC 61800-5-2 adaptions of the circuitry are required. It is the responsibility of the customer to change the circuitry and validate the STO.

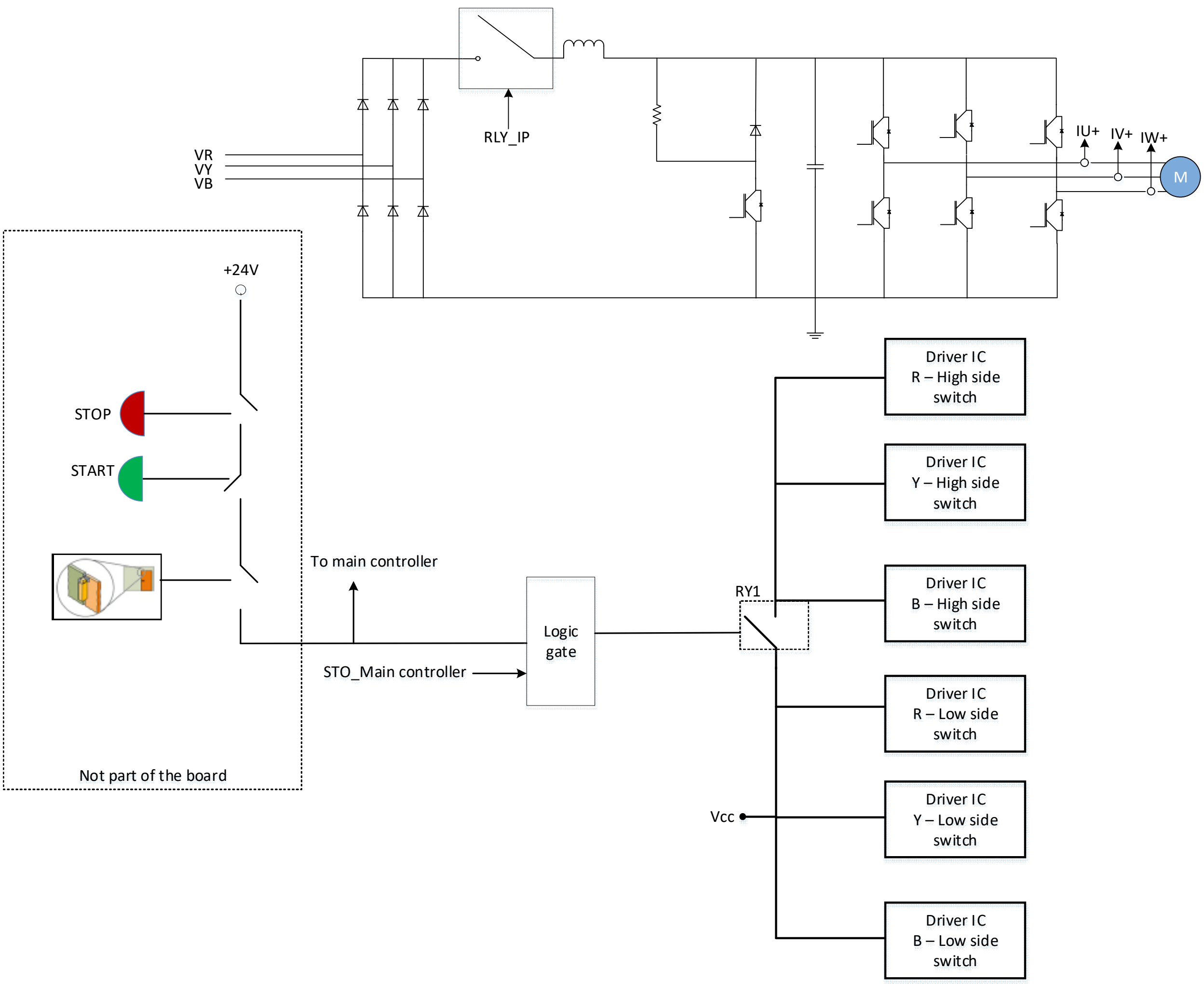

Figure 3 Signal flow of STO

Figure 3 shows the implementation logic and signal flow of STO. STO operates in +24 V logic input to be compatible to PLC (programmable logic controllers) as used in industrial control. STO logic input decides whether the motor should generate torque or not. In the absence of +24 V input, the motor will immediately stop generating torque.

Normally, the emergency shutdown or the stop signal, the start signal or additional protection signals are combined to trigger the STO signal. This STO signal controls the relay RY1 through a logic gate as in Figure 3. An additional input to the logic gate comes from the microcontroller, which will have additional information such as speed, direction of rotation, operating voltages and currents. Relay RY1 will block the power supply for the driver section of the high-side switches. Once the bootstrap power supply gets blocked, it will trigger the UVLO

function of the IGBT gate driver, which will block the gate pulses. The /RDY signal from the high-side driver might be used to acknowledge that this has taken place, i.e., STO is enabled. Without external torque, the motor will come to a standstill unless there is an external torque. Reference [1] can be referred to for additional details related to STO. For functions such as STOP, START and emergency stop, or any other additional protection, customers have to implement them externally, as they are not part of the board. However, provision is made to aid the protection mechanism. In addition, the STO protection mechanism should not succumb to single-point failure, i.e., it is expected to overcome single-point failure, and has to be highly reliable. Normally a combination of hardware and software logic is implemented for STO to protect the operator.

6. Theory of operation

This section provides the theory of operation of the power board. Finer aspects of the design, and details of the sub-circuits are explained in this section.

6.1 Gate driver IC

Infineon's EiceDRIVER[TM] 2ED020I12-F2 dual-gate driver is used in the power board. It is a galvanically isolated driver using coreless transformer technology, and can be used up to 1200 V class of IGBTs. It is advised to refer to the datasheet for complete details on the gate driver. In this design, the galvanic isolation of the driver IC ensures robustness against EMI and voltage spikes. Nevertheless due to the gate driver power supply circuit, the input side and output side are galvanically connected, i.e. the input and the output side are galvanically connected on the board, as control circuits referenced tho DC- is common in these applications.

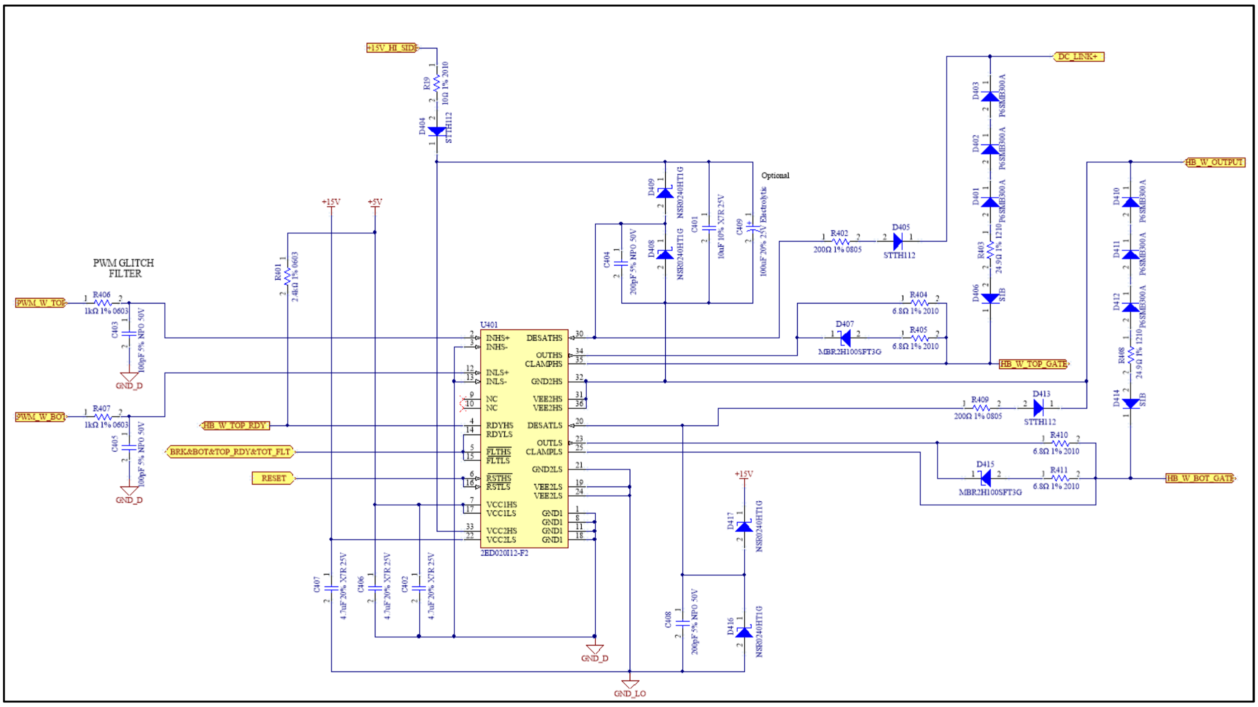

Figure 4 Gate driver circuit

Figure 4 provides the details of the gate driver circuit in the power board. As depicted in the figure, the bootstrap technique is used to power up the high-side switches. A combination of ceramic capacitor of 10 µF and an electrolytic capacitor of 100 µF is used in the bootstrap section. The board is provided with a gate resistor of 6.8 Ω for turn-on, and during turn-off it is 6.8 || 6.8 Ω. This ensures fast and reliable turn-off without negative gate voltage. For further reading, see the application notes in Reference [8]. Furthermore, the application note [11] can be referred to for additional information on designing bootstrap-side components.

Infineon's Schottky diode BAT165 is used in the gate driver section to protect the DESAT pin from negative voltage, and hence to avoid malfunction. Similarly for handling voltage spikes across the IGBT, 3 TVS diodes are used for active clamping. Active clamping is designed to protect against overvoltage spikes at overcurrent and short-circuit turn-off, but is not active for the nominal DC-link voltages up to 750 V and currents up to 150 A / 100 A based on the module. In this design, the TVS diodes' chain will clamp the voltage across the device during turn-off, and the clamping voltage is rated for a nominal value of 900 V. There are 4 gate driver ICs on board to drive 3

legs of the inverter, and the last one to drive the braking IGBT. Reset signals to all the driver ICs are merged together to form a common RST signal, the RDY and /FLT signals are treated likewise.

6.2 Input relay and DC bus

Figure 5 displays the input relay circuit K1 and DC bus capacitor bank. See Figure 2 to understand the position of the input relay in the circuit. The relay K1 contacts are rated for 100 A in parallel connection. PTCs are used to pre-charge the DC bus. It is mandatory to pre-charge the DC bus before the relay is turned on, as it prevents welding of relay contacts. Furthermore, a relay driving circuit is provided with a zener diode D2 and a freewheeling diode D1 to ensure fast turn-off. Proper control of the relay by the controller for pre-charging and voltage dips as well as fast reactivation of the pre-charging circuit is needed for initial charging at start-up as well as for reliable operation in the case of severe voltage fluctuations, see References [7] and [9]. It may be noted that the input relay is not intended for repetitive operation as PTC should not be operated continuously and have to be cooled down after every pre-charge operation.

The power board is designed to work with three-phase input up to 528 V (phase-to-phase RMS voltage) which corresponds to a DC bus voltage of 750 V. To manage such a high voltage, electrolytic capacitors are connected in series. Each electrolytic capacitor is rated for 450 V and 330 µF. In order to prevent a mismatch of voltages between the capacitors, suitable balancing resistors are used on board. Furthermore, customers can connect additional capacitors through terminals (T15, T7, T8, T9, T10, T16) provided on board. The board is also provided with a terminal T5 and T6, through which the customer can connect DC link inductor.

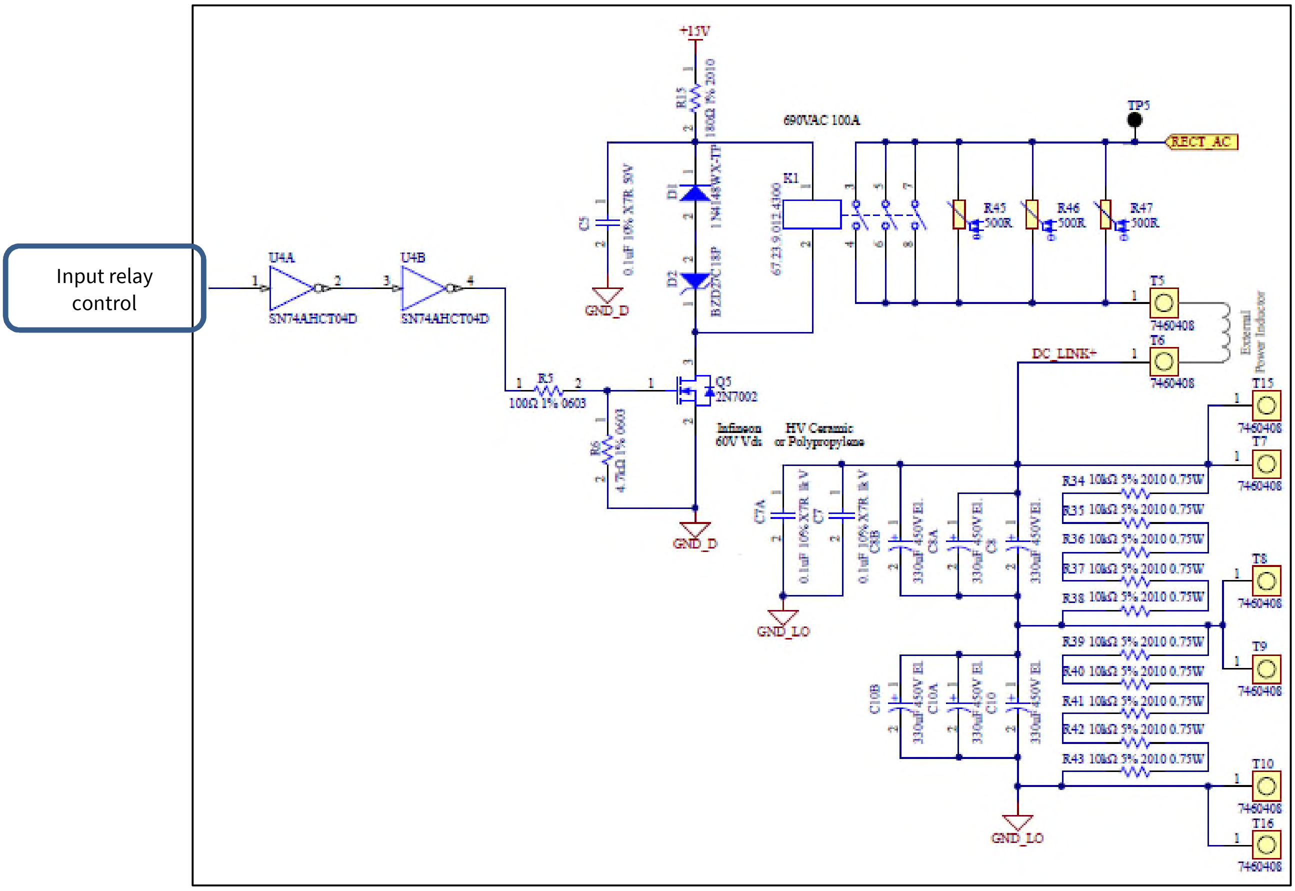

Figure 5 Input relay and DC bus

6.2.1 Selection of DC bus capacitor

The DC bus capacitor selection is based on output voltage ripple and capacitor ripple current. Instead of capacitor filter, LC filter is recommended at the output of the rectifier, as it can reduce the capacitor ripple component. Ideally the inductor when operating in continuous conduction mode, can reduce the capacitor ripple current.

6.3 Logic level shifter

Figure 6 presents the level-shifter circuit. PWM signals, braking signals and safe torque-off signals from the microcontroller with 3.3 V CMOS level are passed through the level shifter IC 74AHCT244D to enable them to drive the subsequent stage, which will handle 5 V CMOS logic signals.

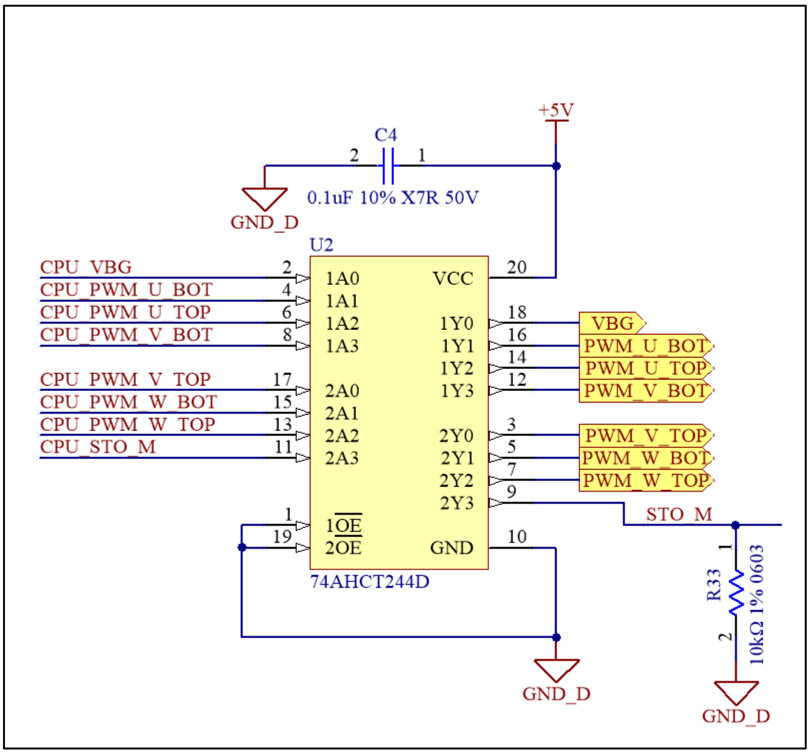

Figure 6 **Level-shifter circuit**

6.4 STO signals

Safe torque-off is explained in section 5.1, and its circuit implementation is depicted in Figure 7. Connector J4 can be used to merge the various protection signals from the external input based on individual requirements. Opto-isolator VO1 isolates this protection signal from the power board. The isolated signal STO_EXT_IN is also routed to the control board as in Figure 7. The microcontroller also generates an additional signal, STO_M based on the operating parameters. The signal from microcontroller STO_M is logically ANDed with STO_EXT_IN to control the relay which then controls the power supply for high-side switches. Additional provision is provided on board to bypass external signals via R7 and J5, which can be used during testing.

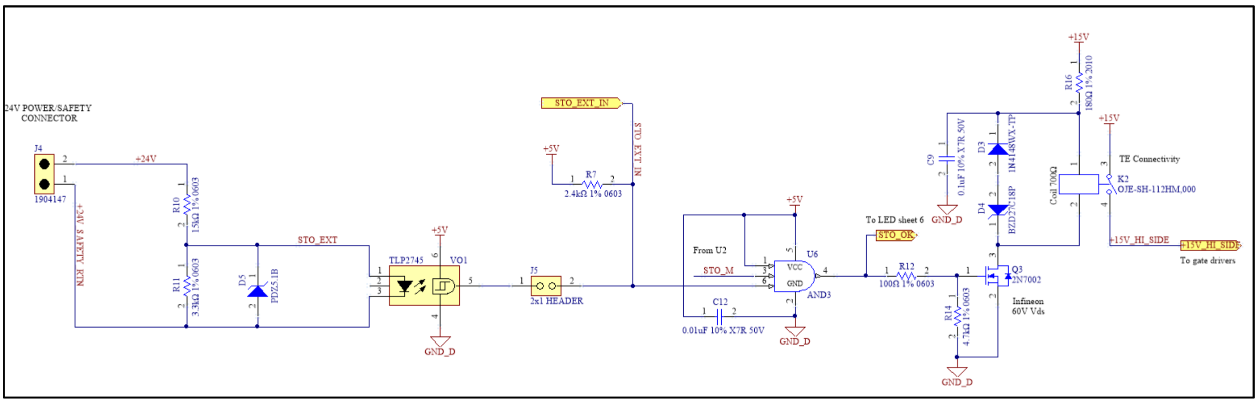

Figure 7 **STO signal**

6.5 HV sensing and indication circuit

Figure 8 indicates the high-voltage sensing and indication circuit. There are two HV sensing circuits: one for DC bus sensing and another one for rectifier output. Both sensing circuits have an attenuation of 200:1. In addition there are 3 green LEDs: D6, D7 and D9, which indicate the presence of +5 V, DC bus and +15 V. The DC bus indication starts working above 50 V.

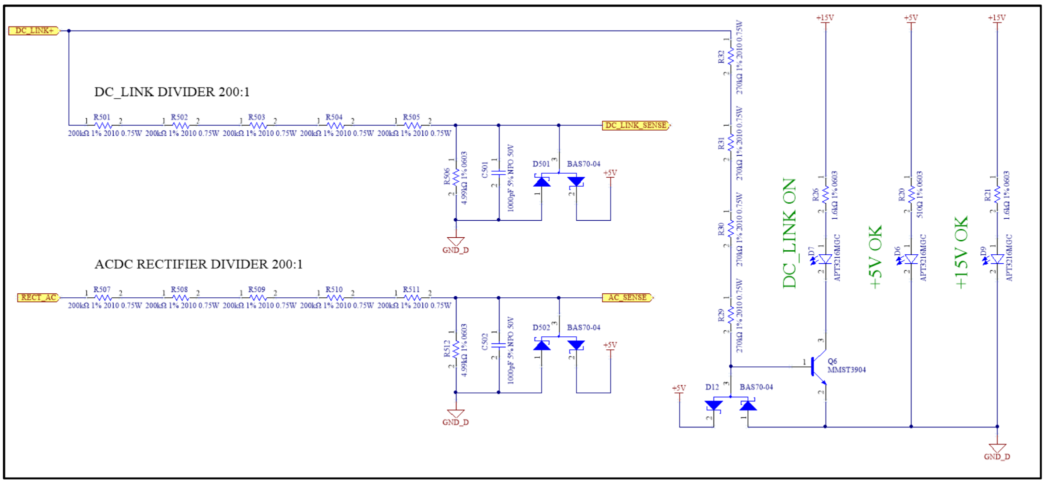

Figure 8 HV sensing and indication circuit

6.6 Current sensing and OC protection circuit

This section explains the details of the current-sensing circuit. There are three on-board current sensors for sensing the phase currents. The current sensor used here is HO 60-NP-0100, which can measure up to 60 A RMS and a peak current of +/- 150 A. The circuit is displayed in Figure 9. The current sensor works with a single supply voltage of +5 V. The current sensor output is amplified and filtered via an op-amp. The portion of the circuit shown in Figure 9 is for the R phase; the op-amp is U604 and the comparator is U603. The output of the op-amp is tied to a comparator circuit which generates the overcurrent fault signal "BRK&BOT&TOP_RDY&TOT_FLT" for phase currents above +/-100 A. The overcurrent trip point slightly drifts with operating voltage and temperature. Refer to [6] for further details on the current sensor. This fault signal is coupled with the gate-driver fault-signal line, which can shut down the gate pulses. This fault signal is also routed to a control card for additional protection.

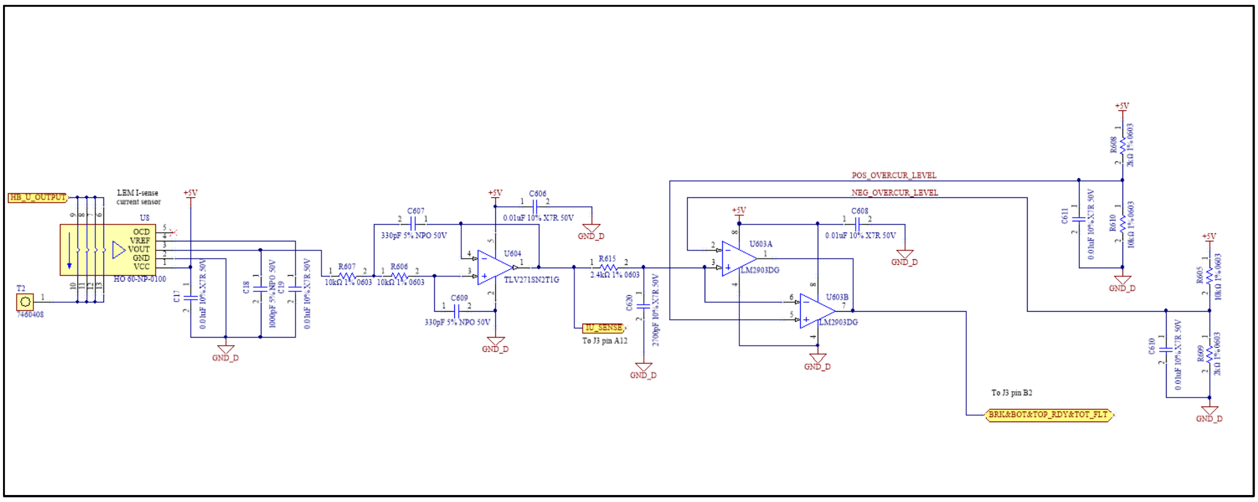

Figure 9 Current sensing and OC protection circuit

6.7 NTC sensing circuit

The power board uses a voltage divider network to sense the voltage across the NTC as in Figure 10. The node V_TEMP is terminated to the NTC in the module. The circuit is designed to provide sufficient signal amplitude for measurement, but to limit NTC power dissipation to avoid incorrect measurements due to self-heating.

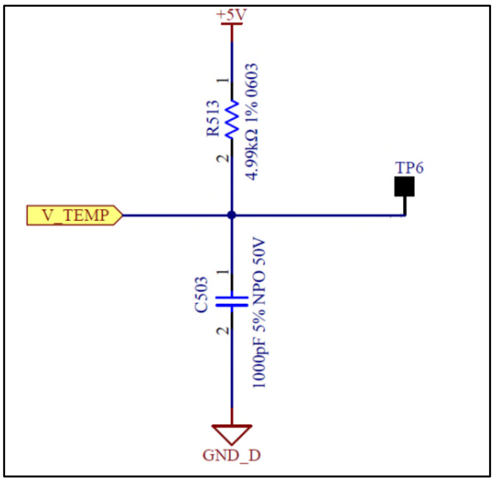

Figure 10 NTC sensing circuit

Hence, the sense voltage is,

Equation 1

$$\mathrm{V_{TEMP}} = 5\ \mathrm{V} * \frac{\mathrm{R_{NTC}}/\Omega}{\mathrm{R_{NTC}}\ /\Omega + 4990}$$

Rearranging Equation 1**,**

Equation 2

$$R_{NTC} = 4990\ \Omega * \frac{V_{TEMP}/V}{5 - V_{TEMP}/V}$$

The equation for R_{NTC} over-temperature T is provided in the FP150R12KT4P datasheet:

Equation 3

$$\mathrm{R_{NTC}} = (5000\ \Omega) * \mathrm{e}^{3433\ \left(\frac{1}{\mathrm{T/K}} - \frac{1}{298.15}\right)}$$

Rearranging Equation 3,

Equation 4

$$\mathrm{T} = \frac{1}{\frac{\ln\left[\frac{\mathrm{R_{NTC}}/\Omega}{5000}\right]}{3433\ \mathrm{K}} + \frac{1}{298.15\ \mathrm{K}}}$$

From Equation 2 and Equation 4,

Equation 5

$$T = \frac{1}{\frac{\ln\left[\frac{4990 * V_{TEMP}/K}{5000 * (5 - V_{TEMP}/K)}\right]}{3433\ K} + \frac{1}{298.15\ K}}$$

Equation 5 is plotted in Figure 11 after converting to ºC. From the figure it is possible to relate the voltage across the NTC and NTC temperature.

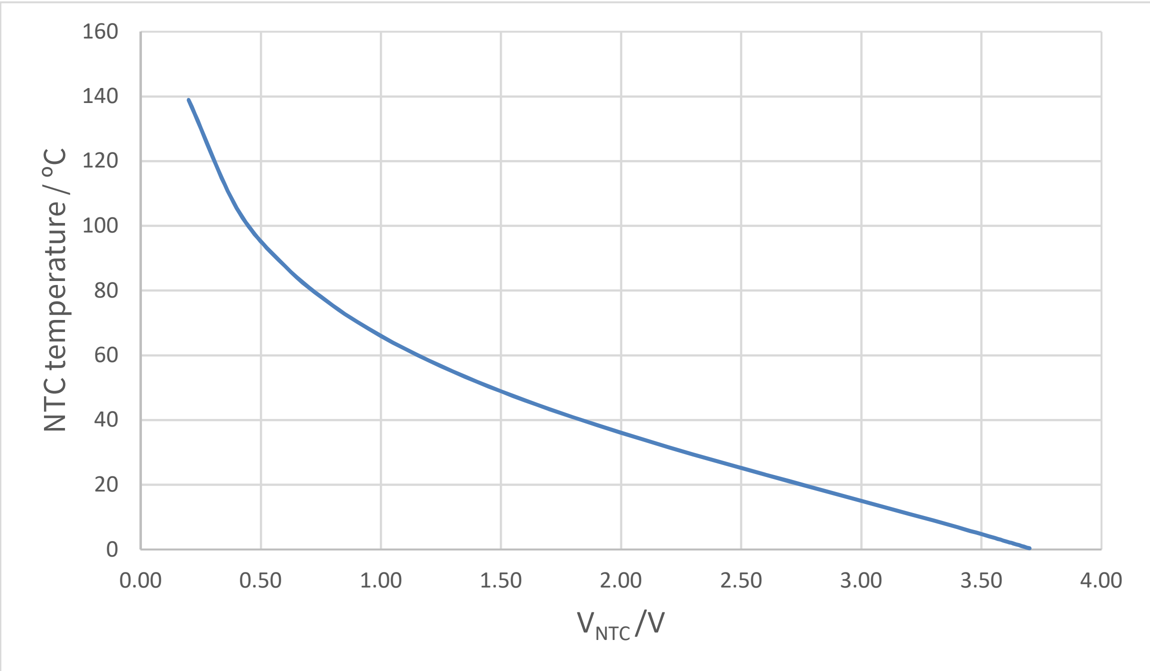

Figure 11 **NTC temperature vs V_{NTC}**

7. Details of the schematics, layout, BOM and connector

This section provides the complete details of the schematics, layout, bill of materials and connector. Please note that the schematics, routing and Gerber generation are done in Altium. Customers who are interested in the original Altium format files or pdf files for better clarity can contact Infineon.

7.1 Schematics

The board that is being described can support two modules, FP150R12KT4 and FP100R12KT4. The complete schematics are provided in Figure 12 - Figure 19.

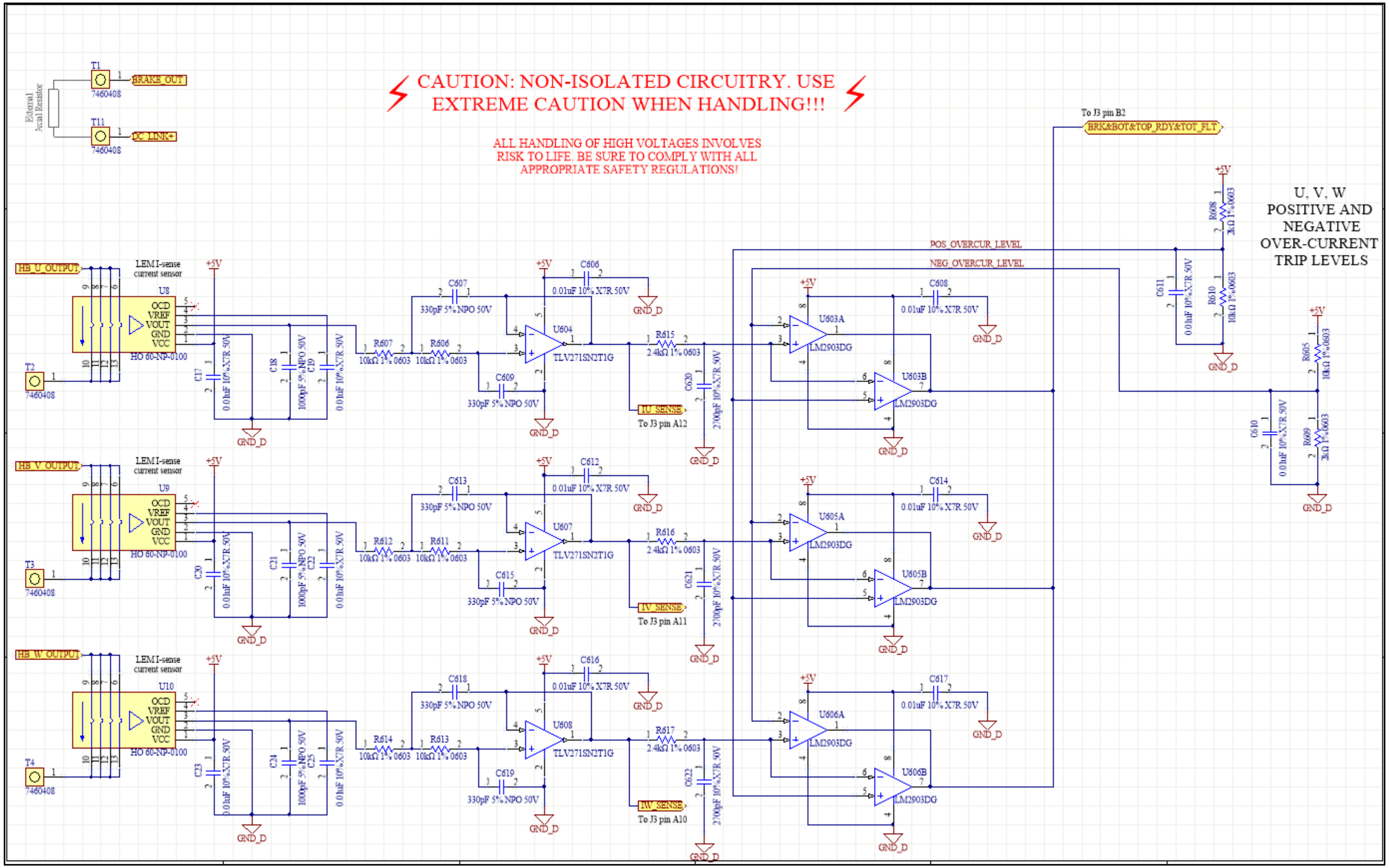

Figure 12 Schematics – Page – 1

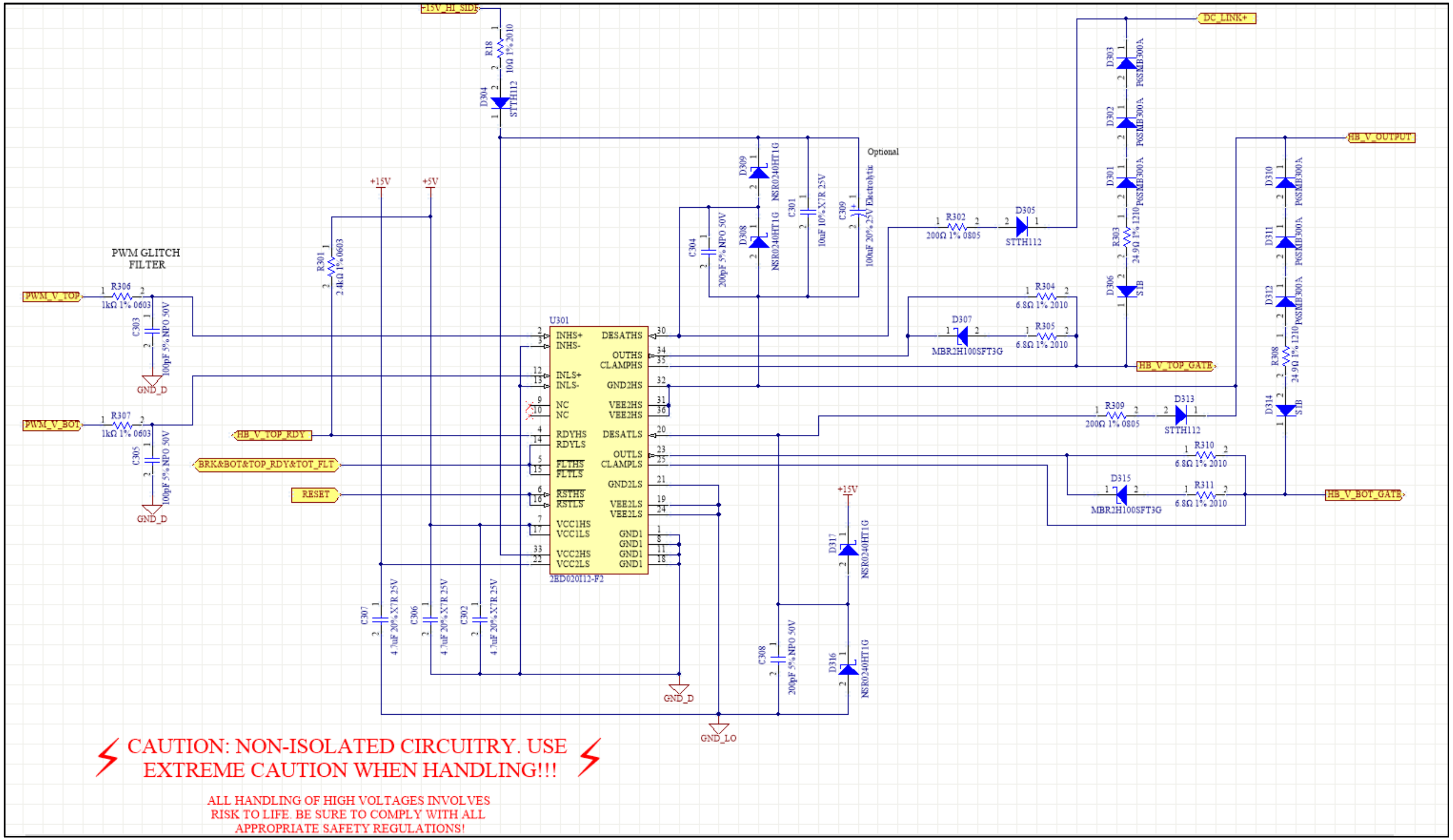

Figure 13 Schematics – Page - 2

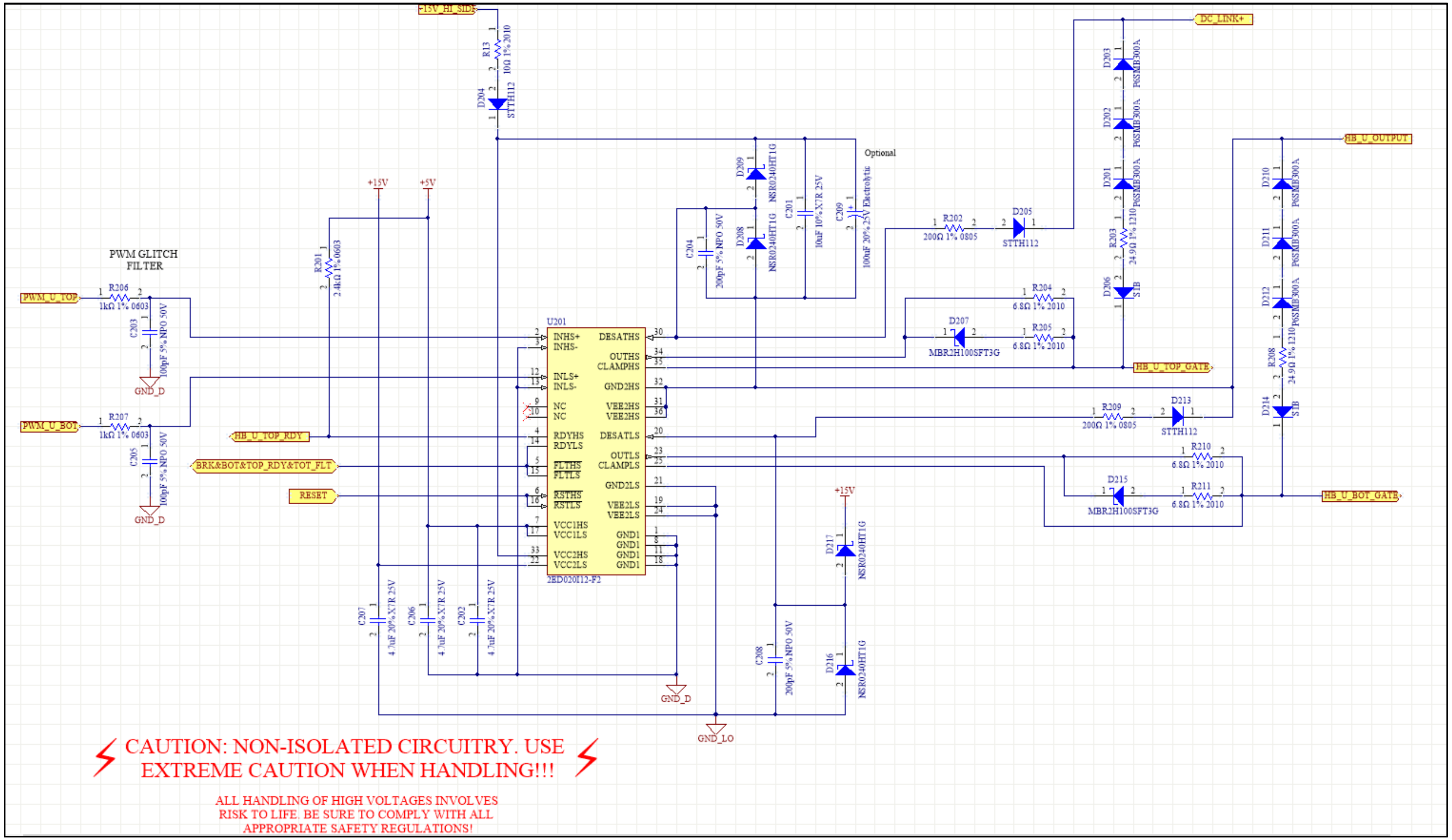

Figure 14 **Schematics – Page – 3**

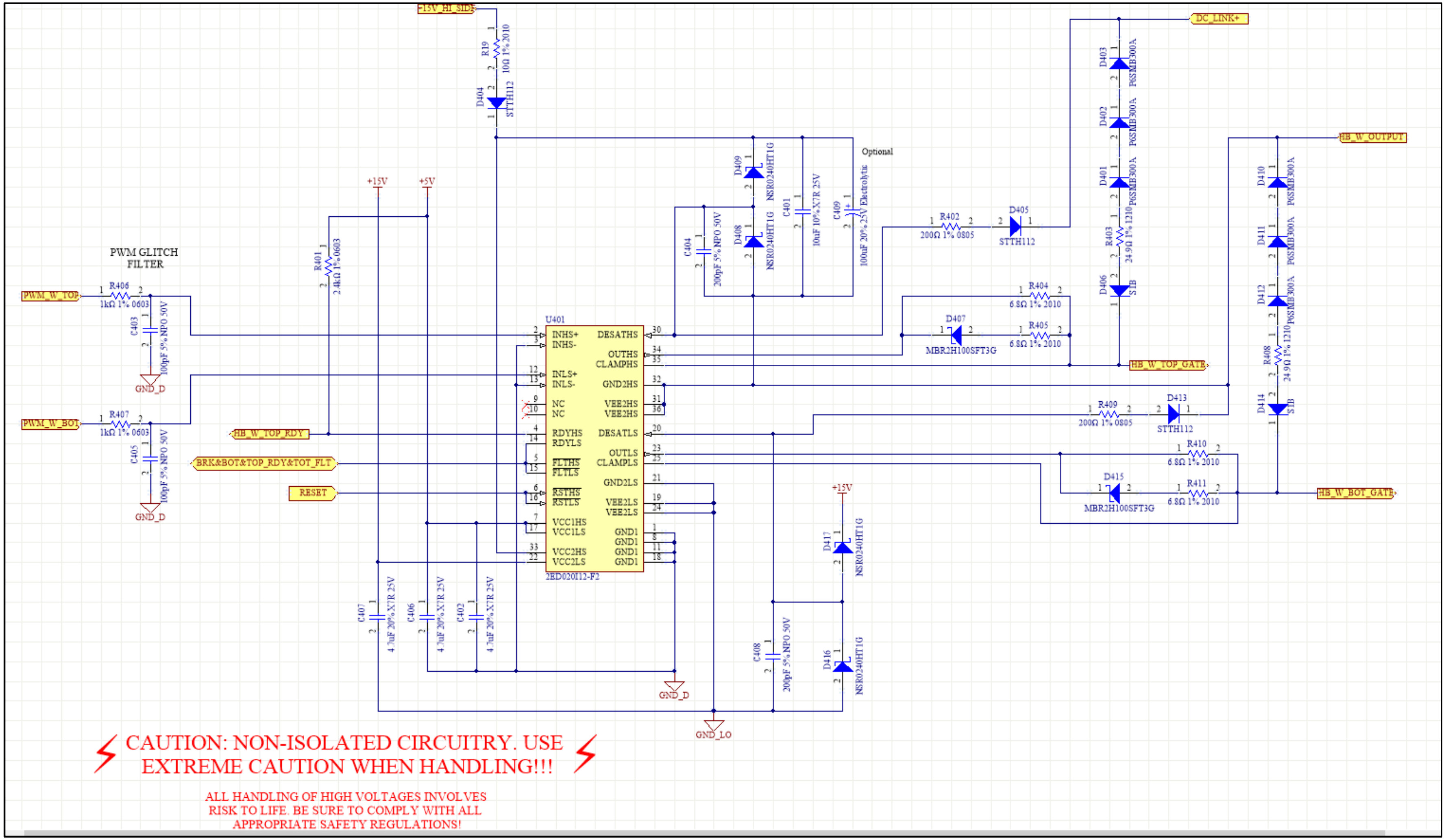

Figure 15 **Schematics – Page - 4**

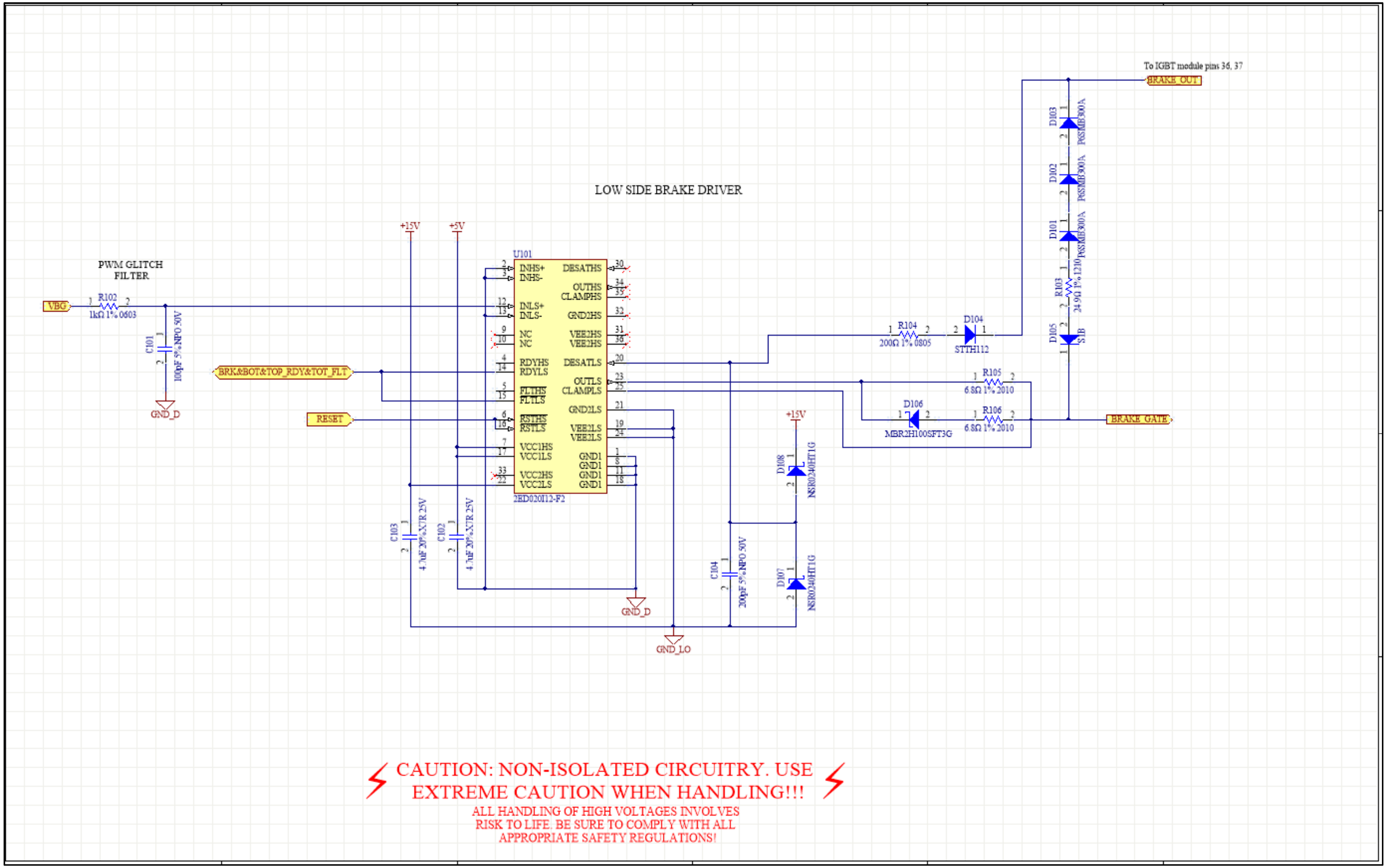

Figure 16 Schematics – Page – 5

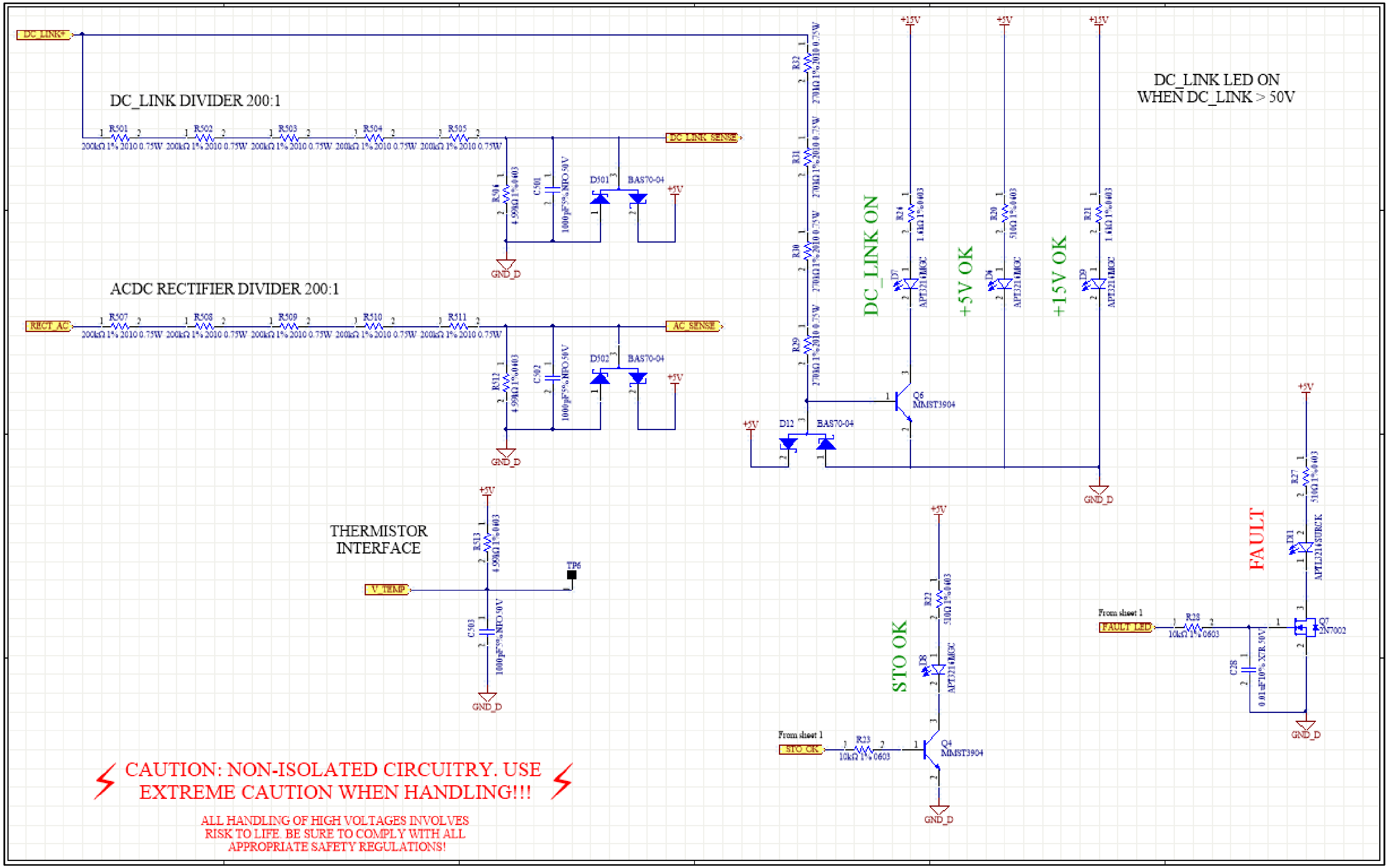

Figure 17 **Schematics – Page - 6**

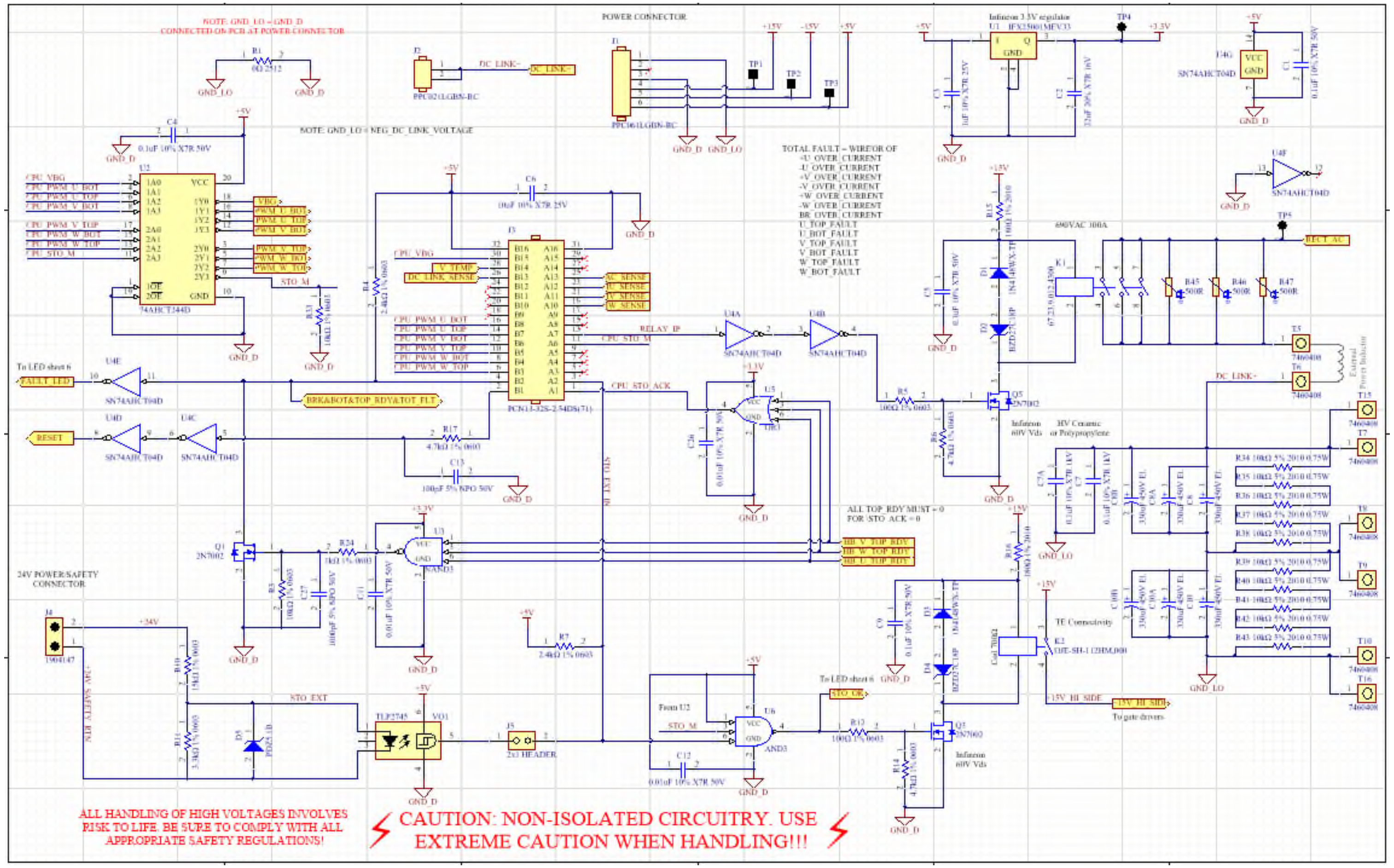

Figure 18 Schematics – Page - 7

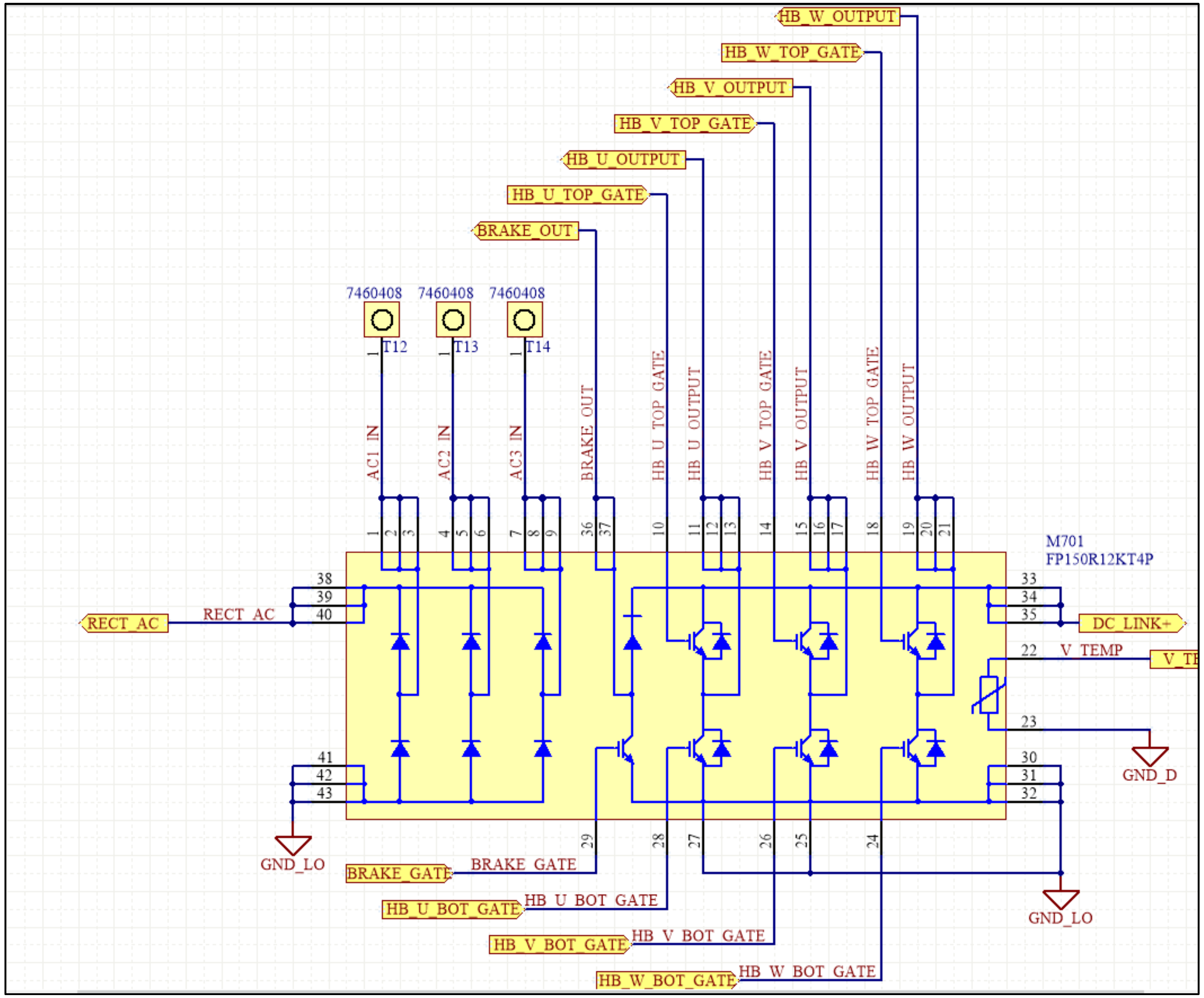

Figure 19 **Schematics – Page - 8**

7.2 Layout

This section provides the layout details and the reasons why it has been routed in this way. This explanation can be considered as a general routing guideline, and can be used elsewhere.

PCB routing basics start with the “right-hand rule” of electromagnetism. This rule states that for any conductor-carrying current pointing in the upwards direction of your thumb, all other fingers will point in the direction of the magnetic lines around the conductor; see Figure 20. Hence, when a PCB trace is routed, its magnetic field lines will influence the nearby circuitry. This problem may be minimized when the return path is placed nearby, as in Figure 20. Thus, their magnetic lines will cancel each other out.

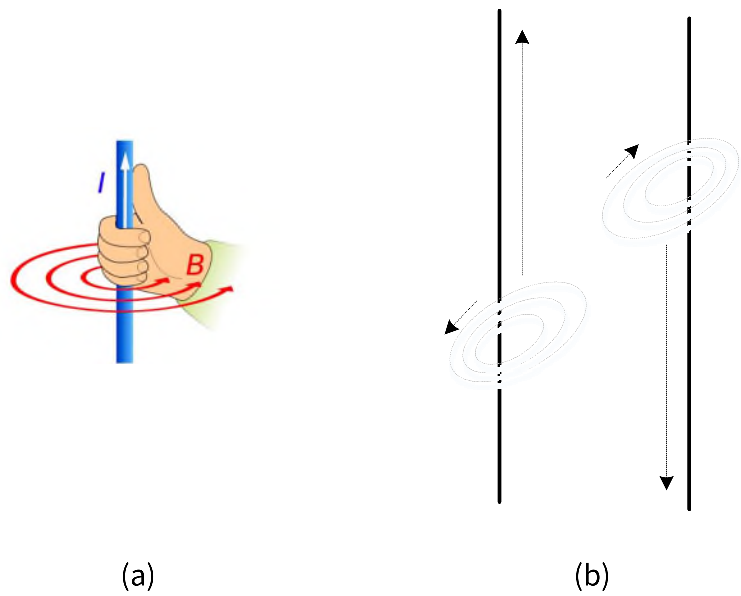

Figure 20 “Right-hand rule” of electromagnetism

The implementation rationale is detailed in Figure 21. In Figure 21, two different logics of routing are explained. Naturally, method (b) is better, as the forward-current path and the return paths are closer, hence, the magnetic field lines will cancel each other out. In multilayer PCB development, this is normally achieved by having an exclusive layer for the forward path, and an exclusive layer for the return path, which are placed as adjacent layers. Hence, the magnetic lines will cancel each other out.

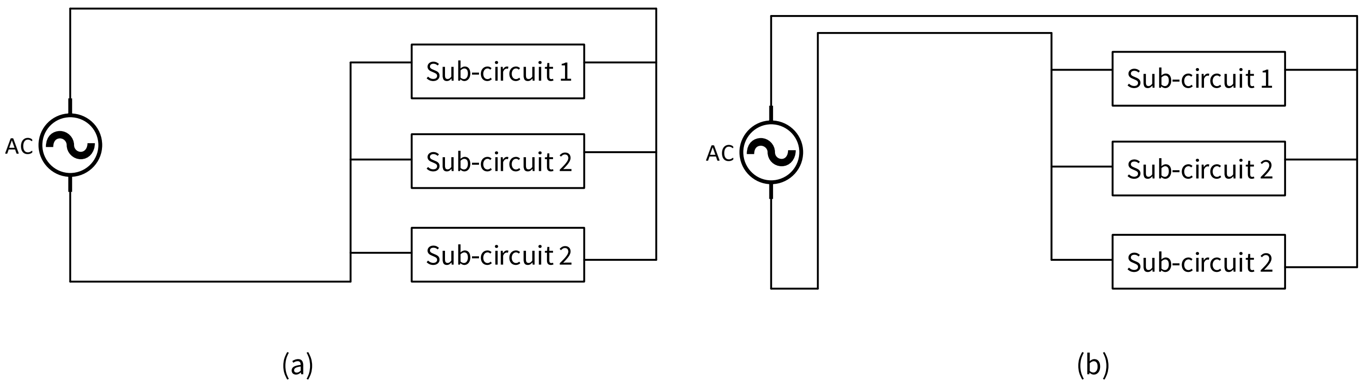

Figure 21 Implementation method while routing

Loop inductance or track inductance is another important parameter that the PCB designer needs to set as low as possible. The loop inductance or track inductance is defined as the inductor between any two nodes. This inductance affects turn-off behavior in a negative way by having over-shoots during the turn-off of IGBTs. Although the over-shoots can be eliminated by a turn-off snubber, the snubber causes additional power loss. Hence, an improperly designed PCB can affect efficiency as well. A typical representation of this parameter for an inverter leg with a DC bus is shown in Figure 22. If the layout rules to minimize external fields, as explained previously, are considered, the self-inductance of the circuit will be minimized.

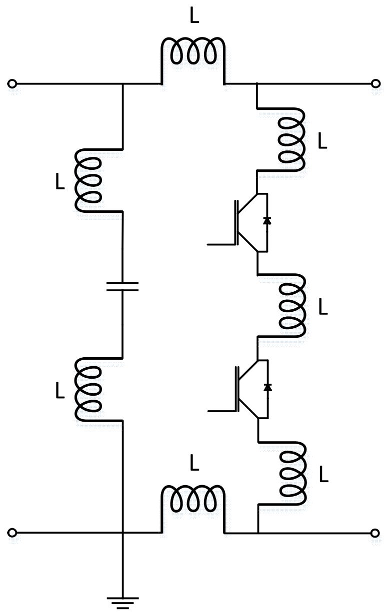

Figure 22 Loop inductance in a typical inverter leg

These concepts were used in the routing of the PCB, and the layout details are provided in Figure 23, Figure 24, Figure 25 and Figure 26. It can be seen in the layout that for all signals with fast current transients, adjacent layers carry currents in the opposite direction, as already explained. However, when optimizing a layout for inductance, capacitive coupling must also be considered. Therefore, large overlaps of layers carrying signals with significant voltage transients are to be avoided.

7.2.1 Ground layer

The ground plane is a large copper pour area which serves as a return path for current from different sub-circuits. Normally the logic ground and the power ground are terminated as a star point. By providing a ground plane or a ground layer, the return signals will follow their corresponding signal path closely. This will help in reducing the EMI. In this design, both power and control ground layers are separately routed and merged in a common point. The power ground and the digital/control ground are mentioned as “GND_LO” and “GND_D” in schematics. Although electrically, both the grounds are the same, concerning noise immunity, they are separately routed and connected at a common point. The ground layer is provided in the bottom layer of the PCB, and is displayed in Figure 26.

7.2.1 Other precautions

- EiceDRIVER™ 2ED020I12-F2 is galvanically isolated between input and output of the driver circuit. In order to avoid crosstalk between the input and output circuit, it is advisable not to provide a copper plane below the driver IC. This will help in reducing the capacitive coupling between the input circuit and output circuit, hence will help in reducing crosstalk.

- Each EiceDRIVER™ 2ED020I12-F2 has two channels that drive high-side and low-side switches. A slot is placed between each channel to increase the electrical clearance; see Figure 23.
- During the turn-on or turn-off transition, the IGBT gate circuit generally draws pulsed currents. Hence, it is advisable to keep the desaturation signal lines away from the gate-driving paths.
- The control-board connector is placed on one of the edges of the PCB, and other power connectors are placed on the other sides of the power board to avoid a crisscross; see Figure 23 and Figure 27.

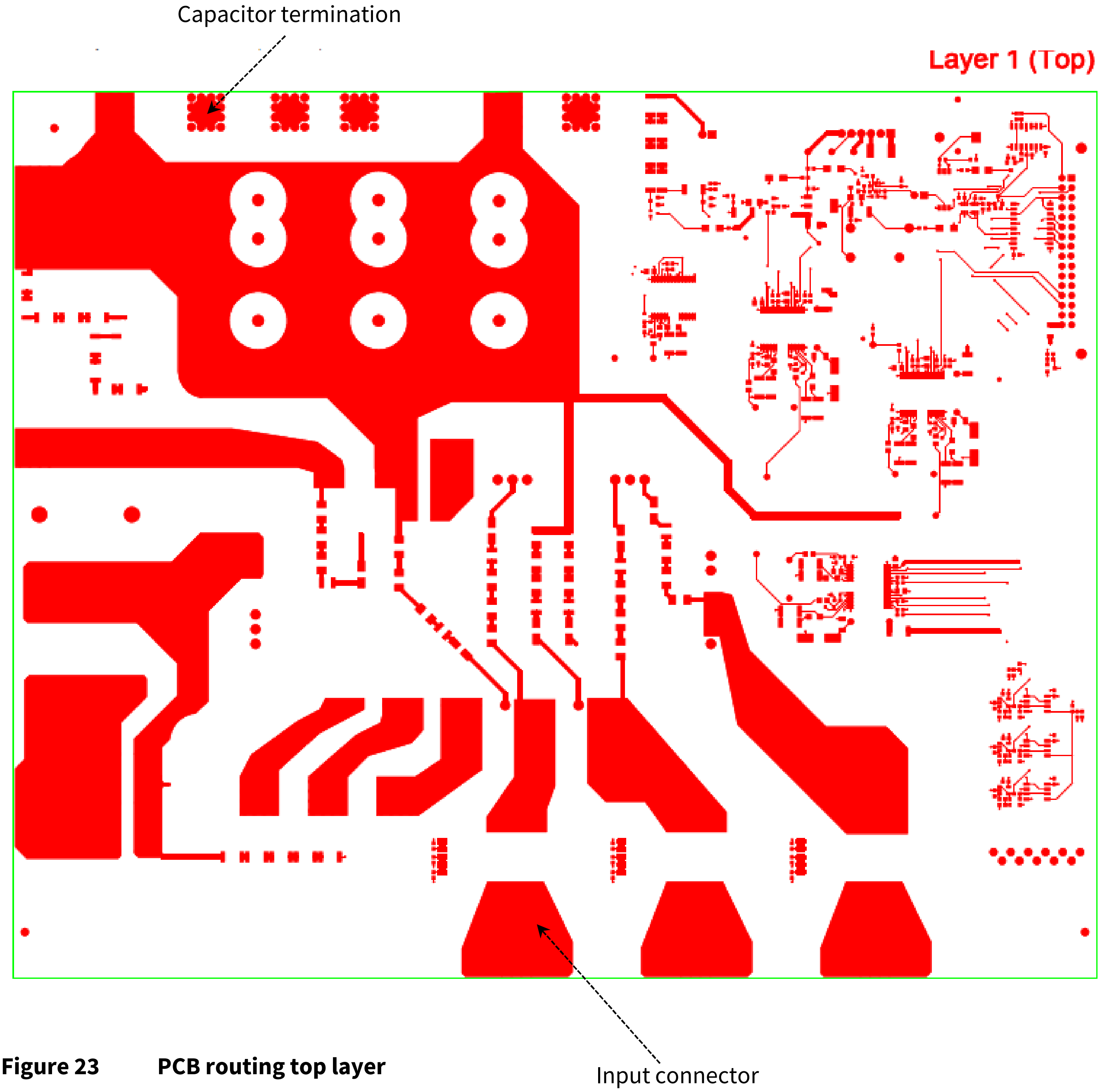

Figure 23 PCB routing top layer

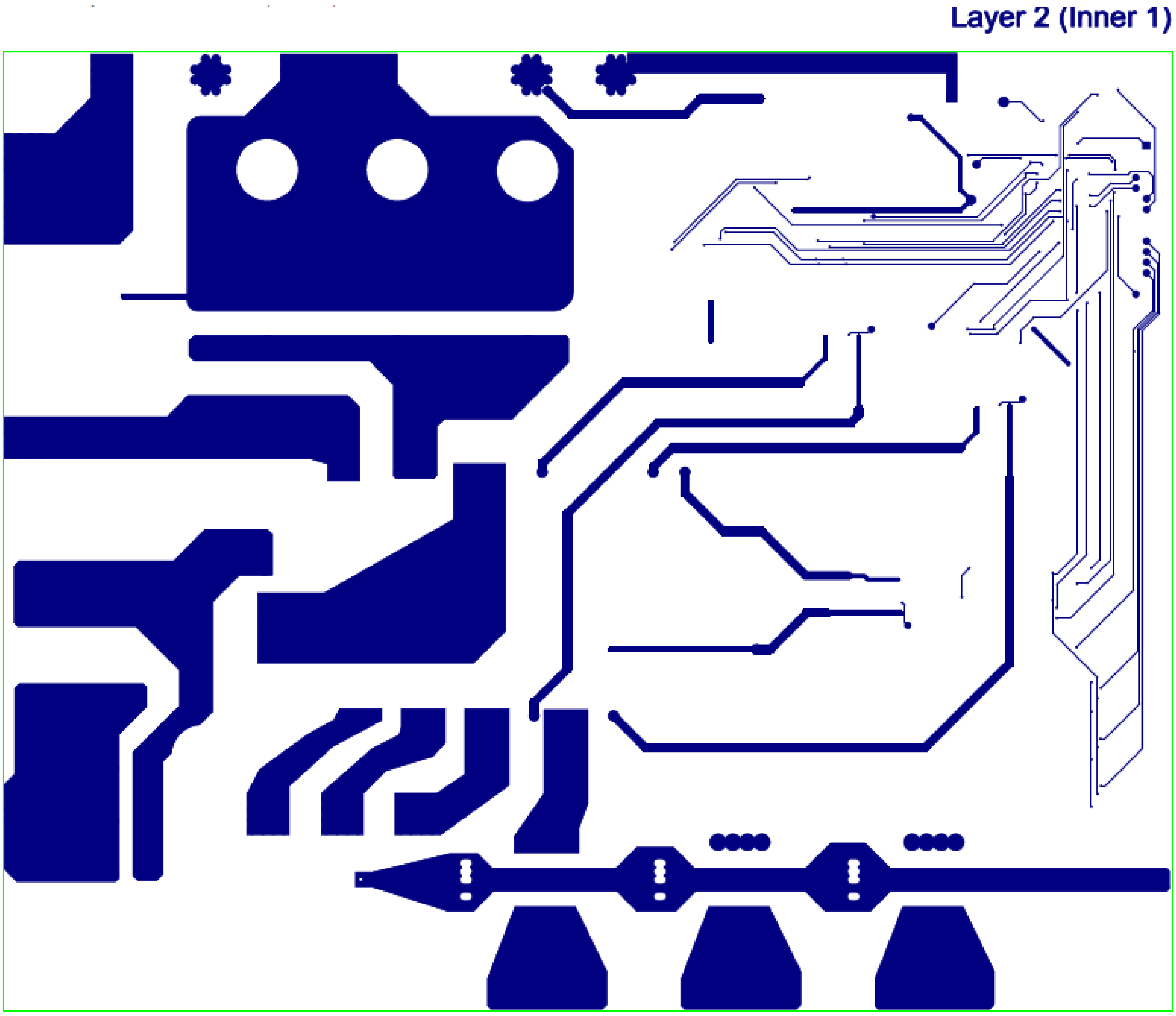

Figure 24 PCB routing inner layer - Layer 2

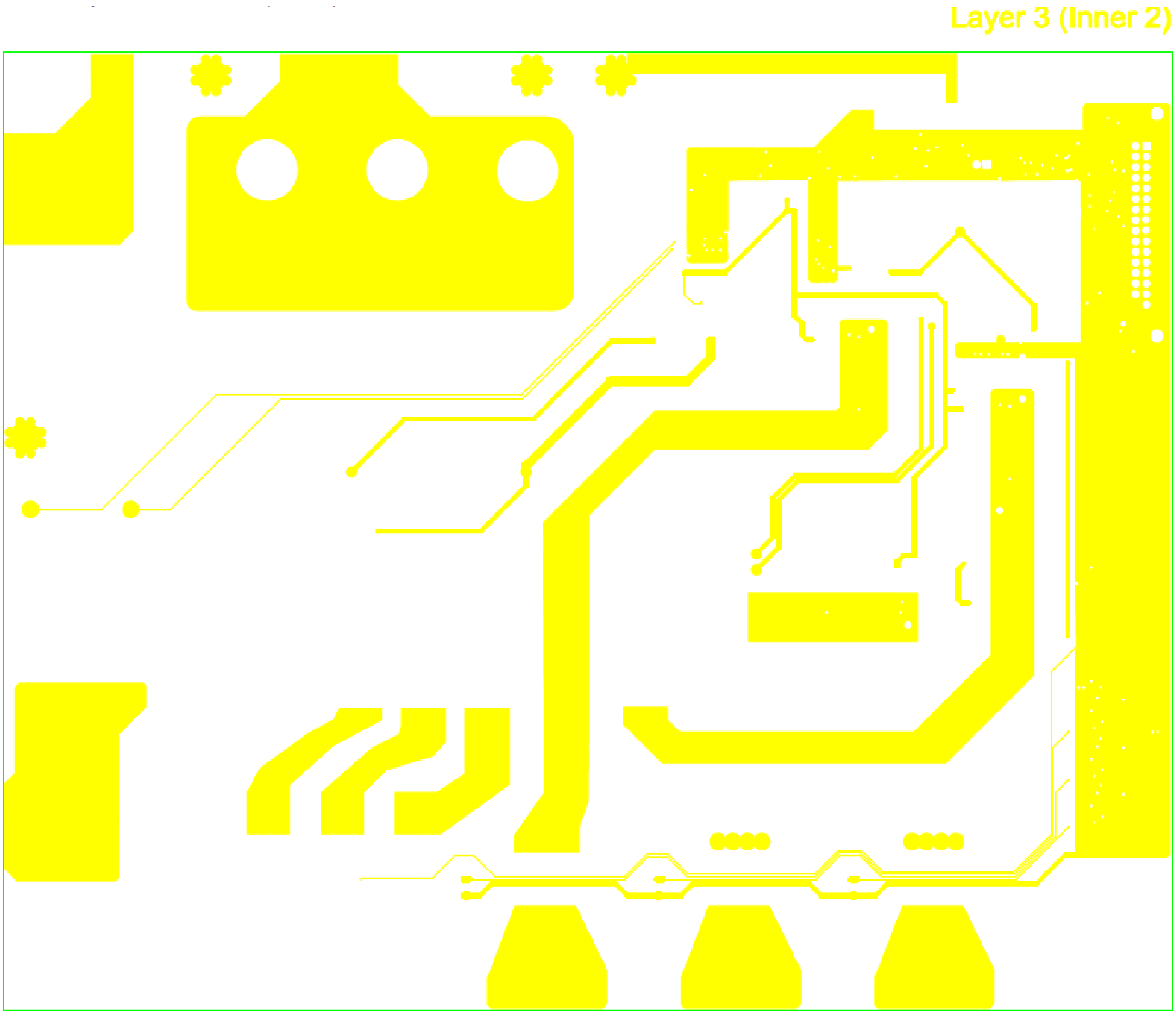

Figure 25 PCB routing inner layer - Layer 3

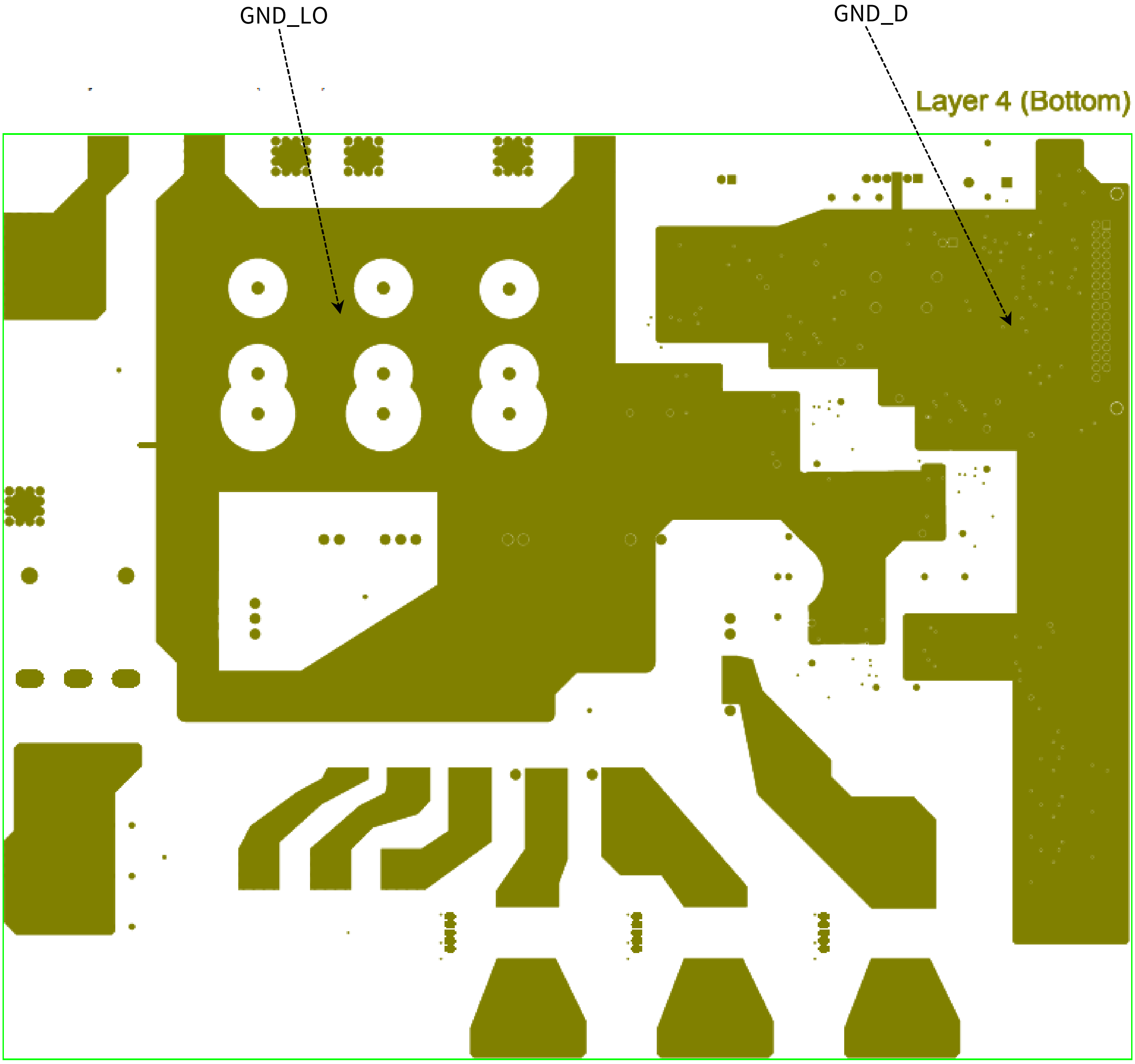

Figure 26 **PCB routing bottom layer**

7.3 BOM

Table 4 provides the BOM with information about the manufacturer, manufacturer's part number and the part details. The BOM also provides the details of both modules. Normally the modules are not soldered in the power board while shipping. The customer needs to order separately based on his/her requirements.

Table 4 BOM of the power board based on FP150R12KT4P or FP100R12KT4P

S. No.	Ref Designator	Description	Manufacturer	Manufacturer P/N
1	C1, C4, C5, C9	CAP SMD CER 0.1µF 50V X7R 0603	Murata	GCM188R71H104KA57J
2	C2	CAP SMD CER 22µF 16V X7R 1206	Taiyo Yuden	EMK316BB7226ML-T
3	C3	CAP SMD CER 1µF 25V X7R 0603	Murata	GRJ188R71E105KE11D
4	C6, C201, C301, C401	CAP SMD CER 10µF 25V X7R 1206	Murata	GRM31CR71E106KA12L
5	C7, C7A	CAP SMD CER 0.1µF 1kV X7R 2220	Murata	GRM55DR73A104KW01L
6	C11, C12, C17, C19, C20, C22, C23, C25, C26, C28, C606, C608, C610, C611, C612, C614, C616, C617	CAP SMD CER 10000pF 50V X7R 0603	Murata	GRM188R71H103KA01D
7	C13, C101, C203, C205, C303, C305, C403, C405	CAP SMD CER 100pF 50V C0G/NP0 0603	Murata	GRM1885C1H101JA01D
8	C18, C21, C24, C27, C501, C502, C503	CAP SMD CER 1000pF 50V C0G/NP0 0603	Murata	GRM1885C1H102JA01D
9	C102, C103, C202, C206, C207, C302, C306, C307, C402, C406, C407	CAP SMD CER 4.7µF 25V X7R 0805	Murata	GRM21BR71E475MA73L
10	C104, C204, C208, C304, C308, C404, C408	CAP SMD CER 200pF 50V C0G/NP0 0603	Murata	GRM1885C1H201JA01D
11	C209, C309, C409	CAP SMD ALUM 100µF 20% 25V	Panasonic	EEEHD1E101AP
12	C607, C609, C613, C615, C618, C619	CAP SMD CER 330pF 50V C0G/NP0 0603	Murata	GRM1885C1H331JA01D
13	C620, C621, C622	CAP SMD CER 2700pF 50V X7R 0603	Murata	CL10B272KB8NNNC
14	D1, D3	DIODE GEN PURP 75V 150mA SOD323	MCC	1N4148WX-TP
15	D2, D4	DIODE ZENER 800mW SMF DO219	Vishay	BZD27C18P
16	D5	DIODE ZENER 5.1V 400mW SOD323	NXP	PDZ5.1B
17	D6, D7, D8, D9	LED GREEN CLEAR CHIP SMD	Kingbright	APT3216MGC
18	D11	LED RED CLEAR CHIP SMD	Kingbright	APTL3216SURCK
19	D12, D501, D502	DIODE SCHOTTKY 70V 70mA SC70	Diodes Inc	BAS70-04
20	D101, D102, D103, D201, D202, D203, D210, D211, D212, D301, D302, D303, D310, D311, D312, D401, D402, D403, D410, D411, D412	TVS DIODE 256V 414V DO214AA	Vishay	P6SMB300A
21	D105, D206, D214, D306, D314, D406, D414	DIODE GEN PURP 100V 1A SMA	ON Semi	S1B
22	D107, D108, D208, D209, D216, D217, D308, D309, D316, D317, D408, D409, D416, D417	DIODE SCHOTTKY 40V 250mA SOD323	ON Semi	NSR0240HT1G
23	Q1, Q3, Q5, Q7	MOSFET N-CH 60V 115mA SOT-323	ON Semi	2N7002W
24	Q4, Q6	TRANS NPN 40V 0.2A SC70-3	Diodes Inc	MMST3904-7-F
25	R1	RES SMD 0Ω JUMPER 1W 2512	Bourns	CR2512-J/-000ELF
26	R3, R23, R28, R605, R606, R607, R610, R611, R612, R613, R614	RES SMD 10kΩ 1% 1/8W 0603	Vishay	MCT06030C1002FP500
27	R4, R7, R201, R301, R401, R615, R616, R617	RES SMD 2.4kΩ 1% 1/10W 0603	Vishay	CRCW06032K40FKEA
28	R5, R12	RES SMD 100Ω 1% 1/10W 0603	Vishay	CRCW0603100RFKEA
29	R6, R14, R17	RES SMD 4.7kΩ 1% 1/4W 0603	Vishay	CRCW06034K70FKEA
30	R10	RES SMD 15kΩ 1% 1/8W 0603	Vishay	MCT06030C1502FP500

S. No.	Ref Designator	Description	Manufacturer	Manufacturer P/N
31	R11	RES SMD 3.3kΩ 1% 1/10W 0603	Vishay	CRCW06033K30FKEA
32	R13, R18, R19	RES SMD 10Ω 1% 3/4W 2010	Vishay	CRCW201010R0FKEF
33	R15, R16	RES SMD 180Ω 5% 3/4W 2010	Vishay	CRCW2010180RJNEF
34	R20, R22, R27	RES SMD 510Ω 1% 1/10W 0603	Vishay	CRCW0603510RFKEA
35	R21, R26	RES SMD 1.6kΩ 1% 1/10W 0603	Vishay	CRCW06031K60FKEA
36	R24, R102, R206, R207, R306, R307, R406, R407	RES SMD 1kΩ 1% 1/10W 0603	Vishay	CRCW06031K00FKEA
37	R29, R30, R31, R32	RES SMD 270kΩ 1% 3/4W 2010	Vishay	CRCW2010270KFKEF
38	R34, R35, R36, R37, R38, R39, R40, R41, R42, R43	RES SMD 10kΩ 5% 3/4W 2010	Vishay	CRCW201010K0JNEF
39	R105, R204, R210, R304, R310, R404, R410	RES SMD 6.8Ω 1% 1W 2010	Vishay	CRCW20106R80FKEFHP
40	R103, R203, R208, R303, R308, R403, R408	RES SMD 24.9Ω 1% 1/2W 1210	Vishay	CRCW121024R9FKEA
41	R104, R202, R209, R302, R309, R402, R409	RES SMD 200Ω 1% 1/8W 0805	Vishay	CRCW0805200RFKEA
42	R501, R502, R503, R504, R505, R507, R508, R509, R510, R511	RES SMD 200kΩ 1% 3/4W 2010	Vishay	CRCW2010200KFKEF
43	R506, R512, R513	RES SMD 4.99kΩ 1% 1/8W 0603	Vishay	MCT06030C4991FP500
44	R608, R609	RES SMD 2kΩ 1% 1/10W 0603	Vishay	CRCW06032K00FKEA
45	U1	IC REG LIN 3.3V 400mA SOT223-4	Infineon	IFX25001MEV33
46	U2	IC BUFFER NON-INVERT 5.5V 20SO	NXP	74AHCT244D
47	U3	IC GATE NAND 1CH 3-INP SC70-6	TI	SN74LVC1G10DCK
48	U4	IC INVERTER 6CH 6-INP 14SOIC	TI	SN74AHCT04D
49	U5	IC GATE OR 1CH 3-INP SC70-6	TI	SN74LVC1G332DCK
50	U6	IC GATE AND 1CH 3-INP SC70-6	TI	SN74LVC1G11DCKR
51	U101, U201, U301, U401	IC DRIVER IGBT DSO36	Infineon	2ED020I12-F2
52	U603, U605, U606	IC COMP DUAL OFFSET LV 8SOIC	On Semi	LM2903DG
53	U604, U607, U608	IC OPAMP GP 3MHZ RRO 5TSOP	ON Semi	TLV271SN2T1G
54	VO1	OPTOISO 5kV PUSH PULL SO6L	Toshiba	TLP2745
55	PCB	REF- GPD30KN3T4M5	Infineon	REF-GPD30KN3T4M5 Rev 1.0
56	C8, C8A, C8B, C10, C10A, C10B	CAP ALUM 330µF 20% 450V SNAP	EPCOS	B43644A5337M007
57	D104, D204, D205, D213, D304, D305, D313, D404, D405, D413	DIODE GEN PURP 1.2kV 1A DO41	STMicroelectronics	STTH112RL
58	J4	2-PIN PCB TERMINAL BLOCK	Phoenix Contact	1904147
59	J5	2-PIN PCB TERMINAL BLOCK 9.52mm	Wurth Electronics	61300211121
60	J1	CONN FEMALE 6POS .100" R/A GOLD	Sullins Connector	PPPC061LGBN-RC
61	J2	CONN FEMALE 2POS .100" R/A GOLD	Sullins Connector	PPPC021LGBN-RC
62	J3	CONN DIN RCPT 32POS DUAL RT ANG	Hirose Electric	PCN13-32S-2.54DS(71)
63	K1	HIGH POWER RELAY 12V 100A	Finder relays	67.23.9.012.4300
64	K2	GENERAL PURPOSE RELAY 12V 10A SPST	TE Connectivity	OJE-SH-112HM,000
65	M701	INFINEON EconoPIM(TM)3 MODULE	Infineon	FP150R12KT4P or FP100R12KT4P
66	T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16	TERM PWR ELEMENT M5 12 PIN PCB	Wurth Electronics	7460408
67	U8, U9, U10	SENSOR CURRENT HALL 120A AC/DC	LEM	HO 60-NP-0100
68	D106, D207, D215, D307, D315, D407, D415	DIODE SCHOTTKY 100V 2A SOD123FL	ON Semi	MBR2H100SFT3G
69	R106, R205, R211, R305, R311, R405, R411	RES SMD 6.8Ω 1% 1W 2010	Vishay	CRCW20106R80FKEFHP
70	R45, R46, R47	PTC THERMISTOR C 755-A 115-A 70	Epcos	B59755C0115A070

7.4 Connector details

The connector is intended to accommodate an auxiliary board containing a SMPS that provides the supply voltages needed on the power board from the main DC link. Alternately, these supply voltages can be supplied from other isolated external sources. Table 5 provides the auxiliary power supply connector details.

Although -15 V supply is not used in this board, provision is made in the auxiliary power supply to accommodate the future generation of power boards.

Table 5 Auxiliary power supply connector

Connector and position	Signal name	Description
J2 - 1	DC Bus - Positive	Connected to pin 26/27 on module FP100R12KT4 or connected to pin 33/34/35 on module FP150R12KT4
J2 - 2		
J1 - 1	DC bus - Negative	Power ground
J1 - 2	NC	
J1 - 3	GND	Bias ground. Power ground and bias ground are connected through a ferrite bead
J1 - 4	+15 VDC	+ 15 V power supply
J1 - 5	-15 VDC	- 15 V power supply
J1 - 6	+5 VDC	+ 5 V power supply

Table 6 lists the safe torque-off connector details.

Table 6 STO connector

Connector and position	Signal name	Description
J4 - 1	+24 V	+24 V provided from the external control
J4 - 2	+24 V_RTN	Return for +24 V

Infineon provides a control card based on XMC4400. The complete details are available in Reference [4]. The voltage and current signals are suitably scaled to suit the control card. Hence, customers can start using it without the need for modifications in the control board. Connector J3 is used to connect the control card and the signal; see details in Table 7.

Table 7 Signal details of control card mating connector

Female - DIN41612-Q/2	Description	Signal	Voltage levels	Direction of signal
A16	Gnd	GND	NA	
A15				
A14				
A13	Line voltage sensing	AC	0 to 5 V	To µC
A12	U phase current	IU+	0 to 5 V	To µC
A11	V phase current	IV+	0 to 5 V	To µC
A10	W phase current	IW+	0 to 5 V	To µC
A9				
A8				
A7	Input relay control	RLY_IP	0 to 3.3 V	From µC
A6	STO signal from micro	STO_M	0 to 3.3 V	From µC
A5				
A4				
A3				
A2	STO signal to micro	STO	0 to 5 V	To µC
A1	STO acknowledge signal	CPU_STO_ACK	0 to 3.3 V	To µC
B16	+5V power supply	Bias +5V		
B15	Braking section gate signal	VBG	0 to 3.3 V	From µC
B14	Thermistor voltage	VTH	0 to 5 V	To µC
B13	DC bus voltage sense	DCBSENSE	0 to 5 V	To µC
B12				
B11				
B10				
B9				
B8	PWM, U phase , bottom signal	PWMUL	0 to 3.3 V	From µC
B7	PWM, U phase , top signal	PWMUH	0 to 3.3 V	From µC
B6	PWM, V phase , bottom signal	PWMVL	0 to 3.3 V	From µC
B5	PWM, V phase , top signal	PWMVH	0 to 3.3 V	From µC
B4	PWM, W phase , bottom signal	PWMWL	0 to 3.3 V	From µC
B3	PWM, W phase , top signal	PWMWH	0 to 3.3 V	From µC
B2	Fault signal	GKB+GKI+FLT	0 to 5 V	To µC
B1	Reset signal from driver IC	RST	0 to 3.3 V	From µC

7.5 Component placement

Figure 27 displays the component placement of the PCB. The subsystems are grouped together, and accordingly, component placement is done.

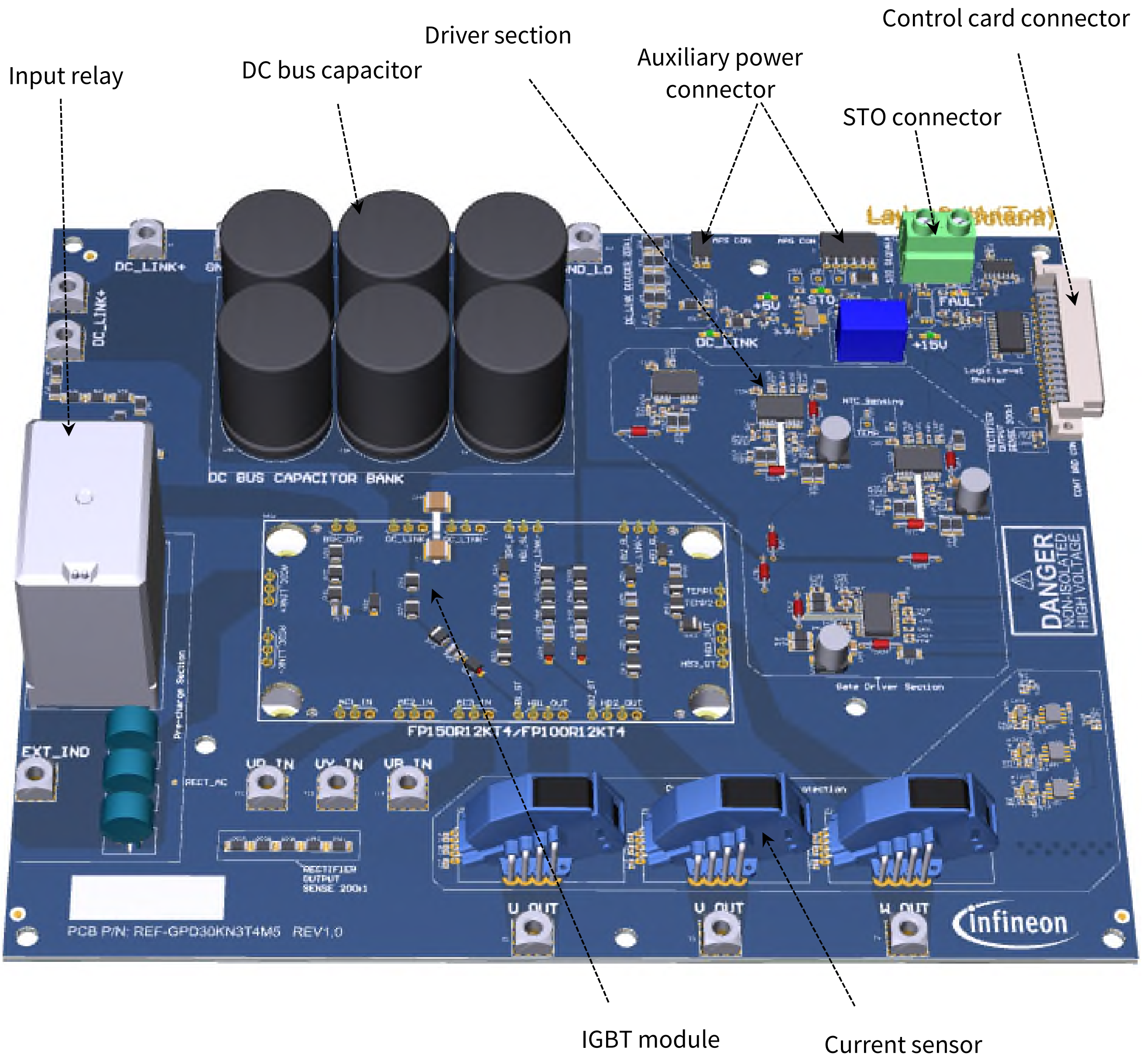

Figure 27 PCB component placement

7.6 Heat-sink recommendation

As the dimensions of the modules FP150R12KT4 and FP100R12KT4 are the same, heat sink either from Wakefield-Vette 511-6M can be used. Complete details of the heat sink is available in the datasheets. A cooling fan with 110 CFM is used to achieve active cooling. The typical fin profile of the heat sink with fan position is provided in Figure 28. It is advised to use an extrusion length of 150 mm for this application.

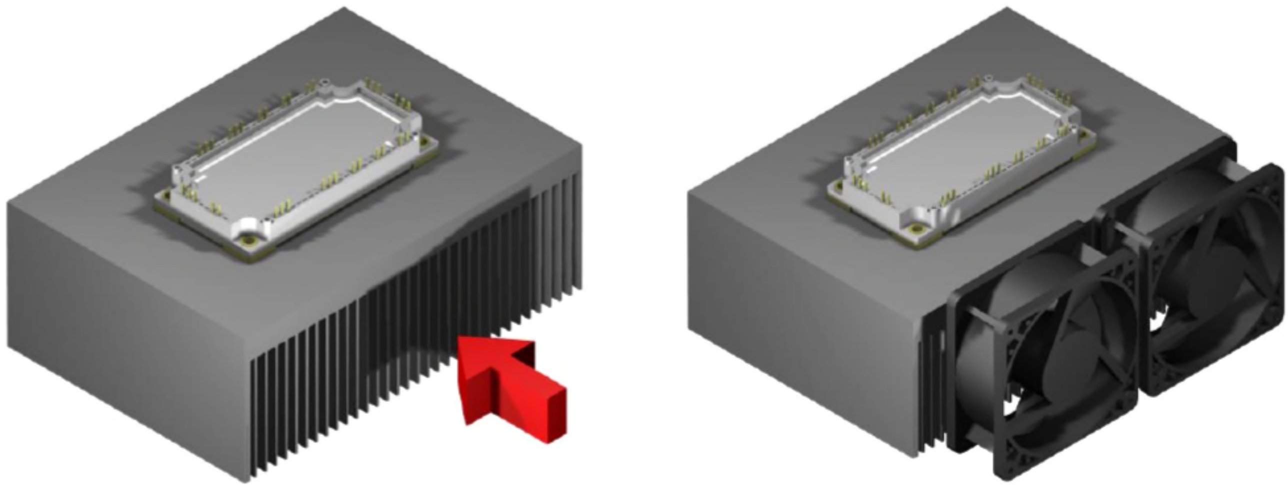

Figure 28 Heat sink and fan arrangement details

8. Test results of FP150R12KT4

This section provides the test results for both modules.

8.1 Double-pulse test and switching loss calculation

Figure 29 shows the double-pulse test for one of the low-side switches with the following operating conditions:

- DC link voltage = 800 V
- Max. current = 150 A
- R_{gate} On = 6.8 Ω and R_{gate} Off = 6.8 Ω || 6.8 Ω
- Pulse width = 7 µs

During turn-off, the maximum voltage spike across the switch is < 950 V for a DC bus voltage of 800 V. In Figure 29, channel 1 displays voltage across the switch with 500 V/div; channel 2 displays the current through the external short with 40 A/div; channel 3 is voltage at gate-to-emitter terminal with 10 V/div; and channel 4 is PWM input to the gate driver IC with 10 V/div.

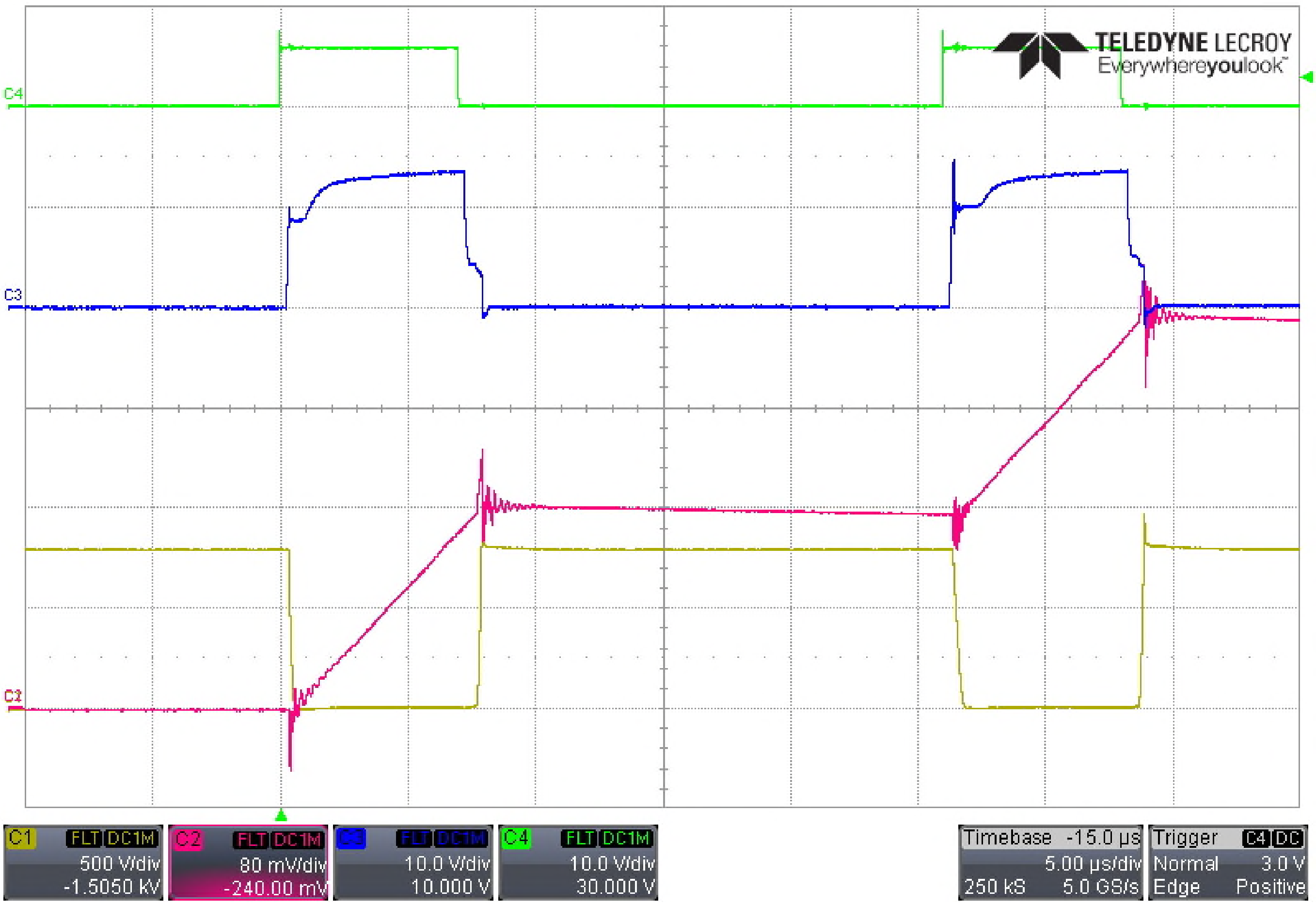

Figure 29 **Double-pulse test**

The waveform in Figure 30 and Figure 31 provides the switching loss details. The switching loss values measured in this experiment can be compared with the values provided in the datasheet. Turn-on and turn-off losses mentioned in the datasheet are 22 mJ and 9.8 mJ, respectively, at 25ºC and 600 VDC. These differences arise due to different operating conditions. Although the turn-off gate resistor value is lower than the datasheet, its effect on turn-off loss is minimal. See Reference [10] for more information about this test.

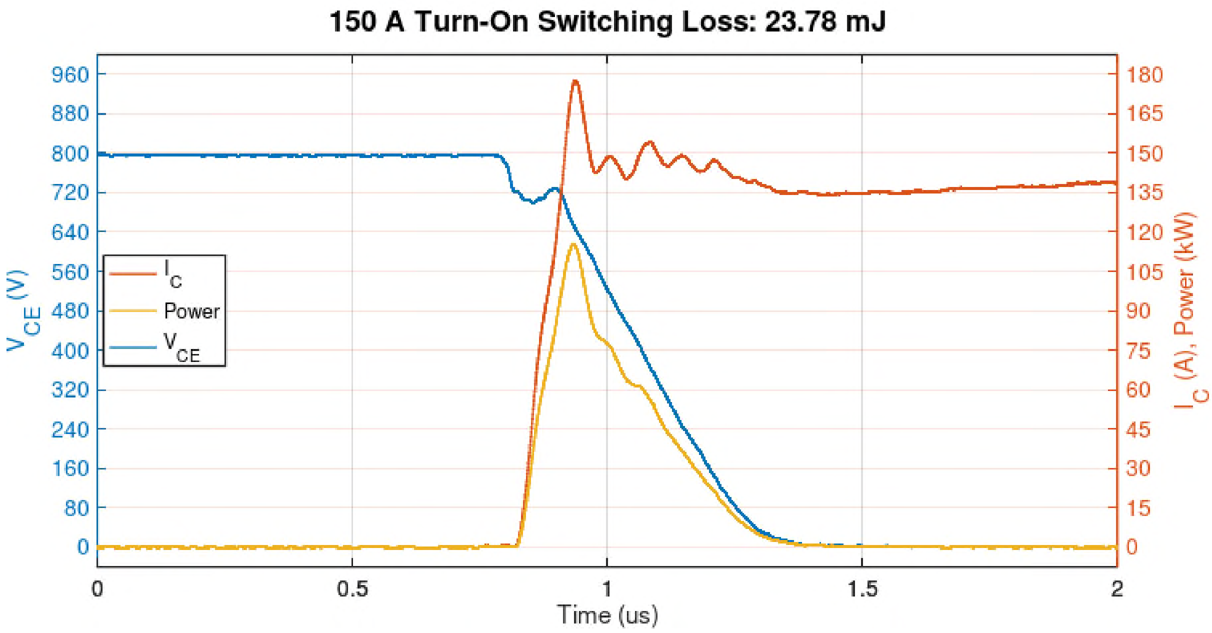

Figure 30 **Switching on transition loss details**

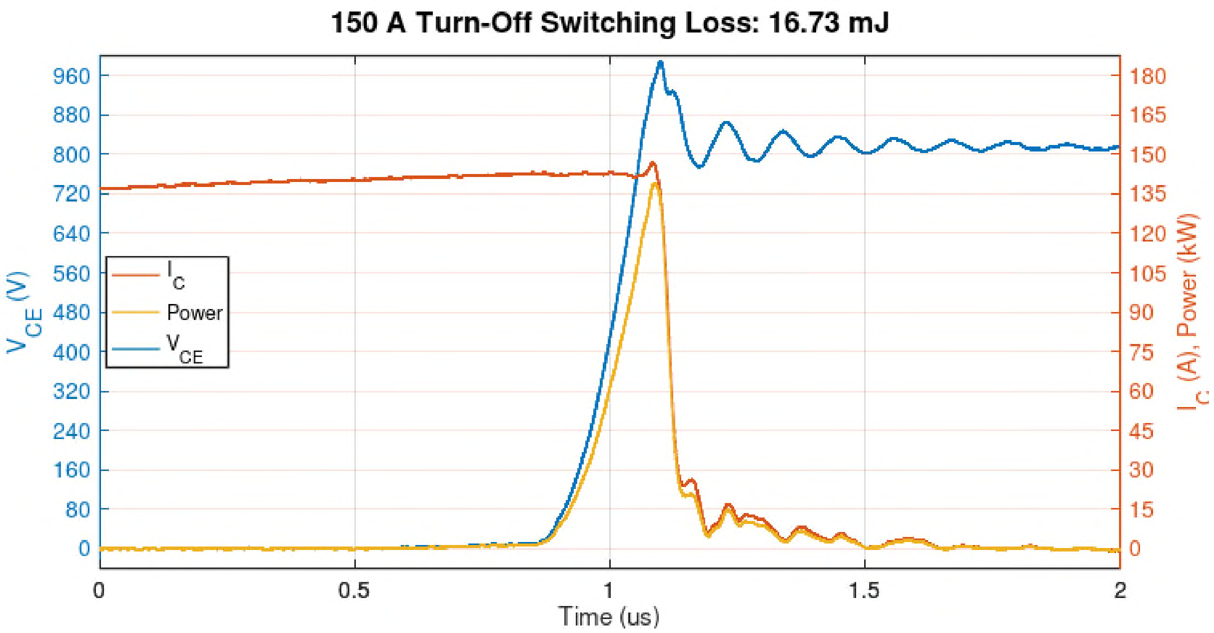

Figure 31 **Switching off transition loss details**

8.2 Temperature rise

The complete setup with the cooling arrangements suggested in 7.6 were subjected to a thermal test. The results were tabulated in Table 8. The unit was switched at 4.4 kHz with a fundamental frequency of 400 Hz. The setup reached a maximum temperature of 104°C at an ambient temperature of 25°C. At every power level, the set up was allowed to stabilize, then the power output was increased.

Table 8 Temperature rise

Output volt V_{rms}	Current A_{rms}	Output power W	Heat sink °C	NTC °C
185	15	4806	37.9	37.1
260	30	13510	47.5	49
312	45	24318	58.9	65
350	60	36373	73.6	79.6
380	75	49363	83	104

8.3 Bootstrap capacitor ripple

The ripple on a bootstrap capacitor was monitored with a load current of 60 A RMS with a fundamental frequency of 900 Hz. In Figure 32, channel 1 provides the voltage ripple across one of the bootstrap capacitors with 2 V/div; channel 2 displays the voltage ripple across +5 V capacitor with 2 V/div; channel 3 provides the voltage ripple at +15 V capacitor with 2 V/div; and channel 4 displays one of the phase currents with 100 A/div.

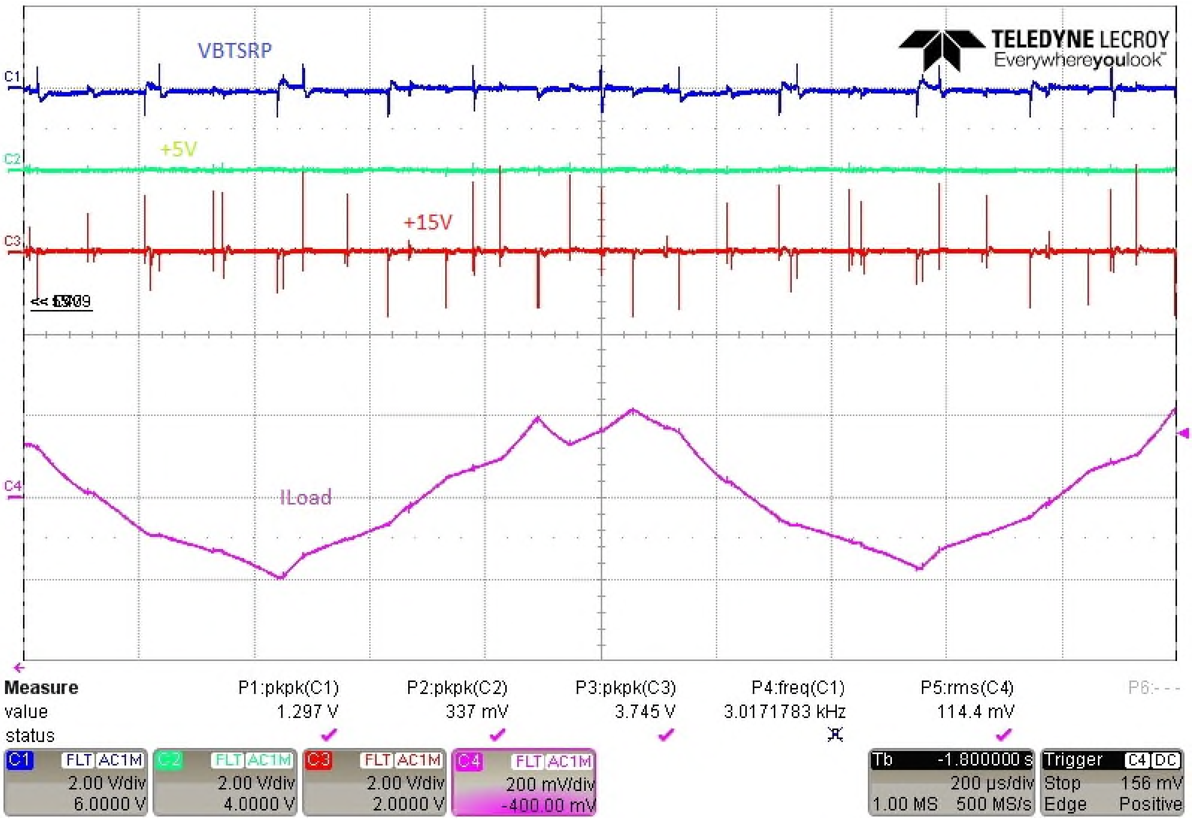

Figure 32 Voltage ripple across bootstrap capacitor, +5 V, +15 V and load current

8.4 Supply current variation

The bias current is monitored for +5 V and +15 V over the switching frequency of operation, and tabulated in Table 9 . This information is essential for the designer to identify a suitable auxiliary power supply. The 5-V supply current remains constant throughout the operating frequency range, however, during *off* conditions, there is a slight increase. There is a slight increase in the 15-V supply current, as the switching power increases with the rise in switching frequency.

Table 9 Supply current variation

Switching frequency	15 V supply	5 V supply
Off	110 mA	230 mA
1 kHz	120 mA	200 mA
4.52 kHz	130 mA	200 mA
7 kHz	135 mA	200 mA
10 kHz	140 mA	200 mA

8.5 Overcurrent detection

The theory of operation of the overcurrent detection is explained in Section 6.6. Overcurrent functionality was verified by connecting an inductor across one of the high-side switches, and a gate signal was applied to a different leg low-side switch. This condition creates a significant current spike and triggers the overcurrent detection. The gate voltage, phase current and fault signal were monitored as shown in Figure 33. Overcurrent detection occurs at around 90 A. Although the overcurrent set point is 100 A, there is a marginal drift due to operating voltage, reference voltage and temperature, as explained in the current sensor datasheet. In Figure 33, channel 1 represents the fault signal with 2 V/div; channel 2 the current through the inductor with 25 A/div; and gate-to-emitter voltage in channel 3 with 10 V/div.

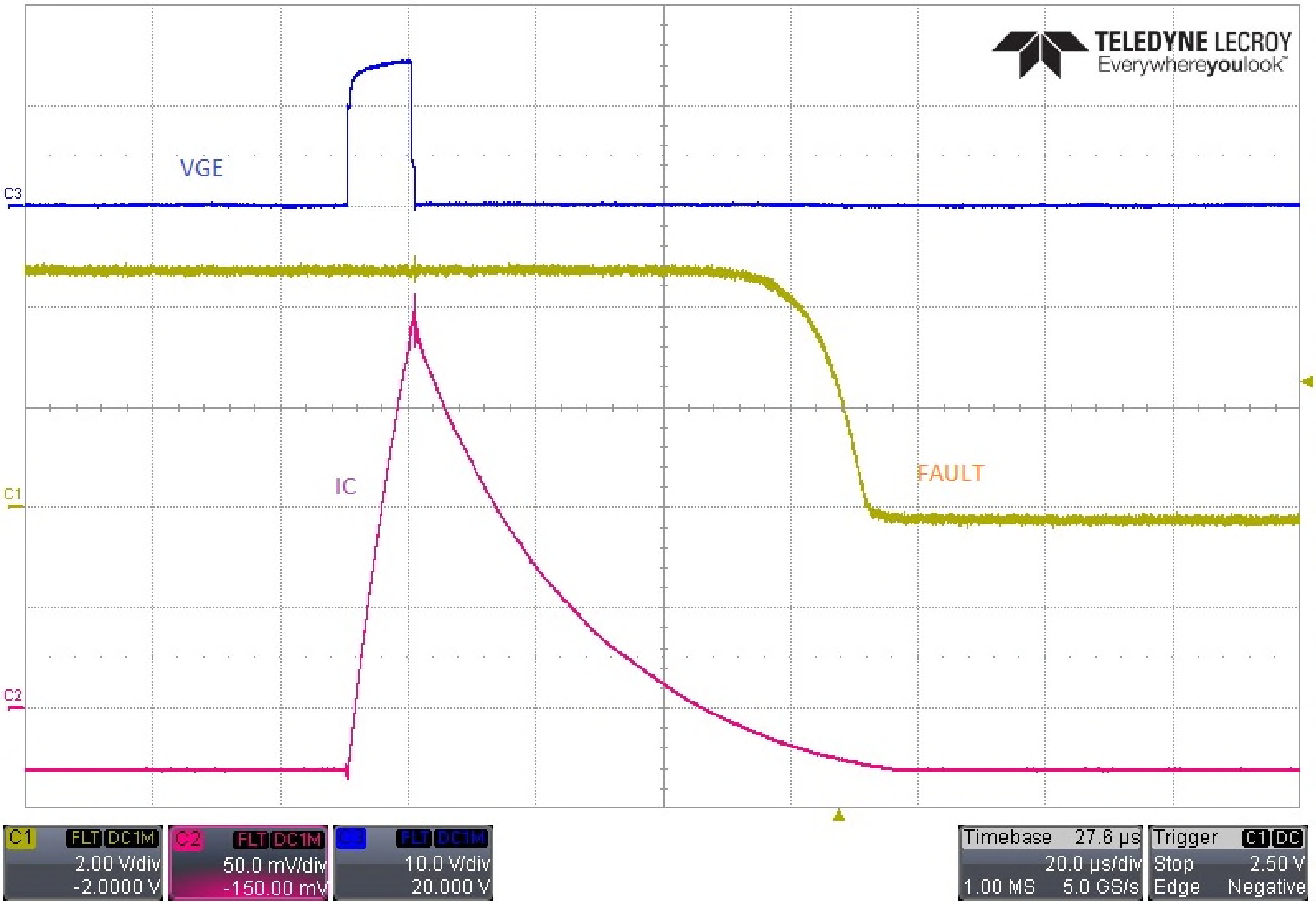

Figure 33 Overcurrent detection

8.6 Undervoltage functionality

The undervoltage functionality of the gate driver IC 2ED020I12-F2 was verified by powering the board normally, and abruptly removing the +15 V supply. Once the power supply is removed, the onboard capacitors start discharging. The undervoltage fault condition is triggered once the voltage goes below 11 V. This behavior is captured in Figure 34. In Figure 34, channel 1 is +15 V with 5 V/div, and channel 2 displays a fault signal with 2 V/div. The time of detection of UV functionality depends on the onboard capacitor size.

Figure 34 Undervoltage detection in +15 V supply

8.7 Short-circuit detection or desaturation functionality

The short-circuit or desaturation functionality detection is possible once the DESATLS or DESATHS pin of the 2ED020I12-F2 voltage exceeds 9 V. When the gate driver IC detects this condition, the output is driven low, and the fault output of the IC is activated.

The programmable blanking time is achieved by the capacitor and the internal current source. The designed blanking time value is 3.6 µs. The EiceDRIVER™ datasheet should be used as a reference to understand additional delay times.

In order to trigger the desaturation functionality of the low-side switch, the high-side switch is bypassed through a 0.6 Ω resistor, and a suitable gate pulse input is applied. In this case, 6 µs gate driver input was applied. The short circuit test was performed with a DC bus at 400 V, and the waveforms were captured and displayed in Figure 35. The short-circuit is detected once the DESATLS pin goes up and reaches 9 V as in Figure 35. Furthermore, even though a 6 µs gate pulse is the input to the gate driver, the gate-to-emitter pulse width is 4 µs, which explains that the gate driver output is driven low due to the short-circuit detection. In Figure 35, channel 1 represents the

voltage across the switch with 200 V/div; channel 2 displays the current through the 0.6 Ω resistor with 250 A/div; channel 3 is gate voltage with 10 V/div; and channel 4 is voltage at DESAT pin of IC with 10 V/div.

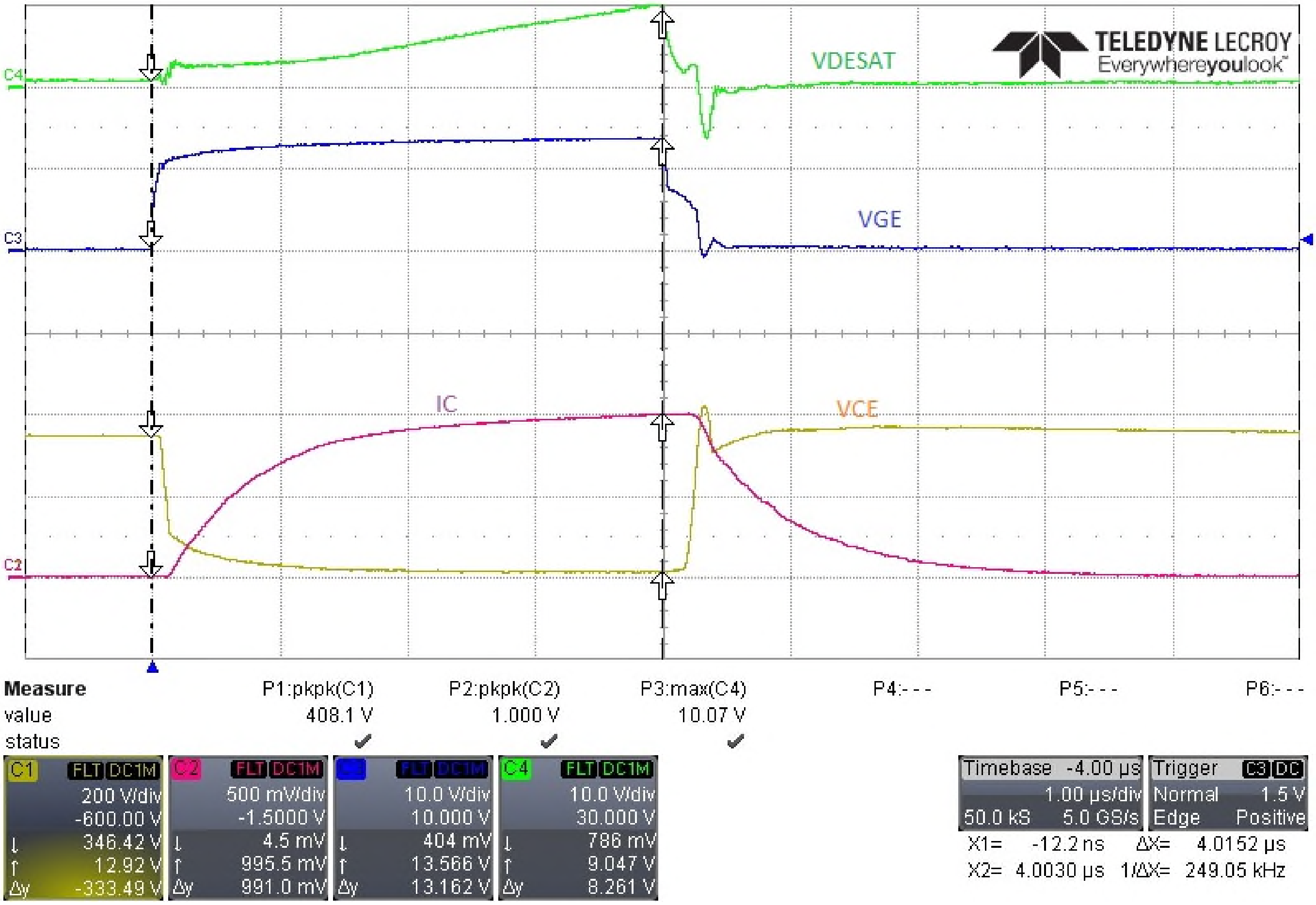

Figure 35 Short-circuit test – Detection of desaturation event of low-side switch

8.8 STO functionality

As explained in 5.1, the STO trigger may come from either the software or the hardware. This document focuses on STO functionality from hardware alone. Performance of the power board during STO events was tested by switching *off* the 24 V on the J4 connector, i.e., the STO line. Toggling the 24 V line is acceptable, as even in real time the external protection inputs disturbs only this STO line.

Once the STO 24 V is cut, the AND gate will open the relay which then cuts off the 15 V power line to the high-side gate driver switches. Based on the bootstrap capacitance, the high side +15 V will fall, and will eventually trigger the UVLO of the driver IC. This event was captured and displayed in Figure 36. Channel 1 displays the +24 V STO input with 20 V/div; channel 2 shows the high-side switch driver output waveform with 10 V/div; and channel 3 displays the bootstrap capacitor voltage with 10 V/div.

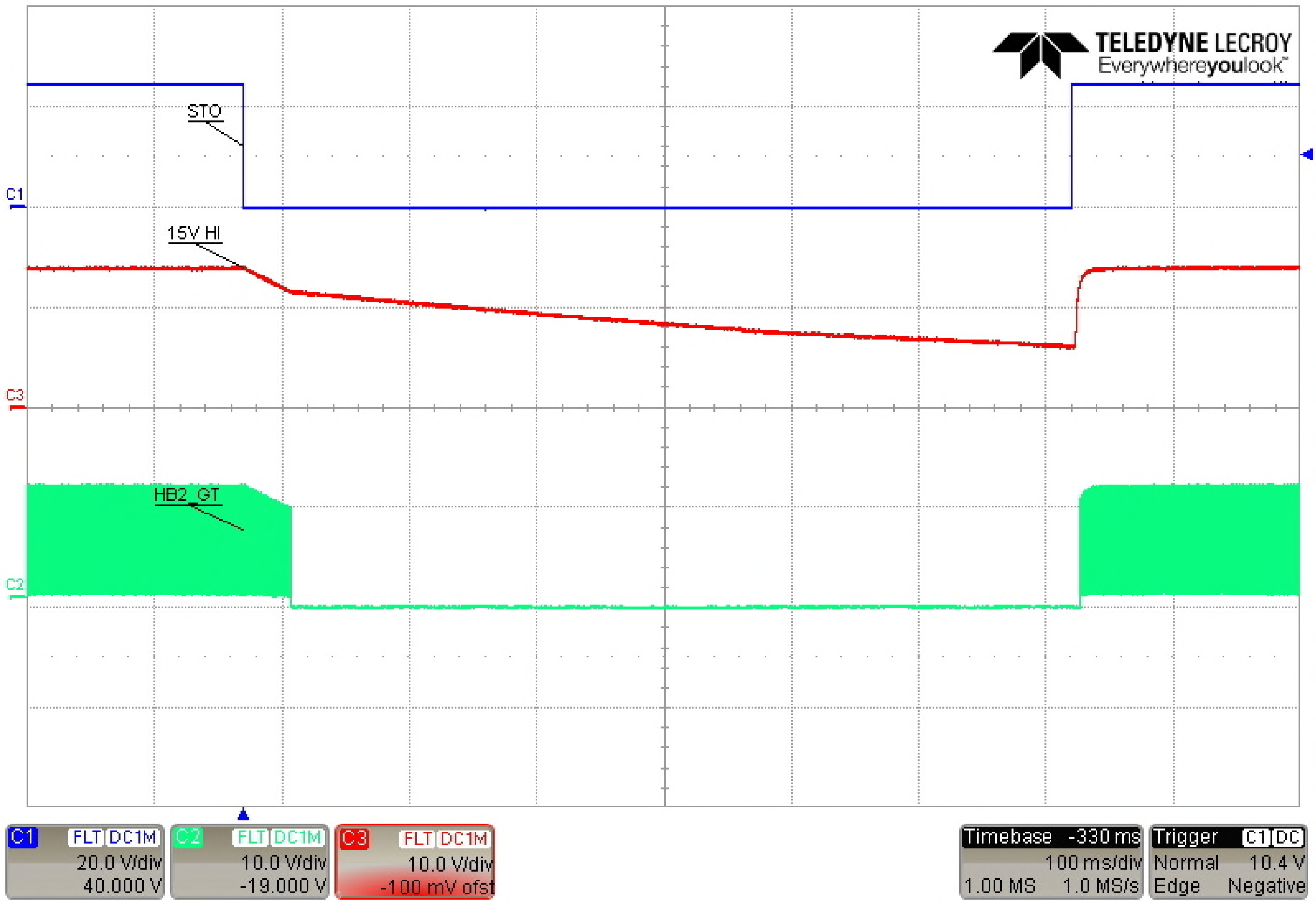

Figure 36 STO event

9. Test results of FP100R12KT4

This section provides the test results of the module FP100R12KT4. Although all the tests that were done for the FP150R12KT4 were repeated for FP100R12KT4, only switching loss alone will be discussed. The waveform in Figure 37 provides the switching loss details. Operating conditions are as follows:

- DC link voltage = 800 V
- Max. current = 100 A
- R_{gate} On = 6.8 Ω, R_{gate} Off = 6.8 || 6.8 Ω

Turn-on and turn-off losses mentioned in the datasheet are 5.5 mJ and 5.5 mJ, respectively, at 25°C and at 600 VDC. The switching loss numbers in the datasheet are different from the experimental results, as the operating parameters like gate resistor values, operating temperature and DC bus voltages are different.

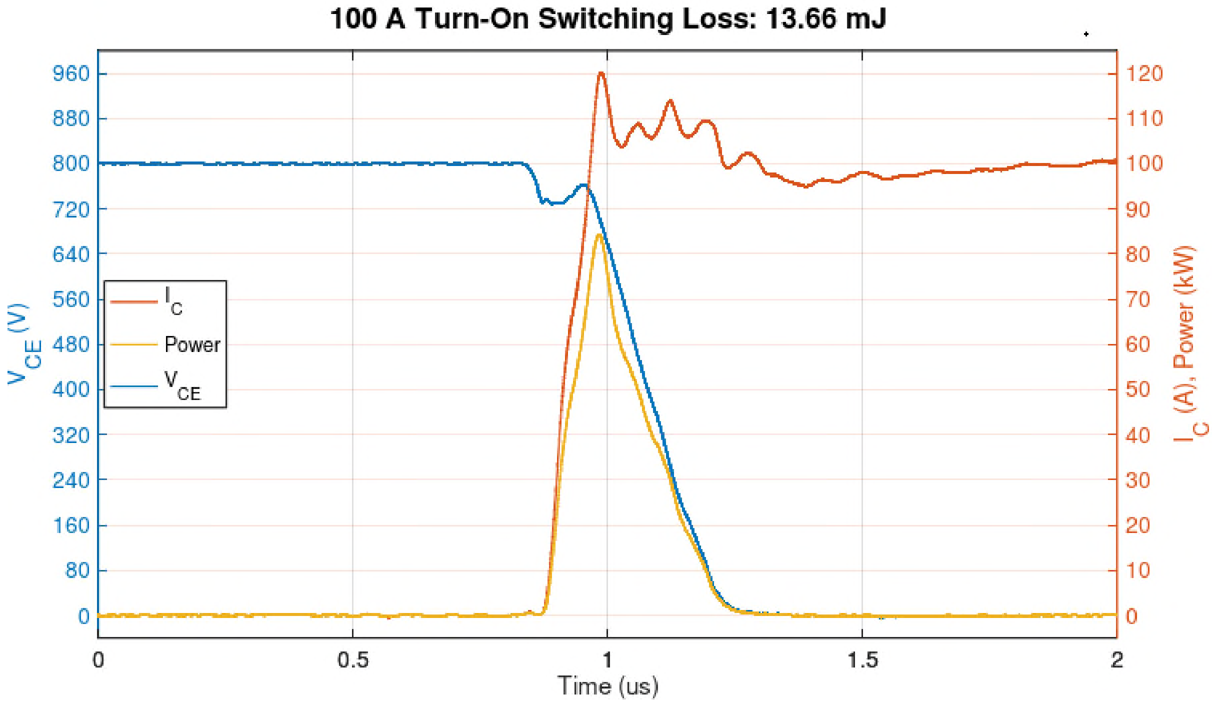

Figure 37 Switching on transition loss details

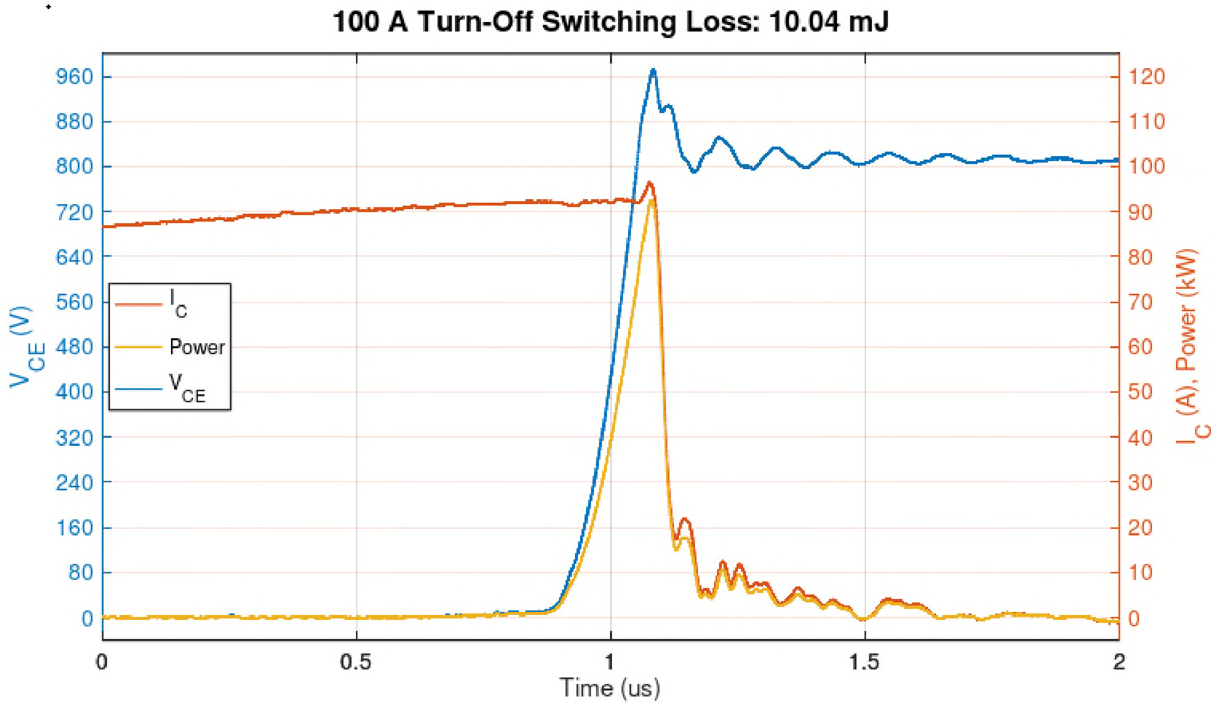

Figure 38 **Switching off transition loss details**

10. Ordering details and other information

The power board is available, and customers can order it in small quantities. PCB and Gerber details are also available and can be shared with customers after a suitable agreement has been reached.

In order to initiate the testing, customers are advised to order the following items:

- Infineon Reference Design Kit for Drives - power board for 30 kW GPD and CAC Applications
- Power modules FP150R12KT4/FP100R12KT4 based on the requirement. Usually power modules are not assembled with the power board.
- Control boards based on XMC4400 have to be ordered separately. Reference [4] provides the details of the control board. Customers are requested to discuss with Infineon before ordering the control board. Customers can also work with microcontrollers from other suppliers, provided they can match the control card connector in the power board.
- Infineon Reference Design Kit for Drives – auxiliary power supply using CooSiC™ MOSFET
- Heat sink and fan mentioned in this document or their equivalents

11. References

[1] http://www.leroy-somer.com/documentation_pdf/4545_en.pdf

[2] https://www.infineon.com/dgdl/Infineon-Board_Users_Manual_3phase_Power_Inverter_750W_R1.0-UM-v02_00-EN.pdf?fileId=db3a304343e0037c0143fc569bdf0047

[3] https://www.infineon.com/dgdl/Infineon-XMC4400-DS-v01_01-en.pdf?fileId=db3a30433afc7e3e013b3cfb455565a3

[4] https://www.infineon.com/dgdl/Board_Users_Manual_DriveCard_XMC4400_R1%200.pdf?fileId=db3a3043427ac3e201427f46ec9b2626

[5] https://www.infineon.com/dgdl/Infineon-2ED020I12_F2-DS-v02_00-en.pdf?fileId=db3a304333227b5e013344c70fc64cc8

[6] https://www.lem.com/sites/default/files/products_datasheets/ho-np_0100__1100_series.pdf

[7] IEC 61000-4-11: Testing and measurement techniques – voltage dips, short interruptions and voltage variations immunity tests

[8] https://www.infineon.com/dgdl/Infineon-AN2006_01_Driving_IGBTs_with_unipolar_gate_voltage-AN-v1.0-en.pdf?fileId=db3a304412b407950112b40ed1711291

[9] Ashish Bendre, Deepak Divan, William Kranz and William E.Brum Sickle, “Are voltage sags destroying equipment?”, IEEE Industry applications magazine, July-August 2006.

[10] Y. Lembeye, J.P. Keradec, and D. Lafore, “Measurement of losses of fast power switches: Impact of typical causes of inaccuracy,” in Proc. European Power Electronics, Seville, vol. 1, pp. 701–706, Sept. 19–21, 1995.

[11] https://www.infineon.com/dgdl/Infineon-HV_Floating_MOS_Gate_Drivers_AN978-AN-v01_00-EN.pdf?fileId=5546d462533600a40153559f7cf21200

12. Revision history

Document version	Date of release	Description of changes
Rev 1.0	2020-05-14	First release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-05-14
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email: erratum@infineon.com

Document reference
UG2018-29