

Two-level slew-rate control driver to optimize IGBT performance

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Abstract

It is difficult to optimize the switching performance of IGBTs with a single fixed value of gate resistor. This is especially true if the level of dv/dt during switching needs to be limited, as is the case for typical motor drives, or for applications where the conducted EMI levels need to be limited. This paper will present a simple two-level slew-rate control gate driver IC. The operating benefits for an industrial motor drive in terms of losses, maximum junction temperatures and switching frequency range will be shown.

1 Introduction

The dimensioning of the gate resistor that interfaces MOS-gated power transistors, such as IGBT or MOSFETs to the gate driver IC has generally two optimization targets [1]: First, the values of gate resistor should be set as low as possible to switch the power transistor switch fast to minimize dynamic losses, and hence, overall losses. Secondly, the gate resistor can also reduce the switching speed, e.g. dv_{CE}/dt or di_C/dt . This will trigger fewer oscillations, for example, of parasitic stray inductances in the gate circuit. A trade-off is therefore needed to find the relative optimum in a given layout. However, due to the limitation of a single fixed gate resistor value it can be selected to manage only one specific operating point, for example, a temporary overload or a low load condition, but not both. Such a limited choice can result in a less optimal switching speed than is desired for an application under normal operating conditions.

A typical case of a design-relevant condition is, for example, the low load operation of an electric motor drive. The current commutation from a diode, which conducts only low forward current to the opposite IGBT, can result in heavy oscillations if the turn-on of the opposite IGBT is too fast. These oscillations are strongly reduced, or even vanish if the forward current is in the range of 25% or more than the nominal current [2].

Conventional gate-drive circuits are fixed in terms of the gate-drive resistor. Therefore, the gate resistor is selected to cover all operating points for an application. It is not possible to apply a specific

gate-drive impedance to cover the most adverse point of operation, and to apply another gate impedance for the other points of operation.

It would be favorable if one could select a second gate impedance by means of a different gate resistor based on the monitoring of the operating conditions. Such driver circuits, which are able to change the switching speed during operation, are available on the market today. They are known as slew-rate-control ([2], [3]), active gate-drive circuits ([4], [5]) or slope-shaping gate-drive systems ([6], [7]). Such circuits are targeted for high-performance, high-power applications, and so their size, cost and complexity do not make them suitable for lower power and cost-sensitive converter designs.

The goal of this research was to design a very simple isolated gate driver with only eight terminals. It includes the ability to switch the value of gate resistor between two values, and implement this changeover on a PWM cycle-to-cycle basis.

2 Advantages of slew-rate-control gate drivers

The dv_{CE}/dt level during turn-on of an IGBT switching edge is typically higher at low temperatures and low currents. It is typical that the gate resistor value has to be increased to match the requirements of the application in terms of dv_{CE}/dt under a test condition of 1/10 nominal current at room temperature.

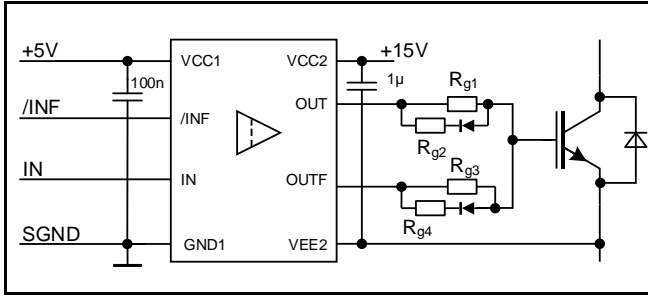


Fig. 1: Schematic of the proposed dual gate resistor gate drive circuit

Such limitations of dv_{CE}/dt are common in motor drives. Detrimental effects of high dv_{CE}/dt on motors are possible including voltage doubling at the motor windings with longer motor cables, high-step voltage changes across stator end windings, bearing currents and track pitting, and an increase in peak capacitive currents to ground in the system e.g. from heatsink and motor case to ground ([8], [9]).

Now this higher value of gate resistor, while allowing the dv_{CE}/dt levels to be limited, causes higher switching losses, and so reduces the converter efficiency. It also causes higher junction temperatures, and reduces lifetimes of power modules.

However, system gains can be achieved if a dual gate resistor can be utilized. This enables a higher value of gate resistor to be used at low currents and low temperatures thus limiting dv_{CE}/dt levels, and a lower value of gate resistor used at higher currents and temperatures to reduce switching losses.

Fig. 1 shows a schematic for the drive circuit. It has a single command input /INF for fast or slow, and a separate command input IN for the PWM signal. For fast operation, both output stages switch at the same time, so the IGBT gate is driven by a combination of R_{g1} and R_{g3} in parallel. During slow operation, the IGBT is driven only by R_{g1} .

The correlation between the effective values R_{gslow} and R_{gfast} of the resistors according to Fig. 1 is for turn-on

$$R_{gslow} = R_{g1} \quad (1)$$

$$R_{gfast} = \frac{R_{g1} + R_{g3}}{R_{g1}R_{g3}} \quad (2)$$

The two values R_{gslow} and R_{gfast} are used throughout this paper instead of R_{g1} and R_{g3} , because they are easier to understand.

3 Characterization data set

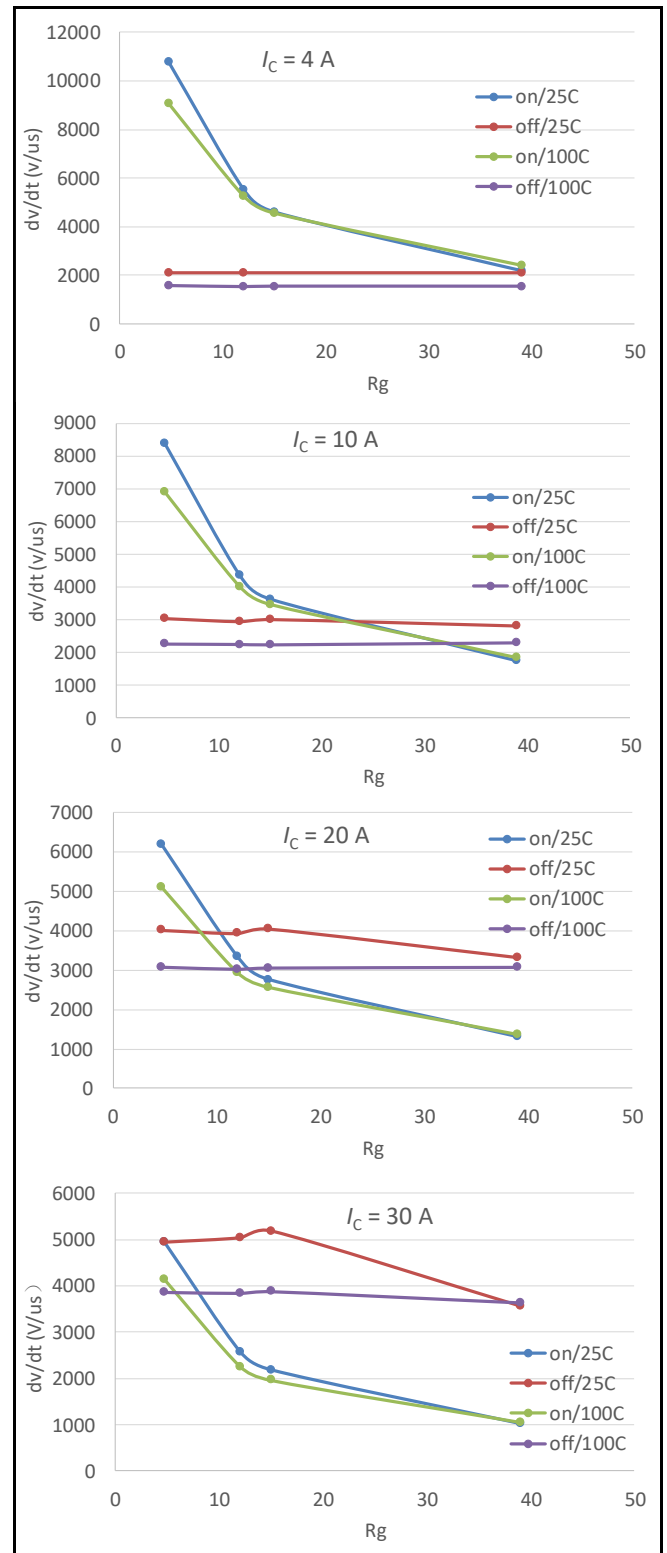


Fig. 2: Characterization data of a 35 A / 1200 V IGBT 7 power module for the collector-emitter slew rates of turn-on and turn-off at junction temperature 25°C and 100°C

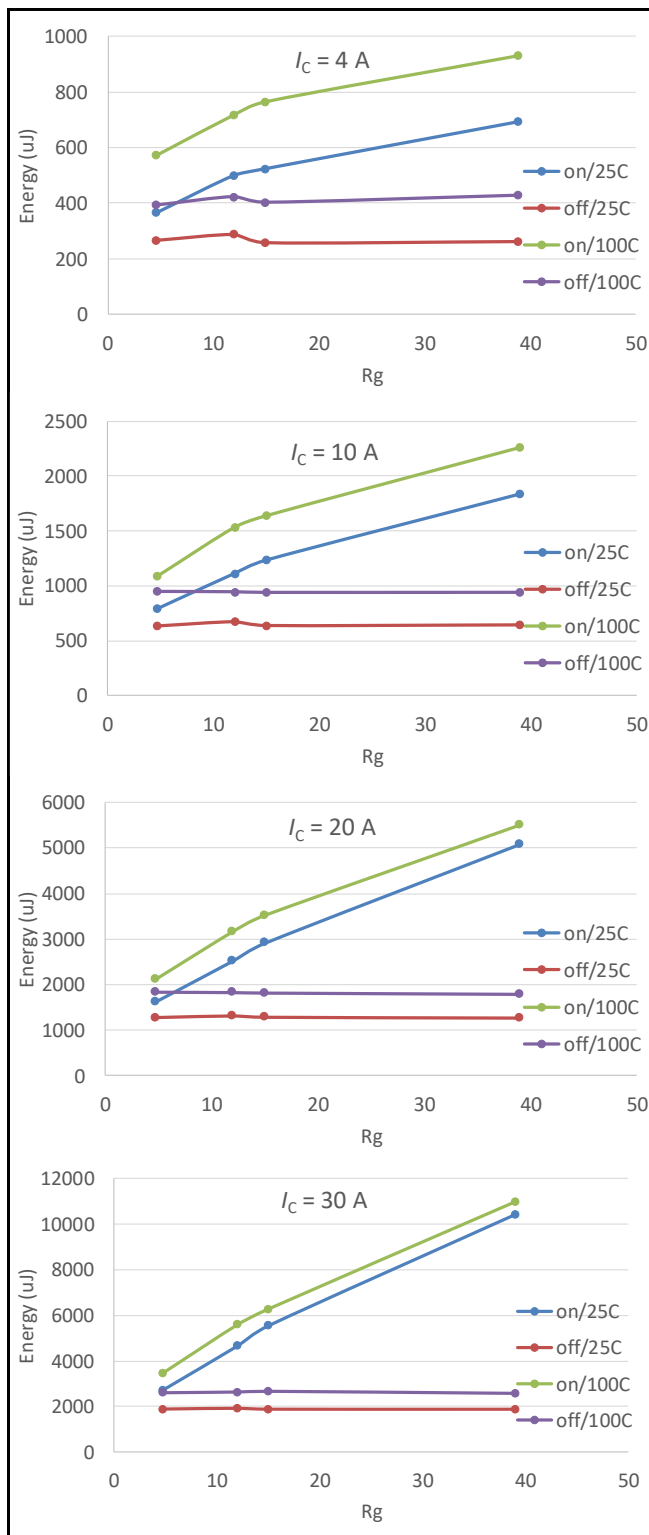


Fig. 3: Characterization data of a 35 A / 1200 V power module for the turn-on and turn-off energies at junction temperature 25°C and 100°C

A double-pulse characterization was performed to obtain the fundamental dependencies between the collector-emitter turn-on dv_{CE}/dt and collector

current, gate resistance and temperature. The test conditions for the data shown in Fig. 2 and Fig. 3 are as follows:

DC-link voltage $V_{DC} = 650$ V

Positive gate voltage: $V_{g,pos} = 14$ V

Negative gate voltage: $V_{g,neg} = -7.5$ V

Junction temperatures: $T_j = 25^\circ\text{C} / 100^\circ\text{C}$

The data for the dv_{CE}/dt in Fig. 2 is from a measurement of the $v_{CE}(t)$ 90%-10% waveforms. The dv_{CE}/dt for turn-on is strongly influenced by the value of gate resistance R_g . This provides an opportunity to adjust the EMI in a given system.

For turn off, the dv_{CE}/dt is quite constant over a wide range of gate resistances, but increases significantly with higher collector current values. Here, the higher collector current charges the output capacitance of the IGBT much faster than a lower collector current. Above approximately half of the nominal current, the dv_{CE}/dt is reduced with gate resistances of 15 Ω and larger. This can be seen in the lower two graphs of Fig. 2.

Fig. 3 depicts the switching energies for turn-on and turn-off as a function of the gate resistance. The turn-off energy is almost independent of the gate resistance. However, the turn-on energy is constantly increasing, correlating to the decreasing turn-on dv_{CE}/dt of Fig. 2.

Of course, diode-relevant data is available, such as the recovery energy E_{rec} . However, that data is not presented in Fig. 2 and Fig. 3.

4 Simulation setup

The characterization data set is entered into an IGBT and diode model. A simulation environment is setup consisting of an induction motor and a standard 6-pack topology, see Fig. 4.

The electrical conditions for the simulation are:

DC-link voltage $V_{DC} = 560$ V

Switching frequency $f_p = 8$ kHz

Motor frequency $f_{mot} = 50$ Hz

Fast-to-slow change point for the gate resistance: $I_{chg} = \pm 5$ A

Fixed heat sink temperature: $T_{HS} = 100^\circ\text{C}$

$\cos \phi = 0.8$

Modulation scheme: sine wave modulation

The proposed system model allows the value of gate resistor to be changed at any different operating point using variables such as a specific collector current, a temperature or other physical parameters.

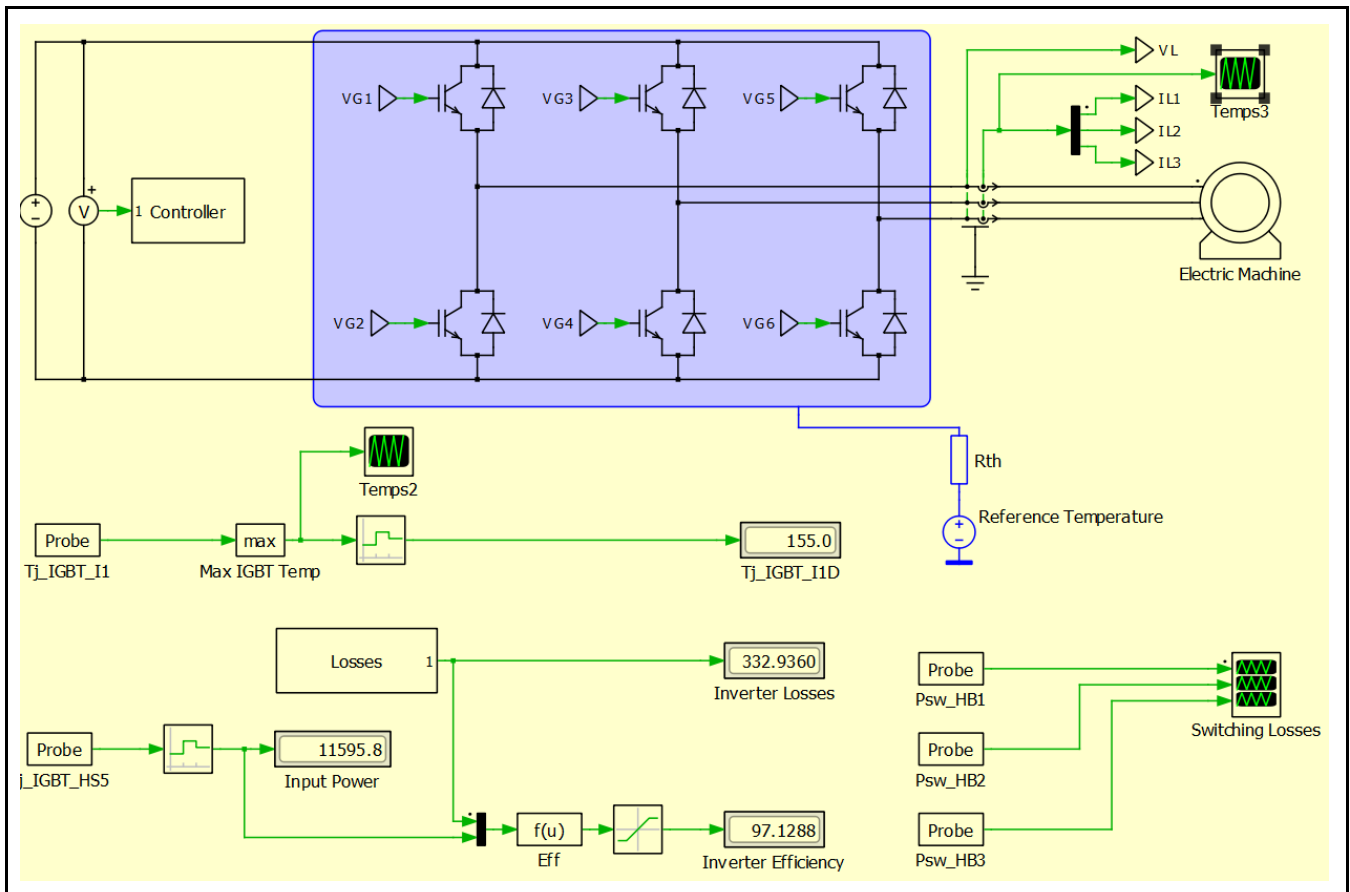
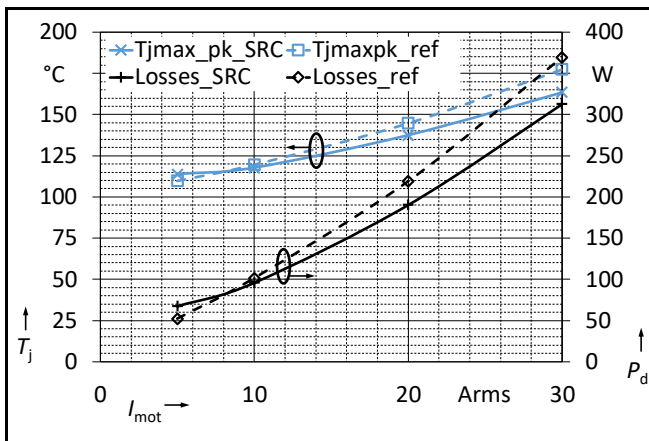


Fig. 4: Simulation setup using PLECS

Fig. 5: Simulation results of conventional (reference) and proposed two-level SRC gate driver circuit ($I_{chg} = 5$ A, $f_p = 8$ kHz)

Combinations of the above-mentioned parameters are also allowed.

To evaluate the potential efficacy of this type of two-level SRC driver, a set of reference conditions were simulated and compared with a conventional standard single fixed value of turn-on and turn-off gate resistor. The resistor values selected were

$R_{goff} = 5.6 \Omega$ and a turn-on gate resistor $R_{gon} = 15 \Omega$. The R_{gon} value limits the dv_{CE}/dt to 5 V/ns at 4 A and 25°C as shown in Fig. 2 top curve.

The simulation results under this reference condition are compared in Fig. 5 to the results using the proposed gate drive with a fast turn-on gate resistor $R_{gfast} = 5.6 \Omega$ and a slow turn-on gate resistor $R_{gslow} = 56 \Omega$. The changeover point from R_{gfast} to R_{gslow} and vice versa is selected at a motor current of ± 5 A. Of course, $R_{gslow} = 56 \Omega$ is a relatively large value compared to the reference. However, very often the low load operation is critical for EMI [10] and R_{gslow} is able to slow down current commutations at low load operation.

One can see that the selected two-level SRC gate resistances have a direct influence on the simulation results. The two-level SRC case uses a larger turn-on resistance, and so dissipates more power resulting in a higher peak junction temperature at low motor current amplitudes. For example, the power dissipation of the reference using $R_{gon} = 15 \Omega$ is $P_{d,ref} = 52$ W at a collector current of $I_c = 5$ A, while the two level SRC gate drive dissipates $P_{d,SRC} = 67.4$ W. However, this increase in losses only applies when operating at

low current levels, where the overall losses are low, but the trade-off advantage of using the larger gate value under these conditions comes from a reduced dv_{CE}/dt level from 5 V/ns to less than 2 V/ns, see Fig. 2, and the possibility of reduced EMI levels.

The real value of the proposed slew-rate control driver is visible when operating at higher motor currents, for example, above 9 A according to Fig. 5. Here, the two-level SRC driver yields consistently lower losses and lower peak junction temperatures.

For example, with the reference design, the maximum output current for a temperature limit of $T_j = 155^\circ\text{C}$ is 26 A r.m.s., but with the two-level SRC it is 30 A r.m.s., a 15% increase. This advantage can be even greater when considering comparisons at higher junction temperatures.

5 Variation of the changeover point

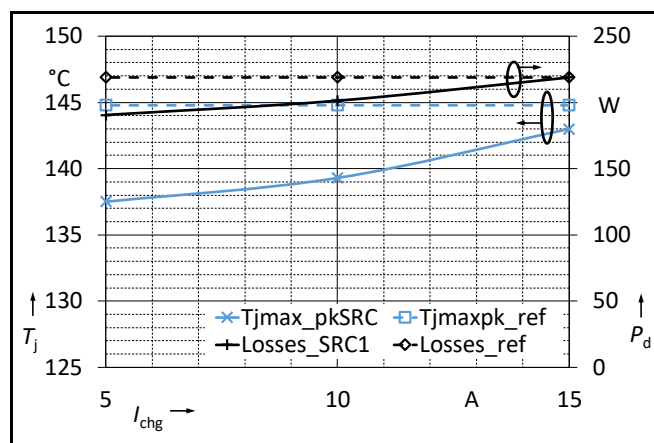


Fig. 6: Simulation results of conventional gate drive ($R_{gon} = R_{goff} = 15 \Omega$) and proposed gate drive circuit with a changeover point of ± 5 A, ± 10 A and ± 15 A ($R_{gslow} = 56 \Omega$, $R_{gfast} = 5.6 \Omega$, $R_{goff} = 5.6 \Omega$) at $f_p = 8$ kHz.

This section compares simulation results of the reference case with possible changeover points of ± 5 A, ± 10 A and ± 15 A. The changeover point defines the ranges where R_{gslow} and R_{gfast} are active. Lower changeover points than ± 5 A are possible of course, but also jeopardize the effect of the proposed scheme, because the changeover point should not interfere with the EMI-sensitive area of low motor current commutations. Fig. 6 shows the simulation results for the above-mentioned changeover points at a fixed switching frequency of $f_p = 8$ kHz.

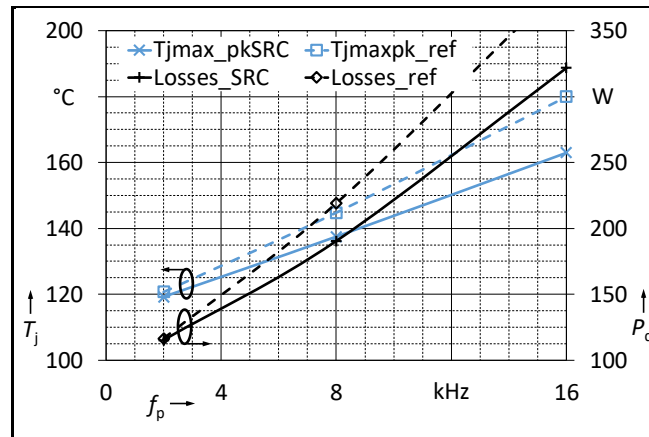


Fig. 7: Simulation results of the conventional gate drive and the new gate drive circuit with switching frequencies of 2 kHz, 8 kHz and 16 kHz at a motor current of 20 A and a changeover point of ± 5 A.

The lower the changeover point value, the higher is the advantage of the proposed gate drive concept with the largest advantage at a change point at 5 A. On the other hand, a higher changeover point can allow even lower values for R_{gfast} . This can compensate for the use of R_{gslow} in a wider range of motor current.

6 Variation of the switching frequency

Fig. 7 shows the simulation results at switching frequencies of 2 kHz, 8 kHz and 16 kHz, while the motor current is fixed to 20 A r.m.s. The switching frequency is a big leverage for using the proposed two-level SRC driver. On the one hand, each and every turn-on contributes to the overall losses. Therefore, the overall losses increase with higher switching frequency for both the conventional gate drive (reference) as well as for the proposed scheme. The operating point with a motor current of $I_{mot} = 20$ A r.m.s., $I_{chg} = \pm 5$ A and $f_p = 2$ kHz results with almost the same losses and junction temperatures. However, increasing the switching frequency leads to lower losses over the compared range of switching frequencies for the two-level SRC driver, as shown in Fig. 7.

For example, one can reach a higher switching frequency, approximately 4 kHz higher, for the same junction temperature of $T_j = 160^\circ\text{C}$. This advantage can be used to reduce the ripple current portion of the motor current.

7 Conclusion

A new gate drive circuit has been proposed, which allows the gate resistance value to be changed on the fly. It enables a better optimization of electric motor drive losses, dv_{CE}/dt and EMI. A two-fold optimization was explained showing benefits in the low load range with respect to dv_{CE}/dt limits, but also having a better optimization in the mid and high load range for reduced power dissipation. Simulation results based on characterization measurements highlighted that the proposed gate drive circuit can provide real system benefits under various operating conditions.

This optimization of the gate drive resistor value results in lower power losses of 10% or even more depending on the operating point with respect to switching frequency, changeover point and junction temperature. This is the key to achieving increased power density or better utilization of a given power module.

8 References

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