Customer Training Workshop

Traveo™ II Time Division Multiplexed (TDM)/Inter-IC sound (I²S) Interface
Target Products

- Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Cluster

› Time Division Multiplexed (TDM) / Inter-IC sound (I²S) Interface is part of Peripheral blocks

Review TRM chapter 33 for additional details
Introduction to TDM/I²S Interface

› Overview
  - TDM/I²S interface consists of a TDM transmitter and a TDM receiver, which can function with multiple channels simultaneously. I²S interface is obtained as a special case of TDM.

› Features
  - Combined I²S and TDM functionality
  - Master and slave functionality
  - Full-duplex transmitter and receiver operation
  - Support for up to 32 channels
  - Programmable interface clock
  - Programmable channel size (up to 32 bits)
  - Programmable late capture extra delay of 1, 2 or 3 cycles
  - Delayed sampling support
  - Programmable Pulse Code Modulation (PCM) sample formatting (8, 10, 12, 14, 16, 18, 20, 24, and 32 bits)
  - Left-aligned and right-aligned sample formatting
  - 128-entry TX and RX FIFOs with interrupt and trigger support
Block Diagram

- **TDM/I²S components**
  - TDM/I²S interface
    - Clock
    - TDM/I²S pair (transmitter, receiver)
    - SRAM

SRSS clock (CLK_IF_SRSS[3:0]) is dependent on the device.
CLK_GR: Clock input to peripheral functions.
TDM/I²S interface clock can be derived from either of these clock signals:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_IF_SRSS[3:0]</td>
<td>SRSS clock</td>
</tr>
<tr>
<td>TDM_MCK_IN</td>
<td>Master clock input</td>
</tr>
</tbody>
</table>

An interface clock (CLK_IF) is derived and then gated to derive the TDM clock.

Note: See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy.
Operation Modes

- Each TDM transmitter and receiver can be configured independently.
- Masters output the TDM clock and Frame synchronization; slaves take the same signals as inputs.

![Diagram of TDM transmitter and receiver configurations]

Review TRM section 33.2.3 for additional details.
I²S Modes

› When the below programming is applied, the transmitter operates according to the I²S protocol:
  - Number of channels equal 2:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.CH_NR = 1
  - FSYNC format over the channel:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.FSYNC_FORMAT = 1
  - FSYNC polarity inverted:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.FSYNC_POLARITY = 1
  - I²S mode setting:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.I2S_MODE = 1

› The receiver also operates according to the I²S protocol:
  - For RX the below register programmed:
    - TDMx_TDM_STRUCTy_TDM_RX_STRUCT_RX_IF_CTL.
Master Clock Output

- TDM_TX_MCK is derived from the fractional PLL to support typical external clock rate for an external audio codec

<table>
<thead>
<tr>
<th>Sampling Rate (Fs) [kHz]</th>
<th>Master Clock Frequency (TDM_TX_MCK) [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TDM_TX_MCK / Fs = 256</td>
</tr>
<tr>
<td>32</td>
<td>8.1920</td>
</tr>
<tr>
<td>44.1</td>
<td>11.2896</td>
</tr>
<tr>
<td>48</td>
<td>12.2880</td>
</tr>
</tbody>
</table>

- Master Clock Output Signal for the External Audio Codec

Review TRM section 33.2.6 for additional details
Transfer Format

Example: Transfer for eight channels, with only channels 0 and 7
- Channels can be enabled individually

Example: 24-bit Channel Size and 20-bit Word Size Format
- PCM data word size is potentially smaller than the channel size
- PCM data word is either left-aligned or right-aligned within the channel

If the data word is left-aligned, a receiver ignores the trailing four bits in the channel

If the data word is right-aligned, a receiver ignores the leading four bits in the channel
Late Capture

- The TDM/I²S interface supports a programmable extra delay:
  - Pushes out the capturing edges used by the receiver to sample TDM_RX_SD
  - Intended to support very large round-trip delays in a master receiver configuration
  - The timing diagrams below illustrate how the receiver interprets the bits of the received TDM frame
    - Late Capture with Non-delayed Format and Late Sample = 0
    - Late Capture with Delayed Format and Late Sample = 1

Review TRM section 33.2.8 for additional details

Hint Bar

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Interfacing with Audio Codecs having Common WS and SCK Signals

› Connections for Codecs with separate WS and SCK signals for RX and TX directions

› Connections for Codecs with common WS and SCK signals for RX and TX directions

Review TRM section 33.2.9 for additional details
The transmitter and receiver have a dedicated FIFO
- Common SRAM is used for all TX and RX FIFOs; each FIFO uses 128 32-bit entries
- Transmitter transmits PCM words from the TX FIFO and a receiver receives PCM words into the RX FIFO
- It is possible to enable/disable the individual channels within a frame
- Disabled channels do not have PCM words in the FIFOs
- When multiple channels are enabled, the channels have their PCM words interleaved in the FIFOs

FIFO

CH_NR = "1", CH0_EN/CH1_EN = ‘1’

-channel 0 PCM i
-channel 1 PCM i
-channel 0 PCM i+1
-channel 1 PCM i+1
-channel 0 PCM i+2
-channel 1 PCM i+2

64 entries

FIFO

CH_NR = "3", CH0_EN/CH1_EN/CH3_EN = ‘1’

-channel 0 PCM i
-channel 1 PCM i
-channel 3 PCM i
-channel 0 PCM i+1
-channel 1 PCM i+1
-channel 3 PCM i+1

64 entries

Review TRM section 33.2.10 and Register TRM for additional details
## Interrupt

The following events trigger a TDM interrupt:

<table>
<thead>
<tr>
<th>TX Interrupt</th>
<th>Set Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_TRIGGER</td>
<td>TX trigger is generated.</td>
</tr>
<tr>
<td>FIFO_OVERFLOW</td>
<td>Writing to a full TX FIFO (TX_FIFO_STATUS.USED is “128”).</td>
</tr>
<tr>
<td>FIFO_UNDERFLOW</td>
<td>Reading from an almost empty TX FIFO (TX_FIFO_STATUS.USED &lt; “number of enabled channels per frame”).</td>
</tr>
<tr>
<td>IF_UNDERFLOW(^1)</td>
<td>PCM samples are generated too fast by the interface logic. May indicate that the IP system frequency is too low with respect to the interface frequency (a SW configuration error).</td>
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<table>
<thead>
<tr>
<th>RX Interrupt</th>
<th>Set Condition</th>
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<tr>
<td>FIFO_TRIGGER</td>
<td>RX trigger is generated.</td>
</tr>
<tr>
<td>FIFO_OVERFLOW</td>
<td>Writing to an almost full RX FIFO (128 -RX_FIFO_STATUS.USED &lt; “number of enabled channels per frame”).</td>
</tr>
<tr>
<td>FIFO_UNDERFLOW</td>
<td>Reading from an empty RX FIFO (RX_FIFO_STATUS.USED is “0”).</td>
</tr>
<tr>
<td>IF_UNDERFLOW(^1)</td>
<td>PCM samples are generated too fast by the interface logic. May indicate that the IP system frequency is too low with respect to the interface frequency (a SW configuration error).</td>
</tr>
</tbody>
</table>

\(^1\) This functionality is for debug purposes
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<tbody>
<tr>
<td>**</td>
<td>6677245</td>
<td>09/18/2019</td>
<td>Initial release</td>
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<tr>
<td>*A</td>
<td>6809284</td>
<td>02/18/2020</td>
<td>Added note descriptions in each slide</td>
</tr>
<tr>
<td>*B</td>
<td>7053683</td>
<td>12/24/2020</td>
<td>Updated page 2, 3, 4, 5, 6, Added 8, 9, 11, 12</td>
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