Customer Training Workshop

Traveo™ II Sound Generator

Q4 2020
Target Products

Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo™ II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Cluster

The Sound Generator (SG) is part of Peripheral Blocks
Sound Generator (SG) Overview

- SG produces PWM tone and amplitude signals
  - Tone signal is used to generate sound frequencies
  - Amplitude signal is used for volume control
- Features
  - PWM-modulated (amplitude, tone) sound generation
  - Double-buffered segment structure control
  - Two operating modes
    - Separate volume and frequency control (two signals) format
    - Combined volume-frequency control (one signal) format
  - Programmable interface clock
SG Block Diagram

- **SG components**
  - Transmitter block
  - Clock
  - Output signals and segment structure
  - Double buffering
  - Audio waveform composition
  - Interrupt

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1. Number of transmitters (n) varies by device
2. See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

Hint Bar

Review TRM section 33.5.2 for additional details

CLK_GR: Clock input to peripheral functions, which is grouped by the clock gater.
PWM Interface Clock

- PWM interface clock can be derived from either of these clock signals:

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_IF_SRSS[3:0]</td>
<td>SRSS clock</td>
</tr>
<tr>
<td>SG_MCK_IN</td>
<td>Master interface clock</td>
</tr>
</tbody>
</table>

- An interface clock (CLK_IF) is derived and then gated to derive the PWM clock:


  Clock gater

  SGx_SG_STRUCTy_IF_CTL.CLOCK_DIV → CLK_IF

  “PWM clock”

  SG_MCK_OUT

- PWM clock drives the SG_AMPL_OUT and SG_TONE_OUT lines and its resolution determines the amplitude PWM period frequency

  See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0]

Hint Bar

Review TRM section 33.5.3 for additional details
SG_AMPL_OUT: Amplitude output
SG_TONE_OUT: Tone output
Review the Clock System Training section for additional details about high-frequency clocks
Output Signals and Segment Structure (1/2)

- SG creates amplitude signals (SG_AMPL) and PWM tone signals (SG_TONE)
  - Amplitude determines how loud the sound will be
  - Tone determines the pitch of the sound
- To control the output of SG_AMPL and SG_TONE, SG uses four 32-bit segment structure registers

<table>
<thead>
<tr>
<th>Segment Structure</th>
<th>Description</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude</td>
<td>Specifies the volume of the sound</td>
<td>AMPL_CTL</td>
</tr>
<tr>
<td>Tone</td>
<td>Specifies the frequency of the sound</td>
<td>TONE_CTL</td>
</tr>
<tr>
<td>Time</td>
<td>Specifies how long a certain tone is played</td>
<td>TIME_CTL</td>
</tr>
<tr>
<td>Step</td>
<td>Specifies whether the volume is constant, decreasing, or increasing</td>
<td>STEP_CTL</td>
</tr>
</tbody>
</table>
Output Signals and Segment Structure (2/2)

- Segment structure
  1. A single amplitude period is 
     (AMPL_CTL.PERIOD + 1) PWM clock cycles
  2. The high time of an amplitude period is specified by 
     (AMPL_CTL.HIGH + 1) PWM clock cycles
  3. A single tone period is two times the 
     (TONE_CTL.PERIOD + 1) amplitude periods
  4. The high time of a tone period is defined by 
     (TONE_CTL.HIGH + 1) amplitude periods
  5. A single time period is (TIME_CTL.PERIOD + 1) tone periods
  6. A single segment is (TIME_CTL.NR + 1) time periods
Double Buffering

› To generate sound continuously, double-buffered structures are used
› Current structure can control the sound generation process
› Buffered structure can be updated by a CPU or P-DMA
› When the current structure is complete, a completion event is activated, and the buffered structure is copied to the current structure

\[^1\] Excluding Start bit or Stop bit

[Hint Bar]

Review TRM section 33.5.5 for additional details
Audio Waveform Composition

- In the diagram, multiple segments are used to describe a sound signal
- After each segment, hardware
  1. Activates a completion event that
     - Updates the current segment's structure with information of the buffered segment structure
     - Activates tr_complete trigger
     - Activates INTR_TX.COMPLETED interrupt cause
  2. If the completion event is not followed by a buffered segment structure, it activates an underflow event and the sound generation ends
Audio Waveform Composition

Audio Waveform Composition Example

6 Segments:
- segment 0: 5 time periods
- segment 1: 1 time period
- segment 2: 5 time periods
- segment 3: 5 time periods
- segment 4: 3 time periods
- segment 5: 2 time periods

Segment 0
Segment 1
Segment 2
Segment 3
Segment 4
Segment 5

Segment 1
Segment 2
Segment 3
Segment 4
Segment 5

"Buffered" segment structure

“completion” event

“underflow” event

STEP_CTL.STEP

Amplitude height after each time period 
(AMPL_CTL.HIGH + 1)

1 time period (TIME_CTL.PERIOD + 1 time periods)

1 segment (TIME_CTL.NR + 1 time periods)
A sound generator interrupt can be triggered by any of the following events:

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Set Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTR_TX.COMPLETE</td>
<td>A segment descriptor is complete</td>
</tr>
<tr>
<td>INTR_TX.UNDERFLOW</td>
<td>A new segment structure is not available</td>
</tr>
<tr>
<td>INTR_TX.IF_UNDERFLOW(^1)</td>
<td>Sample pairs (amplitude, tone) are not generated in time for the interface logic. It may indicate that the SG block system frequency is too low with respect to the interface frequency (a SW configuration error)</td>
</tr>
</tbody>
</table>
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## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
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<tbody>
<tr>
<td>**</td>
<td>6638977</td>
<td>07/29/2019</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6805395</td>
<td>02/12/2020</td>
<td>Added note descriptions in each slide</td>
</tr>
<tr>
<td>*B</td>
<td>7053619</td>
<td>12/24/2020</td>
<td>Updated page 2, 5, 6</td>
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