Customer Training Workshop
Traveo™ II SAR ADC

Q4 2020
## Target Products

### Target product list for this training

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Body Controller Entry

SAR ADC is part of the peripheral blocks

- I/O Subsystem
  - Peripheral Interconnect (MMIO, PPU)
  - Digital DFT
  - Analog DFT
  - System Resources
    - Power
      - Reset
      - Clock
      - Clock Control
    - Clock
      - PLL, LDO
    - System Resources
      - Power Management
      - Low Power Active/Sleep
        - DeepSleep
        - Hibernate
      - Low Power Active/Sleep
      - Deep Sleep
      - Hibernate

- CPU Subsystem
  - Arm Cortex-M4
    - 160 MHz
  - SRAM0
    - 256 KB
  - SRAM1
    - 256 KB
  - Cortex AES, SHA, CRC, TRNG, RSA, ECC
  - Crypto
  - MPU/SMPU
  - System Interconnect
    - Multi Layer AHB, IPC

- Peripheral Resource
  - SAR ADC (12-bit)
    - x3
  - SARMUX 64 ch
  - Status/Control
  - System Resources
    - Power Management
    - Low Power Active/Sleep
    - Deep Sleep
    - Hibernate

- System Resources
  - Power
    - PWRSYS HT
    - REF
    - POR
  - Sleep Control
    - XRES
    - LVD
    - BOD
    - OVD
  - Clock Control
    - IMO
    - WDT
    - CSV
    - 1xPLL
    - ECO
    - 2xILO
    - FLL
    - TCPWM
    - TIMER, CTR, QD, PWM

- I/O Subsystem
  - 5x Smart I/O
  - 8x CANFD
  - 8x CANFD Interface
  - eFUSE
  - 1024 bit

- ROM
  - 32 KB
  - Flash Controller
  - 8 KB
  - 8 KB
  - SRAM1
    - 256 KB
  - SRAM Controller
  - SRAM0
    - 256 KB
    - 25 KB

- CYT2BL
  - MXS40-HT
  - ASIL-B

- More Details
  - Review TRM chapter 31 for additional details

- Copyright © Infineon Technologies AG 2020. All rights reserved.
Introduction to Traveo II Body Controller High

- SAR ADC is part of the peripheral blocks

---

**CPU Subsystem**

- Arm Cortex-M7 350 MHz
- eCT Flash 8384KB Code flash + 256KB Work flash

**System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)**

- Peripheral Interconnect (MMIO, PPU)
- High-Speed I/O Matrix, Smart I/O, Boundary Scan

**I/O Subsystem**

- Up to 196 x GPIO STD, 4x GPIO_ENH, 40x HSIO

**System Resources**

- Power
  - Sleep Control
  - POR / BOD
  - OVP / LVD
  - REF
  - PWRSYS-SS
  - LDO

- Clock
  - Clock Control
  - 2xLO
  - MDC
  - OSC
  - PLL

- Reset
  - Reset Control
  - ARES

- Test
  - Test Mode Entry
  - Digital DFT
  - Analog DFT

- WCO
  - HSE

- Power Modes
  - Active / Sleep
  - Low Power Active / Sleep
  - Deep Sleep
  - Hibernate

---

**Hint Bar**

Review TRM chapter 35 for additional details
Introduction to Traveo II Cluster

- SAR ADC is part of the peripheral blocks

Review TRM chapter 37 for additional details

Hint Bar
SAR ADC Overview

› Overview
  - 12-bit resolution with a maximum sample rate of 1 Mspso
  - Up to three units in Traveo II

› Features (1/2)
  - Programmable sample time for each channel
  - Each logical channel can select an input from
    - Up to 32 analog input pins per unit
    - Diagnostic signals
  - Channels can be individual or grouped
    - Eight priorities, programmable per group
  - Triggered by TCPWM, software, continuous (idle trigger), or generic2
    - Multiple ADC units can be triggered by the same trigger
  - Optional debug freeze

1 1 Msps: 4.5 V ≤ VDDA ≤ 5.5 V, 0.5 Msps: 2.7 V ≤ VDDA < 4.5 V
2 Review the Triggers section for alternative trigger sources
SAR ADC Overview

› Features (2/2)
  - Programmable post-processing options for each channel
    - Averaging: first order accumulate and dump, up to 256 samples
    - Range detection: below/above threshold, inside/outside range
    - Pulse detection: programmable positive and negative event counters
  - Interrupt generation per channel or group
  - Output trigger generation per channel (can trigger DMA transfer)
  - Support for diagnostic measurements including broken wire detection
  - Programmable offset and gain calibration

Review the datasheet and section 1 in the TRM chapter for additional details
SAR ADC Block Diagram

- SAR ADC components

Reference Buffer → Diagnostic Reference → SAR ADC System

Up to 8 Internal Signals → SAR MUX → SAR ADC Core

Up to 32 Analog Inputs (GPIO) → Calibration

VrefH, VrefL

SAR Sequencer

Interruption Inputs

Trigger Input, Trigger Output

Hint Bar

Review section 2 in the TRM chapter for additional details
SAR ADC Block Diagram

- SAR ADC components
  - SAR ADC Core
  - ADC acquisition time
  - Result data format
ADC Conversion Time

A/D conversion time = sample time + comparison time

- **Comparison time:**
  - 15 ADC clock cycles
    (Maximum ADC clock frequency: 26.7 MHz\(^1\))
- **Sample time:**
  - Programmable sample time per channel (SAMPLE_TIME)
  - Recommended sample time is 11 clock cycles or more at 26.7 MHz

\[ \text{ADC Conversion Time} = \text{sample time} + \text{comparison time} \]

\[ \text{Comparison time:} \quad 15 \text{ ADC clock cycles} \]

\[ \text{(Maximum ADC clock frequency: 26.7 MHz\(^1\))} \]

\[ \text{Sample time:} \]

\[ \text{Programmable sample time per channel (SAMPLE_TIME)} \]

\[ \text{Recommended sample time is 11 clock cycles or more at 26.7 MHz} \]

**Use Case: External Impedance Differs per Channel**

```
Sensor Input A
Sensor Input B
Sensor Input C
```

```
ADC
Ch 0
Ch 1
Ch 2
```

\(^1\) Peripheral clock (CLK_PERI). Minimum comparison time: \( \frac{15}{26.7 \, \text{MHz}} = 0.56 \, \mu\text{s} \); minimum sample time: \( \frac{11}{26.7 \, \text{MHz}} = 0.41 \, \mu\text{s} \)
Result Data Format

› Signed/Unsigned result
  – Can be treated as signed or unsigned (default)

› Alignment
  – Can be right aligned (default) or left aligned

<table>
<thead>
<tr>
<th>Alignment</th>
<th>Signed/Unsigned</th>
<th>Result Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Right</td>
<td>Unsigned</td>
<td>15</td>
</tr>
<tr>
<td>Right</td>
<td>Signed</td>
<td>11</td>
</tr>
<tr>
<td>Left</td>
<td>-</td>
<td>11</td>
</tr>
</tbody>
</table>

¹ This bit is zero

Alignment use case:
• Left alignment allows fixed-point arithmetic of values with different resolution
• Compare 12-bit value with 8-bit value
• Compare 16-bit averaged value with 12-bit value without averaging

Review section 3.2 in the TRM chapter for additional details
SAR ADC Block Diagram

SAR ADC components
  - SARMUX
    - Analog input selection
    - Reference buffer
    - Preconditioning

Review section 4 in the TRM chapter for additional details
Analog Input Selection

- **Configuration**
  - Up to 32 analog pins per unit\(^1\)
  - Up to eight special analog signals
  - Supports the external analog multiplexer\(^4\)
    - Each channel configuration has its own 3-bit wide external mux select value (EXT_MUX_SEL)
    - The per channel external mux enable bit (EXT_MUX_EN) is used as a chip select for the external mux select device

---

\(^1\) CYT2B7/9 (176-pin) supports 3 units with the following analog pins: Unit 0: ADC[0]_0-23, Unit 1: ADC[1]_0-23, and Unit 2: ADC[2]_0-15

For other devices, refer to the respective device datasheet

\(^2\) External analog multiplexer pins: EXT_MUX[x]_y - External Analog Multiplexer Select Input and EXT_MUX[x]_EN: External Analog Multiplexer Enable

\(^3\) Traveo II does not support AUX (auxiliary input)

\(^4\) \(V_{MOTOR}\) is connected to the P11[2:0]/ADC[2:0]_M pins

---

**SARMUX Block Diagram**

- **Diagnostic Ref. Signal**
- **Extension to other MUX\(^2\)**
- **Internal Special Signals (Up to 8)**
  - Temperature Sensor
  - Bandgap Voltage
  - \(V_{DDA}\)
  - \(V_{CCD}\)
  - \(V_{AXYB}\)
  - \(V_{AXYBS}\)
  - \(V_{AXY}\)

**Analog Input Signals (Up to 32)**

- **ADC[x]_31**
- **ADC[x]_0**

**To ADC Core Input**

**From SAR Sequencer**

---

**External Analog Multiplexer Advantage:**

This can be used to expand the number of analog signals that can be sampled beyond the number of analog pins

---

Review section 4 in the TRM chapter and Register TRM for additional details
Analog Input Selection

› Advantage
  – Each analog input pin can connect with each channel per ADC unit

› Use Case
  – Scan in order of system control priority without physical constraints from pinout and PCB layout

Example CYT2B7 Unit 0
ADC[0]_0–23 input pins can be freely connected with logical channels 0–23, but not with channels 24 and higher

Review each device datasheet for each unit channel configuration
Reference Buffer

Four Functions

- **Power Supply Monitoring**
- Buffering the 0.9-V bandgap signal from the System Resource Sub System (SRSS)
  - Connects to SAR and diagnostic reference generator multiplexer inputs
- Scaling 1 \( \mu A \) (4x 250 nA currents in parallel) from the SRSS to 10 \( \mu A \) and replicating this current (both source and sink) for diagnostic reference generators
- Use case:
  - Broken wire detection
- Providing a temperature-dependent voltage for one-die temperature sensing

Review section 11 in the TRM chapter for additional details
Review section 9 in the TRM chapter for temperature sensor measurement
Review the device datasheet for temperature sensor spec
Voltage Monitoring by ADC

› ADC is used for all other power supplies
› A monitor switch is provided between power/ground pins and Amuxbus A/B by the HSIOM_MONITOR_CTL register
› The midpoint of the signal (Amuxbus A/B) is connected to the SARMUX (internal signals) and can be selected for ADC by a channel

Supply Monitor Block (Reference Buffer)

- PASS_CTL_SUPPLY_MON_EN_A
- PASS_CTL_SUPPLY_MON_LVL_A
- VREFL
- VREFH
- SARn_CHx_SAMPLE_CTL_PIN_ADDR
- SARMUX
- ADC Core

HSIOM_MONITOR_CTL

I/O PAD

Review section 11 in the TRM chapter for additional details

Review TRM section 16.3.6 for the relation between HSIOM_MONITOR_CTL_0 register and power/ground pins
Preconditioning

› Four possible selections per channel
  - No preconditioning
  - Discharge to VREFL
  - Charge to VREFH
  - Connect to diagnostic reference output

Advantage:
- Detect broken wire by charging or discharging the ADC sampling capacitor before sampling the input signal for functional safety and diagnostics
Use Case:
Detecting Broken Wires by Preconditioning

› “open” detection with two preconditions

- Preconditioning = VREFH

Note: When there is an open load, the conversion result will still be 0 V

- Preconditioning = VREFL

Note: When there is an open load, the conversion result will still be almost 5 V
Use Case:

Broken Wire Detection by Preconditioning

“short to GND” detection preconditions

- Preconditioning = VREFH

Note: When there is a short circuit to GND, the conversion result will immediately be 0 V

- Preconditioning = VREFL

Note: When there is a short circuit to GND, the conversion result will still be 0 V
Use Case:

Broken Wire Detection by Preconditioning

› “short to 5 V” detection preconditions

- Preconditioning = VREFH

- Preconditioning = VREFL

Note: When there is a short circuit to 5 V, the conversion result will still be 5 V

Note: When there is a short circuit to 5 V, the conversion result will immediately be 5 V
Advantage of Preconditioning

› Preconditioning = “OFF”

› Preconditioning = “DIAG” = VREFH/2

Preconditioning always adds at least two ADC cycles

Sample time can be shorter by preconditioning

Review Register TRM and sections 4.1 and 10 in the TRM chapter for additional details

Review the Diagnostic Reference Generator section for more details
SAR ADC Block Diagram

- SAR ADC components
  - Diagnostic Reference
    - Diagnostic reference generator

SAR ADC System

- Reference Buffer
- Diagnostic Reference
- Up to 8 Internal Signals
- SARMUX
- Up to 32 Analog Inputs (GPIO)
- VrefH
- VrefL
- SAR ADC Core
- Calibration
- SAR Sequencer
- Interrupts
- Trigger Input
- Trigger Output

Hint Bar

Review section 10 in the TRM chapter for additional details
Diagnostic Reference Generator

- Provides voltages and currents for diagnostics
  - VREFL, VREFH
  - VREFH x 1/8, x 2/8, x 3/8, x 4/8, x 5/8, x 6/8, x 7/8, x 199/200
  - Bandgap voltage
  - Current source (10 μA)
  - Current sink (10 μA)

Advantage:
Test internal and external signal connection by injecting voltage near pads

Review Register TRM and section 10 in the TRM chapter for additional details
SAR ADC Block Diagram

- SAR ADC components
  - Channel Grouping
  - Triggers
  - Arbitration, Preemption, and Acquisition Scheduling
  - Averaging
  - Range Detect
  - Pulse Detect
  - Interrupts
  - Trigger Outputs
  - Debug Freeze
  - Auto Power Down
  - Channel Disable/Software Abort

Review sections 5, 6, and 7 in the TRM chapter for additional details.
Channel Grouping

› All the (up to 32) channels of the SAR ADC can be grouped

› The first channel defines the trigger for a group

› The last channel defines the end for a group

› A channel in the group may be disabled, in which case it will be skipped

› The grouping can only contain sequential channels, and cannot have overlapping groups or a group within a group

Review the datasheet, Register TRM, and section 6.1 in the TRM chapter for additional details
Triggers

A trigger for a group will cause the acquisitions, as defined by the configurations of the channels in the group, to be executed.

There are seven possible hardware (HW) triggers and one software (SW) trigger:

- The hardware trigger options are:
  - TCPWM: 1-to-1 trigger output from a corresponding 16-bit TCPWM
  - GENERIC0-4: Five generic input triggers routed to this ADC
    - GPIO, ADC, event generator, 32-bit TCPWM, 16-bit TCPWM for motor
  - CONTINUOUS: This trigger is always high, making the group always triggered or in other words, Idle trigger
  - OFF: No hardware trigger

The group can be software-triggered if it is configured to use a hardware trigger.
TCPWM-Triggered ADC

- PWM signals are mainly used to control power supplied to electrical devices. In the automotive market these are mostly LEDs (or other lights) and motors.
- To check the correct function, the voltage and/or current controlled by the PWM signal is measured by the ADC.

Use Case: TCPWM-Triggered ADC

The marking area is the ADC trigger timing that confirms possible high levels in every cycle.

To avoid this glitch, do not use this edge as a trigger for ADC.

Review Register TRM and section 6.2 in the TRM chapter for additional details.
Review TCPWM and Trigger Multiplexer training sections for more information about PWMs and triggers.
Arbitration/Preemption and Acquisition Scheduling

- Arbitration of the pending triggers is based on both an explicit and an implicit priority
  - **Priority**
    - The explicit priority is set as a trigger attribute by software
    - There are eight explicit priority levels, priority level 0 being the highest
    - The implicit priority is defined by the channel ordering as follows:
      - A lower channel has a higher priority than a higher channel with the same explicit priority

**Example of Priority**

- Trigger (Priority 0)
  - Ch 15
- Trigger (Priority 1)
  - Ch 0
  - Ch 9
  - Ch 12

High Priority

Low Priority

- Review Register TRM and section 6.3 in the TRM chapter for additional details
Arbitration/Preemption and Acquisition Scheduling

- Preemption and Acquisition Scheduling
  - The scheduler determines whether preemption occurs or not, based on the explicit priority level and the trigger preemption type of the ongoing group scan
  - Available preemption types: ABORT_RESUME, ABORT_RESTART, ABORT_CANCEL, and FINISH_RESUME

Hint Bar

Review Register TRM and section 6.3 in the TRM chapter for additional details
Preemption Types:

Type 1

- **ABORT_RESUME**
  1. Immediately abort the ongoing acquisition
  2. Keep the pending trigger of the aborted group
  3. After the high-priority group is done, resume the group scan starting with the aborted channel
     - When averaging, discard the averaging results and, on return, restart averaging

![Diagram of sensor groups and triggers]
Preemption Types:

**Type 2**

- **ABORT_RESTART**
  1. Immediately abort the ongoing acquisition
  2. Keep the pending trigger of the aborted group
  3. After the high-priority group is done, restart the group scan from the first channel of the group
Preemption Types:

Type 3

- **ABORT_CANCELM**
  1. Immediately abort the ongoing acquisition and do not return
  2. Clear the pending trigger of the aborted group
  3. Set the cancelled interrupt for the last channel of the aborted group

Diagram showing the interactions between sensor groups and triggers, highlighting the preemption type and the conditions for each group.
FINISH_RESUME

1. Before preempting, complete the ongoing acquisition (including averaging)
2. Keep the pending trigger of the aborted group
3. After the high-priority group is done, resume the group scan starting with the next channel

Preemption Types:
Averaging

› Averaging functionality for every channel
› Accumulate the results (after sign extension) in 20-bit accumulator
› Up to 256 samples can be averaged

Use Case: Two-Sample Averaging (Continuous)

ADC Conversion

<table>
<thead>
<tr>
<th>ADC Conversion</th>
<th>1st Sample</th>
<th>1st Conversion</th>
<th>2nd Sample</th>
<th>2nd Conversion</th>
<th>3rd Sample</th>
<th>3rd Conversion</th>
<th>4th Sample</th>
<th>4th Conversion</th>
<th>5th Sample</th>
<th>5th Conversion</th>
</tr>
</thead>
</table>

Accumulator

<table>
<thead>
<tr>
<th>Accumulator</th>
<th>xxxxx</th>
<th>1st Result</th>
<th>1st + 2nd Result</th>
<th>3rd Result</th>
<th>3rd + 4th Result</th>
</tr>
</thead>
</table>

Result of Averaging

<table>
<thead>
<tr>
<th>Result of Averaging</th>
<th>xxxxx</th>
<th>1st + 2nd Result / 2</th>
<th>3rd + 4th Result / 2</th>
</tr>
</thead>
</table>

Review Register TRM and section 5.4 in the TRM chapter for additional details.
Range Detect can check the ADC result without CPU involvement:

- Two programmable threshold values per channel
  - RANGE_LO, RANGE_HI
- Four modes per channel:
  - BELOW_LO: RESULT < RANGE_LO
  - INSIDE_RANGE: RANGE_LO ≤ RESULT < RANGE_HI
  - ABOVE_HI: RANGE_HI ≤ RESULT
  - OUTSIDE_RANGE: (RESULT < RANGE_LO) || (RANGE_HI ≤ RESULT)

Use Case: Detecting Out of the Setting Temperature Range
Pulse Detect

- Pulse Detect filters input signal level by counting the Range Detect events
  - Positive counter: 8-bit
  - Negative counter: 5-bit

Use Case: Detecting “Sufficiently Long” High Pulses While Ignoring “Short Enough” Low Spikes

- Reload Values

*Overflow interrupt is generated if the previous Pulse Detect interrupt is still not cleared*
Interrupts

Group interrupt (group done) and channel interrupt (range detect) can occur independently
- Can generate the range detect interrupt during group conversion

<table>
<thead>
<tr>
<th>Interrupts</th>
<th>Per Channel</th>
<th>Per Group¹</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range Detect</td>
<td>✔</td>
<td></td>
<td>Interrupt by range detection</td>
</tr>
<tr>
<td>Pulse Detect</td>
<td>✔</td>
<td></td>
<td>Interrupt for pulse detection</td>
</tr>
<tr>
<td>Overflow</td>
<td>✔</td>
<td>✔</td>
<td>Interrupt is set if the new ADC completes while the results from the previous completion have not yet been handled</td>
</tr>
<tr>
<td>Group Done</td>
<td>✔</td>
<td></td>
<td>Interrupt by group scan completion</td>
</tr>
<tr>
<td>Group Cancelled</td>
<td></td>
<td>✔</td>
<td>Interrupt is set by ABORTCANCEL operation</td>
</tr>
</tbody>
</table>

¹ Can be set for the last channel of a group

Review Register TRM and sections 7.2 and 7.3 in the TRM chapter for additional details
ADC Interrupt Timing for Overflow

- **Single channel with continuous trigger**
  - **Normal Case (no overflow)**

<table>
<thead>
<tr>
<th>ADC Conversion</th>
<th>1st Sample</th>
<th>1st Conversion</th>
<th>2nd Sample</th>
<th>2nd Conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Result Register</td>
<td>Previous Result</td>
<td></td>
<td>1st Result</td>
<td>2nd Result</td>
</tr>
<tr>
<td>Done Interrupt</td>
<td>SW Read “1st Result”</td>
<td>Cleared by SW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overflow Interrupt</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Overflow Case**

<table>
<thead>
<tr>
<th>ADC Conversion</th>
<th>1st Sample</th>
<th>1st Conversion</th>
<th>2nd Sample</th>
<th>2nd Conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Result Register</td>
<td>Previous Result</td>
<td></td>
<td>1st Result</td>
<td>2nd Result</td>
</tr>
<tr>
<td>Done Interrupt</td>
<td>SW Did Not Read “1st Result”</td>
<td>Not Cleared By SW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overflow Interrupt</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2nd Conversion Is Started Immediately After 1st Conversion Is Completed
Channel Done Trigger Output

- Channel Done trigger output can be generated per enabled channel
- Indicates that the data for channel is available in the Result register
- Can be used to retrieve external sensor data over a constant period for CPU to handle (see figure below)

**Use Case: DMA Trigger**

![Diagram](image-url)
Range Violation Trigger Output

- Range Violation trigger output can be generated per enabled channel
- ADC generates a pulse if the acquisition result for the channel causes a Range Detect event
- The TCPWM output can be disabled when an abnormal voltage range is detected by the ADC if the TCPWM LED has control

Use Case: TCPWM LED Control

Hint Bar

Review Register TRM and section 7.1 in the TRM chapter for additional details
Review the TCPWM and Trigger Multiplexer training sections for more information about PWM and triggers
Debug Freeze

- Debug freeze prevents the scheduler from starting acquisitions for a new channel
- At averaging, ADC will complete even if the debug freeze trigger is asserted
- Debug freeze is available for each ADC unit
- Debug freeze allows system halting without overwriting ADC values
  - Converted values fit into debug session, avoiding corruption caused by overwritten ADC values (for example, range detect interrupt)

Use Case: System Halting

Review Register TRM (PASS_CTL.DEBUG_FREEZE_EN) and section 6.4 in the TRM chapter for additional details
Auto Idle Power Down

- Automatically powers down the analog circuit when the ADC is idle
- The analog circuit automatically powers up when a trigger inputs
- After power-up, the analog circuit must settle for some time before it can make accurate acquisitions (1 µs, minimum)

Use Case: Cyclic Sensing and Power Saving

ADC Cyclic Sensing, e.g., Temperature, Pressure Sensor, Battery Voltage

ADC Idle Power Down
ADC Idle
No Trigger

ADC Cyclic Sensing, e.g., Temperature, Pressure Sensor, Battery Voltage

ADC Idle Power Mode
ADC Idle
No Trigger

ADC Trigger, e.g., Timer Event

ADC Idle Power Down
ADC Idle
No Trigger

ADC Trigger, e.g., Timer Event

ADC Cyclic Sensing, e.g., Temperature, Pressure Sensor, Battery Voltage

ADC Idle Power Mode
ADC Idle
No Trigger

ADC Trigger, e.g., Timer Event

Review Register TRM (CTL.PWRUP_TIME) and section 6.5 in the TRM chapter for additional details
Channel Disable/Software Abort

› Can disable the ADC channel with software for the unused channel

› Can abort the ADC using software during A/D conversion

› Use cases
  - Emergency stop due to low battery or system down
  - Reconfiguration by changing the external environment (for example, temperature)

Hint Bar

Review Register TRM and section 6.6 in the TRM chapter for additional details
SAR ADC Block Diagram

SAR ADC components
- Calibration
  - Analog
  - Alternate
  - Coherent

Review section 8 in the TRM chapter for additional details.
Analog Calibration

› Brings the actual ADC transfer curve closer to the ideal transfer curve
› Adjusts an offset and a gain value using software to satisfy the following
  – Transition between values 0x000 and 0x001 for $V_{REFL} + 0.5$ LSB input voltage
  – Transition between values 0xFFE and 0xFFF for $V_{REFH} - 1.5$ LSB input voltage
› Total error can be ±5 LSB after offset and gain adjustment

---

**Analog to Digital Transfer Curve**

- **Ideal Curve**
- **Actual Curve**

- **Input Voltage**
  - $V_{REFL}$
  - $V_{REFH}$

- **Converted Value**
  - 0x000
  - 0x400
  - 0x800
  - 0xC00
  - 0x1000
  - 0xFFF

---

**Preconditions:**
Before the ADC is used for acquisitions, it must be set to the correct values (e.g., periodic calibration of the production line due to temperature shift and age)

---

**Hint Bar**
Review Register TRM and section 8.1 in the TRM chapter for additional details
Alternate Calibration/Coherent Calibration Update

› Alternate Calibration
  – Runs the recalibration algorithm in the background while the main application keeps running undisturbed using the active calibration values
  – Changing the calibration in the middle of a group scan leads to incoherent results within that group scan

› Coherent Calibration Update
  – Waits for the right moment to coherently copy values from the alternate calibration registers to the regular calibration registers
  – The right moment for a coherent calibration update is when the ADC becomes idle, or a continuous triggered group completes
Coherent Calibration Update Using Alternate Calibration

Use cases

1. Alternate calibration values are set by software
2. Coherent calibration update is enabled by software
3. ADC waits for the Idle to coherently copy values from the alternate calibration registers to the regular calibration registers by hardware
4. Coherent calibration update is disabled by hardware

Coherent Calibration Update Timing by Using Alternate Calibration

<table>
<thead>
<tr>
<th>ADC Conversion</th>
<th>1st Sample</th>
<th>1st Conversion</th>
<th>Idle</th>
<th>2nd Sample</th>
<th>2nd Conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coherent Update</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Alternate Calibration Registers</td>
<td>XX</td>
<td>①</td>
<td>YY</td>
<td>③</td>
<td>YY</td>
</tr>
<tr>
<td>Regular Calibration Registers</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td>YY</td>
</tr>
</tbody>
</table>
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Data</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6108532</td>
<td>03/28/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6378576</td>
<td>11/09/2018</td>
<td>Added pages 2, 4, 5, 15, 16, and 25, and the note descriptions for all pages</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated pages 3, 13, 14, and 37</td>
</tr>
<tr>
<td>*B</td>
<td>6610655</td>
<td>07/02/2019</td>
<td>Updated page 2, 3, 4, 10, 14, 25, 29 to 32, 38. Added page 5.</td>
</tr>
<tr>
<td>*C</td>
<td>7013756</td>
<td>10/29/2020</td>
<td>Updated page 2, 3, 15.</td>
</tr>
</tbody>
</table>

Copyright © Infineon Technologies AG 2020. All rights reserved.