Customer Training Workshop
Traveo™ II Pulse Width Modulation (PWM) Interface
Target Products

Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Cluster

The PWM is part of Peripheral Blocks

Review TRM chapter 33 for additional details
Pulse Width Modulation (PWM) Overview

› Pulse Width Modulation (PWM)
   - PWM interface drives PWM output lines and their complementary output lines
   - PWM destinations are E-bridges or H-bridges, which drive low-cost speakers
   - PWM interface processes Pulse Code Modulated (PCM) input signals into PWM output signals

› Features
   - Programmable interface clock
   - Programmable doubling mode
   - Programmable gain
   - Programmable PWM
   - Programmable PCM sample formatting (8, 10, 12, 14, 16, 18, 20, 24, and 32 bits)
   - 64-entry TX FIFO with interrupt and trigger support

Review TRM section 33.3 for additional details
PWM Block Diagram

- PWM components
  - PWM Interface
  - Clock
  - Transmitter
  - SRAM

Review TRM section 33.3.2 for additional details

SRSS clock (CLK_IF_SRSS[3:0]) is dependent on the device

CLK_GR: Clock input to peripheral functions
Clock

- PWM interface clock can be derived from either of these clock signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_IF_SRSS[3:0]</td>
<td>SRSS clock.</td>
</tr>
<tr>
<td>PWM_MCK_IN</td>
<td>Master interface clock.</td>
</tr>
</tbody>
</table>

- An interface clock CLK_IF is derived and then gated to derive the PWM clock

```
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</tr>
</thead>
<tbody>
<tr>
<td>PWM_MCK_IN</td>
<td>Master interface clock.</td>
</tr>
<tr>
<td>CLOCK_SEL</td>
<td></td>
</tr>
<tr>
<td>CLOCK_DIV</td>
<td></td>
</tr>
</tbody>
</table>
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1 Note: See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy.
PWM Output

PWM values pwm[15:0] are processed from the incoming TX FIFO PCM data in the following manner:

1. TX FIFO: Translates data into 24-bit PCM values, as specified by PWM_CTL.WORD_SIZE
2. Doubler: Doubles the PCM value frequency through either sample repetition or sample averaging, as specified by PWMx_TXy_DOUBLE_CTL
3. Gain control: Scales the PCM values by programmable multiplier value COEFF[13:0] and scale value SCALE[3:0]
PWM Output

PWM values pwm[15:0] are processed from the incoming TX FIFO PCM data

4. **PWM generation**:
   - PWM format (E-bridge or H-bridge)
   - PWM period (PERIOD[15:0])
   - Offset value (OFFSET[15:0]) (only used in E-bridge mode)

5. **Dead time insertion**

6. **PWM Output**
PWM Format

- **E-bridge format**
  - Used to drive the LINE1_P/N PWM output lines

![Diagram of E-bridge format]

- **PCM to PWM Modulation at a Coarser Grain (E-bridge Format)**

![Diagram of PCM to PWM modulation]
PWM Format

› H-bridge format
  - Used to drive the LINE1_P/N and LINE2_P/N PWM output lines

PCM to PWM Modulation at a Coarser Grain (H-bridge Format)
Dead Time

- Dead Time Insertion
  - Dead time insertion is deployed before polarity inversion of the PWM output lines
  - Dead time insertion effectively “delays” the rising edges of all PWM output signals, but does not affect the falling edges of the signals

- Polarity Control of PWM Output Lines
  - After dead time insertion, the polarity of all four PWM output lines can be inverted
Interrupt

- PWM interrupt can be triggered under any of the following events

<table>
<thead>
<tr>
<th>TX Interrupt</th>
<th>Set condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_TRIGGER</td>
<td>TX trigger is generated.</td>
</tr>
<tr>
<td>FIFO_OVERFLOW</td>
<td>Writing to a full TX FIFO (TX_FIFO_STATUS.USED is &quot;64&quot;). This is referred to as an underflow event.</td>
</tr>
<tr>
<td>FIFO_UNDERFLOW</td>
<td>Reading from an empty TX FIFO (TX_FIFO_STATUS.USED is &quot;0&quot;).</td>
</tr>
<tr>
<td>IF_UNDERFLOW¹</td>
<td>PCM samples are generated too fast by the interface logic. May indicate that the IP system frequency is too low with respect to the interface frequency (a SW configuration error).</td>
</tr>
</tbody>
</table>

¹ This functionality is for debug purposes

Hint Bar

Review TRM section 33.3.6 and Register TRM for additional details
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## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6676158</td>
<td>09/17/2019</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6805471</td>
<td>02/12/2020</td>
<td>Added note descriptions in each slide</td>
</tr>
<tr>
<td>*B</td>
<td>7031887</td>
<td>11/26/2020</td>
<td>Updated pages 2, 5, and 6</td>
</tr>
<tr>
<td>*C</td>
<td>7065462</td>
<td>01/12/2021</td>
<td>Updated page 2</td>
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