## Target Products

### Target product list for this training material

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>


Introduction to Traveo II Body Controller Entry

› The program and debug interface is part of the CPU subsystem

Hint Bar
Review TRM chapter 32 for additional details
Introduction to Traveo II Body Controller High

The program and debug interface is part of the CPU subsystem.
The program and debug interface is part of the CPU subsystem.
The program and debug interface is a communication gateway for an external device to perform programming and debugging.

The external device includes a:
- Cypress-supplied programmer
- Third-party programmer and debugger

Communication protocol between the external device and Traveo II microcontroller is supplied by:
- Serial wire debug (SWD)
- Joint Test Action Group (JTAG)
Multi-Core Debug for CYT2B6/B7/B9/BL

› Arm® Cortex®-M0+ Core debug components
  – Cross-triggering interface (CTI), four hardware breakpoints, and two watchpoints
› Arm Cortex-M4 Core debug components
  – CTI, six hardware breakpoints, and four watchpoints
› Enables multi-core debug
  – Three CTIs connected via cross-triggering matrix (CTM)
  – Start or stop CM0+/CM4 at the same time
  – Start or stop instruction tracing based on whether or not the trace buffer is full, or on the break
› Debug and access port (DAP) security
  – Three access ports (APs) each can be independently disabled
  – eFuse (permanent)
  – System AP is protected by MPU
Multi-Core Debug for CYT2B6/B7/B9/BL

Program and Debug Interface for Debug

DAP

CM0 Access Port

DAP BUS

CM0 Access Port

System Access Port

Port Pins

Arm Cortex®-M0+ subsystem

Cortex®-M0+

SLV

Cortex®-M0+

ATB

Micro Trace Buffer (MTB)

CM0+ AHB decoder

CM0 external ROM table

Cortex®-M4 subsystem

Arm Cortex®-M4 subsystem

CM4 AP

Cortex®-M4

EPB

CM4 AP

Embedded Trace Macro (ETM)

CM4 APB decoder

CM4 ROM table

CM4 APB decoder

CM4 ROM table

System ROM table

Trace Port Interface Unit (TPIU)

Embedded Trace Buffer (ETB)

Embedded Trace Buffer (ETB)

Cross Trigger Interface (CTI)

Cross Trigger Matrix (CTM)

Debug APB decoder

Debug ROM table

Review TRM chapter 31 and CoreSight documentation for additional details
Multi-Core Debug for CYT3BB/4BB/3DL/4DN

› Arm® Cortex®-M0+ Core debug components
  – Cross-triggering interface (CTI), four hardware breakpoints, and two watchpoints

› Arm Cortex-M7 Core debug components
  – CTI, six hardware breakpoints, and four watchpoints

› Enables multi-core debug
  – Three CTIs connected via cross-triggering matrix (CTM)
  – Start or stop CM0+/CM7 at the same time
  – Start or stop instruction tracing based on whether or not the trace buffer is full, or on the break

› Debug and access port (DAP) security
  – Four access ports (APs) each can be independently disabled
  – eFuse (permanent)
  – System AP is protected by MPU
Multi-Core Debug for CYT3BB/4BB/3DL/4DN

Program and Debug Interface for Debug

Arm® Cortex®-M0+ subsystem
- CM0+ AHB decoder
- Cross Trigger Interface (CTI)
- CM0 external ROM table
- Micro Trace Buffer (MTB)

Arm Cortex®-M7 subsystem
- CM7 APB decoder
- Cross Trigger Interface (CTI)
- CM7 ROM table
- Embedded Trace Macro (ETM)

DAP BUS
- SWD/JTAG
- Port Pins
- CM0 Access Port
- CM7_0 Access Port
- CM7_1 Access Port
- System Access Port

DAP
- CM0 Access Port
- CM7_0 Access Port
- CM7_1 Access Port
- System Access Port

Arm® Cortex®-M0+ subsystem
- Cortex®-M0+
- BLV
- ATB

Arm Cortex®-M7 subsystem
- Cortex®-M7
- DBG
- ITM
- EPB

DAP BUS
- SWD/JTAG
- Port Pins
- CM0 Access Port
- CM7_0 Access Port
- CM7_1 Access Port
- System Access Port

DAP
- CM0 Access Port
- CM7_0 Access Port
- CM7_1 Access Port
- System Access Port

Arm® Cortex®-M0+ subsystem
- Cortex®-M0+
- BLV
- ATB

Arm Cortex®-M7 subsystem
- Cortex®-M7
- DBG
- ITM
- EPB

DAP BUS
- SWD/JTAG
- Port Pins
- CM0 Access Port
- CM7_0 Access Port
- CM7_1 Access Port
- System Access Port

DAP
- CM0 Access Port
- CM7_0 Access Port
- CM7_1 Access Port
- System Access Port

Hint Bar
Review TRM chapter 36 and CoreSight documentation for additional details.
Tracing for CYT2B6/B7/B9/BL

› Arm® Cortex®-M0+
  - Micro trace buffer (MTB) for tracing and storing instructions

› Arm Cortex-M4
  - Serial wire viewer (SWV) for output trace information with single pin at SWO
  - Embedded trace macrocell (ETM) for tracing instructions
  - Embedded trace buffer (ETB) for tracing instructions and storing them in a local SRAM
  - Instrumentation trace macrocell (ITM) for tracing output
  - Trace port interface unit (TPIU) for tracing information from the chip to an external trace port analyzer
    - Parallel (4 pins, multiplexed with GPIO and clock pin)
    - SWO (multiplexed on JTAG TDO)

Hint Bar
Review TRM chapter 31 and CoreSight Documentations for additional details
Tracing for CYT2B6/B7/B9/BL

Program and Debug Interface for Tracing

Arm® Cortex®-M0+ subsystem
- CM0+ AHB decoder
- Cross Trigger Interface (CTI)
- CM0 external ROM table
- Micro Trace Buffer (MTB)

Arm Cortex®-M4 subsystem
- CM4 APB decoder
- Cross Trigger Interface (CTI)
- CM4 ROM table
- Embedded Trace Macro (ETM)

System Access Port
- System ROM table
- Cross Trigger Matrix (CTM)
- Trace Port Interface Unit (TPIU)
- Embedded Trace Buffer (ETB)
- Debug APB decoder
- Debug ROM table

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Hint Bar

Review TRM chapter 31 and CoreSight Documentations for additional details
Tracing for CYT3BB/4BB/3DL/4DN

› Arm® Cortex®-M0+
   - Micro trace buffer (MTB) for tracing and storing instructions

› Arm Cortex-M7
   - Embedded trace macrocell (ETM) for tracing instructions
   - Embedded trace buffer (ETB) for tracing instructions and storing them in a local SRAM
   - Instrumentation trace macrocell (ITM) for tracing output
   - Trace port interface unit (TPIU) for tracing information from the chip to an external trace port analyzer
     - Parallel (4 pins, multiplexed with GPIO and clock pin)

Hint Bar
Review TRM chapter 36 and CoreSight Documentations for additional details
Tracing for CYT3BB/4BB/3DL/4DN

Program and Debug Interface for Tracing

- Arm® Cortex®-M0+ subsystem
  - CM0 Access Port
  - Cortex®-M0+
  - CM0 AHB decoder
  - Cross Trigger Interface (CTI)
  - CM0 external ROM table
  - Micro Trace Buffer (MTB)

- Arm Cortex®-M7 subsystem
  - CM7 Access Port
  - Cortex®-M7
  - CM7 AHB decoder
  - Cross Trigger Interface (CTI)
  - CM7 ROM table
  - Embedded Trace Macro (ETM)

- System Access Port
  - System ROM table
  - Cross Trigger Matrix (CTM)
  - Cross Trigger Interface (CTI)

- Port Pins
  - Trace Port Interface Unit (TPIU)
  - Embedded Trace Buffer (ETB)
  - Debug APB decoder
  - Embedded Trace Buffer (ETB)
  - Debug ROM table

Hint Bar

Review TRM chapter 36 and CoreSight Documentations for additional details
Serial Wire Debug (SWD) and JTAG Interface

- The SWD protocol is a packet-based serial transaction protocol
- JTAG controller and interface are compliant to IEEE-1149.1-2001
  - The test access port (TAP) interface is used to control the values in the boundary scan cells
  - Boundary scan test supported

Debug interface pin configuration on Boot ROM

After reset, the debug pins remain in high-impedance mode until Boot ROM initializes them as follows:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Input Enable</th>
<th>Drive Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>swj_trstn</td>
<td>Yes</td>
<td>Internal Pull-up</td>
</tr>
<tr>
<td>swj_swo_tdo</td>
<td>No</td>
<td>Strong (output)</td>
</tr>
<tr>
<td>swj_swdoe_tdi</td>
<td>Yes</td>
<td>Internal Pull-up</td>
</tr>
<tr>
<td>swj_swdio_tms</td>
<td>Yes</td>
<td>Internal Pull-up</td>
</tr>
<tr>
<td>swj_swclk_tclk</td>
<td>Yes</td>
<td>Internal Pull-down</td>
</tr>
</tbody>
</table>

*1: Only needed if SWD connector should also provide JTAG lines

1 Serial wire data I/O
2 Serial wire clock
3 Serial wire output
4 Test reset
5 Test data in
6 Test mode select
7 Test clock
8 Return test clock
9 Test data out

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Programmer and IDEs for Traveo II

› Flash Programmer

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Flash Programmer</th>
<th>Software</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Infineon</td>
<td>MiniProg3</td>
<td>Cypress Programmer 1.0</td>
<td>Only for CYT2B7</td>
</tr>
<tr>
<td></td>
<td>MiniProg4</td>
<td>Auto Flash Utility</td>
<td></td>
</tr>
<tr>
<td>DTS Insight</td>
<td>NET IMPRESS AF430/AFX100</td>
<td>AZ490 Remote Controller</td>
<td></td>
</tr>
<tr>
<td>Segger</td>
<td>J-Link</td>
<td>J-Flash</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Flasher Arm (for mass production)</td>
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<td></td>
</tr>
</tbody>
</table>

› Integrated Design Environment (IDE)

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Debugger</th>
<th>Compiler</th>
</tr>
</thead>
<tbody>
<tr>
<td>GHS</td>
<td>GHS Probe (5.6.4/5.6.6)</td>
<td>MULTI V7 (ver2017.1.4)</td>
</tr>
<tr>
<td>IAR</td>
<td>I -JET</td>
<td>Embedded Workbench for Arm (8.42.1)</td>
</tr>
<tr>
<td>iSystem</td>
<td>i-TAG Family</td>
<td></td>
</tr>
<tr>
<td>Lauterbach</td>
<td>TRACE 32</td>
<td></td>
</tr>
</tbody>
</table>
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Data</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6086858</td>
<td>04/17/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6400751</td>
<td>12/4/2018</td>
<td>Added the note descriptions. Updated the Block Diagram. Updated SWD and JTAG I/F figures. Added CYT4BF information</td>
</tr>
<tr>
<td>*C</td>
<td>7052549</td>
<td>12/22/2020</td>
<td>Updated pages 2, 13, 16. Merged page 3 for Traveo II Body Controller Entry</td>
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