Customer training workshop
TRAVEO™ T2G power supply and monitoring
Target products

Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160 KB</td>
</tr>
</tbody>
</table>
Introduction to TRAVEO™ T2G Body Controller Entry

Power supply and monitoring functions in System Resources

- Power-on reset (POR)
- Brownout detection (BOD)
- Overvoltage detection (OVD)
- Low-voltage detection (LVD)
- Low dropout regulator (LDO)

Review TRM chapter 16 for additional details

Hint Bar

- Power Modes: Active/Deep
- I/O Subsystem: High-speed I/O Matrix, Smart I/O, Boundary Scan
- Peripheral Interconnect (PPU): M-DMA0 4 Channel, P-DMA1 44 Channel, P-DMA0 92 Channel
- System Interconnect (Multi Layer AHB, IPC, MPU/SMPU): 8x CANFD, LIN/UART, LIN/UART, SWJ/ETM/ITM/CTI
- CPU Subsystem: Arm Cortex M4 160 MHz, SRAM0 256 KB, SRAM1 256 KB, CRYPTO AES, SHA, CRC, TRNG, RSA, ECC
- System Resources: Power, Reset, Sleep Control, Clock, Test, IOSS GPIO, PCLK, 7x SCB, I2C, SPI, UART, CPU Subsystem, System Interconnect, Peripheral Interconnect, I/O Subsystem

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Power supply overview

- **2.7 V–5.5 V power supply range**
- **Two on-chip regulators for Active and DeepSleep modes**

### Digital power supply
Generates internal logic voltage for Active/Sleep mode

### Analog power supply
Generates internal logic voltage for DeepSleep mode

### I/O power supply
Pin to connect external smooth capacitor only

### Hint Bar
Review TRM section 16.2 for additional details

- **VDDD/VSSD:** Digital power supply/ground
- **VDDIO/VSSIO:** I/O power supply/ground
- **VDDA/VSSA:** Analog power supply/ground
- **VCCD/VSSD:** Internal core supply/ground
Power supply sources

› All power supplies are in the 2.7-V to 5.5-V voltage range
› VDDIO_1\(^1\) must be greater than or equal to VDDD (except CYT2BL)
› VDDA and VDDIO_2 must be the same

\(^1\) VDDIO_1 is replaced with VDD in the LQFP-64 package.
Voltage monitoring overview

- Multiple voltage monitoring and supply failure protection features

Legend:
- Regulators
- 2.7 V to 5.5 V power line
- 1.1 V power line
- Control lines
- External power pad

Review datasheet and TRM section 16.3 for additional details.
Voltage monitoring overview

› Power-on reset (POR)
Power-on reset

- Initializes the device at power-up
- Always on
  - POR on VDDD
    - Provides a reset pulse during the initial power ramp

Hint Bar

Review datasheet and TRM section 16.3.1 for additional details
Brown-out detection (BOD)

The TRAVEO™ T2G Body Entry family has three units of BOD.

Review datasheet and TRM section 16.3 for additional details.
Brown-out detection (BOD) features

› Detects supply conditions below a threshold and applies a reset to the device
› Always on except in Hibernate and XRES modes
  - BOD on VDDD
    - Generates a reset if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V\(^1\) (default) or < 3.0 V
  - BOD on VDDA
    - Generates a reset, a fault, or no action\(^2\) (default) if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V\(^1\) (default) or < 3.0 V
  - BOD on VCCD
    - Generates a reset if a voltage excursion dips below the falling trip point

\(^1\) If VDDD/VDDA falls below 2.7 V (minimum VDDD/VDDA), the device will operate out of specification. To prevent this, use the 3.0-V trip point.
\(^2\) Even if VDDA is low, the MCU can boot because it does not generate a reset as default.

Review datasheet and TRM section 16.3.2 for additional details
Low-voltage detection (LVD)

The TRAVEO™ T2G Body Entry family has two units of LVD
Low-voltage detection (LVD) features

- Detects the warning voltage level to take preventive measures in the system
- Can be enabled or disabled (default) by software, except in Hibernate and XRES modes
  - LVD on VDDD
    - Generates an interrupt or a fault if a voltage level meets the trip point
    - An interrupt or a fault and trip point are configurable by software
    - Supports up to 26 trip points to monitor between 2.8 V and 5.3 V (0.1-V step)
    - Detection can be configured as falling (low voltage), rising (high voltage), or both
  - Use case for two LVD units
    - LVD1: Uses the falling trip point (3.5 V) to detect the low-voltage warning
    - LVD2: Uses the rising trip (5.3 V) to detect the overvoltage warning

Review datasheet and TRM section 16.3.4 for additional details
POR, BOD, and LVD use cases (1/2)

- **Purpose:** Determine if RAM contents have been retained by using voltage monitoring
- **MCU operating conditions**
  - LVD trip point can be in MCU operation range = RAM retention
    - LVD falling trip point (3.5 V): Warning LVD for safe system operation
    - LVD rising trip point (4.0 V): User program restart trigger
  - BOD reset (< 3.0 V) is an asynchronous reset = No RAM retention

- **Case:** When RAM contents are retained, there is no BOD reset generation

The system can operate normally and use retention RAM data because a BOD reset is not generated.
POR, BOD, and LVD use cases (2/2)

› Purpose: Judge if RAM contents have been retained by using voltage monitoring
› Setting and conditions:
  – MCU operating conditions:
    – LVD trip point can be in MCU operation range = RAM retention
      – LVD falling trip point (3.5 V): Warning LVD for safety system operation
      – LVD rising trip point (4.0 V): User program restart trigger
    – BOD reset (< 3.0 V) is an asynchronous reset = No RAM retention
› Case: For RAM, contents have not been retained (BOD reset generation)
POR, BOD, and LVD advantages

- Reduced BOM costs for low-cost applications using internal POR, BOD, and LVD

1 Review TRM and datasheet to confirm if the POR, BOD, and LVD specifications meet the safety requirements of the system.
Overvoltage detection (OVD)

The TRAVEO™ T2G Body Entry family has three units of OVD.

Legend:
- Regulators
- 2.7 V to 5.5 V power line
- 1.1 V power line
- Control line
- External power pad

Review datasheet and TRM section 16.3 for additional details.
Overvoltage detection (OVD) features

- Detects supply conditions above a threshold and applies a reset to the device
- Always ON except in Hibernate and XRES modes
  - OVD on VDDD
    - Generates a reset if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VDDA
    - Generates a reset, a fault or no action (default) if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VCCD
    - Generates a reset if a voltage excursion dips above the rising trip point

Hint Bar

Review datasheet and TRM section 16.3.3 for additional details
Overcurrent detection (OCD)

The TRAVEO™ T2G Body Entry family has one OCD for each regulator.

Review datasheet and TRM section 16.3 for additional details.
Overcurrent detection (OCD) features

› Detects the device if the current is over the regulator limit
› Always ON except in Hibernate and XRES modes
   - OCD on VCCD
     - Generates a reset by detecting if the load current of a regulator is higher than expected

Review datasheet and TRM section 16.3.5 for additional details
# Summary of voltage monitoring

<table>
<thead>
<tr>
<th>Monitored Supply</th>
<th>Monitor</th>
<th>Trip Point</th>
<th>Output</th>
<th>Available Power Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{DDD}}$</td>
<td>POR</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td>All power modes</td>
</tr>
<tr>
<td></td>
<td>BOD</td>
<td>2 (Programmable)</td>
<td>Reset</td>
<td>All power modes except Hibernate and XRES modes</td>
</tr>
<tr>
<td></td>
<td>OVD</td>
<td>2 (Programmable)</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LVD</td>
<td>26 (Programmable)</td>
<td>Interrupt, Fault, or No action</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{DDA}}$</td>
<td>BOD</td>
<td>2 (Programmable)</td>
<td>Reset, Fault, or No action</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OVD</td>
<td>2 (Programmable)</td>
<td>Reset, Fault, or No action</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{CCD}}$</td>
<td>BOD</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OVD</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OCD</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td></td>
</tr>
</tbody>
</table>
Voltage monitoring by ADC

- All power supplies use ADC
- HSIOM_MONITOR_CTL register provides a monitor switch between power/ground pad and Amuxbus A/B
- The midpoint of the signal (Amuxbus A/B) is connected to SARMUX (internal signals) and can be selected for ADC by a channel
- Use Case:
  - VDDIO monitoring

Review datasheet and Review TRM sections 16.3.6 and 31.10 for additional details
Power supply monitoring by ADC

- Relationship between HSIOM_MONITOR_CTL_0 Register and Power/Ground pins

<table>
<thead>
<tr>
<th>HSIOM_MONITOR_CTL_0</th>
<th>Power/Ground Pins</th>
<th>AMUXBUS</th>
<th>CYT2B Package Pin Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>LQFP-176</td>
</tr>
<tr>
<td>Bit 0</td>
<td>( V_{DDD} )</td>
<td>A</td>
<td>176</td>
</tr>
<tr>
<td>Bit 1</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>1</td>
</tr>
<tr>
<td>Bit 2</td>
<td>( V_{DDD} )</td>
<td>A</td>
<td>22</td>
</tr>
<tr>
<td>Bit 3</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>23</td>
</tr>
<tr>
<td>Bit 4</td>
<td>( V_{DDD} )</td>
<td>A</td>
<td>43</td>
</tr>
<tr>
<td>Bit 5</td>
<td>( V_{DDIO_1} )</td>
<td>A</td>
<td>44</td>
</tr>
<tr>
<td>Bit 6</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>45</td>
</tr>
<tr>
<td>Bit 7</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>46</td>
</tr>
<tr>
<td>Bit 8</td>
<td>( V_{REFL} )</td>
<td>B</td>
<td>76</td>
</tr>
<tr>
<td>Bit 9</td>
<td>( V_{SSA} )</td>
<td>B</td>
<td>77</td>
</tr>
<tr>
<td>Bit 10</td>
<td>( V_{DDA} )</td>
<td>A</td>
<td>78</td>
</tr>
<tr>
<td>Bit 11</td>
<td>( V_{REFH} )</td>
<td>A</td>
<td>79</td>
</tr>
<tr>
<td>Bit 12</td>
<td>( V_{DDIO_2} )</td>
<td>A</td>
<td>88</td>
</tr>
<tr>
<td>Bit 13</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>89</td>
</tr>
<tr>
<td>Bit 14</td>
<td>( V_{DDD} )</td>
<td>A</td>
<td>110</td>
</tr>
<tr>
<td>Bit 15</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>111</td>
</tr>
<tr>
<td>Bit 16</td>
<td>( V_{DDD} )</td>
<td>A</td>
<td>132</td>
</tr>
<tr>
<td>Bit 17</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>133</td>
</tr>
<tr>
<td>Bit 18</td>
<td>( V_{DDD} )</td>
<td>A</td>
<td>153</td>
</tr>
<tr>
<td>Bit 19</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>154</td>
</tr>
<tr>
<td>Bit 20</td>
<td>( V_{SSD} )</td>
<td>B</td>
<td>155</td>
</tr>
</tbody>
</table>

Review datasheet and Review TRM sections 16.3.6 and 31.10 for additional details.
Appendix
## Comparison between CYT2B, CYT3B/4B, and CYT3D/4D

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2B</th>
<th>CYT3B/4B</th>
<th>CYT3D/4D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Supply and Monitoring</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply</td>
<td>$V_{DDD} = 2.7$ V to $5.5$ V</td>
<td>$V_{DDD} = 2.7$ V to $5.5$ V (up to $300$ mA)</td>
<td>$V_{DDD} = 2.7$ V to $5.5$ V and $V_{CCD} = 1.15$ V (exceeds $300$ mA)</td>
</tr>
<tr>
<td>$5.0$ V I/O power supply</td>
<td>$V_{DDIO_{1}}, V_{DDIO_{2}}$</td>
<td>$V_{DDIO_{3}}, V_{DDIO_{4}}$</td>
<td>$V_{DDIO_{GPIO}}, V_{DDIO_{SMC}}$</td>
</tr>
<tr>
<td>$3.3$ V I/O power supply</td>
<td>N/A</td>
<td>$V_{DDIO_{3}}, V_{DDIO_{4}}$</td>
<td>$V_{DDIO_{HSIO}}, V_{DDIO_{SMIF, HV}}$</td>
</tr>
<tr>
<td>$1.8$ V I/O power supply</td>
<td>N/A</td>
<td>$V_{DDIO_{3}}, V_{DDIO_{4}}$</td>
<td>$V_{DDIO_{SMIF}}$</td>
</tr>
<tr>
<td>Analog power supply</td>
<td>$V_{DDA}$</td>
<td>$V_{DDA_{ADC}}, V_{DDA_{DAC}}, V_{DDA_{MII}}, V_{DDA_{FPD}}$</td>
<td>$V_{DDA_{ADC}}, V_{DDA_{DAC}}, V_{DDA_{MII}}, V_{DDA_{FPD}}$</td>
</tr>
<tr>
<td>Active/DeepSleep regulator</td>
<td>Same</td>
<td></td>
<td></td>
</tr>
<tr>
<td>External transistor control</td>
<td>N/A</td>
<td>Available</td>
<td>N/A</td>
</tr>
<tr>
<td>External PMIC control</td>
<td>N/A</td>
<td></td>
<td>Available</td>
</tr>
<tr>
<td>POR/BOD/OVD/LVD</td>
<td></td>
<td></td>
<td>Same</td>
</tr>
</tbody>
</table>
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## Revision history

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission date</th>
<th>Description of change</th>
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<tbody>
<tr>
<td>**</td>
<td>6155466</td>
<td>04/29/2018</td>
<td>Initial release</td>
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<tr>
<td>*A</td>
<td>6333686</td>
<td>10/11/2018</td>
<td>Added page 2, 4, 22, 23, Appendix and the note descriptions of all pages. Updated page 3, 5 to 8, 10 to 15, 17 to 21.</td>
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<td>*B</td>
<td>6595227</td>
<td>06/14/2019</td>
<td>Updated page 1 to 24.</td>
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<tr>
<td>*C</td>
<td>6825047</td>
<td>03/05/2020</td>
<td>Updated page 5.</td>
</tr>
<tr>
<td>*E</td>
<td>7397171</td>
<td>10/22/2021</td>
<td>Updated page 1 to 7, 9, 11, 15, 16, 18, 24.</td>
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