Customer Training Workshop

Traveo™ II Power Supply and Monitoring

Q4 2020

Target Products

› Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576 KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160 KB

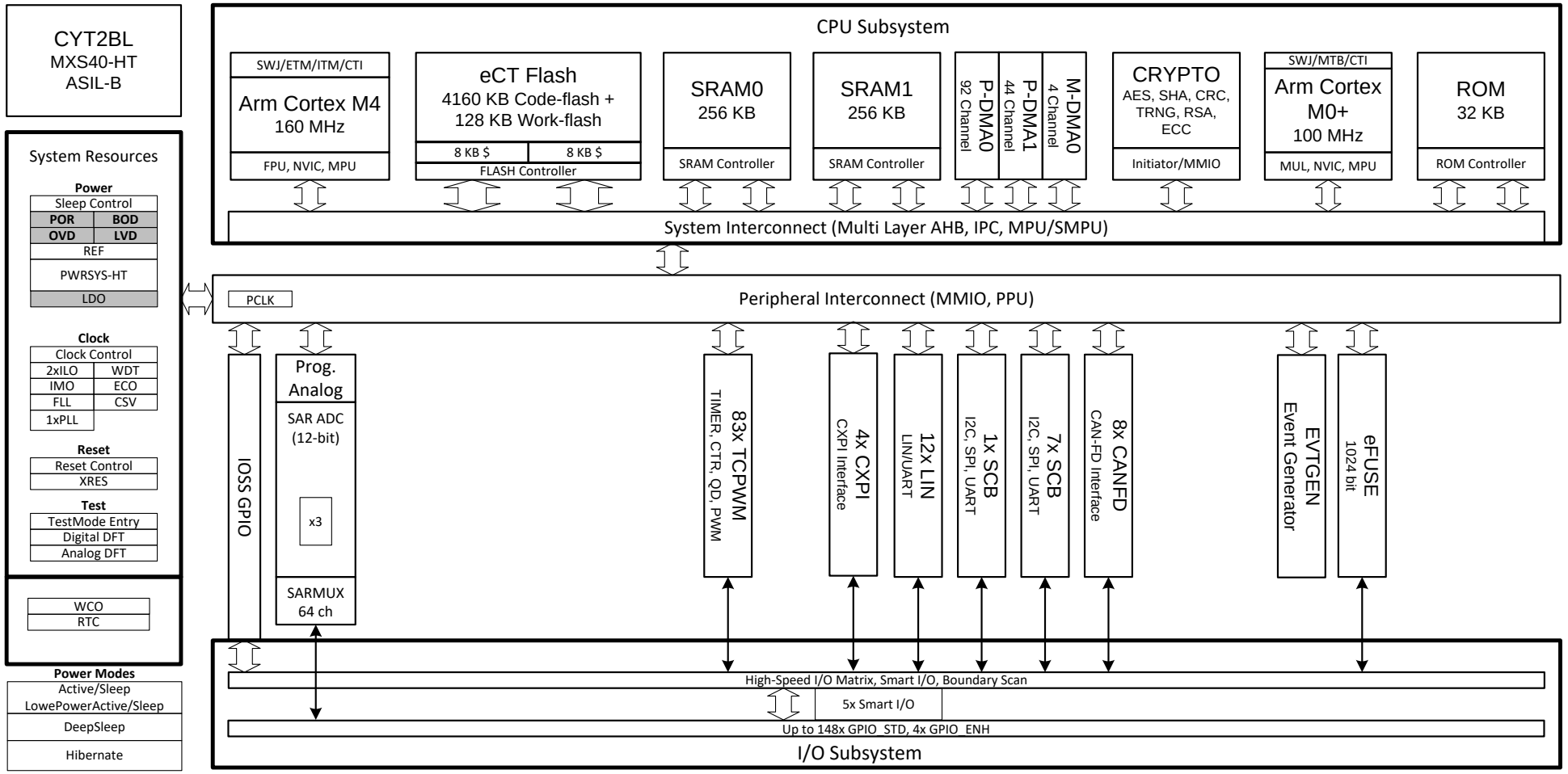
Hint Bar

Training section reference

Power Supply and Monitoring for Traveo II Body High

Introduction to Traveo II Body Controller Entry

› Power supply and monitoring functions in System Resources



Hint Bar

Review TRM chapter 16 for additional details

Power-on reset (POR)

Brownout detection (BOD)

Overvoltage detection (OVD)

Low-voltage detection (LVD)

Low dropout regulator (LDO)

Power Supply Overview

- **2.7 V–5.5 V power supply range**
- **Two on-chip regulators for Active and DeepSleep modes**

Digital power supply

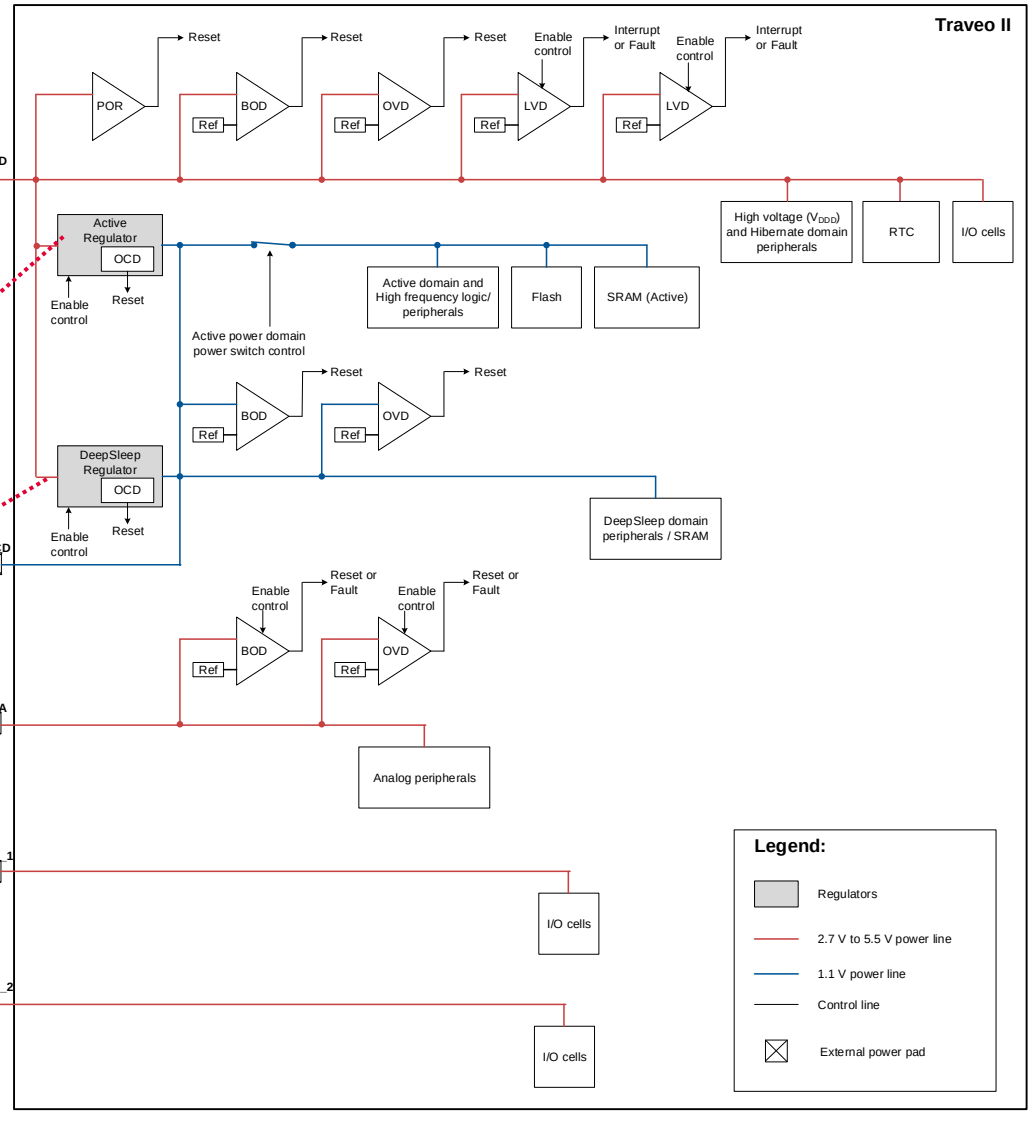
Generates internal logic voltage for Active/Sleep mode

Generates internal logic voltage for DeepSleep mode

Pin to connect external smooth capacitor only

Analog power supply

I/O power supply



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Review TRM section 16.2 for additional details

VDDD/VSSD:
Digital power supply/ ground

VDDIO/VSSIO:
I/O power supply/ ground

VDDA/VSSA:
Analog power supply/ ground

VCCD/VSSD:
Internal core supply/ ground

Power Supply Sources

- All power supplies are in the 2.7-V to 5.5-V voltage range
- VDDIO_1[1] must be greater than or equal to VDDD (except CYT2BL)
- VDDA and VDDIO_2 must be the same

Hint Bar

Review the datasheet

- Recommended Operating Conditions

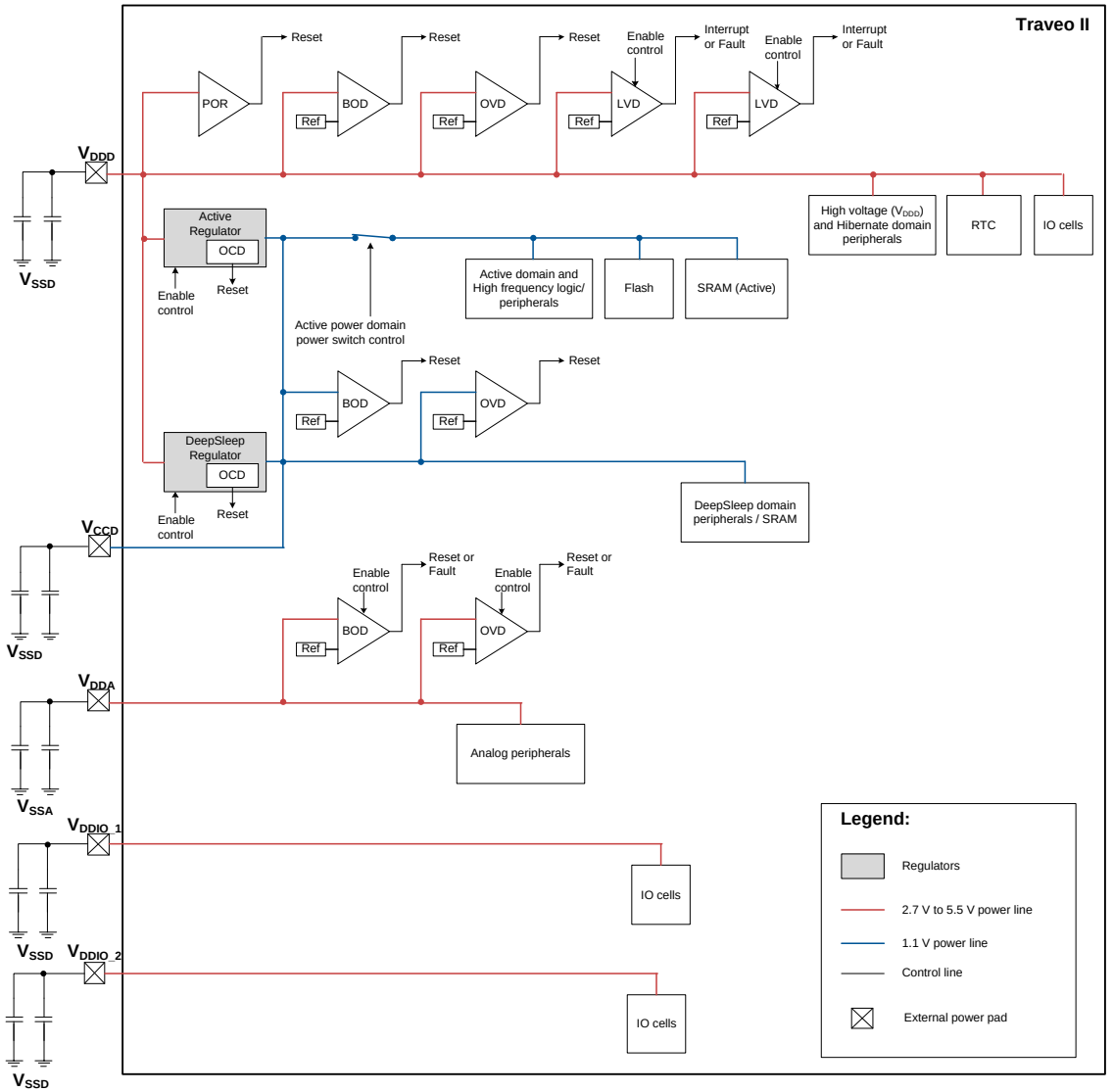
- 12-Bit SAR ADC DC Specifications when using ADC units

Review TRM sections 16.2.3 and 16.2.4 for additional details

[1] V_{DDIO_1} is replaced with V_{DDD} in the LQFP-64 package.

Voltage Monitoring Overview

- Multiple voltage monitoring and supply failure protection features

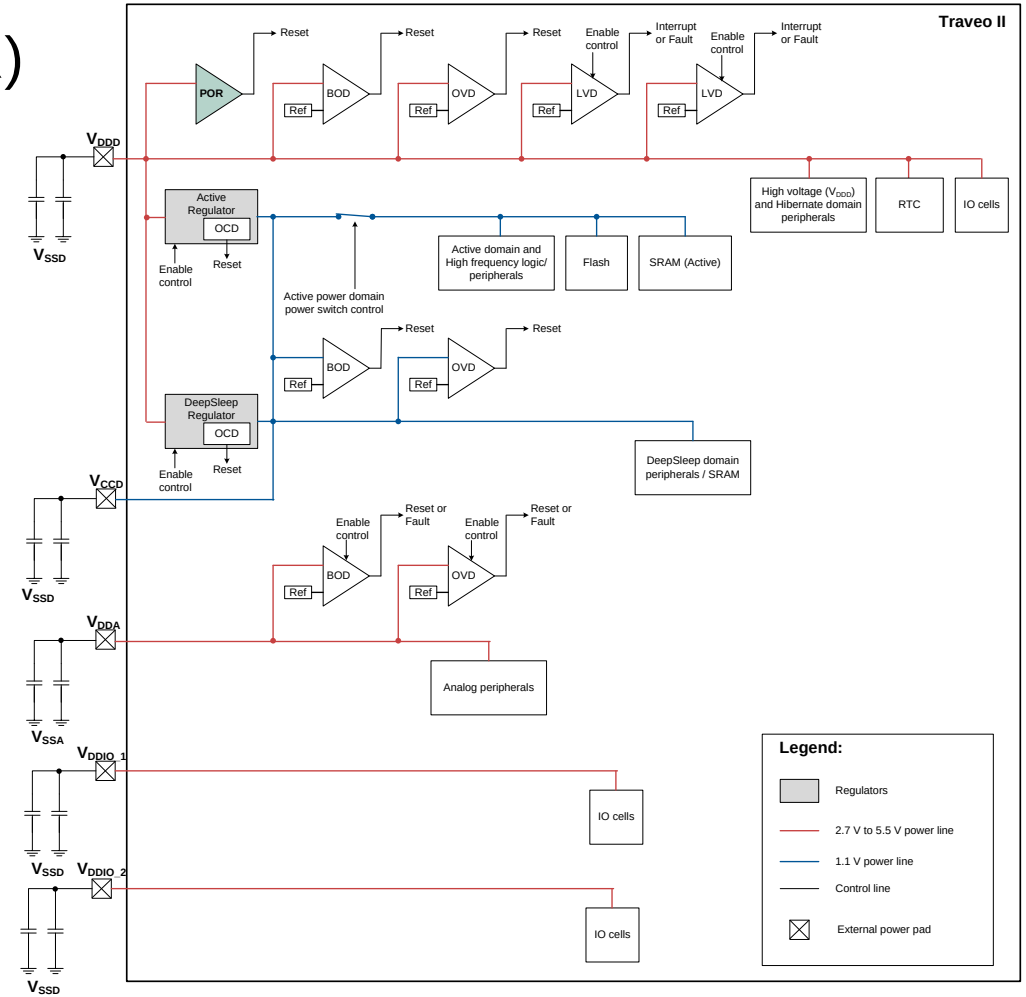


Hint Bar

Review datasheet and TRM section 16.3 for additional details

Voltage Monitoring Overview

- Power-on reset (POR)



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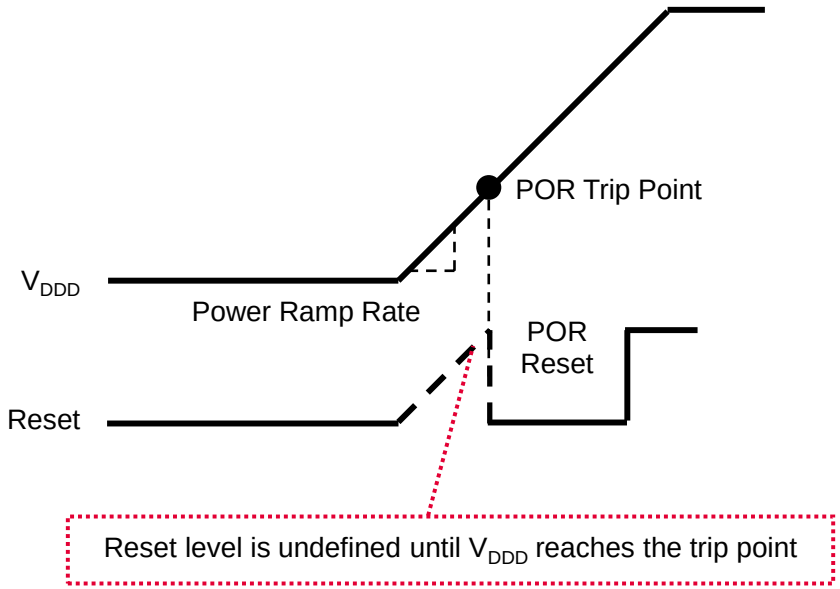
Review datasheet and TRM section 16.3 for additional details

Power-on Reset

- Initializes the device at power-up
- Always on
  - POR on VDDD
    - Provides a reset pulse during the initial power ramp



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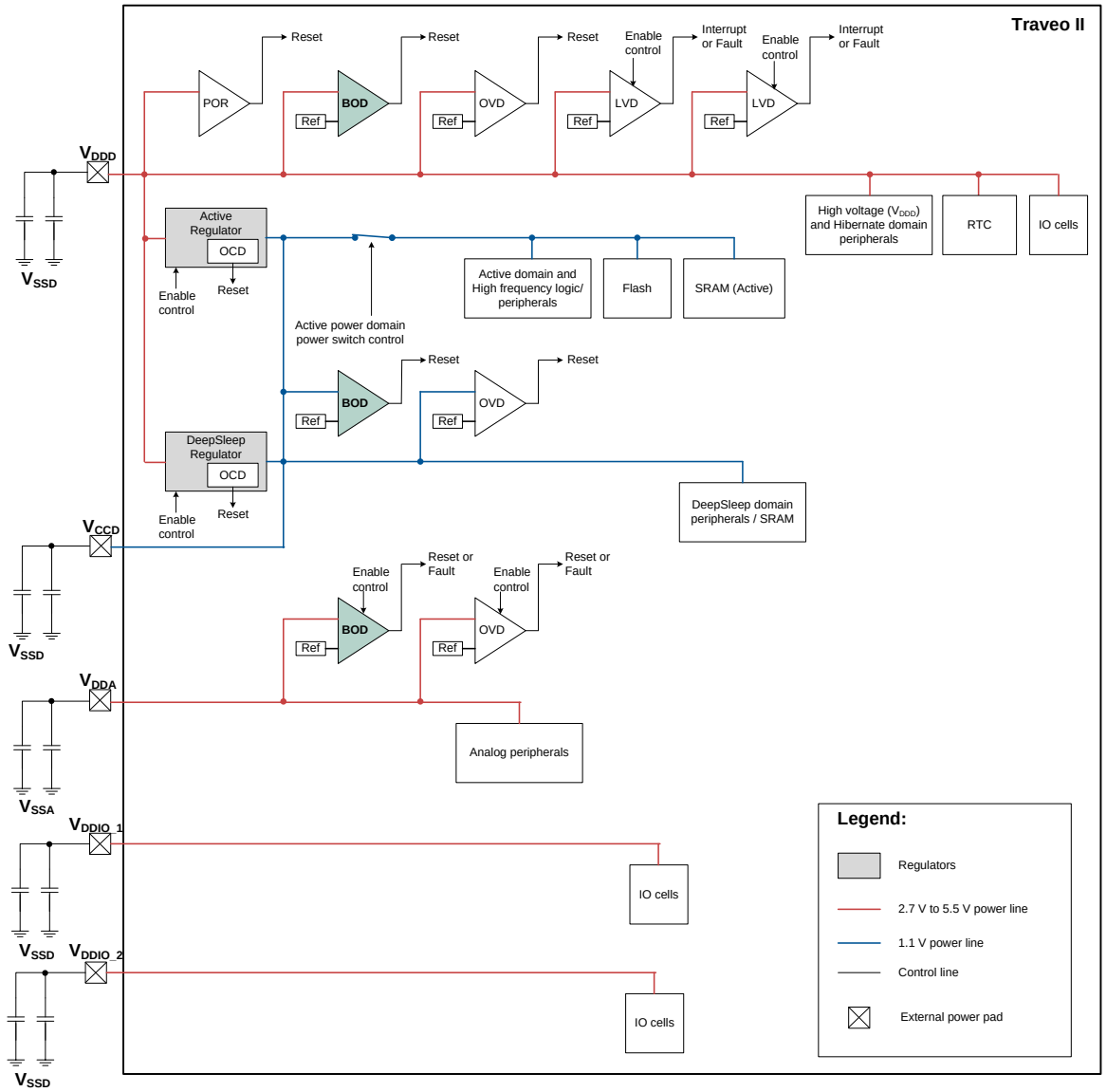
Review datasheet and TRM section 16.3.1 for additional details

Brown-out Detection (BOD)

- The Traveo II Body Entry family has three units of BOD.



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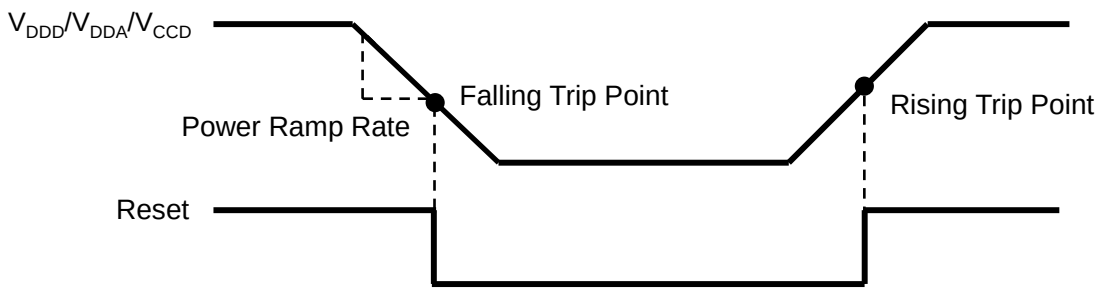
Review datasheet and TRM section 16.3 for additional details.

Brown-out Detection (BOD) Features

- Detects supply conditions below a threshold and applies a reset to the device
- Always on except in Hibernate and XRES modes
  - BOD on VDDD
    - Generates a reset if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V[1] (default) or < 3.0 V
  - BOD on VDDA
    - Generates a reset, a fault, or no action[2] (default) if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V[1] (default) or < 3.0 V
  - BOD on VCCD
    - Generates a reset if a voltage excursion dips below the falling trip point



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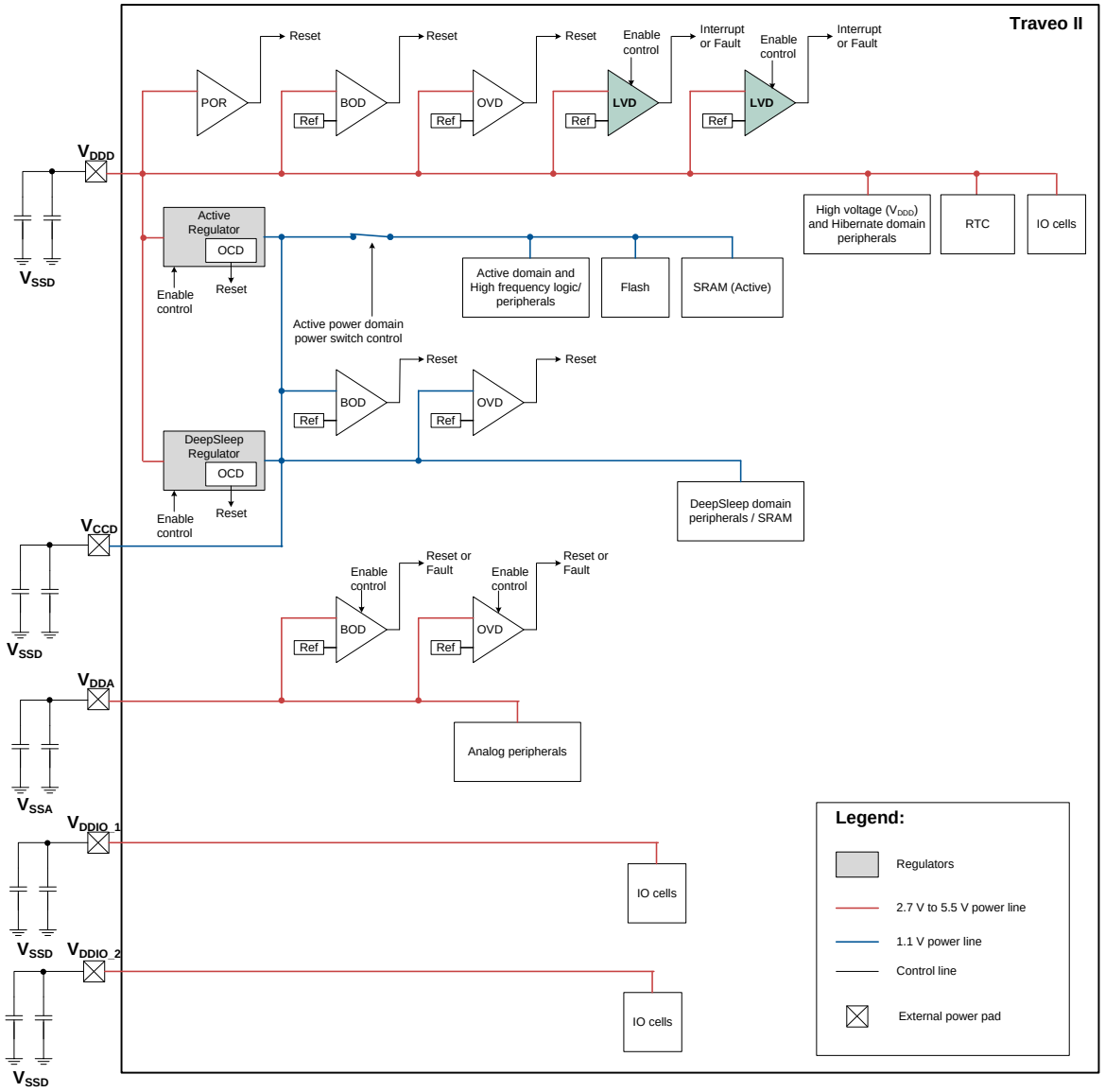
Review datasheet and TRM section 16.3.2 for additional details

[1] If V_{DDD}/V_{DDA} falls below 2.7 V (minimum V_{DDD}/V_{DDA}), the device will operate out of specification. To prevent this, use the 3.0-V trip point.
[2] Even if V_{DDA} is low, the MCU can boot because it does not generate a reset as default.

Low-Voltage Detection (LVD)

- The Traveo II Body Entry family has two units of LVD.

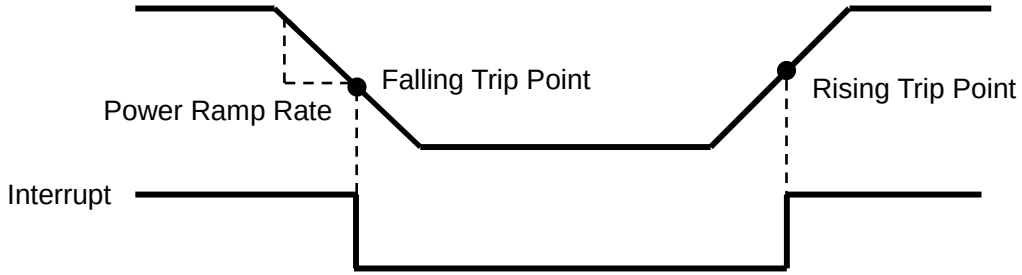


Hint Bar

Review datasheet and TRM section 16.3 for additional details

Low-Voltage Detection (LVD) Features

- Detects the warning voltage level to take preventive measures in the system
- Can be enabled or disabled (default) by software, except in Hibernate and XRES modes
  - LVD on VDDD
    - Generates an interrupt or a fault if a voltage level meets the trip point
    - An interrupt or a fault and trip point are configurable by software
    - Supports up to 26 trip points to monitor between 2.8 V and 5.3 V (0.1-V step)
    - Detection can be configured as falling (low voltage), rising (high voltage), or both
  - Use case for two LVD units
    - LVD1: Uses the falling trip point (3.5 V) to detect the low-voltage warning
    - LVD2: Uses the rising trip (5.3 V) to detect the overvoltage warning



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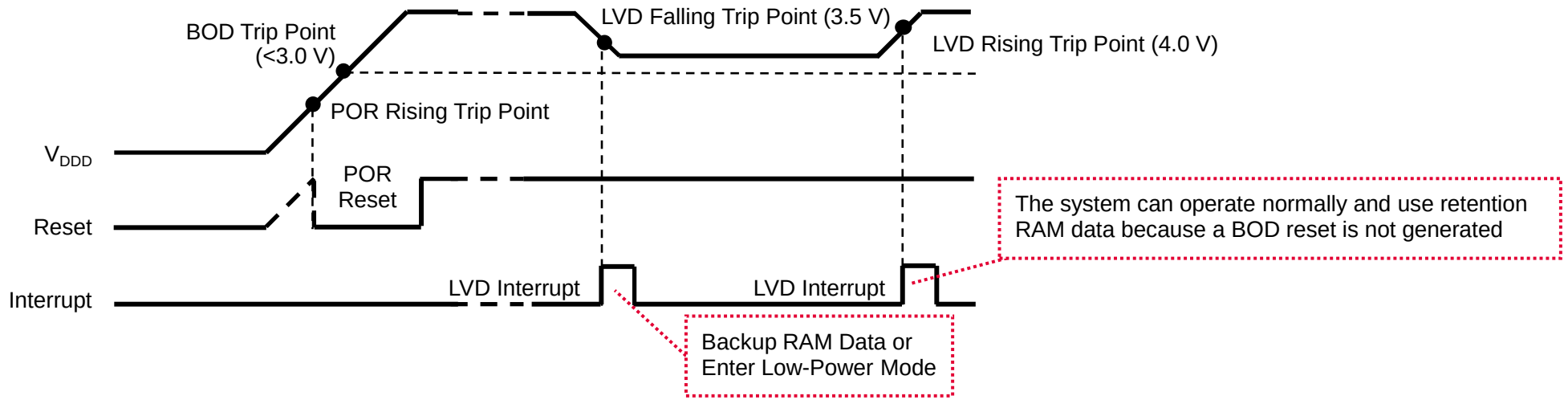
Review datasheet and TRM section 16.3.4 for additional details

POR, BOD, and LVD Use Cases (1/2)

- Purpose: Determine if RAM contents have been retained by using voltage monitoring
- MCU operating conditions
  - LVD trip point can be in MCU operation range = RAM retention
    - LVD falling trip point (3.5 V): Warning LVD for safe system operation
    - LVD rising trip point (4.0 V): User program restart trigger
  - BOD reset (< 3.0 V) is an asynchronous reset = No RAM retention

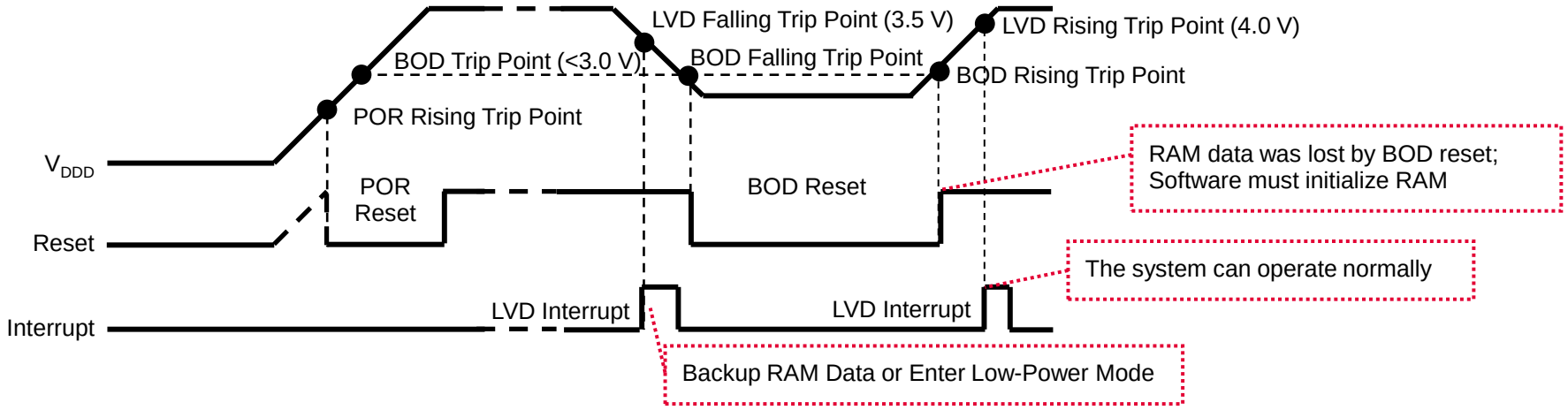
- Case: When RAM contents are retained, there is no BOD reset generation



POR, BOD, and LVD Use Cases (2/2)

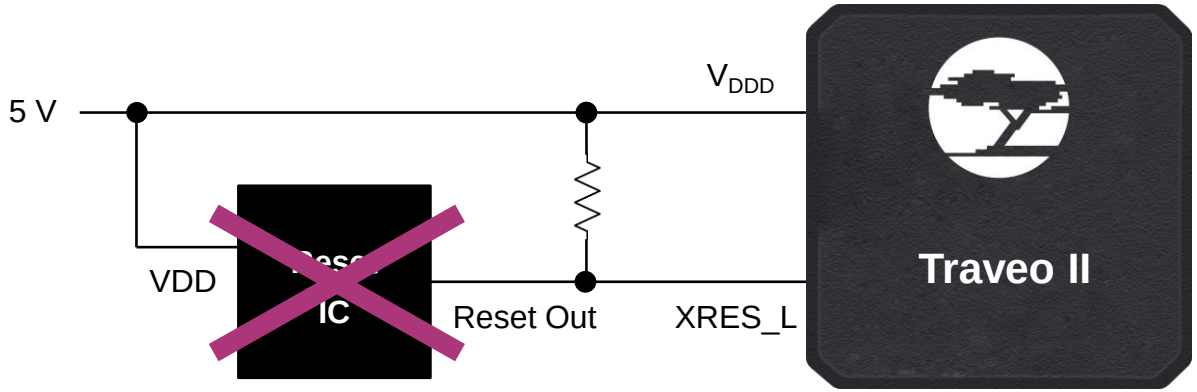
- Purpose: Judge if RAM contents have been retained by using voltage monitoring
- Setting and conditions:
  - MCU operating conditions:
    - LVD trip point can be in MCU operation range = RAM retention
      - LVD falling trip point (3.5 V): Warning LVD for safety system operation
      - LVD rising trip point (4.0 V): User program restart trigger
  - BOD reset (< 3.0 V) is an asynchronous reset = No RAM retention

- Case: For RAM, contents have not been retained (BOD reset generation)



POR, BOD, and LVD Advantages

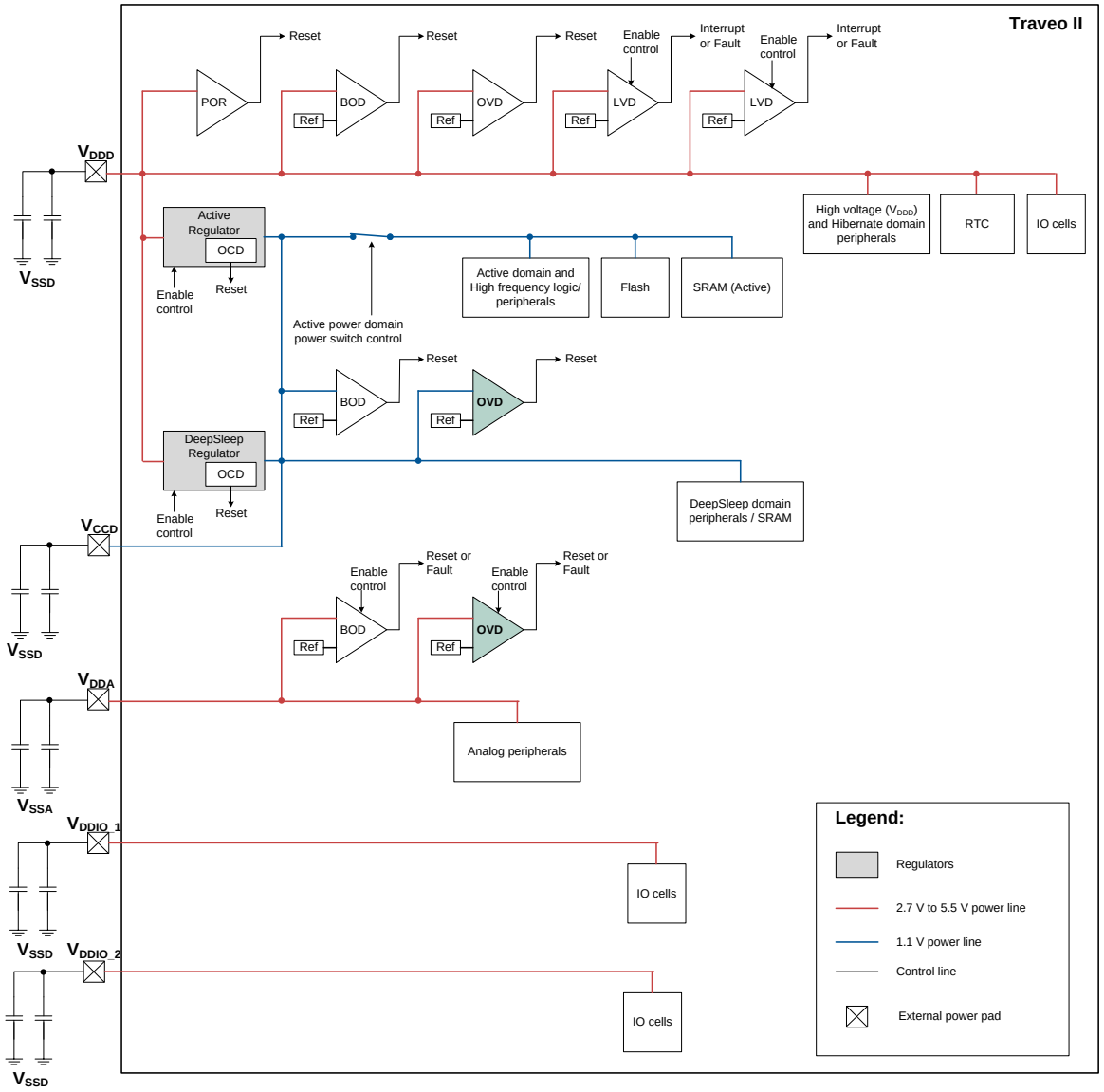
› Reduced BOM costs for low-cost applications using internal POR, BOD, and LVD[1]



[1] Review TRM and datasheet to confirm if the POR, BOD, and LVD specifications meet the safety requirements of the system.

Overvoltage Detection (OVD)

- The Traveo II Body Entry family has three units of OVD.

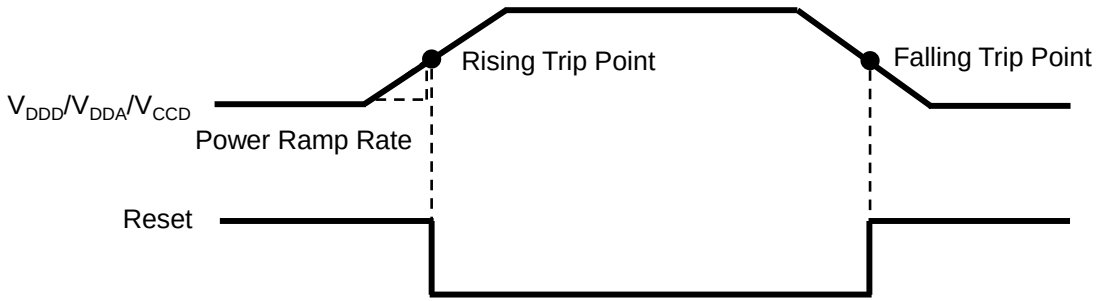


Hint Bar

Review datasheet and TRM section 16.3 for additional details

Overvoltage Detection (OVD) Features

- Detects supply conditions above a threshold and applies a reset to the device
- Always ON except in Hibernate and XRES modes
  - OVD on VDDD
    - Generates a reset if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VDDA
    - Generates a reset, a fault or no action (default) if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VCCD
    - Generates a reset if a voltage excursion dips above the rising trip point



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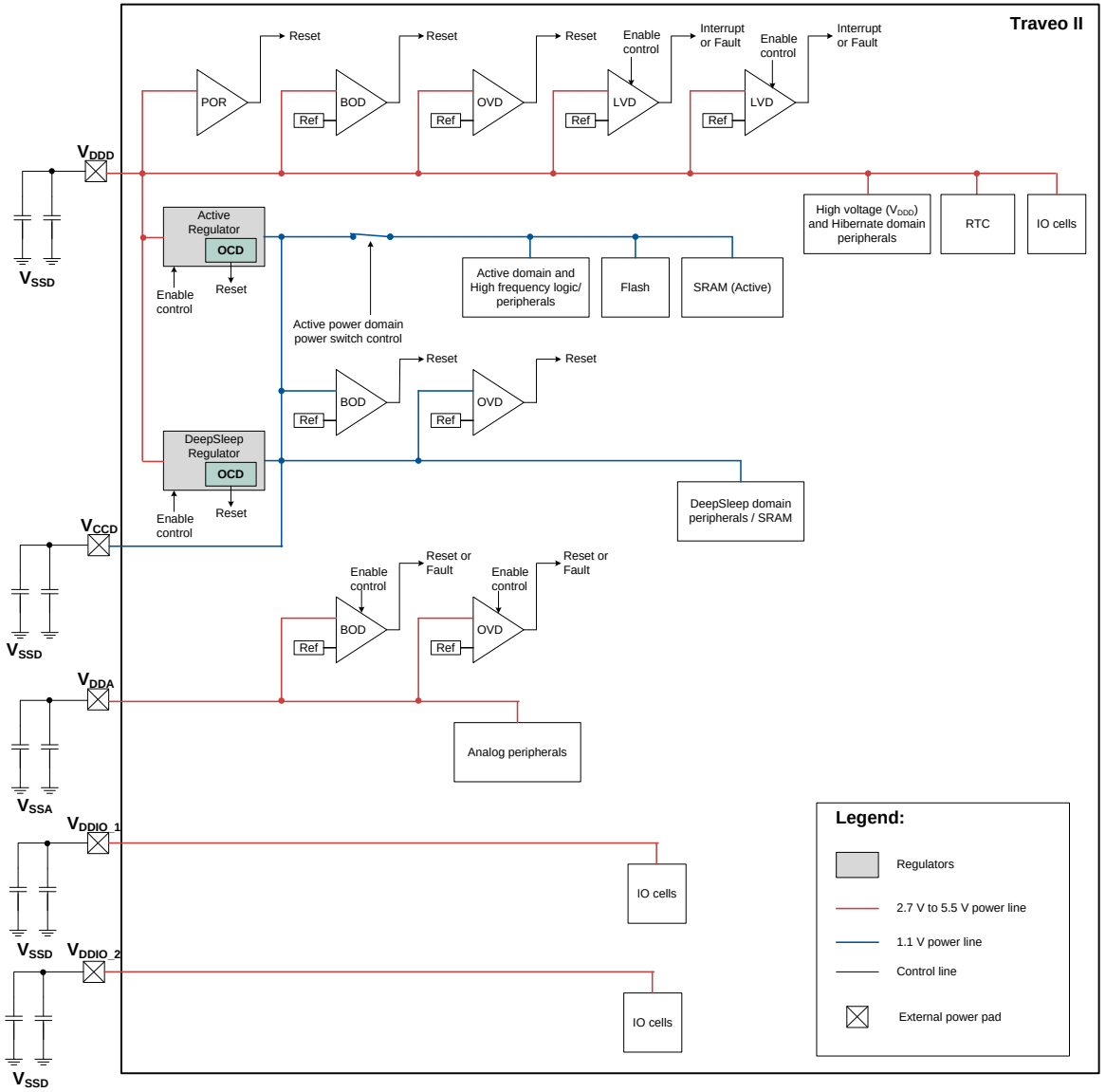
Review datasheet and TRM section 16.3.3 for additional details

Overcurrent Detection (OCD)

- The Traveo II Body Entry family has one OCD for each regulator.



Hint Bar

Review datasheet and TRM section 16.3 for additional details

Overcurrent Detection (OCD) Features

- Detects the device if the current is over the regulator limit
- Always ON except in Hibernate and XRES modes
  - OCD on VCCD
    - Generates a reset by detecting if the load current of a regulator is higher than expected

Hint Bar

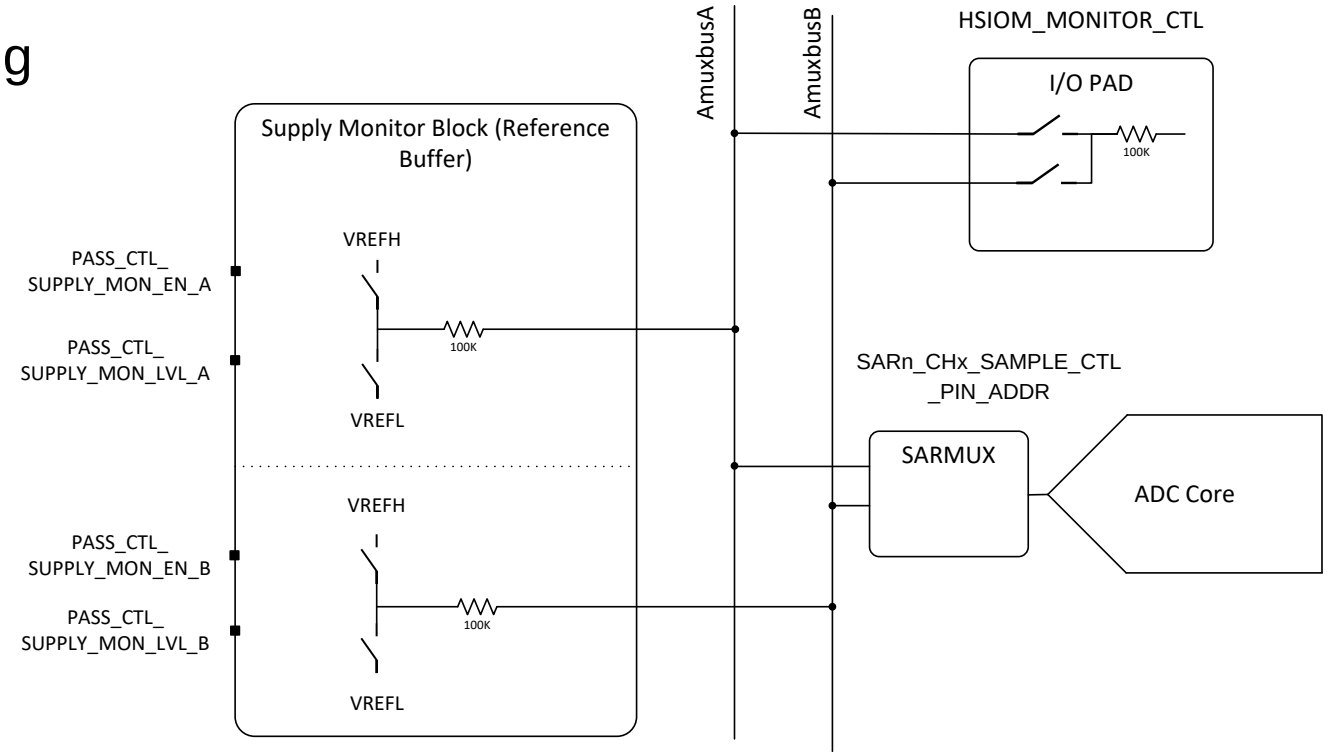
Review datasheet and TRM section 16.3.5 for additional details

Summary of Voltage Monitoring

Monitored Supply	Monitor	Trip Point	Output	Available Power Mode
V_{DDD}	POR	1 (Fixed)	Reset	All power modes
	BOD	2 (Programmable)	Reset	All power modes except Hibernate and XRES modes
	OVD	2 (Programmable)	Reset	
	LVD	26 (Programmable)	Interrupt, Fault, or No action	
V_{DDA}	BOD	2 (Programmable)	Reset, Fault, or No action	
	OVD	2 (Programmable)	Reset, Fault, or No action	
V_{CCD}	BOD	1 (Fixed)	Reset	
	OVD	1 (Fixed)	Reset	
	OCD	1 (Fixed)	Reset	

Voltage Monitoring by ADC

- All power supplies use ADC
- HSIOM_MONITOR_CTL register provides a monitor switch between power/ground pad and Amuxbus A/B
- The midpoint of the signal (Amuxbus A/B) is connected to SARMUX (internal signals) and can be selected for ADC by a channel
- Use Case:
  - VDDIO monitoring



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Review datasheet and Review TRM sections 16.3.6 and 31.10 for additional details

Power Supply Monitoring by ADC

› Relationship between HSIOM_MONITOR_CTL_0 Register and Power/Ground pins

HSIOM_MONITOR_CTL_0	Power/Ground Pins	AMUXBUS	CYT2B Package Pin Numbers				
			LQFP-176	LQFP-144	LQFP-100	LQFP-80	LQFP-64
Bit 0	V_{DDD}	A	176	144	100	80	-
Bit 1	V_{SSD}	B	1	1	1	1	-
Bit 2	V_{DDD}	A	22	18	12	-	-
Bit 3	V_{SSD}	B	23	19	13	-	-
Bit 4	V_{DDD}	A	43	35	24	-	-
Bit 5	V_{DDIO_1}[1]	A	44	36	25	20	16
Bit 6	V_{SSD}	B	45	37	26	21	17
Bit 7	V_{SSD}	B	46	38	27	21	17
Bit 8	V_{REFL}	B	76	62	41	32	26
Bit 9	V_{SSA}	B	77	63	42	33	27
Bit 10	V_{DDA}	A	78	64	43	34	28
Bit 11	V_{REFH}	A	79	65	44	35	29
Bit 12	V_{DDIO_2}	A	88	72	50	40	32
Bit 13	V_{SSD}	B	89	73	51	41	33
Bit 14	V_{DDD}	A	110	-	-	-	-
Bit 15	V_{SSD}	B	111	-	-	-	-
Bit 16	V_{DDD}	A	132	108	75	60	48
Bit 17	V_{SSD}	B	133	109	76	61	49
Bit 18	V_{DDD}	A	153	124	86	69	55
Bit 19	V_{SSD}	B	154	125	87	70	56
Bit 20	V_{SSD}	B	155	126	88	71	57

Hint Bar

Review datasheet and Review TRM sections 16.3.6 and 31.10 for additional details

Appendix

Comparison between CYT2B, CYT3B/4B, and CYT3D/4D

Features		CYT2B	CYT3B/4B	CYT3D/4D
Power Supply and Monitoring	Power supply	V_{DDD} = 2.7 V to 5.5 V	V_{DDD} = 2.7 V to 5.5 V (up to 300 mA) V_{DDD} = 2.7 V to 5.5 V and V_{CCD} = 1.15 V (exceeds 300 mA)	
	5.0 V I/O power supply	V_{DDIO_1}, V_{DDIO_2}		V_{DDIO_GPIO}, V_{DDIO_SMC}
	3.3 V I/O power supply	N/A	V_{DDIO_3}, V_{DDIO_4}	V_{DDIO_HSIO}, $V_{DDIO\_SMIF\_HV}$
	1.8 V I/O power supply	N/A		V_{DDIO_SMIF}
	Analog power supply	V_{DDA}		V_{DDA_ADC}, V_{DDA_DAC}, V_{DDA_MIPI}, V_{DDA_FPD0}, V_{DDA_FPD1}, V_{DDHA_FPD0}, V_{DDHA_FPD1}, V_{DDPLL_FPD0}, V_{DDPLL_FPD1}
	Active/DeepSleep regulator	Same		
	External transistor control	N/A	Available	N/A
	External PMIC control	N/A	Available	
	POR/BOD/OVD/LVD	Same		

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6155466	04/29/2018	Initial release
*A	6333686	10/11/2018	Added page 2, 4, 22, 23, Appendix and the note descriptions of all pages. Updated page 3, 5 to 8, 10 to 15, 17 to 21.
*B	6595227	06/14/2019	Updated page 1 to 24.
*C	6825047	03/05/2020	Updated page 5.
*D	7018164	10/28/2020	Updated page 2, 3, 5, 22, 24.