Customer Training Workshop

Traveo™ II Local Interconnect Network (LIN)

Q4 2020
Target Products

Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336 KB</td>
</tr>
</tbody>
</table>
Introduction for Traveo II Body Controller Entry

LIN is part of peripheral blocks.

Review TRM chapter 26 for additional details.
Introduction for Traveo II Body Controller High

- LIN is part of peripheral blocks.

**System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)**

**CPU Subsystem**
- Cortex M7 350 MHz
- eCT FLASH 8384 KB Code flash + 256 KB Work flash
- SRAM0 512 KB
- SRAM1 256 KB
- SRAM2 256 KB
- P-MAC

**Peripheral Interconnect (MMIO, PPU)**
- Peripheral Interconnect
- High Speed I/O Matrix, Smart I/O, Boundary Scan
- Up to 196x GPIO_STD, 4x GPIO_ENH, 40x HSIO

**I/O Subsystem**
- CYT4BF MXS40-HT ASIL-B
- System Resources
  - Power
    - Sleep Control
    - POR
    - OVP
    - LVD
    - REF
    - PWRSYS-HT
    - LD0
  - Clock
    - Clock Control
    - 2xLDO
    - WDT
    - IMO
    - FLL
    - CSV
    - 4xPLL
  - Reset
    - Reset Control
    - XRES
  - Test
    - TestMode Entry
    - Digital DFT
    - Analog DFT

**Power Modes**
- Active/DeepSleep
- LowPowerActive/DeepSleep
- Hibernate

**Hint Bar**
- Review TRM chapter 26 for additional details
Introduction for Traveo II Cluster

- LIN is part of peripheral blocks.

**Hint Bar**

Review TRM chapter 26 for additional details.
Local Interconnect Network Overview

- The LIN block supports the LIN and UART serial interface protocols
- Features (LIN)
  - ISO 17987 standard
  - Master node functionality
    - Autonomous header transmission
    - Autonomous response transmission and reception
  - Slave node functionality
    - Autonomous header reception
    - Autonomous response transmission and reception
    - Baud rate detection
  - Autonomous Error Handling
    - PID error
    - Checksum error
    - Bit error (leads to transmission stop)

Review Chapter 26 in the TRM for additional details
Features

› LIN
  - Wakeup transmission and detection
  - Timeout detection
  - Data buffer (up to 8 bytes)
  - Test modes

› UART
  - Programmable 5/6/7/8-bit data fields
  - Programmable number of STOP bits: ½, 1, 1½, or 2 bits
  - Optional parity functionality with odd and even parity

› LIN/UART
  - Oversampling
  - Noise filter
LIN Block Diagram

- LIN Unit components
  - LIN channel
  - LIN mode
  - Master operation
  - Slave operation
  - Wakeup
  - Timeout
  - UART mode
  - Test mode
  - Oversampling
  - Noise filter

Review Chapter 26 in the TRM for additional details
Master and Slave Operation Commands

- These commands are set in the CMD register

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX_HEADER</td>
<td>Transmit a header</td>
<td>Master</td>
</tr>
<tr>
<td>RX_HEADER</td>
<td>Receive a header</td>
<td>Slave</td>
</tr>
<tr>
<td>TX_RESPONSE</td>
<td>Transmit a response</td>
<td>Master, Slave</td>
</tr>
<tr>
<td>RX_RESPONSE</td>
<td>Receive a response</td>
<td>Master, Slave</td>
</tr>
<tr>
<td>TX_WAKEUP</td>
<td>Transmit a wakeup signal</td>
<td>Master, Slave</td>
</tr>
</tbody>
</table>

- Advantage
  - Reduces CPU load

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Review TRM section 26.9.1 for additional details.
LIN Mode (Master Operation)

- Header transmission
  - Operated by command
  - Only in master mode

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<table>
<thead>
<tr>
<th>Field</th>
<th>Field Description</th>
<th>Data Length</th>
<th>Buffer Available</th>
<th>Autonomous Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Break</td>
<td>LIN start frame</td>
<td>13–31 bits</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Sync</td>
<td>Baud rate synchronization</td>
<td>10 bits</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PID</td>
<td>Frame identifier and parity bit</td>
<td>8 bits</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
LIN Mode (Master Operation)

- Response transmission
  - Operated by command

<table>
<thead>
<tr>
<th>Field</th>
<th>Field Description</th>
<th>Data Length</th>
<th>Buffer Available</th>
<th>Autonomous Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>Transmission/Reception data</td>
<td>1–8 Bytes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Checksum</td>
<td>Checksum for Data field or PID and Data field (Selectable)</td>
<td>10 bits</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
LIN Mode (Master Operation)

- Response reception
  - Operated by command

Review TRM chapter 26 for additional details
Review Register TRM for additional details about the Data and Checksum field buffers
LIN Mode (Slave Operation)

- Response transmission
  - Operated by command

Hint Bar

Review TRM chapter 26 for additional details

RX RESPONSE is enabled before LIN frame, to avoid Response data loss due to delayed header reception processing.
LIN Mode (Slave Operation)

- Header and Response reception
  - Header and Response reception are operated by command
  - Header reception is only in slave mode

1 Data length and checksum type must be set before receiving the latest Stop bit of Data1 in the Response as slave.
Wakeup

- When a LIN node is in sleep state, a wakeup signal can initiate a transfer to an operational state
- Both wakeup signal generation and detection are supported in hardware
  - Wakeup signal transmission
    - Wakeup signal length is set in the register\(^1\)
  - Wakeup signal reception
    - Minimum low pulse length must be configured for detection\(^2\)
    - Wakeup is detected by the rising edge

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\(^1\) Wakeup signal setting length range: 1–31 bit periods
\(^2\) Wakeup pulse length: 250 µs–5 ms

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Baud Rate Detection

- The sync field synchronizes slave clocks to the master clock in a slave operation
- Baud rate is adjusted by software and a detected correction factor
  - Synchronization procedure
    - 1. HW measures the sync field (8-bit duration from the START bit in the figure) and sets it to SYNC_COUNTER
    - 2. SW calculates PERI clock divider value using the SYNC_COUNTER value
    - 3. SW sets PERI clock divider value to PERI clock divider register

![Synchronization Diagram](image-url)
Timeout Detection

- Timeout detections are of three types
  - Frame mode
  - Frame header mode
  - Frame response mode
- Timeout length must be configured in bit periods

Advantage
- Can set timeout value and initiate interrupt

1 Timeout length range: Frame mode: 54–75 bit periods; Frame header mode: 34–47 bit periods; Frame response mode: 20–28 bit periods.
## Interrupt Events in LIN Master Mode

<table>
<thead>
<tr>
<th>Event Type</th>
<th>Event</th>
<th>Event Detection Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>Header Transmission Done</td>
<td>Header transmission succeeded</td>
</tr>
<tr>
<td>TX</td>
<td>Response Transmission Done</td>
<td>Response transmission succeeded</td>
</tr>
<tr>
<td>RX</td>
<td>Response Reception Done</td>
<td>Response reception succeeded</td>
</tr>
<tr>
<td>Error</td>
<td>Timeout</td>
<td>A frame, header, or response does not finish within a specified time</td>
</tr>
<tr>
<td>TX Error</td>
<td>Transmitter Response Bit Error</td>
<td>During the response transmission, the received bus value does not match the transmitted value</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver Response Frame Error</td>
<td>An invalid start bit or stop bit occurs during response reception (data field, checksum)</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver Response Checksum Error</td>
<td>The calculated checksum over the data bytes, and optionally the PID field, does not match the received checksum</td>
</tr>
</tbody>
</table>
## Interrupt Events in LIN Slave Mode

<table>
<thead>
<tr>
<th>Event Type</th>
<th>Event</th>
<th>Event Detection Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>Response Transmission Done</td>
<td>Response transmission succeeded</td>
</tr>
<tr>
<td>RX</td>
<td>Header Reception Done</td>
<td>Header reception succeeded</td>
</tr>
<tr>
<td>RX</td>
<td>Response Reception Done</td>
<td>Response reception succeeded</td>
</tr>
<tr>
<td>RX</td>
<td>Synchronization Field Reception Done</td>
<td>Synchronization field successfully received</td>
</tr>
<tr>
<td>Error</td>
<td>Timeout</td>
<td>A frame, header, or response does not finish within a specified time</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver Header Frame Error</td>
<td>An invalid start bit occurs during PID field</td>
</tr>
<tr>
<td></td>
<td></td>
<td>An invalid stop bit occurs during SYNC or PID field</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver Synchronization Error</td>
<td>An invalid data field pattern is detected during the reception of the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC field</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver PID Parity Error</td>
<td>The received PID field has a parity error</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver Response Frame Error</td>
<td>An invalid stop bit occurs during response reception (data field, checksum)</td>
</tr>
<tr>
<td>RX Error</td>
<td>Receiver Response Checksum Error</td>
<td>The calculated checksum over the data bytes, and optionally the PID field, does not match the received checksum</td>
</tr>
</tbody>
</table>
LIN Channel Block Diagram

- LIN Unit components
  - LIN channel
  - UART mode

Review TRM chapter 26 for additional details
UART Mode (1/2)

Operation

- The UART frame is transmitted in
  - START bit (single bit)
  - Data field (programmable 5/6/7/8-bit data fields, single data buffer)
  - Parity bit (optional functionality with odd and even parity)
  - STOP bits (programmable ½, 1, 1½, or 2 bits)

![UART Frame Diagram]

Review TRM chapter 26 for additional details
Interrupt Events in UART Mode

<table>
<thead>
<tr>
<th>Event Type</th>
<th>Event</th>
<th>Event Detection Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>Transmission Done</td>
<td>Transmission succeeded</td>
</tr>
<tr>
<td>RX</td>
<td>Reception Done</td>
<td>Reception succeeded</td>
</tr>
<tr>
<td>Error</td>
<td>Transmitter Bit Error</td>
<td>The incoming bus level does not match the transmitted value during transmission</td>
</tr>
<tr>
<td>Error</td>
<td>Receiver Frame Error</td>
<td>An invalid start bit or stop bit occurs during reception</td>
</tr>
<tr>
<td>Error</td>
<td>Receiver Parity Error</td>
<td>The received field has a parity error</td>
</tr>
</tbody>
</table>

Review TRM section 26.11 for additional details
LIN Registers Block Diagram

› LIN Unit components
  – Test registers
    – Test mode
      – Partial Disconnect mode
      – Full Disconnect mode

Review TRM chapter 26 for additional details.
Test Modes (1/2)

- Partial Disconnect mode
  - Loopback mode via the IOSS port pin structure
  - Connection between LIN ch.\([i]\) and LIN ch.\([\text{max}]\)

- Advantage
  - The LIN frame can be monitored on the TX port pins

**Hint Bar**

Review TRM section 26.8.2 for additional details.

TVII-B-E-1M is available in the following LIN channels:
- LIN ch.\([i]\) = 0-6
- LIN ch.\([\text{max}]\) = 7
Test Modes (2/2)

- Full Disconnect mode
  - Full Loopback mode between LIN ch.[i] and LIN ch.[max]
  - There is no connection to port pins

- Advantage
  - Full LIN operation possible without external LIN bus

TVII-B-E-1M is available in the following LIN channels:
  - LIN ch.[i] = 0-6
  - LIN ch.[max] = 7

Review TRM section 26.8.2 for additional details.
Oversampling

- One LIN bit length corresponds to 16 PCLK_LINx_CLOCK_CH_ENy\(^1\) cycles
- A bit value is sampled when the oversample counter changes from ‘7’ to ‘8’

\(^1\)PCLK_LINx_CLOCK_CH_ENy is used for each LIN channel clock. This clock is derived from the peripheral interconnect (PERI) clock.
The noise filter suppresses glitches on the RX input (rx_in) signal.
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
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<tbody>
<tr>
<td>**</td>
<td>6183154</td>
<td>05/24/2018</td>
<td>Initial release</td>
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<tr>
<td>*A</td>
<td>6406686</td>
<td>12/10/2018</td>
<td>Added pages 2, 4, and 5, and the note descriptions for all pages</td>
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<td></td>
<td></td>
<td></td>
<td>Updated page 3</td>
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<tr>
<td>*B</td>
<td>6677193</td>
<td>09/13/2019</td>
<td>Updated page 2, 3, 4, 6, 7, 8, 14, 16, 20, 22, 23, 26 and 27.</td>
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<td></td>
<td></td>
<td></td>
<td>Added page 5</td>
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<tr>
<td>*C</td>
<td>7062547</td>
<td>01/08/2021</td>
<td>Updated page 2, 3, 8, 17, 20, 23, 24 and 25.</td>
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