Customer training workshop
TRAVEO™ T2G interrupts

Q4 2021
### Target product list for this training material:

<table>
<thead>
<tr>
<th>Family category</th>
<th>Series</th>
<th>Code flash memory size</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller High</td>
<td>CYT3BB/CYT4BB</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Cluster</td>
<td>CYT2CL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336 KB</td>
</tr>
</tbody>
</table>
Introduction to TRAVEO™ T2G Body Controller Entry

- The interrupt controller is in the CPUS block

Review TRM chapter 12 for additional details.
Introduction to TRAVEO™ T2G Body Controller High

The interrupt controller is in the CPUSS block

CPU Subsystem

- Cortex M7
- 350 MHz
- eCT FLASH
- 8384 KB Code flash + 256 KB Work flash
- SRAM0
- 512 KB
- SRAM1
- 256 KB
- SRAM2
- 256 KB
- PDM20
- PDM10
- MDM20
- MDM10
- CRYPTO
- AES, SHA, CRC, TRNG, RSA, ECC

System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)

Peripheral Interconnect (MMIO,PPU)

I/O Subsystem

- 196 x GPIO_STD
- 4x GPIO_ENH
- 40xHSIO
- Up to 5x Smart IO

System Resources

- Power
- Sleep Control
- POR
- OVP
- REF
- PWR SYS HT
- LDO
- Clock
- Clock Control
- 2xPLL
- 4xPLL
- IMOD
- ECO
- Test
- TestMode Entry
- Digital DFT
- Analog DFT
- Power Modes
- Active/DeepSleep
- LowPowerActive/DeepSleep

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Introduction to TRAVEO™ T2G Cluster

The interrupt controller is in the CPUSS block

Review TRM chapter 12 for additional details
Interrupts overview

› Interrupts are events generated by peripherals of each CPU
› Exceptions are events generated by each CPU

› Features
  - Up to 1023\textsuperscript{1} system interrupts
  - Any of the system interrupts can be mapped to each CPU NMI (up to four)
  - Vector table is placed in either flash or SRAM
  - Configurable priority levels (eight levels for Cortex\textsuperscript{®-M4/M7 and four levels for Cortex\textsuperscript{®-M0+}) for each interrupt
  - All the available system interrupt sources are usable in Active power mode and wake up from Sleep power mode
  - Wakeup interrupts are capable of waking the device from DeepSleep power mode

\textsuperscript{1} The total number of system interrupts varies depending on the device

Review TRM section 12.1 for additional details specific to Interrupts

Refer to each device datasheet for the list of system interrupts

Refer to the CPUSS Training Section for additional Vector Table Relocation details

\textbf{Hint Bar}
Components in interrupt architecture

The interrupt architecture consists of the following components.

- Interrupt Sources (Peripherals)
- DeepSleep Interrupt Sources (M)
- CM0+ Settings
- CM4/CM7_0/CM7_1 Settings
- Wakeup Interrupt Controller (WIC)
- Interrupt Synchronizer
- CM0+ CPU Interrupt Generation
- CM0+ Wakeup From WIC
- CM7_1 Processor
- NVIC
- Cortex-M0+ Processor Core
- CM4/CM7_0 CPU Interrupt Generation
- CM4/CM7_0 Wakeup From WIC
- NVIC
- Cortex-M4/M7_0 Processor Core

Arm provides additional reference material on their webpage at: infocenter.arm.com

Nested Vectored Interrupt Controller (NVIC)

Interrupt request (IRQ)
Interrupt architecture block diagram

Interrupt architecture components
- Interrupt sources
- System interrupts
- Wakeup interrupts

Interrupt Sources (Peripherals)

System interrupts

Wakeup interrupt Controller (WIC)

CM0+ CPU Interrupt Generation

CM0+ Wakeup From WIC

CM/CM7_0/CM7_1 Wakeup

Wakeup interrupts are mapped to the same number of CPU interrupts

CM4/CM7_0 Processor

CM0+ Processor

CM7_1 Processor

NVIC

Cortex-M0+ Processor Core

Cortex-M4/ M7_0 Processor Core

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Hint Bar

Number of system interrupts (N)
Number of wakeup interrupts (M)

Refer to the Appendix for the number of system interrupts, listed by device

Refer to each device datasheet for the list of system interrupts
Interrupt sources

› System interrupts
  – Originate from peripheral interrupts
  – Include wakeup interrupts
› Wakeup interrupts
  – Wakes CPU up from DeepSleep mode
› Use case
  – The GPIO can be used as a CAN wake-up interrupt

Hint Bar
- Review TRM section 12.5 for additional details about system interrupts
- Refer to each device datasheet for the list of system interrupts
- Review TRM section 12.10 for additional details about wakeup interrupts
- Wakeup from DeepSleep mode involves the WIC
- Review TRM section 12.10 for additional details specific to WIC
- Review the Device Power Modes training section for additional Wakeup Interrupts details
Interrupt synchronizer

Interrupt architecture components

- Interrupt synchronizer

Synchronizes the interrupts to the CPU clock frequency as the peripheral interrupts can be asynchronous to the CPU clock frequency.

Hint Bar

Review TRM section 12.5 for additional details about system interrupts.
Refer to each device datasheet for the list of system interrupts.
Review TRM section 12.10 for additional details about wakeup interrupts.
Wakeup from DeepSleep mode involves the WIC.
Review TRM section 12.10 for additional details specific to WIC.
Review the Device Power Modes training section for additional Wakeup Interrupts details.
CPU interrupt

Interrupt architecture components

- CPU interrupt
  - Each system interrupt can be mapped to exactly one CPU interrupt of each core
  - Achieved using the register setting
    - CM0/CM4/CM7_0/CM7_1_SYSTEM_INT_CTL.CPU_INT_IDX[2:0]
    - CM0/CM4/CM7_0/CM7_1_SYSTEM_INT_CTL.CPU_INT_VALID

Refer to each device datasheet for the list of system interrupts

CM7_0 and CM7_1 represent the first and the second CM7 core in the CYT4 device, respectively
Interrupt handler processing (1/3)

Sequence of a normal interrupt request handling

1. Interrupt request asserts IRQn
2. When the IRQn request can be accepted, the NVIC sets the pending status
3. Jumps to the interrupt handler
4. Entering the interrupt handler clears the pending status
5. Clears the interrupt flag of the peripheral register
6. Reads the interrupt flag of the peripheral register to drain the Write Buffer
7. Return
Interrupt handler processing (2/3)

› The CPU interrupt handler uses the SYSTEM_INT_IDX field to index a system interrupt lookup table and jump to the system interrupt handler
› Read after write (RAW) is important in the interrupt handler processing to ensure completion of the write buffer

Hint Bar

Review TRM section 12.5 for additional details
The lookup table is usually located in one of the system memories
The following code illustrates the sequence:

```c
void CM4/CM7_0/CM7_1_CpuIntr0_Handler (void)
{
    // Clear the peripheral interrupt request flag by register write
    // Read back the register to ensure completion of register write access
    if(CPUSS_CM4/CM7_0/CM7_1_INT_STATUS[0].SYSTEM_INT_VALID)
    {
        system_int_idx = CPUSS_CM4/CM7_0/CM7_1_INT_STATUS[0].SYSTEM_INT_IDX;
        handler = SystemIntr_Table[system_int_idx];
        handler(); // jump to system interrupt handler
    }
    else
    {
        // Triggered by software or due to software cleared a peripheral interrupt flag
        // but did not clear the Pending flag at NVIC
    }
}
...
void CM4/CM7_0/CM7_1_CpuIntr7_Handler (void)
{
    // Clear the peripheral interrupt request flag by register write
    // Read back the register to ensure completion of register write access
    if(CPUSS_CM4/CM7_0/CM7_1_INT_STATUS[7].SYSTEM_INT_VALID)
    {
        system_int_idx = CPUSS_CM4/CM7_0/CM7_1_INT_STATUS[7].SYSTEM_INT_IDX;
        handler = SystemIntr_Table[system_int_idx];
        handler(); // jump to system interrupt handler
    }
    else
    {
        // Triggered by software or due to software cleared a peripheral interrupt flag
        // but did not clear the Pending flag at NVIC
    }
}
void CM4/CM7_0/CM7_1_SystemIntr0_Handler (void)
{
    // Clear the peripheral interrupt request flag by register write
    // Read back the register to ensure completion of register write access
    // Handle system interrupt 0.
}
...
void CM4/CM7_0/CM7_1_SystemIntr1022_Handler (void)
{
    // Clear the peripheral interrupt request flag by register write
    // Read back the register to ensure completion of register write access
    // Handle system interrupt 1022.
}
```
Interrupt architecture components

- NVIC
  - CPU interrupt priority
  - Nested interrupts
The exception vector tables store the entry point addresses for all exception handlers in Cortex®-M0+, Cortex®-M4, and Cortex® M7 cores.

### Cortex-M0+ Exception Vector Table

<table>
<thead>
<tr>
<th>Exception #</th>
<th>Exception</th>
<th>Exception Priority</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>–</td>
<td>Initial stack pointer value</td>
<td>Not applicable (N/A)</td>
<td>Start_Address = 0x0000 or CM0P_SCS_VTOR¹</td>
</tr>
<tr>
<td>1</td>
<td>Reset</td>
<td>–3, highest priority</td>
<td>Start_Address + 0x04</td>
</tr>
<tr>
<td>2</td>
<td>Non-maskable Interrupt (NMI)</td>
<td>–2</td>
<td>Start_Address + 0x08</td>
</tr>
<tr>
<td>3</td>
<td>Hard fault</td>
<td>–1</td>
<td>Start_Address + 0x0C</td>
</tr>
<tr>
<td>4–10</td>
<td>Reserved</td>
<td>N/A</td>
<td>Start_Address + 0x10 to Start_Address + 0x28</td>
</tr>
<tr>
<td>11</td>
<td>Supervisory call (SVCall)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x2C</td>
</tr>
<tr>
<td>12–13</td>
<td>Reserved</td>
<td>N/A</td>
<td>Start_Address + 0x30 to Start_Address + 0x34</td>
</tr>
<tr>
<td>14</td>
<td>Pend supervisory (PendSV)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x38</td>
</tr>
<tr>
<td>15</td>
<td>System tick timer (SysTick)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x3C</td>
</tr>
<tr>
<td>16</td>
<td>External interrupt (IRQ0)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x40</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>23</td>
<td>External interrupt (IRQ7)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x5C</td>
</tr>
<tr>
<td>24</td>
<td>Internal (SW only) interrupt (IRQ8)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x60</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>31</td>
<td>Internal (SW only) interrupt (IRQ15)</td>
<td>Configurable (0–3)</td>
<td>Start_Address + 0x7C</td>
</tr>
</tbody>
</table>

¹ Start Address = 0x0000 on reset and is later modified in the user code by updating the CM0P_SCS_VTOR register

### Hint Bar

- **Review TRM section 12.3.3 for additional details**
- **IRQ0-IRQ7 are connected to the System Interrupt generation logic**
- **IRQ8-IRQ15 can be triggered by software only and are not connected to any peripheral**
### Exception vector table (2/2)

<table>
<thead>
<tr>
<th>Exception #</th>
<th>Exception Description</th>
<th>Exception Priority</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>–</td>
<td>Initial stack pointer value</td>
<td>–</td>
<td>Start_Address = 0x0000 or CM4/CM7_0/CM7_1_SCS_VTOR¹</td>
</tr>
<tr>
<td>1</td>
<td>Reset</td>
<td>–3, highest priority</td>
<td>Start_Address + 0x0004</td>
</tr>
<tr>
<td>2</td>
<td>Non-maskable Interrupt (NMI)</td>
<td>–2</td>
<td>Start_Address + 0x0008</td>
</tr>
<tr>
<td>3</td>
<td>Hard fault</td>
<td>–1</td>
<td>Start_Address + 0x000C</td>
</tr>
<tr>
<td>4</td>
<td>Memory management fault</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x0010</td>
</tr>
<tr>
<td>5</td>
<td>Bus fault</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x0014</td>
</tr>
<tr>
<td>6</td>
<td>Usage fault</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x0018</td>
</tr>
<tr>
<td>7–10</td>
<td>Reserved</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>11</td>
<td>Supervisory call (SVCall)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x002C</td>
</tr>
<tr>
<td>12–13</td>
<td>Reserved</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>14</td>
<td>Pend supervisory (PendSV)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x0038</td>
</tr>
<tr>
<td>15</td>
<td>System tick timer (SysTick)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x003C</td>
</tr>
<tr>
<td>16</td>
<td>External interrupt (IRQ0)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x0040</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>23</td>
<td>External interrupt (IRQ7)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x005C</td>
</tr>
<tr>
<td>24</td>
<td>Internal (SW only) interrupt (IRQ8)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x060</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>31</td>
<td>Internal (SW only) interrupt (IRQ15)</td>
<td>Configurable (0–7)</td>
<td>Start_Address + 0x7C</td>
</tr>
</tbody>
</table>

¹ Start Address = 0x0000 on reset and is later modified by the user code by updating the CM4/CM7_0/CM7_1_SCS_VTOR register

**Hint Bar**

Review TRM section 12.3.3 for additional details

- IRQ0-IRQ7 are connected to the System Interrupt generation logic
- IRQ8-IRQ15 can be triggered by software only and are not connected to any peripheral
CPU interrupt priority

- The priority of each interrupt can be configured to eight levels for both Cortex®-M4 and M7 and four levels for Cortex®-M0+
- Use case for CPU interrupt priority
  - Example of priority levels and interrupts for body application

<table>
<thead>
<tr>
<th>Priority Level</th>
<th>Interrupt</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>Fault</td>
<td>NMI exception, protection violation</td>
</tr>
<tr>
<td>0</td>
<td>GPIO</td>
<td>Ignition detection, wakeup use</td>
</tr>
<tr>
<td>1</td>
<td>CAN</td>
<td>Communication with other ECU</td>
</tr>
<tr>
<td>2</td>
<td>LIN</td>
<td>Communication with other ECU</td>
</tr>
<tr>
<td>3</td>
<td>SCB</td>
<td>Communication with external IC</td>
</tr>
<tr>
<td>4</td>
<td>TCPWM</td>
<td>Task management</td>
</tr>
<tr>
<td>5</td>
<td>Event Generator</td>
<td>Wakeup use</td>
</tr>
<tr>
<td>6</td>
<td>ADC</td>
<td>Sensor data acquisition</td>
</tr>
<tr>
<td>7</td>
<td>RTC</td>
<td>Real-time clock alarm</td>
</tr>
</tbody>
</table>

- Review TRM section 12.5 for additional details
- Refer to each device datasheet for the list of system interrupts
Nested interrupts

- Depending on the interrupt priority level, nested interrupts are possible
- Use case for nested interrupts

Panels:
- **ADC Interrupt**
- **CAN Interrupt**
- **LIN Interrupt**

Flow:
1. Main Routine Resumes
2. ADC Interrupt
3. CAN Interrupt
4. LIN Interrupt
5. CAN Routine
6. Main Routine Resumes
7. LIN Routine
8. LIN Routine
9.Main Routine Resumes
10. Main Routine Resumes
11. ADC Routine

Priority Levels:
- ADC: Priority Level = 6
- CAN: Priority Level = 1
- LIN: Priority Level = 1

**Hint Bar**
- Review TRM section 12.5 for additional details
- CAN is serviced before LIN based on the index order of system interrupts
- Refer to each device datasheet for the list of system interrupts

**Additional Information:**
- CAN is serviced before LIN based on the index order of system interrupts.
Enabling and disabling interrupts

- The NVICs of CM0+, CM4, and CM7 cores provide registers to individually enable and disable the CPU interrupts in software.
- CM0+, CM4, and CM7 interrupts are enabled and disabled using the ISER and ICER.
- If an interrupt is not enabled, the NVIC will not process the interrupt requests on that interrupt line.
- CM0+, CM4, and CM7 provide additional registers to control the activation of exceptions/interrupts based on their priority:
  - PRIMASK: Prevent activation of exceptions having configurable priority.
  - FAULTMASK: Prevent activation of all exceptions other than NMI.
  - BASEPRI: Prevent activation of exceptions having the same or lower priority than the BASEPRI.

Review TRM section 12.7 for additional details.
Exception states

Each exception can be in one of the following states:

1. **Inactive**
   - Not Active
   - Not Pending

2. **Active**
   - IRQ3 (CAN) priority = 1

3. **Pending**
   - IRQ3 (TCPWM) priority = 1

4. **Active**
   - IRQ5 (Fault) Priority= 0

5. **Pending**
   - Pending exception is serviced after the execution of exceptions with higher priority is complete

6. **Active**

7. **Active**

8. **Return**

9. **Active**

10. **Return**

11. **Active**

12. **Return**

Exception is serviced by the processor, pending a request from the same source during exception handler execution.

Review TRM section 12.8 for additional details.
Appendix
Number of interrupts

- Maximum number of system interrupts and wakeup interrupts varies by device.

<table>
<thead>
<tr>
<th>Series</th>
<th>Maximum number of system interrupts</th>
<th>Maximum number of wakeup interrupts</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYT2B6</td>
<td>228</td>
<td>38</td>
</tr>
<tr>
<td>CYT2B7</td>
<td>353</td>
<td>45</td>
</tr>
<tr>
<td>CYT2B9</td>
<td>383</td>
<td>45</td>
</tr>
<tr>
<td>CYT2BL</td>
<td>383</td>
<td>45</td>
</tr>
<tr>
<td>CYT3BB/CYT4BB</td>
<td>443</td>
<td>51</td>
</tr>
<tr>
<td>CYT4BF</td>
<td>567</td>
<td>51</td>
</tr>
<tr>
<td>CYT2CL</td>
<td>786</td>
<td>44</td>
</tr>
<tr>
<td>CYT3DL</td>
<td>795</td>
<td>34</td>
</tr>
<tr>
<td>CYT4DN</td>
<td>795</td>
<td>38</td>
</tr>
</tbody>
</table>
Part of your life. Part of tomorrow.
<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission date</th>
<th>Description of change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6154903</td>
<td>04/29/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6396762</td>
<td>11/29/2018</td>
<td>Added pages 2, 4, and 5 and note descriptions for all pages</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated pages 3, 6, 7, 8, 10, 11, 14, 15, 16, 17, 18, and 20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Changed the contents of the Appendix section</td>
</tr>
<tr>
<td>*B</td>
<td>6612968</td>
<td>07/04/2019</td>
<td>Updated note descriptions for pages 3, 4, 5, 23, and 24</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated pages 2, 5, 14, and 23</td>
</tr>
<tr>
<td>*C</td>
<td>7042917</td>
<td>12/11/2020</td>
<td>Updated page 2, 3, 9 and 23</td>
</tr>
<tr>
<td>*D</td>
<td>7400452</td>
<td>10/15/2021</td>
<td>Updated page 1 to 5, 11, 14, 23</td>
</tr>
</tbody>
</table>