

# Customer Training Workshop Traveo™ II Graphics Subsystem

Q4 2020



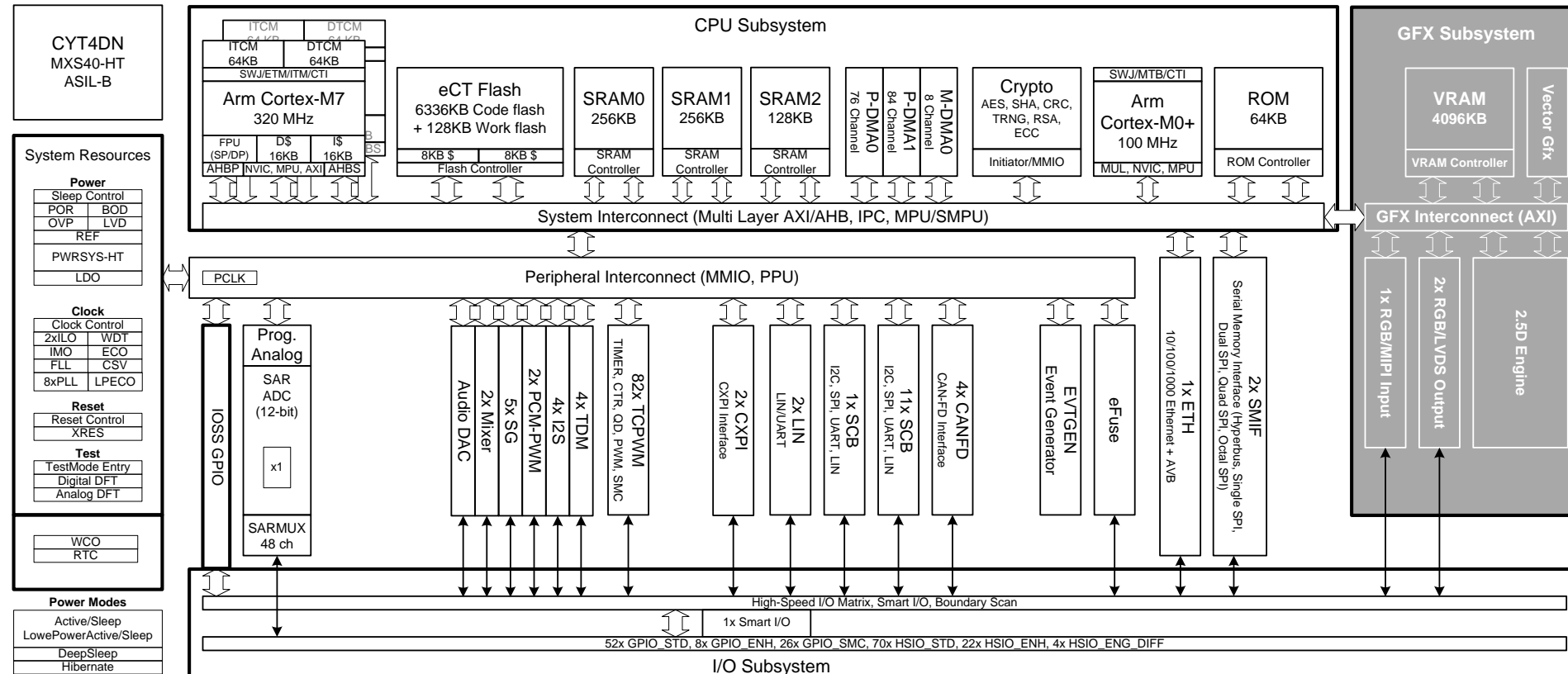
# Target Products

- › Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Cluster 2D	CYT3DL	Up to 4160 KB
Traveo II Automotive Cluster 2D	CYT4DN	Up to 6336 KB

# Introduction to Traveo II Cluster

## > Graphics subsystem connects to the CPU subsystem



**Hint Bar**

**Review TRM chapter 34 for additional details**

# Graphics Subsystem Overview

- › Graphics subsystem integrates an internal video RAM, a 2D graphics core, and interfaces for video input and output processing
- › Features
  - 4-MB internal video RAM
  - Graphics core for rendering 2D
  - Display and composition engines
  - Capture engine for one video input stream
  - Video I/O interface

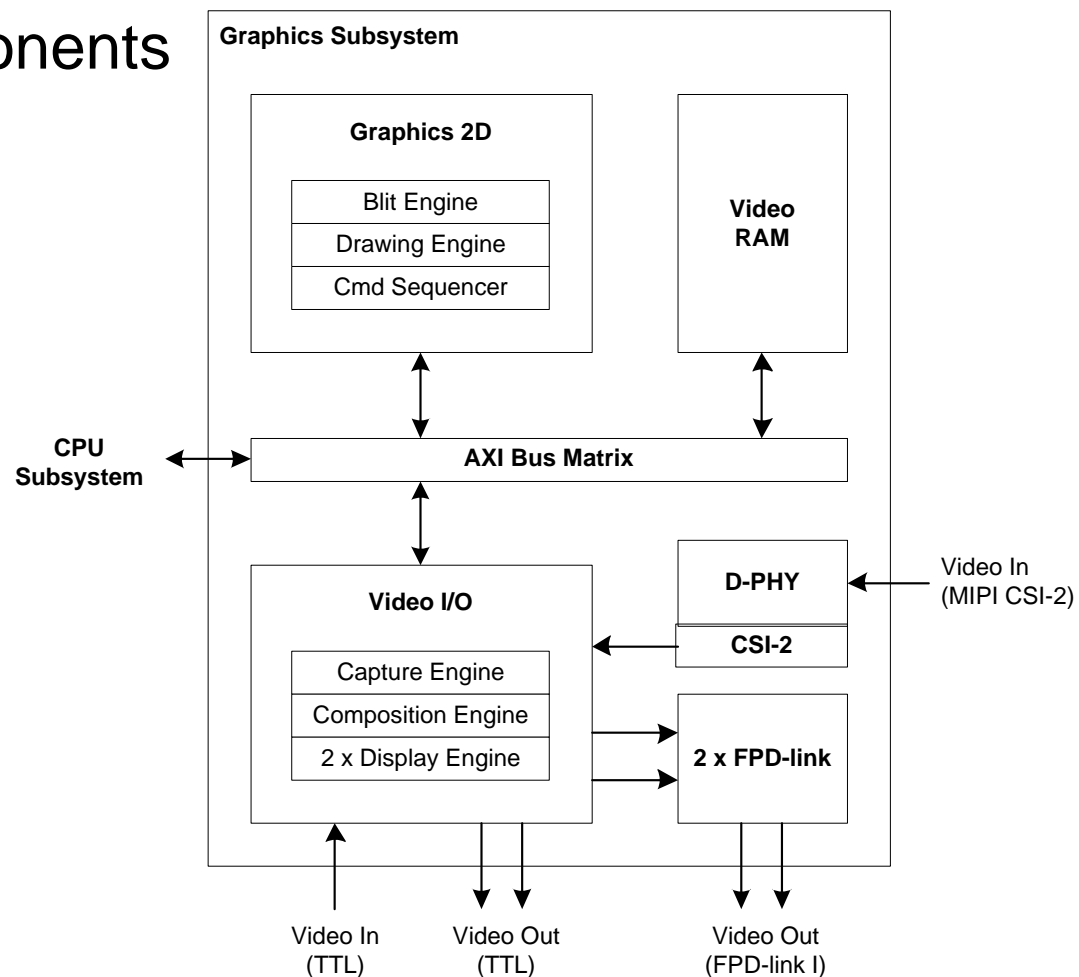
## Hint Bar

Review TRM section 34.1 for additional details

# Graphics Subsystem Block Diagram

## > Graphics subsystem components

- Graphics 2D
- Video I/O
- Video RAM (VRAM)
- D-PHY and CSI-2
- FPD-link



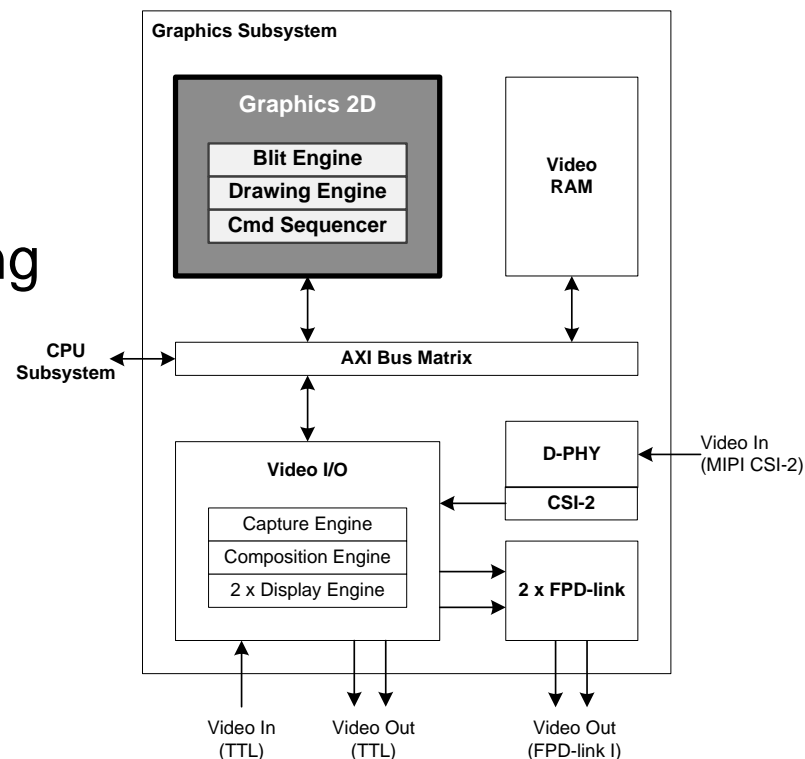
### Hint Bar

Review TRM section 34.3 for additional details

**Graphics Subsystem should not be powered off while AXI interface between CPU Subsystem and VRAM is not IDLE.**

# Graphics 2D (1/2)

- > Graphics 2D engine includes:
  - Blit engine for raster graphics<sup>1</sup>
  - Drawing engine for vector graphics<sup>2</sup>
  - Command sequencer to offload the CPU from programming and controlling the blit and drawing engines
- > Advantages:
  - Renders graphics directly to display (on-the-fly). This enables the internal video RAM to become sufficient for 720p graphics and saves BOM cost because the system does not require external DDR RAM



## Hint Bar

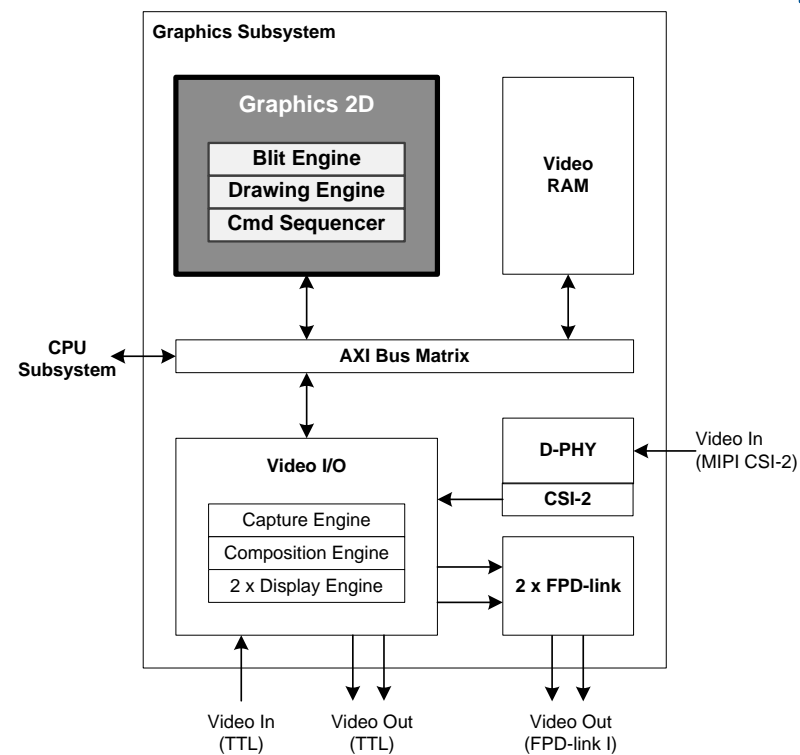
Review TRM section 34.3.1 for additional details.

<sup>1</sup> Raster graphics: Raster graphics draws bitmap images, supports scaling and transformation.

<sup>2</sup> Vector graphics: Vector graphics draws lines and curves, typically used for outline font rendering.

# Graphics 2D (2/2)

- > Features:
  - 250-MHz core clock, 750 Mpixels/s peak rate
  - Image size up to 1600 x 720 pixels
  - Standard blit operations
  - Image scaling and rotation by any angle
  - Perspective correction for 3D effect (2.5D)
  - Compressed source images (lossless or lossy)
  - Vector drawing accelerator (Bezier curve<sup>1</sup> rasterization)
  - Command sequencer to minimize CPU interaction
  - Render on-the-fly to display (except vector drawing)



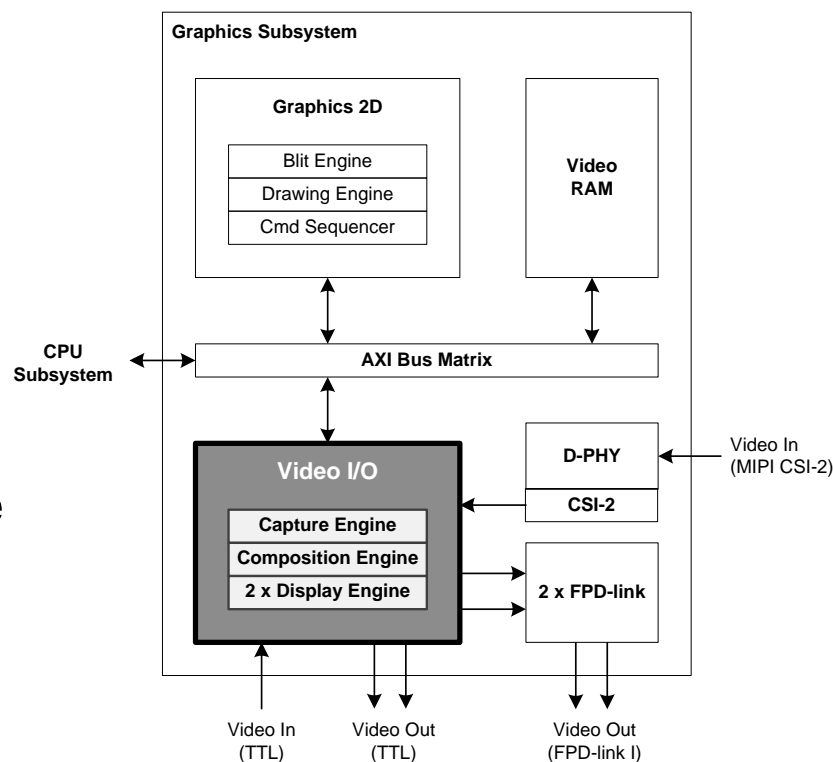
## Hint Bar

Review TRM section 34.3.1 for additional details.

<sup>1</sup> Bezier curve: Bezier curve is a parametric curve, draws a smoothing curve with one control point.

# Video I/O (1/2)

- > Video I/O includes:
  - Capture Engine: control logic for video input
  - Display Engine: control logic for output interfaces
  - Composition Engine: image processing functions, such as display scene composition by layer blending
  
- > Capture Engine Features:
  - 220-MHz pixel clock, 2880 x 1080 active pixels, RGB/YUV format
  - Frame rate conversion via ring buffer in video RAM
  - Downscaling (only if display does not upscale)
  - Feed-through (direct capture) on-the-fly to display with graphics overlay



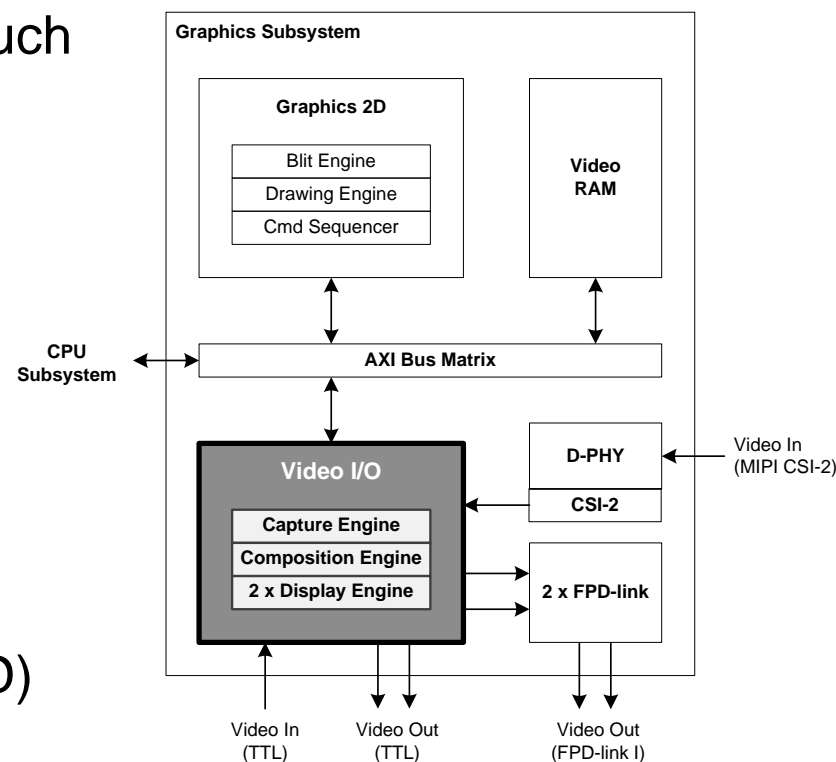
## Hint Bar

Review TRM section 34.3.2 for additional details.



## Video I/O (2/2)

- › Display and Composition Engine Features:
  - Two independent video output stream (such as cluster and HUD<sup>1</sup>)
  - 220 MHz pixel clock, 2880 x 1080 active pixels, RGB format
  - Five transparent layers in total (alpha blending)
  - 26 windows in total (individual setup and frame buffers)
  - Four independent layer composition streams
  - One layer can be warped on-the-fly (HUD)
  - One layer can be upscaled on-the-fly
  - Gamma correction<sup>2</sup> and dithering<sup>3</sup>
  - CRC<sup>4</sup> check on eight regions per display



### Hint Bar

Review TRM section 34.3.2 for additional details.

<sup>1</sup> HUD: Head-Up Display

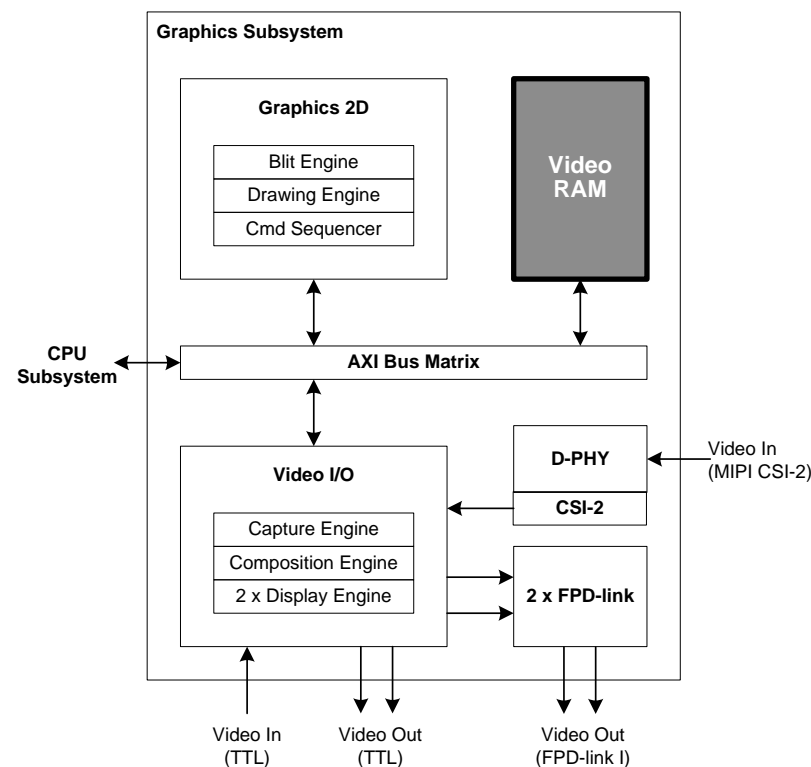
<sup>2</sup> Gamma correction: Gamma correction is a nonlinear operation, typically used for brightness and contrast control.

<sup>3</sup> Dithering: Dithering increases the physical color resolution of a display from 5, 6, 7 or 8 bits per RGB channel to a virtual resolution of 10 bits.

<sup>4</sup> CRC: Cyclic Redundancy Check

# Video RAM (VRAM)

- > VRAM enables simultaneous access to a shared VRAM address space through AXI slave interfaces
- > VRAM maps and interleaves AXI accesses to eight logical VRAM banks
- > A port with a higher priority is always arbitrated first. Ports with the same priority will be round-robin arbitrated



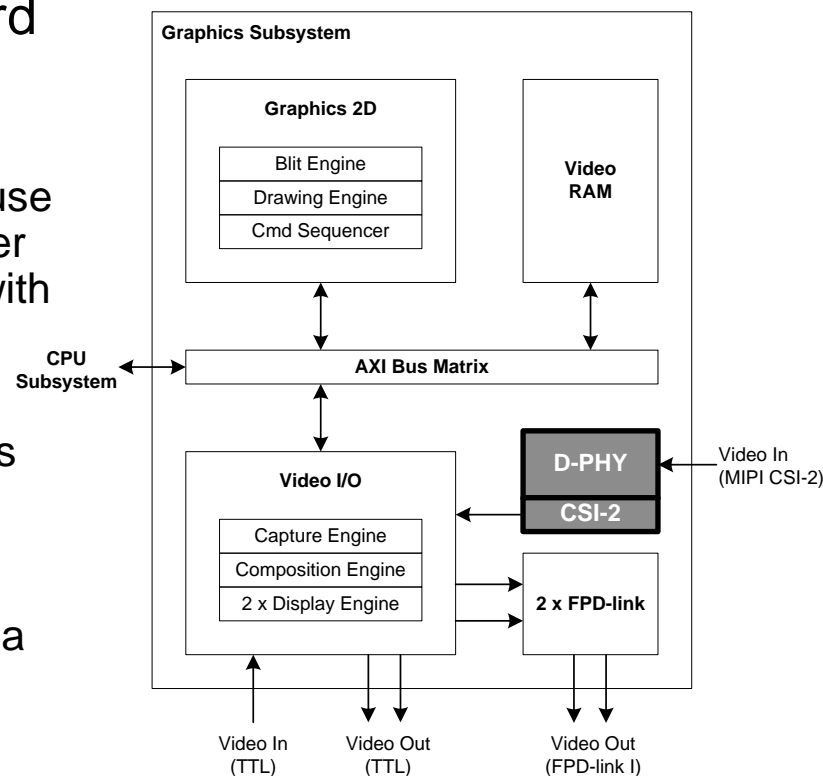
## Hint Bar

Review TRM section 34.3.3 for additional details.

# CSI-2 and D-PHY

› CSI-2 controller and D-PHY<sup>1</sup> capture image information from a camera via a MIPI standard CSI-2 type interface

- CSI-2 controller
  - Provides a flexible, high-performance, easy-to-use MIPI Camera Serial Interface 2 (CSI-2) controller
  - Supports a packet-based protocol to interface with mobile cameras
- D-PHY
  - High-frequency, low-power, source-synchronous physical layer that supports the MIPI Alliance Standard for D-PHY
  - Supports up to four data lanes running at a maximum data rate of 1.5 Gbps per lane giving a maximum aggregate throughput of 6 Gbps



## Hint Bar

Review TRM chapter 36 for additional details.

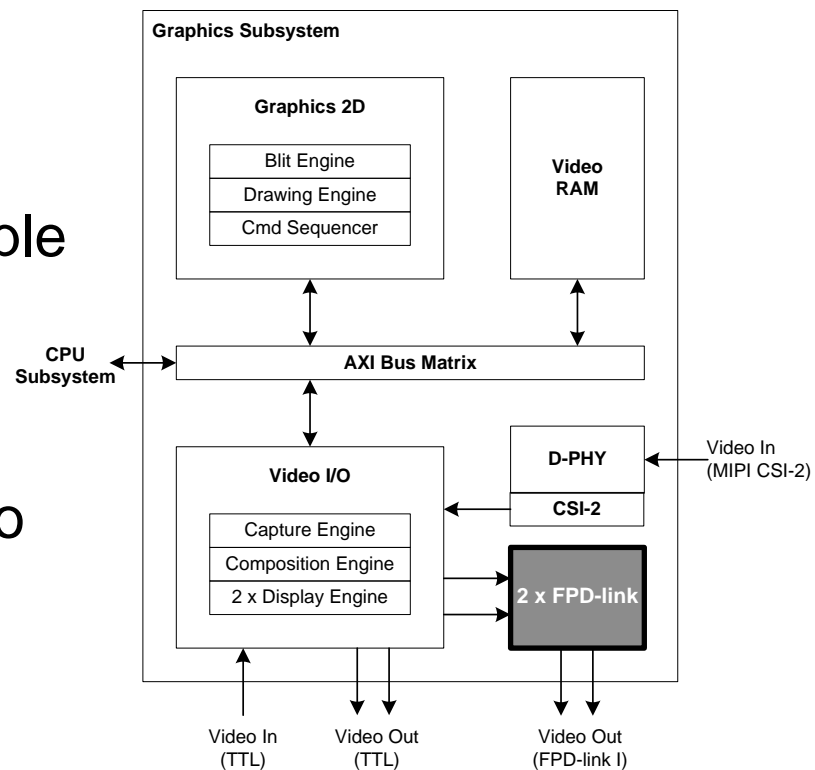
› Use case

- Rear camera
- Parking assist camera

<sup>1</sup> D-PHY: Physical layer for high-performance, cost-optimized cameras and displays

# FPD-link

- > FPD-Link interface is a 7:1 serializer
- > Transports uncompressed digital video across four or five LVDS1 links
- > Converts the wide parallel bus into multiple high-speed serial streams, carried on differential links between the display controller and the display
- > Each serial lane transports 7 bits of video and control data per cycle of the LVDS clock (TXCLK) signal



## Hint Bar

Review TRM chapter 35 for additional details.

<sup>1</sup> LVDS: Low Voltage Differential Signaling



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# Revision History

Revision	ECN	Submission Date	Description of Change
**	6638974	2019-07-29	Initial release
*A	7020960	2020-10-20	Updated slides 2, 5.