Customer Training Workshop
Traveo™ II Graphics Subsystem
Target Products

- Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Cluster 2D</td>
<td>CYT3DL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster 2D</td>
<td>CYT4DN</td>
<td>Up to 6336 KB</td>
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Introduction to Traveo II Cluster

- Graphics subsystem connects to the CPU subsystem

Review TRM chapter 34 for additional details
Graphics Subsystem Overview

- Graphics subsystem integrates an internal video RAM, a 2D graphics core, and interfaces for video input and output processing
- Features
  - 4-MB internal video RAM
  - Graphics core for rendering 2D
  - Display and composition engines
  - Capture engine for one video input stream
  - Video I/O interface

Review TRM section 34.1 for additional details
Graphics Subsystem Block Diagram

- Graphics subsystem components
  - Graphics 2D
  - Video I/O
  - Video RAM (VRAM)
  - D-PHY and CSI-2
  - FPD-link
Graphics 2D (1/2)

Graphics 2D engine includes:
- Blit engine for raster graphics\(^1\)
- Drawing engine for vector graphics\(^2\)
- Command sequencer to offload the CPU from programming and controlling the blit and drawing engines

Advantages:
- Renders graphics directly to display (on-the-fly). This enables the internal video RAM to become sufficient for 720p graphics and saves BOM cost because the system does not require external DDR RAM

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\(^1\) Raster graphics: Raster graphics draws bitmap images, supports scaling and transformation.
\(^2\) Vector graphics: Vector graphics draws lines and curves, typically used for outline font rendering.
Features:
- 250-MHz core clock, 750 Mpixels/s peak rate
- Image size up to 1600 x 720 pixels
- Standard blit operations
- Image scaling and rotation by any angle
- Perspective correction for 3D effect (2.5D)
- Compressed source images (lossless or lossy)
- Vector drawing accelerator (Bezier curve\(^1\) rasterization)
- Command sequencer to minimize CPU interaction
- Render on-the-fly to display (except vector drawing)

\(^1\) Bezier curve: Bezier curve is a parametric curve, draws a smoothing curve with one control point.
Video I/O (1/2)

› Video I/O includes:
  - Capture Engine: control logic for video input
  - Display Engine: control logic for output interfaces
  - Composition Engine: image processing functions, such as display scene composition by layer blending

› Capture Engine Features:
  - 220-MHz pixel clock, 2880 x 1080 active pixels, RGB/YUV format
  - Frame rate conversion via ring buffer in video RAM
  - Downscaling (only if display does not upscale)
  - Feed-through (direct capture) on-the-fly to display with graphics overlay
Video I/O (2/2)

- **Display and Composition Engine Features:**
  - Two independent video output stream (such as cluster and HUD\(^1\))
  - 220 MHz pixel clock, 2880 x 1080 active pixels, RGB format
  - Five transparent layers in total (alpha blending)
  - 26 windows in total (individual setup and frame buffers)
  - Four independent layer composition streams
  - One layer can be warped on-the-fly (HUD)
  - One layer can be upscaled on-the-fly
  - Gamma correction\(^2\) and dithering\(^3\)
  - CRC\(^4\) check on eight regions per display

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\(^1\) HUD: Head-Up Display
\(^2\) Gamma correction: Gamma correction is a nonlinear operation, typically used for brightness and contrast control.
\(^3\) Dithering: Dithering increases the physical color resolution of a display from 5, 6, 7 or 8 bits per RGB channel to a virtual resolution of 10 bits.
\(^4\) CRC: Cyclic Redundancy Check
Video RAM (VRAM)

- VRAM enables simultaneous access to a shared VRAM address space through AXI slave interfaces
- VRAM maps and interleaves AXI accesses to eight logical VRAM banks
- A port with a higher priority is always arbitrated first. Ports with the same priority will be round-robin arbitrated
CSI-2 and D-PHY

› CSI-2 controller and D-PHY\(^1\) capture image information from a camera via a MIPI standard CSI-2 type interface
  - CSI-2 controller
    - Provides a flexible, high-performance, easy-to-use MIPI Camera Serial Interface 2 (CSI-2) controller
    - Supports a packet-based protocol to interface with mobile cameras
  - D-PHY
    - High-frequency, low-power, source-synchronous physical layer that supports the MIPI Alliance Standard for D-PHY
    - Supports up to four data lanes running at a maximum data rate of 1.5 Gbps per lane giving a maximum aggregate throughput of 6 Gbps

› Use case
  - Rear camera
  - Parking assist camera

\(^1\) D-PHY: Physical layer for high-performance, cost-optimized cameras and displays

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FPD-link

- FPD-Link interface is a 7:1 serializer
- Transports uncompressed digital video across four or five LVDS1 links
- Converts the wide parallel bus into multiple high-speed serial streams, carried on differential links between the display controller and the display
- Each serial lane transports 7 bits of video and control data per cycle of the LVDS clock (TXCLK) signal

1 LVDS: Low Voltage Differential Signaling
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<tbody>
<tr>
<td>**</td>
<td>6638974</td>
<td>2019-07-29</td>
<td>Initial release</td>
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<tr>
<td>*A</td>
<td>7020960</td>
<td>2020-10-20</td>
<td>Updated slides 2, 5.</td>
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