

Customer Training Workshop

Traveo™ II Flash

Q4 2020



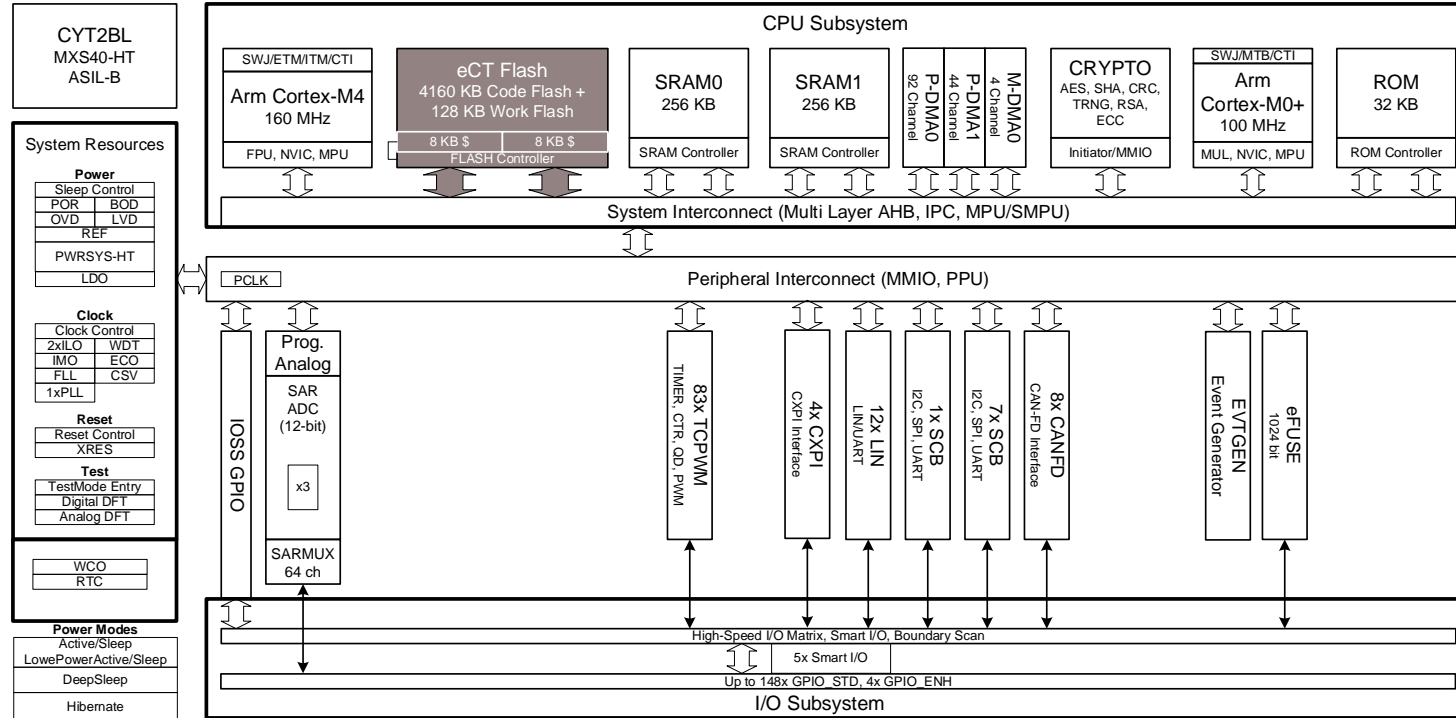
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160KB
Traveo II Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Body Controller Entry

Flash is part of the CPU subsystem

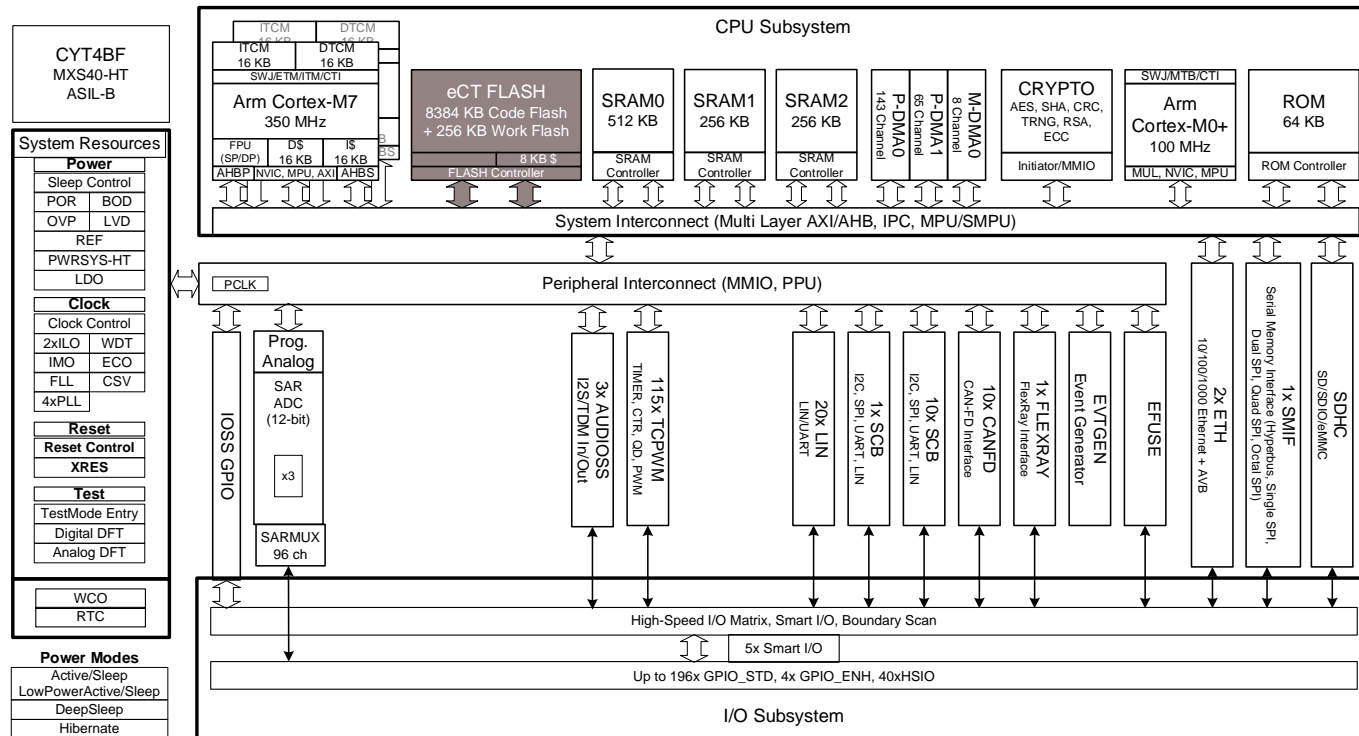


Hint Bar

Review TRM chapters 8 and 9 for additional details

Introduction to Traveo II Body Controller High

Flash is part of the CPU subsystem

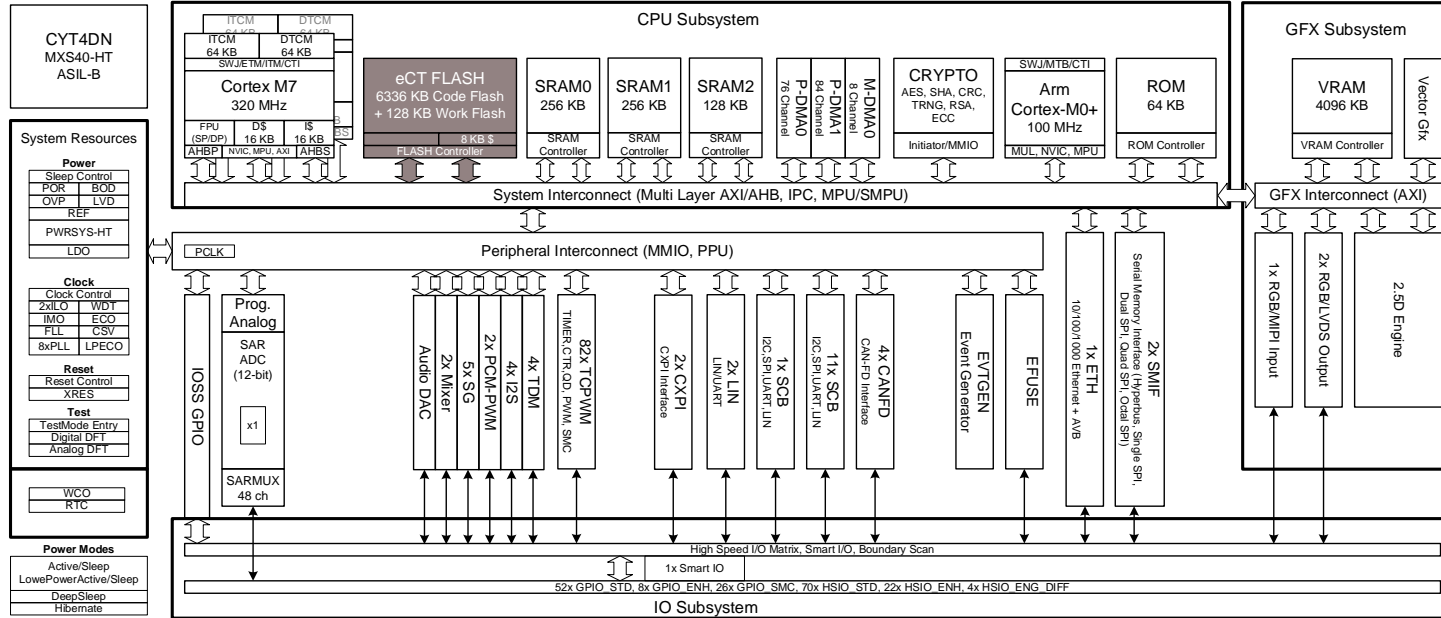


Hint Bar

Review TRM chapters 8 and 9 for additional details

Introduction to Traveo II Cluster

Flash is part of the CPU subsystem



Hint Bar

Review TRM chapters 8 and 9 for additional details

Flash Overview

- › Traveo™ II has Code Flash and Work Flash
 - Code flash is for storing application code
 - Work flash is for storing data or critical parameters
- › Cache
 - CYT2B6/B7/B9/BL
 - 8KB cache for CM0+ and CM4, located in the flash controller
 - Read-only capacity with an LRU replacement scheme
 - CYT3BB/4BB/4BF/3DL/4DN
 - CM0+: 8KB cache in flash; read-only capacity with an LRU replacement scheme
 - CM7: CPU has its own caches (16KB I-cache/16KB D-cache)
- › Flash Wait States
 - CYT2B6/B7/B9/BL
 - 0 wait cycle for $\text{CLK_HF1} \leq 100 \text{ MHz}$
 - 1 wait cycle for $100 \text{ MHz} < \text{CLK_HF} \leq 160 \text{ MHz}$
 - CYT3BB/4BB/4BF/3DL/4DN
 - 0 wait cycle for $\text{CLK_MEM2} \leq 100 \text{ MHz}$
 - 1 wait cycle for $100 \text{ MHz} < \text{CLK_MEM} \leq 200 \text{ MHz}$

Hint Bar

Review TRM chapters 8 and 9 for additional details

¹ High-frequency clock

² Memory clock. This clock is a divided version of CLK_HF.

Flash Overview

Feature	Code Flash			Work Flash		
	CYT2B6/B7/B9/ BL	CYT3BB/4BB/ 4BF	CYT3DL/4DN	CYT2B6/B7/B9/ BL	CYT3BB/4BB/ 4BF	CYT3DL/4DN
Memory Size	Up to 4160KB (4032KB + 128KB)	Up to 8384KB (8128KB + 256KB)	Up to 6336KB (6080KB + 256KB)	Up to 128KB (96KB + 32KB)	Up to 256KB (192KB + 64KB)	Up to 128KB (96KB + 32KB)
Program Size	64-bit, 256-bit, 4096-bit			32-bit		
ECC Function	64-bit + 8-bit Single-Error Correction/Double-Error Detection (SECEDED)			32-bit + 7-bit Single-Error Correction/Double-Error Detection (SECEDED)		
Erase Sector Size	32KB for large sector and 8KB for small sector			2KB for large sector and 128 bytes for small sector		
Security	Supported			Supported		
Single Bank and Dual Bank Modes	Supported			Supported		
Reading While Programming/Erasing	Supported			Supported		
Program/Erase cycles/ Data Retention Time @ 85 °C	1,000/20 years			250,000/10 years		

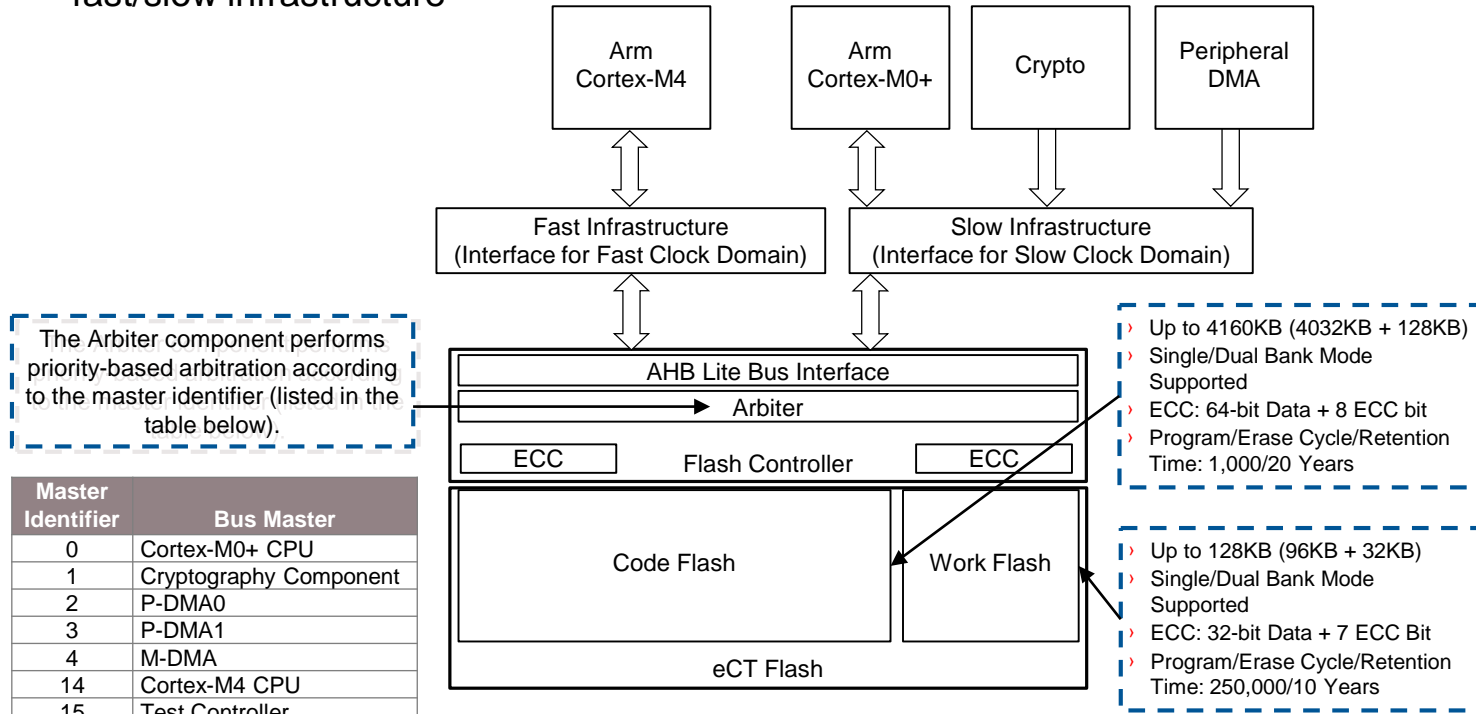
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Review TRM chapters 8 and 9 Flash for additional details

Review the Device Security section for additional details on security

Block Diagram for CYT2B6/B7/B9/BL

- › Arm® Cortex®-M4 and Cortex-M0+ core can access code flash and work flash via fast/slow infrastructure



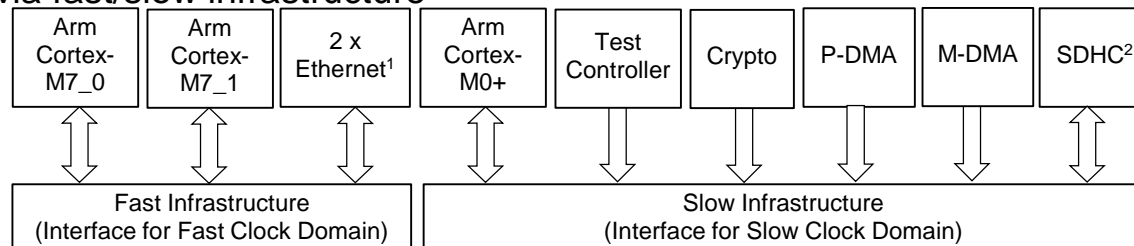
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Review TRM chapters 8 and 9 for additional details

*This figure is an example of some blocks only. Refer to the TRM for details.

Block Diagram for CYT3BB/4BB/4BF/3DL/4DN

- Arm® Cortex®-M7_0, Cortex-M7_1, and Cortex-M0+ cores can access code flash and work flash via fast/slow infrastructure



Hint Bar

Review TRM chapters 8 and 9 for additional details

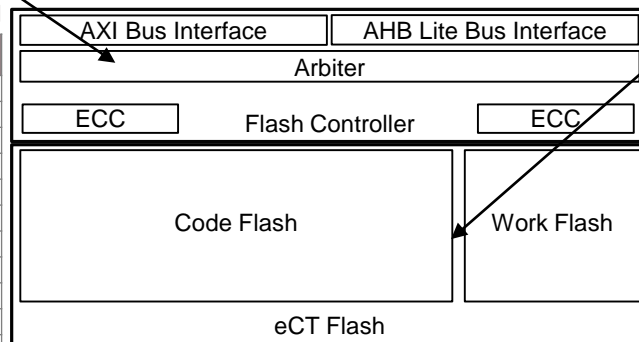
The Arbiter component performs priority-based arbitration according to the master identifier (listed in the table below)

Master Identifier	Bus Master
0	Cortex-M0+ CPU
1	Cryptography Component
2	P-DMA0
3	P-DMA1
4	M-DMA
5	SDHC ²
9	Ethernet 0 ¹
10	Ethernet 1 ¹
13	Cortex-M7_1 CPU ³
14	Cortex-M7_0 CPU
15	Test Controller

¹ CCYT4BF: 2ch, CYT4DN: 1ch (Ethernet 0 only)

² CYT4BF only

³ CYT4BB/4BF/4DN

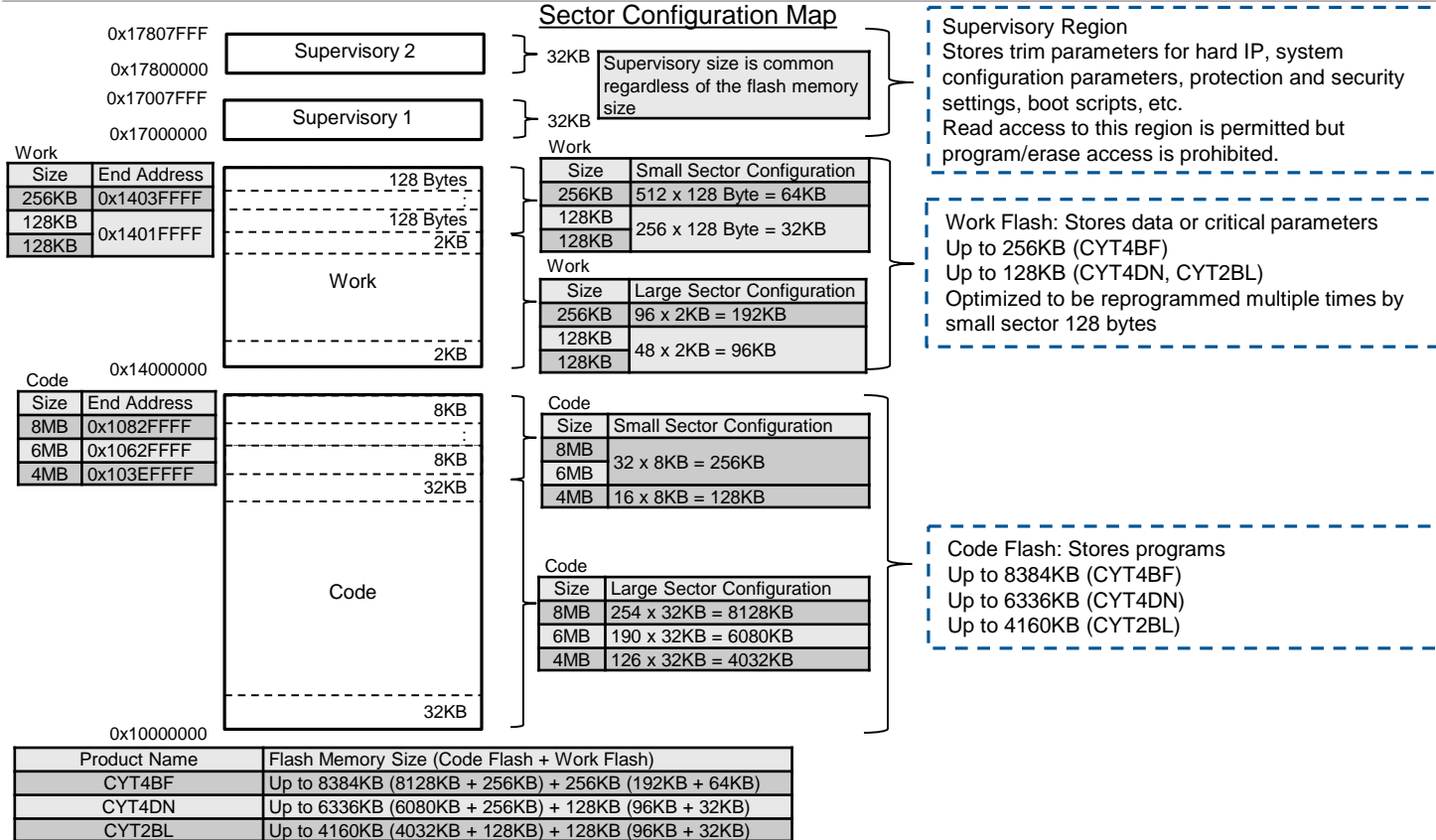


*This figure is an example of some blocks only. Refer to the TRM for details.

- CYT4BF: Up to 8384KB (8128KB + 256KB),
- Single/Dual Bank Mode Supported
- ECC: 64-bit Data + 8 ECC bit
- Program/Erase Cycle/Retention Time: 1,000/20 Years

- CYT4BF: Up to 256KB (192KB + 64KB)
- Single/Dual Bank Mode Supported
- ECC: 32-bit Data + 7 ECC bit
- Program/Erase Cycle/Retention Time: 250,000/10 Years

Sector Configuration



Supervisory Region
 Stores trim parameters for hard IP, system configuration parameters, protection and security settings, boot scripts, etc.
 Read access to this region is permitted but program/erase access is prohibited.

Work Flash: Stores data or critical parameters
 Up to 256KB (CYT4BF)
 Up to 128KB (CYT4DN, CYT2BL)
 Optimized to be reprogrammed multiple times by small sector 128 bytes

Code Flash: Stores programs
 Up to 8384KB (CYT4BF)
 Up to 6336KB (CYT4DN)
 Up to 4160KB (CYT2BL)

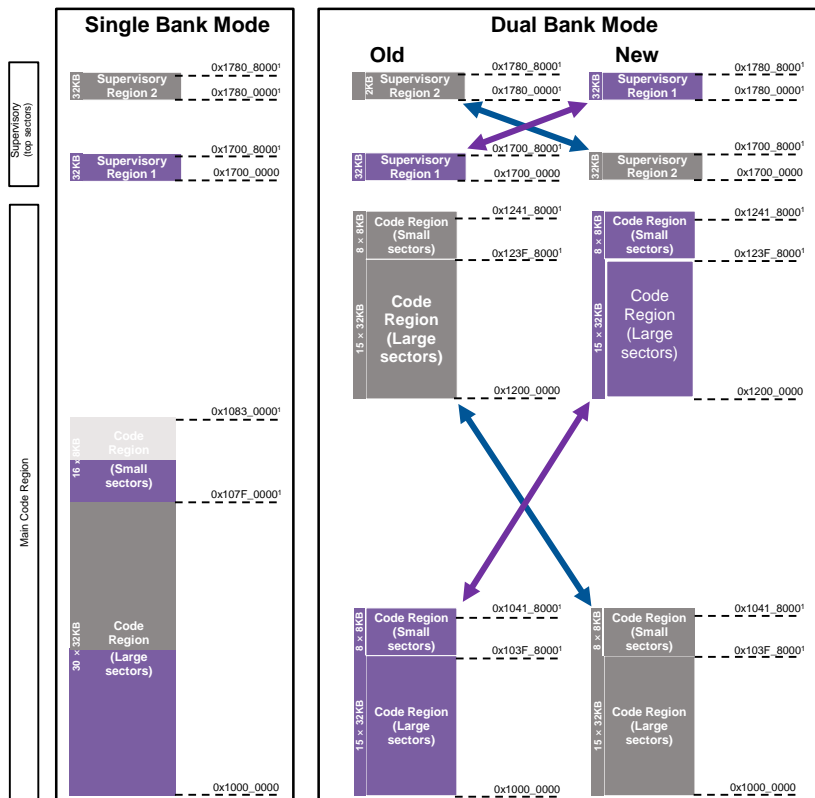
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Review TRM chapters 8 and 9 for additional details

Example of 8MB/6MB/4MB. For other products, refer to the respective TRMs.

Bank Modes

Representative Product: CYT4BF (8MB Code Flash)



- › Single Bank mode: Entire code and supervisory logical regions are mapped as single contiguous address regions
- › Dual Bank mode: Split into two halves, and each half is presented as a separate address region. Can be swapped to support same-location firmware upgrades
 - Old: CPU executes from a current software (Violet region) while the higher sectors are programmed with a new software image (Blue region)
 - New: When the CPU reboots, the user code changes the main map field, such that the CPU is executed from the new Blue region
- › Dual Bank mode enables writing to the other bank while executing flash
- › Work flash and code flash both support Dual Bank mode
- › Mapping of work flash is independent of mapping of code flash

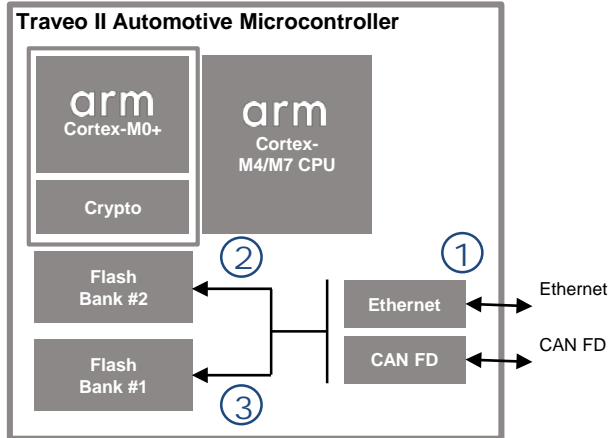
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Review TRM chapters 8 and 9 for additional details

¹ Example of 8MB. The end address is different for other code flash memory sizes. For details, refer to the TRM.

Remap Functionality

- › Software can control the remap functionality, which enables writing during flash execution in both bank modes
 - The higher and lower physical banks are swapped in the main flash region
- › Use Case
 - FOTA¹: The CPU executes from a current software image in the lower bank while the higher bank is programmed with a new software image. When the CPU reboots, the ROM boot code changes the REMAP field such that the CPU executed from the new image is on the higher bank



- ① Software update data is received via any communication interface
- ② Update data can be stored in the internal Flash Bank #2. The vehicle sends a command to switch to the new software version at the next ignition cycle. The new software version is activated
- ③ The previous version is still available in internal Flash Bank #1 and can be reused as a roll-back solution

Hint Bar

Review TRM chapters 8 and 9 for additional details

¹ Firmware-Over-The-Air

Error-Correcting Code (ECC)

- › ECC implements Single-Error Correction/Double-Error Detection (SECDED)
 - Default setting of ECC checking for code flash and work flash interface is “Enable”
 - Behavior at Double-Error Detection
 - For CPU bus transfers, notify with bus error generation¹
 - For non-CPU bus transfers, notify with bus error generation
 - Code flash: 64-bit data + 8 ECC bits
 - Work flash: 32-bit data + 7 ECC bits
- › Fault report structure
 - Both correctable and non-correctable ECC errors are reported to the fault structure in the same way. All data correction and recovery are left to the ISR. There is no hardware support for writing corrected data back to flash
 - Use Case
 - SEC Report: Log the error counts
 - DED Report: Report to NMI
- › Error injection
 - It is possible to generate ECC error by providing an error injection address and error injection data register
 - Use Case
 - As initial diagnosis of ECC before running the application
 - To test the error recovery routines

Hint Bar

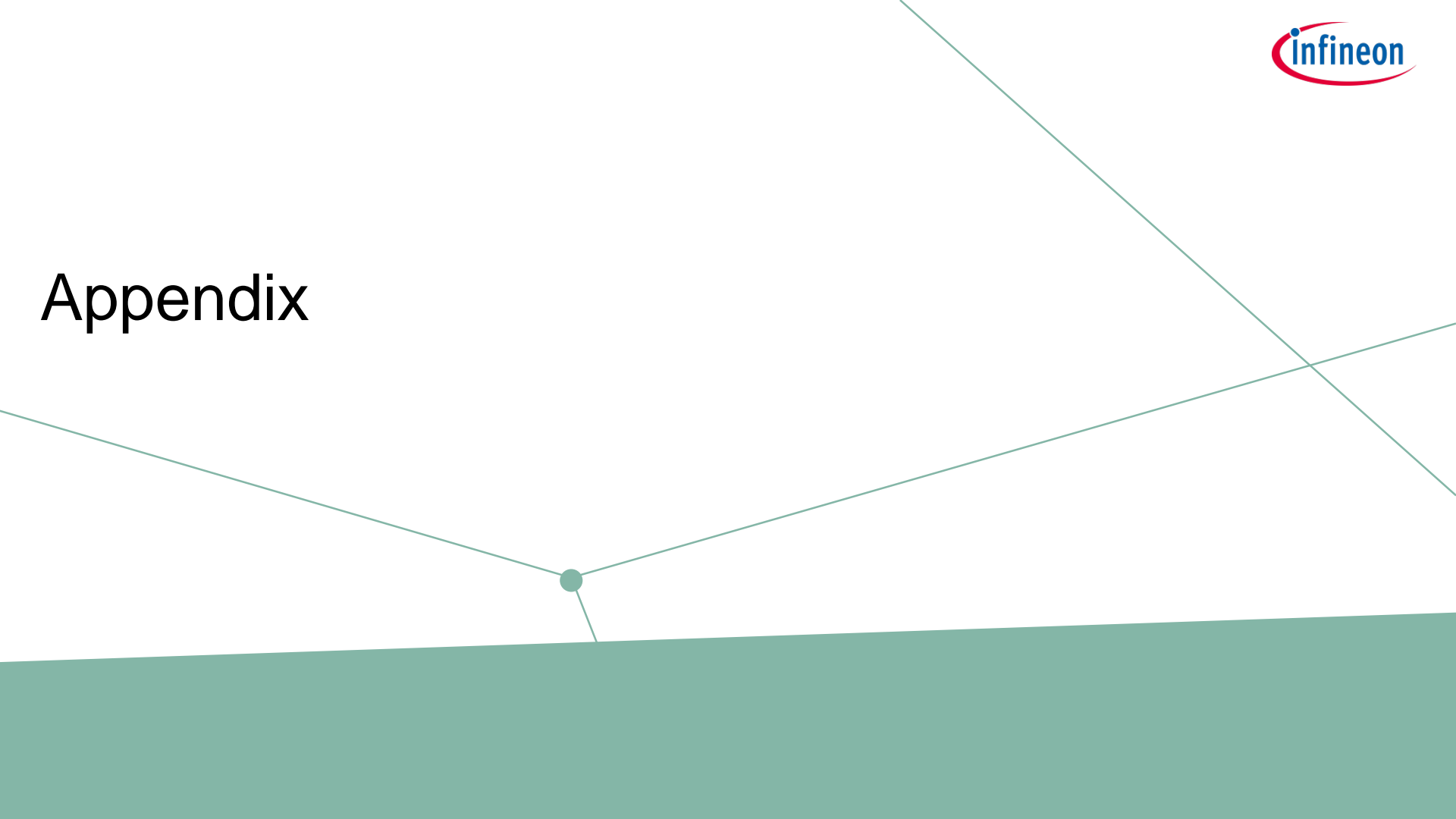
Review TRM chapters 8, 9, and 15 for additional details

Interrupt service routine (ISR)

Nonmaskable interrupt (NMI)

¹ It depends on FLASH_CTL register, MAIN_ERR_SILENT bit

Appendix



Comparison between CYT2BL, CYT4BF, and CYT4DN

Features	CYT2BL	CYT4BF	CYT4DN
Code flash memory size	4160KB (4032KB + 128KB)	8384KB (8128KB + 256KB)	6336KB (6080KB + 256KB)
Work flash memory size	128KB (96KB + 32KB)	256KB (192KB + 64KB)	128KB (96KB + 32KB)
Bus interface	AHB-Lite	AXI, AHB-Lite	
Cache	CM0+ and CM4 inside Flash	CM0+: Cache inside Flash CM7: CPU has own caches (I-Cache, D-Cache)	
Flash wait states	0 wait cycle for CLK_HF ≤ 100 MHz 1 wait cycle for 100 MHz < CLK_HF ≤ 160 MHz	0 wait cycle for CLK_MEM ≤ 100 MHz 1 wait cycle for 100 MHz < CLK_MEM ≤ 200 MHz	
Bus master priority of arbiter	0: Cortex-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 14: Cortex-M4 CPU 15: Test Controller	0: Cortex-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 5: SDHC 9: Ethernet 0 10: Ethernet 1 13: Cortex-M7_1 CPU 14: Cortex-M7_0 CPU 15: Test Controller	0: Cortex-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 9: Ethernet 0 13: Cortex-M7_1 CPU 14: Cortex-M7_0 CPU 15: Test Controller
ECC (SEC/DED)	Code flash: 64-bit + 8-bit and Work flash: 32-bit + 7-bit		
Bank modes	Supported		
Reading while programming/erasing	Supported		
Security	Supported		
Program/Erase cycles/ Data Retention Time @ 85 °C	Code flash: 1,000 cycles/20 years Work flash: 250,000 cycles/10 years		



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Revision History

Revision	ECN	Submission Data	Description of Change
**	6123648	09/03/2018	Initial release
*A	6402267	12/06/2018	<p>Added the note descriptions.</p> <p>Updated the Introduction for CYT2B5/B7, added the Introduction for CYT2B9 and CYT4BF.</p> <p>Added Block Diagram for CYT4BF of slide 10.</p> <p>Added Comparison between CYT2B7 and CYT4BF of slide 16.</p> <p>Fixed the title from Traveo™ Flash to Traveo™ II Flash.</p>
*B	6662240	08/27/2019	<p>Removed Erase and Program time.</p> <p>Removed CYT2B5.</p> <p>Added CYT4DN (page 2, 5, 6, 7, 9, 10, 15).</p>
*C	7051755	12/21/2020	Updated page 2, 3, 6, 7, 8, 9, 10