### Target Products

#### Target product list for this training material

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Body Controller Entry

Flash is part of the CPU subsystem

**CPU Subsystem**

- **Arm Cortex-M4**
  - 180 MHz
- eCT Flash
  - 4160 KB Code Flash + 126 KB Work Flash
- SRAM0
  - 256 KB
- SRAM1
  - 256 KB
- Arm Cortex-M0+
  - 100 MHz
- ROM
  - 32 KB

**System Interconnect**

- Multi Layer AHB, IPC, MPU/SMPU

**Peripheral Interconnect (MMIO, PPU)**

- Peripheral Interconnect
- System Resources
- Power
- Clock
- Reset
- Test
- Power Modes

**System Resources**

- Power
- Clock
- Reset
- Test
- Power Modes

**IO Subsystem**

- UP to 148x GPIO_STD, 4x GPIO_ENH
- 5x Smart I/O
- High-Speed I/O Matrix, Smart I/O, Boundary Scan

**Digital DFT**

- Test
- Analog

**Analog**

- SAR
  - ADC (12-bit)
- SARMUX
  - 64 ch
- SWJ/ETM/ITM/CTI

**Clock**

- Test
- Clock
- Power
- Reset

**Power Modes**

- Active/Deep
- Sleep/LowPower

---

Hint Bar

Review TRM chapters 8 and 9 for additional details

002-22195 °C 2020-12-21
Introduction to Traveo II Body Controller High

Flash is part of the CPU subsystem

Review TRM chapters 8 and 9 for additional details
Introduction to Traveo II Cluster

Flash is part of the CPU subsystem

**CPU Subsystem**
- Cortex M7 320 MHz
- eCT FLASH 6336 KB Code Flash + 128 KB Work Flash
- SRAM0 256 KB
- SRAM1 256 KB
- SRAM2 128 KB
- NPROM
- EEPROM
- Crypto AES, SHA, CRC
- TRNG, RSA, ECC
- Cortex-M0+ 100 MHz

**GFX Subsystem**
- ROM 64 KB
- VRAM 4096 KB

**System Resources**
- Power
- Clock
- Reset
- Test

**Peripheral Interconnect (MMIO, PPU)**

**IO Subsystem**
- 52x GPIO_STD, 8x GPIO_ENH, 26x GPIO_SMC
- 70x HSIO_STD, 22x HSIO_ENH, 4x HSIO_ENG_DIFF

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**GFX Subsystem**
- 2x SMIF

**GFX Interconnect (AXI)**

**FPU**
- Arm Cortex-M0+
- 100 MHz

**FIQ**
- Cortex-M0+
- 100 MHz

**SRAM**
- 0.56 MB
- 0.25 MB

**ROM Controller**
- 64 KB

**M-DMA0**
- 8 Channel

**M-DMA1**
- 84 Channel

**P-DMA0**
- 76 Channel

**P-DMA1**
- 76 Channel

**ROM Controller**
- 64 KB

**2x SMIF**

**Event Generator**
- EVTGEN

**Event Generator**
- Event Generator

**ROM Controller**
- ROM Controller

**ROM Controller**
- ROM Controller

**GFX Subsystem**
- VRAM 4096 KB

**GFX Interconnect (AXI)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM

**IOSS GPIO**

**Peripheral Interconnect (MMIO, PPU)**
- 2x PCIe
- 1x PCIe
- 4x USB
- 2x HDMI
- 2x HDMI
- 2x SATA
- 2x SATA
- 2x USB
- 2x USB

**Digital DFT**
- Test

**Analog DFT**
- Test

**System Resources**
- Power
- Reset
- Clock
- Clock Control

**Power Modes**
- Active/Deep Sleep
- LPM/Low/Power Active/Deep Sleep
- CRM
- Deep CRM
Flash Overview

› Traveo™ II has Code Flash and Work Flash
  - Code flash is for storing application code
  - Work flash is for storing data or critical parameters

› Cache
  - CYT2B6/B7/B9/BL
    - 8KB cache for CM0+ and CM4, located in the flash controller
    - Read-only capacity with an LRU replacement scheme
  - CYT3BB/4BB/4BF/3DL/4DN
    - CM0+: 8KB cache in flash; read-only capacity with an LRU replacement scheme
    - CM7: CPU has its own caches (16KB I-cache/16KB D-cache)

› Flash Wait States
  - CYT2B6/B7/B9/BL
    - 0 wait cycle for CLK_HF1 ≤ 100 MHz
    - 1 wait cycle for 100 MHz < CLK_HF ≤ 160 MHz
  - CYT3BB/4BB/4BF/3DL/4DN
    - 0 wait cycle for CLK_MEM2 ≤ 100 MHz
    - 1 wait cycle for 100 MHz < CLK_MEM ≤ 200 MHz

1 High-frequency clock
2 Memory clock. This clock is a divided version of CLK_HF.
## Flash Overview

<table>
<thead>
<tr>
<th>Feature</th>
<th>Code Flash</th>
<th>Work Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CYT3BB/4BB/4BF</td>
<td>CYT3BB/4BB/4BF</td>
</tr>
<tr>
<td></td>
<td>CYT3DL/4DN</td>
<td>CYT3DL/4DN</td>
</tr>
<tr>
<td>Memory Size</td>
<td>Up to 4160KB (4032KB + 128KB)</td>
<td>Up to 128KB (96KB + 32KB)</td>
</tr>
<tr>
<td></td>
<td>Up to 8384KB (8128KB + 256KB)</td>
<td>Up to 256KB (192KB + 64KB)</td>
</tr>
<tr>
<td></td>
<td>Up to 6336KB (6080KB + 256KB)</td>
<td>Up to 128KB (96KB + 32KB)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Program Size</td>
<td>64-bit, 256-bit, 4096-bit</td>
<td>32-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ECC Function</td>
<td>64-bit + 8-bit</td>
<td>32-bit + 7-bit</td>
</tr>
<tr>
<td></td>
<td>(SECDED)</td>
<td>(SECDED)</td>
</tr>
<tr>
<td>Erase Sector Size</td>
<td>32KB for large sector and 8KB for small sector</td>
<td>2KB for large sector and 128 bytes for small sector</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Security</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>Single Bank and Dual Bank Modes</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>Reading While Programming/Erasing</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>Program/Erase cycles/ Data Retention Time @ 85 °C</td>
<td>1,000/20 years</td>
<td>250,000/10 years</td>
</tr>
</tbody>
</table>

### Hint Bar

- **Review TRM chapters 8 and 9 Flash for additional details**
- **Review the Device Security section for additional details on security**
Arm® Cortex®-M4 and Cortex-M0+ core can access code flash and work flash via fast/slow infrastructure.

- Up to 4160KB (4032KB + 128KB)
- Single/Dual Bank Mode Supported
- ECC: 64-bit Data + 8 ECC bit
- Program/Erase Cycle/Retention Time: 1,000/20 Years

- Up to 128KB (96KB + 32KB)
- Single/Dual Bank Mode Supported
- ECC: 32-bit Data + 7 ECC Bit
- Program/Erase Cycle/Retention Time: 250,000/10 Years

The Arbiter component performs priority-based arbitration according to the master identifier (listed in the table below).

<table>
<thead>
<tr>
<th>Master Identifier</th>
<th>Bus Master</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Cortex-M0+ CPU</td>
</tr>
<tr>
<td>1</td>
<td>Cryptography Component</td>
</tr>
<tr>
<td>2</td>
<td>P-DMA0</td>
</tr>
<tr>
<td>3</td>
<td>P-DMA1</td>
</tr>
<tr>
<td>4</td>
<td>M-DMA</td>
</tr>
<tr>
<td>14</td>
<td>Cortex-M4 CPU</td>
</tr>
<tr>
<td>15</td>
<td>Test Controller</td>
</tr>
</tbody>
</table>

This figure is an example of some blocks only. Refer to the TRM for details.
Arm® Cortex®-M7_0, Cortex-M7_1, and Cortex-M0+ cores can access code flash and work flash via fast/slow infrastructure.

- Arm Cortex-M7_0
- Arm Cortex-M7_1
- 2 x Ethernet
- Arm Cortex-M0+
- Test Controller
- Crypto
- P-DMA
- M-DMA
- SDHC

**Fast Infrastructure**
(Interface for Fast Clock Domain)

**Slow Infrastructure**
(Interface for Slow Clock Domain)

The Arbiter component performs priority-based arbitration according to the master identifier (listed in the table below).

<table>
<thead>
<tr>
<th>Master Identifier</th>
<th>Bus Master</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Cortex-M0+ CPU</td>
</tr>
<tr>
<td>1</td>
<td>Cryptography Component</td>
</tr>
<tr>
<td>2</td>
<td>P-DMA0</td>
</tr>
<tr>
<td>3</td>
<td>P-DMA1</td>
</tr>
<tr>
<td>4</td>
<td>M-DMA</td>
</tr>
<tr>
<td>5</td>
<td>SDHC2</td>
</tr>
<tr>
<td>9</td>
<td>Ethernet 0(^1)</td>
</tr>
<tr>
<td>10</td>
<td>Ethernet 1(^1)</td>
</tr>
<tr>
<td>13</td>
<td>Cortex-M7_1 CPU(^3)</td>
</tr>
<tr>
<td>14</td>
<td>Cortex-M7_0 CPU</td>
</tr>
<tr>
<td>15</td>
<td>Test Controller</td>
</tr>
</tbody>
</table>

\(^1\) CYT4BF: 2ch, CYT4DN: 1ch (Ethernet 0 only)
\(^2\) CYT4BF only
\(^3\) CYT4BF/4BF/4DN

**ECC**
- 64-bit Data + 8 ECC bit
- Program/Erase Cycle/Retention Time: 1,000/20 Years

- CYT4BF: Up to 8384KB (8128KB + 256KB), Single/Dual Bank Mode Supported
- ECC: 64-bit Data + 8 ECC bit
- Program/Erase Cycle/Retention Time: 1,000/20 Years

- CYT4BF: Up to 256KB (192KB + 64KB), Single/Dual Bank Mode Supported
- ECC: 32-bit Data + 7 ECC bit
- Program/Erase Cycle/Retention Time: 250,000/10 Years

*This figure is an example of some blocks only. Refer to the TRM for details.*
Sector Configuration

Supervisory Region
Stores trim parameters for hard IP, system configuration parameters, protection and security settings, boot scripts, etc.
Read access to this region is permitted but program/erase access is prohibited.

Code Flash: Stores programs
Up to 8384KB (CYT4BF)
Up to 6336KB (CYT4DN)
Up to 4160KB (CYT2BL)

Work Flash: Stores data or critical parameters
Up to 256KB (CYT4BF)
Up to 128KB (CYT4DN, CYT2BL)
Optimized to be reprogrammed multiple times by small sector 128 bytes

Sector Configuration Map

Supervisory size is common regardless of the flash memory size

<table>
<thead>
<tr>
<th>Code</th>
<th>Work</th>
<th>Size</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>8MB</td>
<td>0x1082FFFF</td>
<td>128KB</td>
<td>0x1082FFFF</td>
</tr>
<tr>
<td>6MB</td>
<td>0x1062FFFF</td>
<td>128KB</td>
<td>0x1062FFFF</td>
</tr>
<tr>
<td>4MB</td>
<td>0x103EFFFF</td>
<td>128KB</td>
<td>0x103EFFFF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code</th>
<th>Work</th>
<th>Size</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>8KB</td>
<td>0x1082FFFF</td>
<td>128 Bytes</td>
<td>0x1082FFFF</td>
</tr>
<tr>
<td>8KB</td>
<td>0x1062FFFF</td>
<td>128 Bytes</td>
<td>0x1062FFFF</td>
</tr>
<tr>
<td>32KB</td>
<td>0x103EFFFF</td>
<td>128 Bytes</td>
<td>0x103EFFFF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code</th>
<th>Code</th>
<th>Size</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>8KB</td>
<td>Supervisory 2</td>
<td>32KB</td>
<td>0x1082FFFF</td>
</tr>
<tr>
<td>8KB</td>
<td>Supervisory 1</td>
<td>32KB</td>
<td>0x10000000</td>
</tr>
</tbody>
</table>

Example of 8MB/6MB/4MB. For other products, refer to the respective TRMs.

Copyright © Infineon Technologies AG 2020. All rights reserved.
Bank Modes

Representative Product: CYT4BF (8MB Code Flash)

Single Bank Mode:
- Entire code and supervisory logical regions are mapped as single contiguous address regions.

Dual Bank Mode:
- Split into two halves, and each half is presented as a separate address region. Can be swapped to support same-location firmware upgrades.
  - Old: CPU executes from a current software (Violet region) while the higher sectors are programmed with a new software image (Blue region).
  - New: When the CPU reboots, the user code changes the main map field, such that the CPU is executed from the new Blue region.
- Dual Bank mode enables writing to the other bank while executing flash.
- Work flash and code flash both support Dual Bank mode.
- Mapping of work flash is independent of mapping of code flash.

1 Example of 8MB. The end address is different for other code flash memory sizes. For details, refer to the TRM.

Copyright © Infineon Technologies AG 2020. All rights reserved.
Remap Functionality

› Software can control the remap functionality, which enables writing during flash execution in both bank modes
  - The higher and lower physical banks are swapped in the main flash region
› Use Case
  - FOTA\(^1\): The CPU executes from a current software image in the lower bank while the higher bank is programmed with a new software image. When the CPU reboots, the ROM boot code changes the REMAP field such that the CPU executed from the new image is on the higher bank

**Traveo II Automotive Microcontroller**

1. Software update data is received via any communication interface
2. Update data can be stored in the internal Flash Bank #2. The vehicle sends a command to switch to the new software version at the next ignition cycle. The new software version is activated
3. The previous version is still available in internal Flash Bank #1 and can be reused as a roll-back solution

\(^1\) Firmware-Over-The-Air

---

**Hint Bar**

Review TRM chapters 8 and 9 for additional details
Error-Correcting Code (ECC)

- ECC implements Single-Error Correction/Double-Error Detection (SECDED)
  - Default setting of ECC checking for code flash and work flash interface is “Enable”
  - Behavior at Double-Error Detection
    - For CPU bus transfers, notify with bus error generation\(^1\)
    - For non-CPU bus transfers, notify with bus error generation
  - Code flash: 64-bit data + 8 ECC bits
  - Work flash: 32-bit data + 7 ECC bits

- Fault report structure
  - Both correctable and non-correctable ECC errors are reported to the fault structure in the same way. All data correction and recovery are left to the ISR. There is no hardware support for writing corrected data back to flash
  - Use Case
    - SEC Report: Log the error counts
    - DED Report: Report to NMI

- Error injection
  - It is possible to generate ECC error by providing an error injection address and error injection data register
  - Use Case
    - As initial diagnosis of ECC before running the application
    - To test the error recovery routines

\(^1\) It depends on FLASH_CTL register, MAIN_ERR_SILENT bit

Review TRM chapters 8, 9, and 15 for additional details

Interrupt service routine (ISR)

Nonmaskable interrupt (NMI)
Appendix
## Comparison between CYT2BL, CYT4BF, and CYT4DN

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2BL</th>
<th>CYT4BF</th>
<th>CYT4DN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code flash memory size</td>
<td>4160KB (4032KB + 128KB)</td>
<td>8384KB (8128KB + 256KB)</td>
<td>6336KB (6080KB + 256KB)</td>
</tr>
<tr>
<td>Work flash memory size</td>
<td>128KB (96KB + 32KB)</td>
<td>256KB (192KB + 64KB)</td>
<td>128KB (96KB + 32KB)</td>
</tr>
<tr>
<td>Bus interface</td>
<td>AHB-Lite</td>
<td>AXI, AHB-Lite</td>
<td></td>
</tr>
<tr>
<td>Cache</td>
<td>CM0+ and CM4 inside Flash</td>
<td>CM0+: Cache inside Flash</td>
<td></td>
</tr>
<tr>
<td>Flash wait states</td>
<td>0 wait cycle for CLK_HF ≤ 100 MHz</td>
<td>0 wait cycle for CLK_MEM ≤ 100 MHz</td>
<td>1 wait cycle for 100 MHz &lt; CLK_MEM ≤ 200 MHz</td>
</tr>
<tr>
<td>Bus master priority of arbiter</td>
<td>0: Cortex-M0+ CPU</td>
<td>0: Cortex-M0+ CPU</td>
<td>0: Cortex-M0+ CPU</td>
</tr>
<tr>
<td></td>
<td>1: Cryptography Component</td>
<td>1: Cryptography Component</td>
<td>1: Cryptography Component</td>
</tr>
<tr>
<td></td>
<td>2: P-DMA0</td>
<td>2: P-DMA0</td>
<td>2: P-DMA0</td>
</tr>
<tr>
<td></td>
<td>3: P-DMA1</td>
<td>3: P-DMA1</td>
<td>3: P-DMA1</td>
</tr>
<tr>
<td></td>
<td>4: M-DMA</td>
<td>4: M-DMA</td>
<td>4: M-DMA</td>
</tr>
<tr>
<td></td>
<td>5: SDHC</td>
<td>5: SDHC</td>
<td>5: SDHC</td>
</tr>
<tr>
<td></td>
<td>9: Ethernet 0</td>
<td>9: Ethernet 0</td>
<td>9: Ethernet 0</td>
</tr>
<tr>
<td></td>
<td>10: Ethernet 1</td>
<td>10: Ethernet 1</td>
<td>10: Ethernet 1</td>
</tr>
<tr>
<td></td>
<td>13: Cortex-M7_1 CPU</td>
<td>13: Cortex-M7_1 CPU</td>
<td>13: Cortex-M7_1 CPU</td>
</tr>
<tr>
<td></td>
<td>14: Cortex-M7_0 CPU</td>
<td>14: Cortex-M7_0 CPU</td>
<td>14: Cortex-M7_0 CPU</td>
</tr>
<tr>
<td></td>
<td>15: Test Controller</td>
<td>15: Test Controller</td>
<td>15: Test Controller</td>
</tr>
<tr>
<td>ECC (SEC/DED)</td>
<td>Code flash: 64-bit + 8-bit and Work flash: 32-bit + 7-bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank modes</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>Reading while programming/erasing</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>Security</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>Program/Erase cycles/</td>
<td>Code flash: 1,000 cycles/20 years</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Retention Time @ 85 °C</td>
<td>Work flash: 250,000 cycles/10 years</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Data</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>** **</td>
<td>6123648</td>
<td>09/03/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6402267</td>
<td>12/06/2018</td>
<td>Added the note descriptions. Updated the Introduction for CYT2B5/B7, added the Introduction for CYT2B9 and CYT4BF. Added Block Diagram for CYT4BF of slide 10. Added Comparison between CYT2B7 and CYT4BF of slide 16. Fixed the title from Traveo™ Flash to Traveo™ II Flash.</td>
</tr>
<tr>
<td>*B</td>
<td>6662240</td>
<td>08/27/2019</td>
<td>Removed Erase and Program time. Removed CYT2B5. Added CYT4DN (page 2, 5, 6, 7, 9, 10, 15).</td>
</tr>
<tr>
<td>*C</td>
<td>7051755</td>
<td>12/21/2020</td>
<td>Updated page 2, 3, 6, 7, 8, 9, 10</td>
</tr>
</tbody>
</table>