Customer Training Workshop

Traveo™ II Event Generator
## Target Products

Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
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<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT3BB/CYT4BB</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336 KB</td>
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Introduction to Traveo II Body Controller Entry

Event Generator (EVTGEN) is a part of Peripheral blocks

Event Generator (EVTGEN) is a part of Peripheral blocks

Review TRM chapter 28 for additional details
Introduction to Traveo II Body Controller High

Event Generator (EVTGEN) is a part of Peripheral blocks

Review TRM chapter 28 for additional details
Introduction to Traveo II Cluster

- Event Generator (EVTGEN) is a part of Peripheral blocks

Hint Bar

Review TRM chapter 28 for additional details
Event Generator (EVTGEN) Overview

› 32-bit counters, one each for DeepSleep and Active power modes
› Interval range:
  – 30 ns to 76 hours (Active mode)
  – 31 μs to 36 hours (DeepSleep mode)
› Generates interrupts or triggers

1 This interrupt can be used like a normal interval timer
2 This trigger activates ADC

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Counters

- **Active Counter**
  - Works on the divided CLK_REF_DIV\(^1\) (IMO\(^2\) or ECO\(^3\))
  - Restarts from 0 after overflow
  - Enables Read by software in Active mode
  - Not retained in DeepSleep power mode

- **DeepSleep Counter**
  - Works on the CLK_LF\(^4\) (ILO\(^5\) or WCO\(^6\))
  - Cannot be read by software in Active or DeepSleep mode

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1. Reference clock (IMO or ECO)
2. ECO: External crystal oscillator
3. IMO: Internal main oscillator
4. Low-frequency clock (IMO or ECO)
5. ILO: Internal low-speed oscillator
6. WCO: Watch crystal oscillator
Relation of Active and DeepSleep Counter

- Active and DeepSleep counter status with RATIO = 5 (CLK_REF_DIV is 5 times as fast as CLK_LF)
  - Active and DeepSleep counters are always in sync

On every CLK_REF_DIV cycle, the Active counter is incremented by '1'

On every CLK_LF cycle, the RATIO (CLK_REF_DIV/CLK_LF) value is added to the DeepSleep counter status

On the first CLK_LF cycle after a DeepSleep to Active power mode transition, the DeepSleep counter value is used to initialize the Active counter

On the first CLK_LF clock after a DeepSleep to Active power mode transition, the DeepSleep counter value is used to initialize the Active counter

The Active counter is NOT retained in DeepSleep power mode

Active Counter Status

DeepSleep Counter Status

CLK_REF_DIV Cycle #

CLK_LF Cycle #

Active

DeepSleep

Active
Comparators

Active Comparators
- 16 (maximum): COMP0 [31:0]
  - 30 ns (minimum); ECO: 33.33 MHz
  - 76 hours (minimum); ECO: 4 MHz/256
- Compares to Active counter
- Generates triggers and interrupts

DeepSleep Comparators
- 16 (maximum): COMP1 [31:0]
  - 31 μs (minimum); ILO: 32 kHz
  - 36 hours (maximum); ILO: 32 kHz
- Compares to DeepSleep counter
- Generates wakeup interrupt

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CLK_SYS
CLK_REF
Clark REF_DIV
Active Domain
Active Comparators

Event Generator

Active Interrupt
CPU Interrupt Controller

Active Counter

Interrupt Process

Trigger

16 Comparator Outputs

DeepSleep Domain

DeepSleep Comparators

Compare Value Thresholds

DeepSleep Counter

16 Comparator Outputs

Interrupt Process

DeepSleep Interrupt

Wakeup Interrupt Controller (WIC)

CPU Interrupt Controller

ADC
P-DMA

CLK_REF_DIV range is 1 to 256
Comparator Outputs

- **Interrupts**
  - An Active interrupt is generated when the Active counter is ≥ COMP0
    - Use Case: Periodic task management
  - DeepSleep interrupt occurs when the DeepSleep counter is ≥ COMP1
    - Use Case: Wake up from DeepSleep mode

- **Trigger**
  - Available only in Active power mode
  - Generated when the Active counter is ≥ COMP0
    - Use Case: Periodic task management

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**Hint Bar**

Review TRM section 28.2.5 for additional details

Review the Trigger Multiplexer training section for additional trigger details

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Cyclic Wakeup Operation by EVTGEN

- Enables periodic ADC sensing with low power
- Periodic wakeup from DeepSleep mode by using the DeepSleep comparator (using COMP1)
- After CM0+ or CM4/CM7 wakes up (in LP Active mode), EVTGEN can generate trigger for ADC (using COMP0)

- Use case
  - Cyclic touch detection on switch module ECU
  - Cyclic pressure sensing on seat ECU

Hint Bar

- Review TRM section 28.2.6 for additional details
- Review the Power Modes training section for additional low-power details
- Review the Trigger Multiplexer training section for additional trigger details
- Review the Cyclic Wakeup Sequence for Sensing by ADC section for additional cyclic wakeup sequence details
Cyclic Wakeup Sequence for Sensing by ADC

**Active Mode**
- EVTGEN Count With Active/DeepSleep Counter

**DeepSleep Mode**
- EVTGEN Count With DeepSleep Counter
- DeepSleep Counter = COMP1 (Interval Time for Sensing)

**LP Active Mode**
- EVTGEN Count With Active Counter
- Active Counter = COMP0 (Activates A/D Convertor)
- Conversion of up to Selected Number of Channels in Succession

Interrupt Generation (e.g., External or RTC Interrupt)
Reset Generation (e.g., External Reset)

CPU judges power mode with Range Comparison results

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# Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<tr>
<td>**</td>
<td>6140813</td>
<td>04/25/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6354961</td>
<td>10/18/2018</td>
<td>Added slides 2, 4, 5, and note descriptions in all slides. Updated slides 3, 9, 10, and 11.</td>
</tr>
<tr>
<td>*B</td>
<td>6599849</td>
<td>06/13/2019</td>
<td>Updated slides 2, 3, 4, 9 and 10. Added slide 5.</td>
</tr>
<tr>
<td>*D</td>
<td>7065149</td>
<td>01/07/2021</td>
<td>Updated slides 1, 2, 7, 10 and 13.</td>
</tr>
</tbody>
</table>