## Target Products

### Target product list for this training material

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336 KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Body Controller High

- Ethernet MAC is located in the peripheral blocks

CPU Subsystem

System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)

Peripheral Interconnect (MMIO, PPU)

I/O Subsystem

Hint Bar

Review TRM section 31 for additional details
Introduction to Traveo II Cluster

- Ethernet MAC is located in the peripheral blocks

**System Resources**

- Power
  - Sleep Control
  - DFF
  - PLL
  - LVDS
- Clock
  - Clock Control
  - FCT
  - HPLL
- Reset
  - Reset Control
  - WCPU
  - SRAM Off
  - A/D Off
- WCO
  - HIC

**Power Modes**

- Active/Deep
  - Low Power/Active/Deep
  - Sleep
  - Alternate

**CPU Subsystem**

- Arm Cortex M7
  - 320 MHz
- eCT FLASH
  - 6336 KB Code Flash
  - 128 KB Work Flash
- SRAM0
  - 256 KB
- SRAM1
  - 256 KB
- SRAM2
  - 128 KB

**System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)**

- Peripheral Interconnect (MMIO, PPU)
  - IOSS GPIO
  - PCLK

- CPU Subsystem

- System Resources

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  - Alternate

**GFX Subsystem**

- GFX Interconnect (AXI)

- GFX Subsystem

- CYT4DN
  - MXS40-HT
  - ASIL-B

- System Resources

- Power
  - Sleep Control
  - DFF
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- Peripheral Interconnect (MMIO, PPU)

- Peripheral Interconnect (MMIO, PPU)

- CYT4DN
  - MXS40-HT
  - ASIL-B

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**GFX Subsystem**

- GFX Interconnect (AXI)
Ethernet MAC Overview

Ethernet MAC\(^1\) module transmits and receives IEEE 802.3 frames with the PHY\(^2\) device

Review TRM section 31.1 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

\(^1\) MAC: Media Access Control
\(^2\) PHY: Physical layer
\(^3\) MII: Media Independent Interface
\(^4\) RMII: Reduced Media Independent Interface
\(^5\) GMII: Gigabit Media Independent Interface
\(^6\) RGMII: Reduced Gigabit Media Independent Interface
\(^7\) MDIO: Management Data Input/Output
Ethernet MAC Features

- MII, RMII, GMII, and RGMII PHY interface
- MDIO interface for PHY management
- 10/100/1000 Mbps Ethernet MAC compatible with IEEE 802.3
- Full-duplex
- Jumbo frame¹ (Max 1536 bytes)
- IEEE 802.1Q: Virtual LAN (VLAN)
- IEEE 802.3: Pause frame
- IEEE 802.1BA: Audio video bridging systems
- IEEE 802.1Qav: Forwarding and queuing enhancements for time-sensitive streams
- IEEE 802.1AS: Timing and synchronization for time-sensitive applications in bridged LANs
- IEEE 1588 – Precision time protocol

¹ Jumbo frame is not standardized by IEEE
Ethernet MAC Components

- MAC control
  - PHY interface
  - MAC transmitter/receiver
  - Time stamp unit
- TX/RX packet memory
- CLK control

![Ethernet MAC Components Diagram](image)

**Hint Bar**

Review TRM section 31.2 for additional details

Refer to the Features List in the datasheet for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device
PHY Interface

› Supports MII/RMII/GMII/RGMII PHY interface
› Supports MDIO interface

Review TRM section 31.3.14 for additional details. Review the device-specific datasheet to confirm which PHY interfaces are supported in the device.
### PHY Interface Types

- Supports the following interface types and transfer rates

<table>
<thead>
<tr>
<th>Interface Type</th>
<th>10 Mbps</th>
<th>100 Mbps</th>
<th>1000 Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>MII</td>
<td>✓</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>RMII</td>
<td>✓</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>GMII</td>
<td>-</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>RGMII</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

**Hint Bar**

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device
### MII/RMII/GMII/RGMII Interface

#### Supported signals: transmitter/receiver signals

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function of signals</th>
<th>MII</th>
<th>RMII</th>
<th>GMII</th>
<th>RGMII</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXD[1:0]</td>
<td>Transmit data [1:0]</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>TXD[3:2]</td>
<td>Transmit data [3:2]</td>
<td>✓</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>TXD[7:4]</td>
<td>Transmit data [7:4]</td>
<td>-</td>
<td>-</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>TX_CTL</td>
<td>Transmit enable</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>TX_ER</td>
<td>Transmit error</td>
<td>✓</td>
<td>-</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>TX_CLK</td>
<td>Transmit clock</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>RXD[1:0]</td>
<td>Receive data [1:0]</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>RXD[7:4]</td>
<td>Receive data [7:4]</td>
<td>-</td>
<td>-</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>RX_CTL</td>
<td>Receive data valid</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>RX_ER</td>
<td>Receive error</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>RX_CLK</td>
<td>Receive clock</td>
<td>✓</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>REF_CLK</td>
<td>Operation clock out</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Operation clock in</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
Use Case: MII/RMII Interface

**MII Interface**

- TXD[3:0]
- TX_CLK
- RXD[3:0]
- RX_CLK
- TX_EN
- TX_ER
- TX_CTL
- RX_DV
- RX_ER
- RX_CTL

**RMII Interface**

- TXD[3:0]
- RXD[3:0]
- TX_CLK
- RX_CLK
- TX_EN
- TX_ER
- TX_CTL
- RX_DV
- RX_ER
- RX_CTL

**Register info**

**ETH_CTRL** (REFCLK_SRC_SEL)

- TX and RX clock source can be supplied from either the internal reference clock or the external clock source
- ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO

**Hint Bar**

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

Register info

- ETH_CTRL (REFCLK_SRC_SEL)

TX and RX clocks are supplied from external PHY

25 MHz for 100 Mbit/s
2.5 MHz for 10 Mbit/s
TX clock source can be selected either from the internal clock source or from HSIO

ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO

Review TRM section 31.3.14 for additional details

Review the device-specific datasheet to confirm which PHY interfaces are supported in the device

Register info - ETH_CTRL (REFCLK_SRC_SEL)
## MDIO Interface

### Supported signals

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Direction</th>
<th>Function of signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDIO</td>
<td>I/O</td>
<td>Management Data Input/Output</td>
</tr>
<tr>
<td>MDC</td>
<td>O</td>
<td>Management Data Clock</td>
</tr>
</tbody>
</table>

- MDIO is a single bi-directional tristate signal between Ethernet MAC and PHY
- MDC is a clock for MDIO
  - MDC is generated by dividing CLK_GR4
  - MDC should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3az

### Use case

- ETH_phy_management register is implemented as a shift register
- Writing to this register starts a shift operation and outputs to the MDIO pin

<table>
<thead>
<tr>
<th></th>
<th>ST</th>
<th>OP</th>
<th>PHY Address</th>
<th>REG Address</th>
<th>TA</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDIO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MDC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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MAC Transmitter/Receiver, TSU, and Packet Buff

- **MAC Transmitter/Receiver and TX/RX Packet Buff**
  - Supports transfer of packets between Physical Layer and MAC Layer, and stores data in TX/RX packet buffer.

- **Time Stamp Unit (TSU)**
  - Generates a time stamp for the transmit data and checks the time stamp for the receive data.

---

**Diagram:**

- Ethernet MAC
  - AXI interface
  - AHB slave interface
  - TX Packet Buff (16KB)
  - RX Packet Buff (4KB)
  - MII/RMII/GMII/RGMII and MDIO
  - MAC Control
    - Time Stamp Unit (TSU)
    - MAC Transmitter
    - MAC Receiver
  - PHY Interface
  - MMIO Registers
  - Clock Control
    - clk_sys
    - clk_mem
    - clk_tsu
    - int_ref_clock

---

**Hint Bar:**

Review TRM sections 31.3.2 to 31.3.4 for additional details.
MAC Transmitter

Procedure

(1) IP Datagrams are transferred to the TX packet memory via AXI\(^1\)

\(^1\) Support to DMA transfer. DMAC is implemented in the MAC Control
MAC Transmitter

› Procedure

(1) IP Datagrams are transferred to the TX packet memory via AXI\(^1\)
(2) IP Datagram is transferred to the MAC Transceiver\(^1\)

\(^1\) Support to DMA transfer. DMAC is implemented in the MAC Control.
MAC Transmitter

Procedure

1. IP Datagrams are transferred to the TX packet memory via AXI
2. IP Datagram is transferred to the MAC Transceiver
3. MAC frame is multiplexed and transmitted by the hardware

---

1 Support to DMA transfer. DMAC is implemented in the MAC Control.
Procedure

(1) MAC frame is checked and demultiplexed by the hardware
MAC Receiver

Procedure

(1) MAC frame is checked and demultiplexed by the hardware
(2) IP Datagram is transferred to the RX packet memory

1 Support to DMA transfer. DMAC is implemented in the MAC Control.
**MAC Receiver**

### Procedure

1. MAC frame is checked and demultiplexed by the hardware
2. IP Datagram is transferred to the RX packet memory
3. IP Datagram is transferred to the internal memory via the AXI bus

---

### Diagram

- **Internet Layer**
  - IP Header, TCP Header, Application Data, Ethernet Header, IP Header, TCP Header, Application Data, Ethernet Trailer

- **Network Interface Layer**
  - Ethernet Header, IP Header, TCP Header, Application Data, Ethernet Trailer

---

1. Support to DMA transfer. DMAC is implemented in the MAC Control.

---

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MAC Frame

Frame format

- Basic Frame

<table>
<thead>
<tr>
<th>7-octet</th>
<th>1-octet</th>
<th>6-octet</th>
<th>6-octet</th>
<th>2-octet</th>
<th>46 to 1500-octet</th>
<th>4-octet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamble</td>
<td>S</td>
<td>F</td>
<td>D</td>
<td>DESTINATION ADDRESS</td>
<td>SOURCE ADDRESS</td>
<td>LENGTH/TYP</td>
</tr>
</tbody>
</table>

Notes:

SFD: Start of Frame Delimiter
FCS: Flag check sequence

- Q-tagged Frame

<table>
<thead>
<tr>
<th>7-octet</th>
<th>1-octet</th>
<th>6-octet</th>
<th>6-octet</th>
<th>4-octet</th>
<th>2-octet</th>
<th>42 to 1500-octet</th>
<th>4-octet</th>
</tr>
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<td>F</td>
<td>D</td>
<td>DESTINATION ADDRESS</td>
<td>SOURCE ADDRESS</td>
<td>Q Tag Prefix</td>
<td>MAC Client Data, Pad</td>
</tr>
</tbody>
</table>

MAC CLIENT LENGTH/TYP
Jumbo Frame Support

The maximum length of the Traveo II jumbo frame payload is 1536 bytes

<table>
<thead>
<tr>
<th>Preamble</th>
<th>S</th>
<th>F</th>
<th>D</th>
<th>Destination Address</th>
<th>Source Address</th>
<th>Q Tag Prefix</th>
<th>MAC Client Data, Pad</th>
<th>FCS</th>
</tr>
</thead>
</table>

MAC CLIENT LENGTH/TYPE
Set to the following register.
- ETH_jumbo_max_length register
VLAN Support

- Provides a virtual LAN group in the network by VLAN tag.
- VLAN tag is inserted into the Q-tagged frame.

VLAN Tag

- Set to the following register.
  - ETH_stacked_vlan

- Set to the following register.
  - ETH_screening_type_2_register_0 to 15

Register info
- ETH_network_config
- ETH_stacked_vlan
- ETH_dma_config
- ETH_screening_type_2_register_0 to 15

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Pause Frame Support

- Pause frame is used to prevent self-buffer overflow

<table>
<thead>
<tr>
<th>Field</th>
<th>Octets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-octet</td>
<td>Preamble</td>
</tr>
<tr>
<td>1-octet</td>
<td>S F D</td>
</tr>
<tr>
<td>6-octet</td>
<td>Destination Address</td>
</tr>
<tr>
<td>6-octet</td>
<td>Source Address</td>
</tr>
<tr>
<td>2-octet</td>
<td>Type</td>
</tr>
<tr>
<td>46-octet</td>
<td>MAC Client Data, Pad</td>
</tr>
<tr>
<td>4-octet</td>
<td>FCS</td>
</tr>
</tbody>
</table>

- Fix value
  - 01:80:C2:00:00:01

- Set to the following register.
  - ETH_pause_time

Hint Bar

Review the Register TRM for additional details

Register info
- ETH_network_config
- ETH_pause_time
Audio Video Bridging Systems Support

- Supports the timing and synchronization (IEEE 802.1AS)
- Supports the TSU\(^1\)
  - Ethernet MAC has a TSU compatible to IEEE 1588
- Supports the FQTSS\(^2\) (IEEE 802.1Qav)
  - Ethernet MAC has registers to support FQTSS
  - FQTSS is controlled by software using registers and supports priority control of transmission data

\(^1\) TSU: Time Stamp Unit
\(^2\) FQTSS: Forwarding and Queuing Enhancements for Time-Sensitive Streams
The following clocks are needed to execute the internal operation of Ethernet MAC:
- clk_sys
- clk_mem
- clk_tsu
- int_ref_clock

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Clock Sources

- Usage of each clock is listed here

<table>
<thead>
<tr>
<th>Clock</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk_sys</td>
<td>To generate MDC clock and for AHB operation</td>
</tr>
<tr>
<td></td>
<td>clk_sys is derived from CLK_PERI</td>
</tr>
<tr>
<td>clk_tsu</td>
<td>TSU clock for TSU timer</td>
</tr>
<tr>
<td>clk_mem</td>
<td>Fast clock for AXI operation</td>
</tr>
<tr>
<td>int_ref_clock</td>
<td>Internal reference clock supplied from PLL</td>
</tr>
</tbody>
</table>
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6399212</td>
<td>12/03/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6678084</td>
<td>09/19/2019</td>
<td>Updated page 2, 3, 5, 6, 8, 11 to 20, 21, 24, 26, 27 Added page 4</td>
</tr>
<tr>
<td>*B</td>
<td>6950716</td>
<td>08/17/2020</td>
<td>Updated MII and RMII Interface description on page 11.</td>
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<td>*C</td>
<td>7051240</td>
<td>12/22/2021</td>
<td>Updated revision to 0C from 0B Added the new products: page 2 Changed to new block diagram: page 3, 4 Updated TX_CLK assignment: page 10 Updated clock name and description: page 7, 8, 14 to 20, 26, 27 Updated Hint Bar: page 5 to 14, 26, 27</td>
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<td>*D</td>
<td>7082784</td>
<td>02/12/2021</td>
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