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CYTVII-B-H-8M-320-CPU

Evaluation Board User Guide

Document Number: 002-26716 Rev. *A

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Contents

Safety Information

Regulatory Compliance

This Evaluation Board is intended for use as a development platform for hardware in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. This may cause interference to other electrical or electronic devices in close proximity.

In a domestic environment, this product may cause radio interference. The user may then be required to take adequate prevention measures. Also, the board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

	This Evaluation Board contains electrostatic discharge (ESD) sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused this board in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to chassis ground (any unpainted metal surface) on your board when handling parts.

Handling Boards

This board is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide board over any surface.

1. Introduction

This user guide provides instructions to handle the CYTVII-B-H-8M-320-CPU and CYTVII-B-H-320-SO evaluation boards, collectively referred to as 'CPU board' in this document. This is an evaluation platform for the CYT4BFCC Traveo™ II device. The board can be used as a standalone board for basic validation or in combination with the CYTVII-B-E-BB Traveo II base board (available separately from Cypress). This document assumes that you will work with the combination (CPU board + base board), and provides guidance on how to use the features of the evaluation platform.

1.1 Precautions and Warnings

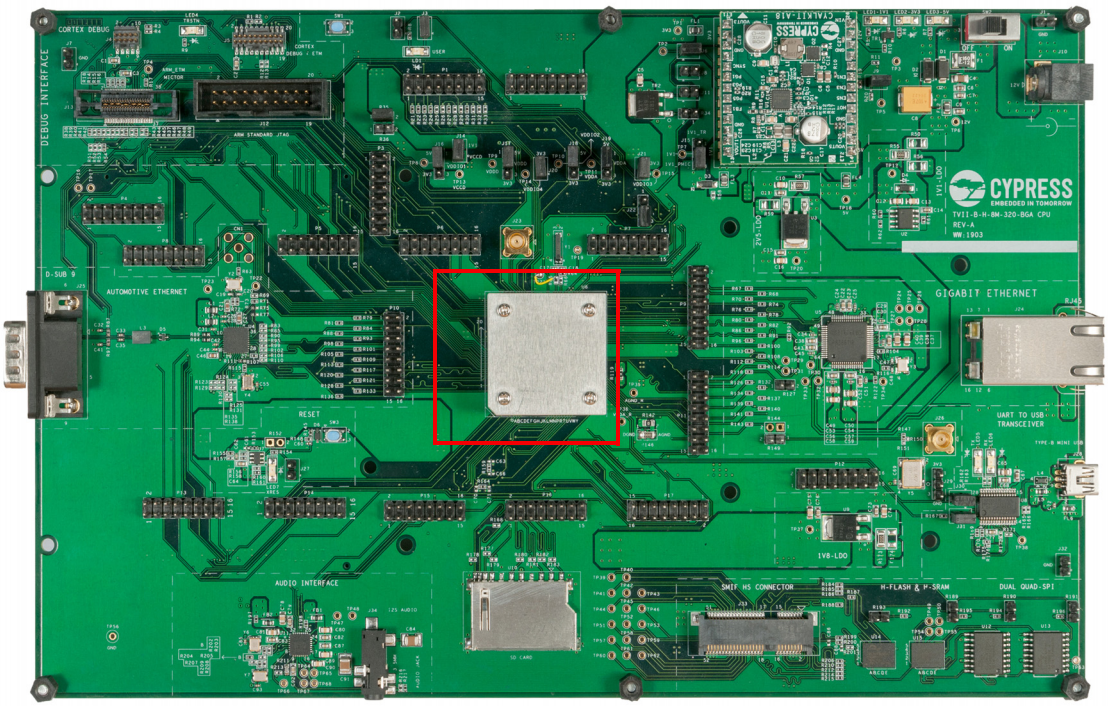
The board is a delicate PCB; make sure that the evaluation board is handled by qualified personnel who are aware of the capabilities of the board. Handle the board carefully and make sure it is not bent or subjected to stress. Ensure your own safety arising from electrical hazards and other sources.

The CPU board is shipped with a 12 V DC power adapter. This adapter can be plugged into the AC mains supply anywhere in the world and is designed to receive 100-240 V AC V @ 50/60 Hz. While powering the board, you must connect only the power adapter supplied with the evaluation board and not any other part.

2. Overview

Figure 2-1 shows the CYTVII-B-H-320-SO board. Insert a Traveo II device into the IC socket (highlighted in red) while the evaluation board is powered OFF.

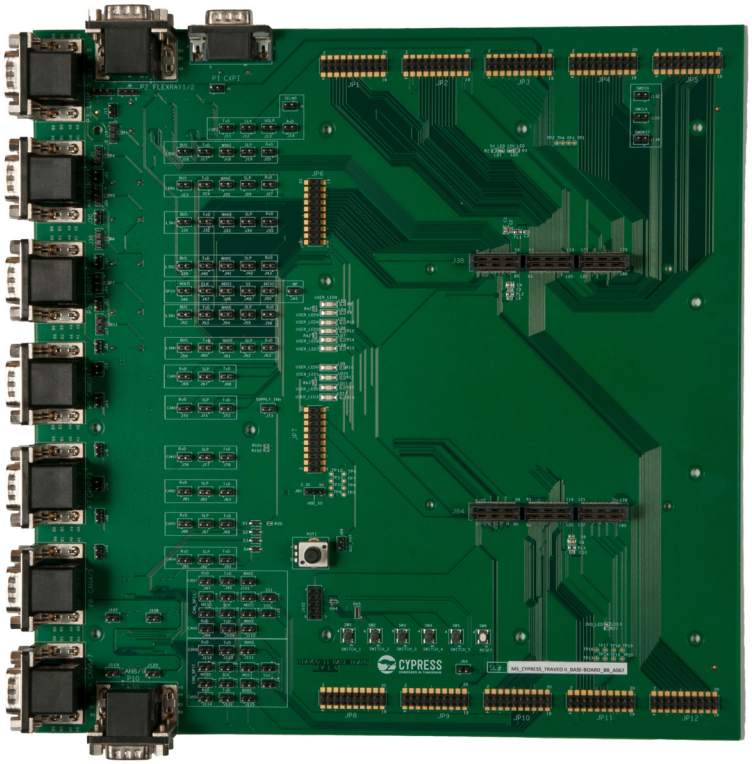
Figure 2-1. CYTVII-B-H-320-SO Board



A variant of the CPU board (CYTVII-B-H-8M-320-CPU) is also available, where the Traveo II device is soldered directly onto the PCB. Functionally, the CYTVII-B-H-8M-320-CPU and CYTVII-B-H-320-SO boards are identical, except that the device can be easily replaced in the latter.

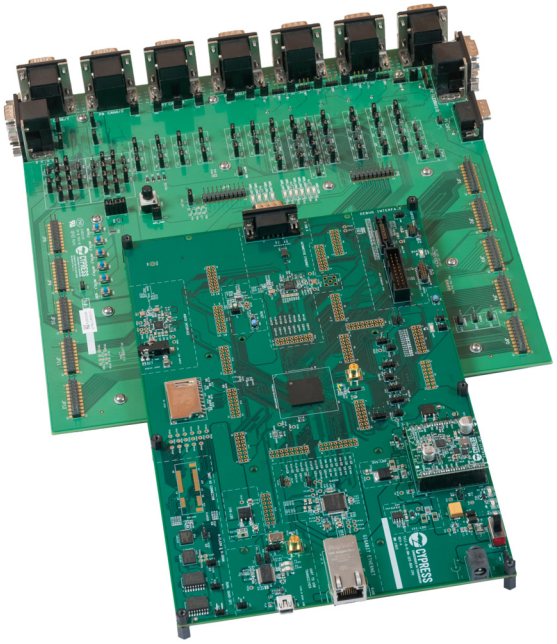
The CPU board is meant to be used along with a Traveo II base board (CYTVII-B-E-BB). The base board brings out all important interface connections such as CAN, LIN, SPI EEPROM, CXPI, and FlexRay, and can be used in conjunction with several CPU boards of the Traveo II family. Figure 2-2 shows the base board.

Figure 2-2. Traveo II Base Board (CYTVII-B-E-BB)



Two Samtec connectors on the CPU board and corresponding mating connectors on the base board are used to connect signals across the two boards. When put together, the boards appear as shown in Figure 2-3.

Figure 2-3. Combination of CPU Board and Traveo II Base Board



2.1 Functional Overview

The CPU board has the following components:

1. One Traveo II device, either soldered or mounted on a socket (U6).
2. PMIC to generate the 5-V, 3.3-V, and 1.1-V outputs, which power the CPU board and the base board (if connected).
3. Programming interface (Arm® Standard JTAG, Cortex® Debug, Cortex Debug + ETM and Arm ETM Mictor) to connect several programming tools such as IAR I-jet, Green Hills MULTI, also Cypress MiniProg.
4. USB-UART interface for terminal logging (J28).
5. One user switch (SW1) and one user LED (LD1) for standalone operation without the base board.
6. Reset controller with manual reset switch (SW3) and voltage supervision.
7. Measurement of device current on VCCD using jumper J14, VDDD using jumper J17, VDDIO_1 using jumper J16, VDDIO_2 using jumper J18, VDDIO_3 using jumper J21, VDDIO_4 using jumper J20, and VDDA using jumper J19 respectively.
8. Samtec connector interface (J35 and J36) for connecting to the base board CYTVII-B-E-BB.
9. Gigabit Ethernet Interface (J24).
10. Automotive Ethernet(J25)
11. I^2S Audio Codec (J34)
12. SD Card Connector (U10)
13. HyperFlash and HyperRAM (U15, U14)
14. Dual Quad SPI Flash (U13, U12)
15. 0.10-inch Through-Hole Test Points

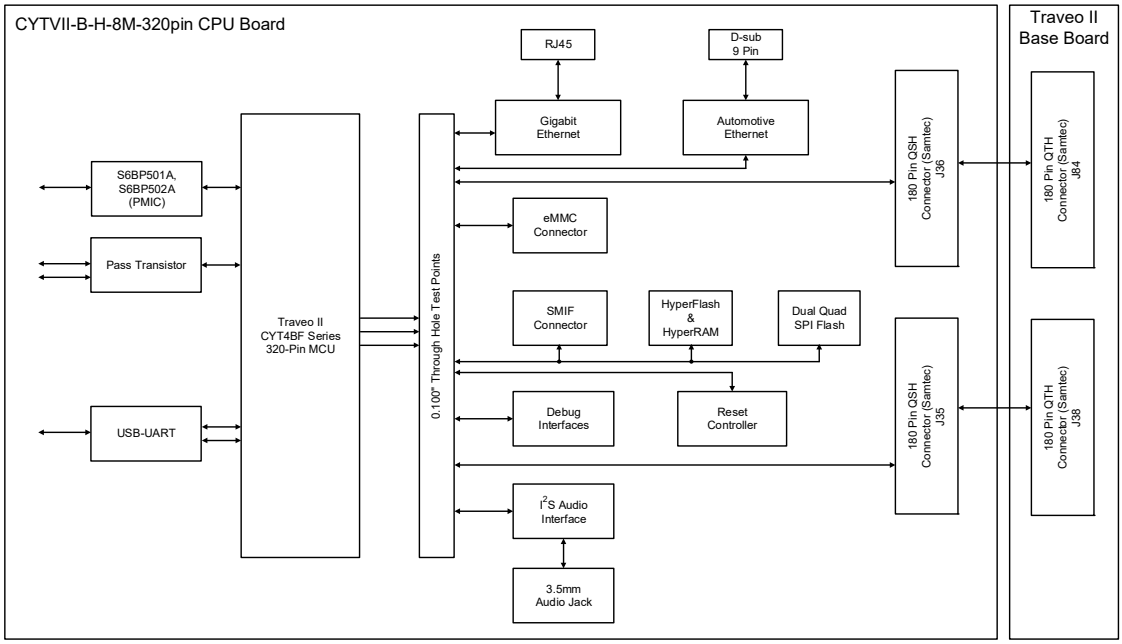
The Traveo II base board has the following components:

1. Six CAN-FD transceivers based on TJA1057GT (Dual connectors P6, P7, P8).
2. Four CAN-FD transceivers based on TJA1145T, with SPI-based transceiver configuration (Dual connectors P9, P10).
3. Six LIN transceivers based on TJA1021T (Dual connectors P3, P4, P5).
4. Two FlexRay transceivers based on TJA1081TS (Dual connector P2).
5. One CXPI transceiver based on S6BT112A01 (Connector P1).
6. One SPI EEPROM 25LC320A (U9).
7. Five user switches (SW1 through SW5), 10 user LEDs (USER_LED0 through USER_LED9), and one potentiometer (POT1) for analog input.
8. Pin headers to access all I/Os of the Traveo II device (when a CPU board is connected to the base board).
9. Samtec connector interface (J38 and J84) for connecting to a CPU board.

2.1.1 Block Diagram

The block diagram is shown in Figure 2-4.

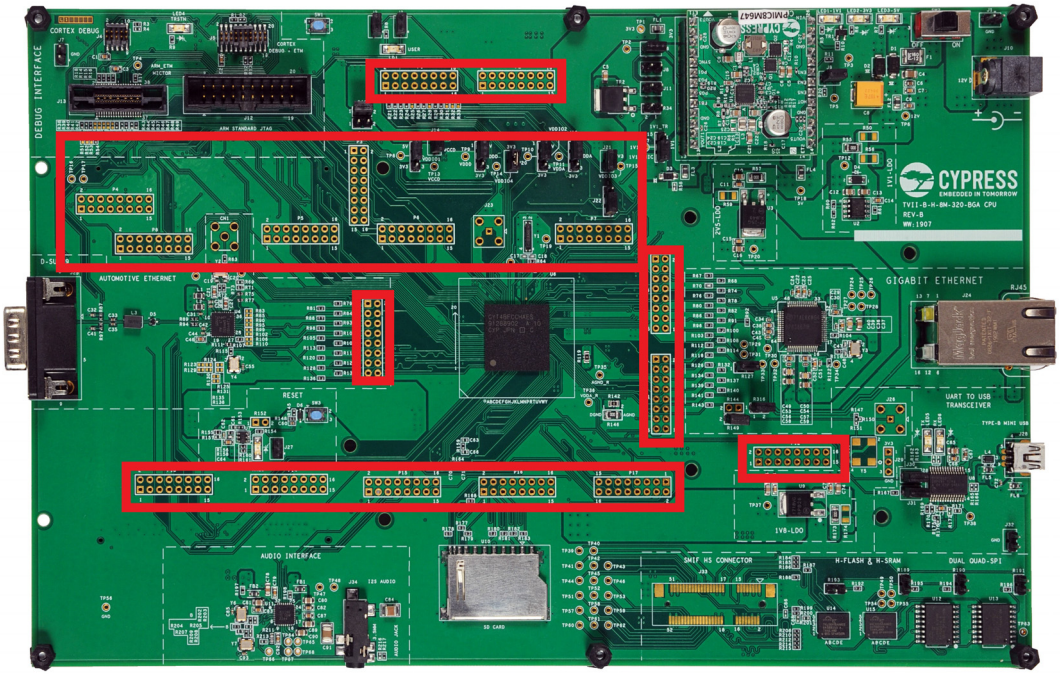
Figure 2-4. Block Diagram



2.1.2 Through-Hole Test Points

The location of the Through-Hole Test Points is shown in Figure 2-5.

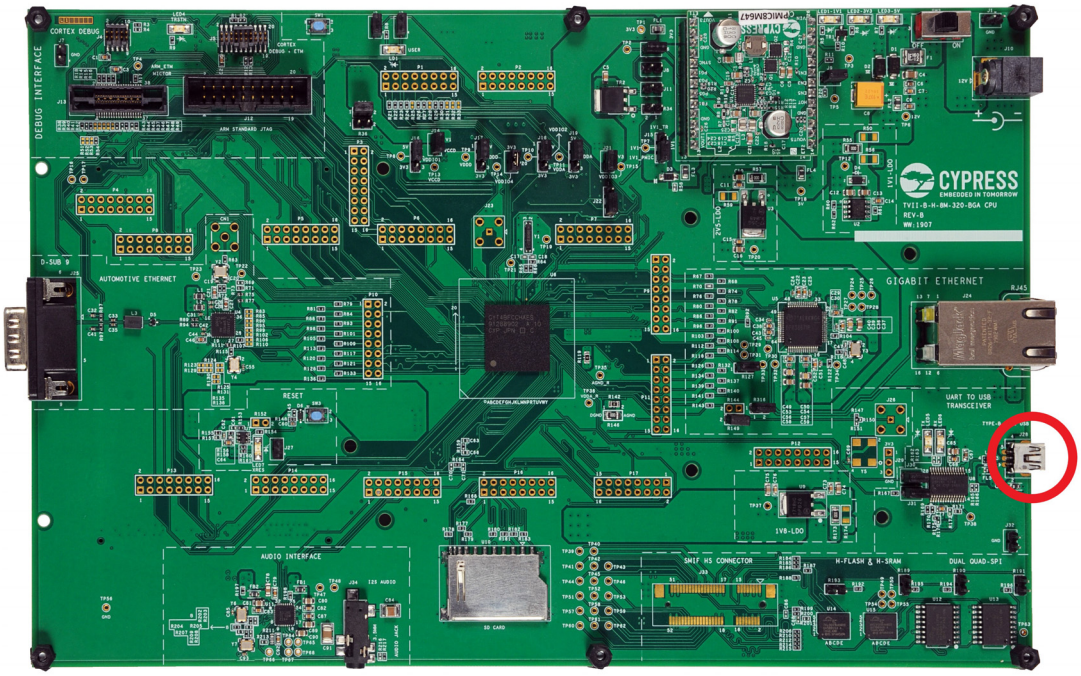
Figure 2-5. Through-Hole Test Points



2.1.3 USB Connector

The location of the USB connector is shown in Figure 2-6.

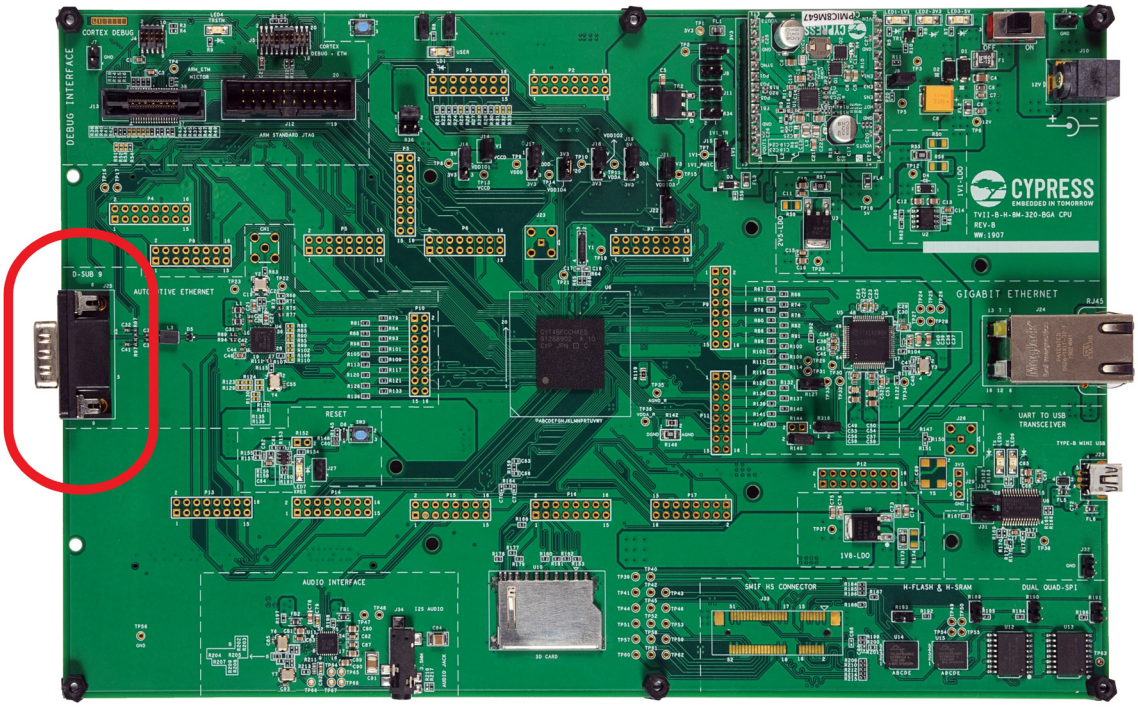
Figure 2-6. USB Connector



2.1.4 Ethernet Connector (Automotive Ethernet)

The location of the Ethernet connector (Automotive Ethernet) is shown in Figure 2-7.

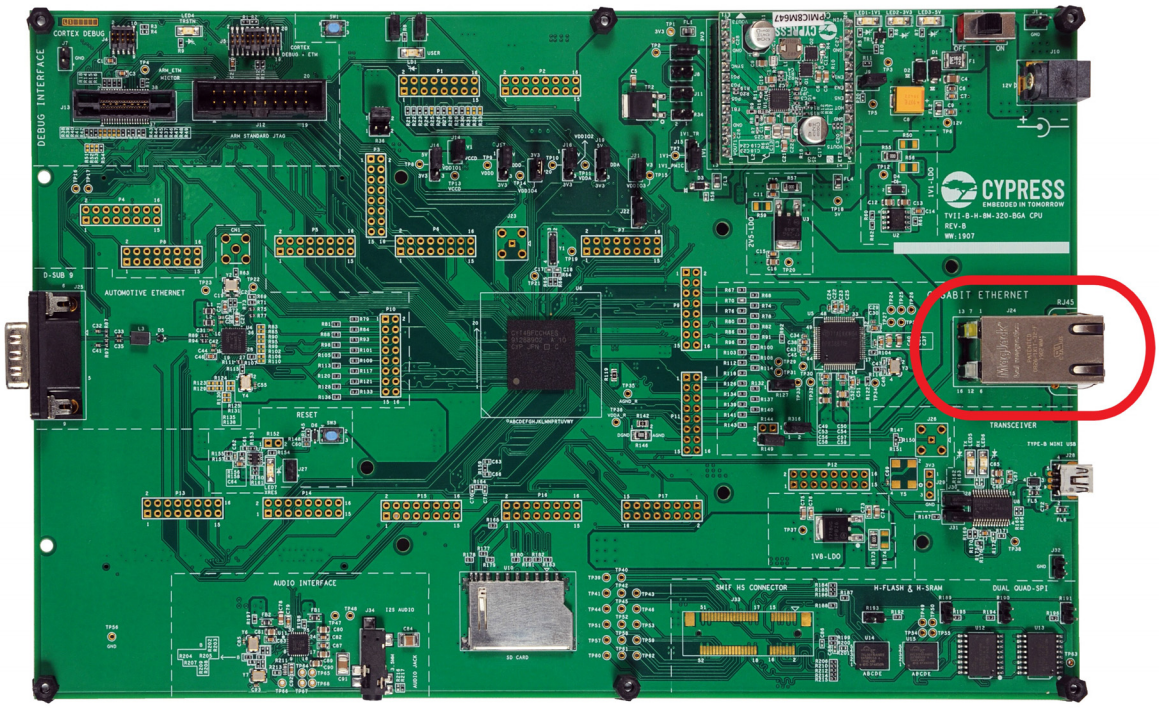
Figure 2-7. Ethernet Connector (Automotive Ethernet)



2.1.5 Ethernet Connector (Gigabit Ethernet)

The location of the Ethernet connector (Gigabit Ethernet) is shown in Figure 2-8.

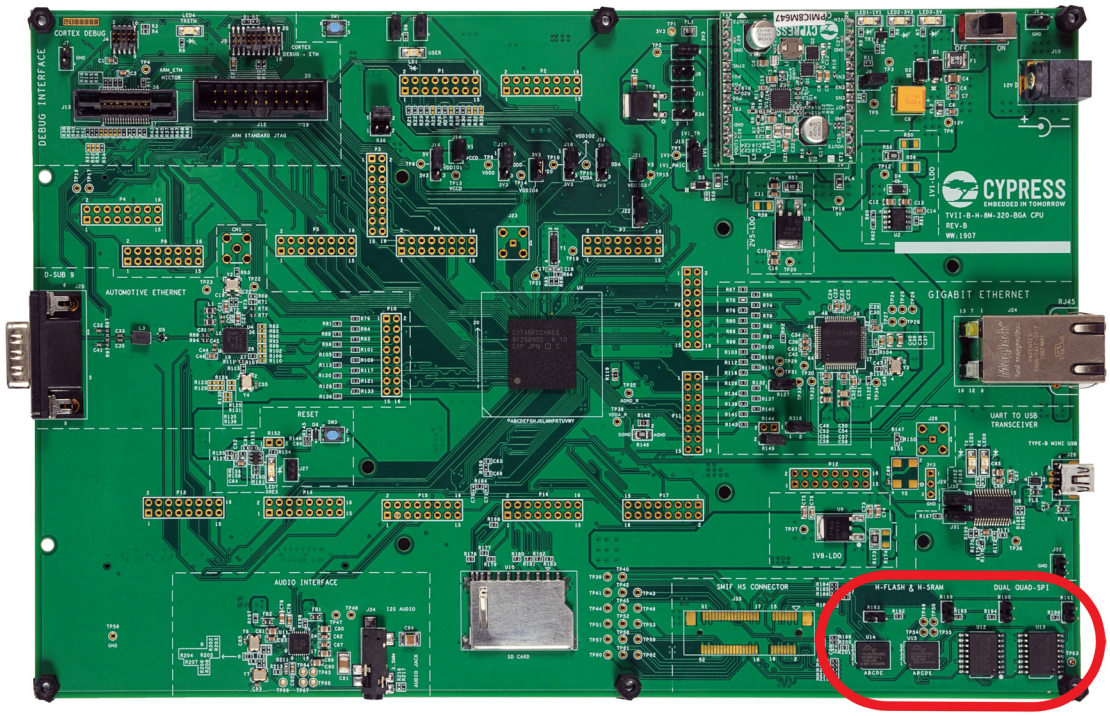
Figure 2-8. Ethernet Connector (Gigabit Ethernet)



2.1.6 On-board SMIF Devices

The location of the onboard SMIF devices in shown in Figure 2-9.

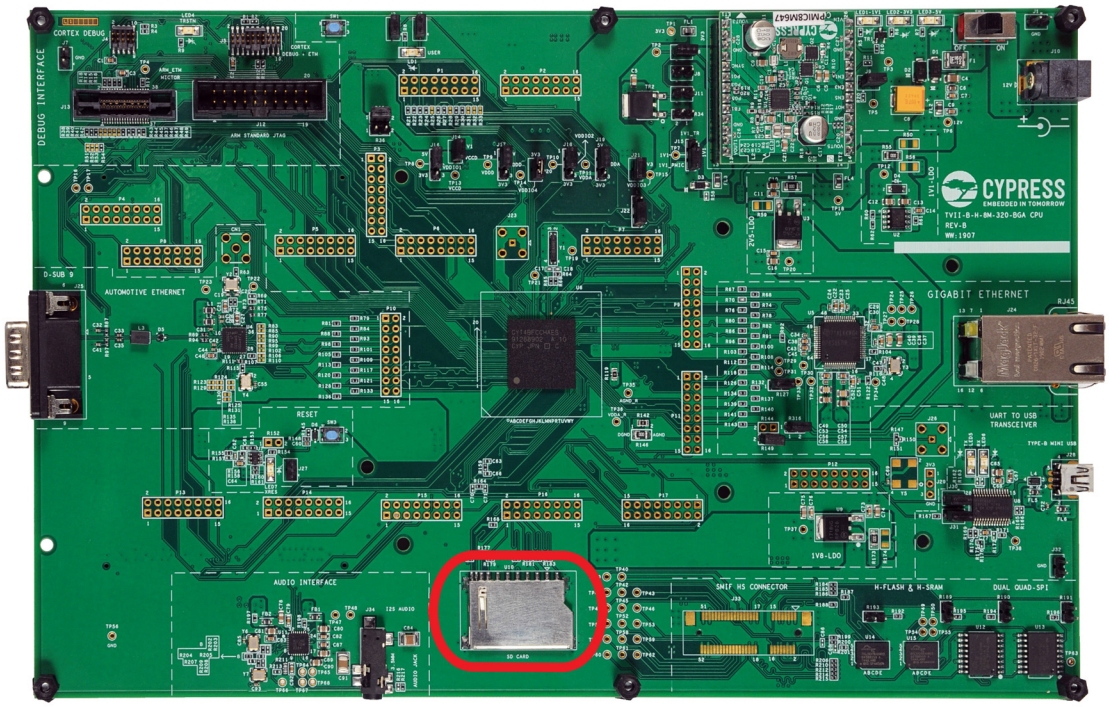
Figure 2-9. SMIF Connector



2.1.7 SD Card Connector

The location of the SD Card connector is shown in Figure 2-10.

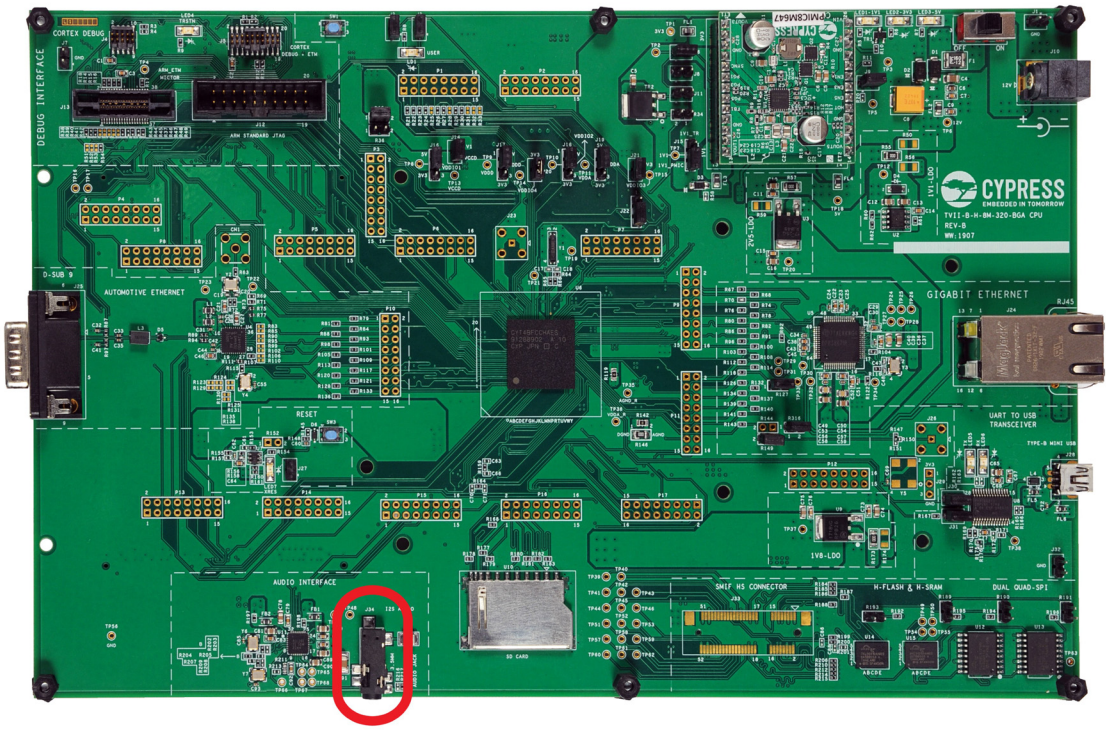
Figure 2-10. eMMC Connector



2.1.8 Audio Connector

The location of the audio connector is shown in Figure 2-11.

Figure 2-11. Audio Connector

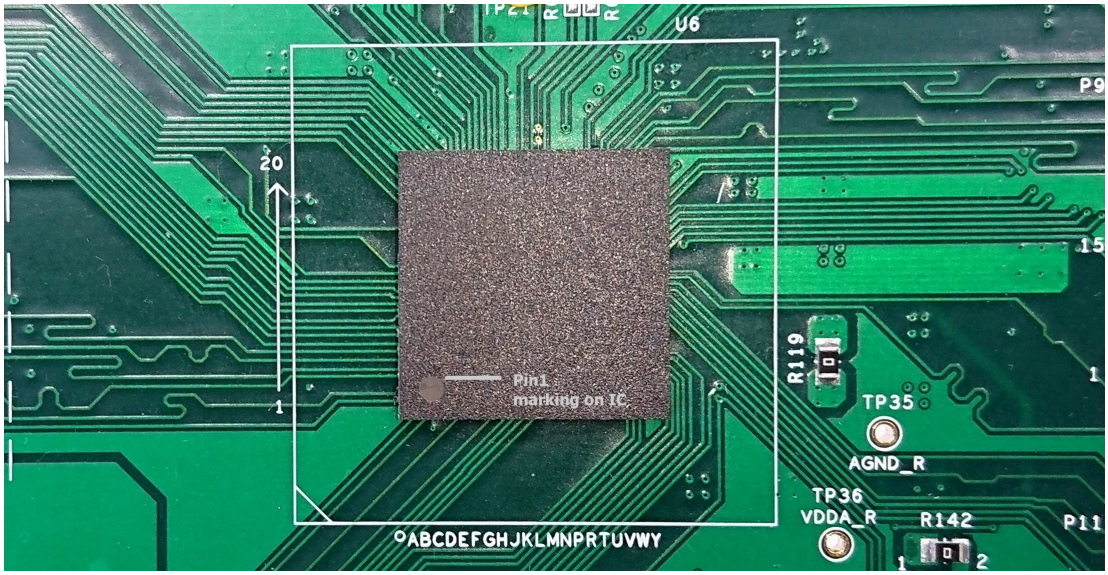


3. Operation

This section describes the operation of the CPU board and the base board. It is assumed that you have connected the CPU board to the base board using the Samtec interface and inserted a Traveo II device into the IC socket (applicable to CYTVII-B-H-320-SO boards only). Follow these steps to operate the CPU board and the base board:

1. For the socketed CPU board, ensure that the device is inserted into the socket. Remove the four screws on the socket using the screwdriver provided in the box and open the socket cover. If the device is not present, place one carefully using a vacuum picker or a pair of tweezers.
2. Ensure that pin 1 of the device is near the pin 1 marking on the PCB, as shown in Figure 3-1. Also ensure that the device is placed in an angle such that the pins on all four sides of the FBGA package match well with the socket pins. Align the device slightly, if required.

Figure 3-1. Orientation of Device when Inserted in Socket



3. Replace the socket cover and fix the four screws so that the socket cover tightly sits on the socket base.
4. A 12 V wall adapter board is supplied along with the CPU board. Connect the 12 V wall adapter to the barrel connector marked “12V DC” on the CPU board. Connect its plug to a mains socket using one of the four plug adapters provided in the white box (depending on the geographical location and the socket type available).
5. Ensure that jumpers J16, J17, J18, J19 (position “1-2”), J14, J20, J21 (current measurement jumpers) are inserted on the CPU board.
6. Turn on the mains supply to the wall adapter. Turn on the switch SW2 on the CPU board. The LED labeled PWR should light up.

7. Connect an appropriate programming tool to one of the programming interfaces (J13, J4, J12, J5). Programming tool options are:
   - Arm ETM MICTOR on J13
   - Cortex DEBUG on J4
   - Arm Standard JTAG on J12
   - Cortex DEBUG and ETM on J5
8. Install the appropriate programming integrated development environment (IDE) on a PC. The programming IDE (GHS MULTI, IAR Embedded Workbench, Cypress Programmer, etc.) should be able to detect a device (read the device ID) and to load a firmware HEX file (*.srec*) into the device flash successfully.
   As part of the release package, various firmware examples compiled in *.srec* programming IDEs are available. Some examples use specific transceivers on the base board.
9. To start with, use the LED blink example provided with the release package to test the functioning of the board.
10. Connect a USB-mini cable to J28 and the other end to a PC. Open Tera Term or your preferred terminal logging application and set the appropriate port and baud rate (typically 115,200 baud, 8, N, 1). Ensure that jumpers J30 and J31 are inserted on the CPU board. Some firmware examples provide data logs from the device or ask for user inputs over the terminal.

4. Connections and Settings

4.1 Evaluation Board Connections

4.1.1 Base Board Connections

Make sure that the following jumpers are inserted on the base board, so that each transceiver on the base board can be used with the respective firmware example that activate each functionality of the device:

- CAN1.4 from the device uses the CAN0 transceiver on the base board (connect jumpers J70, J71, J72).
- CAN1.3 from the device uses the CAN1 transceiver on the base board (connect jumpers J66, J67, J68).
- CAN0.2 from the device uses the CAN2 transceiver on the base board (connect jumpers J81, J82, J83).
- CAN1.0 from the device uses the CAN3 transceiver on the base board (connect jumpers J76, J77, J78).
- CAN1.2 from the device uses the CAN4 transceiver on the base board (connect jumpers J91, J92, J93).
- CAN1.1 from the device uses the CAN6 transceiver on the base board (connect jumpers J86, J87, J88).
- LIN0 from the device uses the LIN0 transceiver on the base board (connect jumpers J58, J59, J60, J63).
- LIN6 from the device uses the LIN1 transceiver on the base board (connect jumpers J51, J52, J53, J56).
- LIN8 from the device uses the LIN2 transceiver on the base board (connect jumpers J37, J39, J40, J43).
- LIN7 from the device uses the LIN3 transceiver on the base board (connect jumpers J30, J31, J32, J35).
- LIN10 from the device uses the LIN4 transceiver on the base board (connect jumpers J22, J23, J24, J27).
- LIN5 from the device uses the LIN5 transceiver on the base board (connect jumpers J10, J16, J17, J20).
- EEPROM on the base board is enabled by connecting jumpers J47, J48, J49.
- The user switch functionality is enabled by connecting jumper J102.
- The potentiometer functionality is enabled by connecting jumper J89.

4.1.2 CPU Board Connections

- Gigabit Ethernet on the CPU board is enabled for GMII and RGMII mode by shorting the jumpers R127 and R149. R316 should be open. For MII mode, by shorting the jumper R316. R127 and R149 should be open.
- Automotive Ethernet on the CPU Board is enabled for RMII mode by shorting jumper R107. For MII mode, R107 should be open.
- SMIF - Dual Quad SPI on the CPU Board is enabled by shorting jumpers R190 and R191.
- SMIF - HyperFlash and HyperRAM on the CPU Board is enabled by shorting jumpers R189 and R193.
- SD Card Connector on the CPU board is always enabled.
- I2S Audio Codec on the CPU board is always enabled.

In addition, power is supplied to the base board by connecting jumper J80 to the 3 V or 5 V select jumper pin in the ‘5 V’ position. Make sure that jumper J80 is always connected. Once a specific functionality is chosen by connecting the jumpers listed above, ensure that the appropriate firmware is loaded onto the device. Incorrect firmware can result in port pins being configured incorrectly leading to bus contention and damage to hardware. For example, if you connect jumpers related to CAN0.0, you must ensure that firmware configures the related ports as CAN pins. Contact Cypress technical support for firmware examples.

Apart from these interface transceivers that can be used for specific functions, all pins of the device are also accessible on the base board using pin headers JP1 through JP12.

The device port pins are connected to pin headers on the CPU board as listed in Table 4-1.

Table 4-1. Device Port Pin Connections on CPU Board

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
1	J20	DRV_VOUT	R34.1	DRV_VOUT		
2	A18	P0_0/PWM1_18/PWM1_22_N/TC1_18_TR0/TC1_22_TR1/PWM0_H_0/SCB0_RX/ SCB7_SDA/SCB0_MISO/LIN1_RX	J52.2	GPIO_P0_0		
3	B18	P0_1/PWM1_17/PWM1_18_N/TC1_17_TR0/TC1_18_TR1/PWM0_H_0_N/ SCB0_TX/SCB7_SCL/SCB0_MOSI/LIN1_TX	P14.2	GPIO_P0_1		
4	B17	P0_2/PWM1_14/PWM1_17_N/TC1_14_TR0/TC1_17_TR1/TC0_H_0_TR0/ SCB0_RTS/SCB0_SCL/SCB0_CLK/SCB4_MISO/LIN1_EN/CAN0_1_TX	P14.7	GPIO_P0_2		
5	C17	P0_3/PWM1_13/PWM1_14_N/TC1_13_TR0/TC1_14_TR1/TC0_H_0_TR1/ SCB0_CTS/SCB0_SDA/SCB0_SEL0/SCB4_MOSI/CAN0_1_RX	P14.4	GPIO_P0_3		
6	A17	P1_0/PWM1_12/PWM1_13_N/TC1_12_TR0/TC1_13_TR1/PWM1_H_4/SCB0_SCL/ SCB0_MISO/SCB4_CLK	P13.7	BB_CAN5_S		
7	A16	P1_1/PWM1_11/PWM1_12_N/TC1_11_TR0/TC1_12_TR1/PWM1_H_5/SCB0_SDA/ SCB0_MOSI/SCB4_SEL0	P13.9	BB_CAN4_S		
8	B16	P1_2/PWM1_10/PWM1_11_N/TC1_10_TR0/TC1_11_TR1/PWM1_H_6/SCB0_CLK/ LIN0_RX/TRIG_IN[0]	P6.9	BB_LIN0_RXD		
9	C16	P1_3/PWM1_8/PWM1_10_N/TC1_8_TR0/TC1_10_TR1/PWM1_H_7/SCB0_SEL0/ LIN0_TX/TRIG_IN[1]	P6.10	BB_LIN5_WAKE		
10	C15	P1_4/PWM1_71/PWM1_70_N/TC1_71_TR0/TC1_70_TR1/LIN8_RX/SCB8_RX/ SCB8_MISO	P6.8	BB_LIN4_WAKE		
11	E15	P1_5/LIN8_TX/SCB8_TX/SCB8_SDA/SCB8_MOSI	P1.6	GPIO_P1_5		
12	F14	P1_6/LIN8_EN/SCB8_RTS/SCB8_SCL/SCB8_CLK	P1.10	GPIO_P1_6		
13	A15	P2_0/PWM1_7/PWM1_8_N/TC1_7_TR0/TC1_8_TR1/TC1_H_4_TR0/SCB7_RX/ SCB0_SEL1/SCB7_MISO/LIN0_RX/CAN0_0_TX/SWJ_TRSTN/TRIG_IN[2]	J13.21	TRSTN_PRM		
14	B15	P2_1/PWM1_6/PWM1_7_N/TC1_6_TR0/TC1_7_TR1/TC1_H_5_TR0/SCB7_TX/ SCB7_SDA/SCB0_SEL2/SCB7_MOSI/LIN0_TX/CAN0_0_RX/TRIG_IN[3]	P14.9	GPIO_P2_1		
15	A14	P2_2/PWM1_5/PWM1_6_N/TC1_5_TR0/TC1_6_TR1/ETH0_RX_ER/ TC1_H_6_TR0/SCB7_RTS/SCB7_SCL/SCB0_SEL3/SCB7_CLK/LIN0_EN/ TRIG_IN[4]	P10.13	AUTO_ETH_RXER_R		
16	B14	P2_3/PWM1_4/PWM1_5_N/TC1_4_TR0/TC1_5_TR1/ETH0_ETH_TSU_TIMER_C-MP_VAL/TC1_H_7_TR0/SCB7_CTS/SCB7_SEL0/LIN5_RX/TRIG_IN[5]	P14.12	GPIO_P2_3		
17	C14	P2_4/PWM1_3/PWM1_4_N/TC1_3_TR0/TC1_4_TR1/PWM1_H_4_N/SCB7_SEL1/ LIN5_TX/TRIG_IN[6]	P6.7	BB_LIN3_WAKE		
18	E14	P2_5/PWM1_2/PWM1_3_N/TC1_2_TR0/TC1_3_TR1/PWM1_H_5_N/SCB7_SEL2/ LIN5_EN/TRIG_IN[7]	P1.11	GPIO_P2_5		
19	C13	P2_6/PWM1_72/PWM1_71_N/TC1_72_TR0/TC1_71_TR1/SCB8_CTS/SCB8_SEL0	P6.6	BB_LIN2_WAKE		
20	E13	P2_7/PWM1_73/PWM1_72_N/TC1_73_TR0/TC1_72_TR1/SCB8_SEL1/LIN11_RX	P5.12	BB_USER_LED9		
21	A13	P3_0/PWM1_1/PWM1_2_N/TC1_1_TR0/TC1_2_TR1/ETH0_MDIO/PWM1_H_6_N/ SCB6_RX/SCB6_MISO/CAN0_3_TX/TRIG_DBG[0]	P10.15	AUTO_ETH_MDIO_R		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
22	B13	P3_1/PWM1_0/PWM1_1_N/TC1_0_TR0/TC1_1_TR1/ETH0_MDC/PWM1_H_7_N/ SCB6_TX/SCB6_SDA/SCB6_MOSI/CAN0_3_RX/TRIG_DBG[1]	P10.16	AUTO_ETH_MDC_R		
23	A12	P3_2/PWM1_M_3/PWM1_0_N/TC1_M_3_TR0/TC1_0_TR1/TC1_H_4_TR1/ SCB6_RTS/SCB6_SCL/SCB6_CLK	P13.13	BB_CAN3_S		
24	B12	P3_3/PWM1_M_2/PWM1_M_3_N/TC1_M_2_TR0/TC1_M_3_TR1/TC1_H_5_TR1/ SCB6_CTS/SCB6_SEL0	P5.16	BB_CXPI_TXD		
25	C12	P3_4/PWM1_M_1/PWM1_M_2_N/TC1_M_1_TR0/TC1_M_2_TR1/TC1_H_6_TR1/ SCB6_SEL1/LIN1_RX	P5.13	BB_LIN1_WAKE		
26	E12	P3_5/PWM1_M_0/PWM1_M_1_N/TC1_M_0_TR0/TC1_M_1_TR1/TC1_H_7_TR1/ SCB6_SEL2/LIN1_TX	P5.11	BB_USER_LED8		
27	C11	P3_6/PWM1_74/PWM1_73_N/TC1_74_TR0/TC1_73_TR1/SCB8_SEL2/LIN11_TX/ CAN1_2_TX	P5.15	BB_LIN0_WAKE		
28	E11	P3_7/PWM1_75/PWM1_74_N/TC1_75_TR0/TC1_74_TR1/LIN11_EN/CAN1_2_RX	P5.10	BB_USER_LED7		
29	A9	P4_0/PWM1_4/PWM1_M_0_N/TC1_4_TR0/TC1_M_0_TR1/EXT_MUX[0]_0/ SCB5_RX/SCB5_MISO/LIN1_RX/TRIG_IN[10]	P15.9	BB_SPI0_MISO		
30	A8	P4_1/PWM1_5/PWM1_4_N/TC1_5_TR0/TC1_4_TR1/EXT_MUX[0]_1/SCB5_TX/ SCB5_SDA/SCB5_MOSI/LIN1_TX/TRIG_IN[11]	P15.12	BB_SPI0_MOSI		
31	B8	P4_2/PWM1_6/PWM1_5_N/TC1_6_TR0/TC1_5_TR1/EXT_MUX[0]_2/SCB5_RTS/ SCB5_SCL/SCB5_CLK/LIN1_EN/TRIG_IN[12]	P14.1	BB_SPI0_CLK		
32	C8	P4_3/PWM1_7/PWM1_6_N/TC1_7_TR0/TC1_6_TR1/EXT_MUX[0]_EN/SCB5_CTS/ SCB5_SEL0/CAN0_1_TX/TRIG_IN[13]	P14.11	BB_SPI0_SS0		
33	E8	P4_4/PWM1_8/PWM1_7_N/TC1_8_TR0/TC1_7_TR1/LIN15_RX/SCB5_SEL1/ CAN0_1_RX	P15.11	AUDIO_SPI0_SS1		
34	A7	P4_5/SCB9_RX/SCB9_MISO/TRIG_IN[32]	P8.2	BB_CAN0_S		
35	B7	P4_6/SCB9_TX/SCB9_SDA/SCB9_MOSI/TRIG_IN[33]	P8.13	BB_CXPI_CLK		
36	A5	P5_0/PWM1_9/PWM1_8_N/TC1_9_TR0/TC1_8_TR1/PWM0_M_0/PWM1_H_10/ LIN15_TX/SCB5_SEL2/LIN7_RX/TRIG_IN[38]	P15.4	GPIO_P5_0		
37	B5	P5_1/PWM1_10/PWM1_9_N/TC1_10_TR0/TC1_9_TR1/PWM0_M_0_N/ PWM1_H_10_N/SCB9_SEL3/LIN7_TX/TRIG_IN[39]	P15.3	GPIO_P5_1		
38	C5	P5_2/PWM1_11/PWM1_10_N/TC1_11_TR0/TC1_10_TR1/TC0_M_0_TR0/ TC1_H_10_TR0/LIN10_RX/LIN7_EN	P15.2	GPIO_P5_2		
39	A4	P5_3/PWM1_12/PWM1_11_N/TC1_12_TR0/TC1_11_TR1/TC0_M_0_TR1/ TC1_H_10_TR1/LIN10_TX/LIN2_RX	P15.6	GPIO_P5_3		
40	B4	P5_4/PWM1_13/PWM1_12_N/TC1_13_TR0/TC1_12_TR1/LIN9_RX/PWM1_H_11/ LIN2_TX	P14.13	BB_CAN8_WAKE		
41	C4	P5_5/PWM1_14/PWM1_13_N/TC1_14_TR0/TC1_13_TR1/LIN9_TX/ PWM1_H_11_N/LIN2_EN	P8.12	BB_FRB_ERRN		
42	A3	P6_0/PWM1_M_0/PWM1_14_N/TC1_M_0_TR0/TC1_14_TR1/PWM0_0/LIN9_EN/ TC1_H_11_TR0/SCB4_RX/SCB4_MISO/LIN3_RX/ADC[0]_0	P15.5	GPIO_P6_0		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
43	B3	P6_1/PWM1_0/PWM1_M_0_N/TC1_0_TR0/TC1_M_0_TR1/TC1_H_11_TR1/ SCB4_TX/SCB4_SDA/SCB4_MOSI/LIN3_TX/ADC[0]_1	P15.8	GPIO_P6_1		
44	A2	P6_2/PWM1_M_1/PWM1_0_N/TC1_M_1_TR0/TC1_0_TR1/PWM0_0_N/SDHC_- CARD_MECH_WRITE_PROT/PWM1_H_12/SCB4_RTS/SCB4_SCL/SCB4_CLK/ LIN3_EN/CAN0_2_TX/ADC[0]_2	P16.2	EMMC_WP		
45	B1	P6_3/PWM1_1/PWM1_M_1_N/TC1_1_TR0/TC1_M_1_TR1/SPIHB_CLK/SDHC_- CARD_CMD/PWM1_H_12_N/SCB4_CTS/SCB4_SEL0/LIN4_RX/CAN0_2_RX/ CAL_SUP_NZ/ADC[0]_3	P16.3	GPIO_P6_3	EMMC_CMD	BB_CAN2_RXD
46	B2	P6_4/PWM1_M_2/PWM1_1_N/TC1_M_2_TR0/TC1_1_TR1/TC0_0_TR0/SPIHB_R- WDS/SDHC_CLK_CARD/TC1_H_12_TR0/SCB4_SEL1/LIN4_TX/ADC[0]_4	P16.4	GPIO_P6_4	EMMC_CLK	BB_CAN7_WAKE
47	C1	P6_5/PWM1_2/PWM1_M_2_N/TC1_2_TR0/TC1_M_2_TR1/TC0_0_TR1/SPIHB_- SEL0/SDHC_CARD_DETECT_N/TC1_H_12_TR1/SCB4_SEL2/LIN4_EN/ADC[0]_5	P16.1	EMMC_CD		
48	C2	P6_6/PWM1_M_3/PWM1_2_N/TC1_M_3_TR0/TC1_2_TR1/SCB4_SEL3/ TRIG_IN[8]/ADC[0]_6	P8.10	BB_FRA_WAKE		
49	D1	P6_7/PWM1_3/PWM1_M_3_N/TC1_3_TR0/TC1_M_3_TR1/TRIG_IN[9]/ADC[0]_7	P3.14	BB_USER_BUT- TON_1		
50	F1	P7_0/PWM1_M_4/PWM1_3_N/TC1_M_4_TR0/TC1_3_TR1/PWM0_1/SPIHB_SEL1/ SDHC_CARD_IF_PWR_EN/SCB5_RX/SCB5_MISO/LIN4_RX/ADC[0]_16	P16.15	GPIO_P7_0		
51	F2	P7_1/PWM1_15/PWM1_M_4_N/TC1_15_TR0/TC1_M_4_TR1/SPIHB_DATA0/SDH- C_CARD_DAT_3TO0_0/SCB5_TX/SCB5_SDA/SCB5_MOSI/LIN4_TX/ADC[0]_17	P16.6	EMMC_DATA0		
52	G1	P7_2/PWM1_M_5/PWM1_15_N/TC1_M_5_TR0/TC1_15_TR1/PWM0_1_N/SPIHB_- DATA1/SDHC_CARD_DAT_3TO0_1/SCB5_RTS/SCB5_SCL/SCB5_CLK/LIN4_EN/ ADC[0]_18	P16.5	EMMC_DATA1		
53	G2	P7_3/PWM1_16/PWM1_M_5_N/TC1_16_TR0/TC1_M_5_TR1/TC0_1_TR0/SPIHB_- DATA2/SDHC_CARD_DAT_3TO0_2/SCB5_CTS/SCB5_SEL0/CAN0_4_TX/ ADC[0]_19	P16.8	EMMC_DATA2		
54	G3	P7_4/PWM1_M_6/PWM1_16_N/TC1_M_6_TR0/TC1_16_TR1/TC0_1_TR1/SPIHB_- DATA3/SDHC_CARD_DAT_3TO0_3/SCB5_SEL1/CAN0_4_RX/ADC[0]_20	P16.7	EMMC_DATA3		
55	G5	P7_5/PWM1_17/PWM1_M_6_N/TC1_17_TR0/TC1_M_6_TR1/PWM0_H_2/SPIHB_- DATA4/SDHC_CARD_DAT_7TO4_0/LIN10_RX/SCB5_SEL2/ADC[0]_21	P16.10	GPIO_P7_5		
56	G6	P7_6/PWM1_M_7/PWM1_17_N/TC1_M_7_TR0/TC1_17_TR1/LIN10_TX/ TRIG_IN[16]/ADC[0]_22	P5.3	BB_LIN4_TXD		
57	H5	P7_7/PWM1_18/PWM1_M_7_N/TC1_18_TR0/TC1_M_7_TR1/LIN10_EN/ TRIG_IN[17]/ADC[0]_23	P5.2	BB_LIN4_SLP		
58	H1	P8_0/PWM1_19/PWM1_18_N/TC1_19_TR0/TC1_18_TR1/PWM0_H_2_N/SPIHB_- DATA5/SDHC_CARD_DAT_7TO4_1/PWM1_H_8/LIN2_RX/CAN0_0_TX	P15.1	GPIO_P8_0		
59	H2	P8_1/PWM1_20/PWM1_19_N/TC1_20_TR0/TC1_19_TR1/TC0_H_2_TR0/SPIHB_- DATA6/SDHC_CARD_DAT_7TO4_2/PWM1_H_8_N/LIN2_TX/CAN0_0_RX/ TRIG_IN[14]/ADC[0]_24	P16.14	GPIO_P8_1		
60	H3	P8_2/PWM1_21/PWM1_20_N/TC1_21_TR0/TC1_20_TR1/TC0_H_2_TR1/SPIHB_- DATA7/SDHC_CARD_DAT_7TO4_3/TC1_H_8_TR0/LIN2_EN/TRIG_IN[15]/ ADC[0]_25	P17.2	GPIO_P8_2		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
61	J1	P8_3/PWM1_22/PWM1_21_N/TC1_22_TR0/TC1_21_TR1/TC1_H_8_TR1/ LIN16_RX/TRIG_DBG[0]/ADC[0]_26	P15.16	GPIO_P8_3		
62	J2	P8_4/PWM1_23/PWM1_22_N/TC1_23_TR0/TC1_22_TR1/LIN16_TX/TRIG_DBG[1]/ ADC[0]_27	P15.13	GPIO_P8_4		
63	K1	P9_0/PWM1_24/PWM1_23_N/TC1_24_TR0/TC1_23_TR1/PWM1_H_9/LIN16_EN/ ADC[0]_28	P16.11	GPIO_P9_0		
64	K2	P9_1/PWM1_25/PWM1_24_N/TC1_25_TR0/TC1_24_TR1/PWM1_H_9_N/ LIN12_RX/ADC[0]_29	P15.15	GPIO_P9_1		
65	J3	P9_2/PWM1_26/PWM1_25_N/TC1_26_TR0/TC1_25_TR1/TC1_H_9_TR0/ LIN12_TX/ADC[0]_30	P17.6	GPIO_P9_2		
66	J5	P9_3/PWM1_27/PWM1_26_N/TC1_27_TR0/TC1_26_TR1/TC1_H_9_TR1/ LIN12_EN/ADC[0]_31	P16.16	GPIO_P9_3		
67	K5	P10_0/PWM1_28/PWM1_27_N/TC1_28_TR0/TC1_27_TR1/PWM1_H_10/ SCB4_RX/SCB4_MISO/LIN7_RX/TRIG_IN[18]	P1.14	GPIO_P10_0		
68	L5	P10_1/PWM1_29/PWM1_28_N/TC1_29_TR0/TC1_28_TR1/PWM1_H_10_N/ SCB4_TX/SCB4_SDA/SCB4_MOSI/LIN7_TX/TRIG_IN[19]	P16.13	GPIO_P10_1		
69	M5	P10_2/PWM1_30/PWM1_29_N/TC1_30_TR0/TC1_29_TR1/LIN8_RX/ TC1_H_10_TR0/SCB4_RTS/SCB4_SCL/SCB4_CLK/FLEXRAY_RXDA	P13.4	BB_FRA_RXD		
70	N5	P10_3/PWM1_31/PWM1_30_N/TC1_31_TR0/TC1_30_TR1/LIN8_TX/ TC1_H_10_TR1/SCB4_CTS/SCB4_SEL0/FLEXRAY_TXDA	P13.2	BB_FRA_TXD		
71	R1	P10_4/PWM1_32/PWM1_31_N/TC1_32_TR0/TC1_31_TR1/LIN8_EN/PWM1_H_11/ SCB4_SEL1/FLEXRAY_TXENA_N/ADC[1]_0	P4.12	BB_FRA_TXEN		
72	R2	P10_5/PWM1_33/PWM1_32_N/TC1_33_TR0/TC1_32_TR1/PWM1_H_11_N/ SCB4_SEL2/LIN13_RX/FLEXRAY_RXDB/ADC[1]_1	P4.11	BB_FRB_RXD		
73	R3	P10_6/PWM1_33_N/TC1_33_TR1/PWM1_34/TC1_H_11_TR0/TC1_34_TR0/ LIN13_TX/FLEXRAY_TXDB/ADC[1]_2	P3.3	BB_FRB_TXD		
74	T1	P10_7/PWM1_35/PWM1_34_N/TC1_35_TR0/TC1_34_TR1/TC1_H_11_TR1/ LIN13_EN/FLEXRAY_TXENB_N/ADC[1]_3	P4.14	BB_FRB_TXEN		
75	P5	P11_0/PWM1_61/PWM1_62_N/TC1_61_TR0/TC1_62_TR1/AUDIOSS0_MCLK/ ADC[0]_M		AUDIO_0_I2S_MCLK		
76	P6	P11_1/PWM1_60/PWM1_61_N/TC1_60_TR0/TC1_61_TR1/AUDIOSS0_TX_SCK/ ADC[1]_M		AUDIO_0_I2S_TX-_SCK		
77	R5	P11_2/PWM1_59/PWM1_60_N/TC1_59_TR0/TC1_60_TR1/AUDIOSS0_TX_WS/ ADC[2]_M		AUDIO_0_I2S_TX-_WS		
78	T2	P12_0/PWM1_36/TC1_36_TR0/PWM0_H_1/PWM1_35_N/AUDIOSS0_TX_SDO/ SCB8_RX/TC1_35_TR1/SCB8_MISO/CAN0_2_TX/TRIG_IN[20]/ADC[1]_4	P14.8	GPIO_P12_0	AUDIO_0_I2S_TX-_SDO	BB_CAN2_TXD
79	T3	P12_1/PWM1_37/PWM1_36_N/TC1_37_TR0/TC1_36_TR1/PWM0_H_1_N/ AUDIOSS0_CLK_I2S_IF/SCB8_TX/SCB8_SDA/SCB8_MOSI/LIN6_EN/ CAN0_2_RX/TRIG_IN[21]/ADC[1]_5	P4.10	GPIO_P12_1	AUDIO_0_-CLK_I2S_IF	BB_LIN1_SLP

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
80	U1	P12_2/PWM1_38/PWM1_37_N/TC1_38_TR0/TC1_37_TR1/TC0_H_1_TR0/ AUDIOSS0_RX_SCK/EXT_MUX[1]_EN/SCB8_RTS/SCB8_SCL/SCB8_CLK/ LIN6_RX/ADC[1]_6	P4.5	GPIO_P12_2	AUDIO_0_I2S_RX-_SCK	BB_LIN1_RXD
81	U2	P12_3/PWM1_39/PWM1_38_N/TC1_39_TR0/TC1_38_TR1/TC0_H_1_TR1/ AUDIOSS0_RX_WS/EXT_MUX[1]_0/SCB8_CTS/SCB8_SEL0/LIN6_TX/ADC[1]_7	P3.2	GPIO_P12_3	AUDIO_0_I2S_RX-_WS	BB_LIN1_TXD
82	U3	P12_4/PWM1_40/PWM1_39_N/TC1_40_TR0/TC1_39_TR1/TC0_2_TR1/ AUDIOSS0_RX_SDI/EXT_MUX[1]_1/SCB8_SEL1/CAN1_1_TX/ADC[1]_8		AUDIO_0_I2S_RX-_SDI		
83	V1	P12_5/PWM1_41/PWM1_40_N/TC1_41_TR0/TC1_40_TR1/EXT_MUX[1]_2/ CAN1_1_RX/ADC[1]_9	P16.9	GPIO_P12_5_R		
84	V2	P12_6/PWM1_42/PWM1_41_N/TC1_42_TR0/TC1_41_TR1/ADC[1]_10	P8.7	BB_ADC_POT		
85	W1	P12_7/PWM1_43/PWM1_42_N/TC1_43_TR0/TC1_42_TR1/ADC[1]_11	P16.12	GPIO_P12_7_R		
86	Y2	P13_0/PWM1_M_8/PWM1_43_N/TC1_M_8_TR0/TC1_43_TR1/TC0_2_TR0/ AUDIOSS1_MCLK/EXT_MUX[2]_0/SCB3_RX/LIN3_RX/SCB3_MISO/ADC[1]_12	P15.7	GPIO_P13_0	AUDIO_1_I2S_MCLK	UART_RX
87	W2	P13_1/PWM1_44/PWM1_M_8_N/TC1_44_TR0/TC1_M_8_TR1/PWM0_2_N/ AUDIOSS1_TX_SCK/EXT_MUX[2]_1/SCB3_TX/SCB3_SDA/LIN3_TX/SCB3_MOSI/ ADC[1]_13	J47.2	GPIO_P13_1	AUDIO_1_I2S_TX-_SCK	UART_TX
88	Y3	P13_2/PWM1_M_9/PWM1_44_N/TC1_M_9_TR0/TC1_44_TR1/PWM0_2/ AUDIOSS1_TX_WS/EXT_MUX[2]_2/SCB3_RTS/SCB3_SCL/LIN3_EN/SCB3_CLK/ ADC[1]_14	P8.9	GPIO_P13_2	AUDIO_1_I2S_TX-_WS	BB_UART0_RTS
89	W3	P13_3/PWM1_45/PWM1_M_9_N/TC1_45_TR0/TC1_M_9_TR1/AUDIOSS1_TX-_SDO/EXT_MUX[2]_EN/SCB3_CTS/LIN2_RX/SCB3_SEL0/ADC[1]_15	P15.14	GPIO_P13_3	AUDIO_1_I2S_TX-_SDO	BB_UART0_CTS
90	Y4	P13_4/PWM1_M_10/PWM1_45_N/TC1_M_10_TR0/TC1_45_TR1/LIN8_RX/ AUDIOSS1_CLK_I2S_IF/PWM1_H_4/LIN2_TX/SCB3_SEL1/ADC[1]_16	P8.1	GPIO_P13_4	AUDIO_1_-CLK_I2S_IF	BB_LIN2_RXD
91	W4	P13_5/PWM1_46/PWM1_M_10_N/TC1_46_TR0/TC1_M_10_TR1/LIN8_TX/ AUDIOSS1_RX_SCK/PWM1_H_4_N/SCB3_SEL2/ADC[1]_17	P8.3	GPIO_P13_5	AUDIO_1_I2S_RX-_SCK	BB_LIN2_TXD
92	Y5	P13_6/PWM1_M_11/PWM1_46_N/TC1_M_11_TR0/TC1_46_TR1/LIN8_EN/ AUDIOSS1_RX_WS/PWM1_H_5/SCB3_SEL3/TRIG_IN[22]/ADC[1]_18	P8.5	GPIO_P13_6	AUDIO_1_I2S_RX-_WS	BB_LIN2_SLP
93	W5	P13_7/PWM1_47/PWM1_M_11_N/TC1_47_TR0/TC1_M_11_TR1/AUDIOSS1_RX-_SDI/PWM1_H_5_N/TRIG_IN[23]/ADC[1]_19		AUDIO_1_I2S_RX-_SDI		
94	V5	P14_0/PWM1_48/PWM1_47_N/TC1_48_TR0/TC1_47_TR1/PWM0_M_1/ AUDIOSS2_MCLK/PWM1_H_6/SCB2_MISO/SCB2_RX/CAN1_0_TX/ADC[1]_20	P11.15	GPIO_P14_0		
95	T5	P14_1/PWM1_49/PWM1_48_N/TC1_49_TR0/TC1_48_TR1/PWM0_M_1_N/ AUDIOSS2_TX_SCK/PWM1_H_6_N/SCB2_MOSI/SCB2_SDA/SCB2_TX/ CAN1_0_RX/ADC[1]_21	P4.4	BB_I2C1_SDA		
96	Y6	P14_2/PWM1_50/PWM1_49_N/TC1_50_TR0/TC1_49_TR1/TC0_M_1_TR0/ PWM1_H_7/SCB2_CLK/SCB2_SCL/SCB2_RTS/LIN6_RX/ADC[1]_22	P4.13	BB_I2C1_SCL		
97	W6	P14_3/PWM1_51/PWM1_50_N/TC1_51_TR0/TC1_50_TR1/TC0_M_1_TR1/ PWM1_H_7_N/SCB2_SEL0/SCB2_CTS/LIN6_TX/ADC[1]_23	P11.14	GPIO_P14_3		
98	V6	P14_4/PWM1_52/PWM1_51_N/TC1_52_TR0/TC1_51_TR1/AUDIOSS2_TX_WS/ TC1_H_4_TR0/SCB2_SEL1/LIN6_EN/ADC[1]_24	P11.16	GPIO_P14_4		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
99	T6	P14_5/PWM1_53/PWM1_52_N/TC1_53_TR0/TC1_52_TR1/AUDIOSS2_TX_SDO/ TC1_H_4_TR1/SCB2_SEL2/LIN14_RX/ADC[1]_25	P12.12	GPIO_P14_5		
100	R7	P14_6/PWM1_54/PWM1_53_N/TC1_54_TR0/TC1_53_TR1/TC1_H_5_TR0/ LIN14_TX/TRIG_IN[24]/ADC[1]_26	P12.16	GPIO_P14_6		
101	T7	P14_7/PWM1_55/PWM1_54_N/TC1_55_TR0/TC1_54_TR1/TC1_H_5_TR1/ LIN14_EN/TRIG_IN[25]/ADC[1]_27	P17.8	GPIO_P14_7		
102	Y7	P15_0/PWM1_56/PWM1_55_N/TC1_56_TR0/TC1_55_TR1/AUDIOSS2_- CLK_I2S_IF/TC1_H_6_TR0/SCB9_RX/SCB9_MISO/CAN1_3_TX/ADC[1]_28	P3.6	BB_CAN1_TXD		
103	W7	P15_1/PWM1_57/PWM1_56_N/TC1_57_TR0/TC1_56_TR1/AUDIOSS2_RX_SCK/ TC1_H_6_TR1/SCB9_TX/SCB9_SDA/SCB9_MOSI/CAN1_3_RX/ADC[1]_29	P4.6	BB_CAN1_RXD		
104	V7	P15_2/PWM1_58/PWM1_57_N/TC1_58_TR0/TC1_57_TR1/AUDIOSS2_RX_WS/ TC1_H_7_TR0/SCB9_RTS/SCB9_SCL/SCB9_CLK/ADC[1]_30	P12.14	GPIO_P15_2		
105	T8	P15_3/PWM1_59/PWM1_58_N/TC1_59_TR0/TC1_58_TR1/AUDIOSS2_RX_SDI/ TC1_H_7_TR1/SCB9_CTS/SCB9_SEL0/ADC[1]_31	P12.10	GPIO_P15_3		
106	T9	P16_0/PWM1_60/PWM1_59_N/TC1_60_TR0/TC1_59_TR1/PWM1_H_0/SCB9_- SEL1/LIN11_RX/ADC[2]_0	P12.15	GPIO_P16_0		
107	T10	P16_1/PWM1_61/PWM1_60_N/TC1_61_TR0/TC1_60_TR1/PWM1_H_0_N/SCB9_- SEL2/LIN11_TX/ADC[2]_1	P12.9	GPIO_P16_1		
108	T11	P16_2/PWM1_62/PWM1_61_N/TC1_62_TR0/TC1_61_TR1/PWM1_H_1/SCB9_- SEL3/LIN11_EN/ADC[2]_2	P11.13	GPIO_P16_2		
109	T12	P16_3/PWM1_62/PWM1_62_N/TC1_62_TR0/TC1_62_TR1/PWM1_H_1_N/ ADC[2]_3	P2.6	GPIO_P16_3		
110	T13	P16_4/PWM1_68/PWM1_69_N/TC1_68_TR0/TC1_69_TR1/ADC[2]_4	P2.16	GPIO_P16_4		
111	Y12	P16_5/PWM1_67/PWM1_68_N/TC1_67_TR0/TC1_68_TR1/ADC[2]_5	P12.5	GPIO_P16_5		
112	Y13	P16_6/PWM1_66/PWM1_67_N/TC1_66_TR0/TC1_67_TR1/ADC[2]_6	P12.4	GPIO_P16_6		
113	Y14	P16_7/PWM1_65/PWM1_66_N/TC1_65_TR0/TC1_66_TR1/ADC[2]_7	P12.3	GPIO_P16_7		
114	W14	P17_0/PWM1_61/PWM1_62_N/TC1_61_TR0/TC1_62_TR1/LIN11_RX/CAN1_1_TX/ ADC[2]_8	P14.15	BB_CAN6_TXD		
115	V14	P17_1/PWM1_60/PWM1_61_N/TC1_60_TR0/TC1_61_TR1/SCB3_RX/LIN11_TX/ CAN1_1_RX/ADC[2]_9	P14.16	BB_CAN6_RXD		
116	T14	P17_2/PWM1_59/PWM1_60_N/TC1_59_TR0/TC1_60_TR1/SCB3_TX/SCB3_SDA/ LIN11_EN/ADC[2]_10	P2.15	GPIO_P17_2		
117	R14	P17_3/PWM1_58/PWM1_59_N/TC1_58_TR0/TC1_59_TR1/PWM1_H_3/ SCB3_RTS/SCB3_SCL/SCB3_CLK/TRIG_IN[26]/ADC[2]_11	P1.13	GPIO_P17_3		
118	Y15	P17_4/PWM1_57/PWM1_58_N/TC1_57_TR0/TC1_58_TR1/PWM1_H_3_N/ SCB3_CTS/SCB3_SEL0/TRIG_IN[27]/ADC[2]_12	P12.2	GPIO_P17_4		
119	W15	P17_5/PWM1_56/PWM1_57_N/TC1_56_TR0/TC1_57_TR1/PWM1_H_2/LIN15_RX/ SCB3_SEL1/ADC[2]_13	P12.6	GPIO_P17_5		
120	Y16	P17_6/PWM1_M_4/PWM1_56_N/TC1_M_4_TR0/TC1_56_TR1/PWM1_H_2_N/ LIN15_TX/SCB3_SEL2/ADC[2]_14	P12.7	GPIO_P17_6		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
121	W16	P17_7/PWM1_M_5/PWM1_M_4_N/TC1_M_5_TR0/TC1_M_4_TR1/LIN15_EN/ LIN12_RX/ADC[2]_15	P12.8	GPIO_P17_7		
122	V16	P18_0/PWM1_M_6/PWM1_M_5_N/TC1_M_6_TR0/TC1_M_5_TR1/ETH0_REF_- CLK/PWM1_H_0/SCB1_RX/SCB1_MISO/LIN12_TX/FAULT_OUT_0/ADC[2]_16	P7.5	GPIO_P18_0	AUTO_ETH_REF_- CLK_R	BB_CAN_SPI1_MISO
123	Y17	P18_1/PWM1_M_7/PWM1_M_6_N/TC1_M_7_TR0/TC1_M_6_TR1/ETH0_TX_CTL/ PWM1_H_0_N/SCB1_TX/SCB1_SDA/SCB1_MOSI/SCB3_MISO/FAULT_OUT_1/ ADC[2]_17	P7.16	GPIO_P18_1	AUTO_ETH_TXEN_R	BB_CAN_SPI1_MOSI
124	W17	P18_2/PWM1_55/PWM1_M_7_N/TC1_55_TR0/TC1_M_7_TR1/ETH0_TX_ER/ PWM1_H_1/SCB1_RTS/SCB1_SCL/SCB1_CLK/SCB3_MOSI/ADC[2]_18	P7.6	GPIO_P18_2	AUTO_ETH_TXER_R	BB_CAN_SPI1_SCK
125	Y18	P18_3/PWM1_54/PWM1_55_N/TC1_54_TR0/TC1_55_TR1/ETH0_TX_CLK/ PWM1_H_1_N/SCB1_CTS/SCB1_SEL0/SCB3_CLK/TRACE_CLOCK/ADC[2]_19	P7.14	GPIO_P18_3	AUTO_ETH_TXC_R	TRACE_CLOCK_0
126	Y19	P18_4/PWM1_53/PWM1_54_N/TC1_53_TR0/TC1_54_TR1/PWM0_M_2/ETH0_TX- D_0/PWM1_H_2/SCB1_SEL1/SCB3_SEL0/TRACE_DATA_0/ADC[2]_20	P15.10	GPIO_P18_4	AUTO_ETH_TXD0_R	TRACE_DATA_0_0
127	T15	P18_5/PWM1_52/PWM1_53_N/TC1_52_TR0/TC1_53_TR1/PWM0_M_2_N/ ETH0_TXD_1/PWM1_H_2_N/SCB1_SEL2/TRACE_DATA_1/ADC[2]_21	P7.8	GPIO_P18_5	AUTO_ETH_TXD1_R	TRACE_DATA_1_0
128	T16	P18_6/PWM1_51/PWM1_52_N/TC1_51_TR0/TC1_52_TR1/TC0_M_2_TR0/ ETH0_TXD_2/PWM1_H_3/SCB1_SEL3/CAN1_2_TX/TRACE_DATA_2/ADC[2]_22	P7.3	GPIO_P18_6	AUTO_ETH_TXD2_R	TRACE_DATA_2_0
129	R16	P18_7/PWM1_50/PWM1_51_N/TC1_50_TR0/TC1_51_TR1/TC0_M_2_TR1/ ETH0_TXD_3/PWM1_H_3_N/CAN1_2_RX/TRACE_DATA_3/ADC[2]_23	P7.4	GPIO_P18_7	AUTO_ETH_TXD3_R	TRACE_DATA_3_0
130	P19	P19_0/PWM1_M_3/PWM1_50_N/TC1_M_3_TR0/TC1_50_TR1/ETH0_RXD_0/ TC1_H_0_TR0/SCB2_MISO/SCB2_RX/CAN1_3_TX/FAULT_OUT_2/ADC[2]_24	P7.12	GPIO_P19_0	AUTO_ETH_RXD0_R	TRSTN_SEC
131	P18	P19_1/PWM1_26/PWM1_M_3_N/TC1_26_TR0/TC1_M_3_TR1/ETH0_RXD_1/ TC1_H_0_TR1/SCB2_MOSI/SCB2_SDA/SCB2_TX/CAN1_3_RX/FAULT_OUT_3/ ADC[2]_25	P7.9	GPIO_P19_1	AUTO_ETH_RXD1_R	SWO_TDO_SEC
132	P16	P19_2/PWM1_27/PWM1_26_N/TC1_27_TR0/TC1_26_TR1/ETH0_RXD_2/ TC1_H_1_TR0/SCB2_CLK/SCB2_SCL/SCB2_RTS/TRIG_IN[28]/ADC[2]_26	P7.1	GPIO_P19_2	AUTO_ETH_RXD2_R	SWDOE_TDI_SEC
133	P15	P19_3/PWM1_28/PWM1_27_N/TC1_28_TR0/TC1_27_TR1/ETH0_RXD_3/ TC1_H_1_TR1/SCB2_SEL0/SCB2_CTS/TRIG_IN[29]/ADC[2]_27	P7.15	GPIO_P19_3	AUTO_ETH_RXD3_R	SWDIO_TMS_SEC
134	N16	P19_4/PWM1_29/PWM1_28_N/TC1_29_TR0/TC1_28_TR1/TC1_H_2_TR0/SCB2_- SEL1/ADC[2]_28	P7.2	SWCLK_TCLK_SEC		
135	N18	P20_0/PWM1_30/PWM1_29_N/TC1_30_TR0/TC1_29_TR1/TC1_H_2_TR1/SCB2_- SEL2/LIN5_RX/ADC[2]_29	P3.5	BB_LIN5_RXD		
136	M18	P20_1/PWM1_49/PWM1_30_N/TC1_49_TR0/TC1_30_TR1/TC1_H_3_TR0/ LIN5_TX/ADC[2]_30	P3.8	BB_LIN5_TXD		
137	M16	P20_2/PWM1_48/PWM1_49_N/TC1_48_TR0/TC1_49_TR1/TC1_H_3_TR1/ LIN5_EN/ADC[2]_31	P3.7	BB_LIN5_SLP		
138	L19	P20_3/PWM1_47/PWM1_48_N/TC1_47_TR0/TC1_48_TR1/SCB1_RX/SCB1_MISO/ CAN1_2_TX	P13.8	BB_CAN4_TXD		
139	L18	P20_4/PWM1_46/PWM1_47_N/TC1_46_TR0/TC1_47_TR1/SCB1_TX/SCB1_SDA/ SCB1_MOSI/CAN1_2_RX	P13.6	BB_CAN4_RXD		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
140	L16	P20_5/PWM1_45/PWM1_46_N/TC1_45_TR0/TC1_46_TR1/SCB1_RTS/SCB1_SCL/SCB1_CLK	P1.15	GPIO_P20_5		
141	K16	P20_6/PWM1_44/PWM1_45_N/TC1_44_TR0/TC1_45_TR1/SCB1_CTS/SCB1_-SEL0/CAN1_4_TX	P13.10	BB_CAN_SPI1_SS0		
142	J16	P20_7/PWM1_43/PWM1_44_N/TC1_43_TR0/TC1_44_TR1/SCB1_SEL1/CAN1_4_RX	P13.12	BB_CAN_SPI1_SS1		
143	N19	P21_0/PWM1_42/PWM1_43_N/TC1_42_TR0/TC1_43_TR1/SCB1_SEL2/WCO_IN		CPU_WCO_IN		
144	N20	P21_1/PWM1_41/PWM1_42_N/TC1_41_TR0/TC1_42_TR1/WCO_OUT	TP19	CPU_WCO_OUT		
145	M19	P21_2/PWM1_40/PWM1_41_N/TC1_40_TR0/TC1_41_TR1/EXT_CLK/TRIG_DBG[1]/ECO_IN		CPU_ECO_IN		
146	M20	P21_3/PWM1_39/PWM1_40_N/TC1_39_TR0/TC1_40_TR1/ECO_OUT		CPU_ECO_OUT		
147	K19	P21_4/PWM1_38/PWM1_39_N/TC1_38_TR0/TC1_39_TR1/HIBER-NATE_WAKEUP[0]	J2.1	CB_BUTTON_P21_4		
148	J19	P21_5/PWM1_37/PWM1_38_N/TC1_37_TR0/TC1_38_TR1/PWM1_34/PWM1_35_N/ETH0_RX_CTL/TC1_35_TR1/TC1_34_TR0/LIN0_RX/CAN1_1_TX/TRACE_DATA_0	P10.10	GPIO_P21_5	AUTO_ETH_RXD-V_R	TRACE_DATA_0_1
149	H19	P21_6/PWM1_36/PWM1_37_N/TC1_36_TR0/TC1_37_TR1/LIN0_TX/LIN13_RX	P6.14	BB_LIN0_TXD		
150	H18	P21_7/PWM1_35/PWM1_36_N/TC1_35_TR0/TC1_36_TR1/SCB6_RX/SCB6_MISO/LIN0_EN/LIN13_TX/CAL_SUP_NZ/RTC_CAL	P6.15	BB_LIN0_SLP		
151	H20	P22_1/PWM1_33/PWM1_34_N/TC1_33_TR0/TC1_34_TR1/SCB6_TX/SCB6_SDA/SCB6_MOSI/CAN1_1_RX/TRACE_DATA_1/EXT_PS_CTL0	P1.9	GPIO_P22_1	TRACE_DATA_1_1	EXT_PS_CTL0
152	G20	P22_2/PWM1_32/PWM1_33_N/TC1_32_TR0/TC1_33_TR1/SCB6_RTS/SCB6_SCL/SCB6_CLK/TRACE_DATA_2/EXT_PS_CTL1	P1.7	GPIO_P22_2	TRACE_DATA_2_1	EXT_PS_CTL1
153	F20	P22_3/PWM1_31/PWM1_32_N/TC1_31_TR0/TC1_32_TR1/SCB6_CTS/SCB6_-SEL0/TRACE_DATA_3/EXT_PS_CTL2	P1.3	GPIO_P22_3	TRACE_DATA_3_1	EXT_PS_CTL2
154	G19	P22_4/PWM1_30/PWM1_31_N/TC1_30_TR0/TC1_31_TR1/SCB6_SEL1/TRACE_-CLOCK	P1.5	TRACE_CLOCK_1		
155	G18	P22_5/PWM1_29/PWM1_30_N/TC1_29_TR0/TC1_30_TR1/PWM1_H_8/SCB6_-SEL2/LIN7_RX	P6.12	BB_LIN3_RXD		
156	H16	P22_6/PWM1_28/PWM1_29_N/TC1_28_TR0/TC1_29_TR1/PWM1_H_8_N/LIN7_TX	P3.10	BB_LIN3_TXD		
157	G16	P22_7/PWM1_27/PWM1_28_N/TC1_27_TR0/TC1_28_TR1/TC1_H_8_TR0/LIN14_RX/LIN7_EN	P6.16	BB_LIN3_SLP		
158	F19	P23_0/PWM1_M_8/PWM1_27_N/TC1_M_8_TR0/TC1_27_TR1/TC1_H_8_TR1/SCB7_RX/LIN14_TX/SCB7_MISO/CAN1_0_TX/FAULT_OUT_0	P6.11	BB_CAN3_TXD		
159	F18	P23_1/PWM1_M_9/PWM1_M_8_N/TC1_M_9_TR0/TC1_M_8_TR1/SCB7_TX/SCB7_SDA/SCB7_MOSI/CAN1_0_RX/FAULT_OUT_1	P6.13	BB_CAN3_RXD		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
160	E20	P23_2/PWM1_M_10/PWM1_M_9_N/TC1_M_10_TR0/TC1_M_9_TR1/SCB7_RTS/ SCB7_SCL/SCB7_CLK/LIN6_RX/FAULT_OUT_2	J3.2	CB_LED_P23_2		
161	E19	P23_3/PWM1_M_11/PWM1_M_10_N/TC1_M_11_TR0/TC1_M_10_TR1/ETH0_RX_-CLK/SCB7_CTS/SCB7_SEL0/LIN6_TX/FAULT_OUT_3/TRIG_IN[30]	P10.14	AUTO_ETH_RXC_R		
162	E18	P23_4/PWM1_25/PWM1_M_11_N/TC1_25_TR0/TC1_M_11_TR1/PWM1_H_9/ SCB2_MISO/SCB7_SEL1/TRIG_DBG[0]/SWJ_SWO_TDO/TRIG_IN[31]	P2.3	SWO_TDO_PRM		
163	D20	P23_5/PWM1_24/PWM1_25_N/TC1_24_TR0/TC1_25_TR1/LIN9_RX/ PWM1_H_9_N/SCB2_MOSI/SCB7_SEL2/SWJ_SWCLK_TCLK	P2.5	SWCLK_TCLK_PRM		
164	F16	P23_6/PWM1_23/PWM1_24_N/TC1_23_TR0/TC1_24_TR1/LIN9_TX/ TC1_H_9_TR0/SCB2_CLK/SWJ_SWDIO_TMS	P2.9	SWDIO_TMS_PRM		
165	G15	P23_7/PWM1_22/PWM1_23_N/TC1_22_TR0/TC1_23_TR1/EXT_CLK/LIN9_EN/ TC1_H_9_TR1/SCB2_SEL0/CAL_SUP_NZ/SWJ_SWDOE_TDI/HIBER-NATE_WAKEUP[1]	P2.7	SWDOE_TDI_PRM		
166	K3	P24_0/EXT_CLK/SDHC_CARD_DETECT_N/LIN16_RX	P17.4	GPIO_P24_0		
167	L1	P24_1/SPIHB_CLK/SDHC_CARD_MECH_WRITE_PROT	P17.13	GM_CK_R		
168	L2	P24_2/SPIHB_RWDS/SDHC_CLK_CARD	P17.15	GM_RWDS_R		
169	L3	P24_3/SPIHB_SEL0/SDHC_CARD_CMD/LIN16_TX	P17.11	GM_CS#0_R		
170	M1	P24_4/SPIHB_SEL1/SDHC_CARD_IF_PWR_EN/LIN16_EN	P17.9	GM_CS#1_R		
171	M2	P25_0/SPIHB_DATA0/SDHC_CARD_DAT_3TO0_0	P17.7	GM_DQ0_R		
172	M3	P25_1/SPIHB_DATA1/SDHC_CARD_DAT_3TO0_1	P17.16	GM_DQ1_R		
173	N1	P25_2/SPIHB_DATA2/SDHC_CARD_DAT_3TO0_2	P17.5	GM_DQ2_R		
174	N2	P25_3/SPIHB_DATA3/SDHC_CARD_DAT_3TO0_3	P17.3	GM_DQ3_R		
175	N3	P25_4/SPIHB_DATA4/SDHC_CARD_DAT_7TO4_0	P17.14	GM_DQ4_R		
176	P1	P25_5/SPIHB_DATA5/SDHC_CARD_DAT_7TO4_1	P17.1	GM_DQ5_R		
177	P2	P25_6/SPIHB_DATA6/SDHC_CARD_DAT_7TO4_2	P17.10	GM_DQ6_R		
178	P3	P25_7/SPIHB_DATA7/SDHC_CARD_DAT_7TO4_3	P17.12	GM_DQ7_R		
179	Y8	P26_0/ETH1_REF_CLK	R144.2	GIG_ETH_REF_-CLK_R		
180	W8	P26_1/ETH1_TX_CTL	P11.5	GIG_ETH_TX_EN_C-TRL_R		
181	V8	P26_2/ETH1_TX_CLK	P11.4	GIG_ETH_TX_CLK_R		
182	Y9	P26_3/ETH1_TXD_0	P11.10	GIG_ETH_TX_D0_R		
183	W9	P26_4/ETH1_TXD_1	P11.11	GIG_ETH_TX_D1_R		
184	V9	P26_5/ETH1_TXD_2	P11.2	GIG_ETH_TX_D2_R		
185	Y10	P26_6/ETH1_TXD_3	P11.8	GIG_ETH_TX_D3_R		
186	W10	P26_7/ETH1_RXD_0	P11.9	GIG_ETH_RX_D0_R		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
187	V10	P27_0/ETH1_RXD_1	P11.7	GIG_ETH_RX_D1_R		
188	Y11	P27_1/ETH1_RXD_2	P11.6	GIG_ETH_RX_D2_R		
189	W11	P27_2/ETH1_RXD_3	P11.3	GIG_ETH_RX_D3_R		
190	V11	P27_3/ETH1_RX_CTL	P11.1	GIG_ETH_RX_DV_C-TRL_R		
191	W12	P27_4/ETH1_RX_CLK	P9.15	GIG_ETH_RX_CLK_R		
192	V12	P27_5/ETH1_MDIO	P9.16	GIG_ETH_MDIO_R		
193	W13	P27_6/ETH1_MDC	P9.14	GIG_ETH_MDC_R		
194	V13	P27_7/ETH1_ETH_TSU_TIMER_CMP_VAL	P12.1	GPIO_P27_7		
195	E16	P28_0/PWM1_63/PWM1_65_N/TC1_63_TR0/TC1_65_TR1/PWM1_H_12/ SCB10_RX/SCB10_MISO	P1.2	GPIO_P28_0		
196	D19	P28_1/PWM1_64/PWM1_63_N/TC1_64_TR0/TC1_63_TR1/PWM1_H_12_N/ SCB10_TX/SCB10_SDA/SCB10_MOSI/LIN17_RX	P6.5	BB_USER_BUT-TON_5		
197	D18	P28_2/PWM1_65/PWM1_64_N/TC1_65_TR0/TC1_64_TR1/TC1_H_12_TR0/ SCB10_RTS/SCB10_SCL/SCB10_CLK/LIN17_TX	P13.1	BB_USER_BUT-TON_4		
198	C20	P28_3/PWM1_66/PWM1_65_N/TC1_66_TR0/TC1_65_TR1/TC1_H_12_TR1/ SCB10_CTS/SCB10_SEL0/LIN17_EN	P6.4	BB_SPI0_WP		
199	C19	P28_4/PWM1_67/PWM1_66_N/TC1_67_TR0/TC1_66_TR1/SCB10_SEL1/ LIN18_RX	P6.3	BB_SPI0_HOLD		
200	B20	P28_5/PWM1_68/PWM1_67_N/TC1_68_TR0/TC1_67_TR1/SCB10_SEL2/ LIN18_TX	P6.2	BB_FRA_STBN		
201	B19	P28_6/PWM1_69/PWM1_68_N/TC1_69_TR0/TC1_68_TR1/SCB10_SEL3/ LIN18_EN	P6.1	BB_FRA_ERRN		
202	A19	P28_7/PWM1_70/PWM1_69_N/TC1_70_TR0/TC1_69_TR1/LIN19_RX	P13.11	BB_CAN6_WAKE		
203	A11	P29_0/PWM1_76/PWM1_75_N/TC1_76_TR0/TC1_75_TR1/LIN19_TX	P13.15	BB_CAN2_S		
204	B11	P29_1/PWM1_77/PWM1_76_N/TC1_77_TR0/TC1_76_TR1/LIN19_EN	P5.14	BB_CXPI_SELMS		
205	A10	P29_2/PWM1_78/PWM1_77_N/TC1_78_TR0/TC1_77_TR1	P4.7	BB_CAN1_S		
206	B10	P29_3/PWM1_79/PWM1_78_N/TC1_79_TR0/TC1_78_TR1	P4.3	BB_CXPI_RXD		
207	E10	P29_4/PWM1_80/PWM1_79_N/TC1_80_TR0/TC1_79_TR1	P5.9	BB_USER_LED6		
208	B9	P29_5/PWM1_81/PWM1_80_N/TC1_81_TR0/TC1_80_TR1	P4.8	BB_CXPI_NSLP		
209	C9	P29_6/PWM1_82/PWM1_81_N/TC1_82_TR0/TC1_81_TR1	P8.6	BB_GPIO_56_RESET		
210	E9	P29_7/PWM1_83/PWM1_82_N/TC1_83_TR0/TC1_82_TR1	P5.8	BB_USER_LED5		
211	C7	P30_0/PWM1_83/PWM1_83_N/TC1_83_TR0/TC1_83_TR1/SCB9_RTS/SCB9_SCL/ SCB9_CLK/TRIG_IN[34]	P5.6	BB_FRB_WAKE		
212	A6	P30_1/PWM1_82/PWM1_83_N/TC1_82_TR0/TC1_83_TR1/SCB9_CTS/SCB9_-SEL0/LIN16_RX/TRIG_IN[35]	P1.8	GPIO_P30_1		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
213	B6	P30_2/PWM1_81/PWM1_82_N/TC1_81_TR0/TC1_82_TR1/SCB9_SEL1/LIN16_TX/ CAN1_3_TX/TRIG_IN[36]	P14.14	BB_CAN9_WAKE		
214	C6	P30_3/PWM1_80/PWM1_81_N/TC1_80_TR0/TC1_81_TR1/SCB9_SEL2/LIN16_EN/ CAN1_3_RX/TRIG_IN[37]	P8.11	BB_FRB_STBN		
215	E7	P31_0/PWM1_79/PWM1_80_N/TC1_79_TR0/TC1_80_TR1/LIN17_RX	P5.7	BB_USER_LED4		
216	F7	P31_1/PWM1_78/PWM1_79_N/TC1_78_TR0/TC1_79_TR1/LIN17_TX	P1.12	GPIO_P31_1		
217	E6	P31_2/PWM1_77/PWM1_78_N/TC1_77_TR0/TC1_78_TR1/LIN17_EN	P5.5	BB_USER_LED3		
218	D2	P32_0/PWM1_76/PWM1_77_N/TC1_76_TR0/TC1_77_TR1/SCB10_RX/ SCB10_MISO/TRIG_IN[40]/ADC[0]_8	P3.15	BB_USER_BUT-TON_2		
219	D3	P32_1/PWM1_75/PWM1_76_N/TC1_75_TR0/TC1_76_TR1/SCB10_TX/ SCB10_SDA/SCB10_MOSI/TRIG_IN[41]/ADC[0]_9	P3.13	BB_USER_BUT-TON_3		
220	E5	P32_2/PWM1_74/PWM1_75_N/TC1_74_TR0/TC1_75_TR1/SCB10_RTS/ SCB10_SCL/SCB10_CLK/LIN18_RX/TRIG_IN[42]/ADC[0]_10	P3.16	BB_USER_LED2		
221	E1	P32_3/PWM1_73/PWM1_74_N/TC1_73_TR0/TC1_74_TR1/SCB10_CTS/SCB10_-SEL0/LIN18_TX/TRIG_IN[43]/ADC[0]_11	P14.5	BB_USER_LED0		
222	E2	P32_4/PWM1_72/PWM1_73_N/TC1_72_TR0/TC1_73_TR1/LIN10_RX/SCB10_-SEL1/LIN18_EN/TRIG_IN[44]/ADC[0]_12	P4.16	BB_LIN4_RXD		
223	E3	P32_5/PWM1_71/PWM1_72_N/TC1_71_TR0/TC1_72_TR1/LIN10_TX/SCB10_-SEL2/LIN19_RX/TRIG_IN[45]/ADC[0]_13	P5.1	BB_USER_LED1		
224	F3	P32_6/PWM1_70/PWM1_71_N/TC1_70_TR0/TC1_71_TR1/LIN10_EN/SCB10_-SEL3/LIN19_TX/CAN1_4_TX/TRIG_IN[46]/ADC[0]_14	P4.15	BB_CAN0_TXD		
225	F5	P32_7/PWM1_69/PWM1_70_N/TC1_69_TR0/TC1_70_TR1/LIN19_EN/ CAN1_4_RX/TRIG_IN[47]/ADC[0]_15	P5.4	BB_CAN0_RXD		
226	W18	P33_0/ETH0_REF_CLK	P2.12	GPIO_P33_0		
227	V17	P33_1/ETH0_TX_CTL/ETH1_TX_ER	P9.13	GIG_ETH_TX_ER_R		
228	W19	P33_2/ETH0_TX_CLK	P2.10	GPIO_P33_2		
229	V18	P33_3/ETH0_TXD_0/ETH1_TXD_4	P9.1	GPIO_P33_3	AUTO_ETH_TXD0_R	GIG_ETH_TX_D4_R
230	W20	P33_4/ETH0_TXD_1/ETH1_TXD_5	P9.11	GIG_ETH_TX_D5_R		
231	V20	P33_5/ETH0_TXD_2/ETH1_TXD_6	P9.9	GIG_ETH_TX_D6_R		
232	V19	P33_6/ETH0_TXD_3/ETH1_TXD_7	P9.10	GIG_ETH_TX_D7_R		
233	U20	P33_7/ETH0_RXD_0/ETH1_RXD_4	P9.7	GIG_ETH_RX_D4_R		
234	U19	P34_0/ETH0_RXD_1/ETH1_RXD_5	P9.8	GIG_ETH_RX_D5_R		
235	U18	P34_1/ETH0_RXD_2/ETH1_RXD_6	P9.12	GIG_ETH_RX_D6_R		
236	T20	P34_2/ETH0_RXD_3/ETH1_RXD_7	P9.5	GIG_ETH_RX_D7_R		
237	T19	P34_3/ETH0_RX_CTL/ETH1_RX_ER	P9.6	GIG_ETH_RX_ER_R		
238	T18	P34_4/ETH0_RX_CLK	P2.8	GPIO_P34_4		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
239	R20	P34_5/ETH0_MDIO	P2.11	GPIO_P34_5		
240	R19	P34_6/ETH0_MDC	P2.4	GPIO_P34_6		
241	R18	P34_7/ETH0_ETH_TSU_TIMER_CMP_VAL	P2.2	GPIO_P34_7		
242	F15	VCCD		CPU_VCCD		
243	R6	VCCD		CPU_VCCD		
244	R15	VCCD		CPU_VCCD		
245	F6	VCCD		CPU_VCCD		
246	N6	VDDA		CPU_VDDA		
247	F8	VDDD		CPU_VDDD		
248	F9	VDDD		CPU_VDDD		
249	H15	VDDD		CPU_VDDD		
250	J15	VDDD		CPU_VDDD		
251	K15	VDDD		CPU_VDDD		
252	M15	VDDD		CPU_VDDD		
253	L15	VDDD		CPU_VDDD		
254	N15	VDDD		CPU_VDDD		
255	R12	VDDD		CPU_VDDD		
256	R13	VDDD		CPU_VDDD		
257	F11	VDDIO_1		CPU_VDDIO1		
258	F12	VDDIO_1		CPU_VDDIO1		
259	F13	VDDIO_1		CPU_VDDIO1		
260	F10	VDDIO_1		CPU_VDDIO1		
261	R8	VDDIO_2		CPU_VDDIO2		
262	N8	VSSA		AGND		
263	A1	VSSD		DGND		
264	A20	VSSD		DGND		
265	C3	VSSD		DGND		
266	C10	VSSD		DGND		
267	C18	VSSD		DGND		
268	H9	VSSD		DGND		
269	H10	VSSD		DGND		
270	H11	VSSD		DGND		
271	H12	VSSD		DGND		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
272	H13	VSSD		DGND		
273	J9	VSSD		DGND		
274	J10	VSSD		DGND		
275	J11	VSSD		DGND		
276	J12	VSSD		DGND		
277	J13	VSSD		DGND		
278	J18	VSSD		DGND		
279	K9	VSSD		DGND		
280	K10	VSSD		DGND		
281	K11	VSSD		DGND		
282	K12	VSSD		DGND		
283	K13	VSSD		DGND		
284	K18	VSSD		DGND		
285	L9	VSSD		DGND		
286	L10	VSSD		DGND		
287	L11	VSSD		DGND		
288	L12	VSSD		DGND		
289	L13	VSSD		DGND		
290	M9	VSSD		DGND		
291	Y20	VSSD		DGND		
292	Y1	VSSD		DGND		
293	V15	VSSD		DGND		
294	V4	VSSD		DGND		
295	V3	VSSD		DGND		
296	N12	VSSD		DGND		
297	M13	VSSD		DGND		
298	M12	VSSD		DGND		
299	M11	VSSD		DGND		
300	M10	VSSD		DGND		
301	N13	VSSD_1		DGND		
302	L20	VSSD_2		DGND		
303	H6	VDDIO_3		CPU_VDDIO3		
304	J6	VDDIO_3		CPU_VDDIO3		

Table 4-1. Device Port Pin Connections on CPU Board *(continued)*

Pin Order	Pad	Pin Text	Test Point	Connection 1	Connection 2	Connection 3
305	K6	VDDIO_3		CPU_VDDIO3		
306	L6	VDDIO_3		CPU_VDDIO3		
307	R9	VDDIO_4		CPU_VDDIO4		
308	R10	VDDIO_4		CPU_VDDIO4		
309	R11	VDDIO_4		CPU_VDDIO4		
310	M6	VREFH		CPU_VDDA_R		
311	M8	VREFL		AGND_R		
312	P20	VSSD_2		DGND		
313	J8	VSSIO_3		DGND		
314	K8	VSSIO_3		DGND		
315	L8	VSSIO_3		DGND		
316	H8	VSSIO_3		DGND		
317	N10	VSSIO_4		DGND		
318	N11	VSSIO_4		DGND		
319	N9	VSSIO_4		DGND		
320	K20	XRES		CPU_XRES		

The first column in Table 4-1 lists the pin number on the MCU, followed by pad information and then the port pin name.

For each pin, the connected peripheral or net on the CPU / Base board is depicted by the Connection-x column.

The Test Point column indicates the place where the signal can be probed on the CPU board. Refer to the schematics / component assembly below to locate them. The ones named in the format Pxx.y, refer to the pin-y on the '8 x 2' Pxx header.

If the Test Point column is empty for a pin, it indicates that the signal is unavailable on a test point. Refer to the schematics for more information.

For details on the alternate functionality of each MCU pin, see the device datasheet.

Note:

If there are pins with more than one connection, make sure that no two peripherals are driven at the same time. The unused peripheral jumpers must be disconnected before using the other connection.

4.1.3 Reset Switch

The correspondence between the Reset switch and port number is given in Table 4-2.

Table 4-2. Reset Switch

Switch	Part No.	Port Name
Reset Switch	SW3	XRES

4.1.4 User Switch

The correspondence between the User switch and port number is given in Table 4-3.

Table 4-3. User Switch

Switch	Part No.	Port Name
User Switch	SW1	P21.4

4.1.5 User LED

The correspondence between the User LED and port number is given in Table 4-4.

Table 4-4. User LED

Switch	Part No.	Port Name
User LED	LD1	P23.2

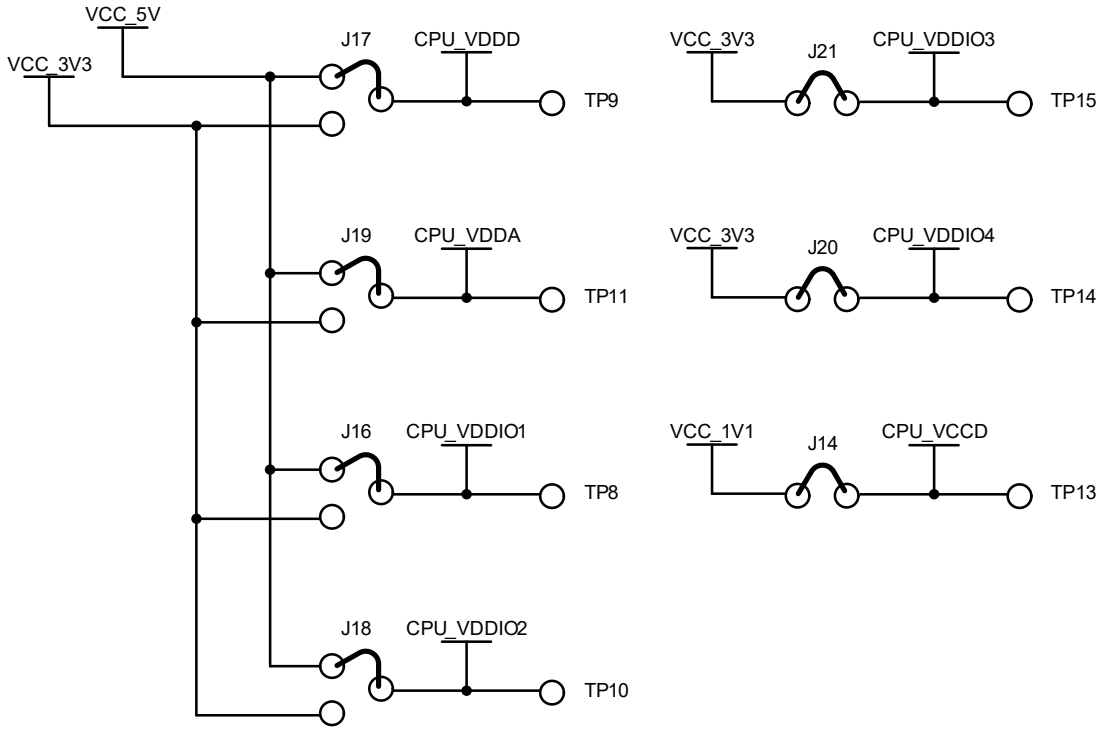
4.2 Power Supply Settings

Power supply settings are shown in Table 4-5 and Figure 4-1.

Table 4-5. Power Supply Jumpers Settings

Jumper	Pin	MCU Power	Remarks
J17	1-2 (default)	VDDD = +5.0 V	
	2-3	VDDD = +3.3 V	
J19	1-2 (default)	VDDA = +5.0 V	
	2-3	VDDA = +3.3 V	
J16	1-2 (default)	VDDIO_1 = +5.0 V	
	2-3	VDDIO_1 = +3.3 V	
J18	1-2 (default)	VDDIO_2 = +5.0 V	
	2-3	VDDIO_2 = +3.3 V	
J21	1-2 (default)	VDDIO_3 = +3.3 V	
J20	1-2 (default)	VDDIO_4 = +3.3 V	
J14	1-2 (default)	VCCD = +1.1 V	

Figure 4-1. Power Supply Jumpers Settings



4.3 External Power Supply Control Signals Settings

Jumper settings of the external power supply control signals from MCU are shown in Table 4-6.

Table 4-6. External Power Supply Control Signals Jumper Settings

Jumpers Name	PASS Transistor	S6BP501A	Remarks
EXT_PS_CTL0	J11	J6	J11 open (default)
			J6 closed (default)
EXT_PS_CTL1	J8	J9	J8 open (default)
			J9 closed (default)
EXT_PS_CTL2	-	R11	Connected a 0-ohm resistor (R11)

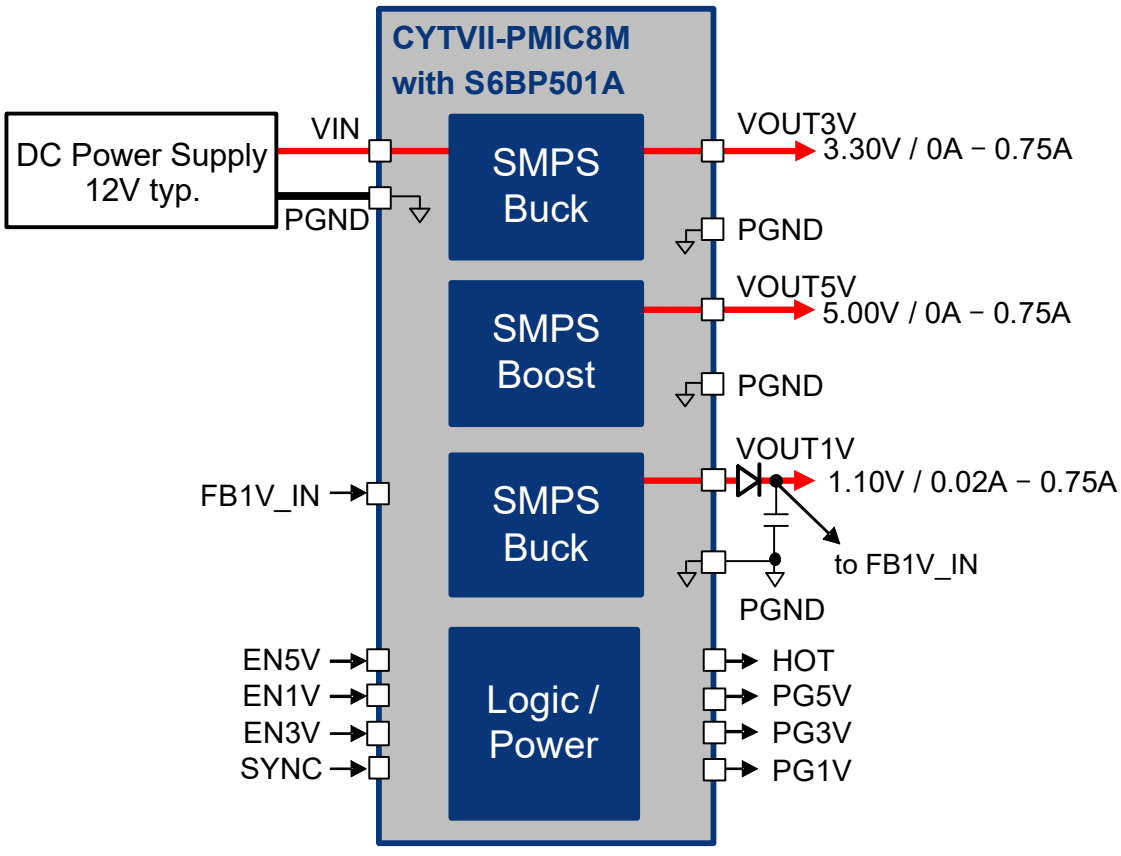
5. Power Management IC (PMIC)

5.1 Power Management IC (PMIC) Module

5.1.1 PMIC Module - CYTVII-PMIC8M

CYTVII-PMIC8M is the PMIC module for the power block of an automotive application with CYT4B Series MCU. The PMIC module implements the Cypress PMIC S6BP501A and is optimized for power supply of CYT4B Series MCU. 1.1-V output of the supply to VCCD of CYT4B Series MCU needs external schottky barrier diode (SBD), output capacitor, and constant load current no less than 20 mA.

Figure 5-1. Evaluation Board Block Diagram



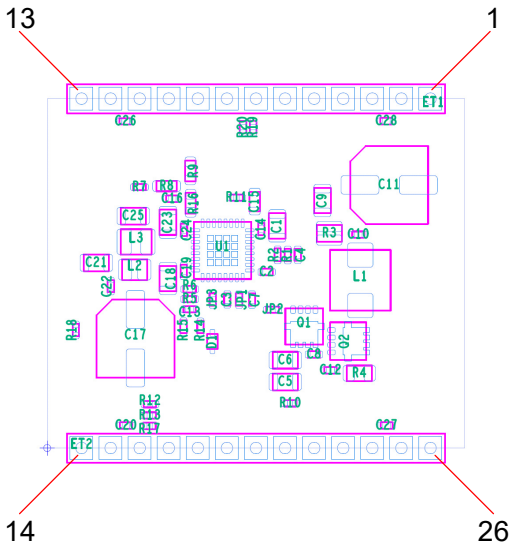
*SMPS: Switching Mode Power Supply

5.1.2 Input / Output Pin Descriptions

Table 5-1. Input / Output Pin Descriptions

Connector Symbol		I/O	Function Description
1, 2	VOUT3V	O	3.3 V power rail output terminal (0 A - 0.75 A)
3, 4	PGND	O	Ground terminal
5	SYNC	I	Mode setting or external clock input terminal Refer to the S6BP501A datasheet
6	PG1V	O	Power good terminal of 1.1 V power rail
7	PG3V	O	Power good terminal of 3.3 V power rail
8	PG5V	O	Power good terminal of 5 V power rail
9	FB1V_IN	I	Feed-back terminal for 1.1 V power rail
10, 11	PGND	–	Ground terminal
12, 13	VOUT1V	O	1.1 V output terminal (0 A - 0.75 A)
14, 15	VOUT5V	O	5 V output terminal (0 A - 0.75 A)
16, 17	PGND	–	Ground terminal
18	HOT	O	Thermal warning output terminal
19	EN5V	I	5 V power rail output enable terminal
20	EN3V	I	3.3 V power rail output enable terminal
21	EN1V	I	1.1 V power rail output enable terminal
22	N.C.	N.C.	No connection
23, 24	PGND	–	Ground terminal
25, 26	VIN	I	DC power supply terminal (4.5 V-42 V, 12 V typ.)

Figure 5-2. Pin Layout



A. Schematics of CPU Board

This appendix contains the schematics of CYTVII-B-H-8M-320-CPU board.

Figure A-1. Block Diagram

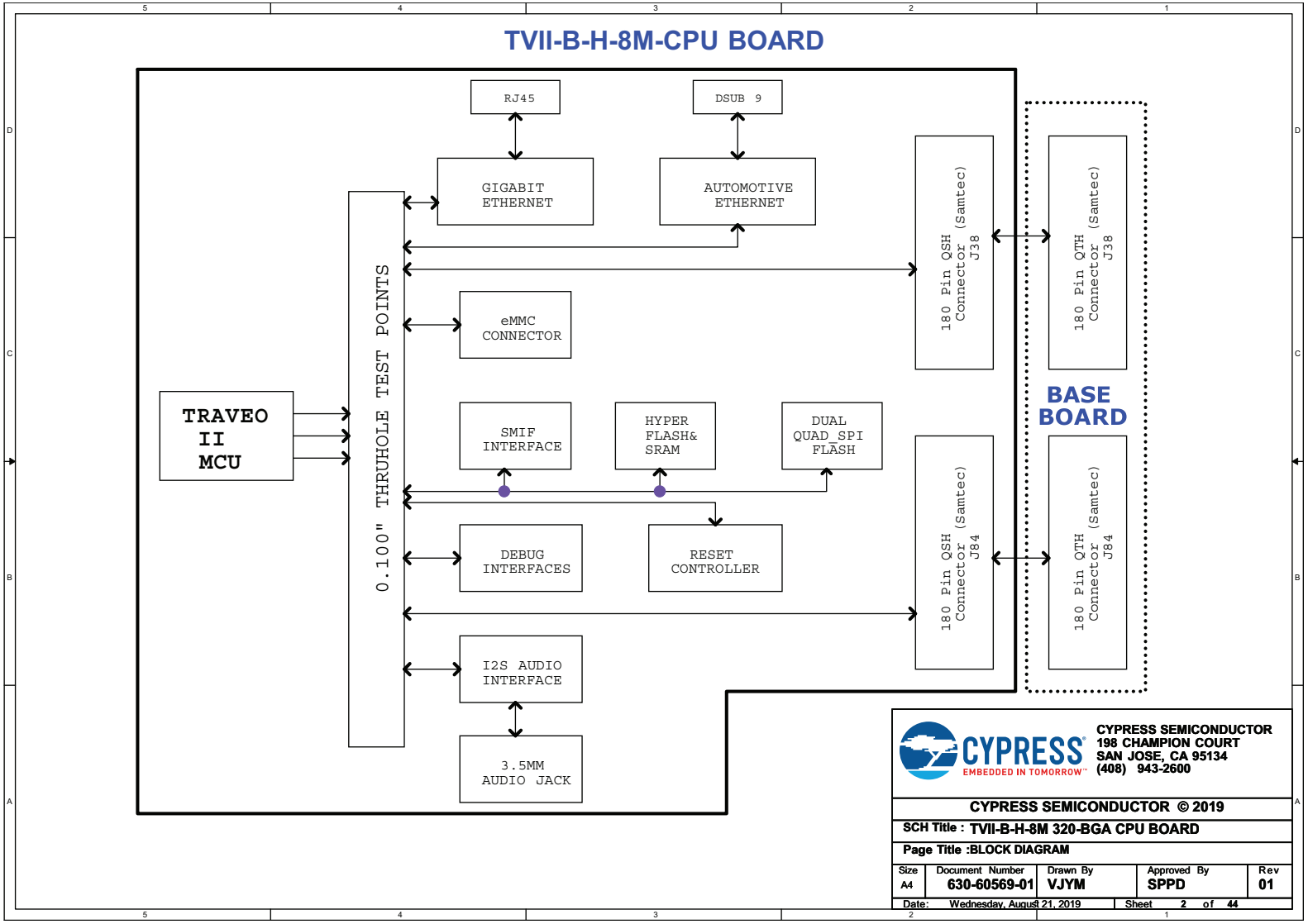


Figure A-2. Power Architecture

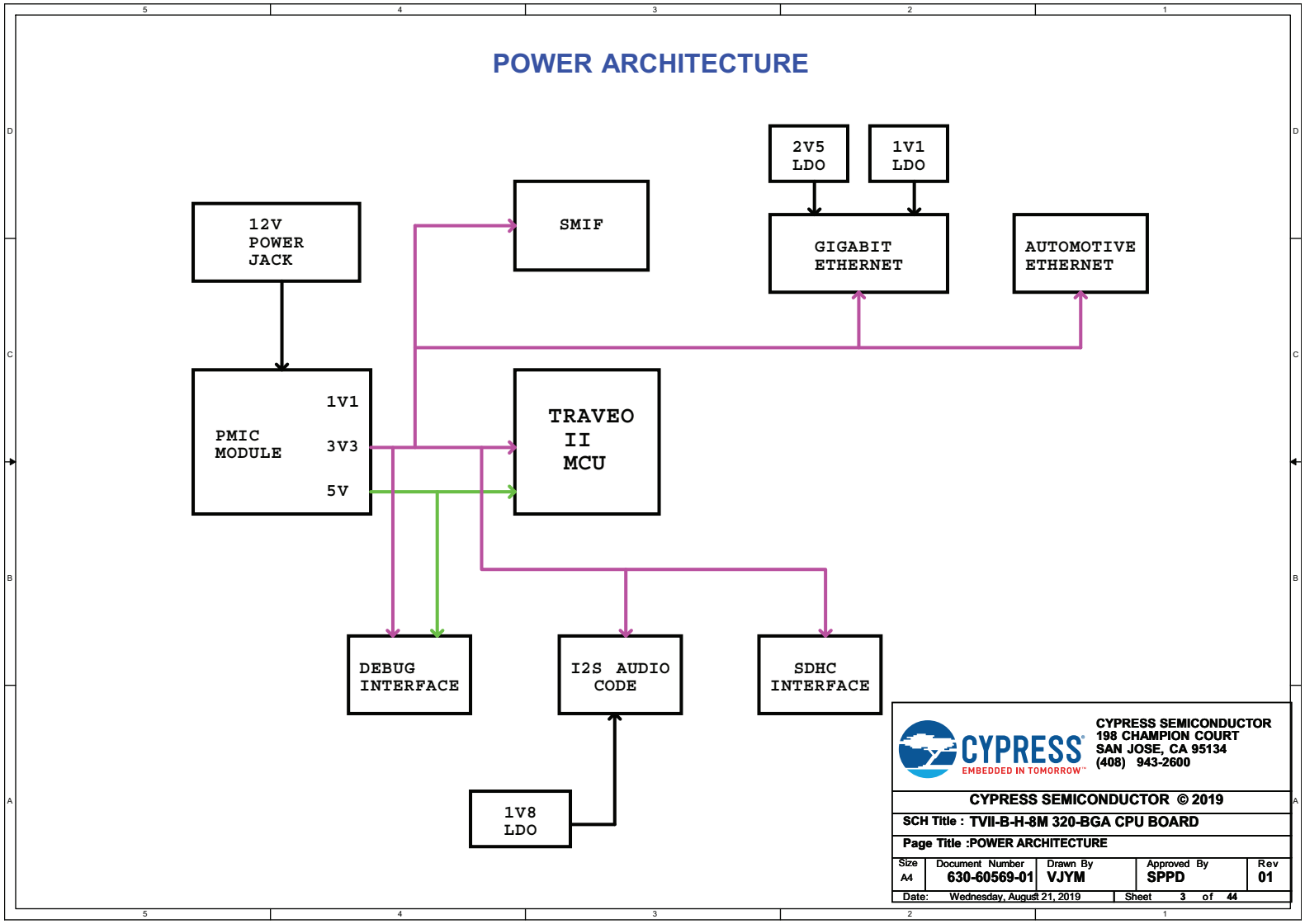


Figure A-3. Power Input-1

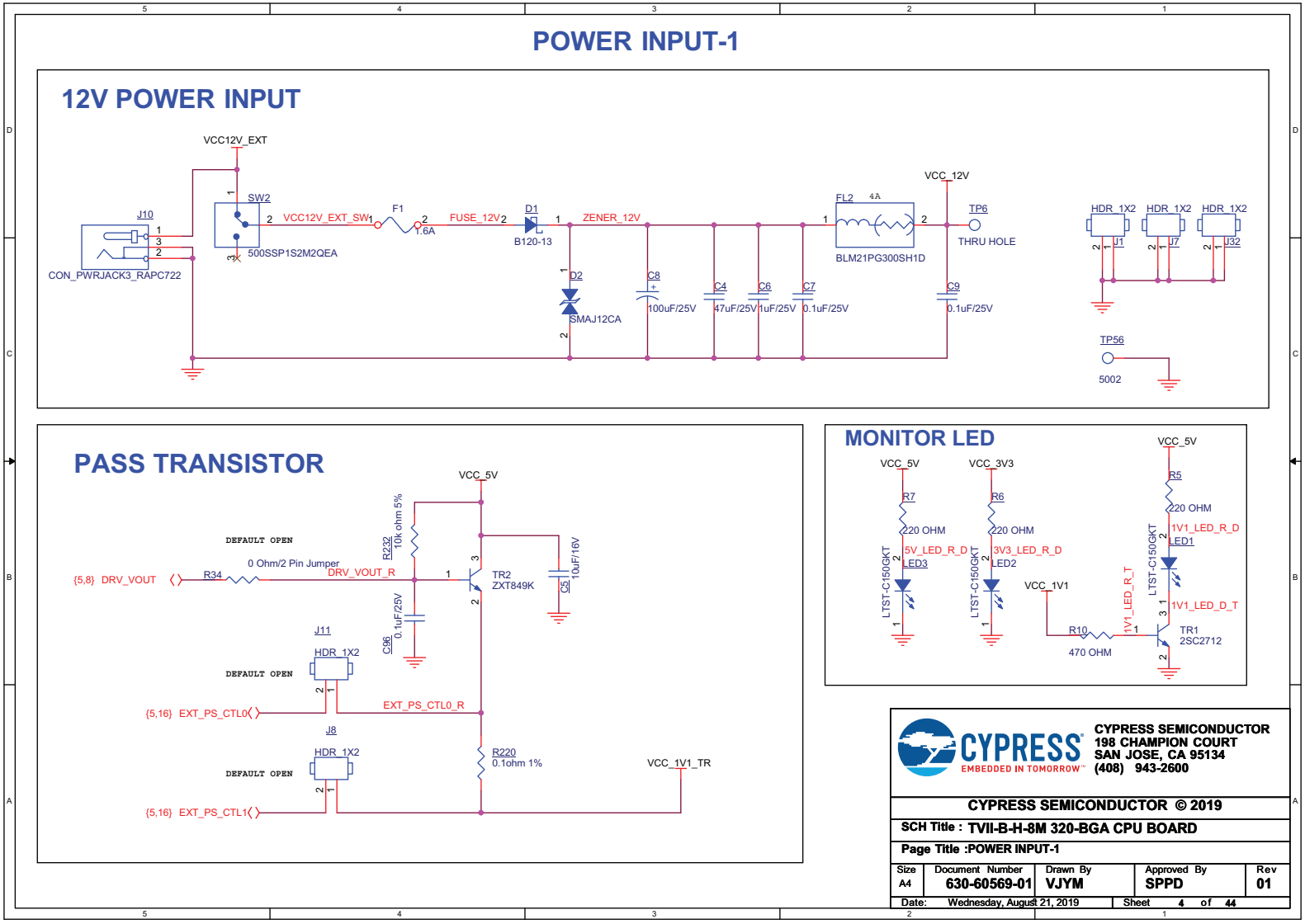


Figure A-4. Power Input-2

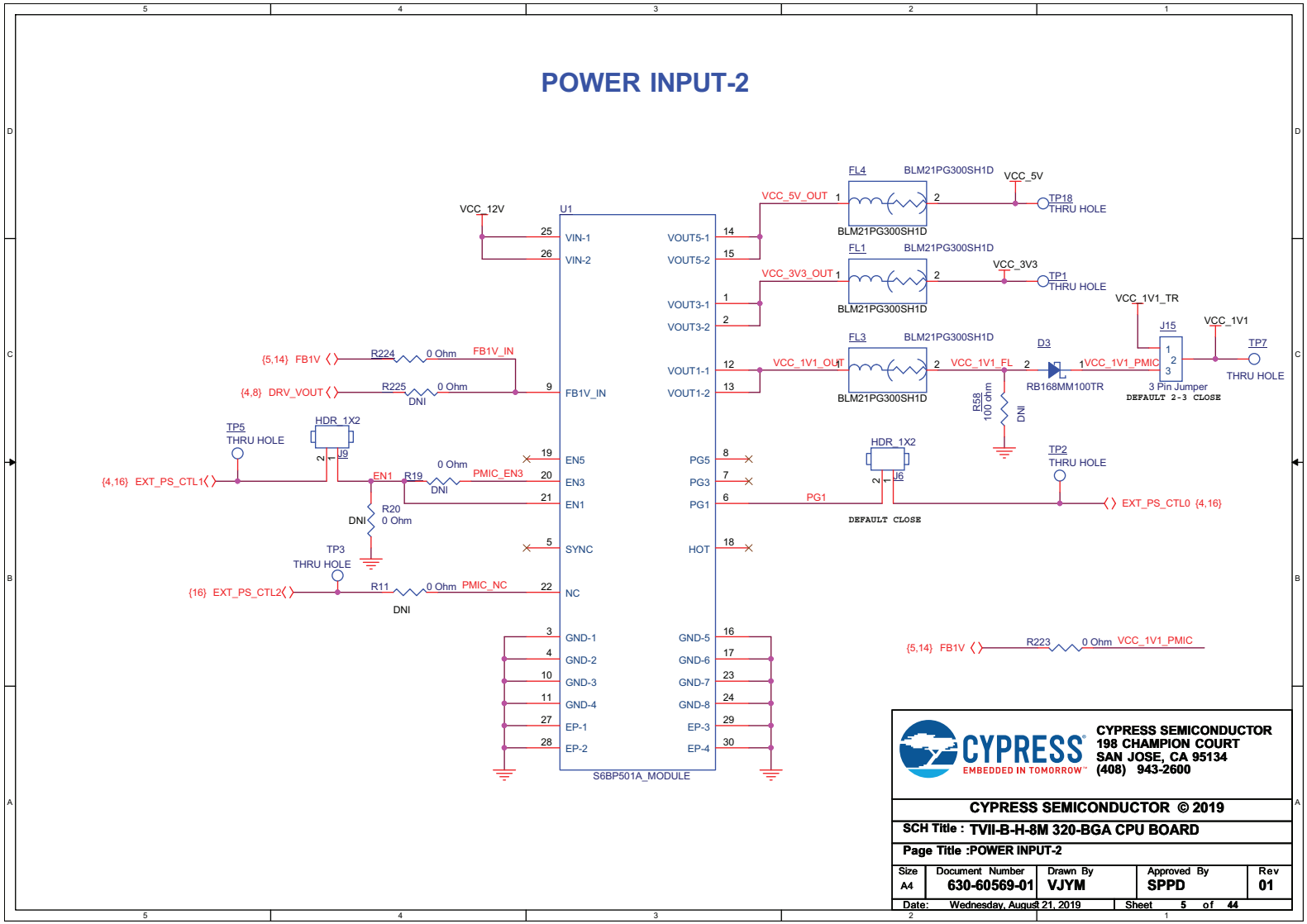


Figure A-5. Power Input-3

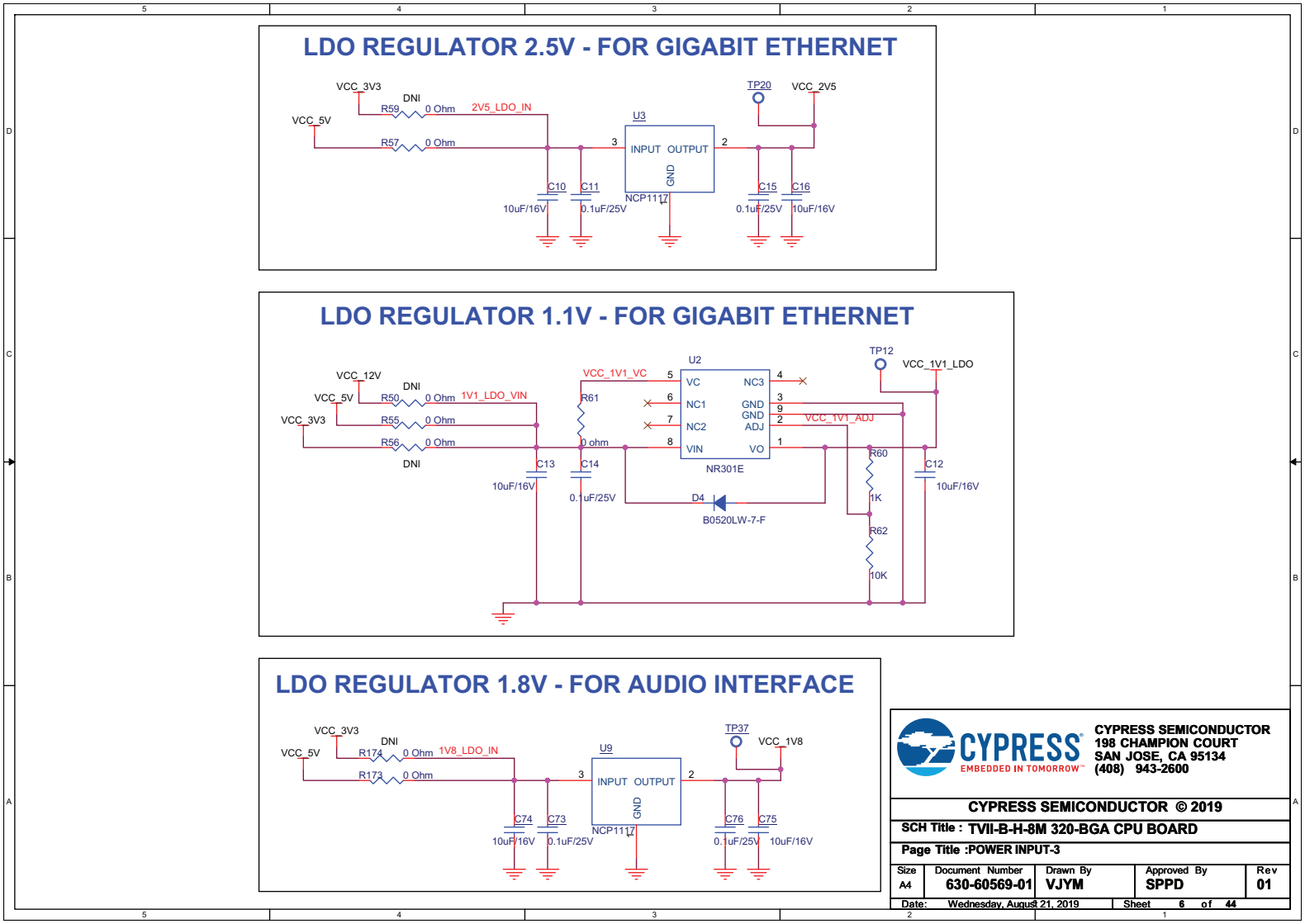


Figure A-6. MCU Power Rail-Supply Select

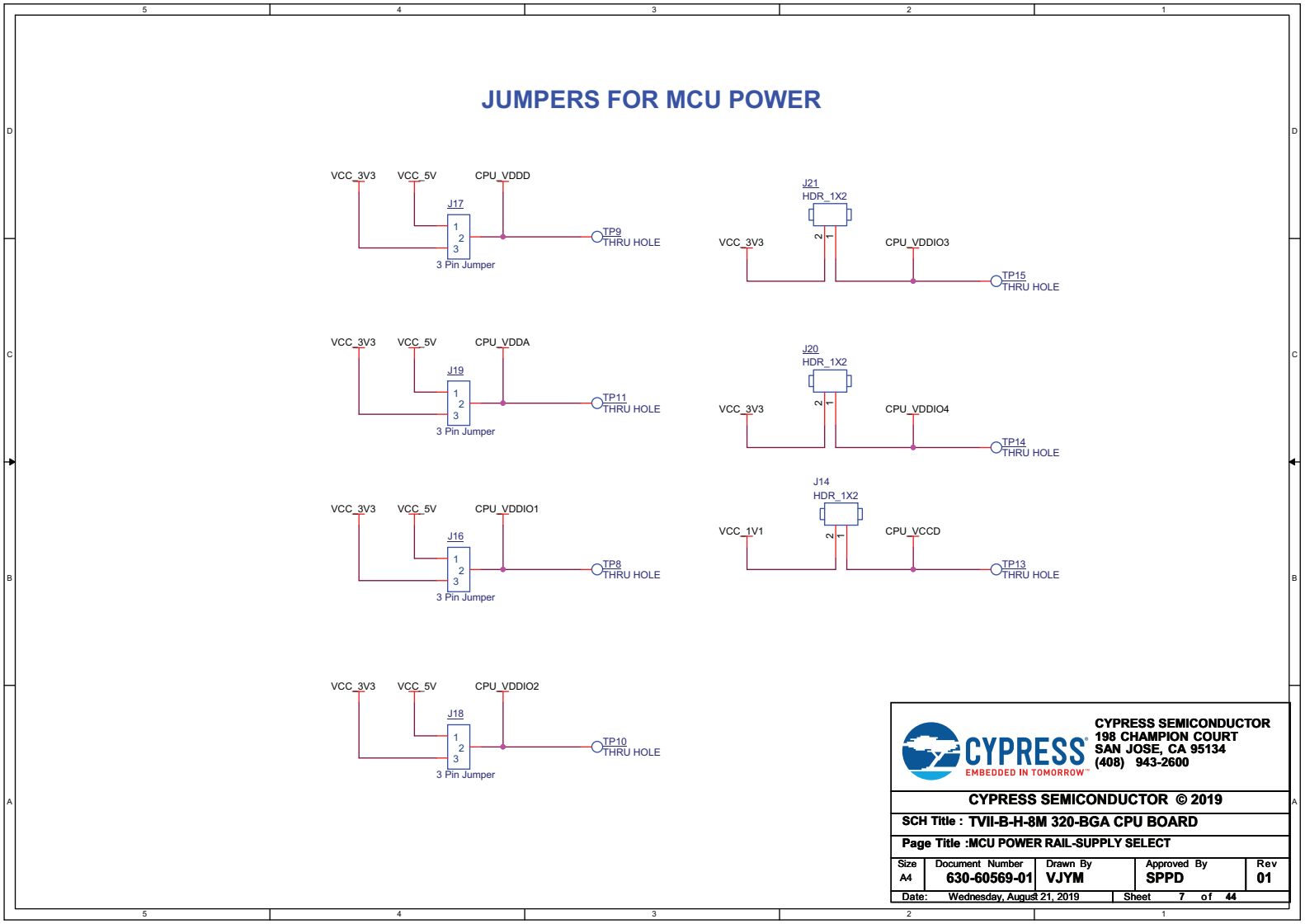


Figure A-7. TVII-B-H-8M-320-BGA

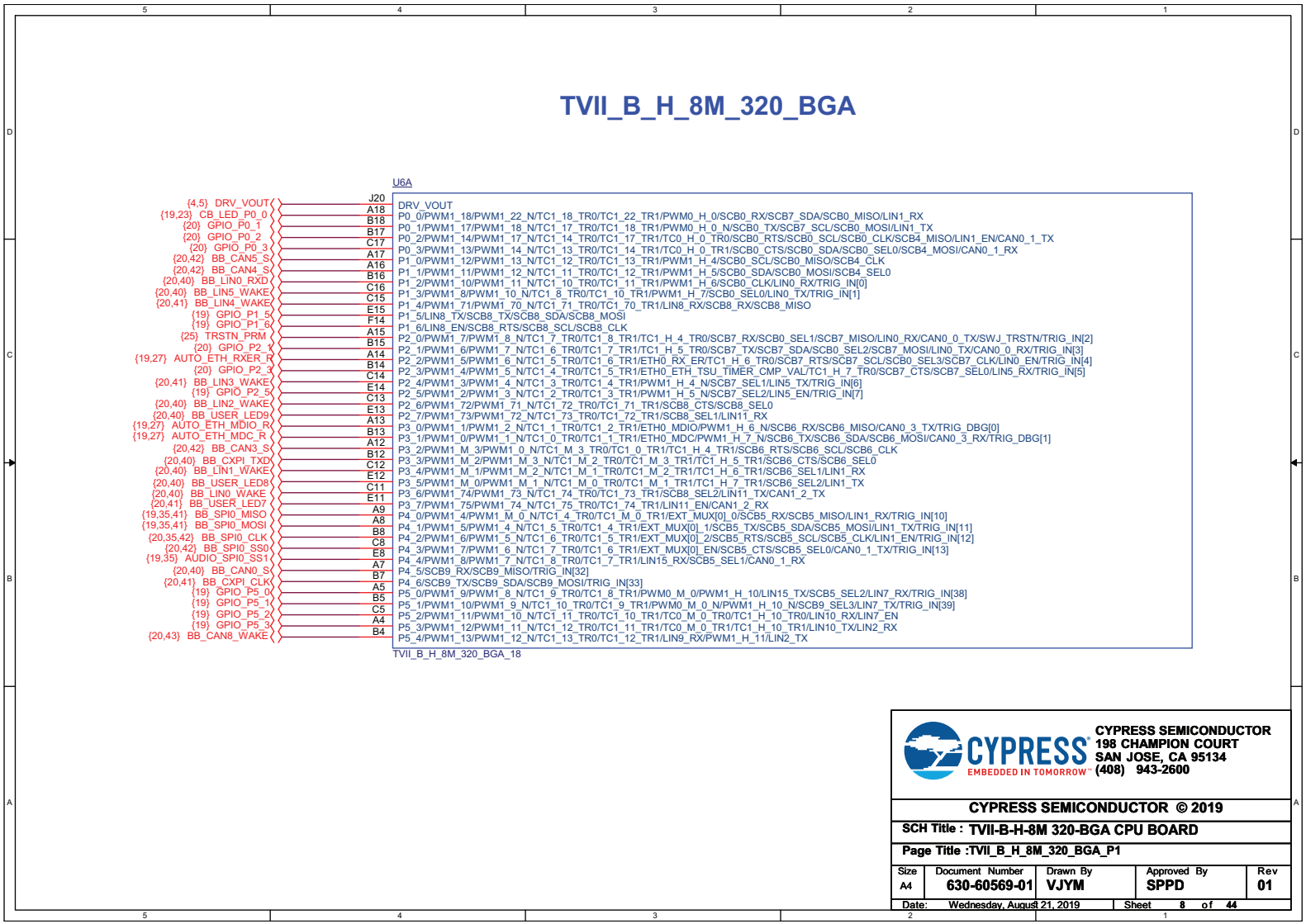


Figure A-8. TVII-B-H-8M-320-BGA

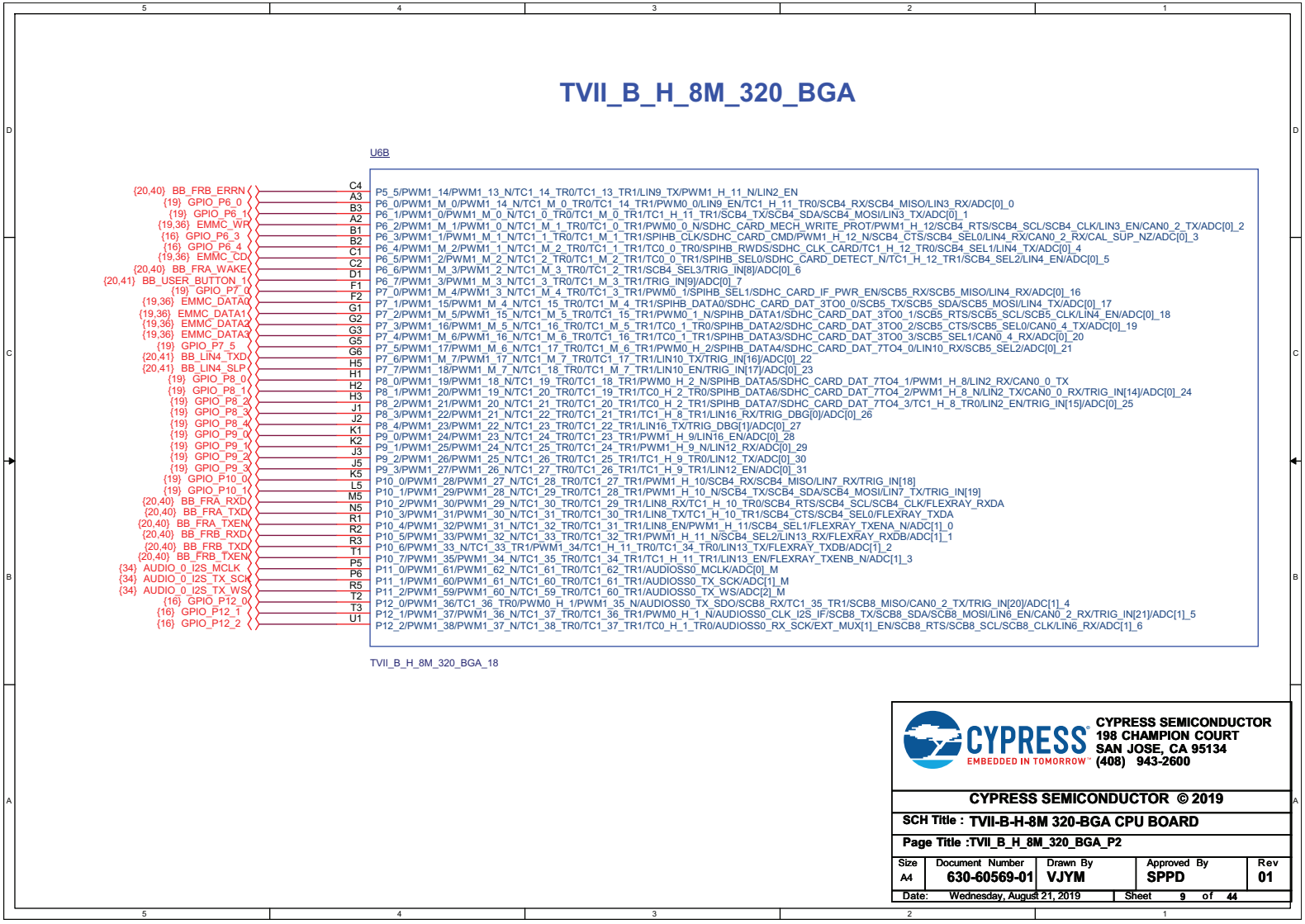


Figure A-9. TVII-B-H-8M-320-BGA

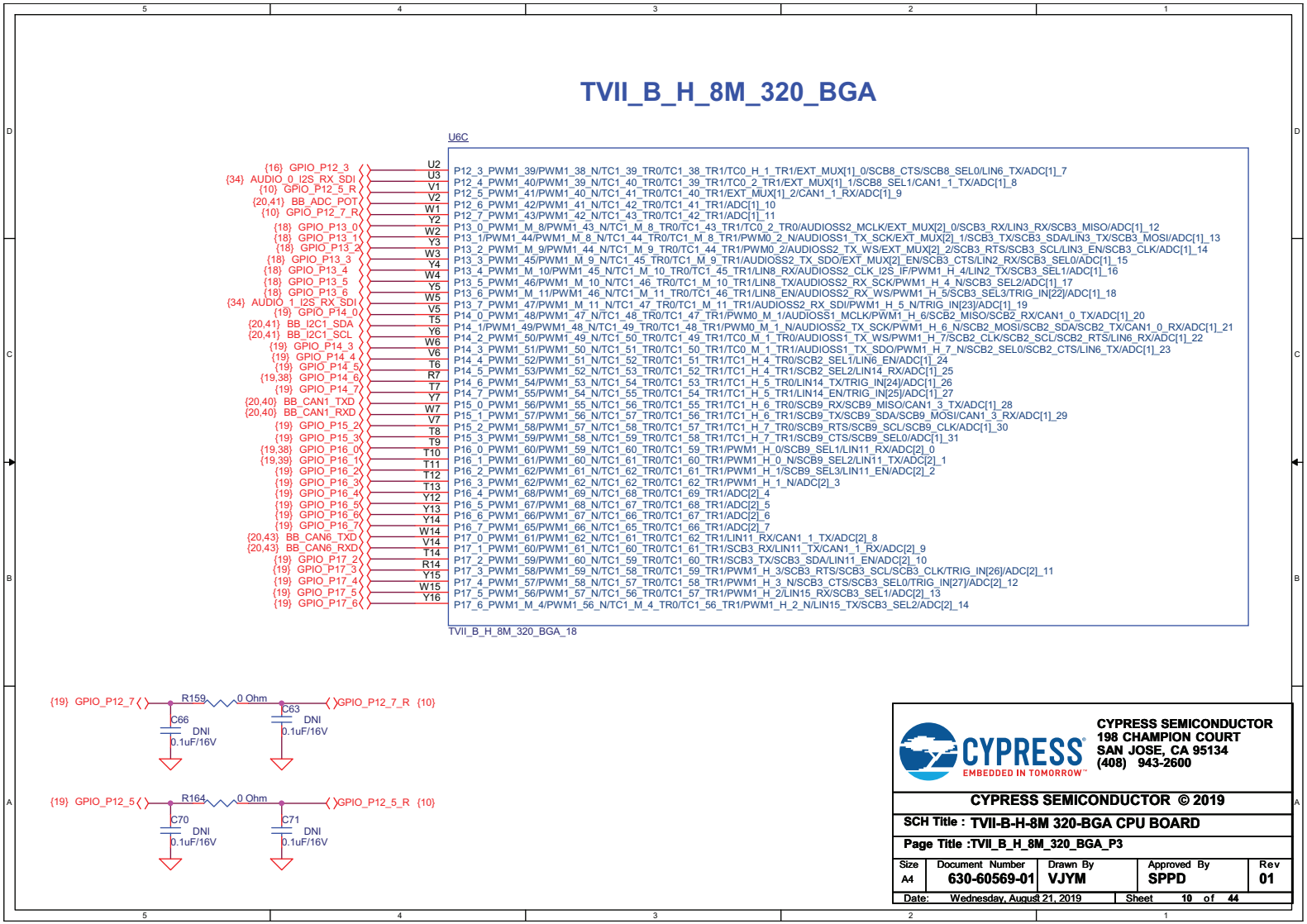


Figure A-10. TVII-B-H-8M-320-BGA

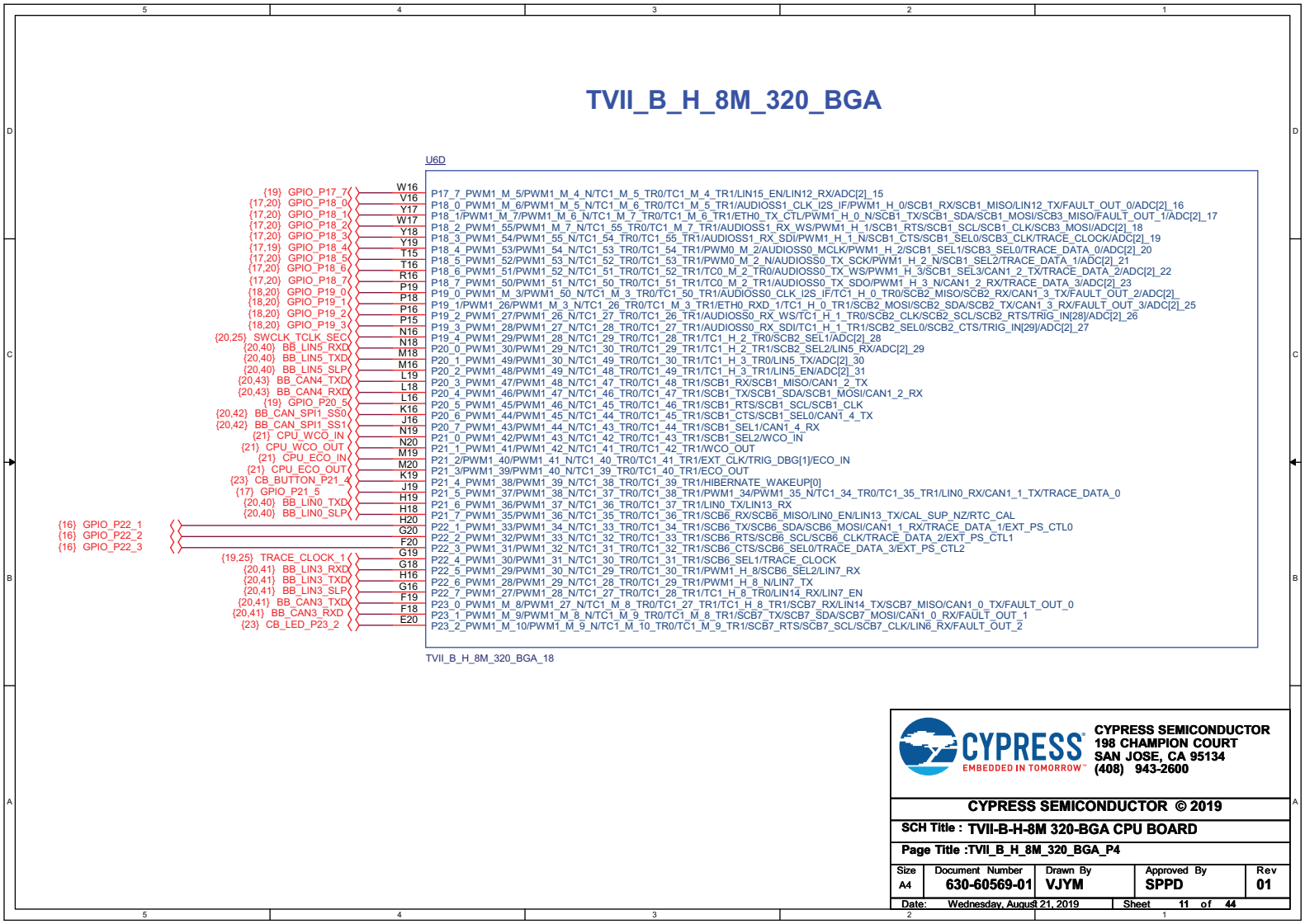


Figure A-11. TVII-B-H-8M-320-BGA

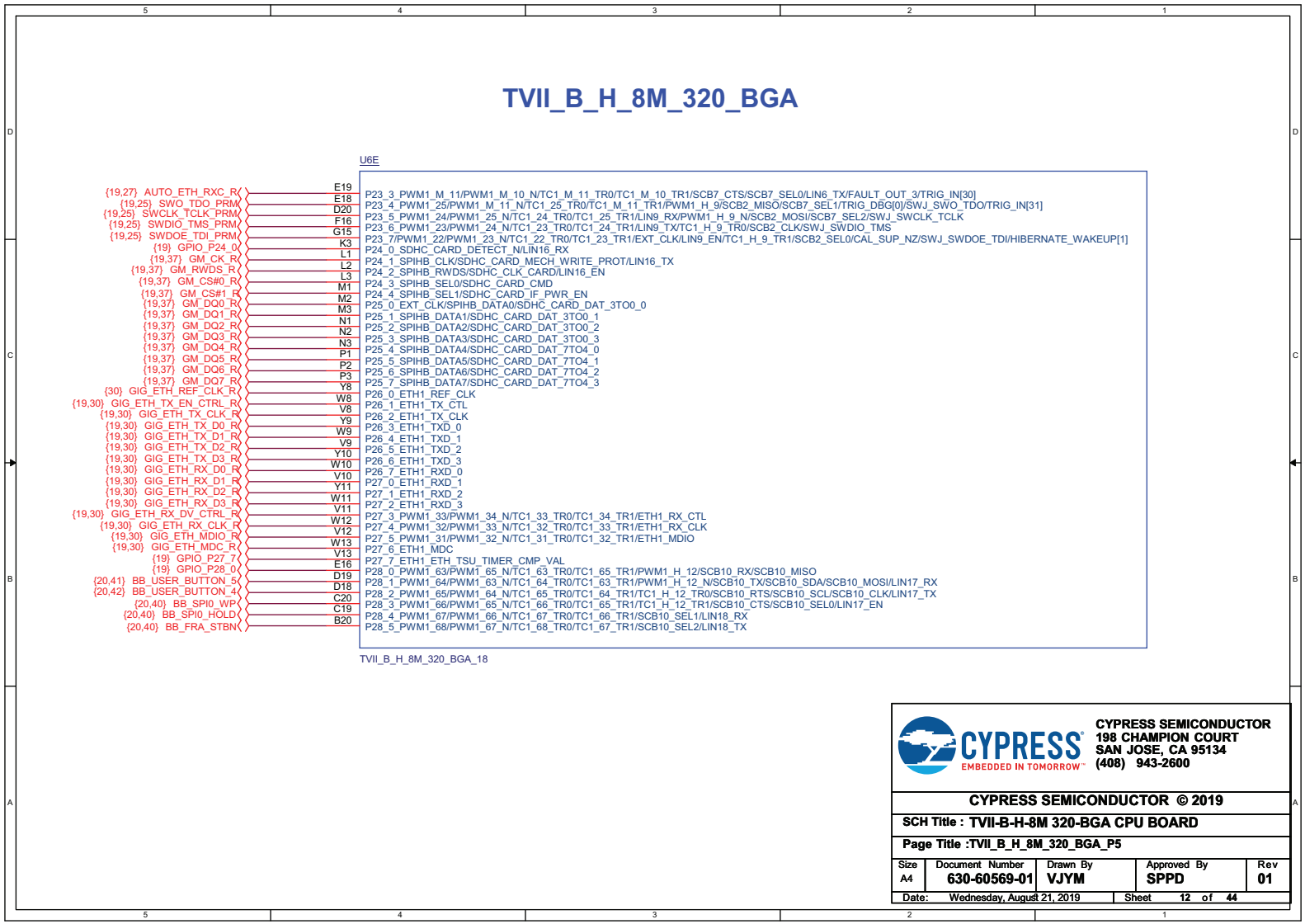


Figure A-12. TVII-B-H-8M-320-BGA

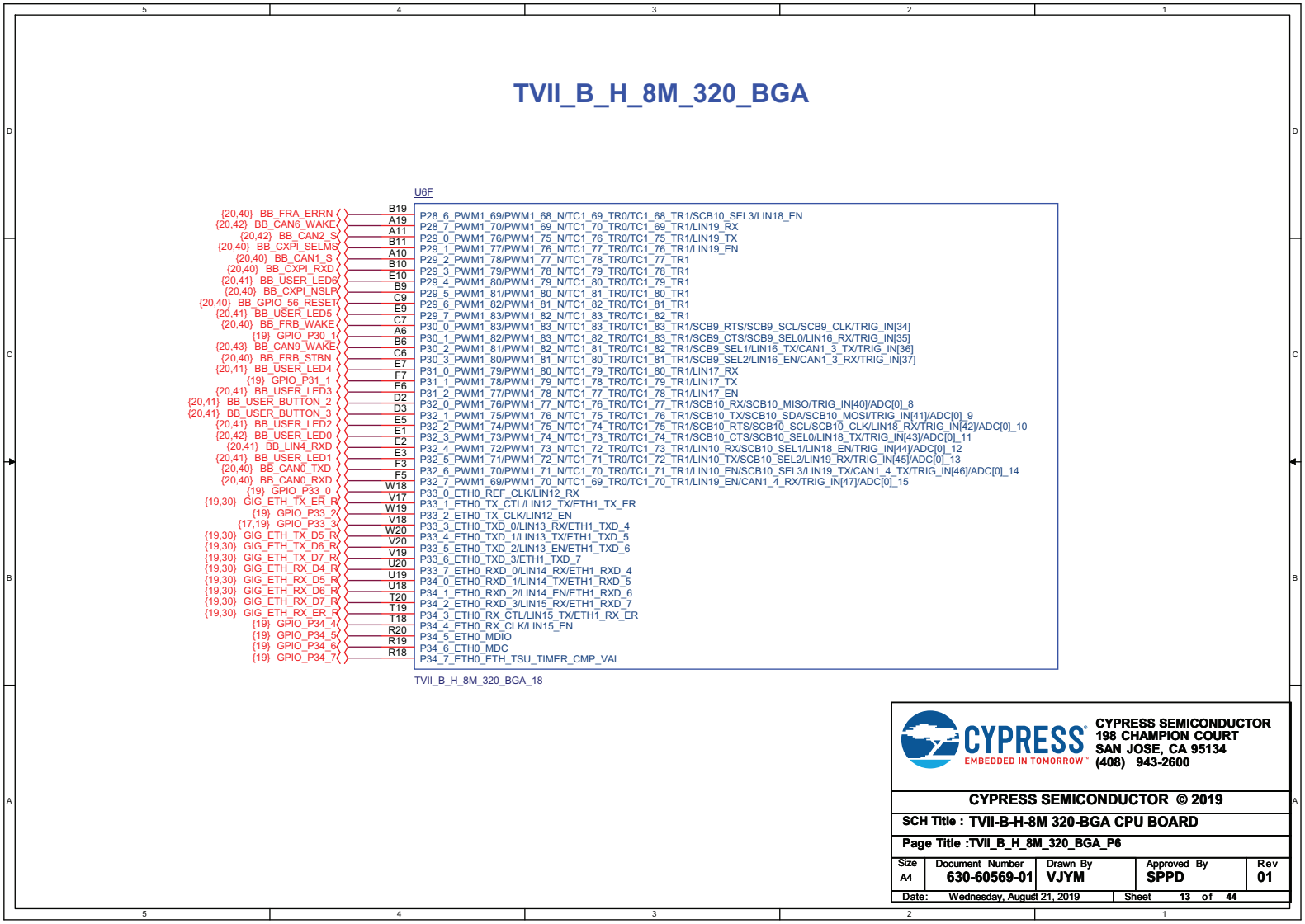


Figure A-13. TVII-B-H-8M-320-BGA

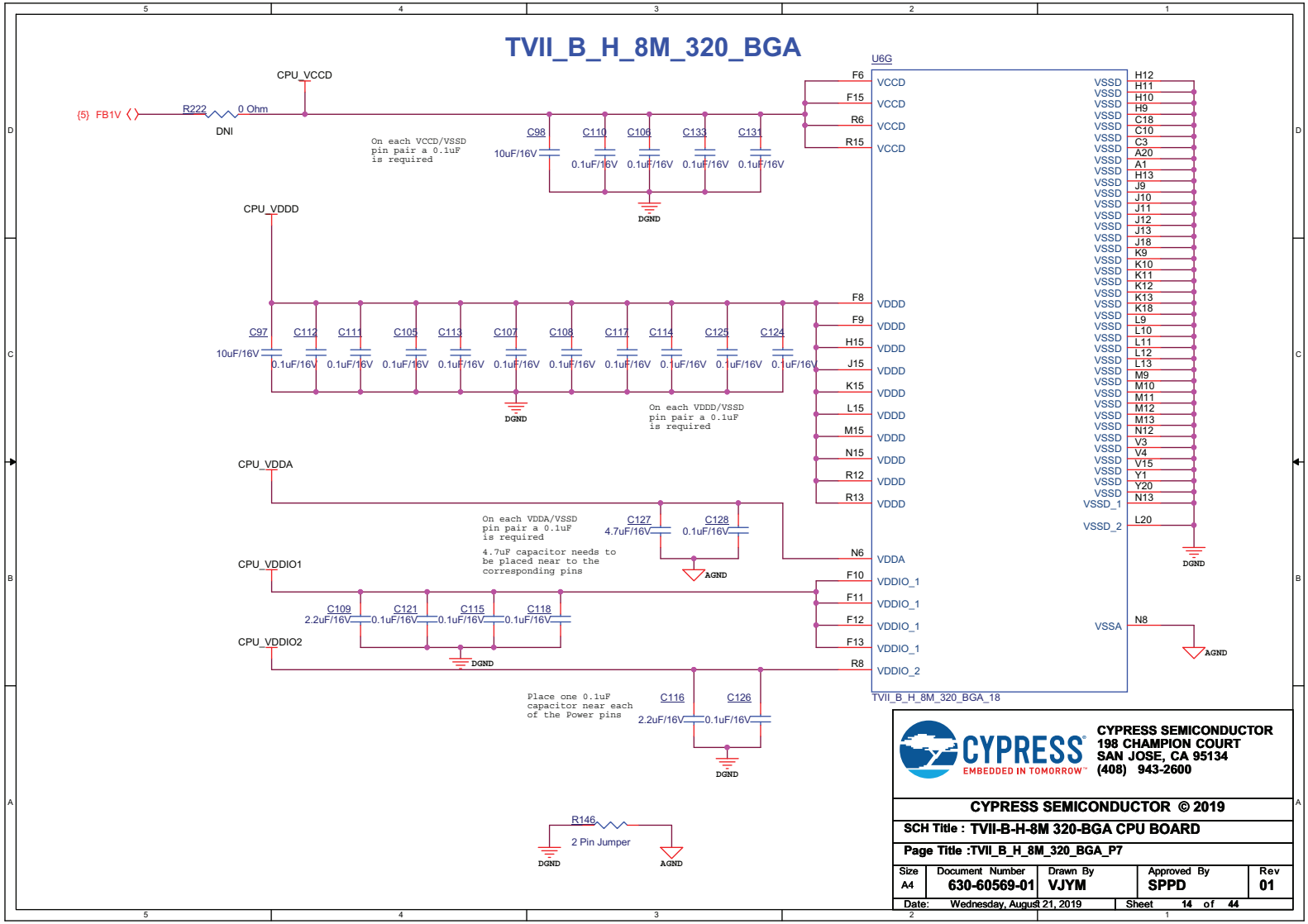


Figure A-14. TVII-B-H-8M-320-BGA

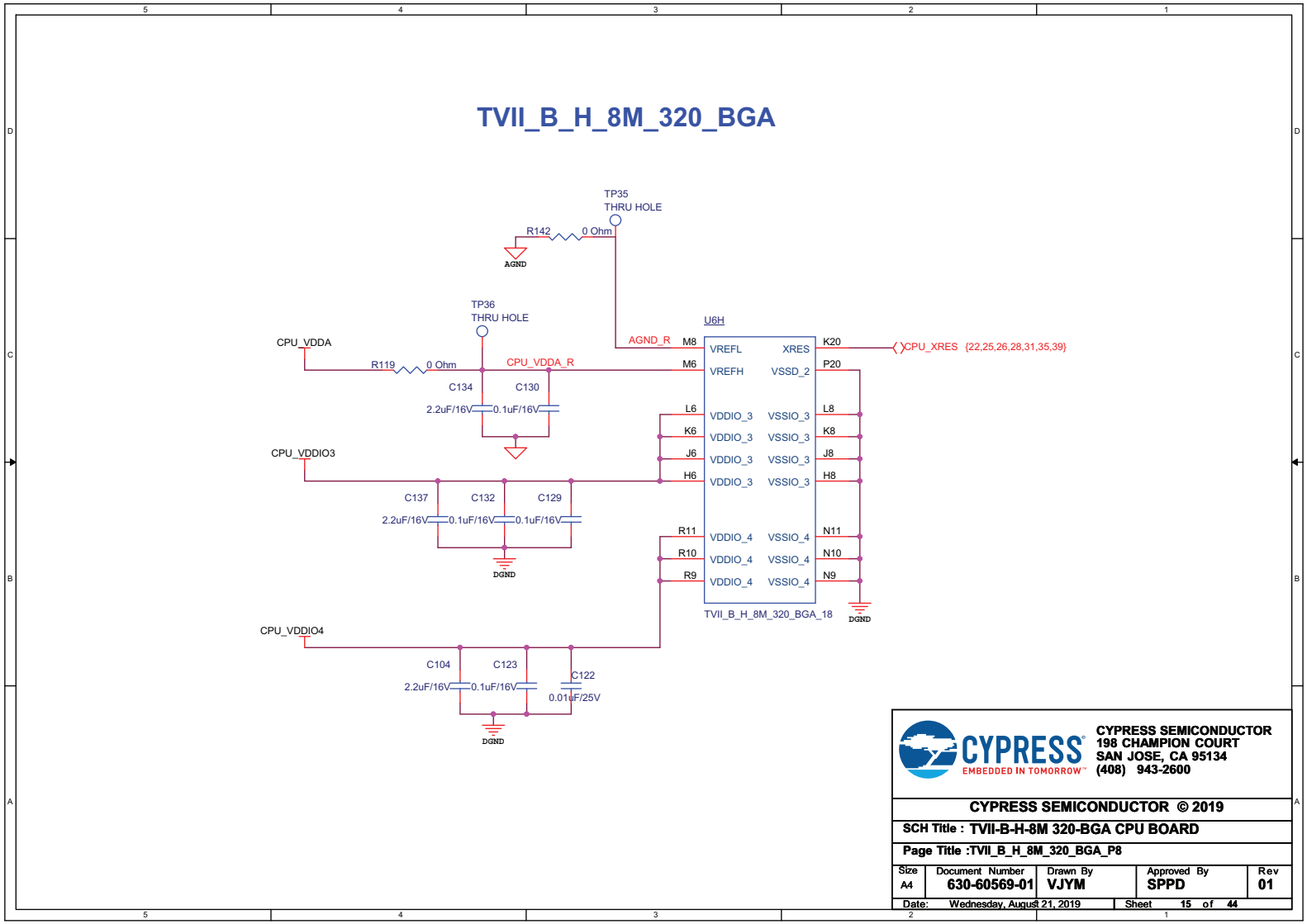


Figure A-15. MCU Port Pin Mux Options

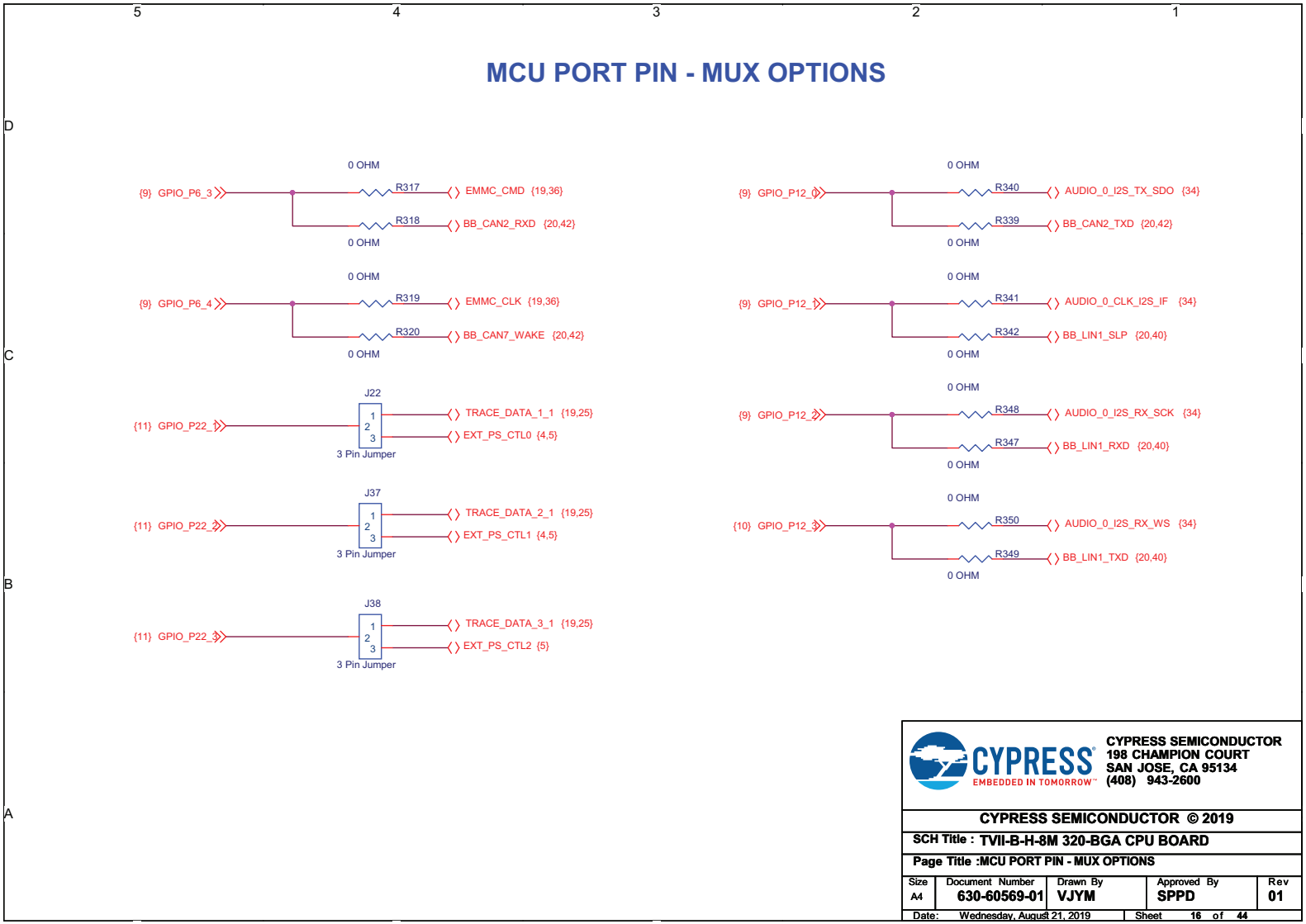


Figure A-16. MCU Port Pin Mux Options

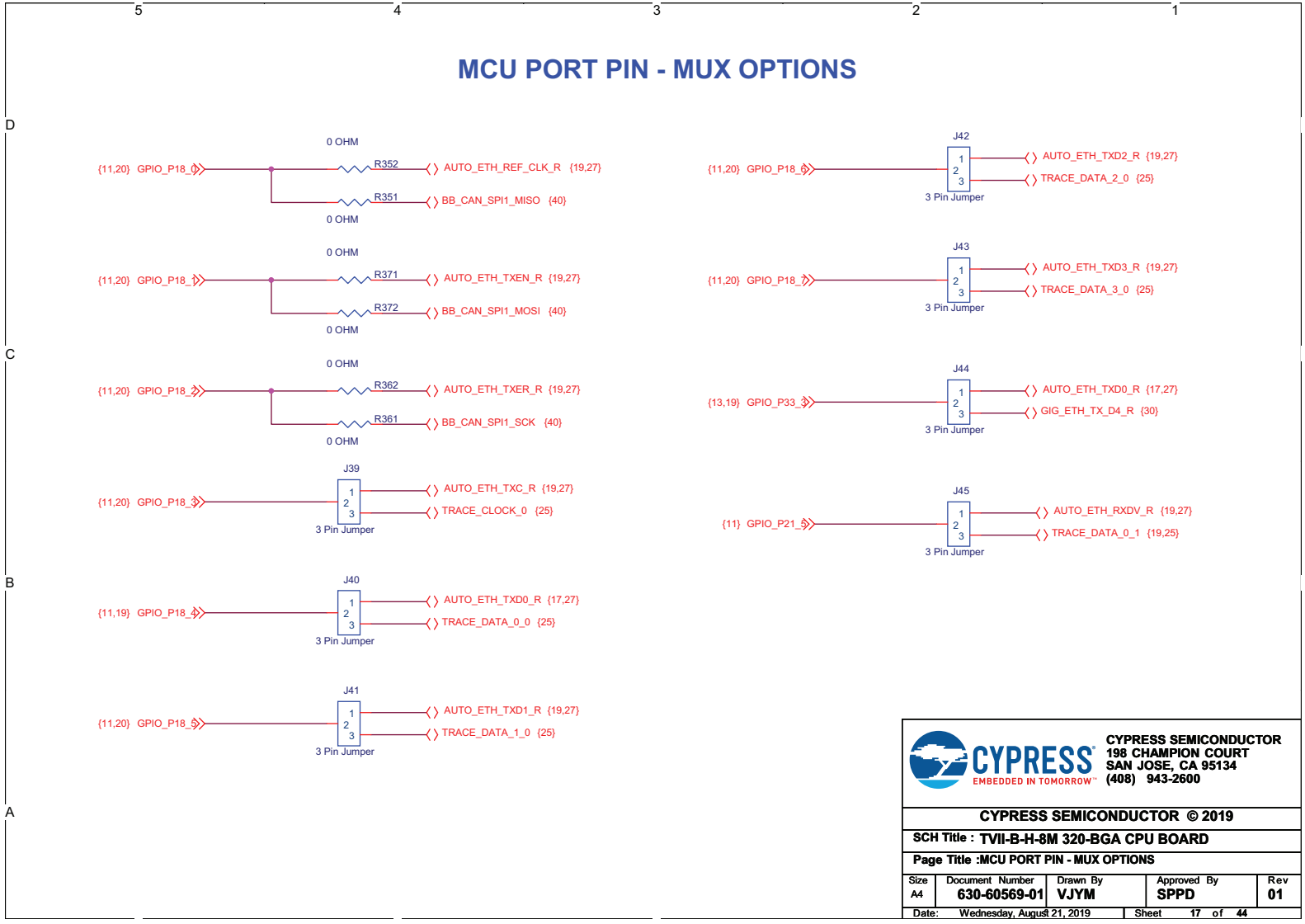


Figure A-17. MCU Port Pin Mux Options

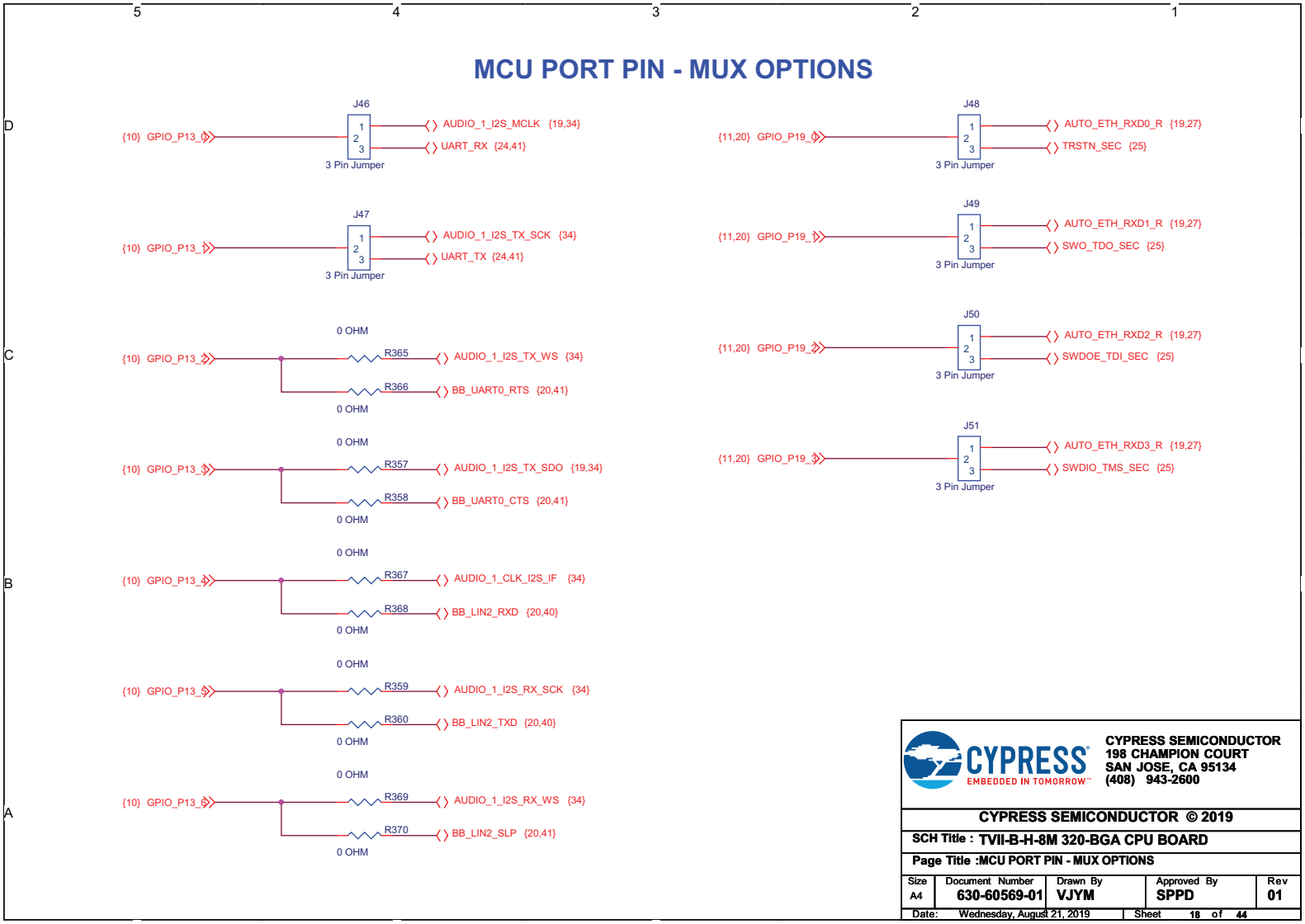


Figure A-18. Test Points-1

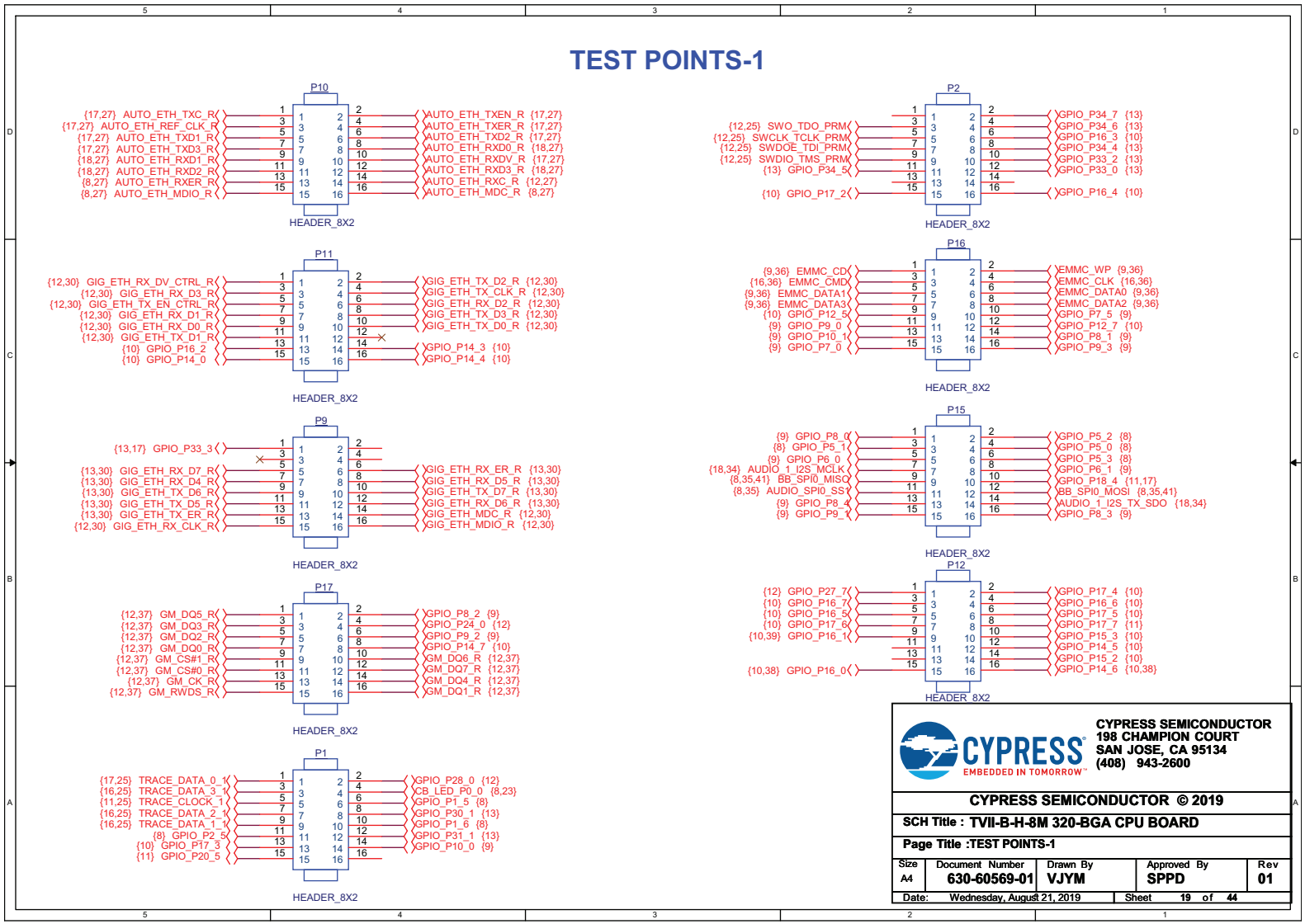


Figure A-19. Test Points-2

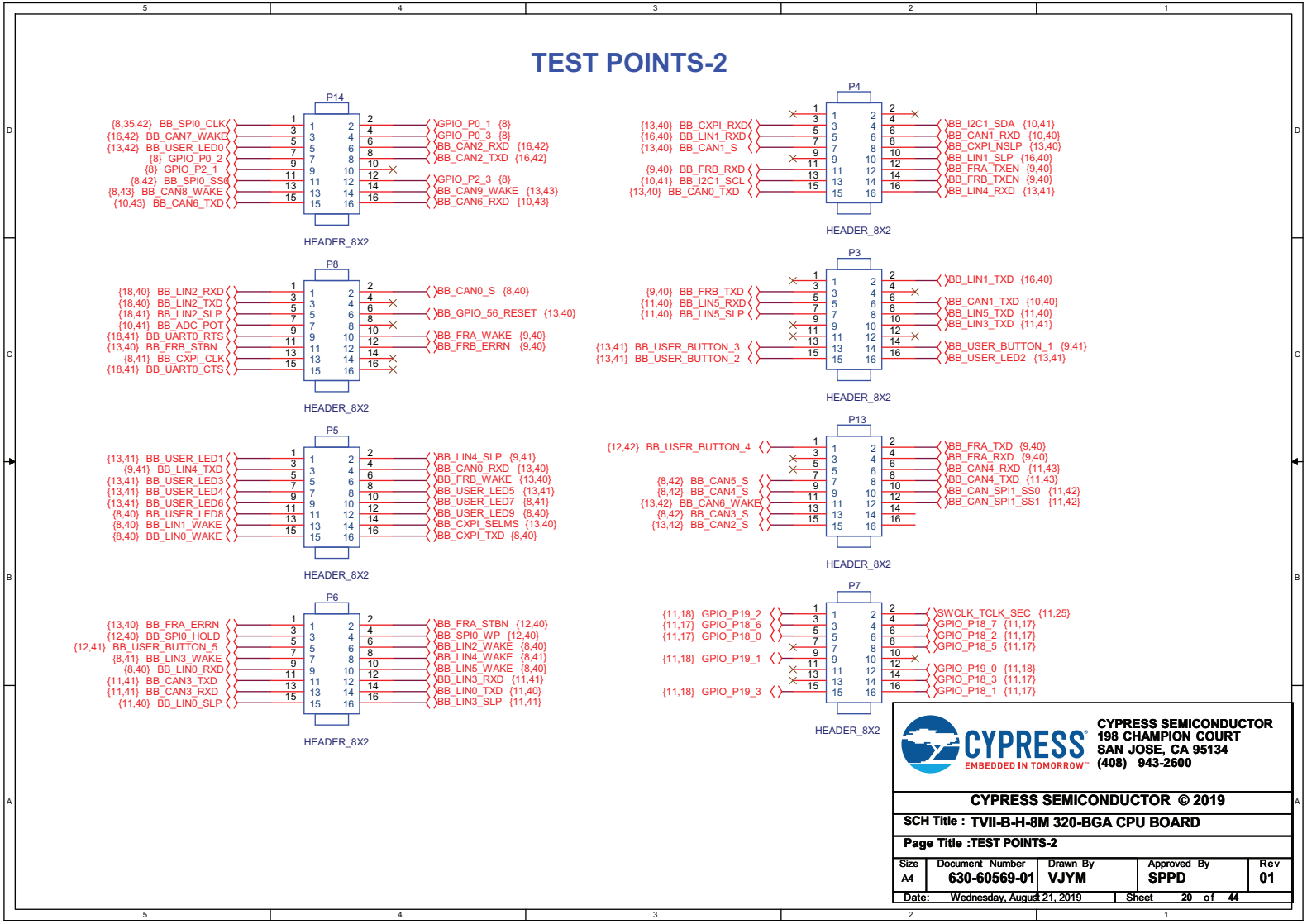


Figure A-20. Clock

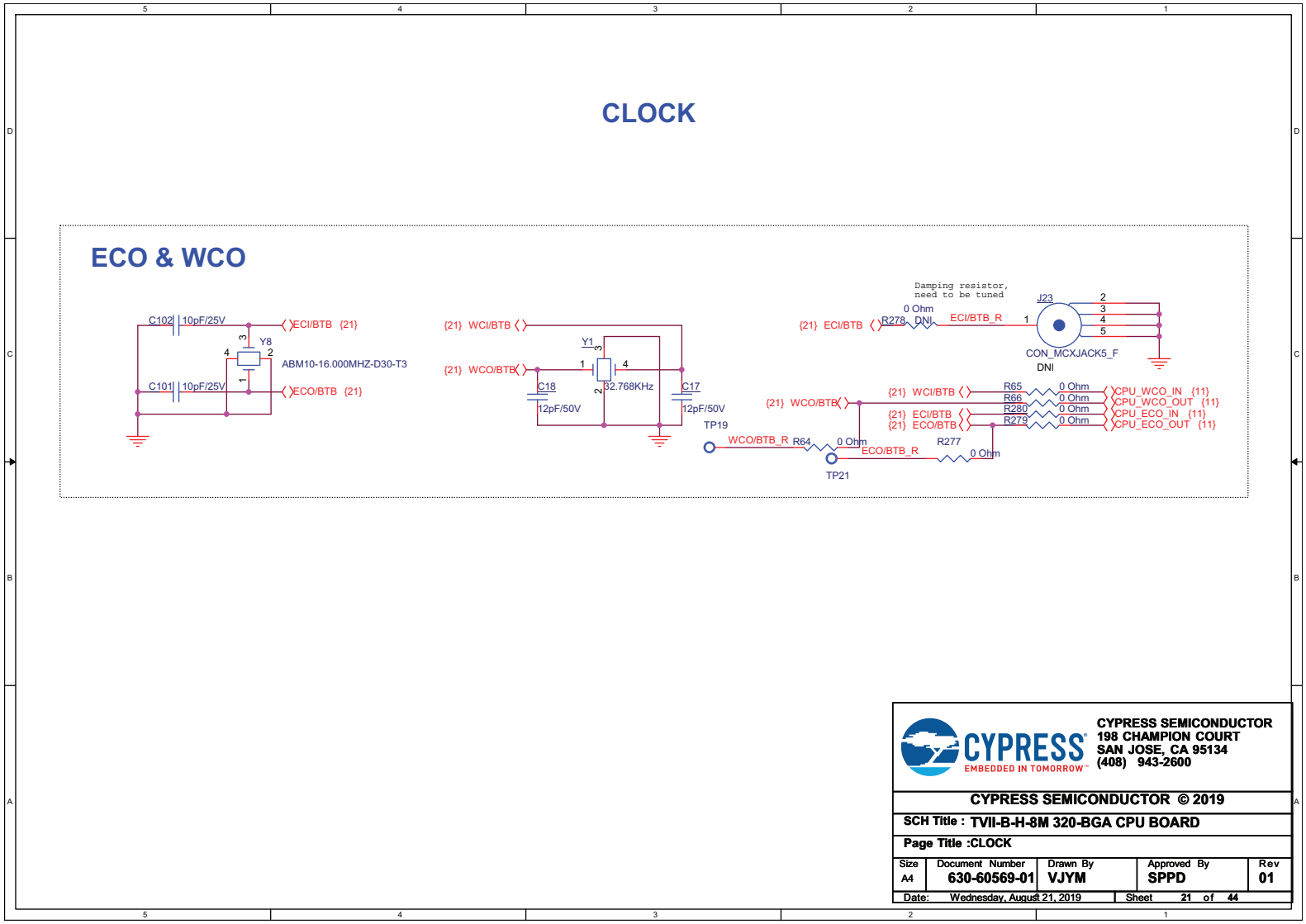


Figure A-21. Reset Controller

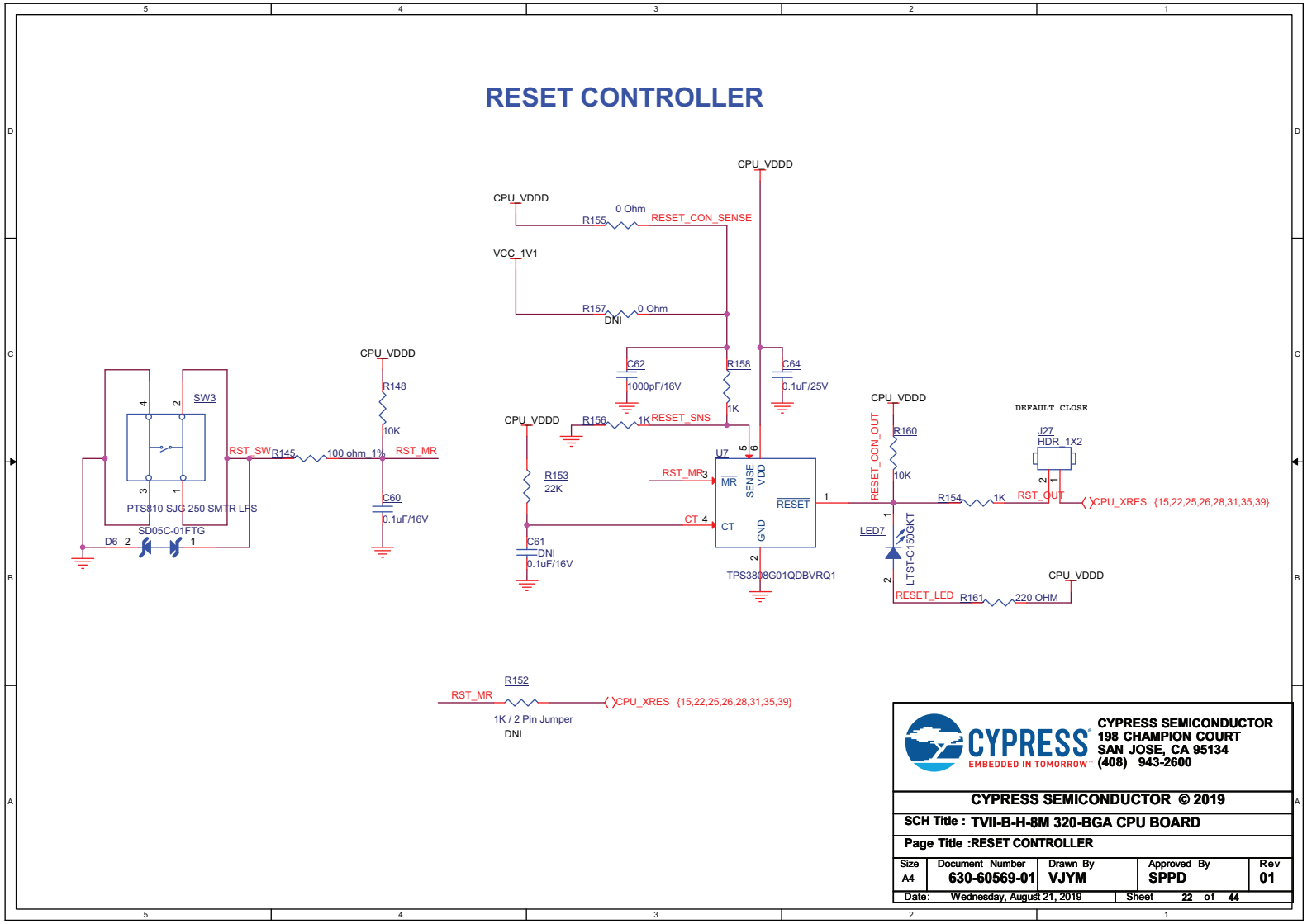


Figure A-22. GPIO - Button & Led

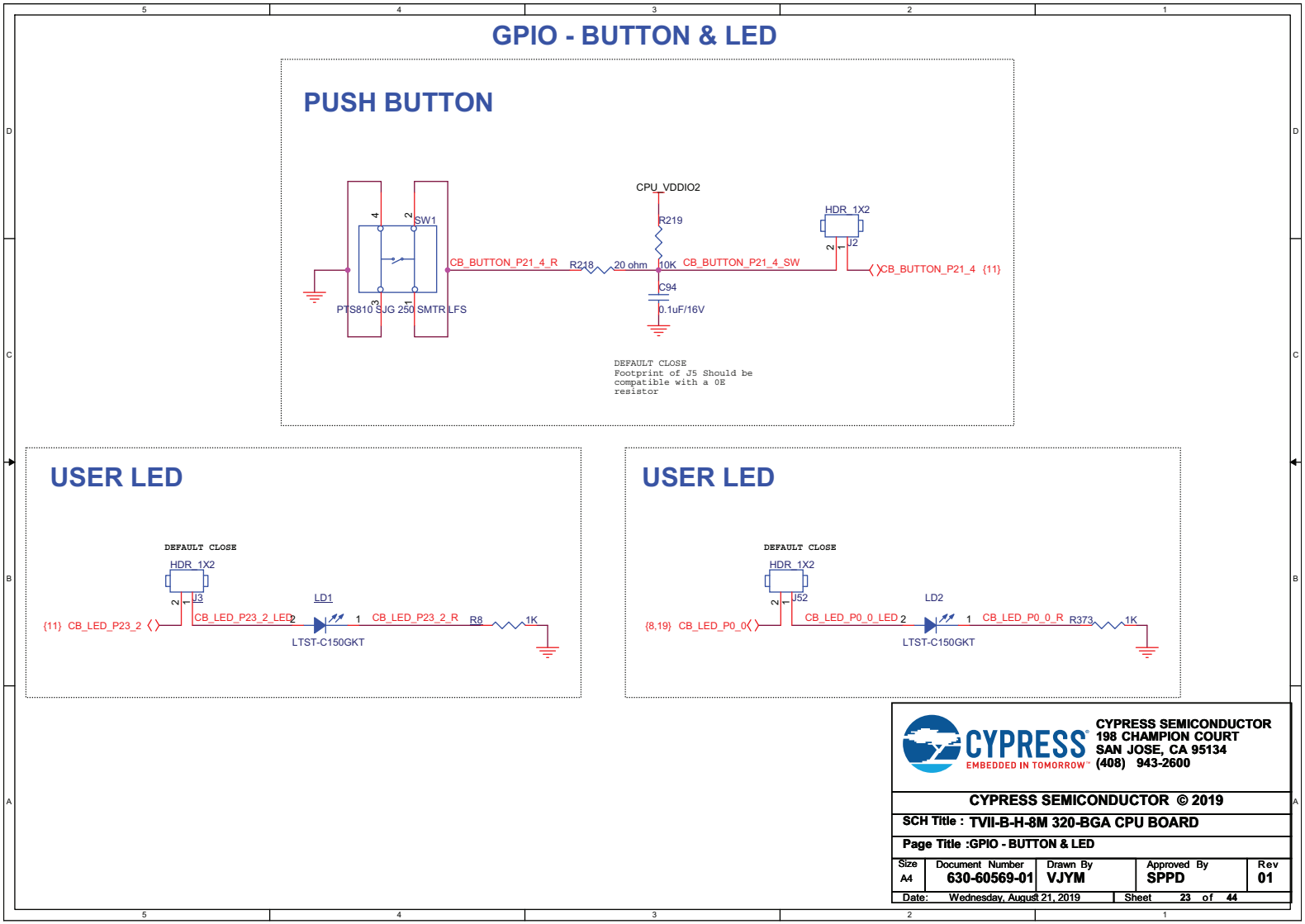


Figure A-23. UART - USB Transceiver

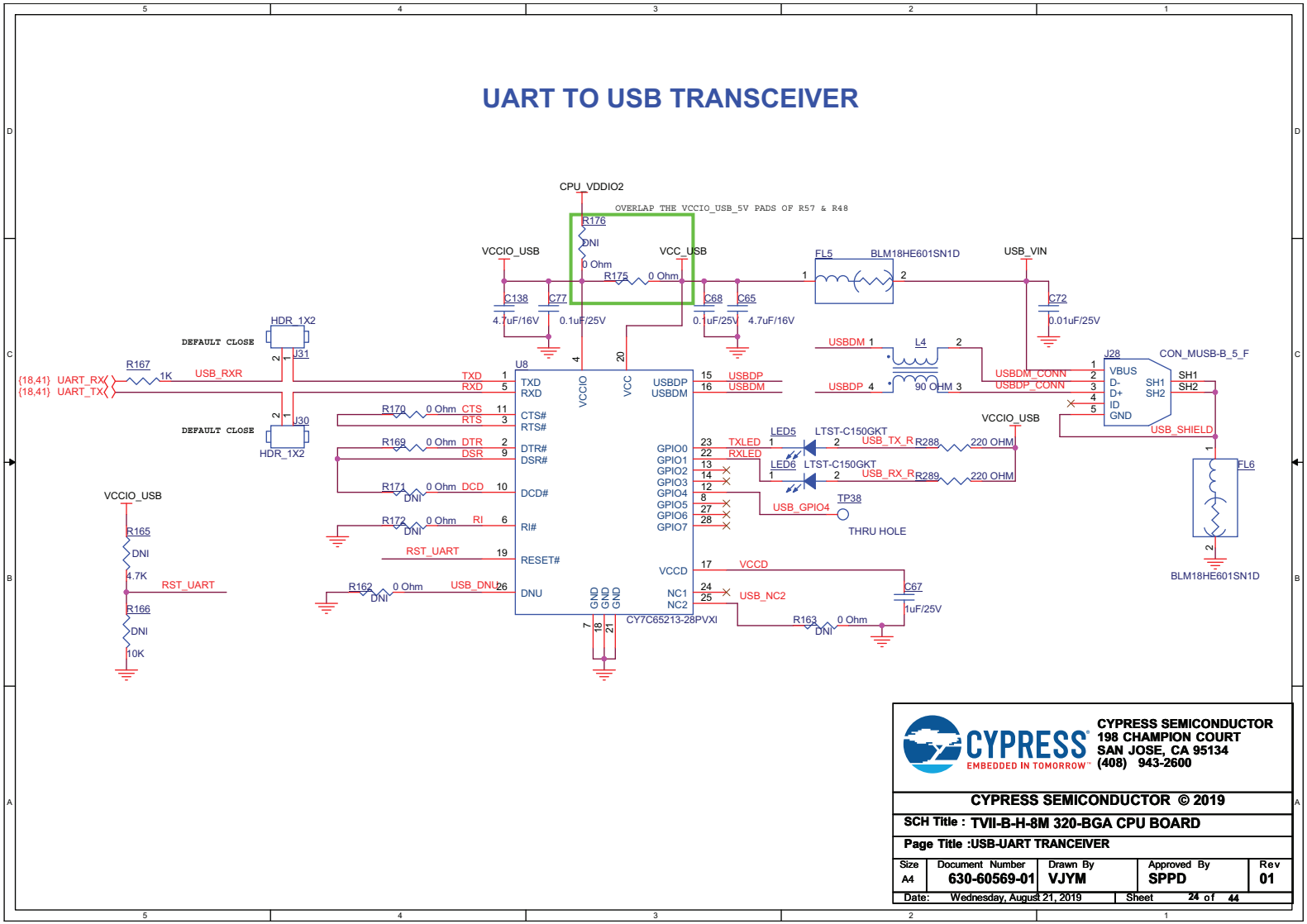


Figure A-24. Debug Interface-1

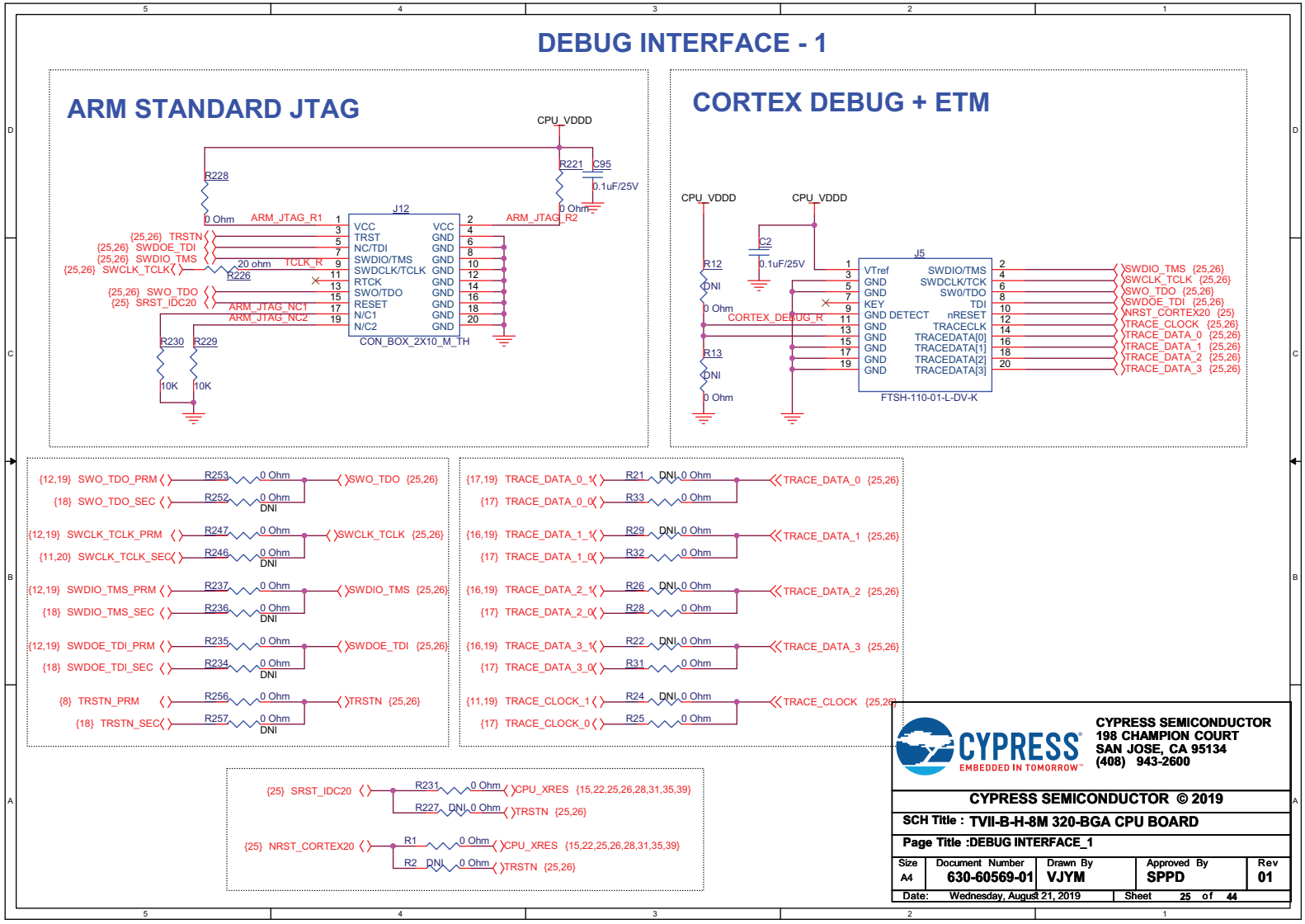


Figure A-25. Debug Interface-2

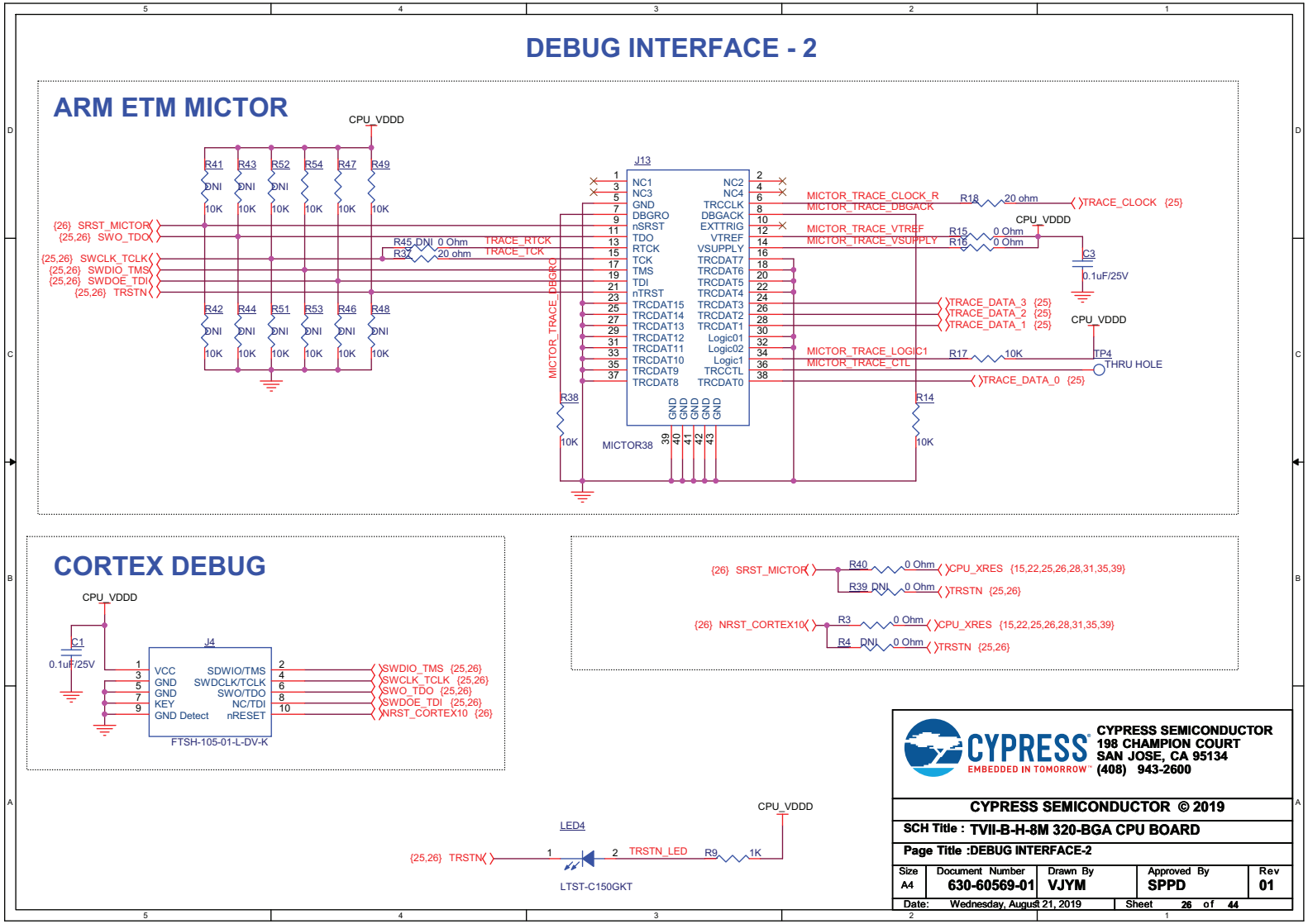


Figure A-26. Automotive Ethernet-1

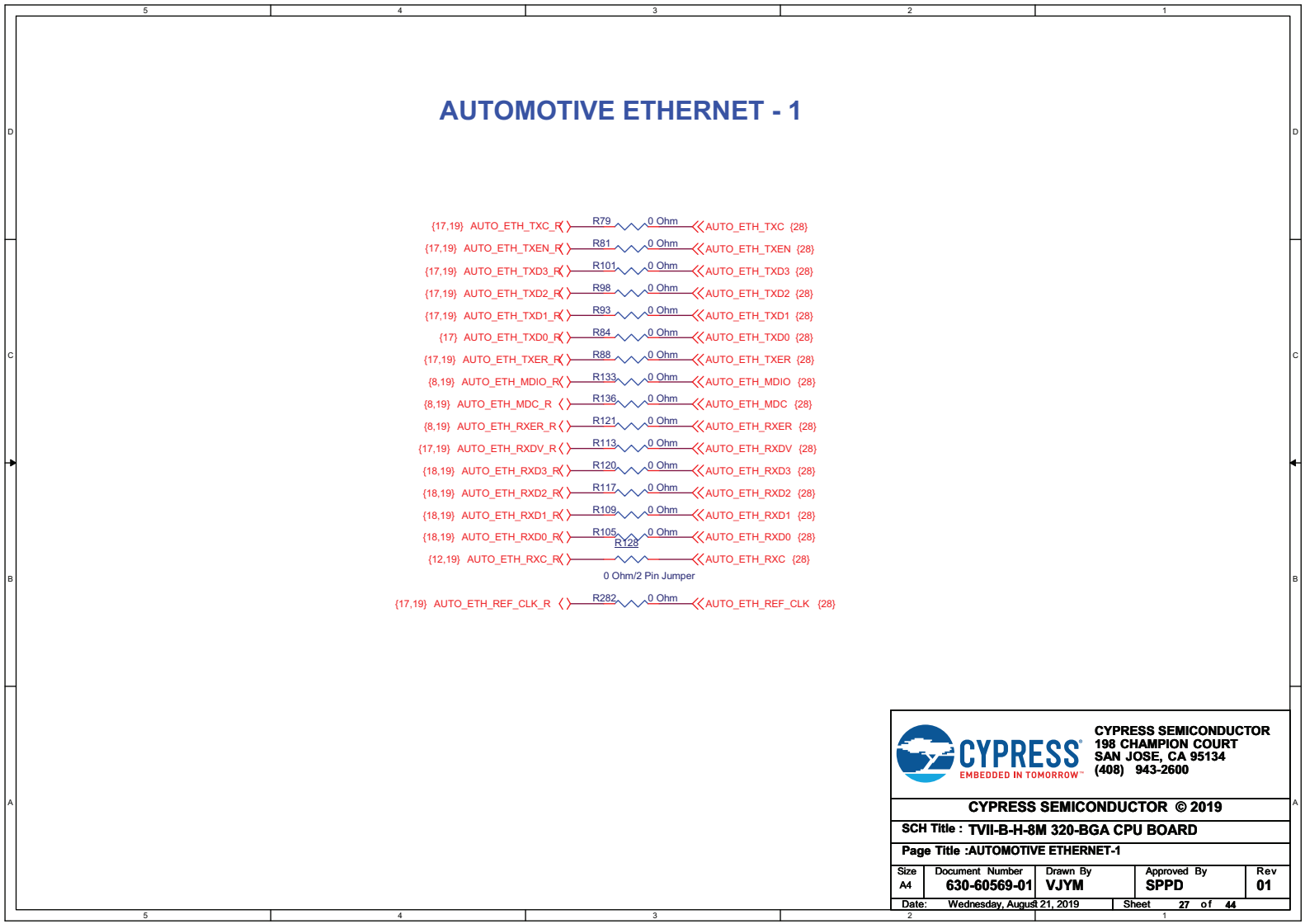


Figure A-27. Automotive Ethernet-2

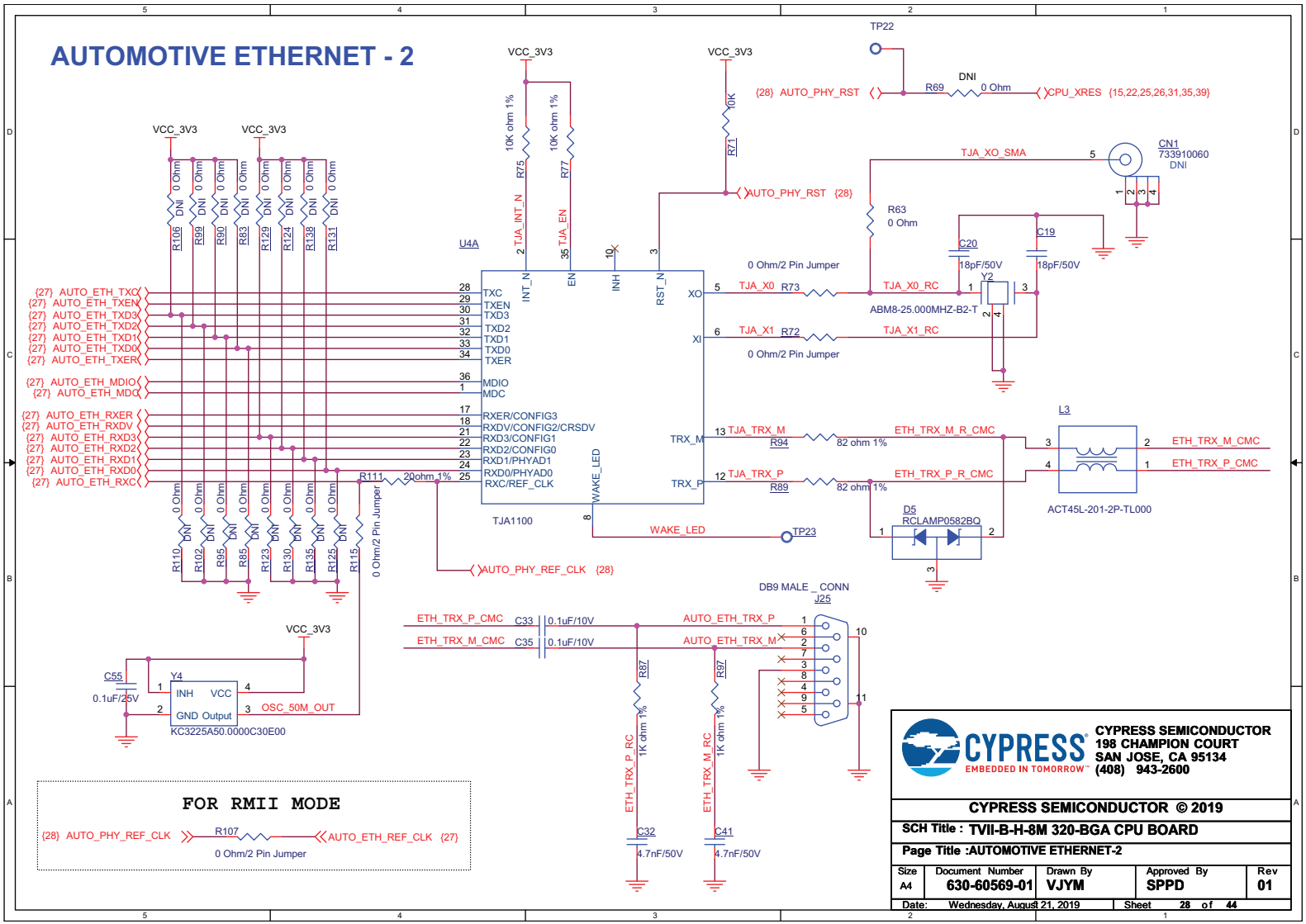


Figure A-28. Automotive Ethernet-3

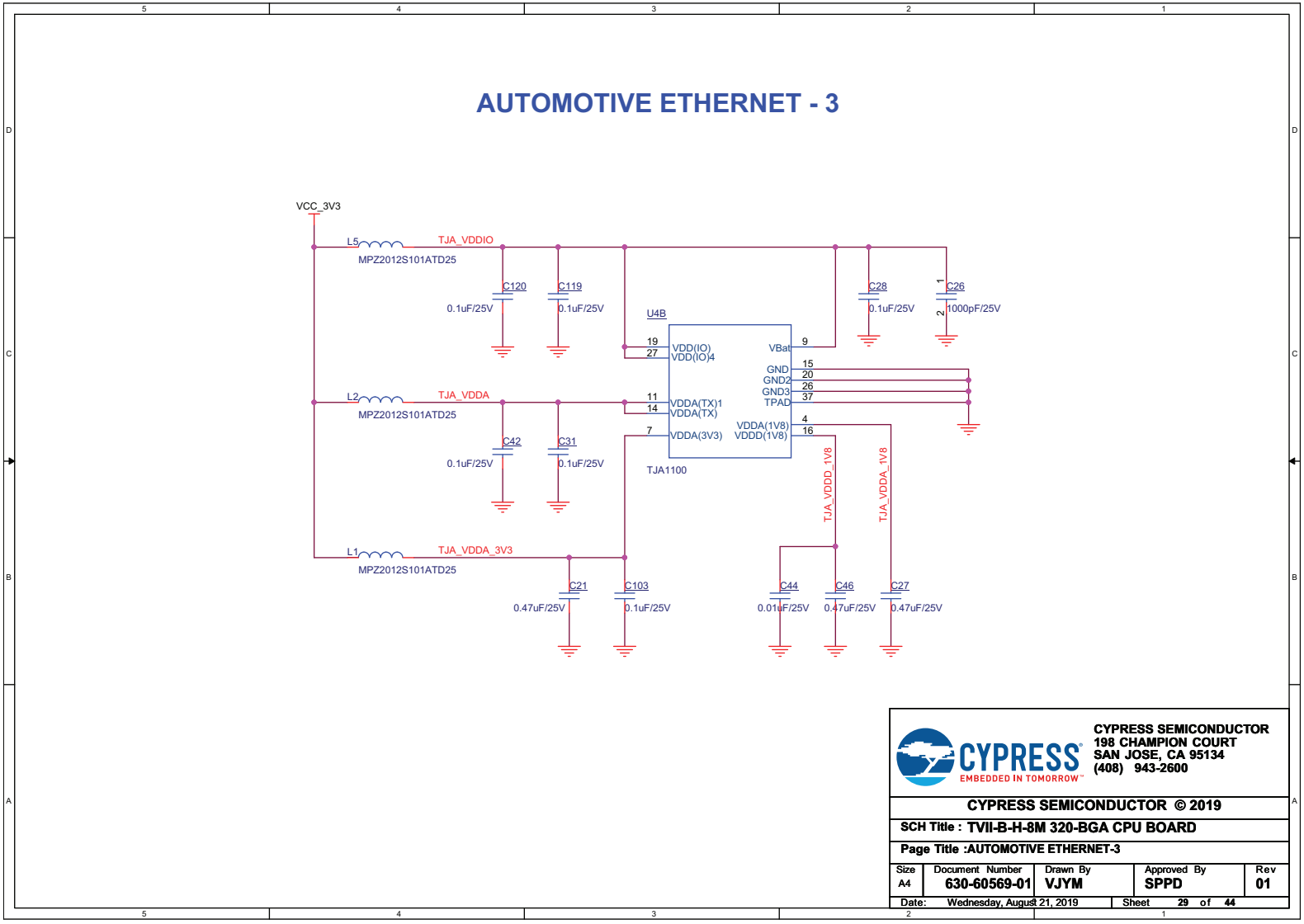


Figure A-29. Gigabit Ethernet-1

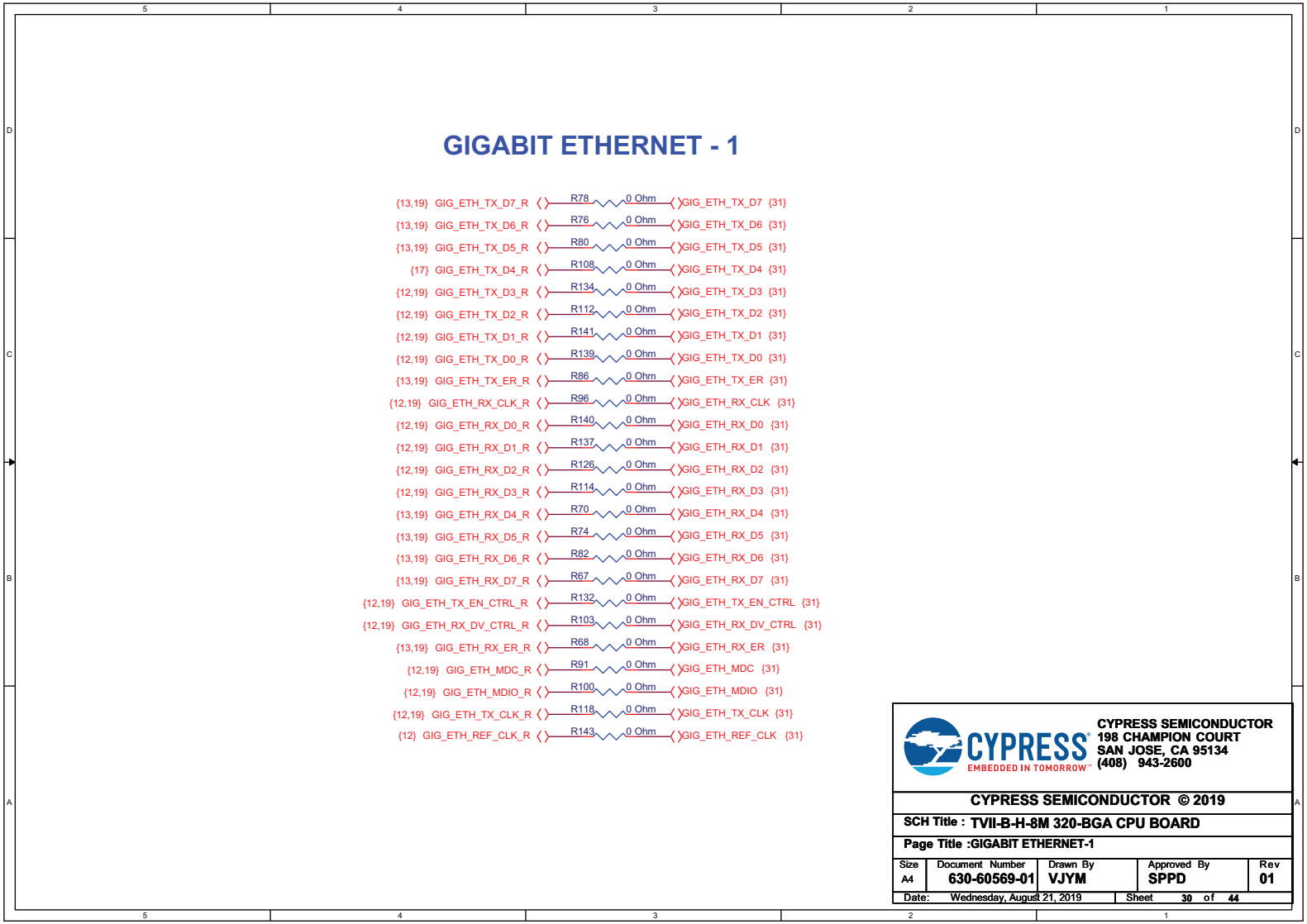


Figure A-30. Gigabit Ethernet-2

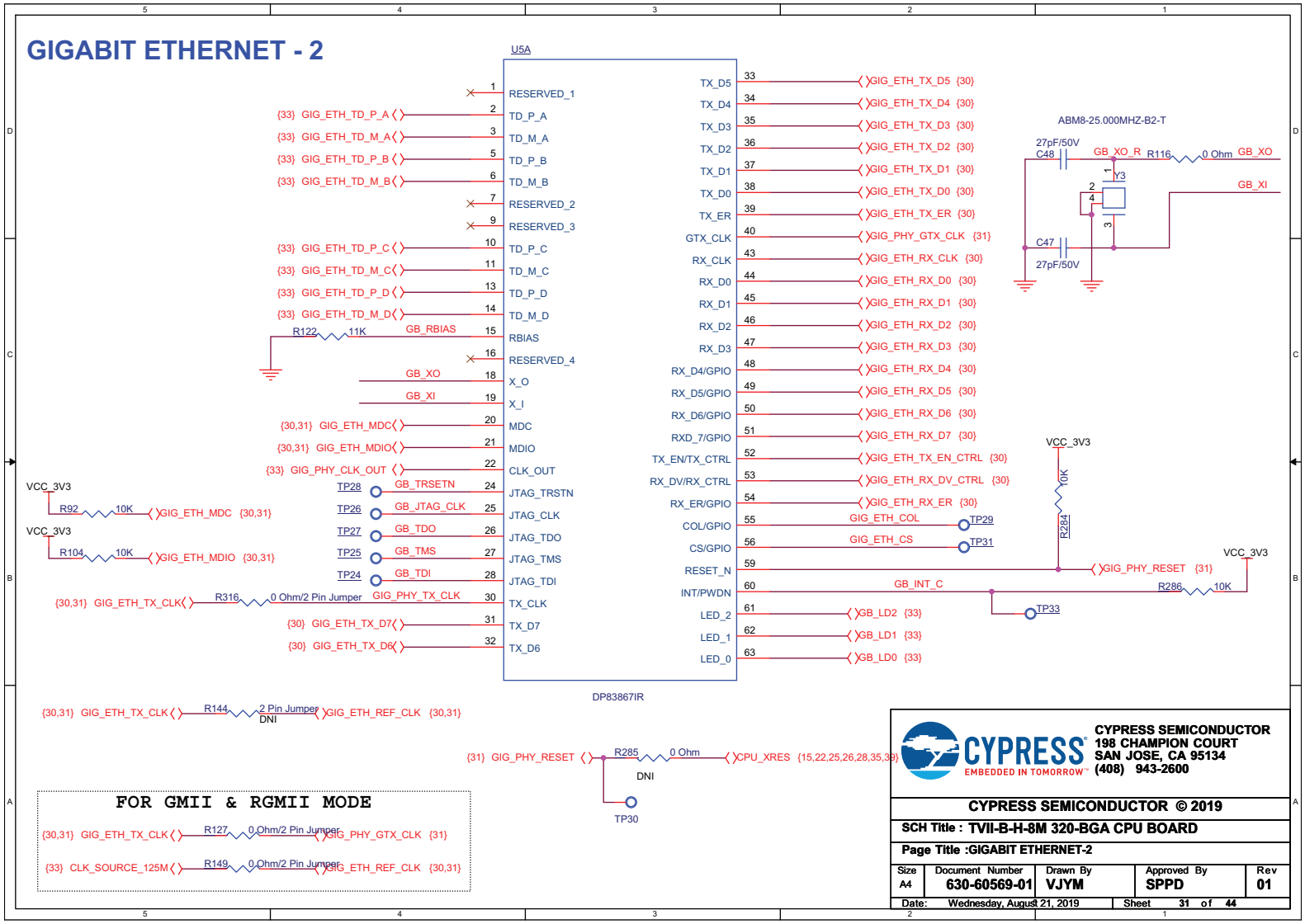


Figure A-31. Gigabit Ethernet-3

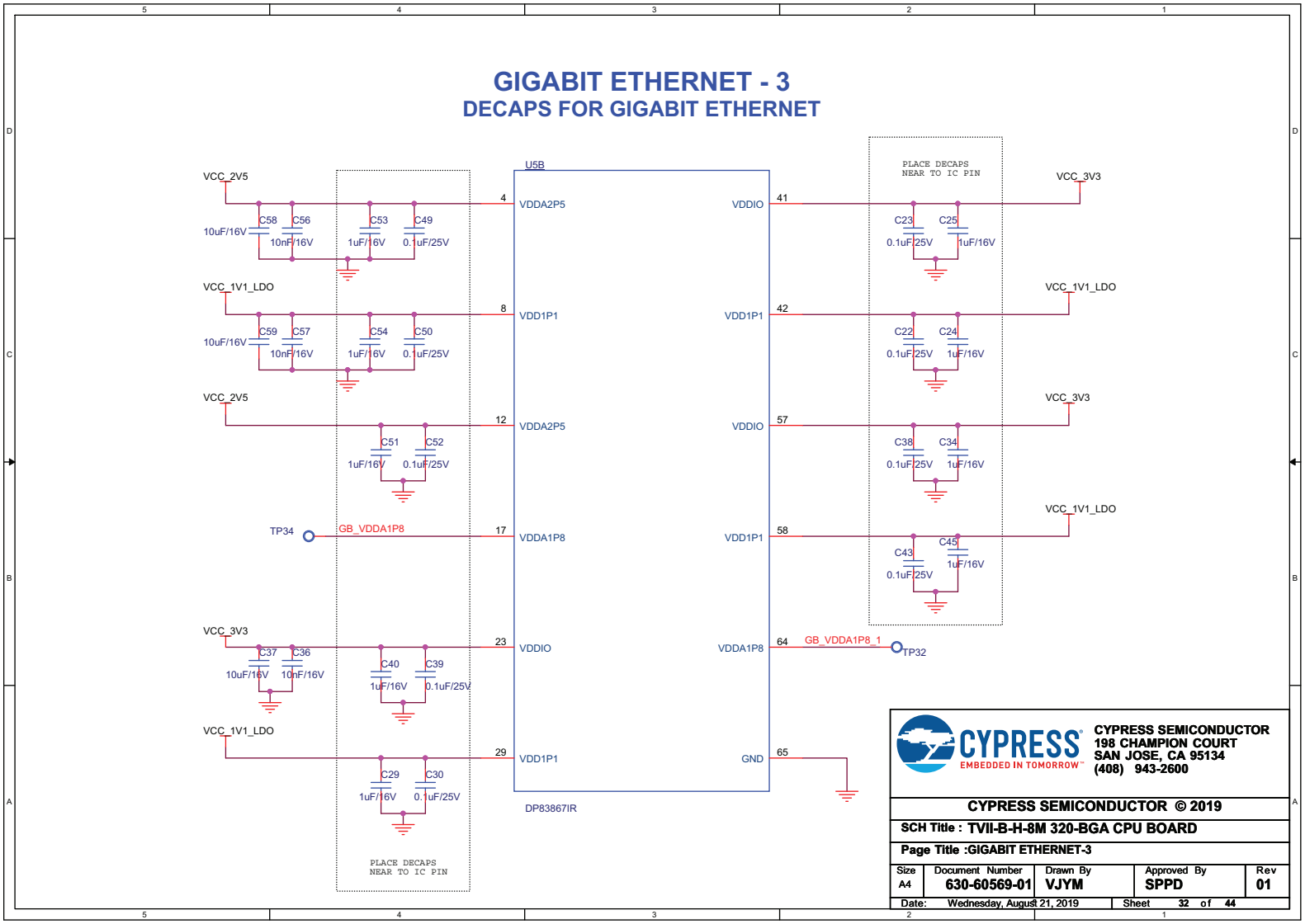


Figure A-32. Gigabit Ethernet-4

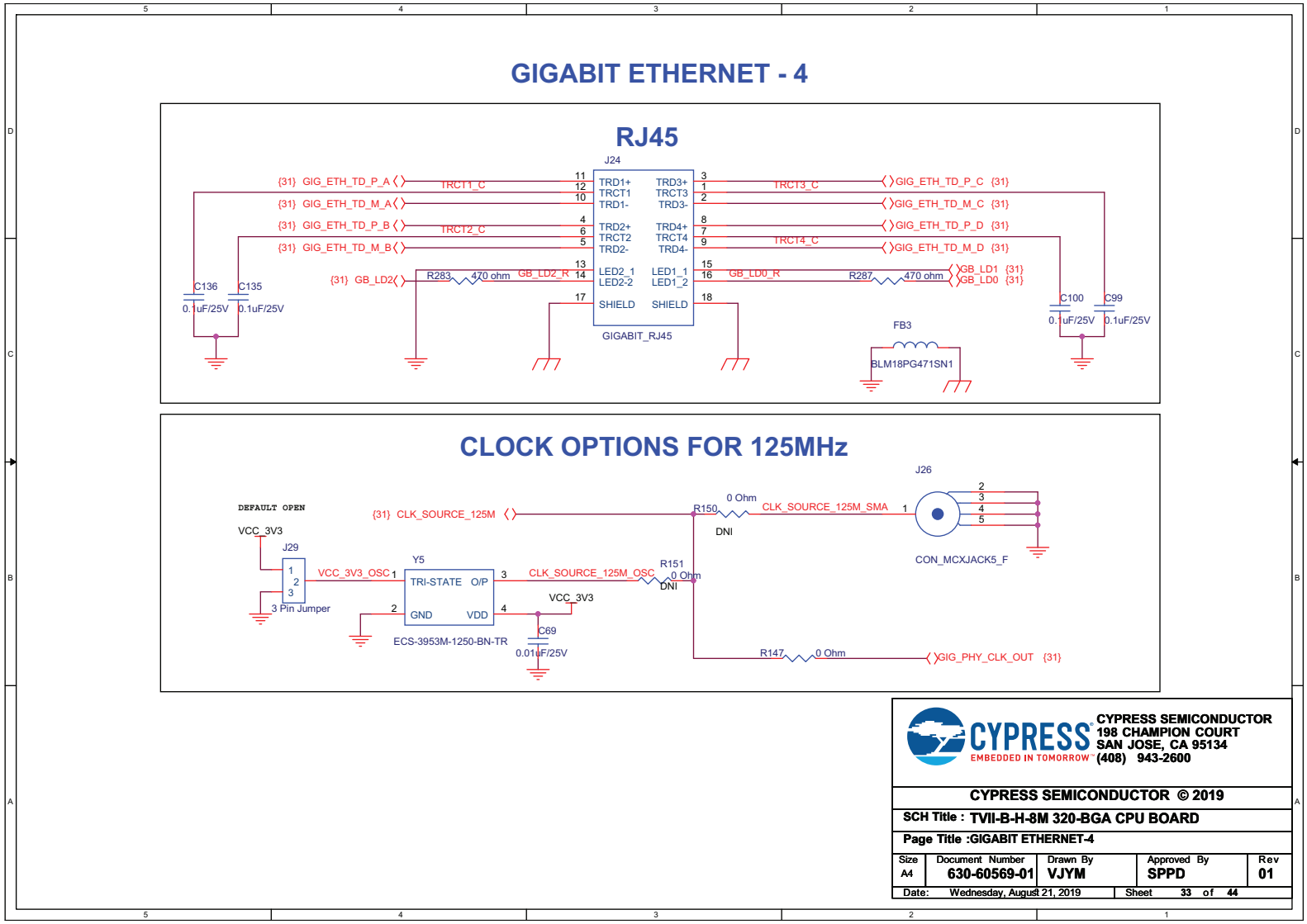


Figure A-33. Audio Interface-1

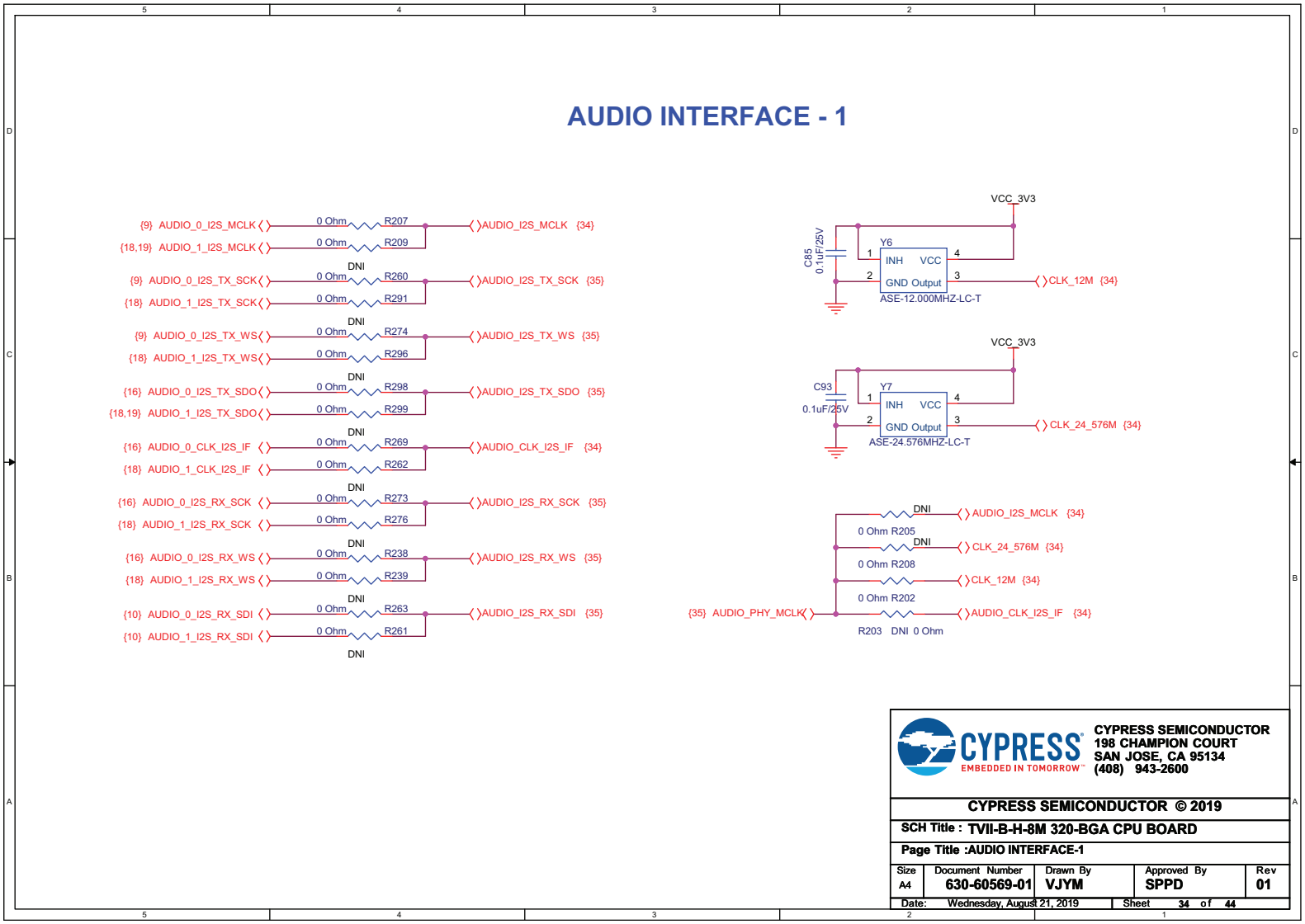


Figure A-34. Audio Interface-2

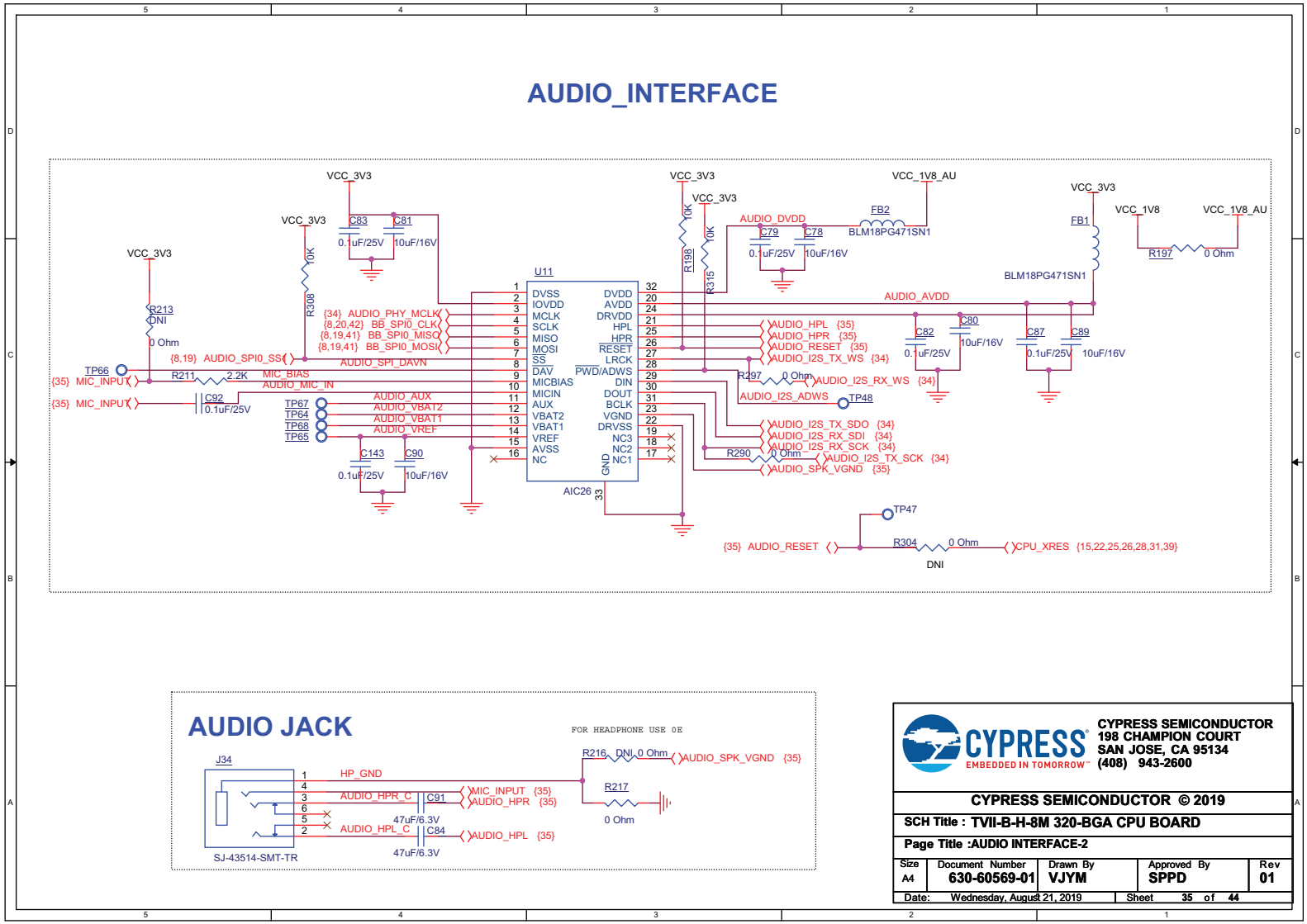


Figure A-35. eMMC Interface

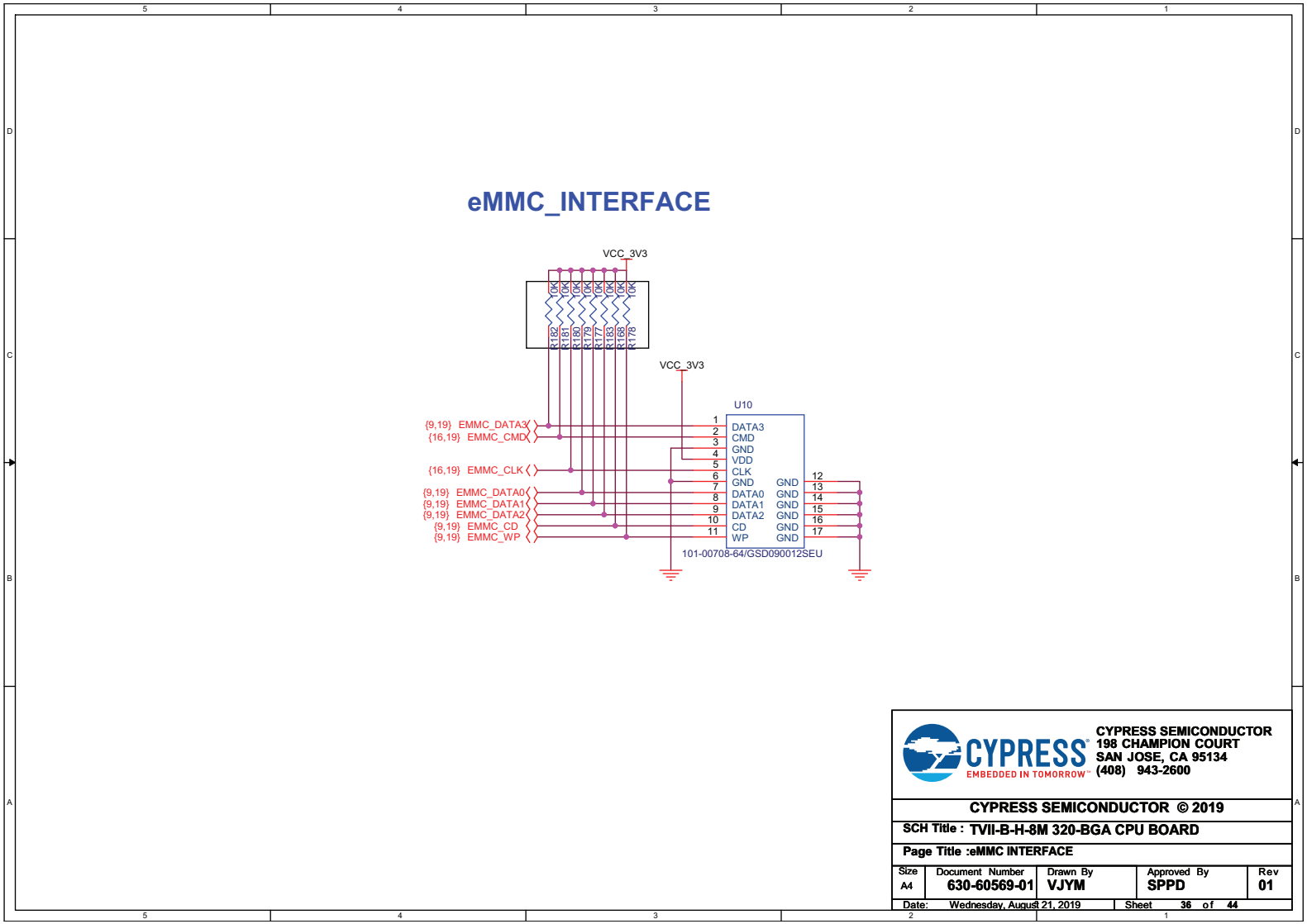


Figure A-36. SMIF HS Connector

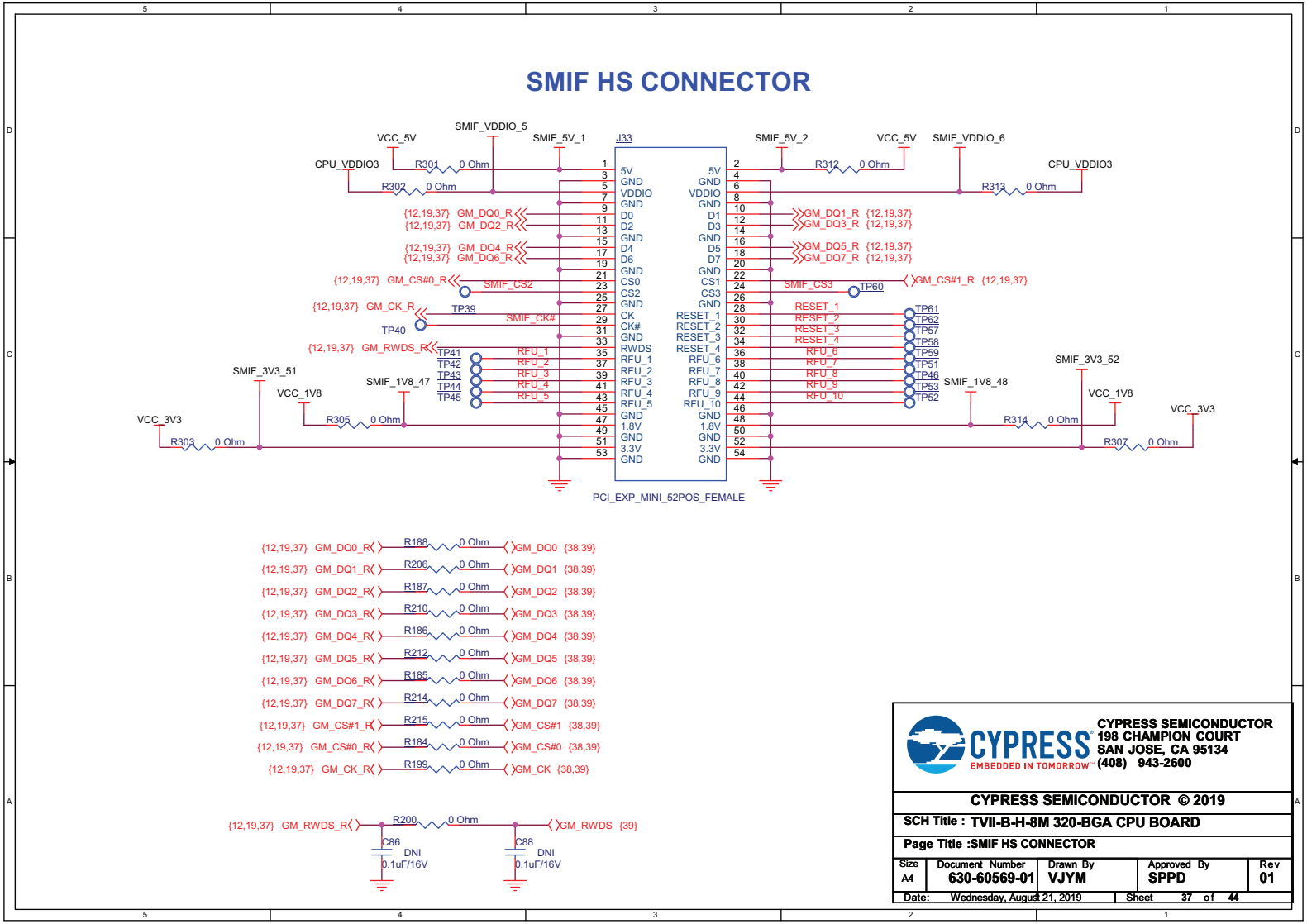


Figure A-37. Dual Quad-SPI

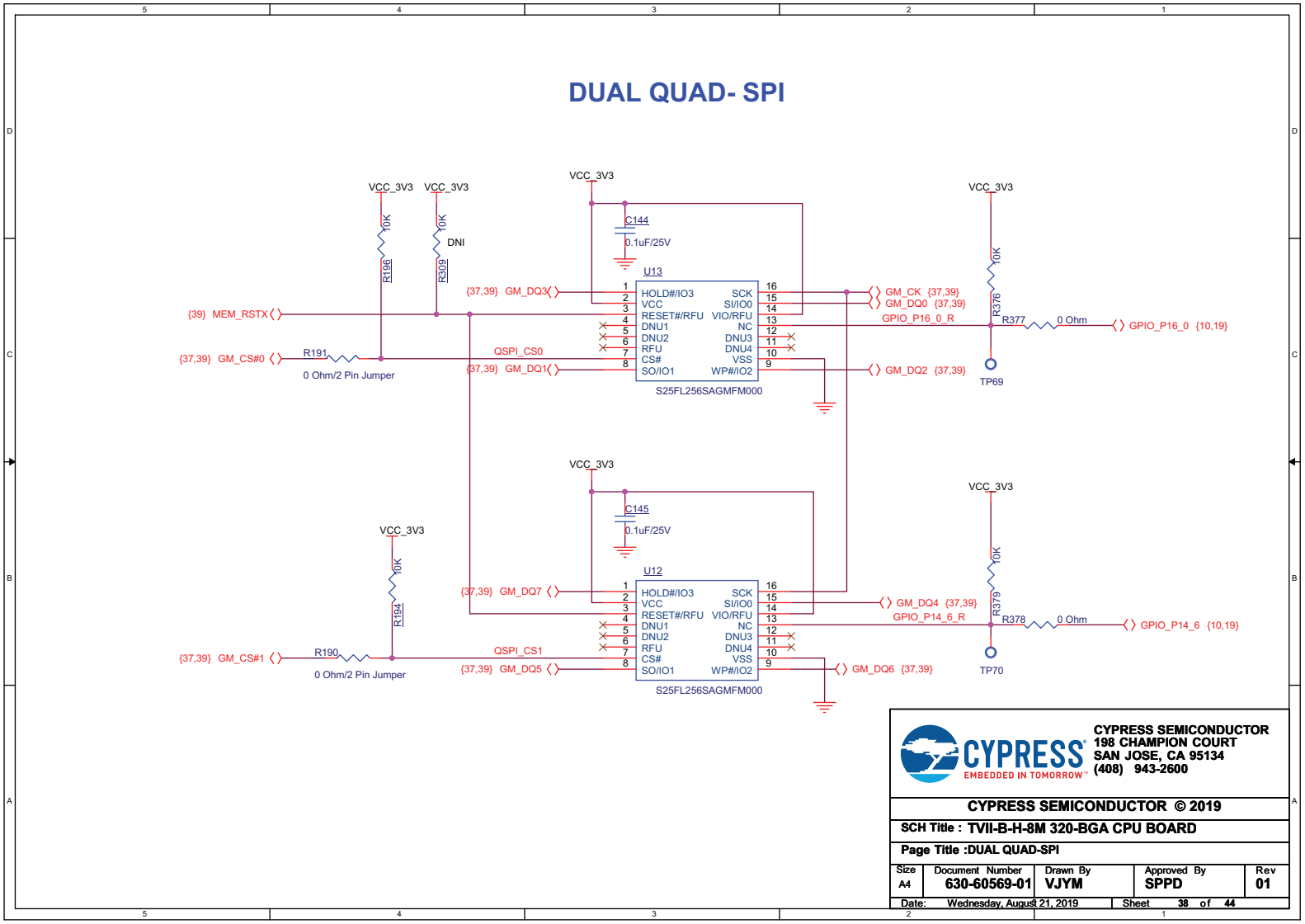


Figure A-38. H-Flash & H-SRAM

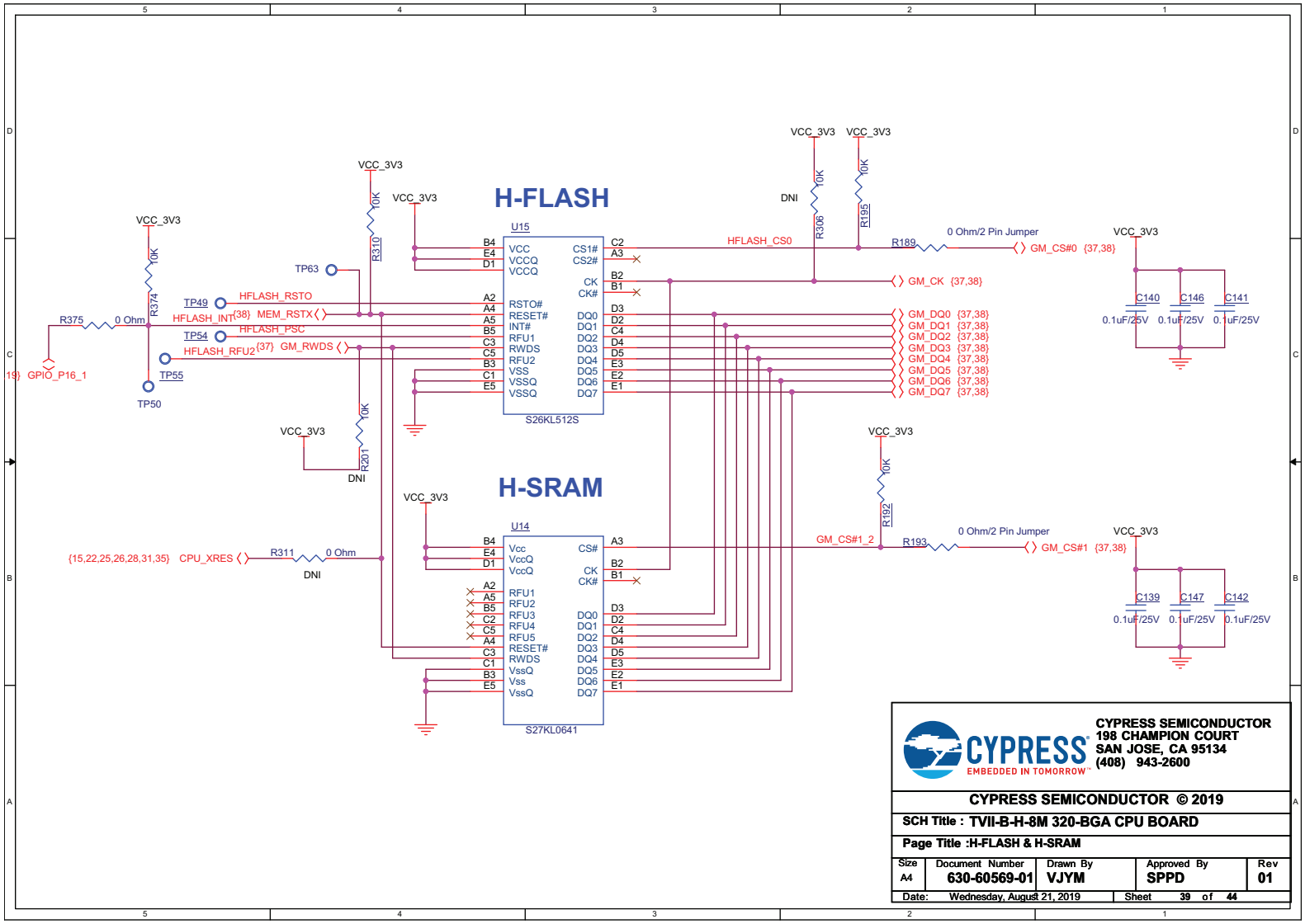


Figure A-39. Base Board Connector - J35A

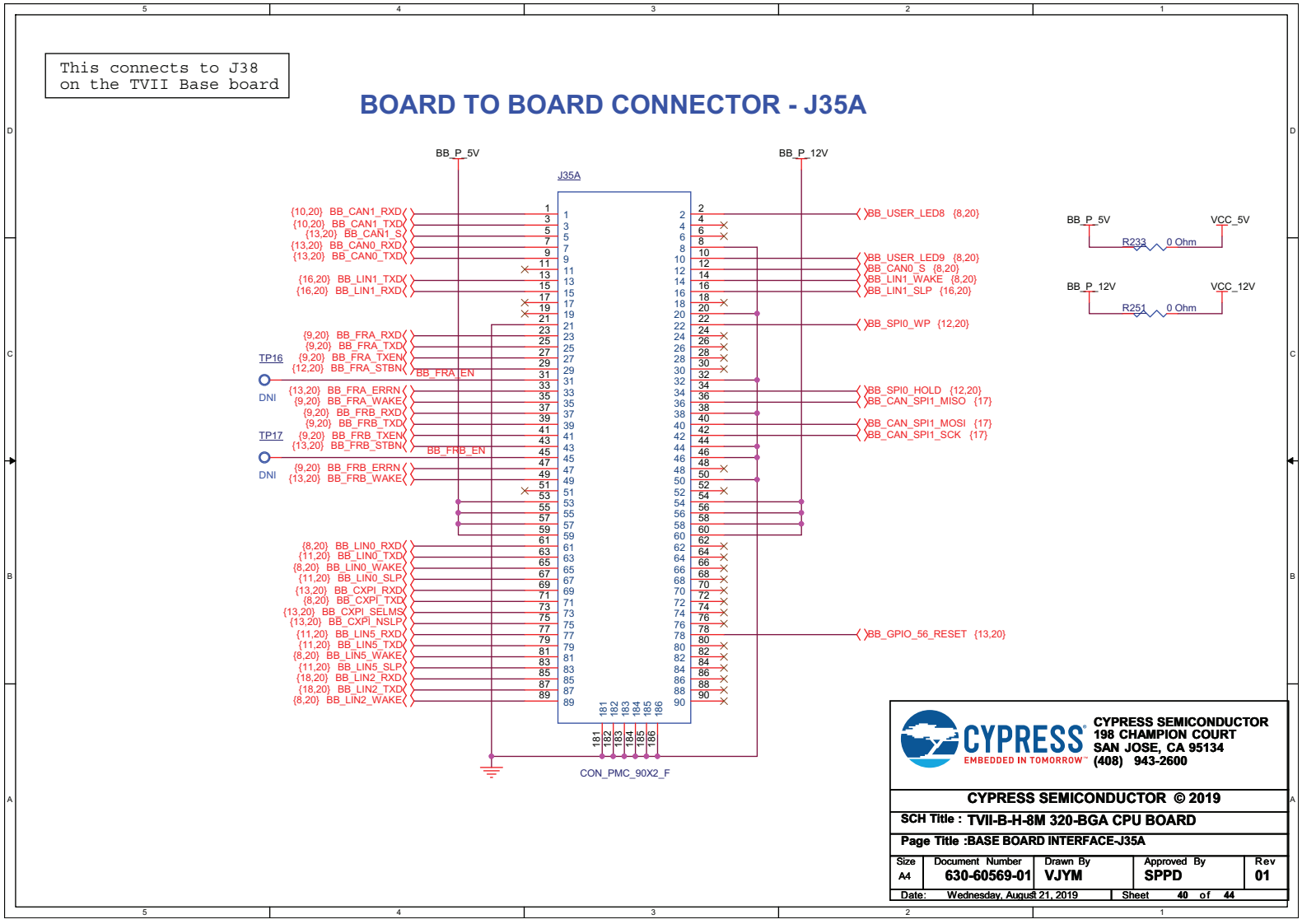


Figure A-40. Base Board Connector - J35B

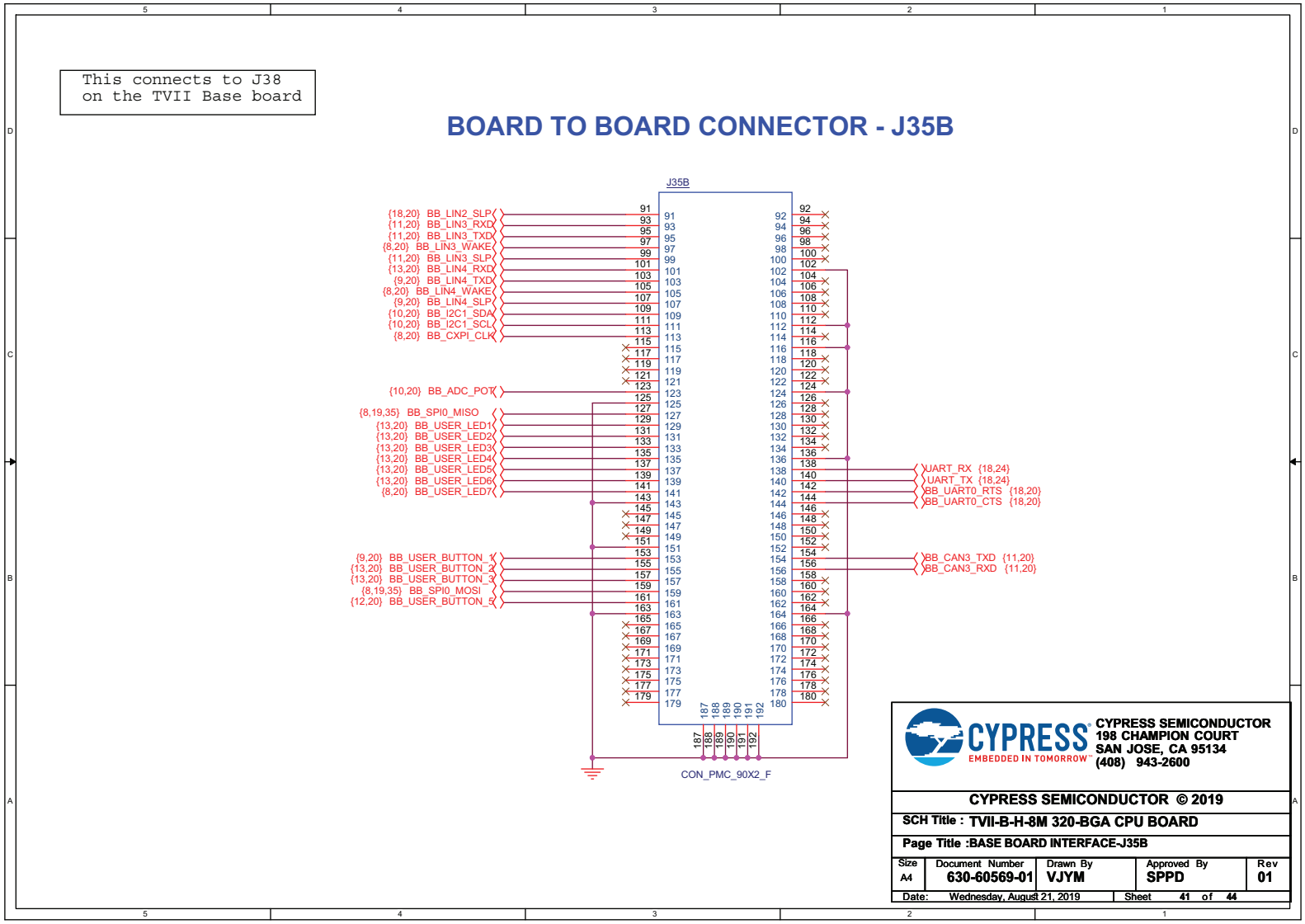


Figure A-41. Base Board Connector - J36A

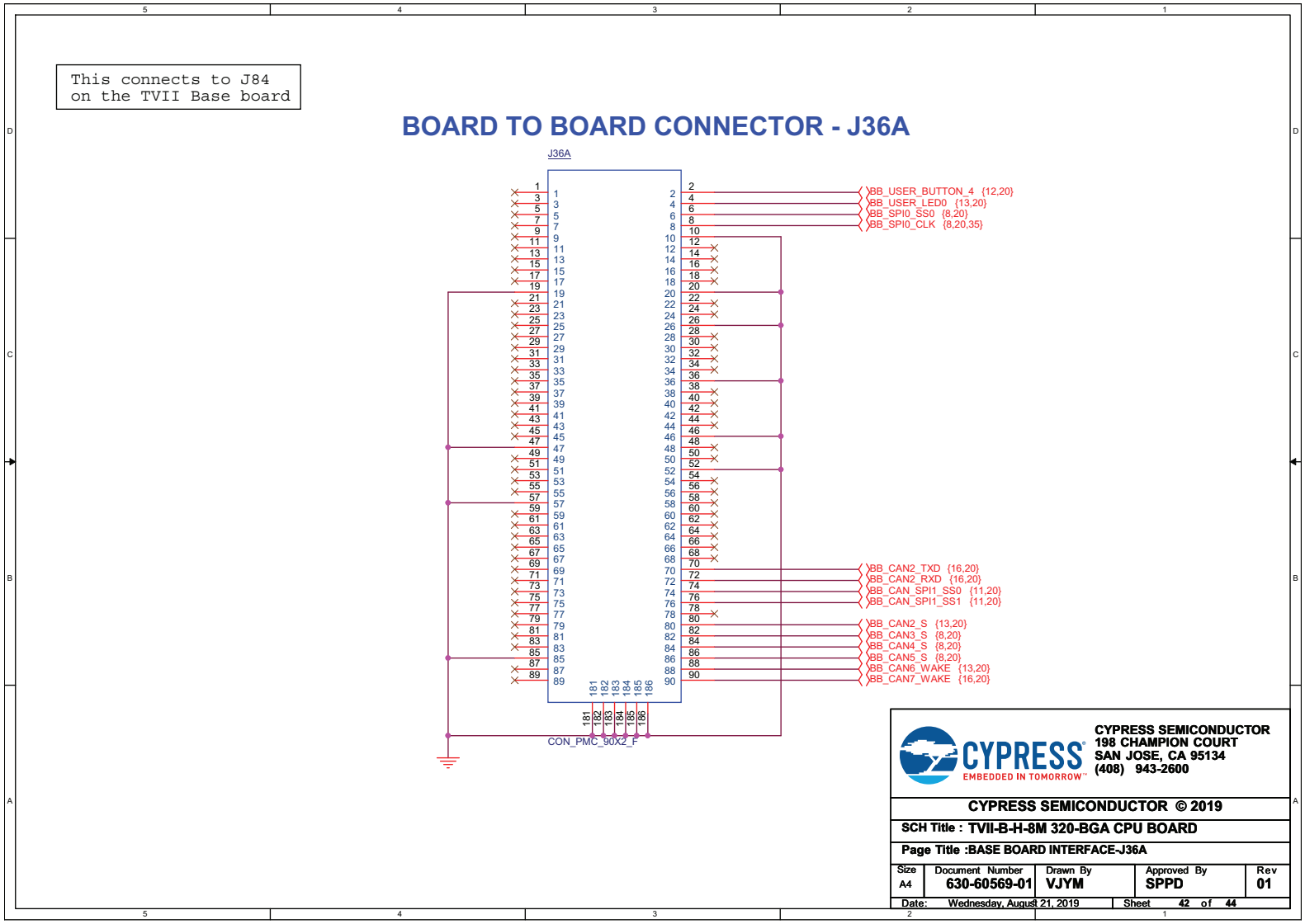
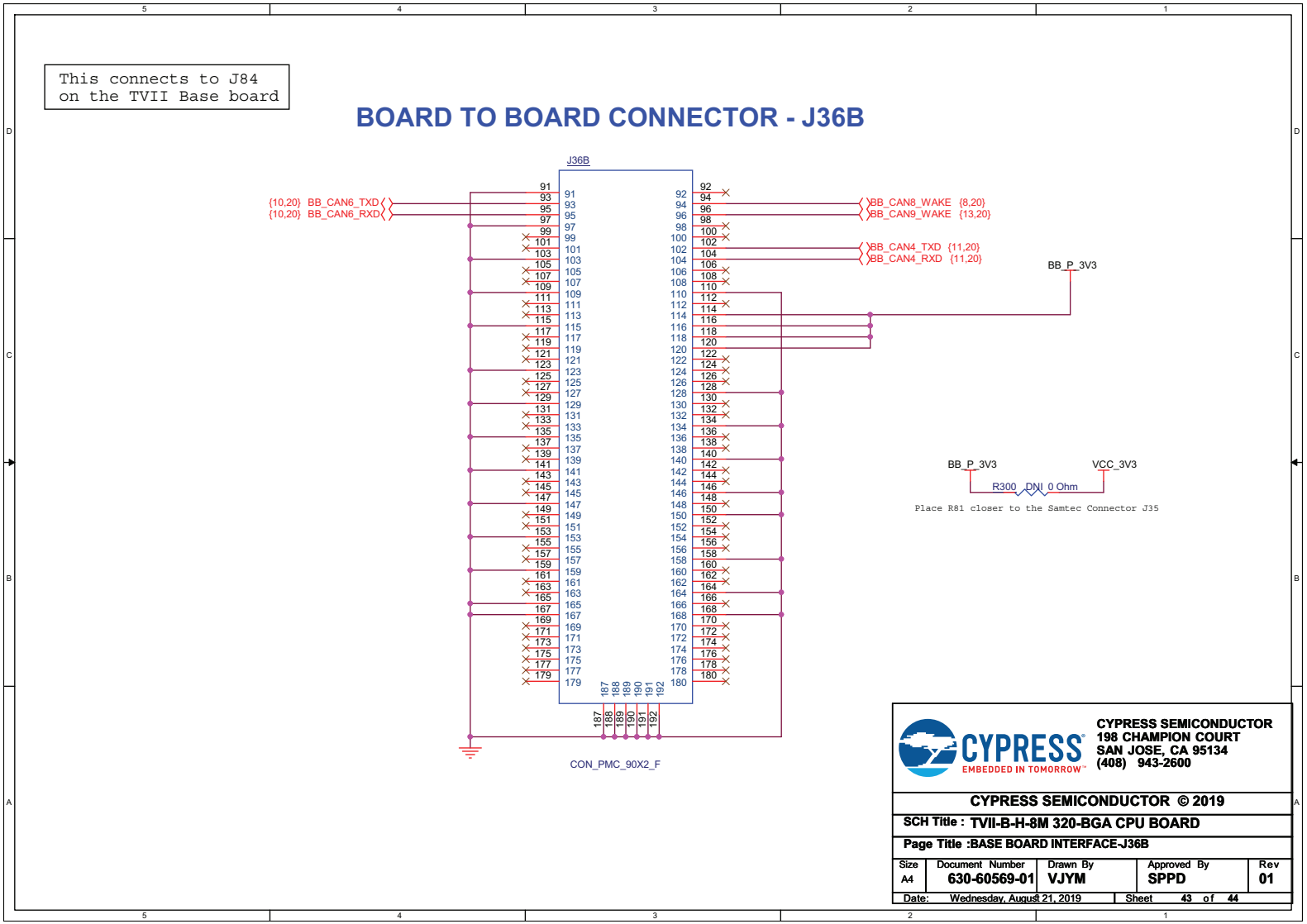


Figure A-42. Base Board Connector - J36B



B. Component Assembly on CPU Board

This appendix shows the top and bottom assembly of the CYTVII-B-H-8M-320-CPU board.

Figure B-1. Component Assembly (Top)

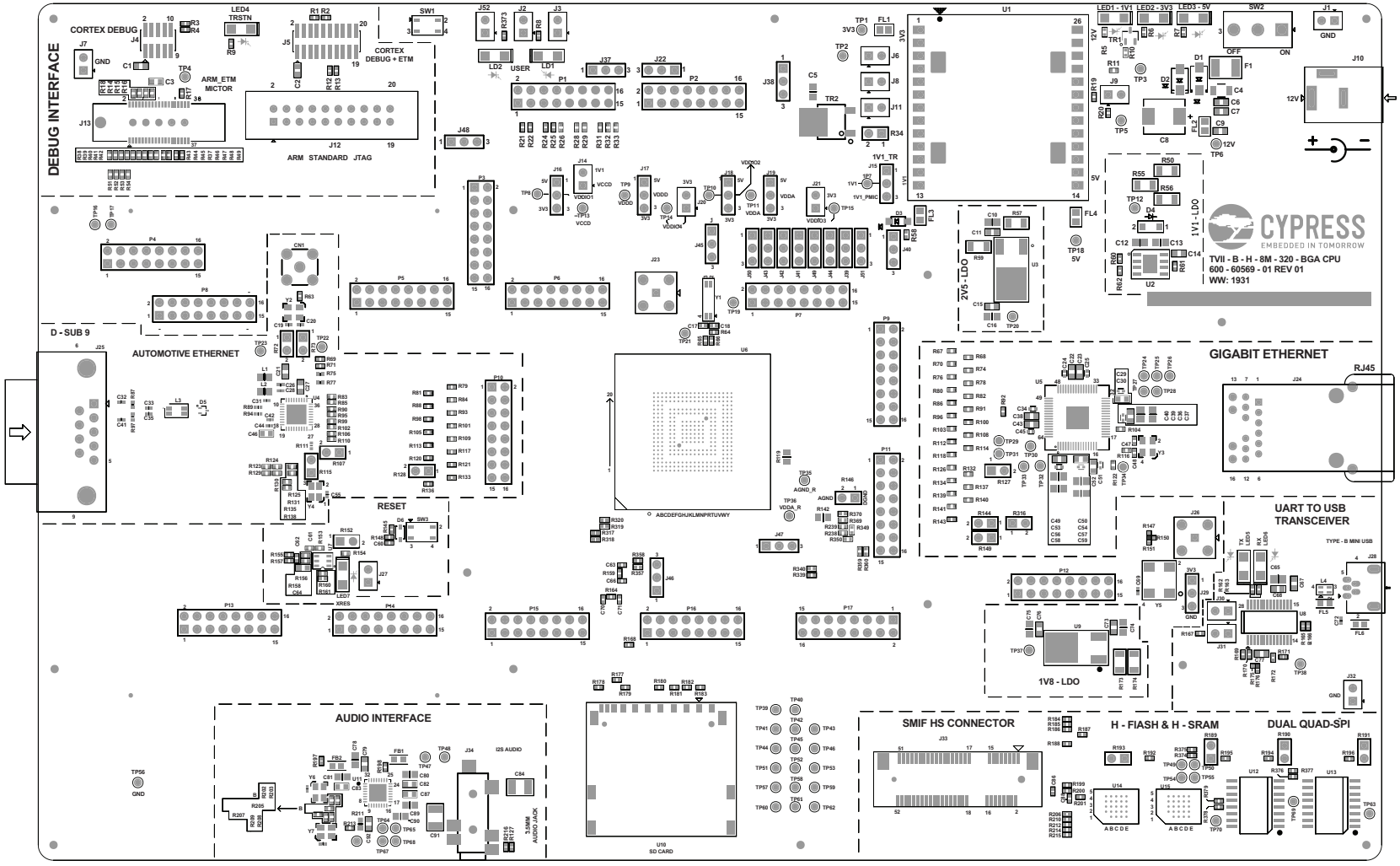
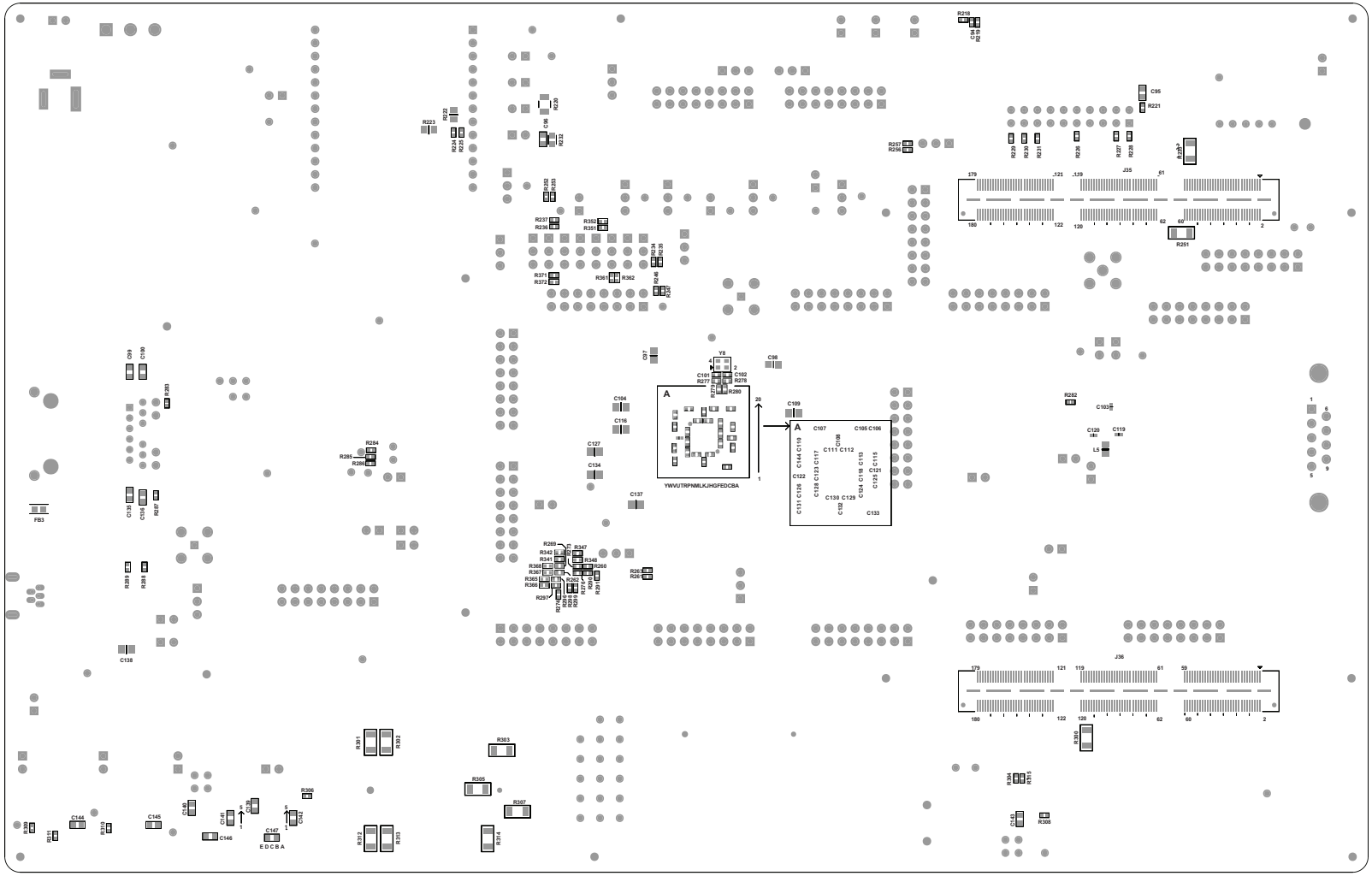


Figure B-2. Component Assembly (Bottom)



C. Schematics of Base Board

This appendix contains the schematics of Traveo II Base board (CYTVII-B-E-BB).

Figure C-1. Block Diagram

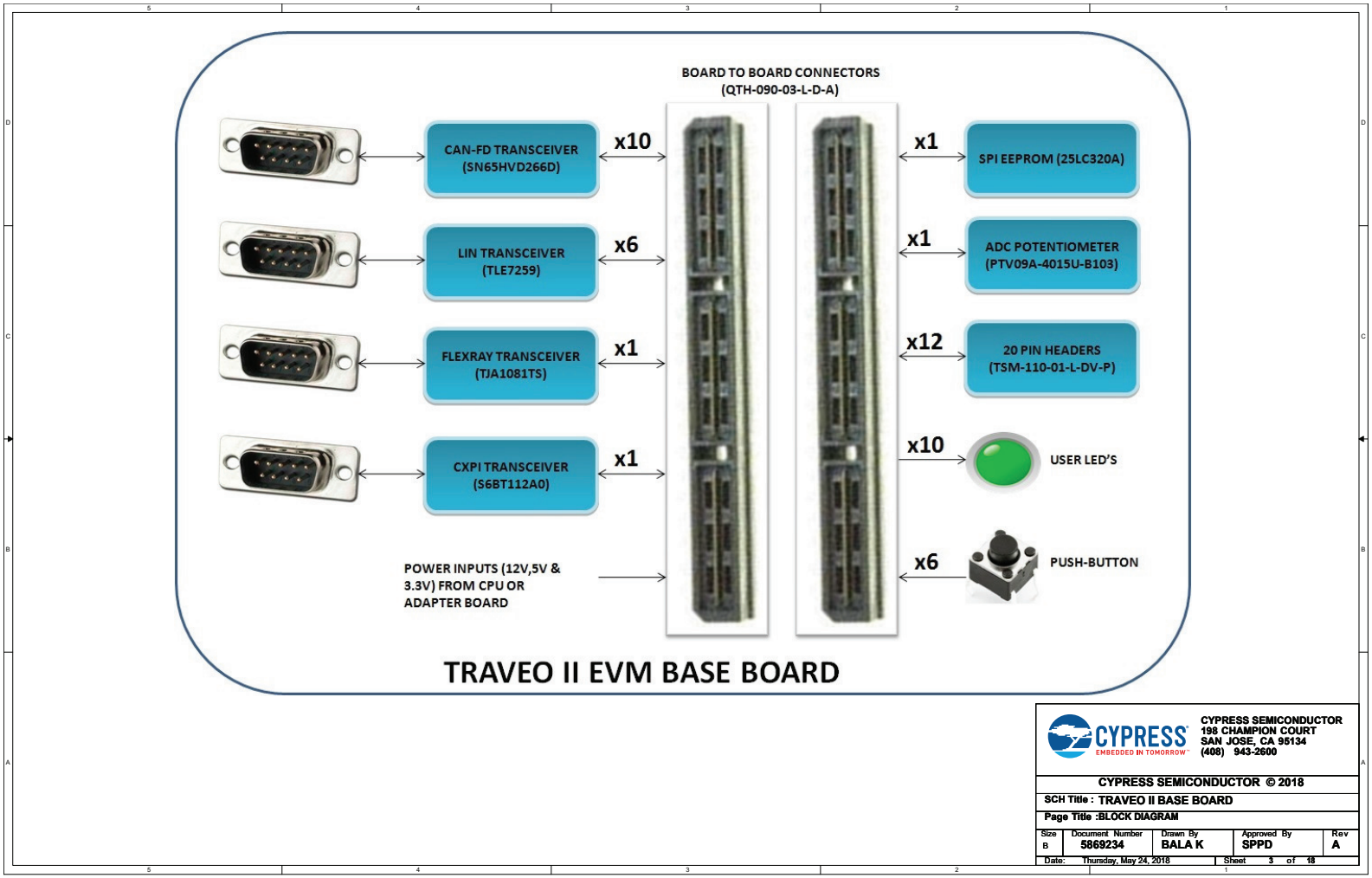


Figure C-2. BTOB Connector-01

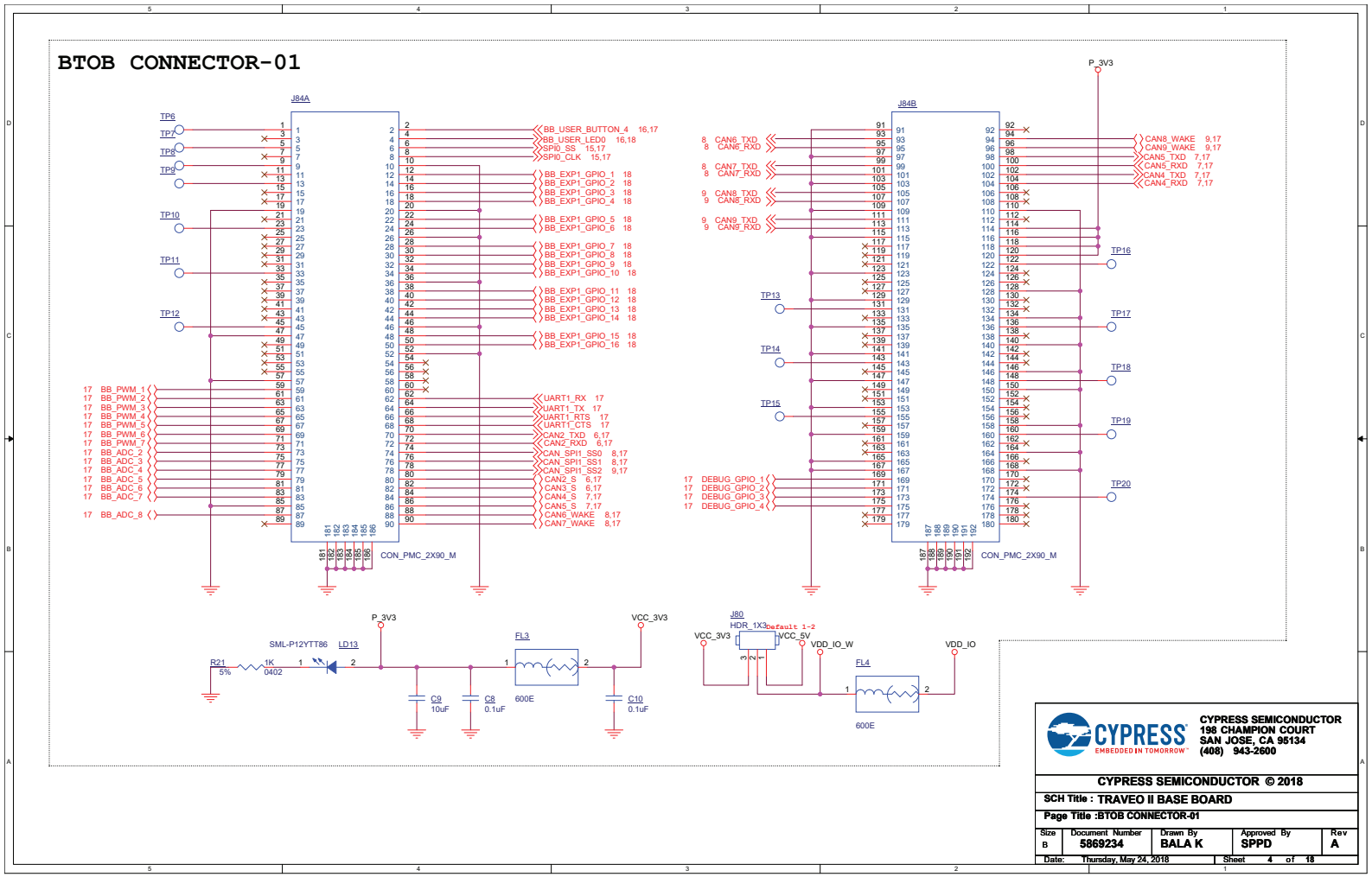


Figure C-3. BTOB Connector-02

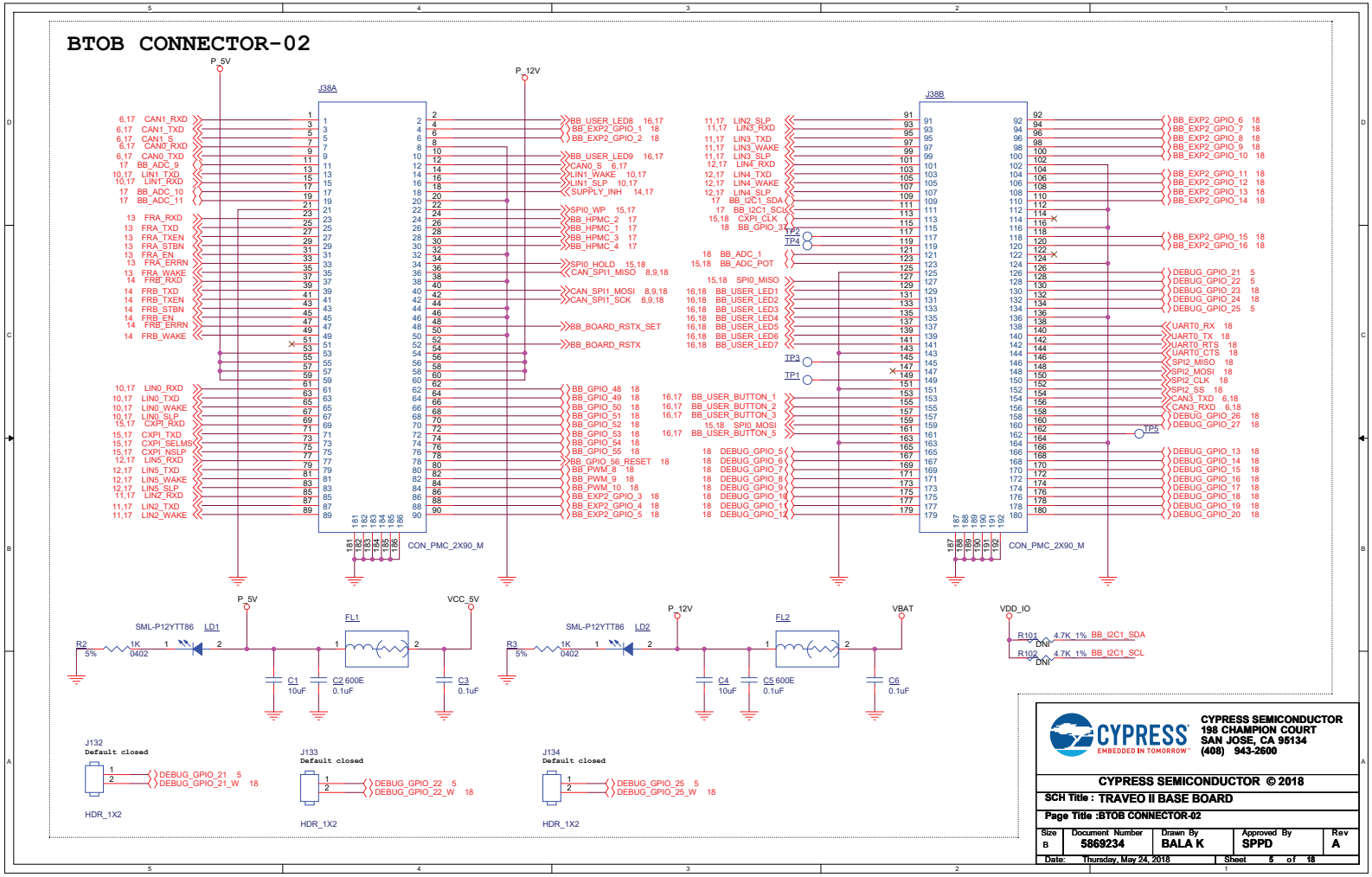


Figure C-4. CAN-FD_0 to 3

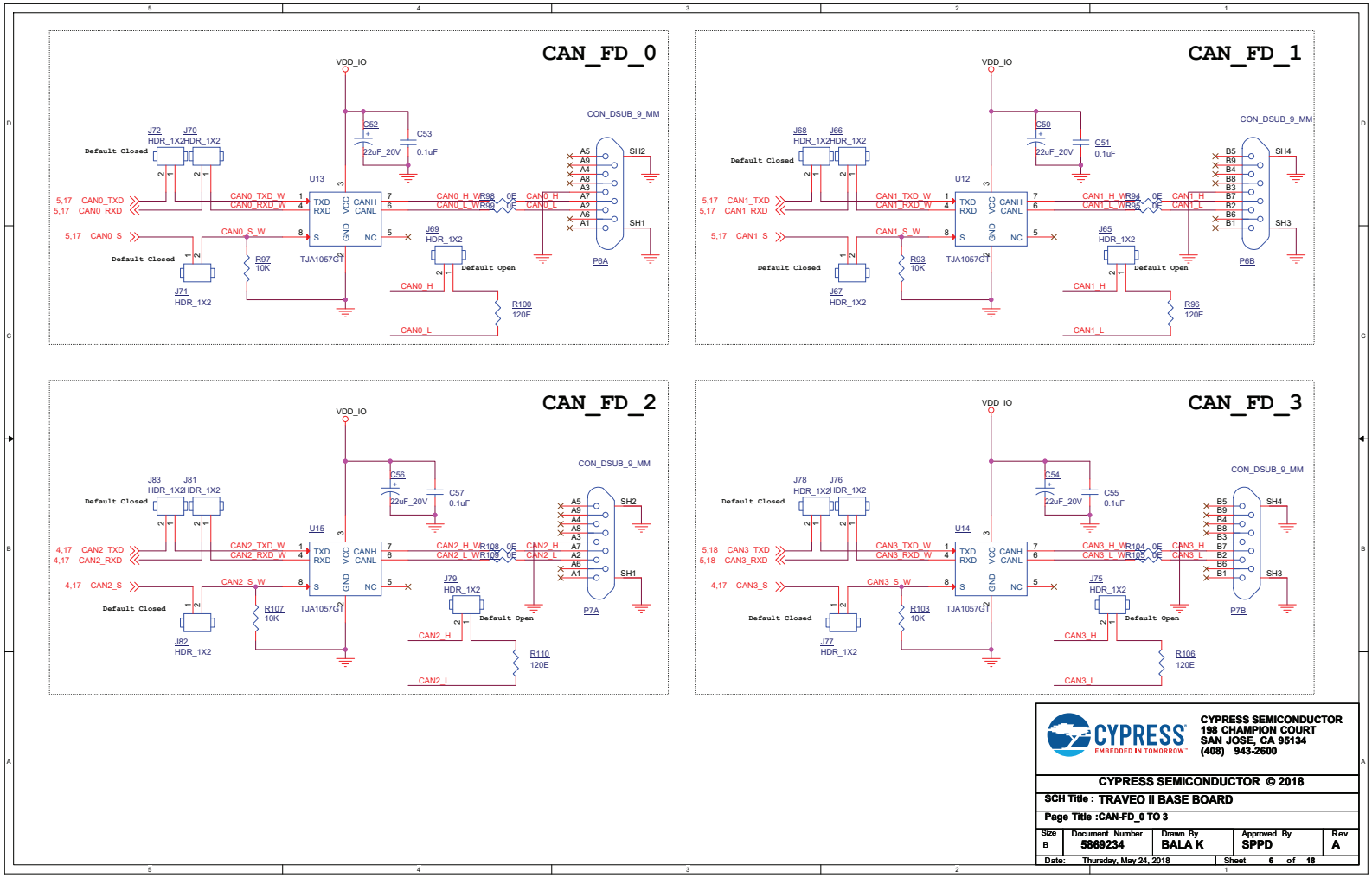


Figure C-5. CAN-FD_4 & 5

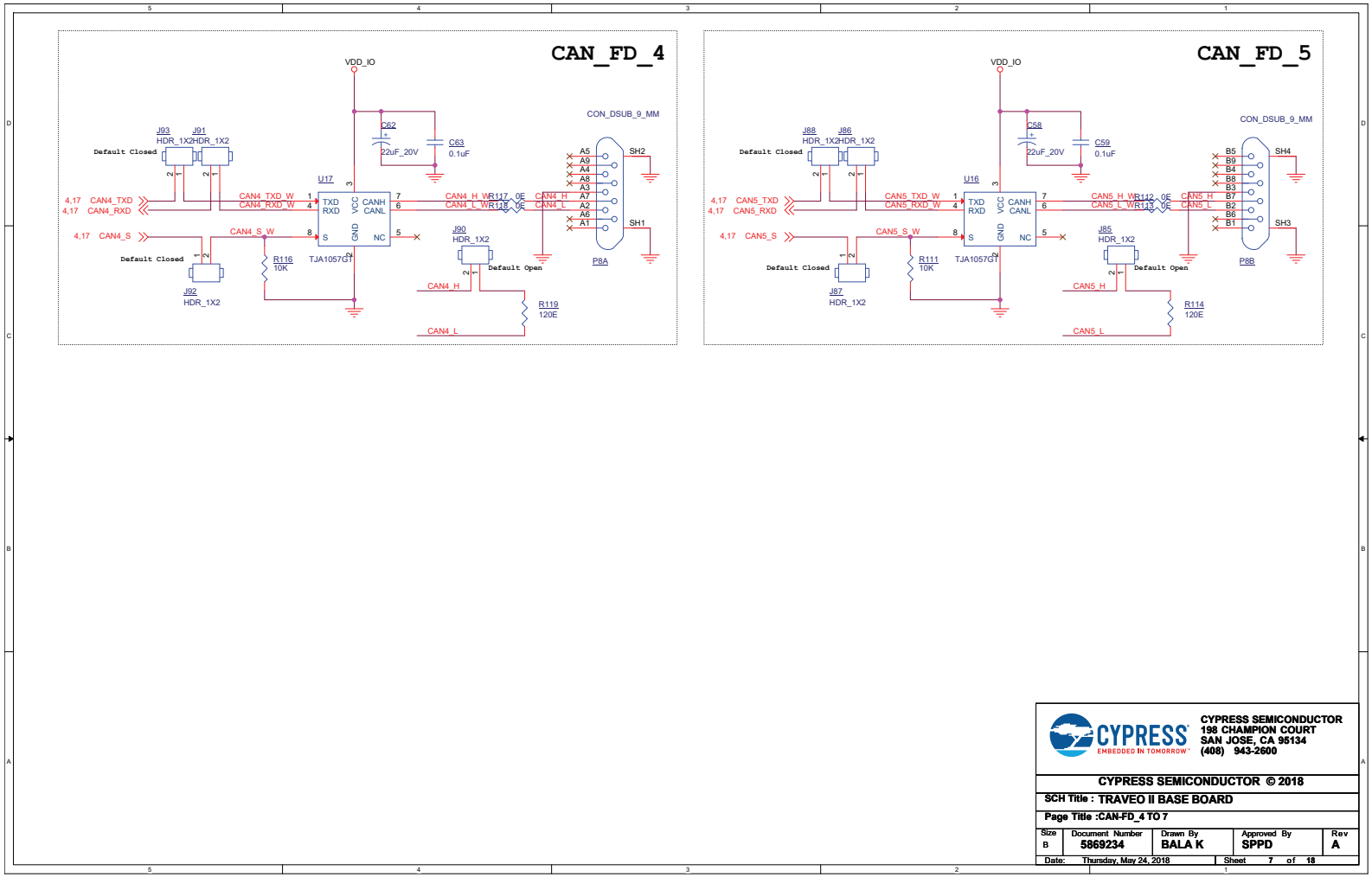


Figure C-6. CAN-FD_6 & 7

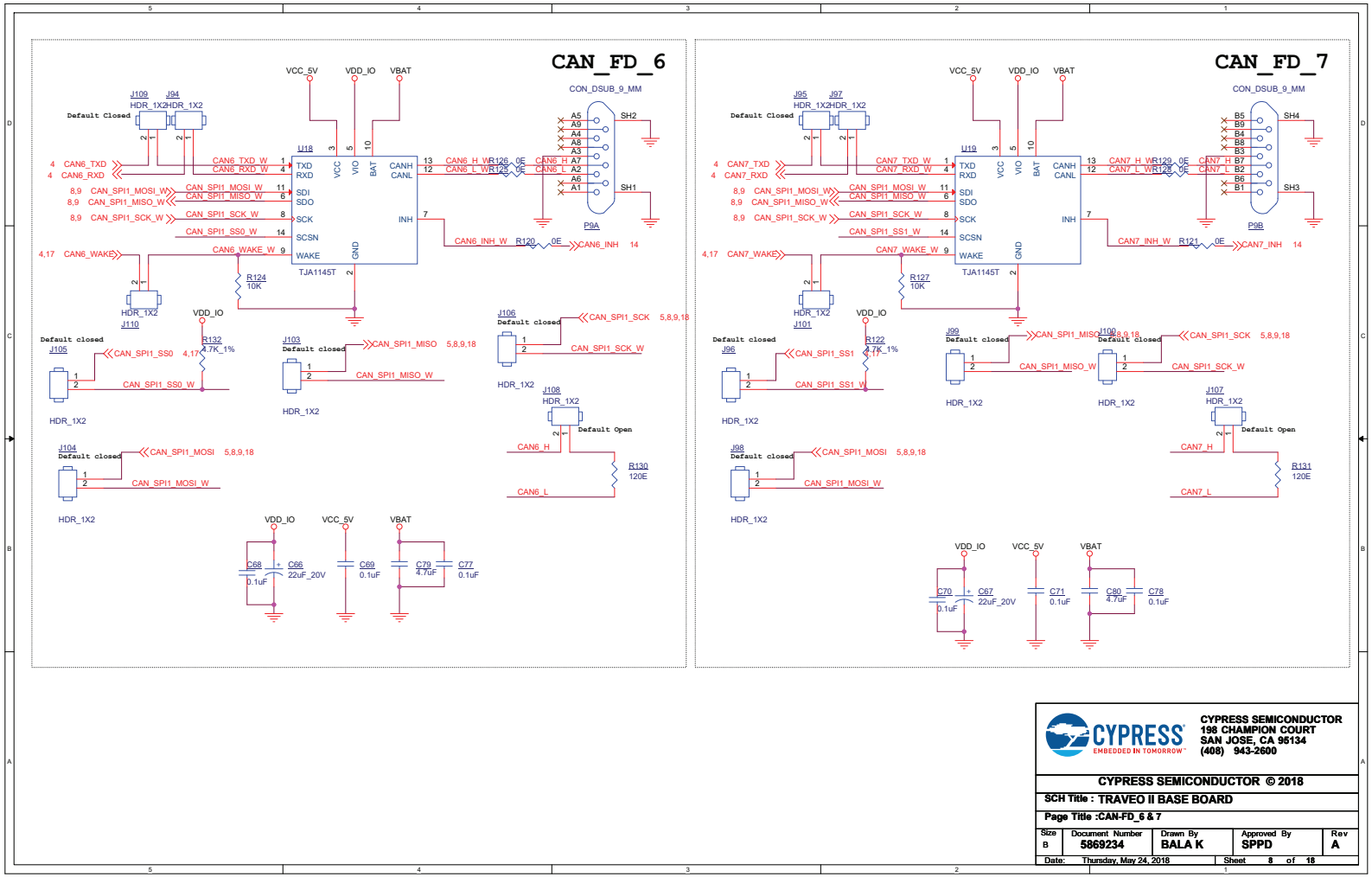


Figure C-7. CAN-FD_8 & 9

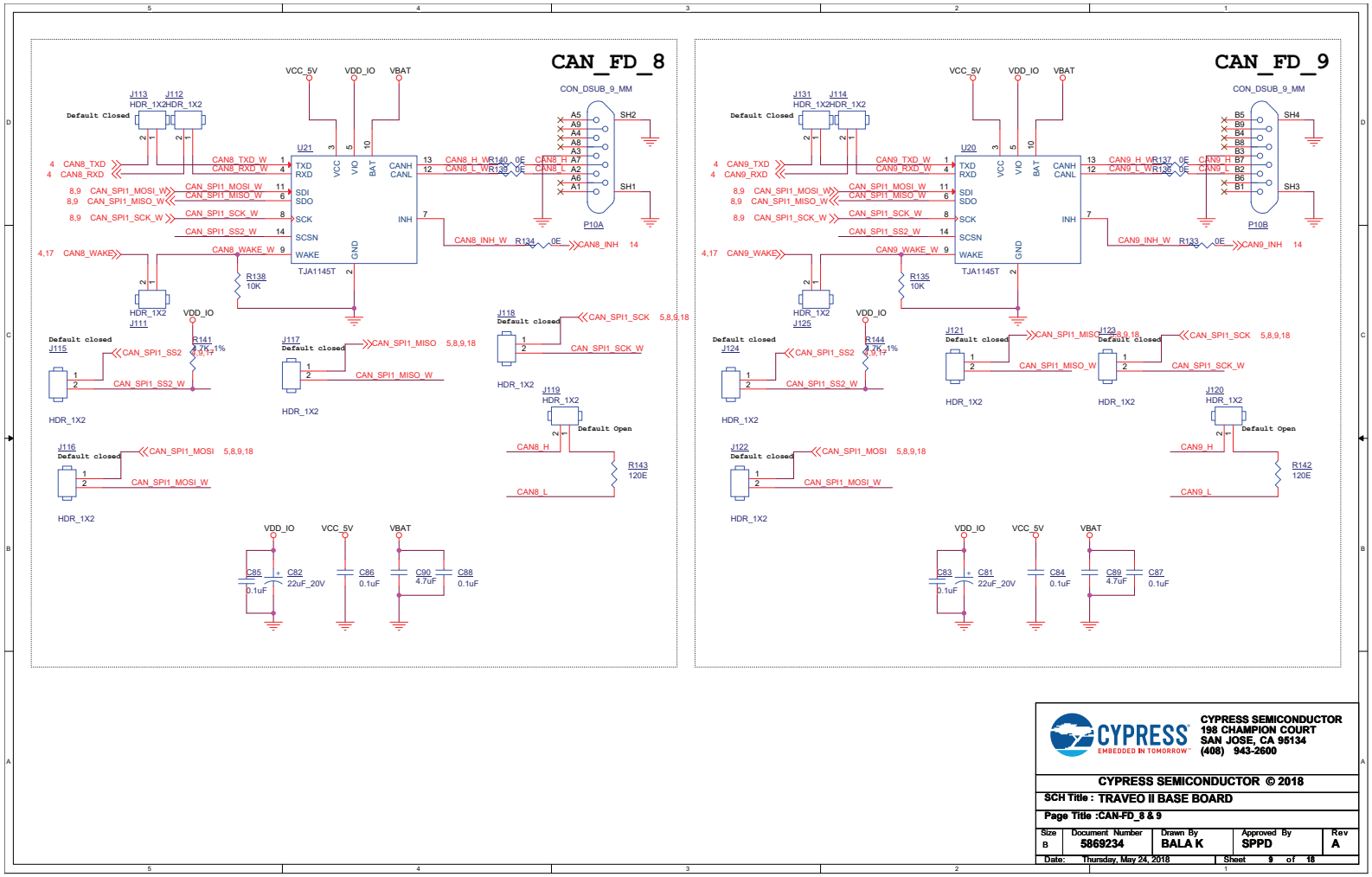


Figure C-8. LIN Interface_0 to 1

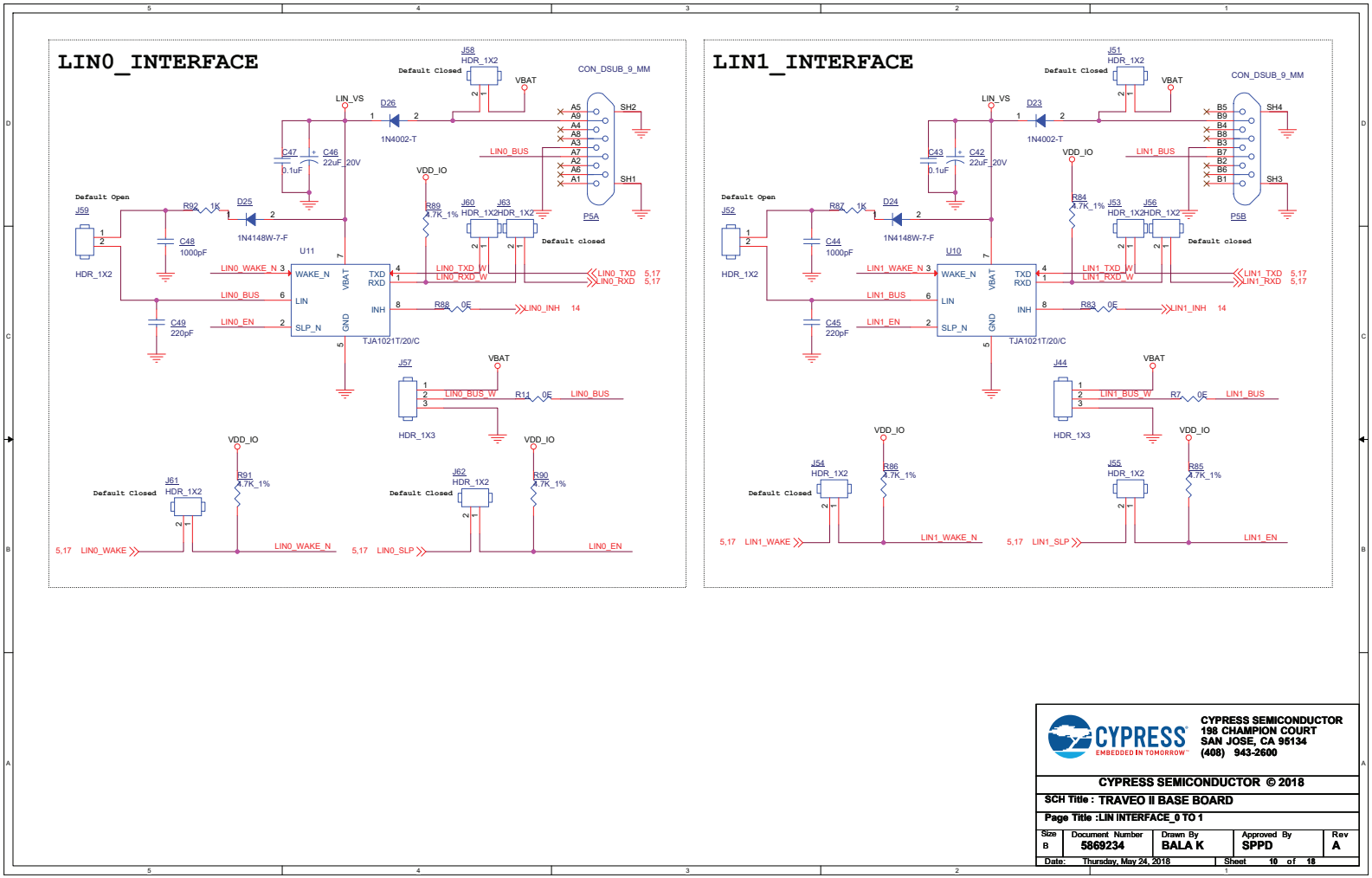


Figure C-9. LIN Interface_2 to 3

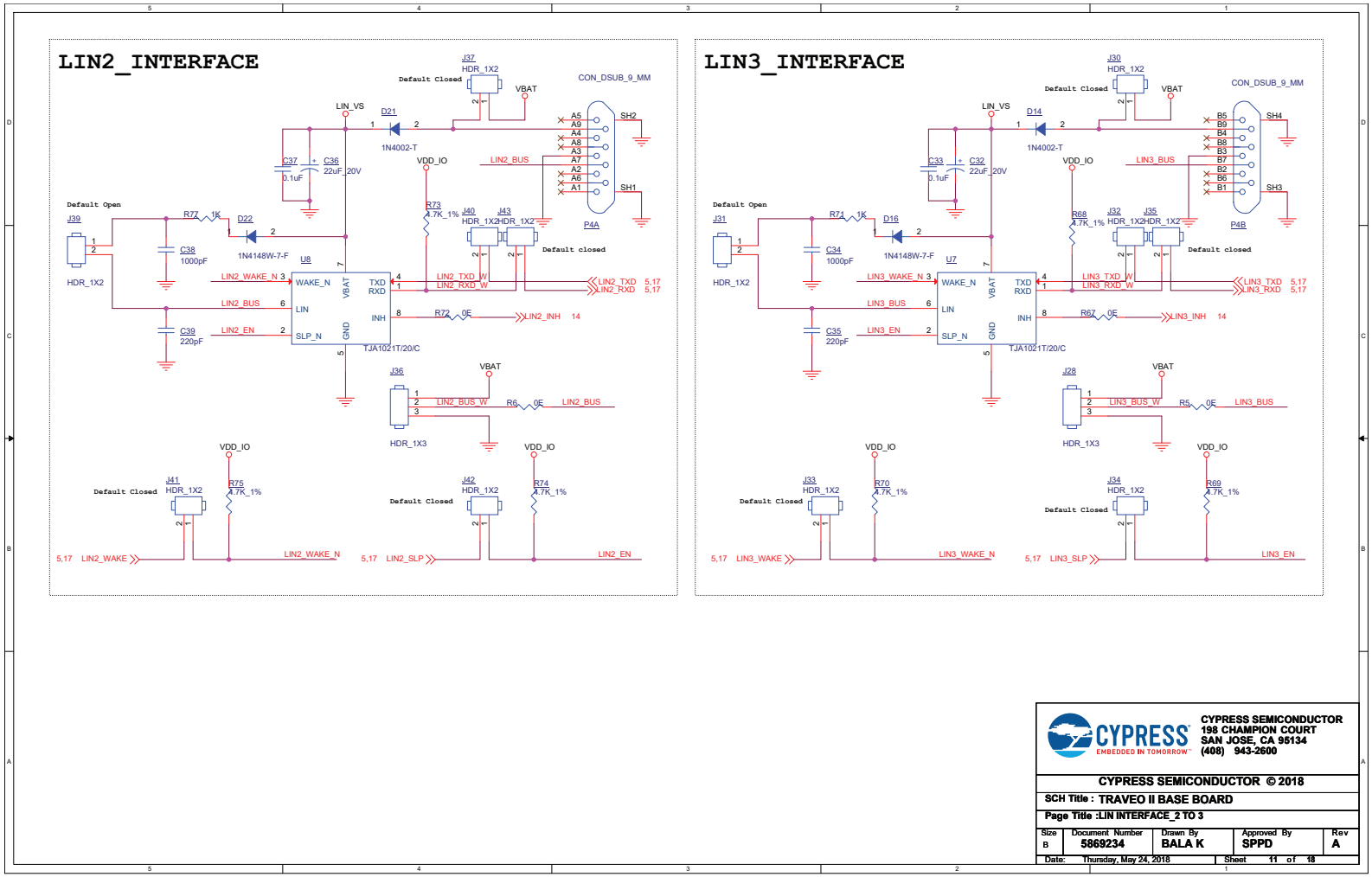


Figure C-10. LIN Interface_4 to 5

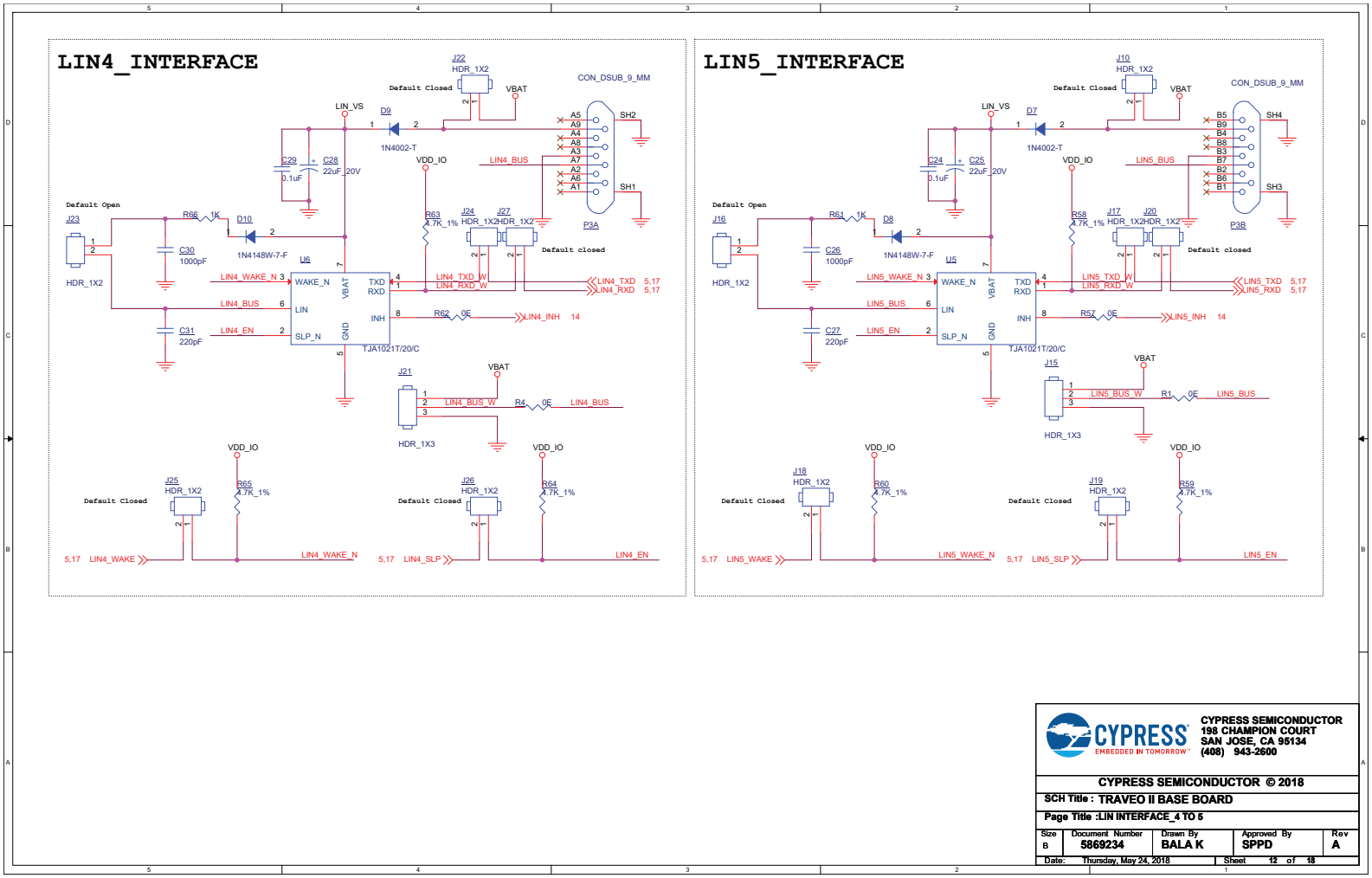


Figure C-11. FlexRay-01 & Reset

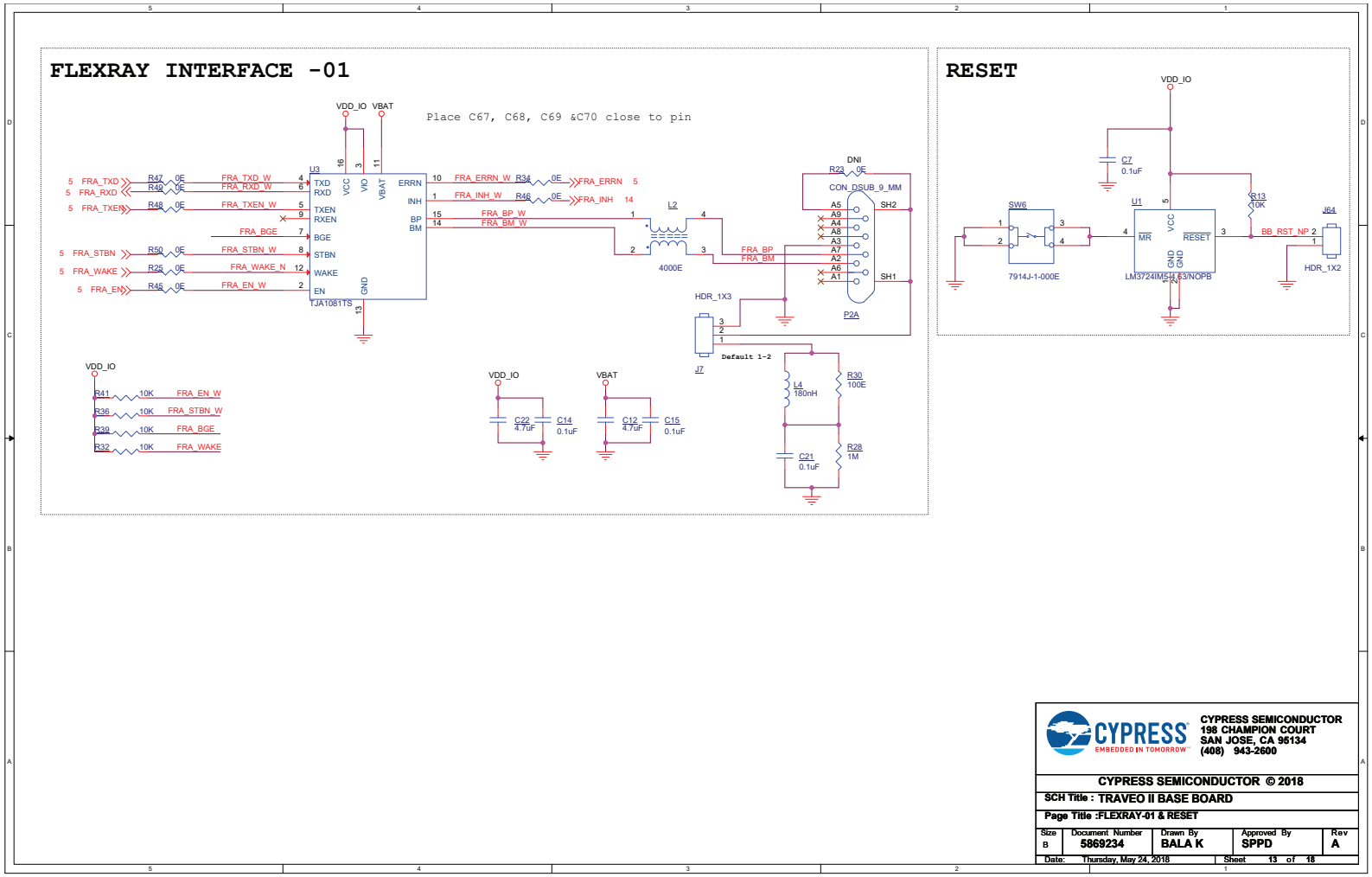


Figure C-12. FlexRay-02 & INH

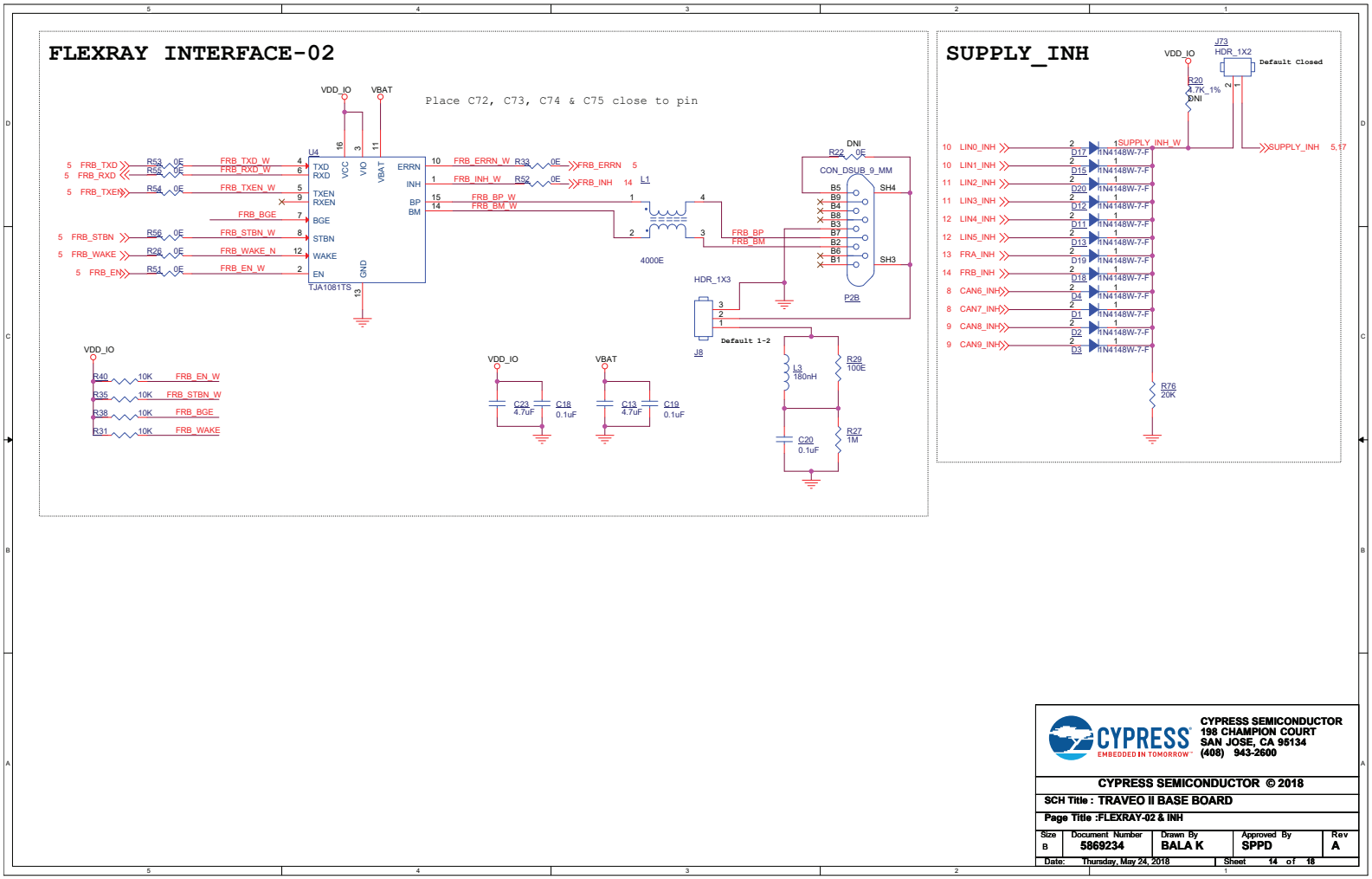


Figure C-13. CXPI, EEPROM & POT

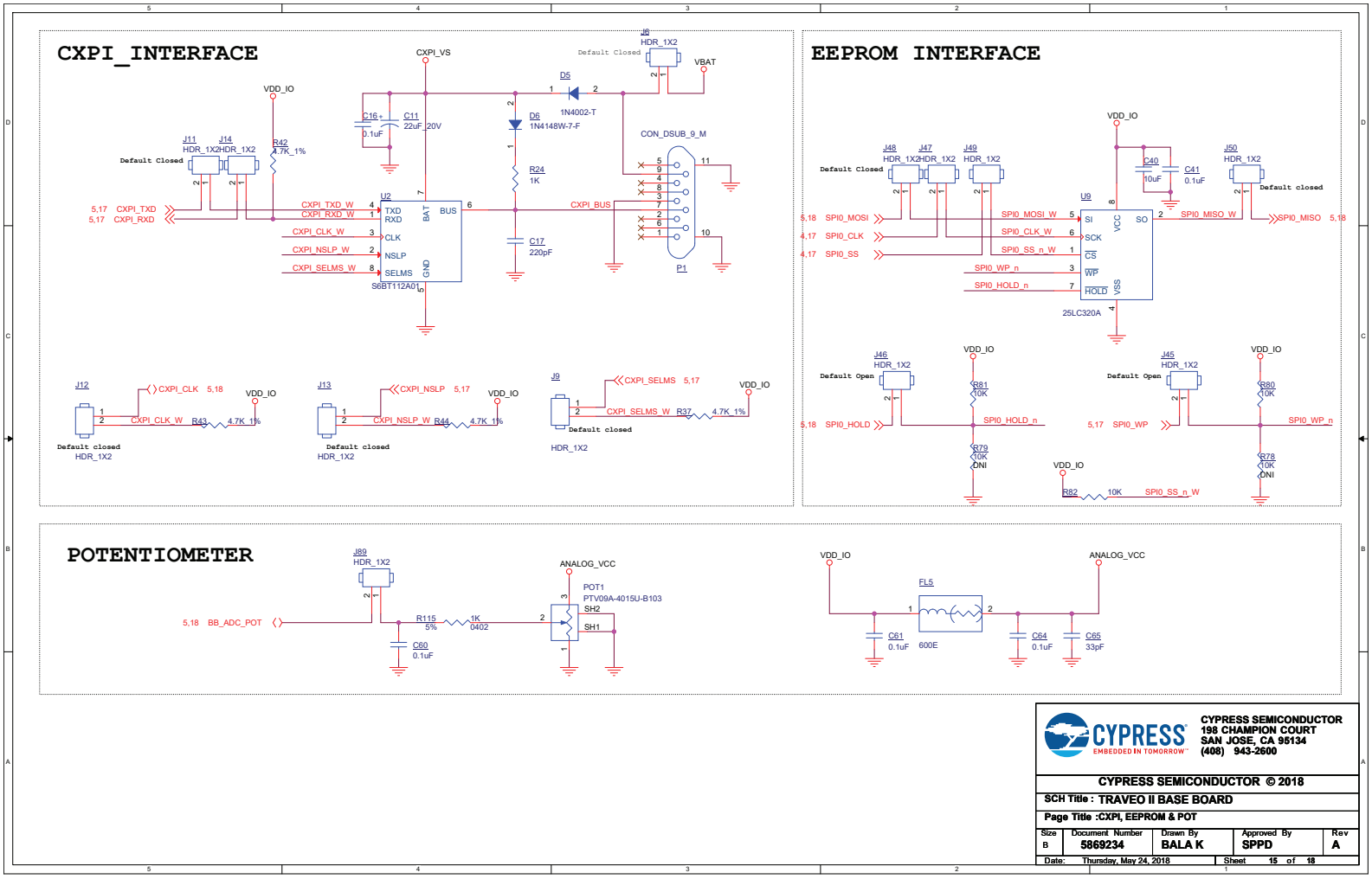


Figure C-14. User_Led & Pushbutton

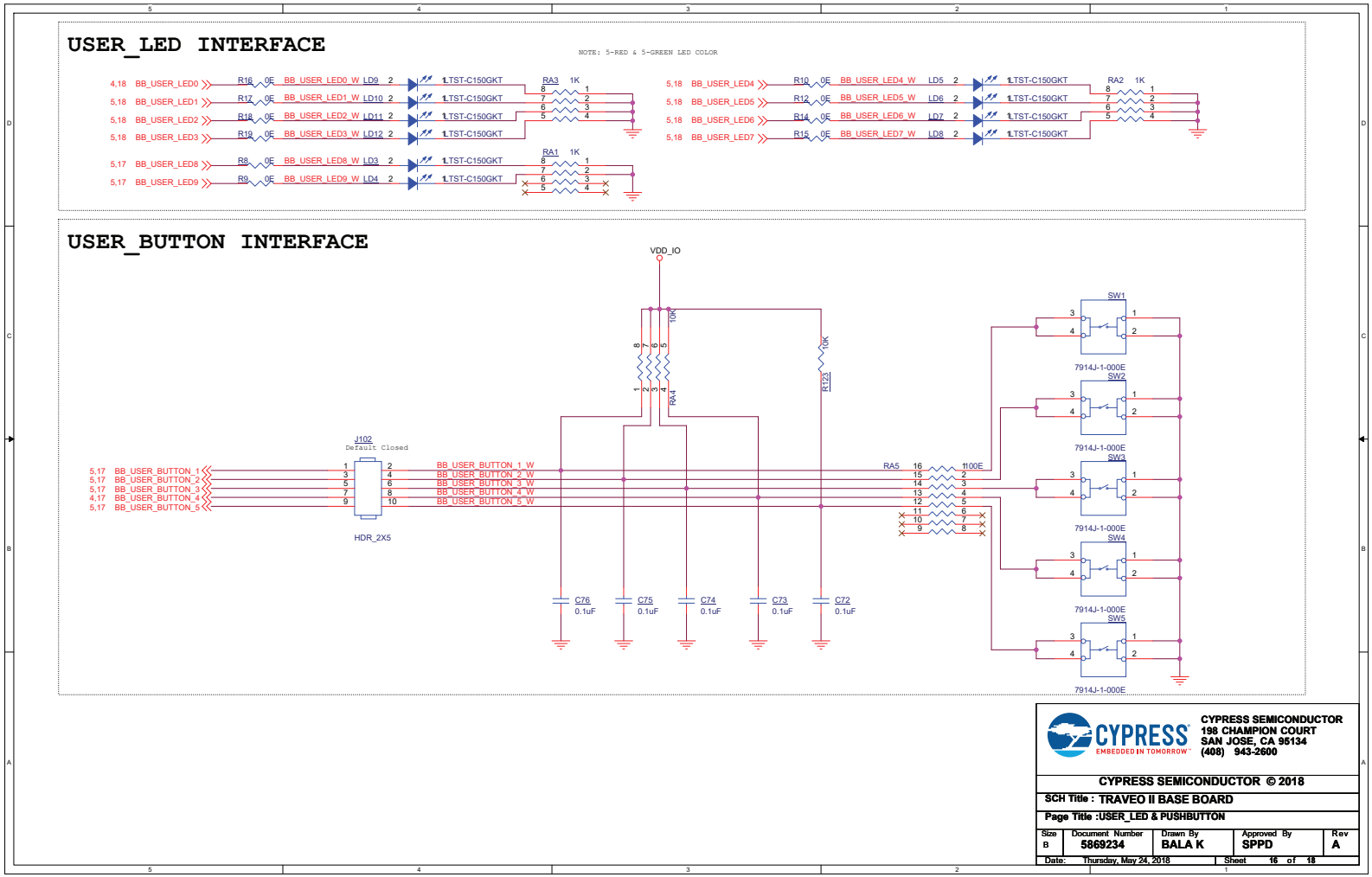


Figure C-15. Pin Header Section-01

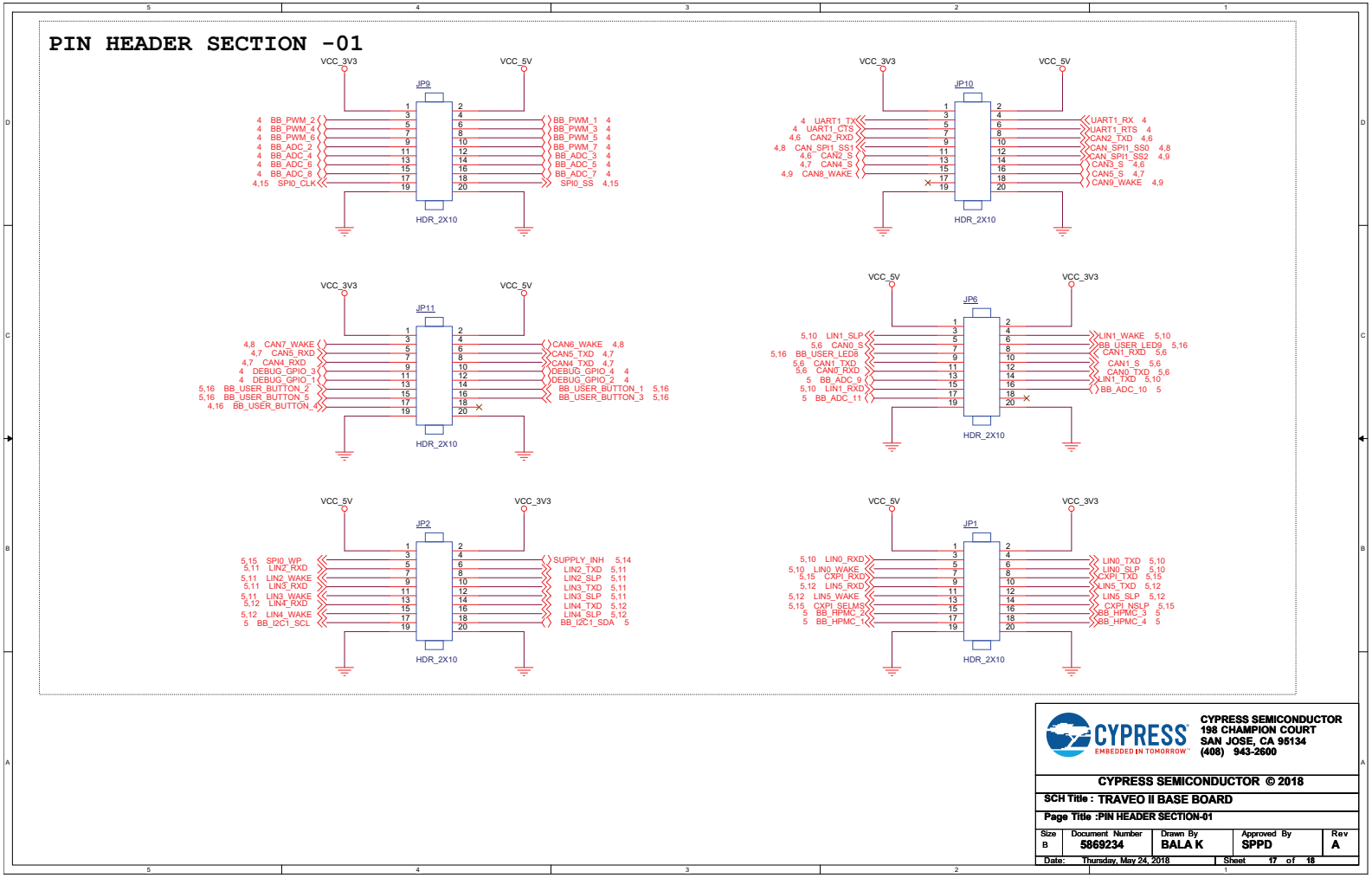
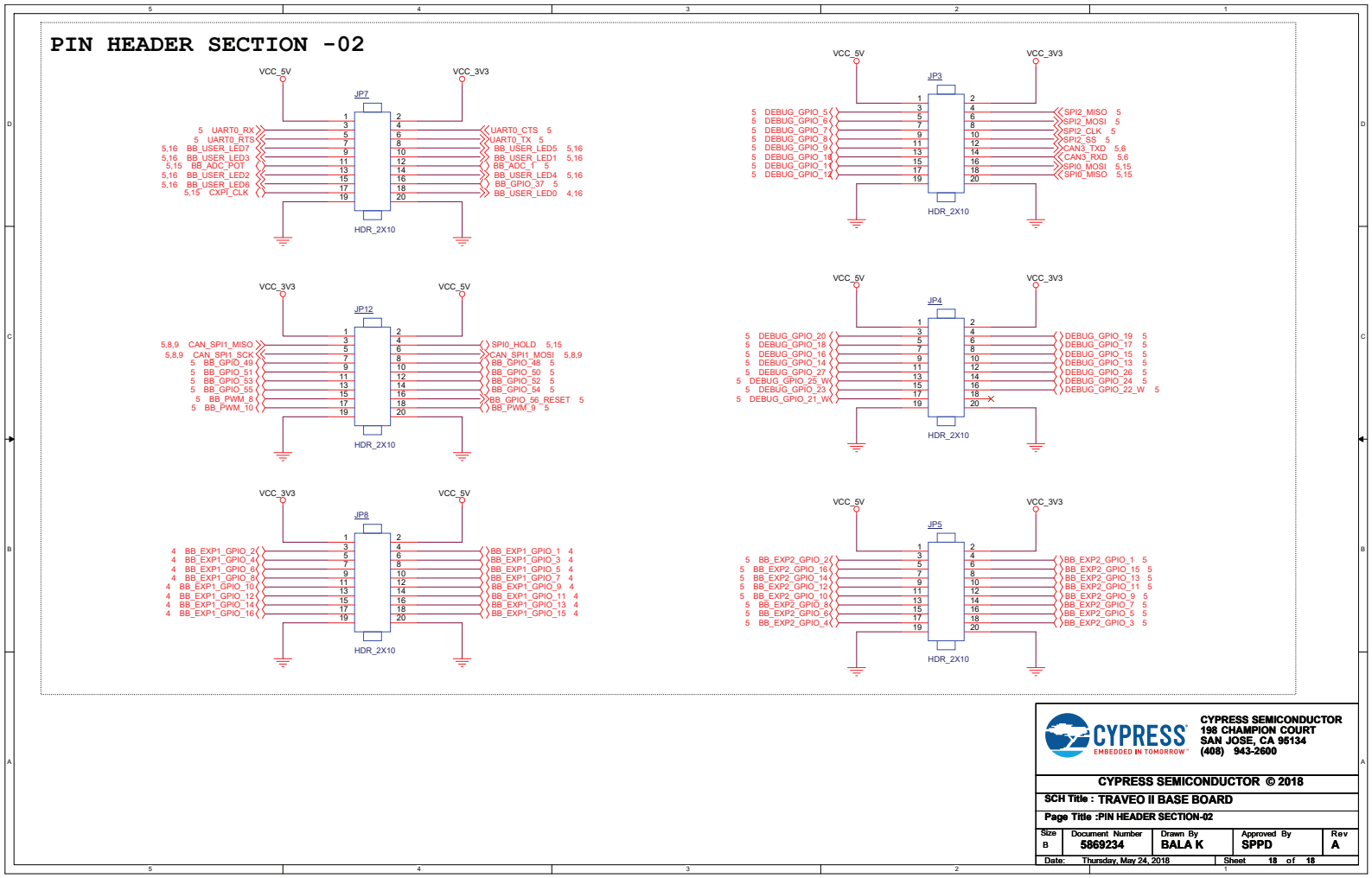


Figure C-16. Pin Header Section-02



D. Component Assembly on Base Board

This appendix shows the top and bottom assembly of the Traveo II Base board (CYTVII-B-E-BB).

Figure D-1. Component Assembly (Top)

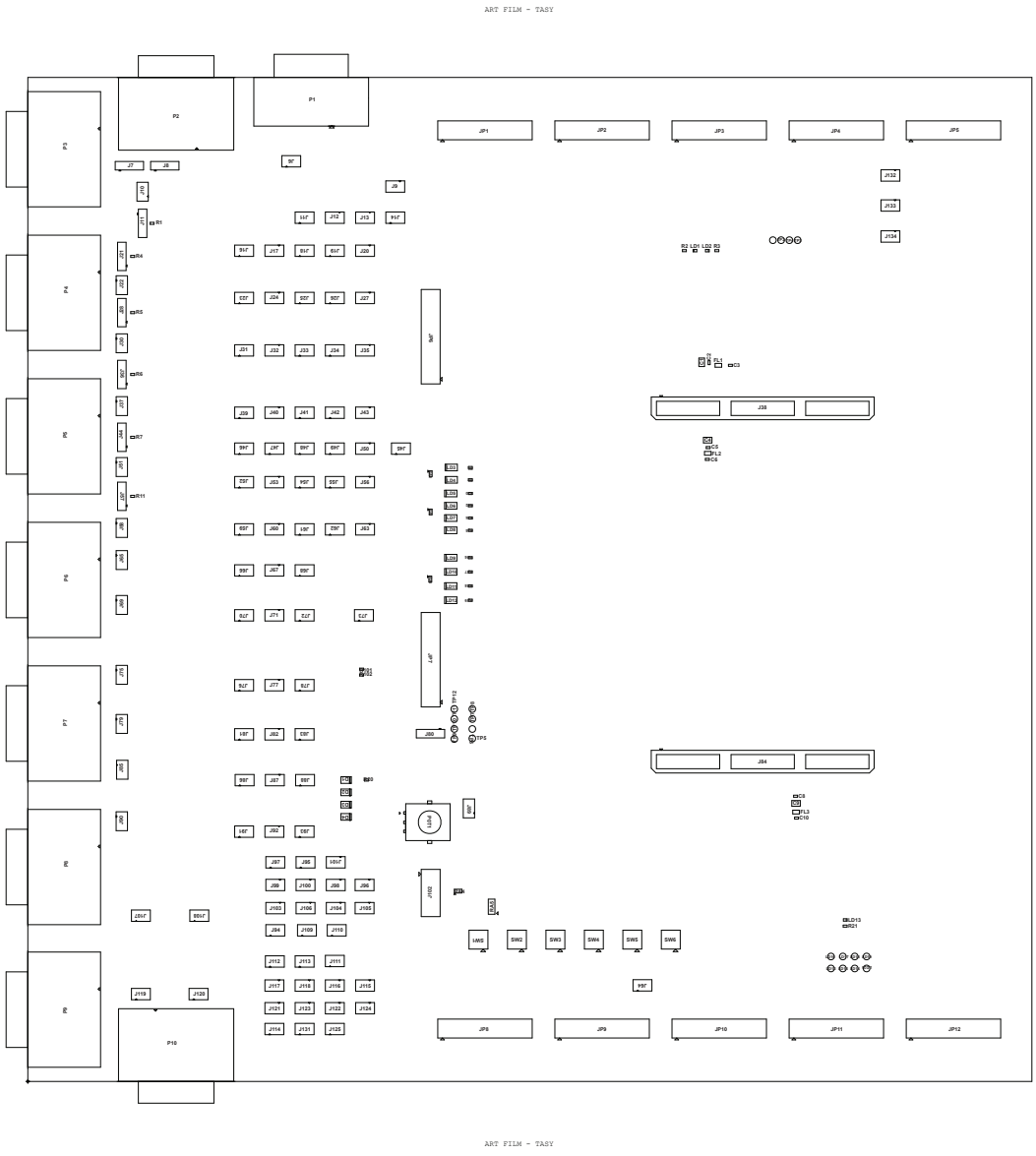
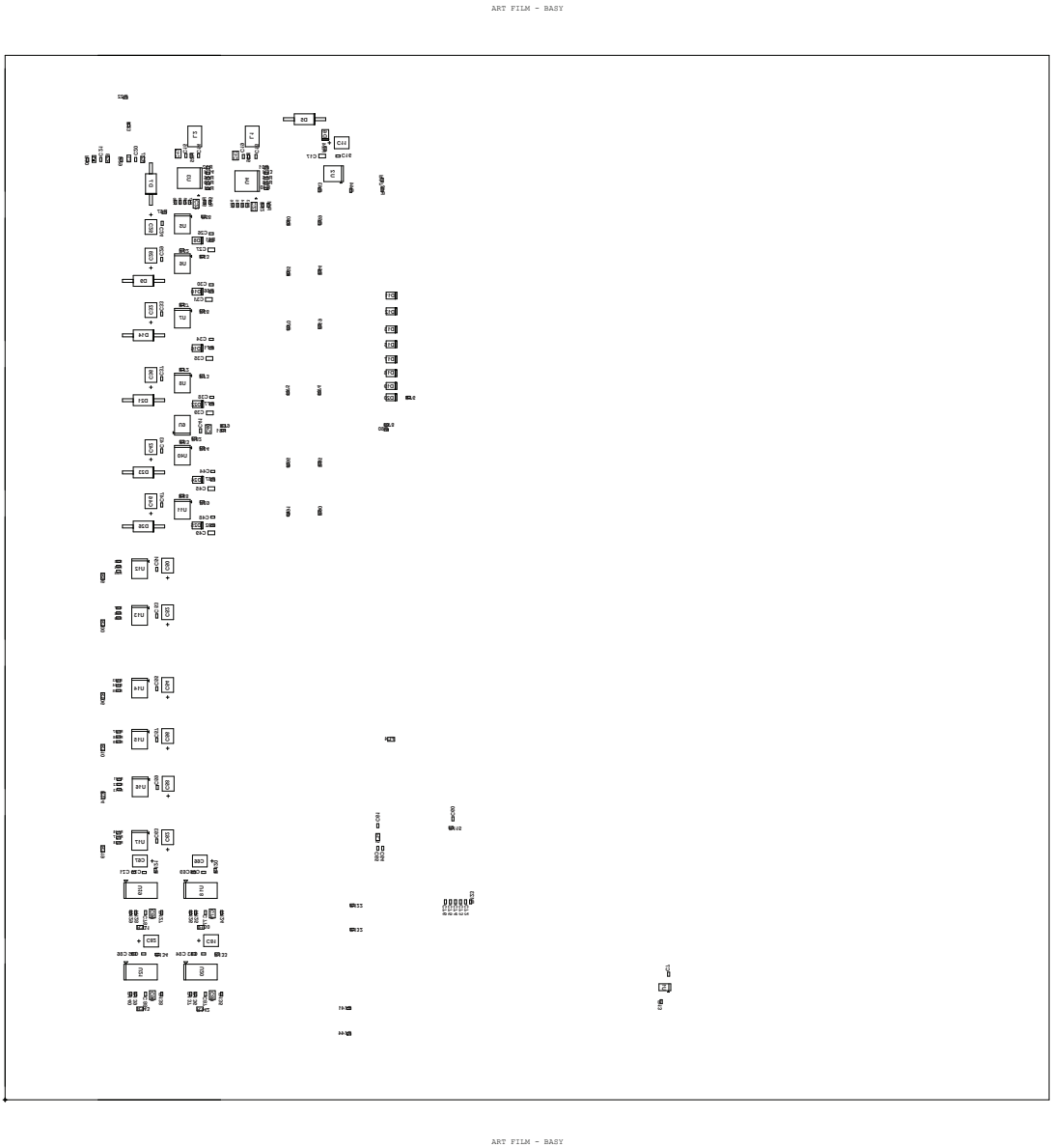


Figure D-2. Component Assembly (Bottom)



Revision History

Document Revision History

Document Title: CYTVII-B-H-8M-320-CPU Evaluation Board User Guide Document Number: 002-26716			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	6605794	06/27/2019	New User Guide
*A	6835229	04/09/2020	The following changes are made with reference to TVII-B-H-8M 320 Rev B0 & B1 silicon: Updated Figure 2-5, Figure 2-6, Figure 2-7, Figure 2-8, Figure 2-9, Figure 2-10, and Figure 2-11. Updated Table 4-1. Updated A. Schematics of CPU Board and B. Component Assembly on CPU Board Schematics.