

# Customer Training Workshop

## Traveo™ II CAN FD Controller

Q4 2020



# Target Products

› Target product list for this training material:

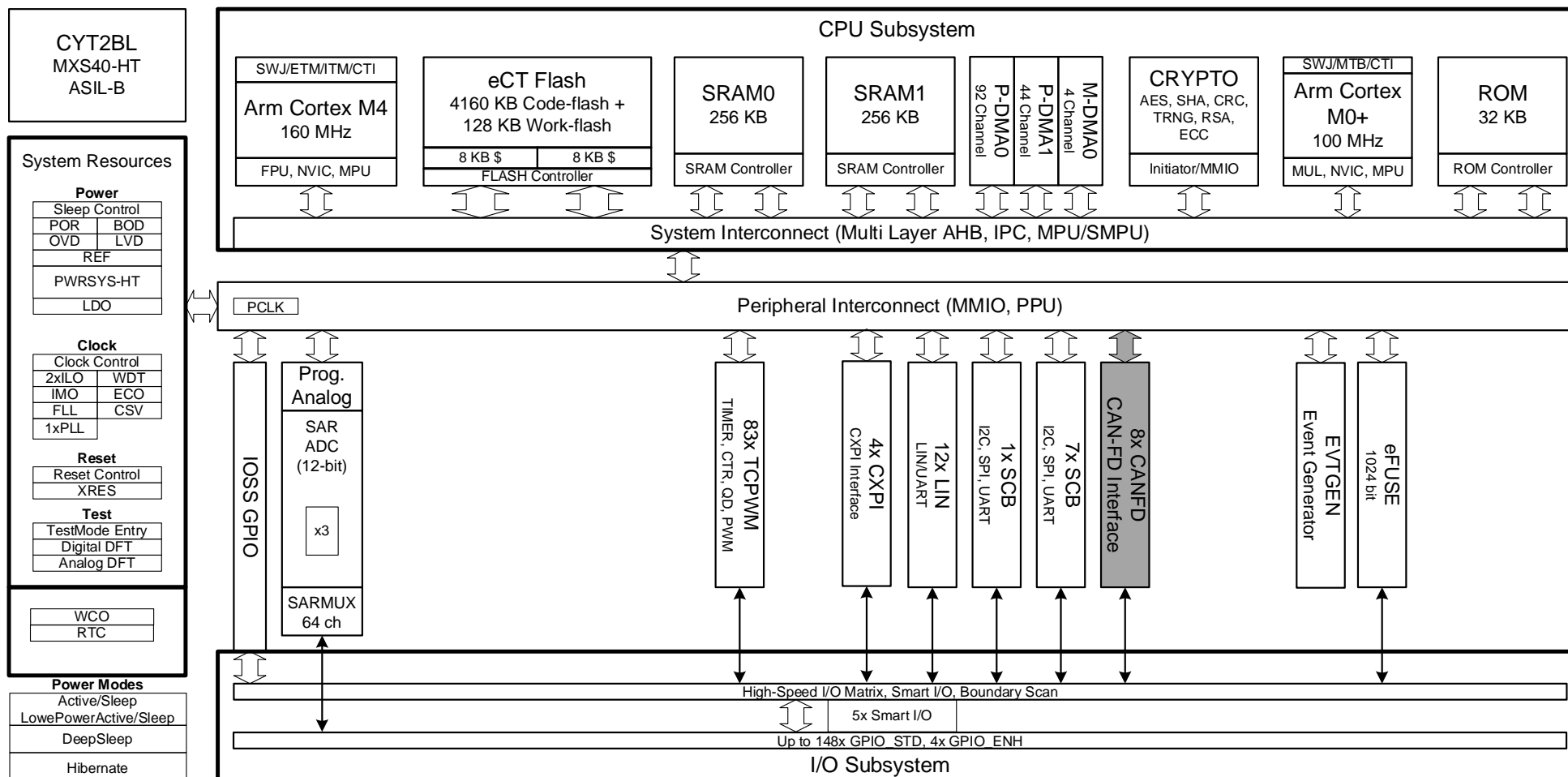
Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576 KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT3BB/ CYT4BB	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384 KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160 KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336 KB

# Introduction to Traveo II Body Controller Entry

## > CAN FD is part of the peripheral blocks

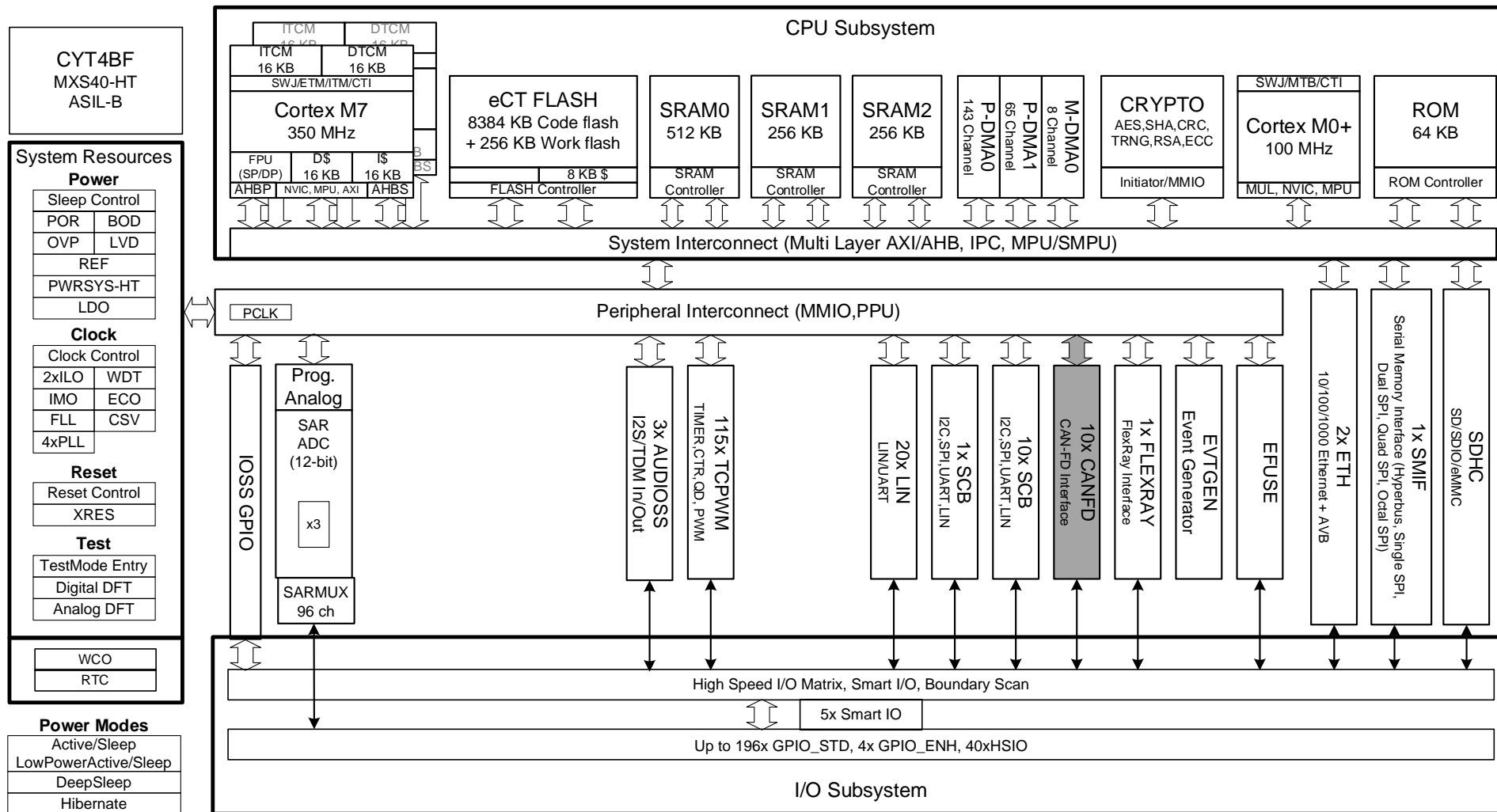
**Hint Bar**

**Review TRM chapter 23 for additional details**



# Introduction to Traveo II Body Controller High

## > CAN FD is part of the peripheral blocks

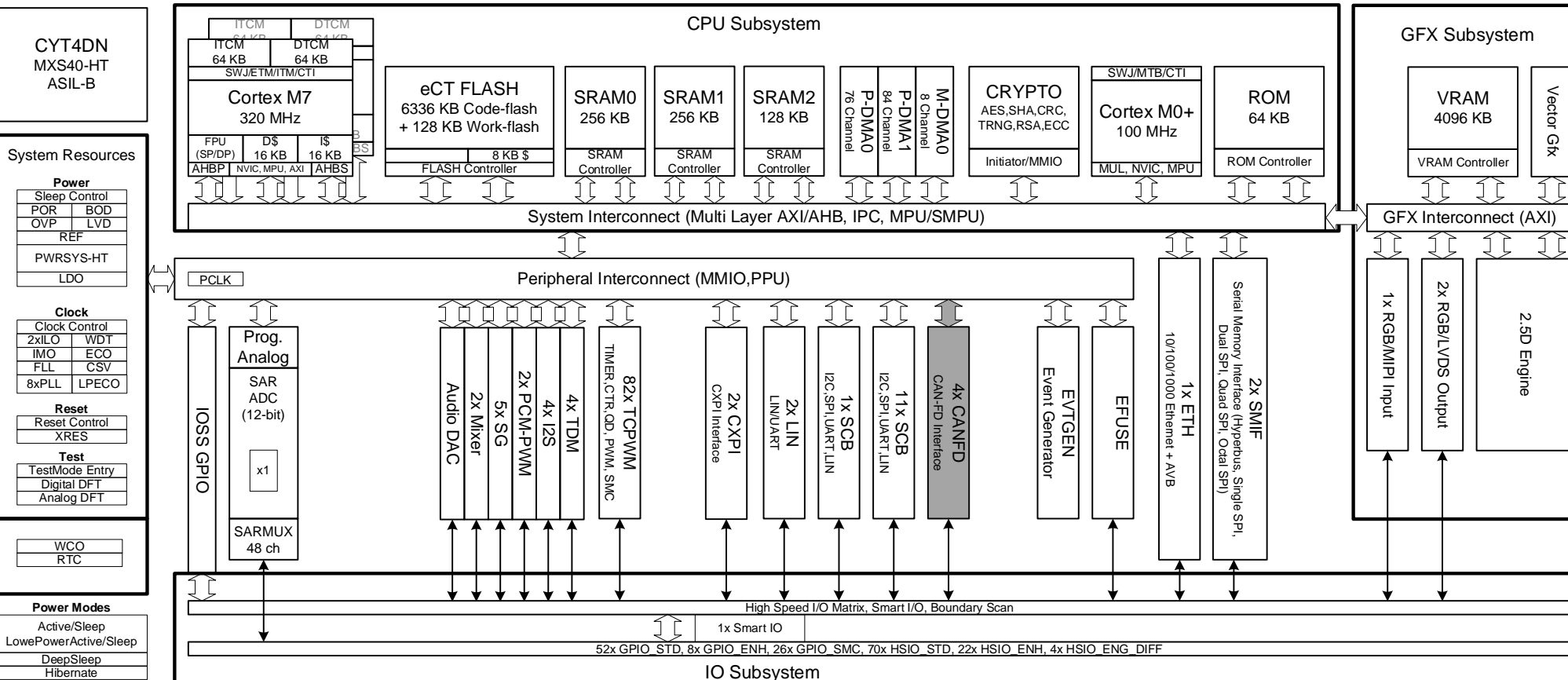


**Hint Bar**

**Review TRM chapter 24 for additional details**

# Introduction to Traveo II Cluster

## > CAN FD is part of the peripheral blocks



**Hint Bar**

**Review TRM chapter 24 for additional details**

# CAN-FD Controller Overview

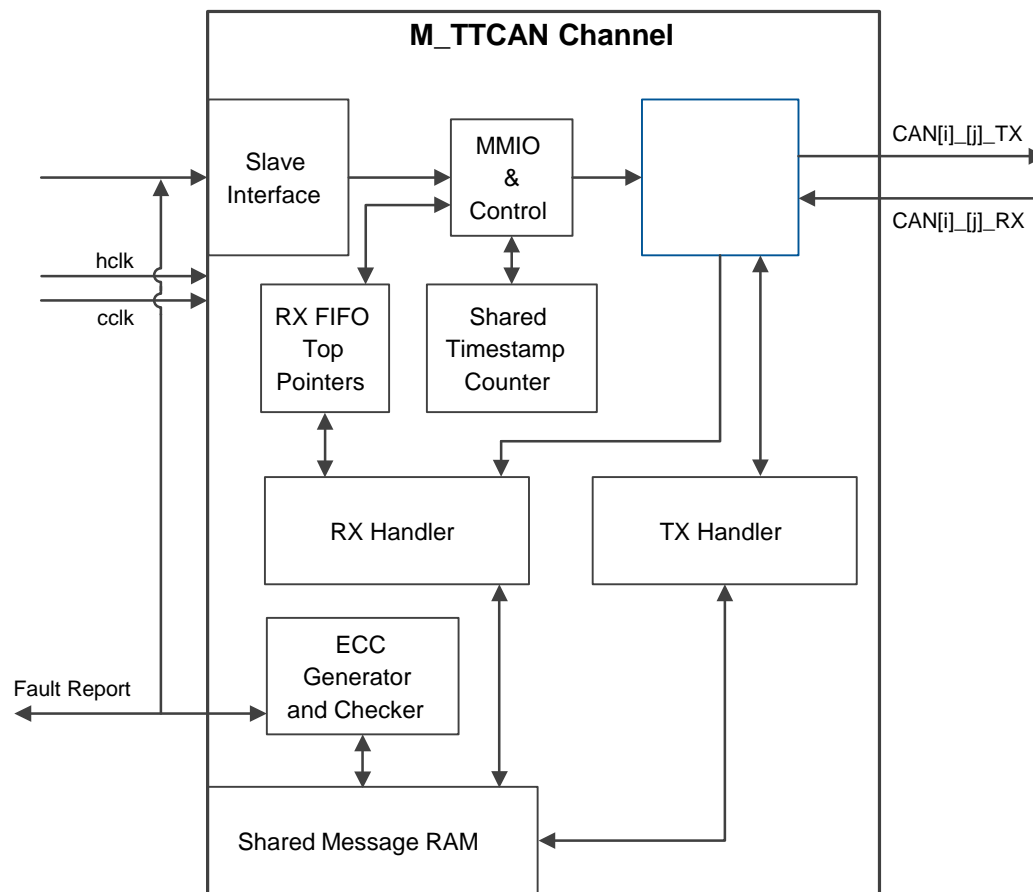
- > Overview
  - ISO11898-1:2015 standard
  - Supports up to 8 Mbps
- > Features
  - Flexible datarate (FD) with up to 64 data bytes per message
  - Time-Triggered (TT) communication on CAN (ISO 11898-4: 2004)
  - Programmable loopback test mode
  - Shared timestamp counter
  - Acceptance filtering
  - Receive FIFO top pointer
  - Enables DMA access on the FIFO
  - Shared Message RAM (MRAM)
  - Error-correcting code (ECC) generator and checker

## Hint Bar

Review datasheet and section 1 of the CAN FD TRM chapter for additional details

# CAN FD Controller Block Diagram

## > CAN FD controller components

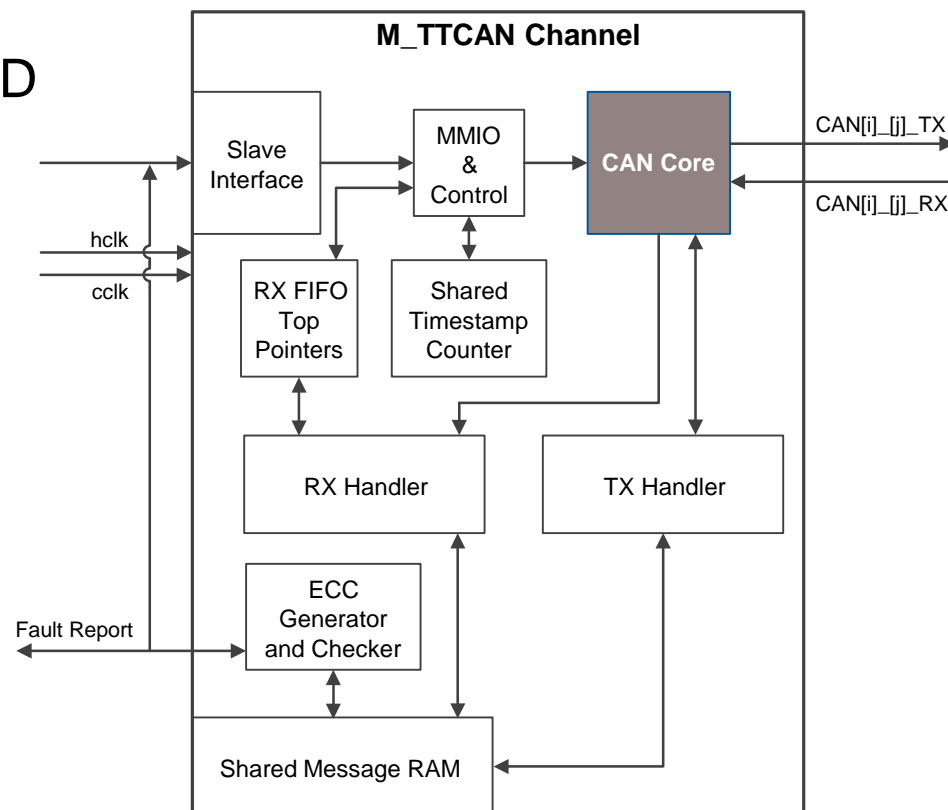


### Hint Bar

Review section 2.1 of the CAN FD TRM chapter for additional details

# CAN Core

- > Classic CAN & CAN FD operation
  - Supports Standard and Extended ID
- > Transmitter Delay Compensation
  - Supports the transmitter delay measurement and offset setting
- > Power Down
  - Supports sleep mode
- > Test Mode
  - Supports loopback mode
- > Interrupt
  - Two types of interrupts



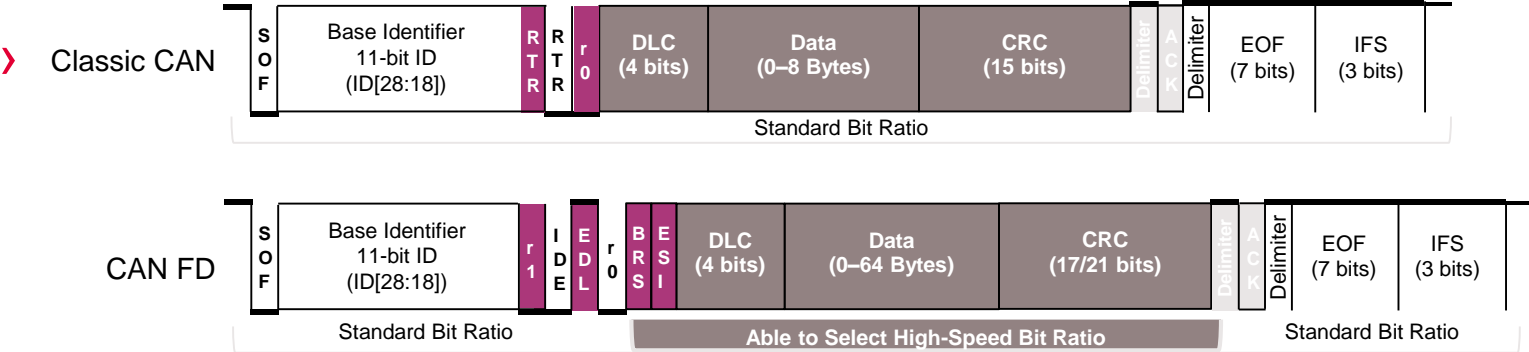
## Hint Bar

Review section 3.1 of the CAN FD TRM chapter for additional details

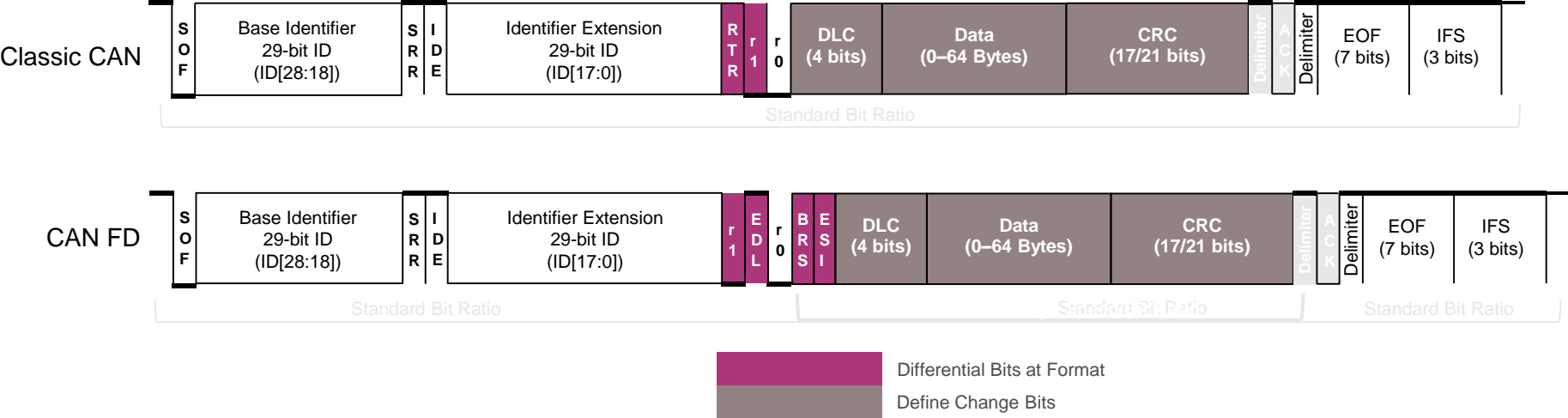


# Classic CAN & CAN FD Operation

## > Standard format (11-bit ID)



## > Extended format (29-bit ID)



### Hint Bar

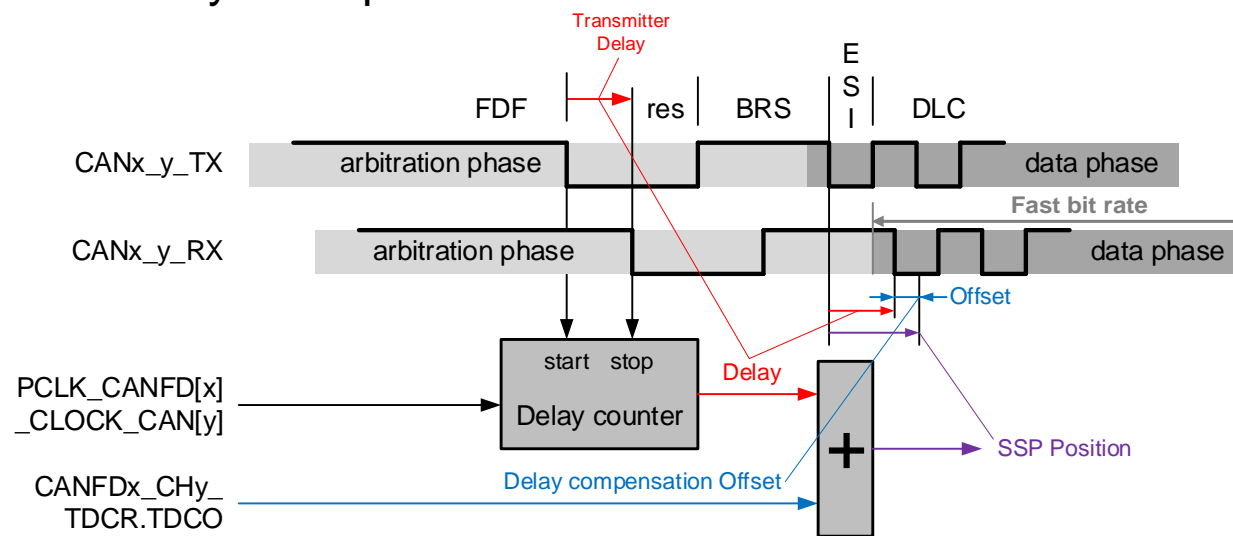
Review section 3.1 of the CAN FD TRM chapter and Register TRM for additional details

# Transmitter Delay Compensation

- > Supports the transmitter delay measurement and offset setting
- > Background
  - When transmitting via CANx\_y\_TX, CAN FD controller receives the transmitted data from its local CAN transceiver via CANx\_y\_RX. The received data is delayed by the transmitter delay. In case this delay is greater than TSEG1<sup>1</sup>, a bit error is detected. To enable a data phase bit time that is even shorter than the transmitter delay, the delay compensation is introduced.
- > Advantage
  - This enables transmission with higher bit rates during the CAN FD data phase, independent of the delay of a specific CAN transceiver

**Hint Bar**

Review section 3.1.4 of the CAN FD TRM chapter and Register TRM for additional details



<sup>1</sup> time segment before sample point

# Power Down (Sleep Mode)

- › A clock provided to the CAN channel can be stopped by raising a clock stop request through the CTL.STOP\_REQ bit
- › After receiving an acknowledge from the CAN channel, hardware automatically stops the clock
- › Clearing CTL.STOP\_REQ allows exit from power down mode<sup>1</sup>
- › All CAN configurations and MRAM except the timestamp counter are retained during DeepSleep mode
  
- › **Advantages:**
  - Unlike older approaches, software does not have to wait for an acknowledge and can be used for other functionality
  - Power down (stopping clock) reduces power consumption when the CAN bus is idle

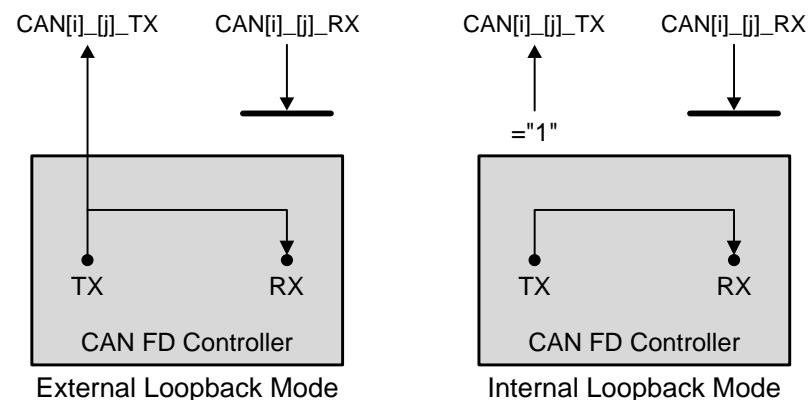
## Hint Bar

**Review section 3.1.8 of the CAN FD TRM chapter and Register TRM for additional details**

<sup>1</sup> CTL.STOP\_REQ must not be cleared before receiving an acknowledge from the CAN channel

# Test Mode

- > External Loopback mode
  - Ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in loopback mode
  - Performs an internal feedback from TX output to RX input
  - Transmitted messages can be monitored at the CAN[i]\_[j]\_TX pin
- > Internal Loopback mode
  - Can be tested without affecting a running CAN system connected to the CAN[i]\_[j]\_TX and CAN[i]\_[j]\_RX pins
- > Use Case
  - CAN diagnosis without the influence of external ECU<sup>1</sup> by using the internal loopback mode



## Hint Bar

Review section 3.1.9 of the CAN FD TRM chapter and Register TRM for additional details

<sup>1</sup> Electrical Control Unit

# Interrupt

- › Each interrupt source in the M\_TTCAN channel can be separately enabled or disabled using the IE register
- › Each enabled interrupt from the channel can be routed either to the interrupt 0 or interrupt 1 line using the ILS and ILE registers. By default, all interrupts are routed to the interrupt 0 line

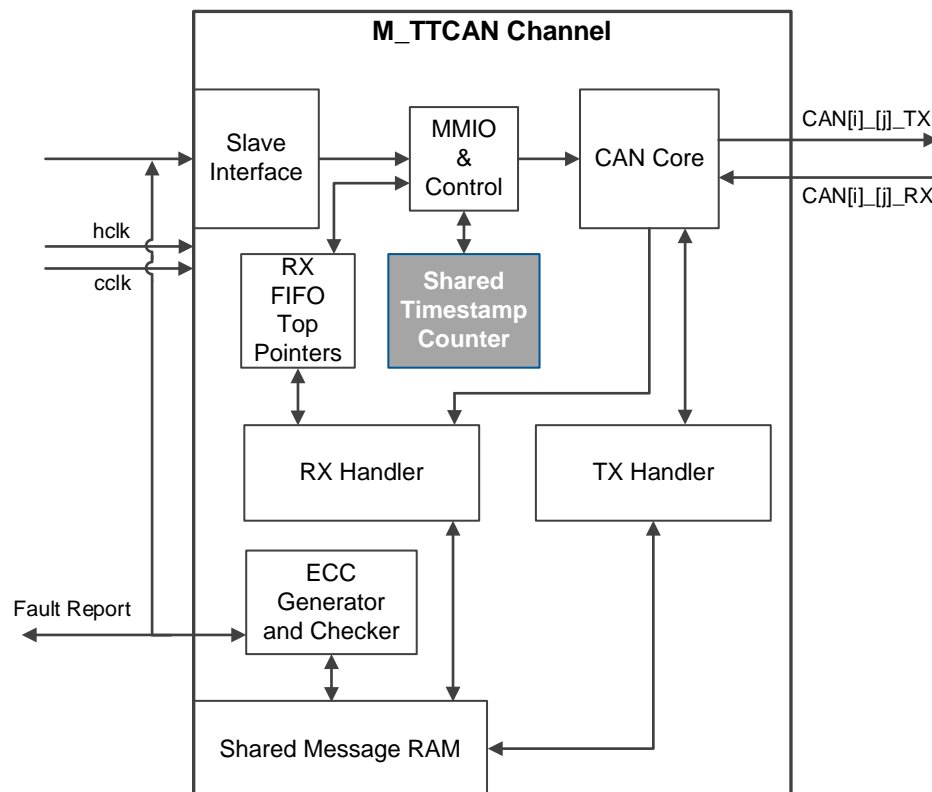
## Hint Bar

**Review section 2.3 of the CAN FD TRM chapter and Register TRM for additional details**

**The description of the IE register in the Register TRM provides a list of all possible interrupt sources**

# Shared Timestamp

- > The shared timestamp counter supports a 16-bit timestamp value.



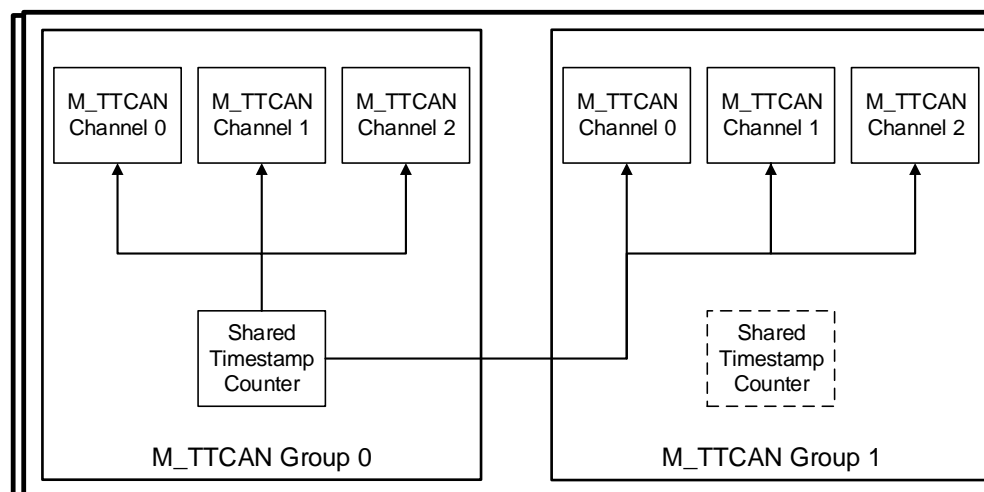
## Hint Bar

Review section 3.2 of the CAN FD TRM chapter for additional details

# Shared Timestamp Counter

- > The timestamp counter records a 16-bit timestamp value when messages are sent or received
- > The captured timestamp value is stored in the respective buffer or FIFO element
- > Advantage:
  - To make event ordering global in the device, the 16-bit timestamp counter is shared among all M\_TTCAN channels

CYT2B7 Configuration



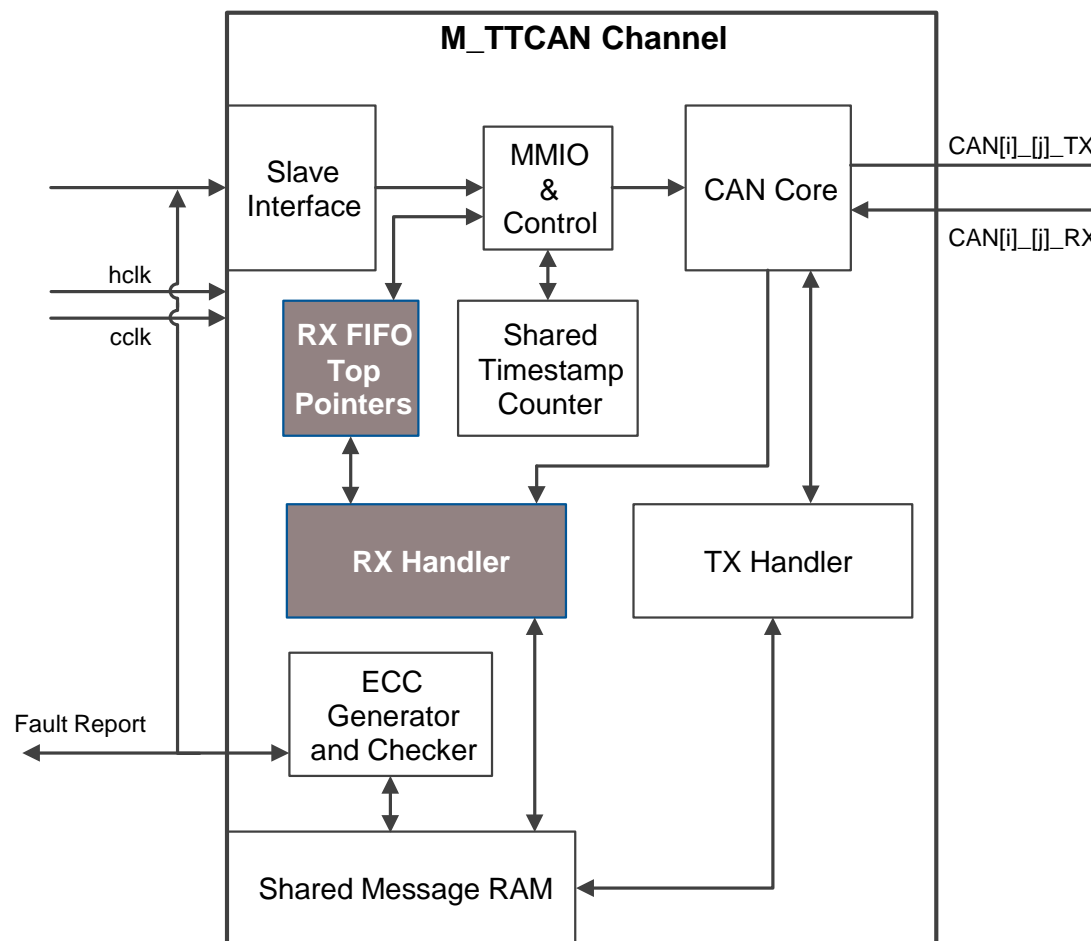
## Hint Bar

Review section 3.2 of the CAN FD TRM chapter and Register TRM (TS\_CNT) for additional details

# RX Handler

## CAN FD controller components

- > RX Handler
  - Acceptance Filtering
  - Dedicated RX Buffers
  - RX FIFOs
- > RX FIFO Top Pointers



### Hint Bar

Review section 3.4 of the CAN FD TRM chapter for additional details.



# Acceptance Filtering

- › Two sets of acceptance filters
  - For standard identifiers
  - For extended identifiers
- › Features
  - Each filter element<sup>1</sup> can be configured as
    - Range filter (from - to)
    - Filter for one or two dedicated IDs
    - Classic bit mask filter
  - Each filter element is configurable for acceptance or rejection filtering
  - Each filter element can be enabled/disabled individually
  - Filters are checked sequentially from element #0 until the first match

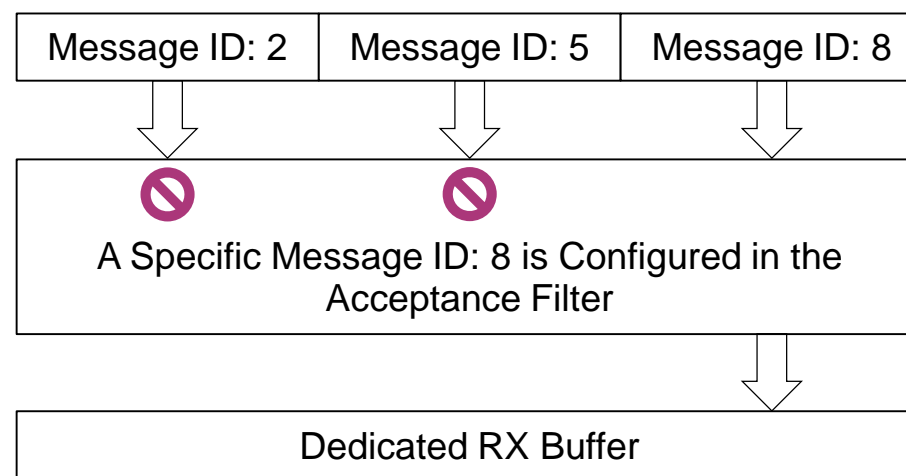
## Hint Bar

Review section 3.4.1 of the CAN FD TRM chapter and Register TRM for additional details

<sup>1</sup> A filter element is a condition of the filtering list. There can be up to 192 filter elements

# Dedicated RX Buffers

- > Up to 64 dedicated RX Buffers
  - After a received message is accepted by a filter element, the message is stored in the RX Buffer in the Message RAM referenced by the filter element
- > Use Case
  - Receive only the specific message ID (8) with the dedicated RX Buffer and acceptance filter
- > Advantage
  - Accepts frames only with specific message IDs

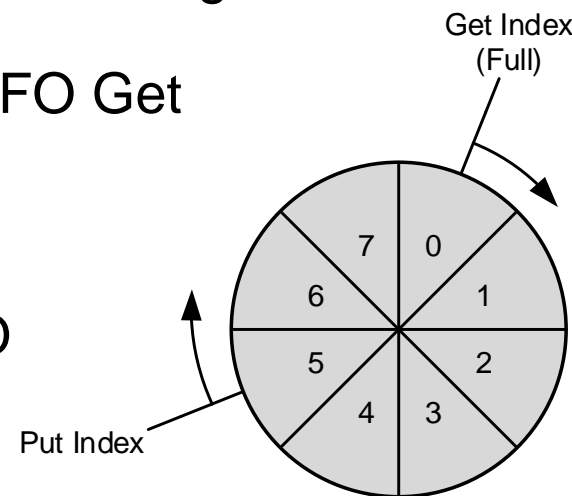


Hint Bar

Review section 3.4.3 of the CAN FD TRM chapter and Register TRM for additional details

# RX FIFOs

- > RX FIFOs can be configured to hold up to 64 elements each
- > Received messages that pass acceptance filtering are transferred to the RX FIFO as configured by the matching filter element
- > When the RX FIFO Put Index reaches the RX FIFO Get Index, the RX FIFO Full condition interrupt flag is set
- > Watermark interrupt
  - To avoid RX FIFO overflow, use the RX FIFO Watermark interrupt
- > Use Case
  - The RX FIFO Watermark interrupt flag can be used to trigger DMA

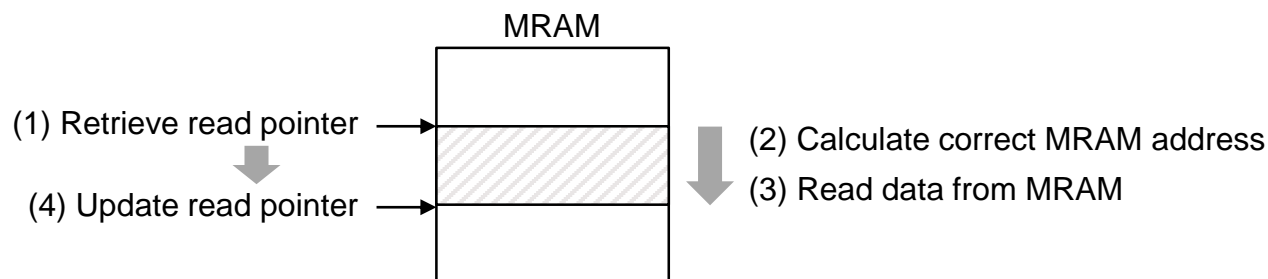


## Hint Bar

Review section 3.4.2 of the CAN FD TRM chapter and Register TRM for additional details

# RX FIFO Top Pointer

- › Tracks the number of message data words read, and updates the pointer information after reading the last word



- › Provides a single location<sup>1</sup> to read the data
- › Advantages
  - Reduces the software process to retrieve the read pointer, calculate correct MRAM address, and update the read pointer
  - Reduces bus load and latency
  - Enables DMA on FIFOs

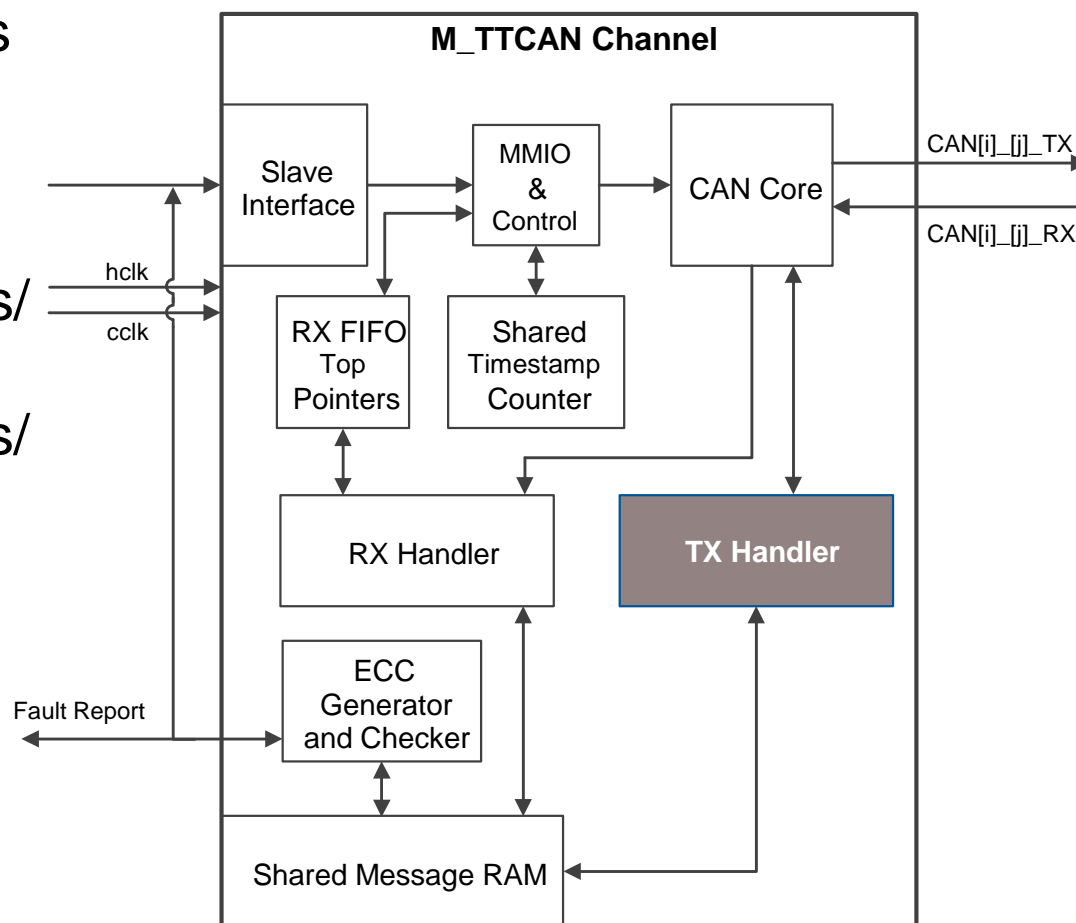
**Hint Bar**

**Review section 3.4.2 of the CAN FD TRM chapter and Register TRM for additional details**

<sup>1</sup> RXFTOP0\_DATA for RX FIFO0, RXFTOP1\_DATA for RX FIFO1

# TX Handler

- > CAN FD controller components
  - TX Handler
  - Dedicated TX Buffers
  - TX FIFO and TX Queue
  - Mixed Dedicated TX Buffers/  
TX FIFO
  - Mixed Dedicated TX Buffers/  
TX Queue
  - TX Event FIFO

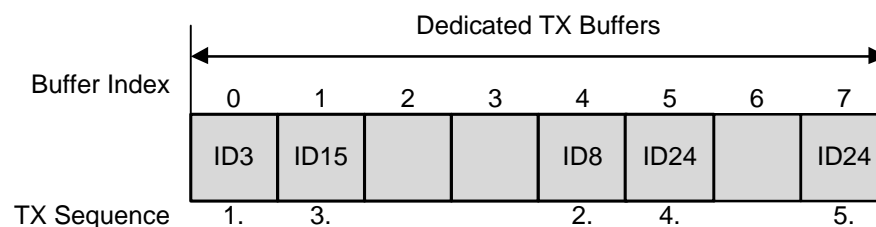


Hint Bar

**Review section 3.5 of the CAN FD TRM chapter for additional details**

# Dedicated TX Buffers

- › Each 32-bit dedicated TX Buffer is configured with a specific Message ID
- › If multiple TX Buffers are configured with the same Message ID, the TX Buffer with the lowest buffer number is transmitted first



- › Dedicated TX Buffers allocate “Element Size” 32-bit words in the MRAM

TX Buffer/FIFO/Queue Element Size

Data Field [bytes]	Element Size [RAM words]
8	4
12	5
16	6
20	7
24	8
32	10
48	14
64	18

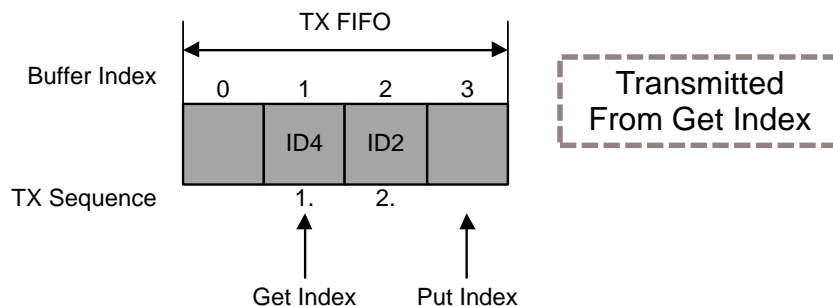
**Hint Bar**

Review section 3.5.2 of the CAN FD TRM chapter and Register TRM (TXESC.TBDS) for additional details

# TX FIFO and TX Queue

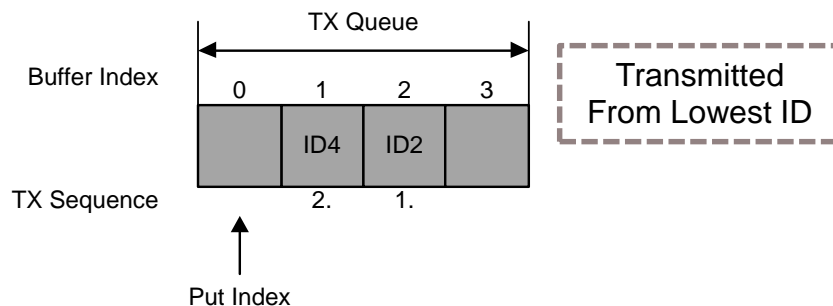
## > TX FIFO

- Messages stored in the TX FIFO are transmitted starting with the message referenced by the Get Index<sup>1</sup>
- After each transmission, the Get Index is incremented cyclically until the TX FIFO is empty



## > TX Queue

- Messages stored in the TX Queue are transmitted starting with the message with the lowest Message ID (highest priority)
- If multiple TX Queues are configured with the same Message ID, the TX Queue with the lowest buffer number is transmitted first



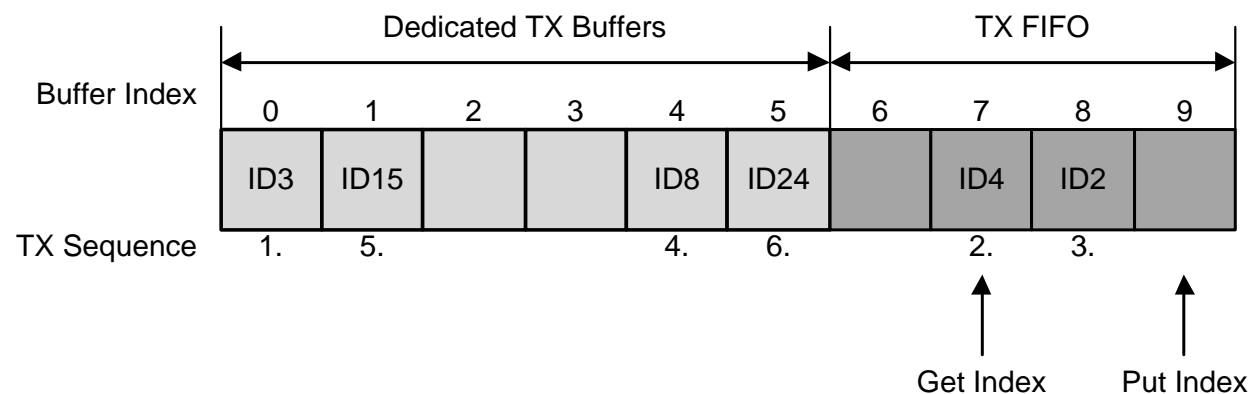
**Hint Bar**

Review sections 3.5.3 and 3.5.4 of the CAN FD TRM chapter and Register TRM for additional details

<sup>1</sup> TXFQS.TFGI

# Mixed Dedicated TX Buffers/TX FIFO

- > The MRAM TX Buffer section is subdivided into a set of dedicated TX Buffers and TX FIFO



- > TX Prioritization
  - Scan dedicated TX Buffers and the oldest pending TX FIFO Buffer (referenced by Get Index)
  - The TX Buffer with the lowest Message ID has the highest priority and is transmitted next

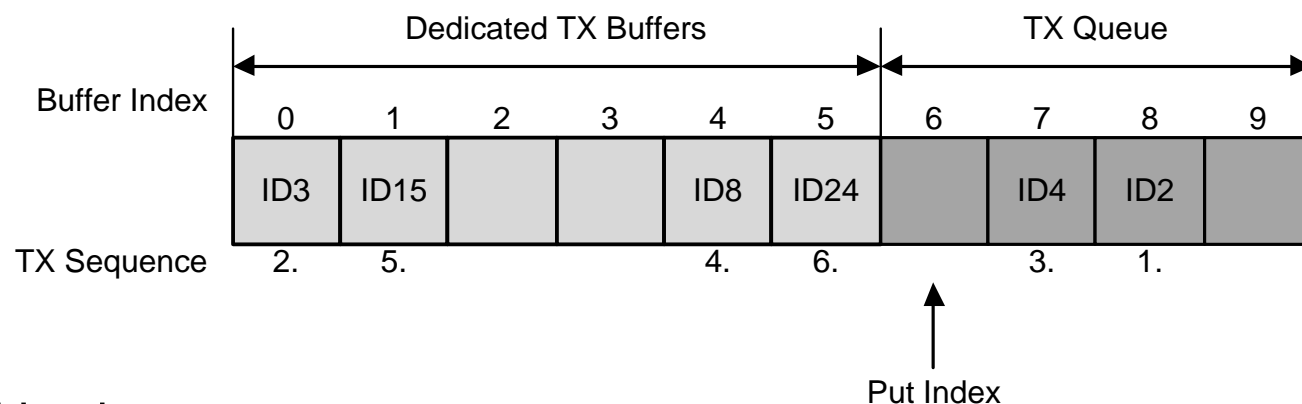
**Hint Bar**

Review section 3.5.5 of the CAN FD TRM chapter and Register TRM for additional details



# Mixed Dedicated TX Buffers/TX Queue

- > The MRAM TX Buffer section is subdivided into a set of dedicated TX Buffers and a TX Queue



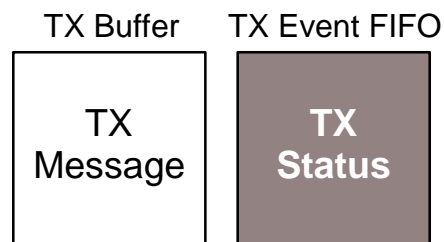
- > TX Prioritization
  - Scan all TX Buffers with an activated transmission request
  - The TX Buffer with the lowest Message ID has the highest priority and is transmitted next

**Hint Bar**

**Review section 3.5.6 of the CAN FD TRM chapter and Register TRM for additional details**

# TX Event FIFO

- > Message ID and timestamp are stored in the TX Event FIFO element
- > Can be configured to a maximum of 32 elements
- > Use Case
  - A TX Buffer holds only the message to be transmitted, while the transmit status is stored separately in the TX Event FIFO



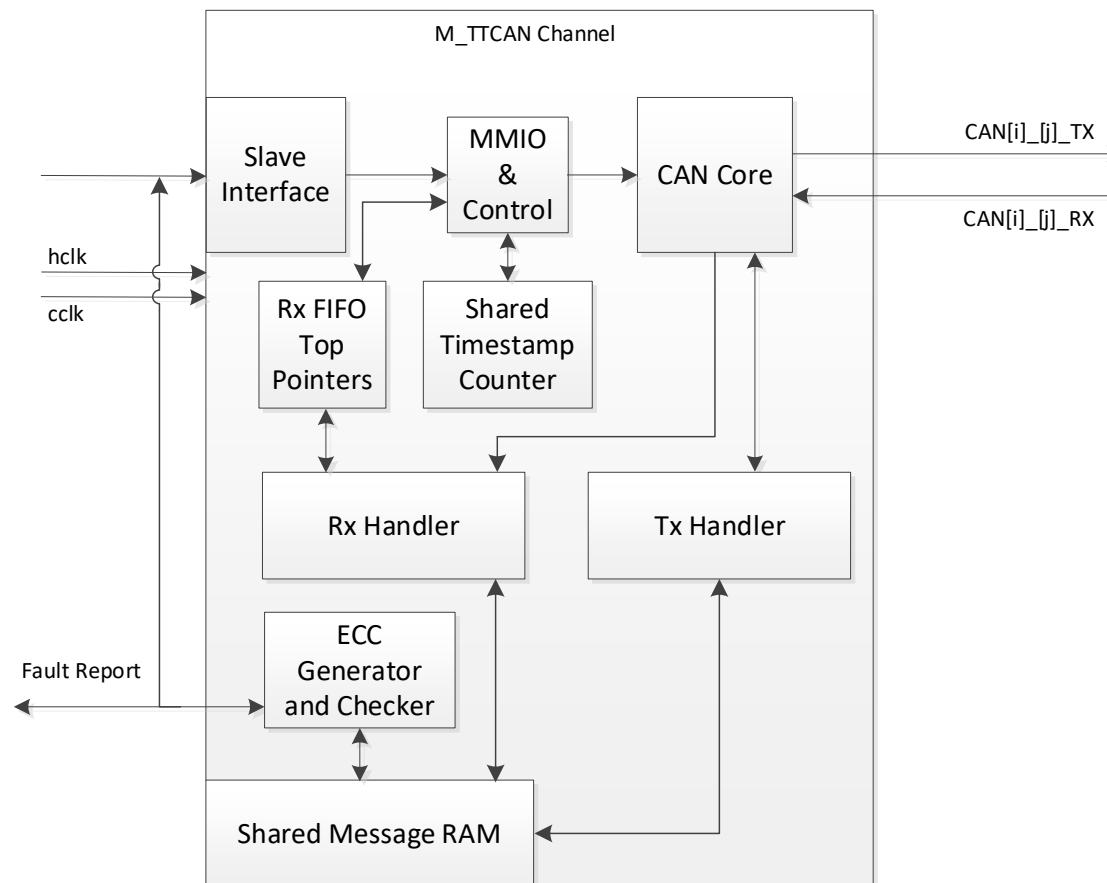
- > Advantages
  - When operating a dynamically managed transmit queue, a TX Buffer can be used for a new message immediately after successful transmission
  - It is not necessary to save transmit status information from a TX Buffer before overwriting that TX Buffer

## Hint Bar

Review section 3.5.8 of the CAN FD TRM chapter and Register TRM for additional details

# Message RAM

- > CAN FD controller components
  - Shared Message RAM
    - Message RAM Configuration
- > The following slides provide more information on Shared Message RAM

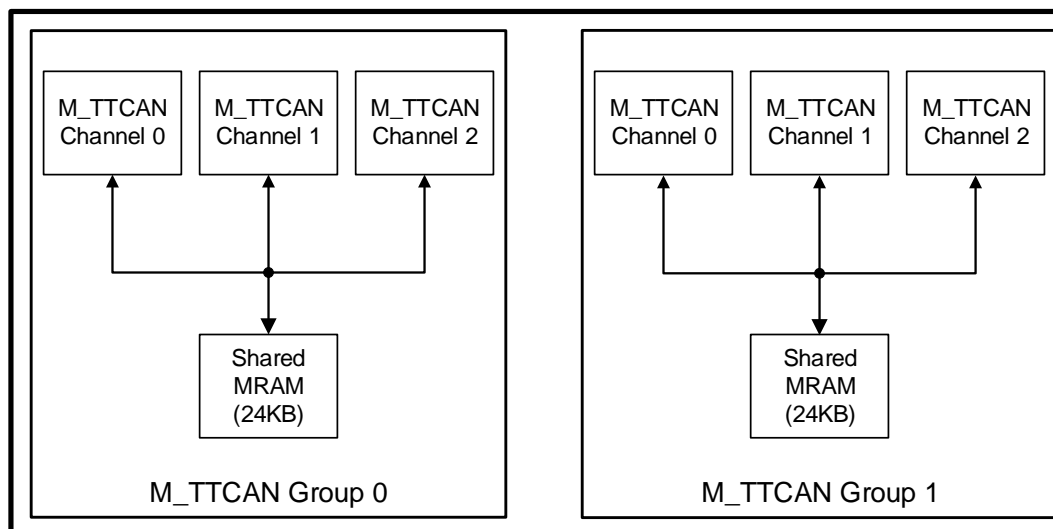


## Hint Bar

Review section 4 of the CAN FD TRM chapter for additional details

# Shared Message RAM

- > Message RAM in the Traveo II family devices is shared among multiple M\_TTCAN channels in the M\_TTCAN group
  - Following is the CYT2B7 Message RAM<sup>1</sup> diagram



- > Advantage
  - Each M\_TTCAN channel in the module can configure its required message RAM according to the needs of the application

**Hint Bar**

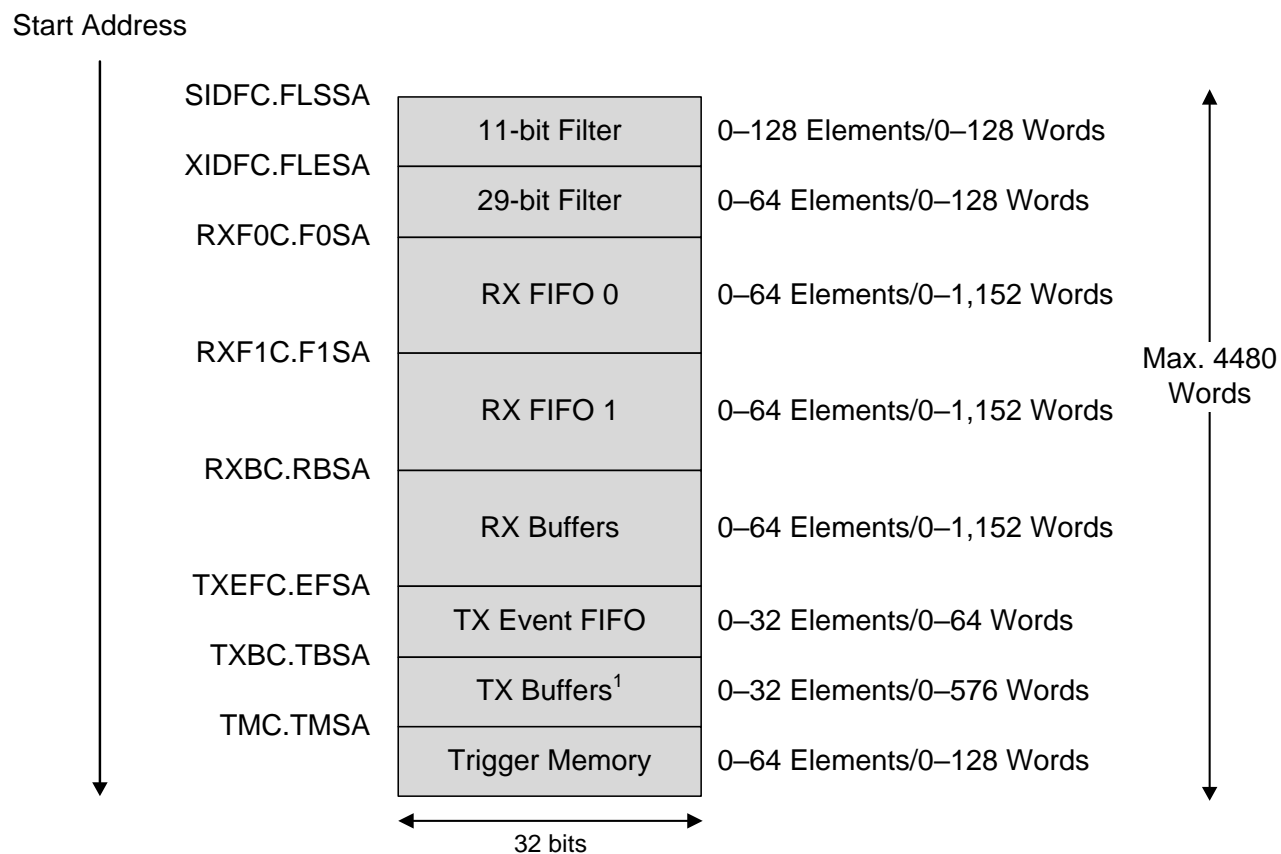
Review section 4 of the CAN FD TRM chapter and Register TRM for additional details

**Note: Message RAM cannot be used for system RAM**

<sup>1</sup> CYT2B9: 32KB among four channels, CYT4BF: 40KB among five channels

# Message RAM Configuration

- > Filter and messages are managed separately
- > Sent and received messages are managed separately



**Hint Bar**

**Review section 4 of the CAN FD TRM chapter and Register TRM for additional details**

<sup>1</sup> The TX Buffer section can be configured to hold dedicated TX Buffers as well as a TX FIFO/TX Queue

## Turning Message RAM OFF

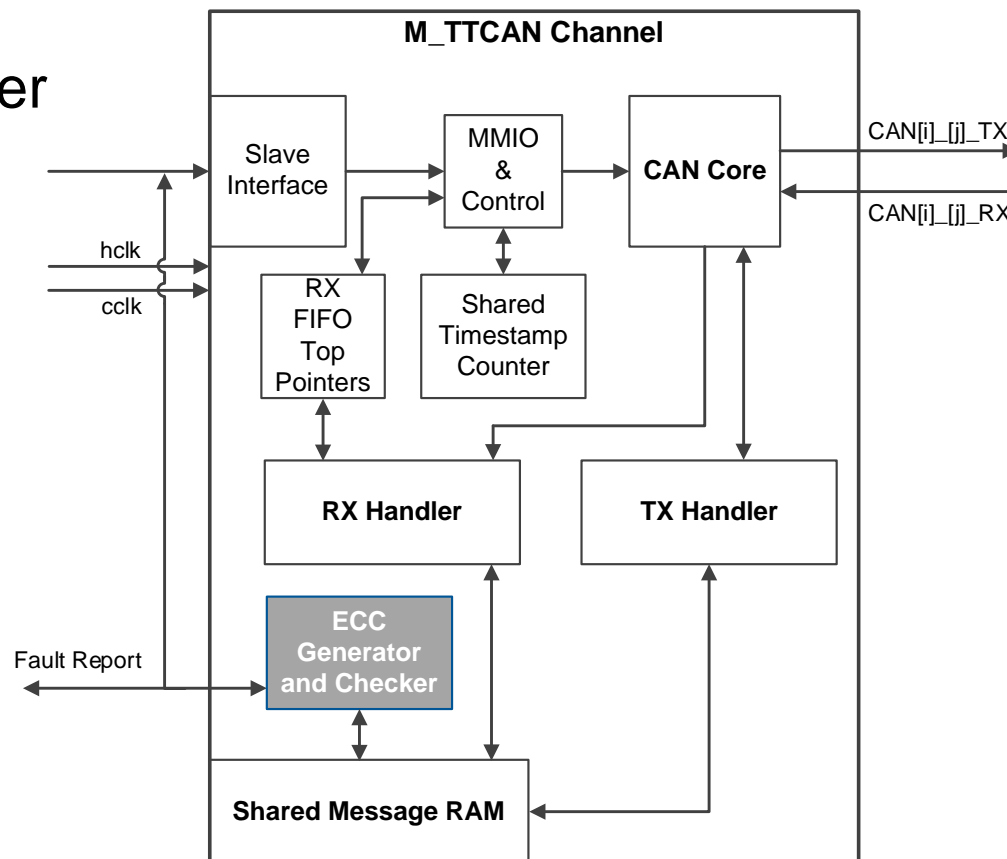
- › Message RAM can be turned off to save power by setting the CTL.MRAM\_OFF bit
- › Default value of this bit is '0' and MRAM is retained in this configuration during DeepSleep power mode
- › All M\_TTCAN channels must be powered down before setting the MRAM\_OFF bit

### Hint Bar

Review section 4.9 of the CAN FD TRM chapter and Register TRM for additional details

# ECC Generator and Checker

- > CAN FD components
  - ECC Generator and Checker
    - Single-Error Correction
    - Double-Error Detection
    - ECC-Error Injection
    - Address Error



Hint Bar

**Review section 4.8 of the CAN FD TRM chapter for additional details**

# ECC Generator and Checker (1/2)

- › Single-bit Error Correction and Double-bit Error Detection (SECDED)
  - SEC report action:
    - Report to the fault subsystem
- › DED report action:
  - Report to master
    - In the case of an AHB master, a bus error occurs
    - In the case of an M\_TTCAN channel, the M\_TTCAN channel shuts down immediately
  - Interrupt
  - Report to the fault subsystem
- › Software ECC error injection support
- › Use Case
  - SEC report: Not needed because single-bit error is corrected automatically
  - DED report: Use for failsafe operation such as stop system control
  - ECC error injection: Use for initial diagnosis of ECC before application running

## Hint Bar

Review section 4.8 of the CAN FD TRM chapter and Register TRM for additional details



## ECC Generator and Checker (2/2)

- › Address Error
- › Detects when TTCAN or MCU is trying to access out-of-range MRAM<sup>1</sup>
- › Unlike ECC errors, this can happen for both writes and reads
- › Report action:
  - Read from M\_TTCAN master:
    - To prevent sending corrupt data, shut down the M\_TTCAN channel immediately
    - Interrupt
  - Read from the AHB interface:
    - Bus error
  - Any case (read, write, and any master):
    - Report to the fault subsystem
- › Advantage
  - Makes software debugging easier

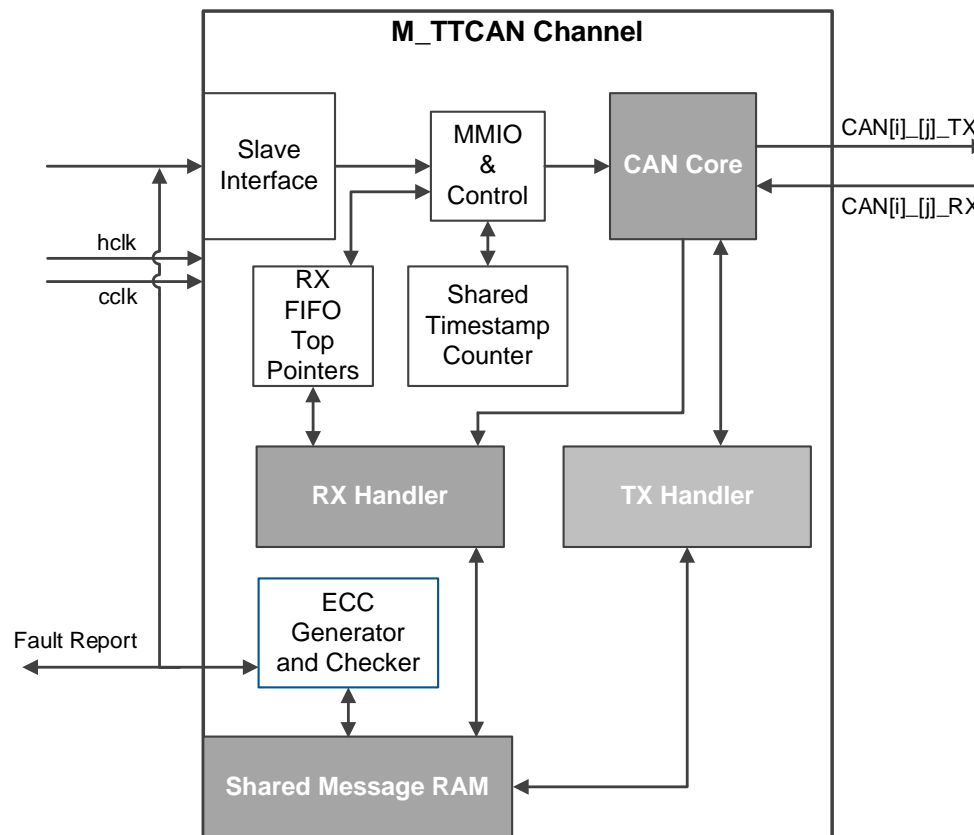
### Hint Bar

Review section 4.8.3 of the CAN FD TRM chapter and Register TRM for additional details

<sup>1</sup> CYT2B7: 24KB, CYT2B9: 32KB, CYT4BF: 40KB

# TTCAN

- > TTCAN Operation
  - Reference Message
  - Message Scheduling
  - Trigger Memory
  - Schedule Initialization
  - TTCAN Gap Control
  - Stop Watch
  - TTCAN Error Level
  - TTCAN Message Handling



Hint Bar

**Review section 4.8.3 of the CAN FD TRM chapter and Register TRM for additional details**

# Reference Message

- › A data frame characterized by a specific CAN identifier
- › Received and accepted by all nodes except the Time Master (sender of the reference message)
- › Level 1
  - Data length must be at least one
- › Level 0, 2
  - Data length must be at least four
- › Extended by other data up to the sum of eight CAN data bytes
- › All bits of the identifier except the three LSBs characterize the message as a reference message
- › The last three bits specify the priorities of up to eight potential time masters

## Hint Bar

Review section 5.1 of the CAN FD TRM chapter for additional details

# Message Scheduling

- › TTOCF.TM controls whether M\_TTCAN operates as a potential time master or as a time slave
- › If it is a potential time master, the three LSBs of the reference message's identifier, TTRMC.RID, define the master priority:
  - 0: Highest priority
  - 7: Lowest priority

## Hint Bar

Review section 5.2.2 of the CAN FD TRM chapter and Register TRM for additional details

# Trigger Memory

- › Part of the Message RAM
- › Stores up to 64 trigger elements
- › A trigger memory element consists of:
  - Time Mark (TM)
  - Cycle Code (CC)
  - Trigger Type (TYPE)
  - Filter Type (FTYPE)
  - Message Number (MNR)
  - Message Status Count (MSC)
  - Time Mark Event Internal (TMIN)
  - Time Mark Event External (TMEX)
  - Asynchronous Serial Communication (ASC)

## Hint Bar

**Review section 5.2.3 and 4.7 of the CAN FD TRM chapter for additional details**

# TTCAN Schedule Initialization

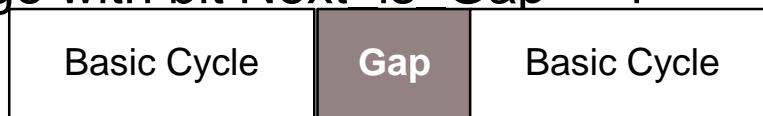
- › Synchronization to M\_TTCAN's message schedule starts when CCCR.INIT is reset
- › M\_TTCAN can operate strictly time-triggered (TTOCF.GEN = 0) or external event-synchronized time-triggered (TTOCF.GEN = 1)
- › All nodes start with cycle time zero at the beginning of their trigger list with TTOST.SYS = 00 (out of synchronization); no transmission is enabled with the exception of the reference message

## Hint Bar

Review section 5.2.4 of the CAN FD TRM chapter and Register TRM for additional details

# TTCAN Gap Control

- › All functions related to gap control apply only when M\_TTCAN is operated in external event-synchronized time-triggered mode (TTOCF.GEN = '1')
  - TTCAN message schedule can be interrupted by inserting gaps between basic cycles of the system matrix
  - During a gap, all transmissions are stopped and the CAN bus remains idle
  - A gap is finished when the next reference message starts a new basic cycle
  - A gap starts at the end of a basic cycle that itself was started by a reference message with bit Next is Gap = '1'



- › Use Case
  - Gaps are initialized by the current time master

## Hint Bar

Review section 5.3 of the CAN FD TRM chapter and Register TRM for additional details

# Stop Watch

- › The stop watch function enables capturing of M\_TTCAN internal time values (local time, cycle time, or global time) triggered by an external event
- › To enable the stop watch function, the application program must first define local time, cycle time, or global time as the stop watch source via TTOCN.SWS

## Hint Bar

Review section 5.4 of the CAN FD TRM chapter and Register TRM for additional details



# TTCAN Error Level

- › ISO 11898-4 specifies four levels of error severity
  - S0: No Error
  - S1: Warning
    - Only notification of application; reaction is application-specific
  - S2: Error
    - Notification of application. All transmissions in exclusive or arbitrating time windows are disabled (no data or remote frames may be started)
    - Potential time masters still transmit reference messages with the reference trigger offset TTOST.RTO set to the maximum value of 127
- › S3: Severe Error
  - Notification of application. All CAN bus operations are stopped (transmission of dominant bits is not allowed) and CCCR.MON is set. The S3 error condition remains active until the application updates the configuration (set CCCR.CCE)

## Hint Bar

Review section 5.7 of the CAN FD TRM chapter and Register TRM for additional details

# TTCAN Message Handling

- › Reference Message
  - For potential time masters, the identifier of the reference message is configured via TTRMC.RID
  - No dedicated TX Buffer is required for transmission of the reference message
  - When a reference message is transmitted, the first data byte (TTCAN Level 1) corresponding to the first four data bytes (TTCAN Level 0 and Level 2) will be provided by the Frame Synchronization Entry (FSE)<sup>1</sup>
- › Message Reception
  - Message reception is done via the two RX FIFOs, similar to event-driven CAN communication
- › Message Transmission
  - For time-triggered message transmission, M\_TTCAN supplies 32 dedicated TX Buffers
  - TX FIFO or TX Queue is not available when M\_TTCAN is configured for time-triggered operation (TTOCF.OM = “01” or “10”)

## Hint Bar

Review section 5.8 of the CAN FD TRM chapter and Register TRM for additional details

<sup>1</sup> Frame Synchronization Event (FSE) occurs at the sample point of each Start-of-Frame (SoF) bit



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# Revision History

Revision	ECN	Submission Date	Description of Change
**	6144419	04/25/2018	Initial release
*A	6362522	10/24/2018	Added pages 2, 4, 5, 29, and 33 to 41, and note descriptions in all pages. Updated page 3.
*B	6585632	05/31/2019	Updated pages 2, 3, 4, 14, 21, 26, 27, 32, 41. Added page 5.
*C	7033664	11/30/2020	Updated page 2 and 8, and added page 10. Merged page 3 for Traveo II Body Controller Entry.