Customer Training Workshop
Traveo™ II Body High and Cluster 2D Clock System

Q4 2020
## Target Products

### Target product list for this training material

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Body Controller High

The clock system is part of the System Resources block.
Introduction to Traveo II Cluster

The clock system is part of the System Resources block.

Review TRM chapter 18 for additional details.
Clock System Overview

Features

- Internal clock sources
  - IMO: Internal main oscillator (8 MHz)
  - ILO0/1: Internal low-speed oscillator (32.768 kHz)
- External clock sources
  - ECO: External crystal oscillator
  - WCO: Watch crystal oscillator
  - EXT_CLK: External clock generated using a signal through the I/O pin
    Also possible to output the internal clock
  - LPECO\(^1\): Low-power external crystal oscillator
- Clock generation
  - Phase-locked loops (PLL) - with and without SSCG\(^2\) and fractional operation\(^3\)
  - Frequency-locked loop (FLL)
- Clock supervision (CSV) to detect clock abnormality
- Clock calibration counter

\(^1\) CYT4BF does not have LPECO
\(^2\) Spread Spectrum Clock Generation
\(^3\) Fractional operation provides an output frequency that is a fractional multiple of the input frequency
Clock System Block Diagram

Clock system components

Legend:
- D: The number of direct select paths
- P: The number of PLLs
- R: The number of clock roots (CLK_HF)

See the device datasheet for the number of D, P, and R
Clock System Block Diagram

- Clock system components
  - Internal clock sources
    - IMO
    - ILO 0/1
Internal Clock Sources (1/2)

IMO: Internal main oscillator
- Produces an 8-MHz fixed-frequency clock
- An accurate, high-speed internal (crystal-less) oscillator
- Available only in Active and Sleep modes
- Default clock source after POR or any other reset
- Used by PLLs to generate a wide range of high-frequency clocks
- Enabled and disabled by register\(^1\)
  - Default is ENABLE\(^2\)

\(^1\) IMO should not be disabled if it is the source of the clock path to CLK_HF[0]
\(^2\) Refer to the Register TRM (CLK.IMO_CONFIG) for additional details
Internal Clock Sources (2/2)

› ILO 0/1: Internal low-speed oscillator
  – ILO0
    – Produces a 32.768-kHz nominal fixed-frequency clock
    – Low power and low accuracy
    – Available in all power modes
    – Always the source of the watchdog timer (WDT)\(^1\)
  – ILO1
    – Used for ILO0 clock monitoring
    – Parameters for ILO1 are the same as ILO0

\(^1\) Always leave the ILO enabled because it is the source of the watchdog timer
Clock System Block Diagram

- Clock system components
  - External clock sources
    - ECO
    - WCO
    - EXT_CLK
    - LPECO
External Clock Sources (1/3)

› ECO: External crystal oscillator
  - Contains an oscillator to drive an external up to 33.34-MHz crystal
  - Used by PLLs to generate a wide range of high-frequency clocks
  - ECO prescaler
  - ECO trimming
  - Enabled and disabled by register\(^1\)
    - Default is DISABLE

› WCO: External low-frequency watch crystal oscillator
  - Highly accurate 32.768-kHz clock source
  - Primary clock source for the real-time clock (RTC)
  - Enabled and disabled by register\(^2\)
    - Default is DISABLE

\(^1\) Refer to the Register TRM (CLK_ECO_CONFIG) for additional details
\(^2\) Refer to the Register TRM (CTL) for additional details
External Clock Sources (2/3)

ECO Trimming
- ECO supports a wide variety of crystals and ceramic resonators
- ECO can be configured by register
  - The following trim bit fields can be configured to control the maximum peak oscillation voltage across the crystal ($V_P$), the transconductance ($g_m$), and the nominal frequency ($f$):
    - ATRIM (Amplitude Trim by AGC)
    - GTRIM (Gain Trim)
    - WDTRIM (Watchdog Trim)
    - FTRIM (Filter Trim)
    - RTRIM (Feedback Resistor Trim)

\[ V_P = \frac{D_L}{\sqrt{2 \times ESR}} \times \frac{1}{\pi f (C_0 + C_L)} \]

\[ g_m > 20 \times ESR \times (2\pi \times f)^2 \times (C_0 + C_L)^2 \]

\[ |R_{neg}| = \frac{g_m \times 4 \times C_L^2}{(2\pi \times f)^2 \times (4 \times C_L^2 + 4 \times C_L \times C_0)^2} \]

\(^1\) Refer to the Register TRM (CLK_ECO_CONFIG2) for additional details
External Clock Sources (3/3)

› EXT_CLK: External clock
  - 0.25- to 100-MHz\(^1\) clock that can be sourced from a designated I/O pin
  - Can be used as the source clock for either the PLL or FLL
  - Can be used as the output for the internal clock (CLK_HF3 is available)
  - When using a pin as input or output to EXT_CLK, I/O must be set appropriately

› LPECO: Low-power external crystal oscillator
  - 3.99- to 8.01-MHz clock source
  - Support only cluster product
  - Can operate in Active, LPACTIVE, Sleep, LPSLEEP, DeepSleep, and Hibernate
  - Can generate CPU and peripheral clock source in conjunction with PLLs
  - Can use a real-time-clock (RTC) source instead of WCO
  - LPECO prescaler
  - Enabled and disabled by register\(^2\)
    - Default is DISABLE

\(^1\) Refer to datasheet for the target product
\(^2\) Refer to the Register TRM (BACKUP_LPECO_CTL) for additional details
Clock System Block Diagram

- Clock system components
  - High-speed clock generation
    - PLL
    - FLL
Clock Generation

PLL: Phase-locked loop
- Input clock can be IMO (8 MHz), ECO, or EXT_CLK
- Two types of PLL: PLL and PLL400
- PLL without SSCG and fractional operation¹
  - Input clock range: 3.988 to 33.34 MHz (CYT4BF)²
  - Output clock range: 11 to 200 MHz (CYT4BF)²
- PLL400 with SSCG and fractional operation¹
  - Input clock range: 3.988 to 33.34 MHz (CYT4BF)²
  - Output clock range: 25 to 350 MHz (CYT4BF)²
  - Supports down spread
  - 24-bit fractional divider³
  - SSCG and fractional operation are enabled and disabled by register⁴
    - Default is Disable

¹ Refer to the device datasheet for number and location each PLL type
² Refer to the device datasheet for the target product
³ Refer to the Register TRM (PLL400_CONFIG2 register) for additional details
⁴ Refer to the Register TRM (CLK_PLL400M_CONFIG2 and CLK_PLL400M_CONFIG3 registers) for additional details

Hint Bar
Review TRM section 18.3 and Register TRM for additional details
Refer to the datasheet for additional details on AC specification
Output clock range of PLL400 changes depending on spreading configuration

Refer to the datasheet for additional details on AC specification
Clock Generation

› FLL: Frequency-locked loop
  - Input clock can be IMO (8 MHz), ECO, or EXT_CLK
  - A counter with a current-controlled oscillator (CCO)
    - Starts up (locks) faster and uses lower power than the PLL
    - The lock tolerance is user adjustable
  - The parameters on the FLL configuration are as follows:
    - Input clock range: 0.25 to 80 MHz (CYT4BF)\(^1\)
    - Output clock range: 24 to 100 MHz (CYT4BF)\(^1\)
  - FLL is set by ROM boot, and FLL can reduce startup time

\(^1\) Refer to the device datasheet for the target product
## PLL connection table

<table>
<thead>
<tr>
<th>CLK_PATH</th>
<th>CYT4BF PLL Type</th>
<th>CYT4DN PLL Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_PATH1</td>
<td>PLL400#0</td>
<td>PLL400#0</td>
</tr>
<tr>
<td>CLK_PATH2</td>
<td>PLL400#1</td>
<td>PLL400#1</td>
</tr>
<tr>
<td>CLK_PATH3</td>
<td>PLL#2</td>
<td>PLL400#2</td>
</tr>
<tr>
<td>CLK_PATH4</td>
<td>PLL#3</td>
<td>PLL400#3</td>
</tr>
<tr>
<td>CLK_PATH5</td>
<td>Not supported</td>
<td>PLL400#4</td>
</tr>
<tr>
<td>CLK_PATH6</td>
<td>Not supported</td>
<td>PLL#5</td>
</tr>
<tr>
<td>CLK_PATH7</td>
<td>Not supported</td>
<td>PLL#6</td>
</tr>
<tr>
<td>CLK_PATH8</td>
<td>Not supported</td>
<td>PLL#7</td>
</tr>
</tbody>
</table>
# Clock Generation PLL (1/4)

PLL configuration parameters (CYT4BF)\(^1\)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>PLL w/o SSCG and Fractional Operation</th>
<th>PLL with SSCG and Fractional Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fref</td>
<td>3.988 to 33.34 MHz</td>
<td>3.988 to 33.34 MHz</td>
</tr>
<tr>
<td>Fout (Fvco/Output divider)</td>
<td>11 to 200 MHz</td>
<td>25 to 350 MHz</td>
</tr>
<tr>
<td>Fpfd (Fref/Reference divider)</td>
<td>4 to 8 MHz</td>
<td>8 to 20 MHz</td>
</tr>
<tr>
<td>Fvco (Fpfd * Feedback divider)</td>
<td>170 to 400 MHz</td>
<td>400 to 800 MHz</td>
</tr>
</tbody>
</table>

1. Refer to the device datasheet for the target product

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**Hint Bar**

Review TRM section 18.3.1, 18.3.2, and Register TRM for additional details

Fout range changes depending on spreading configuration

Fpfd range changes depending on fractional divider configuration

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\(^1\) Refer to the device datasheet for the target product
Configuration example for PLL without SSCG and Fractional Operation

In this case, 200-MHz clock (Fout) is generated from the 8-MHz input clock (Fref)

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Fref</th>
<th>Fout</th>
<th>Fpfd</th>
<th>Fvco</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8 MHz</td>
<td>200 MHz = Fvco/2</td>
<td>4 MHz = Fref/2</td>
<td>400 MHz = Fpfd x 100</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Divider Setting</th>
<th></th>
<th>Output Divider¹: 2</th>
<th>Reference Divider¹: 2</th>
<th>Feedback Divider¹: 100</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ Refer to the Register TRM (CLK_PLL_CONFIG register) for additional details of PLL without SSCG and fractional operation
² Refer to the Register TRM (PLL400_CONFIG register) for additional details of PLL with SSCG and fractional operation
Configuration for SSCG

- Spread energy contained in the narrow band of the clock source to a wide band

The parameters on the PLL configuration\(^1\) are as follows:

- Modulation Depth: Between -3\%, -2\%, -1\%, or -0.5\%
- Modulation Rate: Between \(F_{pfd}/4096\), \(F_{pfd}/2048\), \(F_{pfd}/1024\), or \(F_{pfd}/512\)
- Modulation Type: Down-spread mode only

Advantage

- Reduces the peak spectral amplitude of the fundamental and the harmonics to lower radiated emission from the clock source

It can be represented as \(F_{out} = F_c - \Delta F\)

\(^1\) Refer to the Register TRM (PLL400_CONFIG3 register) for additional details
**Clock Generation PLL (4/4)**

› **Configuration for fractional operation**
  - PLL400 has a 24-bit fractional divider
    - Set according to the following formula
    - Accuracy is only guaranteed for the upper 21 bits
  
› **Configuration example for fractional operation**
  - In this case, 196.608-MHz clock (Fout) is generated from the 8-MHz input clock (Fref)

\[
F_{\text{out}} = \frac{F_{\text{ref}} \times P + \text{Frac}_\text{div}}{Q \times \text{OUTPUT}_\text{DIV}}
\]

\[
= \frac{8\text{--MHz}}{1} \times \frac{73 + 0.727999985}{3}
\]

\[
= 196.608 \text{ --MHz}
\]

<table>
<thead>
<tr>
<th>Fref</th>
<th>Q</th>
<th>P</th>
<th>Frac_div</th>
<th>OUTPUT_DIV</th>
<th>Fout</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 MHz</td>
<td>1</td>
<td>73</td>
<td>0.727999985 = 12213813 / 2^24</td>
<td>3</td>
<td>196.608 MHz</td>
</tr>
<tr>
<td>Setting</td>
<td>Reference Divider(^1): 1</td>
<td>Feedback Divider(^1): 73</td>
<td>FRAC_DIV(^2): 12213813</td>
<td>Output Divider(^1): 3</td>
<td>-</td>
</tr>
</tbody>
</table>

› **Advantage**
  - Can generate source clock of the sampling frequency (e.g., 96 kHz) in the sound system

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\(^1\) Refer to the Register TRM (PLL400_CONFIG register) for additional details
\(^2\) Refer to the Register TRM (PLL400_CONFIG2 register) for additional details
Clock System Block Diagram

- Clock system components
  - Clock trees
    - CLK_PATHx
    - CLK_HFx
    - CLK_REF_HF
    - CLK_LF
    - CLK_BAK
    - CLK_TIMER

DeepSleep/Hibernate/HV Domain

Active Domain

Predivider (1/2/4/8)

ECO Prescaler

IMO

EXT_CLK

R

ECO

LPECO

Prescaler

CLK_TIMER

PLL#0

PLL#1

PLL#(P-1)

PLL#(R-1)

FLL

MCWDT

WDT

IMO

ECO

ILO0

ILO1

WCO

LPECO

Prescaler

CLKTIMER

CLK_PATH0

CLK_PATH1

CLK_PATH2

CLK_PATH(P+1)

CLK_PATH(P+D)

CLK_REF_HF

CLK_TIMER

CLK_HF0

CLK_HF1

CLK_HF(R-1)

CLK_HF

CLK_LF

CLK_BAK
Active Domain Clock Trees

- **Clock distribution**
  - **CLK_PATHx**
    - Input sources for the CLK_HFx roots
    - CLK_PATH0 contains the FLL output
      - Up to 100 MHz (using FLL)
    - CLK_PATH1 to (P+1) contains the PLL output
      - Up to 200 MHz when using PLLs without SSCG and fractional operation
      - Up to 350 MHz when using PLLs with SSCG and fractional operation
    - CLK_PATH (P+D) is a connection to root clocks
      - Up to 33.34 MHz (using ECO)
  - **CLK_REF_HF**
    - Selects IMO, ECO, EXT_CLK
    - Typically selects the IMO (8 MHz)
    - Used as reference clock for CSV_CLK_HF0 to R-1 (CLK_HF 0 to R-1 clock supervision)

- **TIMER_CLK**
  - CLK_IMO is input source for CLK_TIMER
  - Used as source clock of SysTick timer in CPU

---

1 Refer to the device datasheet for the target product
CLK_HF Clock Trees

CLK_HFx can select CLK_PATHx as source clock by register¹

<table>
<thead>
<tr>
<th>CLK Path</th>
<th>Usage Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYT4BF</td>
<td>CYT4DN</td>
</tr>
<tr>
<td>CLK_HF0</td>
<td>Root clock for CPUSS, PERI (CLK_MEM, CLK_SLOW, CLK_PERI)</td>
</tr>
<tr>
<td>CLK_HF1</td>
<td>CM7 CPU Core#0, CM7 CPU Core#1</td>
</tr>
<tr>
<td>CLK_HF2</td>
<td>Peripheral clock root other than CLK_PERI</td>
</tr>
<tr>
<td>CLK_HF3</td>
<td>Event generator, clock output on EXT_CLK pins (when used as output)</td>
</tr>
<tr>
<td>CLK_HF4</td>
<td>Ethernet Channel#0 and Channel#1 internal clock</td>
</tr>
<tr>
<td>CLK_HF5</td>
<td>I2S channel#0, I2S channel#1, I2S channel# Channel#0 TSU, Ethernet Channel#1 TSU</td>
</tr>
<tr>
<td>CLK_HF6</td>
<td>Root clock for SDHC, SMIF interface clock</td>
</tr>
<tr>
<td>CLK_HF7</td>
<td>Not connect</td>
</tr>
<tr>
<td>CLK_HF8</td>
<td>Not supported</td>
</tr>
<tr>
<td>CLK_HF9</td>
<td>Not supported</td>
</tr>
<tr>
<td>CLK_HF10</td>
<td>Not supported</td>
</tr>
<tr>
<td>CLK_HF11</td>
<td>Not supported</td>
</tr>
<tr>
<td>CLK_HF12</td>
<td>Not supported</td>
</tr>
<tr>
<td>CLK_HF13</td>
<td>Not supported</td>
</tr>
</tbody>
</table>

¹ Refer to the Register TRM (CLK_ROOT_SELECT) for additional details
CLK_HF0\(^1\) distribution

- Distributed to CLK_MEM, CLK_SLOW, CLK_PERI, and CLK_TRC_DBG
- CLK_MEM
  - Source clock for CPUSS fast infrastructure
  - Up to 200 MHz\(^2\)
- CLK_SLOW
  - Source clock for CPUSS slow infrastructure such as CM0+, Crypto, DMAs, test controller, and some peripherals\(^3\)
  - Up to 100 MHz
- CLK_PERI
  - Source clock for some peripherals via divider
  - Up to 100 MHz
- PCLK and CLK_GR
  - Source clock for peripheral functions via divider
- CLK_TRC_DBG
  - Source clock for trace components in debug infrastructure
  - Runs only when debugger is connected

\(^1\) CLK_HF0 can be enabled and disabled by register. CLK_HF0 is always enabled as the clock source of CPU
\(^2\) Refer to the device datasheet for the target product
\(^3\) eFuse and SRSS registers
CLK_HF Distribution (2/2)

› CLK_HF1 distribution
  - Root clock for the CM7 CPUs
  - Distributed to CLK_FAST_0 and CLK_FAST_1
  - Divider setting is possible independently for each M7 CPU

› CLK_HF2 distribution
  - Input clock for peripheral clock dividers
  - Root clock such as CAN FD, LIN, SCB, SAR ADC
Peripheral Clock Distribution

- PERI Clock Divider
  - Output of dividers can be routed to any peripheral
  - Two dividers
    - Peripheral clock divider#0
      - Input clock: CLK_PERI
      - Used for IOSS, TCPWM, and CPUSS
    - Peripheral clock divider#1
      - Input clock: CLK_HF2
      - Used for CAN FD, LIN, SCB, and SAR ADC
  - Four types of dividers¹
    - 8-bit divider²
    - 16-bit divider²
    - 16.5-bit divider²
    - 24.5-bit divider²

- Supports fractional clock dividers
- Phase aligning
  - Can be phase-aligned with any of the other (enabled) clock dividers

¹ Not all dividers are supported
² The supported number of each divider differs between Peripheral clock divider#0 and Peripheral clock divider#1

Hint Bar
Review TRM section 18.6 for additional details on clock numbers, which are assigned for each peripheral

Clock dividers can be configured through the following registers:
- DIV_8_CTL
- DIV_16_CTL
- DIV_16_5_CTL
- DIV_24_5_CTL

Clock Enable multiplexers can be configured through CLOCK_CTL registers, which are assigned for each peripheral
DeepSleep/Hibernate/HV Domain Clock Trees

› Clock distribution
  - **CLK_LF**
    - Selects ILO0, ILO1, WCO, LPECO
    - Input source for MCWDT
    - Used as reference clock for CSV_ILO (CLK_ILO0 clock supervision)
  - **CLK_BAK**
    - Selects CLK_LF, ILO0, ILO1, WCO, LPECO
    - Input source for RTC\(^1\) clock

\(^1\) Typically, WCO is connected to RTC. CLK_LF can also connect to RTC
Clock System Block Diagram

- Clock system components
  - Clock supervision (CSV) allows one clock to be monitored with another clock (reference clock)
  - Monitored clock sources
    - CLK_HFx
    - CLK_REF_HF
    - CLK_ILO0
    - CLK_LF
  - CSV power domain
    - Active domain CSV
    - DeepSleep domain CSV
Clock Supervision (1/2)

- Checks if the frequency of the monitored clock is within the allowed frequency window
  - Uses a reference clock to supervise the behavior of the monitor clock

<table>
<thead>
<tr>
<th>CSV Components</th>
<th>Monitor Clock</th>
<th>Reference Clock</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSV_HFx</td>
<td>CLK_HFx</td>
<td>CLK_REF_HF</td>
<td>CLK_REF_HF is selected the IMO or EXT_CLK or ECO CLK_REF_HF is typically selected the IMO (default)</td>
</tr>
<tr>
<td>CSV_REF</td>
<td>CLK_REF_HF</td>
<td>CLK_ILO0</td>
<td>–</td>
</tr>
<tr>
<td>CSV_ILO</td>
<td>CLK_ILO0</td>
<td>CLK_LF</td>
<td>CLK_LF is selected WCO or ILO1 or ECO Pre-scaler</td>
</tr>
<tr>
<td>CSV_LF</td>
<td>CLK_LF</td>
<td>CLK_ILO0</td>
<td>–</td>
</tr>
</tbody>
</table>

- Active domain CSV: CSV_HF0/1 and CSV_REF
  - Automatically stops during DeepSleep and restarts by wakeup
  - “Wait” function to monitor startup time
  - Possible to generate a reset or a fault report
- DeepSleep domain CSV: CSV_ILO, CSV_LF
  - Operates during Active and DeepSleep
  - Generates wakeup and fault reports
- All CSVs are initially off

1 Need to prevent a false error detection at startup
CSV operation
- The monitored clock generates a Monitor event (Period) and the reference clock generates a lower and upper limit
- The Monitor event is compared against a lower limit/upper limit
- An error is reported if the Monitor event ≤ lower limit or the Monitor event > upper limit

Advantages
- Detects clock stop, too fast, and too slow by frequency window
- Monitors clock in Active, Sleep, and DeepSleep power modes with Active domain CSV and DeepSleep domain CSV
- Can achieve ASIL-B
Clock Calibration Counter

Clock Calibration Counter Operation

- Two counters: Counter1 and Counter2
  - Counter1 is clocked by clock1 (reference clock)
  - Counter2 is clocked by clock2 (measurement clock)
- Counter1 sets the measurement period by the count number of clock1 (1)
- Counter2 indicates the count number of clock2 during the measurement period (2)
- Clock2 frequency can be calculated using the following formula with two counter values
  \[
  \text{clock2frequency} = \frac{\text{Counter2value}}{\text{Counter1value}} \times \text{clock1frequency}
  \]
- All clock sources are available for these two clocks (clock1 and clock2)

Use Case

- Measure a low-accuracy clock such as the ILO using a high-accuracy clock such as the ECO

Hint Bar

Review TRM section 18.7 for additional details

Count Clock1 and 2 can be selected through the CLK_OUTPUT_FAST register
Comparison Between CYT2BL, CYT4BF, and CYT4DN (1/4)

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2BL</th>
<th>CYT4BF</th>
<th>CYT4DN</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMO</td>
<td>Supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ECO</td>
<td>Supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILO 0</td>
<td>Supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILO 1</td>
<td>Supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WCO</td>
<td>Supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPECO</td>
<td>Not implemented</td>
<td>Supported</td>
<td></td>
</tr>
<tr>
<td><strong>FLL</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of FLL</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Range</td>
<td>0.25 to 80 MHz</td>
<td>0.25 to 100 MHz</td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>24 to 100 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PLL</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of PLL</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Input Range</td>
<td>3.988 to 33.34 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>11 to 160 MHz</td>
<td>11 to 200 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>PLL400</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of PLL</td>
<td>Not implemented</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Input Range</td>
<td>Not implemented</td>
<td>3.988 to 33.34 MHz</td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>Not implemented</td>
<td>25 to 350 MHz (*)</td>
<td>25 to 400 MHz</td>
</tr>
<tr>
<td>SSCG</td>
<td>Not implemented</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>Fractional Operation</td>
<td>Not implemented</td>
<td></td>
<td>Yes</td>
</tr>
</tbody>
</table>

(*) Spreading off
## Comparison Between CYT2BL, CYT4BF, and CYT4DN (2/4)

<table>
<thead>
<tr>
<th>CLK Trees Source Clock</th>
<th>CYT2BL</th>
<th>CYT4BF</th>
<th>CYT4DN</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_PATH 0</td>
<td>CLK_PATH 0</td>
<td>FLL</td>
<td>PLL400</td>
</tr>
<tr>
<td>CLK_PATH 1</td>
<td>PLL</td>
<td>PLL400</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 2</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1</td>
<td>PLL400</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 3</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1</td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 4</td>
<td>Not implemented</td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 5</td>
<td>Not implemented</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1</td>
<td>PLL400</td>
</tr>
<tr>
<td>CLK_PATH 6</td>
<td>Not implemented</td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 7</td>
<td>Not implemented</td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 8</td>
<td>Not implemented</td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 9</td>
<td>Not implemented</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1, LPECO</td>
<td></td>
</tr>
<tr>
<td>CLK_REF_HF</td>
<td>ECO,IMO,EXT_CLK</td>
<td>ECO,IMO,EXT_CLK, LPECO</td>
<td></td>
</tr>
<tr>
<td>CLK_TIMER</td>
<td>CLK_HF0, IMO</td>
<td>IMO</td>
<td></td>
</tr>
<tr>
<td>CLK_LF</td>
<td>ILO0/1, WCO, ECO</td>
<td>ILO0/1, WCO, ECO, LPECO</td>
<td></td>
</tr>
<tr>
<td>CLK_BAK</td>
<td>CLK_LF, ILO0, WCO</td>
<td>CLK_LF, ILO0, WCO, LPECO</td>
<td></td>
</tr>
</tbody>
</table>
Comparison Between CYT2BL, CYT4BF, and CYT4DN (3/4)

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2BL</th>
<th>CYT4BF</th>
<th>CYT4DN</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_HF0</td>
<td>CPUSS clocks, PERI, and AHB infrastructure</td>
<td>CPUSS (Memories, CLK_SLOW, Peripherals)</td>
<td>CPUSS (Memories, CLK_SLOW, Peripherals)</td>
</tr>
<tr>
<td>CLK_HF1</td>
<td>Event Generator</td>
<td>CPUSS (Cortex-M7 CPU 0, 1)</td>
<td>CPUSS (Cortex-M7 CPU 0, 1)</td>
</tr>
<tr>
<td>CLK_HF2</td>
<td>Not connect</td>
<td>CAN FD, FlexRay, LIN, TCPWM, SCB, SAR ADC</td>
<td>CAN FD, CXPI, LIN, SCB, SAR ADC</td>
</tr>
<tr>
<td>CLK_HF3</td>
<td>Not implemented</td>
<td>Event Generator</td>
<td>Event Generator</td>
</tr>
<tr>
<td>CLK_HF4</td>
<td>Not implemented</td>
<td>Ethernet</td>
<td>Ethernet</td>
</tr>
<tr>
<td>CLK_HF5</td>
<td>Not implemented</td>
<td>Audio subsystem</td>
<td>Sound Subsystem #0</td>
</tr>
<tr>
<td>CLK_HF6</td>
<td>Not implemented</td>
<td>SDHC Interface, SMIF</td>
<td>Sound Subsystem #1</td>
</tr>
<tr>
<td>CLK_HF7</td>
<td>Not implemented</td>
<td>Not connect</td>
<td>Sound Subsystem #2</td>
</tr>
<tr>
<td>CLK_HF8</td>
<td>Not implemented</td>
<td>Not implemented</td>
<td>SMIF #0</td>
</tr>
<tr>
<td>CLK_HF9</td>
<td>Not implemented</td>
<td>Not implemented</td>
<td>SMIF #1</td>
</tr>
<tr>
<td>CLK_HF10</td>
<td>Not implemented</td>
<td>Not implemented</td>
<td>Video Subsystem</td>
</tr>
<tr>
<td>CLK_HF11</td>
<td>Not implemented</td>
<td>Not implemented</td>
<td>Video Display #0</td>
</tr>
<tr>
<td>CLK_HF12</td>
<td>Not implemented</td>
<td>Not implemented</td>
<td>Video Display #1</td>
</tr>
<tr>
<td>CLK_HF13</td>
<td>Not implemented</td>
<td>Not implemented</td>
<td>Not connect</td>
</tr>
</tbody>
</table>
## Comparison Between CYT2BL, CYT4BF, and CYT4DN (4/4)

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2BL</th>
<th>CYT4BF</th>
<th>CYT4DN</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock Divider</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of Dividers</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Fractional Clock Divider</td>
<td></td>
<td>24.5-bit dividers</td>
<td>16.5-bit dividers, 24.5-bit dividers</td>
</tr>
<tr>
<td>Phase Aligning</td>
<td></td>
<td>Supported</td>
<td></td>
</tr>
<tr>
<td><strong>Clock Supervision</strong></td>
<td></td>
<td>Supported</td>
<td></td>
</tr>
<tr>
<td><strong>Calibration Counter</strong></td>
<td></td>
<td>Supported</td>
<td></td>
</tr>
</tbody>
</table>
Part of your life. Part of tomorrow.
<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6400993</td>
<td>12/7/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6633414</td>
<td>7/22/2019</td>
<td>Added slide 4,12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated Figure slide 6, 7, 10, 13, 19, 20, 22, 23, 25, 26</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated slide 2, 5, 13, 15 - 17, 21, 22, 24, 25, 28, 32 – 34</td>
</tr>
<tr>
<td>*B</td>
<td>7060646</td>
<td>01/06/2021</td>
<td>Updated slide 2-5, 9, 11, 13, 15-17, 21-23, 25, 30, 32-35</td>
</tr>
</tbody>
</table>