Customer training workshop

TRAVEO™ T2G Body Entry Clock System

Q4 2021
Target products

Target product list for this training material:

<table>
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<tr>
<th>Family category</th>
<th>Series</th>
<th>Code flash memory size</th>
</tr>
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<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112 KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160 KB</td>
</tr>
</tbody>
</table>
Introduction to CYT2BL

The clock system is part of the System Resources block.
The clock system supplies clocks for MCU operation

Features

- Internal clock sources
  - 8-MHz IMO
  - 32.768-kHz ILO0/1

- External clock sources
  - External crystal oscillator (ECO)
  - Watch crystal oscillator (WCO)
  - External clock (EXT_CLK) generated using a signal through I/O pin
    It is also possible to output the internal clock

- Clock generation
  - Phase lock loop (PLL)
  - Frequency lock loop (FLL)

- Clock supervision (CSV) for detecting clock abnormality
- Clock calibration counter

Review Chapter 18 in the TRM for additional details
Clock system block diagram

Active domain

- IMO
- ECO

Predivider
(1/2/4/8)

CLK_ECO

Prescaler

clk_ref_hf

DeepSleep/Hibernate/HV domain

- ILO0
- ILO1

clk_wco

CLK_BAK

CLK_LF

WDT
MCWDT

CSV

CSV

CSV

CSV

Predivider
(1/2/4/8)

Predivider
(1/2/4/8)

PRECLK0

PRECLK1

PRECLK2
Internal clock sources

- Internal main oscillator (IMO)
- Internal low-speed oscillator 0/1 (ILO0/1)
IMO: Internal main oscillator

› Produces an 8-MHz fixed frequency
› An accurate, high-speed internal (crystal-less) oscillator
› Available in only Active and Sleep modes
› Default clock source after POR or any other reset
› Used by PLL0 to generate a wide range of high-frequency clocks
› Enabled and disabled by register¹
  – Default is ENABLE²

¹ IMO should not be disabled if it is the source of the clock path to CLK_HF[0]
² Refer to the Register TRM (CLK.IMO.CONFIG) for additional details

Hint Bar
Review Section 18.2 in the TRM for additional details
Refer to the datasheet for additional details on AC specifications
ILO 0/1: Internal low-speed oscillators

› ILO0
  - Produces a 32.768-kHz nominal fixed frequency
  - Low power and low accuracy
  - Available in all power modes
  - Always the source of the Watchdog timer\(^1\)

› ILO1
  - Used for ILO0 clock monitoring
  - Parameters for ILO1 are the same as ILO0

\(^1\) Always leave the ILO enabled, as it is the source of the Watchdog timer
External clock sources

- ECO
- WCO
- EXT_CLK
External clock sources overview

› ECO
  - Contains an oscillator to drive an external 3.988 MHz to 33.34 MHz crystal
  - Used by PLL0 to generate a wide range of high-frequency clocks
  - ECO pre-scaler
  - ECO trimming
  - Enabled and disabled by register\(^1\)
    - Default is DISABLE

› WCO
  - Highly accurate 32.768-kHz clock source
  - Primary clock source for the real-time clock (RTC)
  - Enabled and disabled by register\(^2\)
    - Default is DISABLE

› EXT_CLK
  - 0.25 MHz to 80 MHz clock that can be sourced from a designated I/O pin
  - Can be used as the source clock for either the PLL or FLL
  - Can be used to output the internal clock (CLK_HF1 is available)
  - When using a pin as an input to EXT_CLK, I/O must be set appropriately\(^3\)

\(^1\) Refer to the Register TRM (CLK_ECO_CONFIG) for additional details
\(^2\) Refer to the Register TRM (CTL) for additional details
\(^3\) Refer to the TRM section 18.2.3 and the datasheet for additional details
ECO trimming

- ECO supports a wide variety of crystals and ceramic resonators
- ECO can be configured by register\(^1\)
  - The following trim bit fields can be configured to control the maximum peak oscillation voltage across the crystal (VP), the transconductance (gm), and the nominal frequency (f):
    - ATRIM (Amplitude Trim by AGC)
    - GTRIM (Gain Trim)
    - WDTRIM (Watchdog Trim)
    - FTRIM (Filter Trim)
    - RTRIM (Feedback Resistor Trim)

\[
\text{Max peak value: } V_P = \frac{\sqrt{D_L}}{2\times ESR} \frac{1}{\pi f (C_0 + C_L)}
\]

f: Fundamental frequency of the crystal (XTAL)

D\(_L\): Maximum drive level of XTAL

ESR: Equivalent series resistance

C\(_0\): Shunt capacitance of XTAL

C\(_L\): Parallel load capacitance of XTAL

Transconductance: \(g_m > 20 \times ESR \times (2\pi \times f)^2 \times (C_0 + C_L)^2\)

Negative resistance: \(|R_{neg}| = \frac{g_m \times 4 \times C_L^2}{(2\pi f)^2 \times (4 \times C_L^2 + 4 \times C_L \times C_0)^2}\)

\(^1\) Refer to the Register TRM (CLK_ECO_CONFIG2) for additional details.
High-speed clock generation

- Phase lock loop (PLL)
- Frequency lock loop (FLL)
Clock generation: PLL and FLL

› PLL
  - Input clock can be IMO (8 MHz), ECO, or EXTCLK
  - PLL configuration parameters:
    - Input clock range: 3.988 to 33.34 MHz
    - Output clock range: 11 to 160 MHz (CYT2BL)\(^1\)

› FLL
  - Input clock can be IMO (8 MHz), ECO, or EXTCLK
  - A counter with a current-controlled oscillator (CCO)
    - Starts up (locks) faster and uses lower power than the PLL
    - The lock tolerance is user adjustable
  - Parameters on the FLL configuration:
    - Input clock range: 0.25 MHz to 80 MHz
    - Output clock range: 24 MHz to 100 MHz (CYT2BL)\(^1\)

\(^1\) Refer to the data sheet for target product.

Review Section 18.3 in the TRM and Register TRM for additional details
Refer to the datasheet for additional details on AC specification
PLL configuration example

- Parameters on PLL configuration:
  - Fref: 3.988 MHz to 33.34 MHz
  - Fout (Fvco/Output divider): 11 MHz to 160 MHz (CYT2BL)¹
  - Fpfd (Fref/Reference divider): 4 MHz to 8 MHz
  - Fvco (Fpfd * Feedback divider): 170 MHz to 400 MHz

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¹ Refer to the data sheet for target product.

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Review section 18.3.1 in the TRM and Register TRM for additional details.
Clock trees

- CLK_PATH0/1/2
- CLK_HF0/1
- clk_ref_hf
- CLK_LF
- CLK_BAK
- CLK_HF0 distribution
Clock distribution

› CLK_PATHx
- Input sources for the CLK_HF roots
  - CLK_PATH0 contains the FLL output
    Up to 100 MHz (using FLL)¹
  - CLK_PATH1 contains the PLL output
    Up to 160 MHz (using PLL)¹
  - CLK_PATH2 is a connection to root clocks
    Up to 33.34 MHz (using ECO)

› CLK_REF_HF
- Selects IMO, ECO, EXTCLK
  - Typically selects the IMO (8 MHz)
  - Used as a reference clock for CLK_HF0/1 clock supervision

› CLK_HF0/1
- Selects CLK_PATH0, 1, 2
  - CLK_HF0 is the input source for the CPUSS and resources such as Timer, SCB, and SAR ADC
  - CLK_HF1 is the input source for the event generator

¹ Refer to the data sheet for target product.
Clock distribution

› **CLK_LF**
  - ILO0, ILO1, or WCO (32.768 kHz) can be the input clock for CLK_LF
  - Input sources for the MCWDT clock
  - Uses reference clock for CLK_ILO0 Clock Supervision

› **CLK_BAK**
  - ILO0, ILO1, or WCO (32.768 kHz) can be the input clock for CLK_BAK
  - Input sources for RTC\(^1\) clock

\(^1\) Typically WCO is connected to RTC. CLK_LF also can connect to RTC.
CLK_HF0\(^1\) distribution

- The root clock for the CPUSS and the peripherals
- Distributed to CLK_FAST, CLK_SLOW, and CLK_PERI
- CPUSS has CLK_FAST and CLK_SLOW domains
- CLK_FAST
  - Source clock for CM4
  - Up to 160 MHz\(^2\)
- CLK_SLOW
  - Source clock for the CM0+, Crypto, DMAs, test controller, some peripherals\(^3\)
  - Up to 100 MHz\(^2\)
- CLK_PERI
  - Source clock for all peripherals such as TCPWM and SCB, via divider
  - Up to 100 MHz\(^2\)

\(^1\)CLK_HF0 can be enabled and disabled by register. CLK_HF0 is always enabled as the clock source of CPU.
\(^2\) Refer to the data sheet for target product.
\(^3\) CPUSS and PPU registers
Peri clock distribution

- **PERI clock divider**
  - Four types of dividers\(^1\)
    - 8-bit divider
    - 16-bit divider
    - 16.5-bit divider
    - 24.5-bit divider
  - Fractional clock dividers supported
  - Output of dividers can be routed to any peripheral
  - Phase aligning
    - Can be phase-aligned with any of the other (enabled) clock dividers.

\(^1\) Not all dividers are supported

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**Hint Bar**

Clock dividers can be configured through the following registers:

- DIV_8_CTL
- DIV_16_CTL
- DIV_16_5_CTL
- DIV_24_5_CTL

Clock Enable multiplexers can be configured through CLOCK_CTL registers, which are assigned for each peripheral.

Review Section 18.7 in the TRM for additional details on clock numbers, which are assigned for each peripheral.
Clock supervision (CSV)

- Clock supervision (CSV) allows one clock to be monitored with another clock (reference clock)
- Monitored clock sources:
  - CLK_HF0
  - CLK_HF1
  - CLK_REF_HF
  - ILO0
  - CLK_LF
- CSV power domains:
  - Active domain CSV
  - DeepSleep domain CSV
Clock supervision features

- Checks that the frequency of the monitored clock is within the allowed frequency window
  - Uses a reference clock to supervise the behavior of the monitor clock

<table>
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<tr>
<th>CSV Components</th>
<th>Monitor Clock</th>
<th>Reference Clock</th>
<th>Note</th>
</tr>
</thead>
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<tr>
<td>CSV_HF0/1</td>
<td>CLK_HF0/1</td>
<td>clk_ref_hf</td>
<td>clk_ref_hf is typically selected the IMO (default)</td>
</tr>
<tr>
<td>CSV_REF</td>
<td>clk_ref_hf</td>
<td>ILO0</td>
<td>–</td>
</tr>
<tr>
<td>CSV_ILO</td>
<td>ILO0</td>
<td>CLK_LF</td>
<td>CLK_LF is selected WCO or ILO1</td>
</tr>
<tr>
<td>CSV_LF</td>
<td>CLK_LF</td>
<td>ILO0</td>
<td>–</td>
</tr>
</tbody>
</table>

- Active domain CSV: CSV_HF0/1, CSV_REF
  - Automatically stops during DeepSleep, and restarts by wakeup
  - Wait function of monitoring start for startup time
  - Possible to generate a Reset or a Fault report
- DeepSleep domain CSV: CSV_ILO, CSV_LF
  - Operates during Active and DeepSleep
  - Generates Wakeup and Fault reports
- All CSVs are initially OFF

1 Need to prevent a false error detection at startup
CSV operation

› The monitored clock generates a monitor event (Period), and the reference clock generates a lower and upper limit
› The monitor event is compared against a lower limit/upper limit
› An error is reported if the monitor event ≤ lower limit, or if the monitor event > upper limit

Advantages
– Detects whether the clock stops, runs too fast or runs too slow, and if the period is not within the frequency window
– Monitors clock in each power mode such as Active, Sleep, and DeepSleep with Active domain CSV and DeepSleep domain CSV
– Can achieve ASIL-B
Clock calibration counter

Clock calibration counter operation
- Two counters: Counter1 and Counter2
  - Counter1 is clocked by clock1: reference clock
  - Counter2 is clocked by clock2: measurement clock.
- Counter1 sets the measurement period by the count number of clock1
- Counter2 indicates the count number of clock2 during the measurement period
- Clock2 frequency can be calculated from the following formula using two count numbers:

\[
\text{clock2frequency} = \frac{\text{Counter2value}}{\text{Counter1value}} \times \text{clock1frequency}
\]

- All clock sources are available as a source for these two clocks.

Use case
- Measure a lower-accuracy clock, such as the ILO, using a higher-accuracy clock such as the ECO

Hint Bar
Review Section 18.8 in the TRM for additional details
Count Clock1, 2 can be selected through registers:
CLK_OUTPUT_FAST
Appendix
## Comparison Between CYT2BL, CYT4BF, and CYT4DN (1/4)

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<th>CYT4DN</th>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ECO</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILO 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILO 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WCO</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPECO</td>
<td></td>
<td>Not implemented</td>
<td>Supported</td>
<td></td>
</tr>
<tr>
<td>FLL</td>
<td>Number of FLL</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>Input Range</td>
<td>0.25 to 80 MHz</td>
<td>0.25 to 100 MHz</td>
<td>3.988 to 33.34 MHz</td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>24 to 100 MHz</td>
<td></td>
<td>11 to 200 MHz</td>
<td></td>
</tr>
<tr>
<td>PLL</td>
<td>Number of PLL</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Input Range</td>
<td>3.988 to 33.34 MHz</td>
<td>11 to 160 MHz</td>
<td>11 to 200 MHz</td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>11 to 160 MHz</td>
<td>11 to 200 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLL400</td>
<td>Number of PLL</td>
<td>Not implemented</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Input Range</td>
<td>Not implemented</td>
<td>3.988 to 33.34 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>Not implemented</td>
<td>25 to 350 MHz (*)</td>
<td>25 to 400 MHz</td>
<td>(*) Spreading off</td>
</tr>
<tr>
<td>SSCG</td>
<td>Not implemented</td>
<td></td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Fractional Operation</td>
<td>Not implemented</td>
<td></td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>
## Comparison Between CYT2BL, CYT4BF, and CYT4DN (2/4)

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<th>Features</th>
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<th>CYT4DN</th>
<th>Note</th>
</tr>
</thead>
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<td>CLK Trees Source Clock</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 0</td>
<td></td>
<td>FLL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 1</td>
<td>PLL</td>
<td>PLL400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 2</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1</td>
<td>PLL400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 3</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1</td>
<td>PLL</td>
<td>PLL400</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 4</td>
<td>Not implemented</td>
<td>PLL</td>
<td>PLL400</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 5</td>
<td>Not implemented</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1</td>
<td>PLL400</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 6</td>
<td>Not implemented</td>
<td></td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 7</td>
<td>Not implemented</td>
<td></td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 8</td>
<td>Not implemented</td>
<td></td>
<td>PLL</td>
<td></td>
</tr>
<tr>
<td>CLK_PATH 9</td>
<td>Not implemented</td>
<td>ECO,IMO,EXT_CLK,WCO, ILO0/1, LPECO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_REF_HF</td>
<td>ECO,IMO,EXT_CLK</td>
<td>ECO,IMO,EXT_CLK, LPECO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_TIMER</td>
<td>CLK_HF0, IMO</td>
<td>IMO</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>ILO0/1, WCO, ECO</td>
<td>ILO0/1, WCO, ECO, LPECO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_BAK</td>
<td>CLK_LF, ILO0, WCO</td>
<td>CLK_LF, ILO0, WCO, LPECO</td>
<td></td>
<td></td>
</tr>
</tbody>
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Comparison between CYT2BL, CYT4BF, and CYT4DN (3/4)

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<th>CYT4DN</th>
<th>Note</th>
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<td>CLK_HF0 CPUSS clocks, PERI, and AHB infrastructure</td>
<td>CPUSS (Memories, CLK_SLOW, Peripherals)</td>
<td>CPUSS (Memories, CLK_SLOW, Peripherals)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF1 Event Generator</td>
<td>CPUSS (Cortex-M7 CPU 0, 1)</td>
<td>CPUSS (Cortex-M7 CPU 0, 1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF2 Not connect</td>
<td>CAN FD, FlexRay, LIN, TCPWM, SCB, SAR</td>
<td>CAN FD, CXPI, LIN, SCB, SAR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF3 Not implemented</td>
<td>Event Generator</td>
<td>Event Generator</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF4 Not implemented</td>
<td>Ethernet</td>
<td>Ethernet</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF5 Not implemented</td>
<td>Audio subsystem</td>
<td>Sound Subsystem #0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF6 Not implemented</td>
<td>SDHC Interface, SMIF</td>
<td>Sound Subsystem #1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF7 Not implemented</td>
<td>Not connect</td>
<td>Sound Subsystem #2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF8 Not implemented</td>
<td>Not implemented</td>
<td>SMIF #0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF9 Not implemented</td>
<td>Not implemented</td>
<td>SMIF #1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF10 Not implemented</td>
<td>Not implemented</td>
<td>Video Subsystem</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF11 Not implemented</td>
<td>Not implemented</td>
<td>Video Display #0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF12 Not implemented</td>
<td>Not implemented</td>
<td>Video Display #1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK_HF13 Not implemented</td>
<td>Not implemented</td>
<td>Not connect</td>
<td></td>
</tr>
</tbody>
</table>
## Comparison between CYT2BL, CYT4BF, and CYT4DN (4/4)

<table>
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<th>CYT4DN</th>
<th>Note</th>
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<td>Clock Divider</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of Dividers</td>
<td>1</td>
<td></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Fractional Clock Divider</td>
<td>24.5-bit dividers</td>
<td></td>
<td>16.5-bit dividers, 24.5-bit dividers</td>
<td></td>
</tr>
<tr>
<td>Phase Aligning</td>
<td></td>
<td></td>
<td>Supported</td>
<td></td>
</tr>
<tr>
<td>Clock Supervision</td>
<td></td>
<td></td>
<td>Supported</td>
<td></td>
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<tr>
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<td></td>
<td></td>
<td>Supported</td>
<td></td>
</tr>
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</table>
Part of your life. Part of tomorrow.
## Revision History

<table>
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<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6157641</td>
<td>04/29/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6364397</td>
<td>10/25/2018</td>
<td>Added slide 2 and the note descriptions of all pages.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated slides 3-6, 9, 11, 14, 19.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Added Clock Calibration Counter slide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated the figures</td>
</tr>
<tr>
<td>*B</td>
<td>7060645</td>
<td>01/06/2021</td>
<td>Updated slide 2 - 4, 8, 10, 13, 16, 17, 18, 25-28</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Deleted slide 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Added slide 11</td>
</tr>
<tr>
<td>*C</td>
<td>7450141</td>
<td>11/16/2021</td>
<td>Updated slide 1, 2, 14</td>
</tr>
</tbody>
</table>