

# Customer Training Workshop

## Traveo™ II Body Entry Clock System

Q1 2021



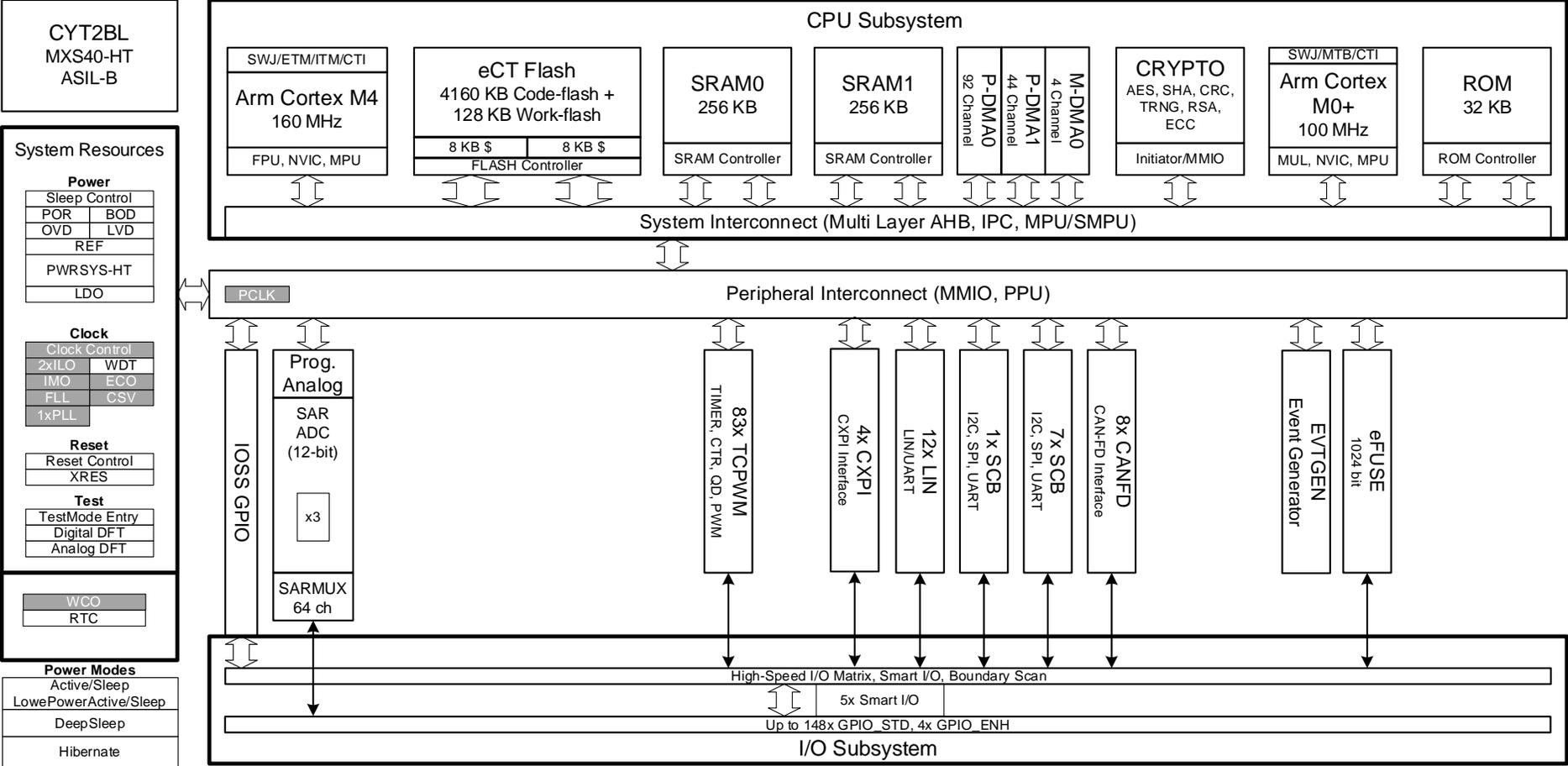
# Target Products

- › Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576 KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160 KB

# Introduction to CYT2BL

> The Clock system is part of the System Resources block



**Hint Bar**

**Review Chapter 18 in the TRM for additional details**

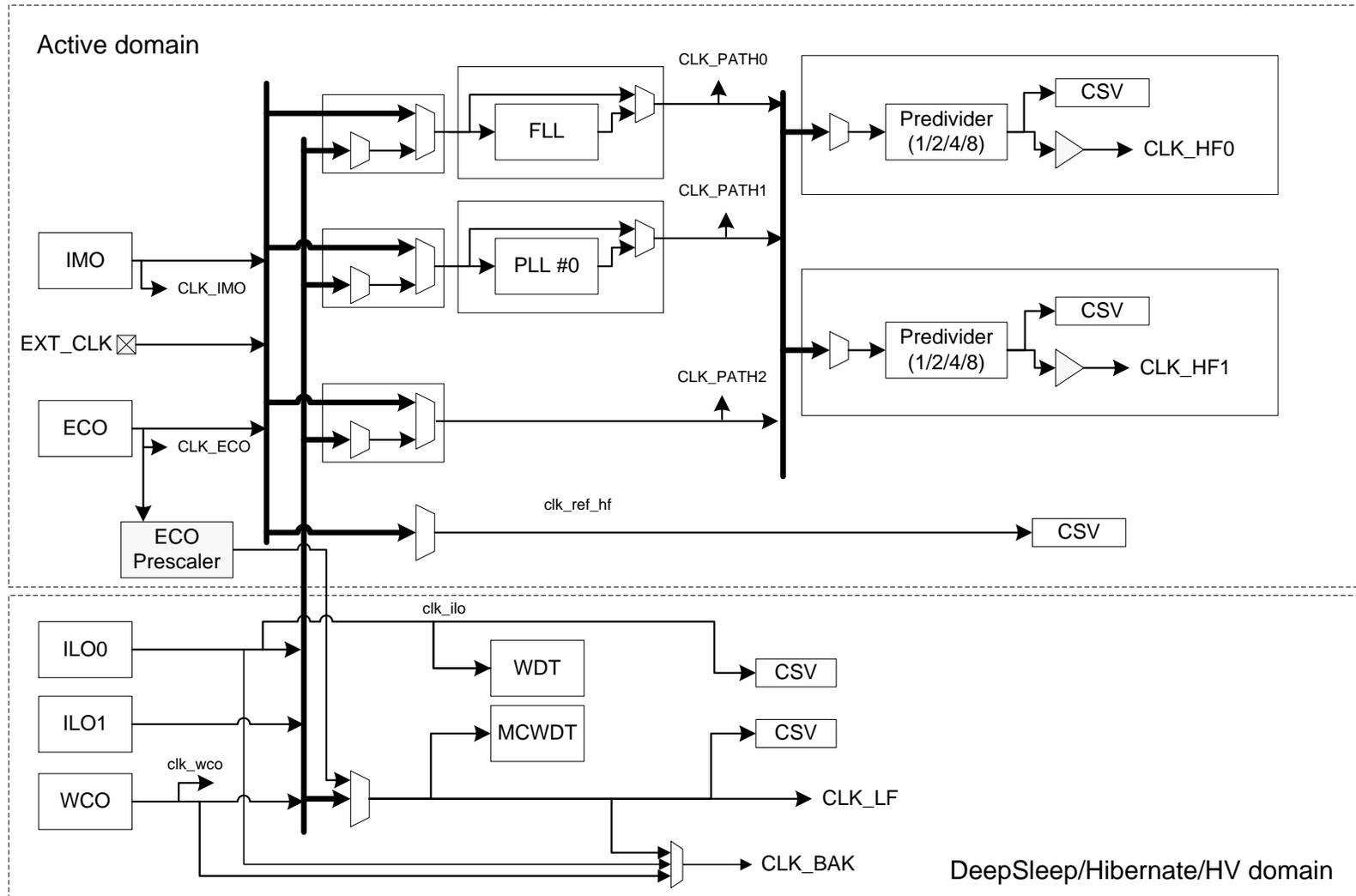
# Clock System Overview

- › The clock system supplies clocks for MCU operation
- › Features
  - Internal clock sources
    - 8-MHz IMO
    - 32.768-kHz ILO0/1
  - External clock sources
    - External crystal oscillator (ECO)
    - Watch crystal oscillator (WCO)
    - External clock (EXT\_CLK) generated using a signal through I/O pin  
It is also possible to output the internal clock
  - Clock generation
    - Phase lock loop (PLL)
    - Frequency lock loop (FLL)
- › Clock supervision (CSV) for detecting clock abnormality
- › Clock Calibration Counter

## Hint Bar

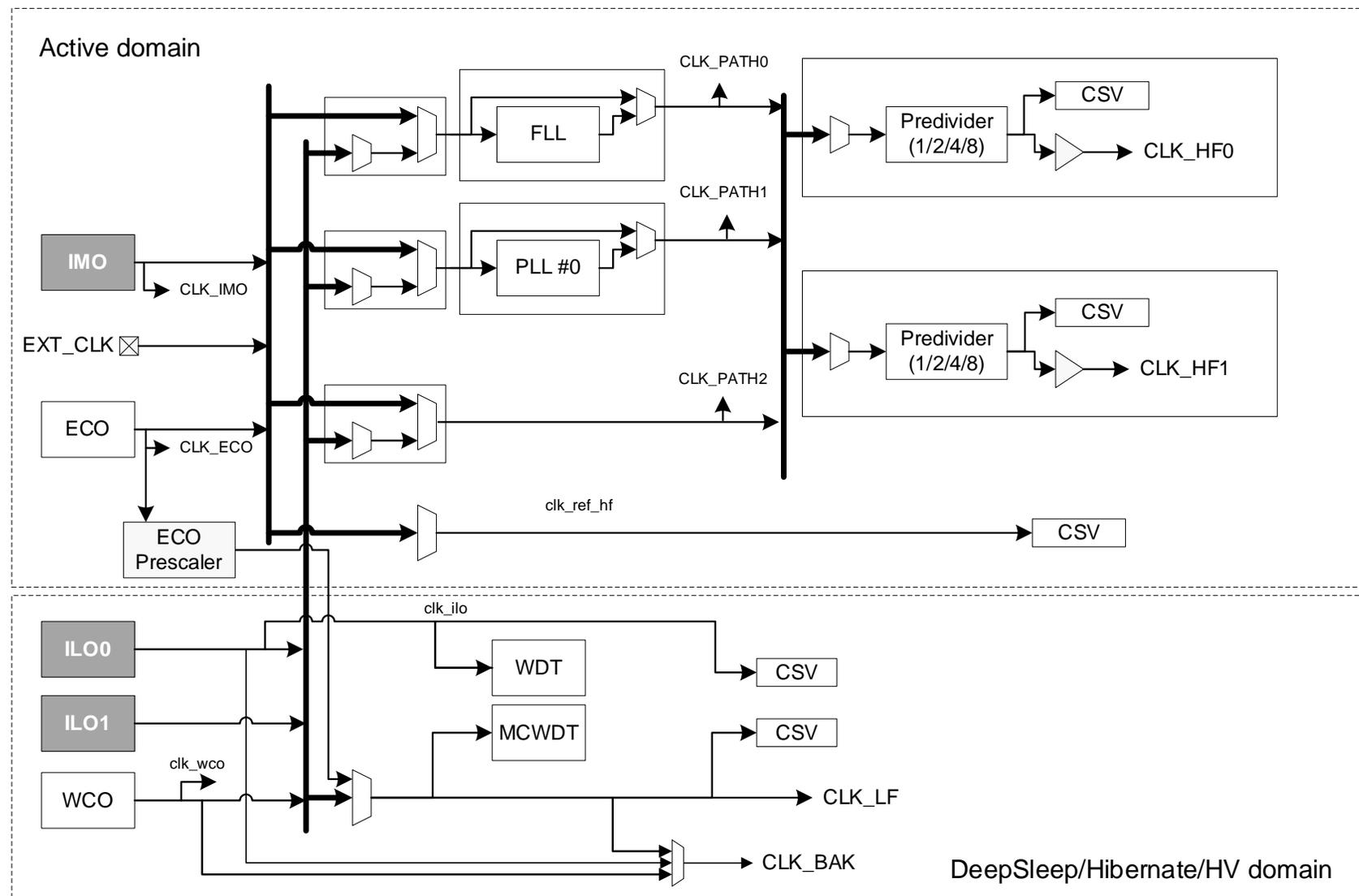
**Review Chapter 18 in the TRM for additional details**

# Clock System Block Diagram



# Internal Clock Sources

- > Internal Main Oscillator (IMO)
- > Internal low-speed oscillator 0/1 (ILO0/1)



# IMO: Internal Main Oscillator

- › Produces an 8-MHz fixed frequency
- › An accurate, high-speed internal (crystal-less) oscillator
- › Available in only Active and Sleep modes
- › Default clock source after POR or any other reset
- › Used by PLL0 to generate a wide range of high-frequency clocks
- › Enabled and disabled by register<sup>1</sup>
  - Default is ENABLE<sup>2</sup>

## Hint Bar

**Review Section 18.2 in the TRM for additional details**

**Refer to the datasheet for additional details on AC specifications**

<sup>1</sup> IMO should not be disabled if it is the source of the clock path to CLK\_HF[0]

<sup>2</sup> Refer to the Register TRM (CLK\_IMO\_CONFIG) for additional details

# ILO 0/1: Internal Low-speed Oscillators

- > ILO0
  - Produces a 32.768-kHz nominal fixed frequency
  - Low power and low accuracy
  - Available in all power modes
  - Always the source of the Watchdog timer<sup>1</sup>
- > ILO1
  - Used for ILO0 clock monitoring
  - Parameters for ILO1 are the same as ILO0

## Hint Bar

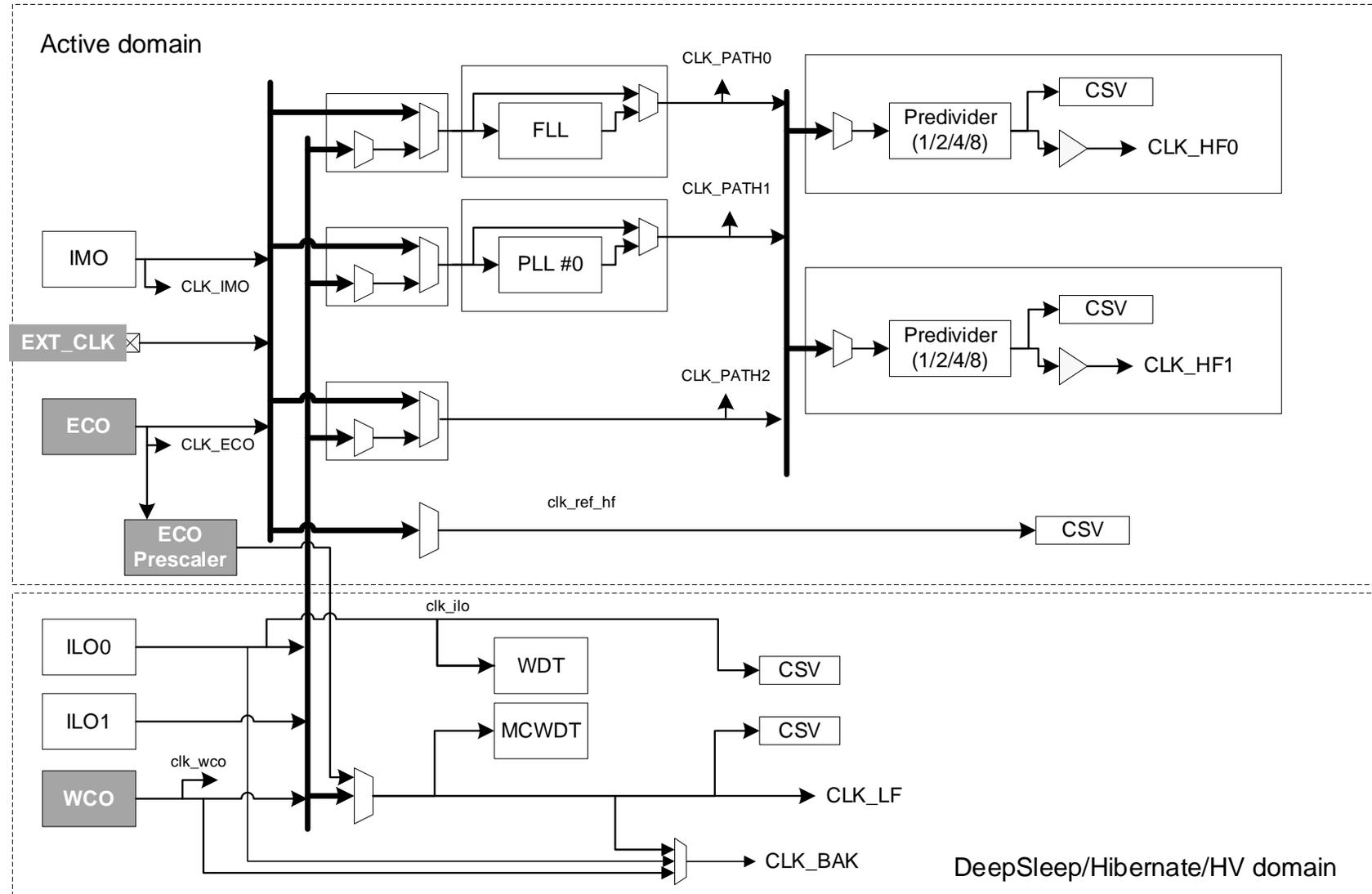
**Review Section 18.2 in the TRM for additional details**

**Refer to the datasheet for additional details on AC specification**

<sup>1</sup> Always leave the ILO enabled, as it is the source of the Watchdog timer

# External Clock Sources

- > ECO
- > WCO
- > EXT\_CLK



# External Clock Sources Overview

- › ECO
  - Contains an oscillator to drive an external 3.988 MHz to 33.34 MHz crystal
  - Used by PLL0 to generate a wide range of high-frequency clocks
  - ECO pre-scaler
  - ECO trimming
  - Enabled and disabled by register<sup>1</sup>
    - Default is DISABLE
- › WCO
  - Highly accurate 32.768-kHz clock source
  - Primary clock source for the real-time clock (RTC)
  - Enabled and disabled by register<sup>2</sup>
    - Default is DISABLE
- › EXT\_CLK
  - 0.25 MHz to 80 MHz clock that can be sourced from a designated I/O pin
  - Can be used as the source clock for either the PLL or FLL
  - Can be used to output the internal clock (CLK\_HF1 is available)
  - When using a pin as an input to EXT\_CLK, I/O must be set appropriately<sup>3</sup>

<sup>1</sup> Refer to the Register TRM (CLK\_ECO\_CONFIG) for additional details

<sup>2</sup> Refer to the Register TRM (CTL) for additional details

<sup>3</sup> Refer to the TRM section 18.2.3 and the datasheet for additional details

## Hint Bar

**Review Section 18.2 in the TRM for additional details**

**Refer to the datasheet for additional details on AC specification**

# ECO Trimming

- > ECO supports a wide variety of crystals and ceramic resonators
- > ECO can be configured by register<sup>1</sup>
  - The following trim bit fields can be configured to control the maximum peak oscillation voltage across the crystal ( $V_P$ ), the transconductance ( $g_m$ ), and the nominal frequency ( $f$ ):
    - ATRIM (Amplitude Trim by AGC)
    - GTRIM (Gain Trim)
    - WDTRIM (Watchdog Trim)
    - FTRIM (Filter Trim)
    - RTRIM (Feedback Resistor Trim)

$$\text{Max peak value: } V_P = \frac{\sqrt{\frac{D_L}{2ESR}}}{\pi f (C_0 + C_L)}$$

$f$ : Fundamental frequency of the crystal (XTAL)

$D_L$ : Maximum drive level of XTAL

ESR: Equivalent series resistance

$C_0$ : Shunt capacitance of XTAL

$C_L$ : Parallel load capacitance of XTAL

$$\text{Transconductance: } g_m > 20 \times ESR \times (2\pi \times f)^2 \times (C_0 + C_L)^2$$

$$\text{Negative resistance: } |R_{neg}| = \frac{g_m \times 4 \times C_L^2}{(2\pi \times f)^2 \times (4 \times C_L^2 + 4 \times C_L \times C_0)^2}$$

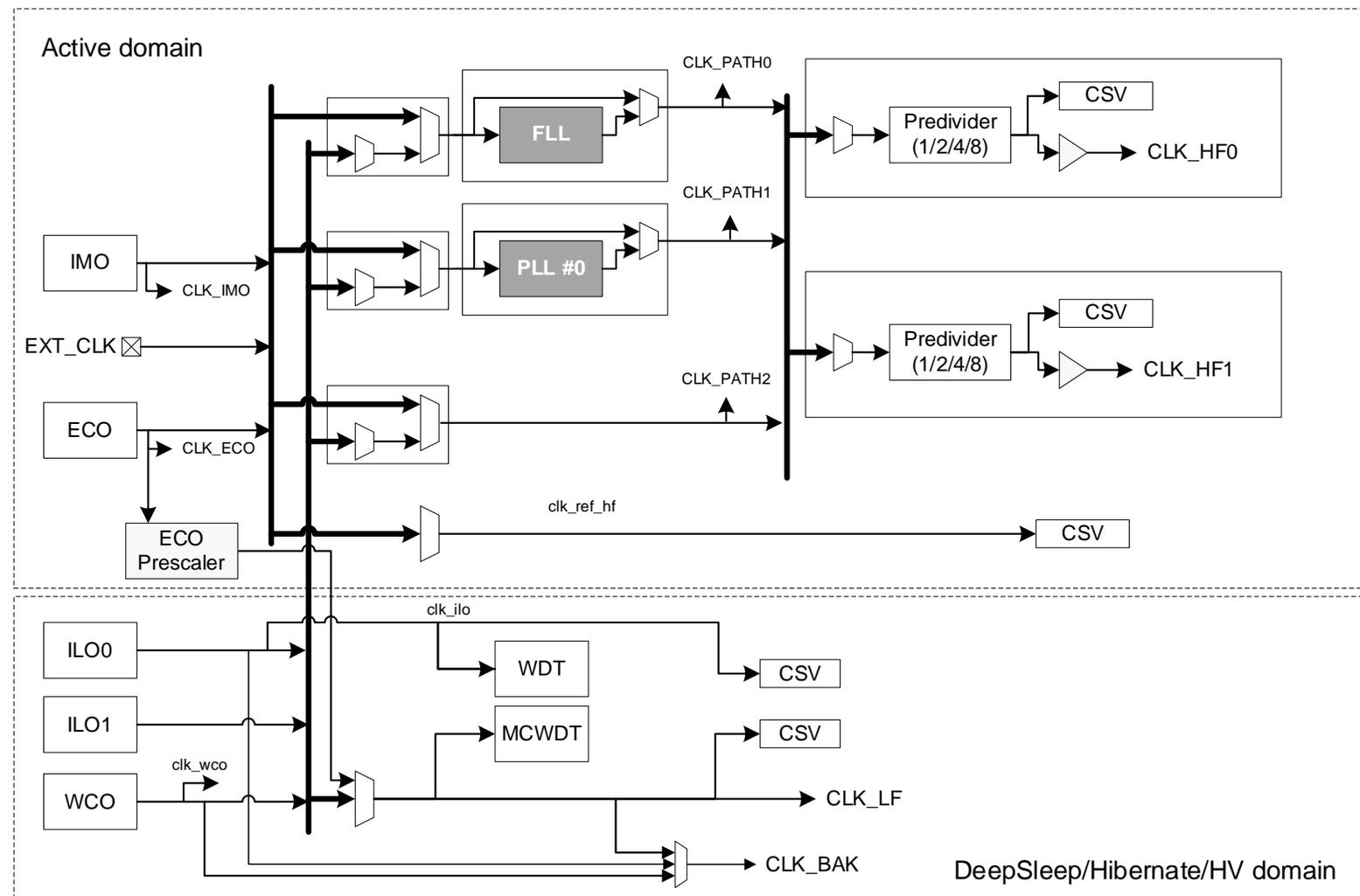
<sup>1</sup> Refer to the Register TRM (CLK\_ECO\_CONFIG2) for additional details.

## Hint Bar

Review TRM section 18.2 for additional details

# High-speed Clock Generation

- > Phase lock loop (PLL)
- > Frequency lock loop (FLL)



# Clock Generation: PLL and FLL

## > PLL

- Input clock can be IMO (8 MHz), ECO, or EXTCLK
- PLL configuration parameters:
  - Input clock range: 3.988 to 33.34 MHz
  - Output clock range: 11 to 160 MHz (CYT2BL)<sup>1</sup>

## > FLL

- Input clock can be IMO (8 MHz), ECO, or EXTCLK
- A counter with a current-controlled oscillator (CCO)
  - Starts up (locks) faster and uses lower power than the PLL
  - The lock tolerance is user adjustable
- Parameters on the FLL configuration:
  - Input clock range: 0.25 MHz to 80 MHz
  - Output clock range: 24 MHz to 100 MHz (CYT2BL)<sup>1</sup>

### Hint Bar

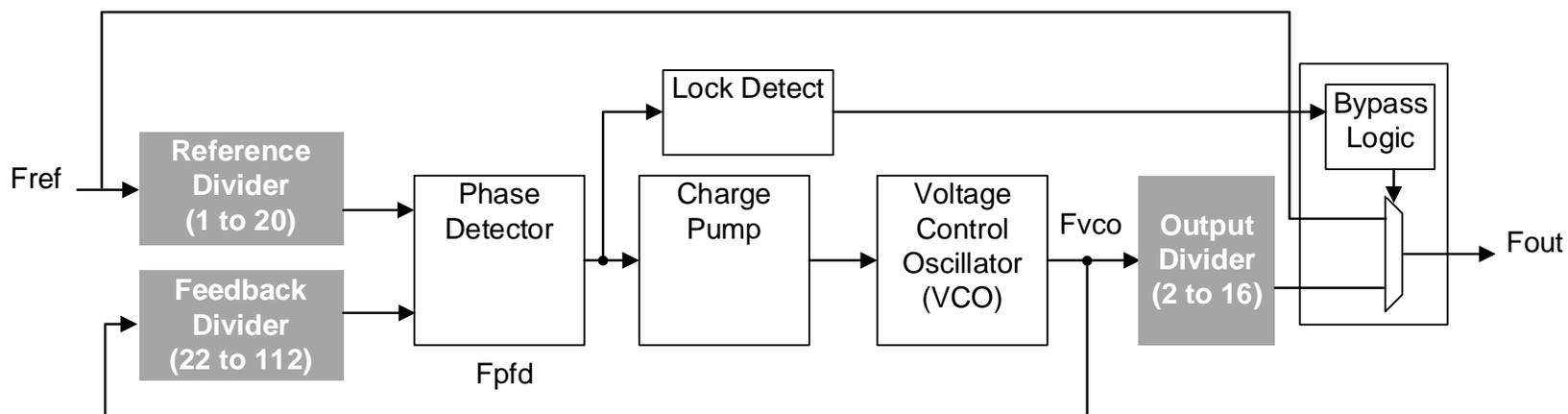
**Review Section 18.3 in the TRM and Register TRM for additional details**

**Refer to the datasheet for additional details on AC specification**

<sup>1</sup> Refer to the data sheet for target product.

# PLL Configuration Example

- > Parameters on PLL configuration:
- > Fref: 3.988 MHz to 33.34 MHz
- > Fout (Fvco/Output divider): 11 MHz to 160 MHz (CYT2BL)<sup>1</sup>
- > Fpdf (Fref/Reference divider): 4 MHz to 8 MHz
- > Fvco (Fpdf \* Feedback divider): 170 MHz to 400 MHz



	Fref	Fout	Fpdf	Fvco
<b>Frequency</b>	8 MHz	160 MHz = Fvco/2	4 MHz = Fref/2	320 MHz = Fpdf x 80
<b>Divider Setting</b>	-	Output Divider: 2	Reference Divider: 2	Feedback Divider: 80

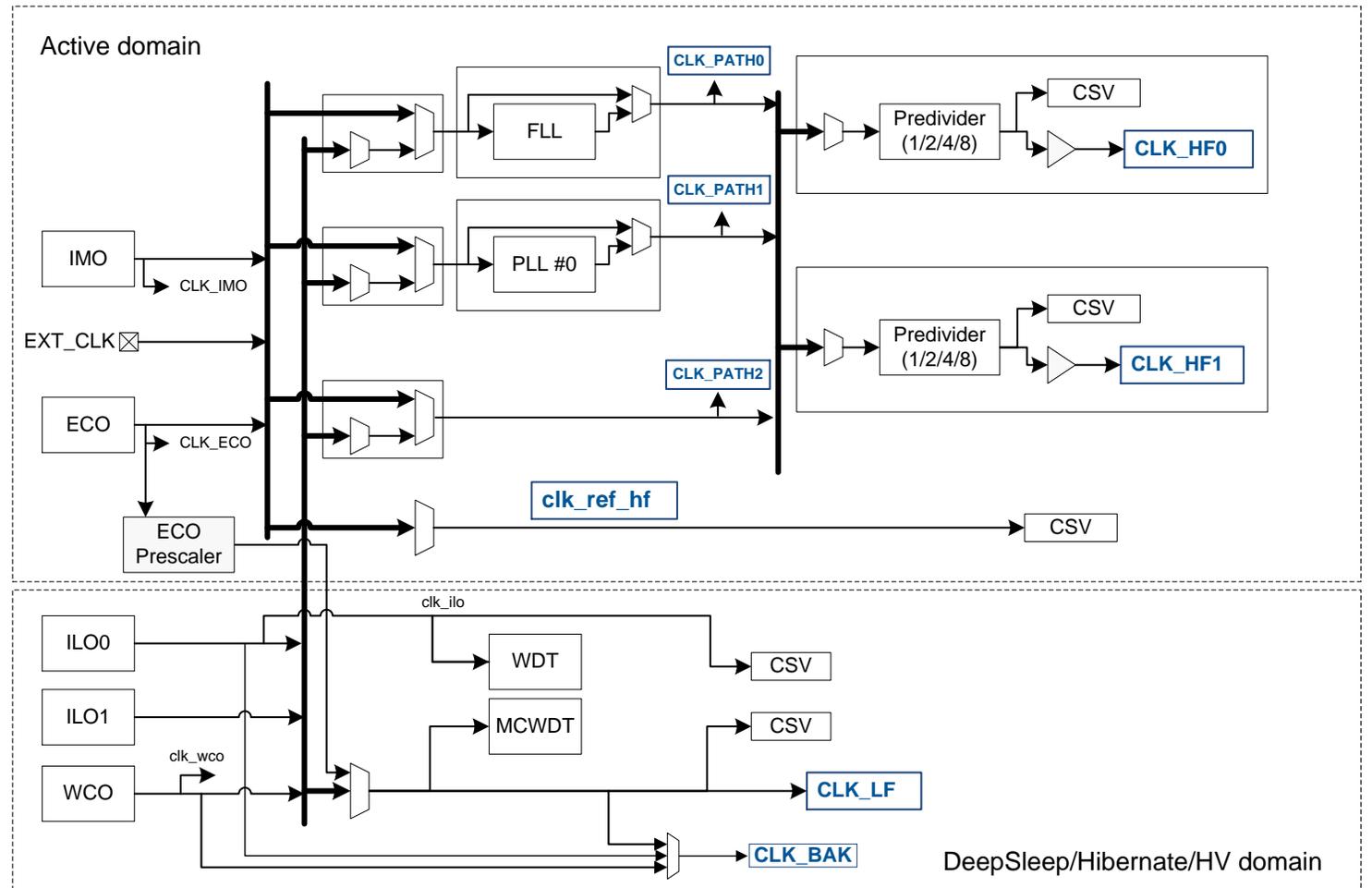
<sup>1</sup> Refer to the data sheet for target product.

**Hint Bar**

Review section 18.3.1 in the TRM and Register TRM for additional details

# Clock Trees

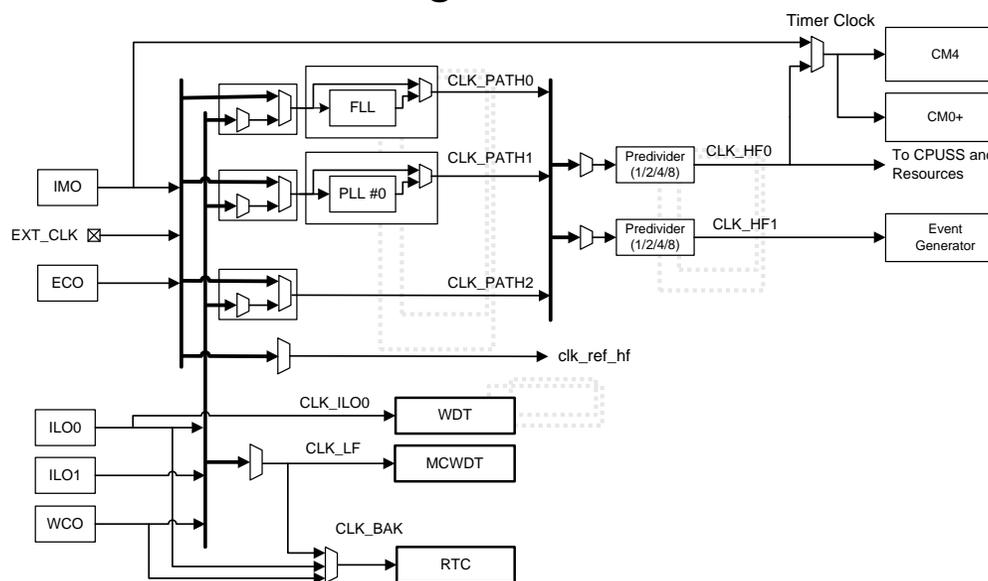
- > CLK\_PATH0/1/2
- > CLK\_HF0/1
- > clk\_ref\_hf
- > CLK\_LF
- > CLK\_BAK
- > CLK\_HF0 distribution



# Clock Distribution

- > CLK\_PATHx
  - Input sources for the CLK\_HF roots
  - CLK\_PATH0 contains the FLL output  
Up to 100 MHz (using FLL)<sup>1</sup>
  - CLK\_PATH1 contains the PLL output  
Up to 160 MHz (using PLL)<sup>1</sup>
  - CLK\_PATH2 is a connection to root clocks  
Up to 33.34 MHz (using ECO)
- > CLK\_REF\_HF
  - Selects IMO, ECO, EXTCLK
  - Typically selects the IMO (8 MHz)
  - Used as a reference clock for CLK\_HF0/1 clock supervision

- > CLK\_HF0/1
  - Selects CLK\_PATH0, 1, 2
  - CLK\_HF0 is the input source for the CPUSS and resources such as Timer, SCB, and SAR ADC
  - CLK\_HF1 is the input source for the event generator



## Hint Bar

Training section reference:

- CPU Subsystem

<sup>1</sup> Refer to the data sheet for target product.

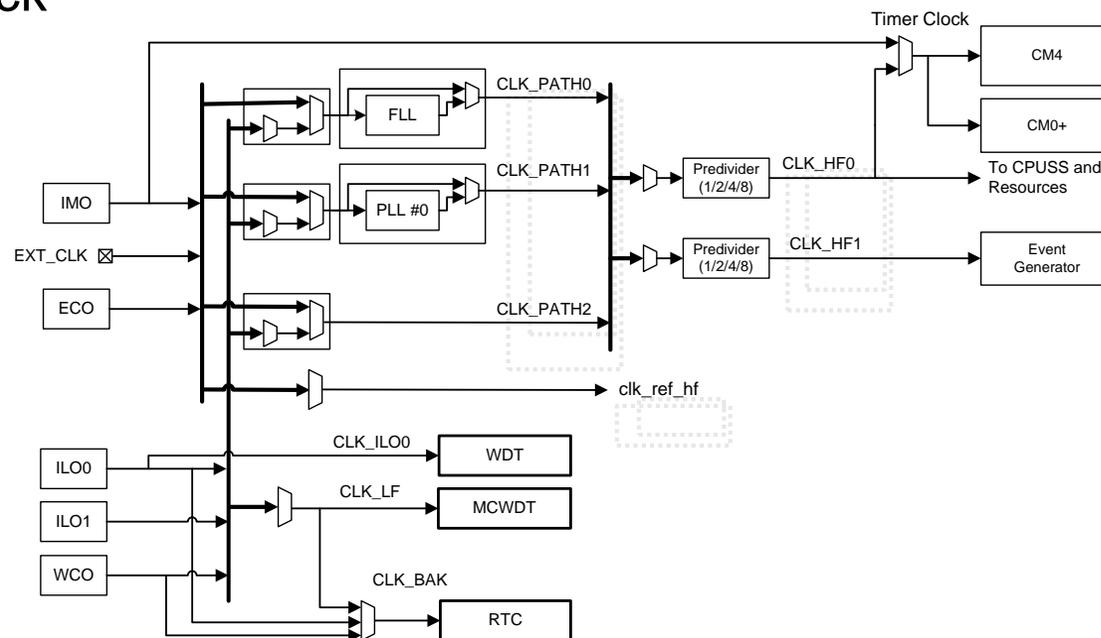
# Clock Distribution

- > CLK\_LF
  - ILO0, ILO1, or WCO (32.768 kHz) can be the input clock for CLK\_LF
  - Input sources for the MCWDT clock
  - Uses reference clock for CLK\_ILO0 Clock Supervision
- > CLK\_BAK
  - ILO0, ILO1, or WCO (32.768 kHz) can be the input clock for CLK\_BAK
  - Input sources for RTC<sup>1</sup> clock

Hint Bar

**Training section reference:**

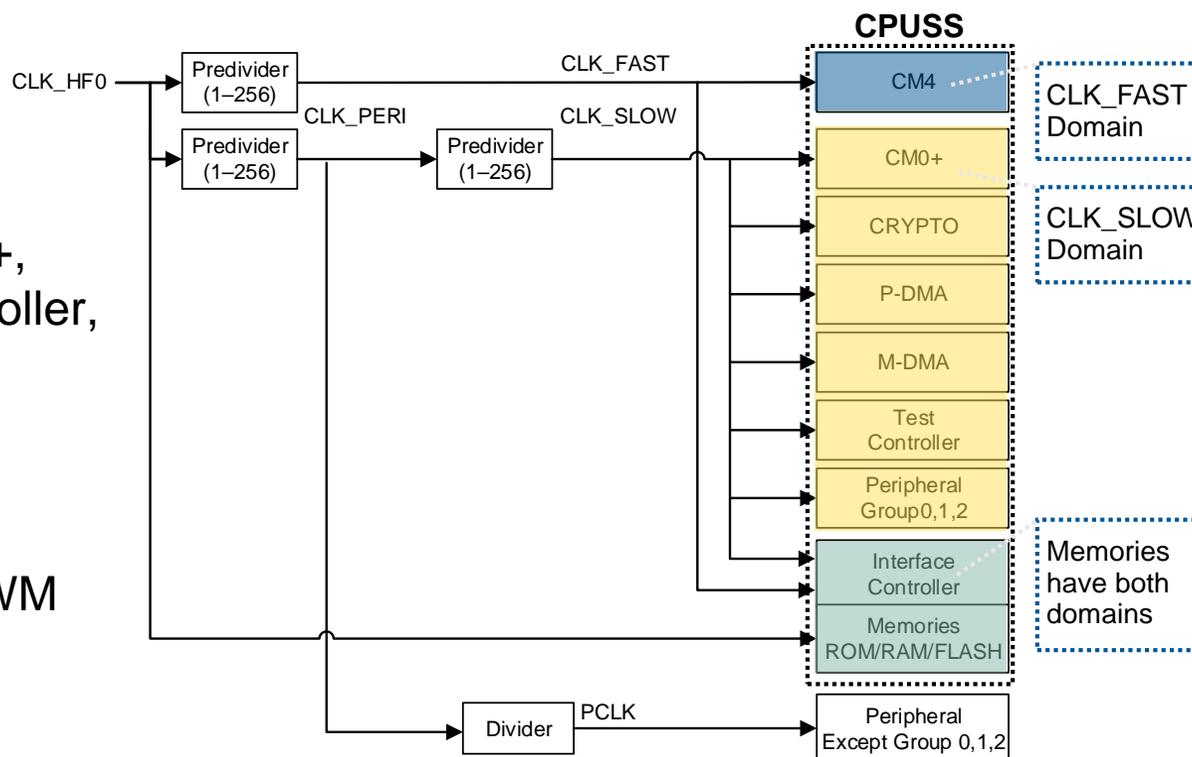
**- CPU Subsystem**



<sup>1</sup> Typically WCO is connected to RTC. CLK\_LF also can connect to RTC.

# CLK\_HF0<sup>1</sup> Distribution

- > The root clock for the CPUSS and the peripherals
- > Distributed to CLK\_FAST, CLK\_SLOW, and CLK\_PERI
- > CPUSS has CLK\_FAST and CLK\_SLOW domains
- > CLK\_FAST
  - Source clock for CM4
  - Up to 160 MHz<sup>2</sup>
- > CLK\_SLOW
  - Source clock for the CM0+, Crypto, DMAs, Test Controller, some peripherals<sup>3</sup>
  - Up to 100 MHz<sup>2</sup>
- > CLK\_PERI
  - Source clock for all peripherals such as TCPWM and SCB, via divider
  - Up to 100 MHz<sup>2</sup>



Hint Bar

**Training section references:**

**- CPU Subsystem**

<sup>1</sup> CLK\_HF0 can be enabled and disabled by register. CLK\_HF0 is always enabled as the clock source of CPU.

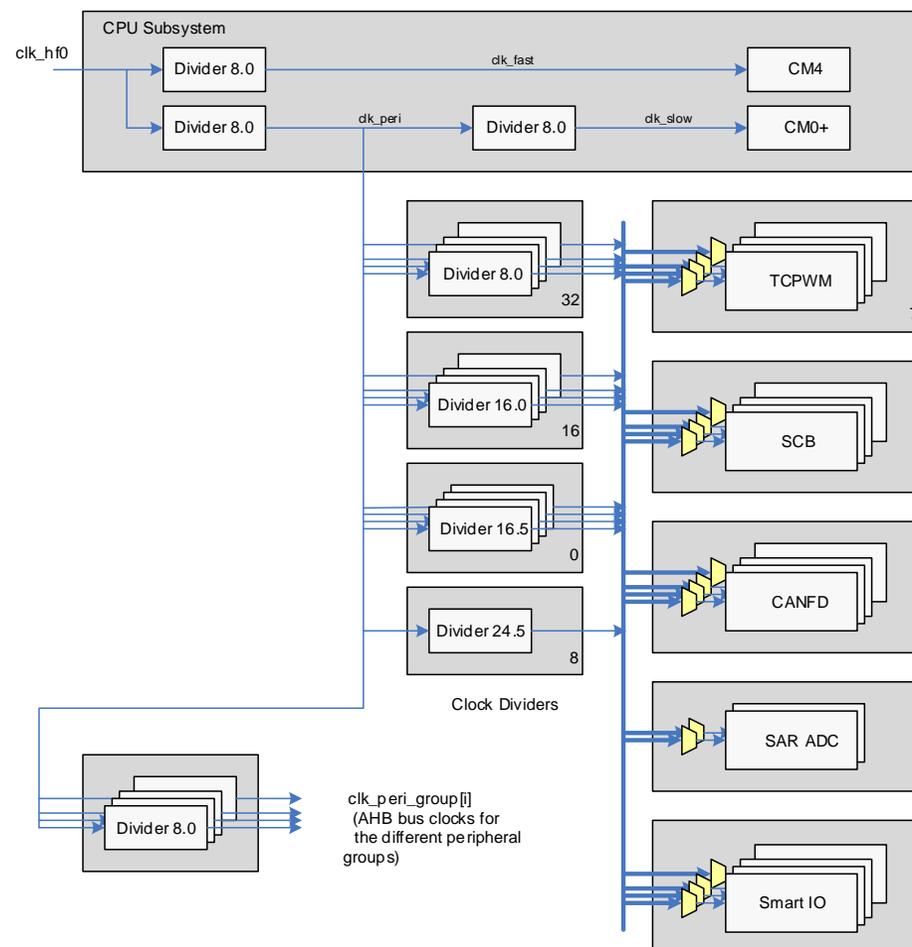
<sup>2</sup> Refer to the data sheet for target product.

<sup>3</sup> CPUSS and PPU registers

# Peri Clock Distribution

## > PERI Clock Divider

- Four types of dividers<sup>1</sup>
  - 8-bit divider
  - 16-bit divider
  - 16.5-bit divider
  - 24.5-bit divider
- Fractional clock dividers supported
- Output of dividers can be routed to any peripheral
- Phase aligning
  - Can be phase-aligned with any of the other (enabled) clock dividers.



## Hint Bar

**Clock dividers can be configured through the following registers:**

- DIV\_8\_CTL
- DIV\_16\_CTL
- DIV\_16\_5\_CTL
- DIV\_24\_5\_CTL

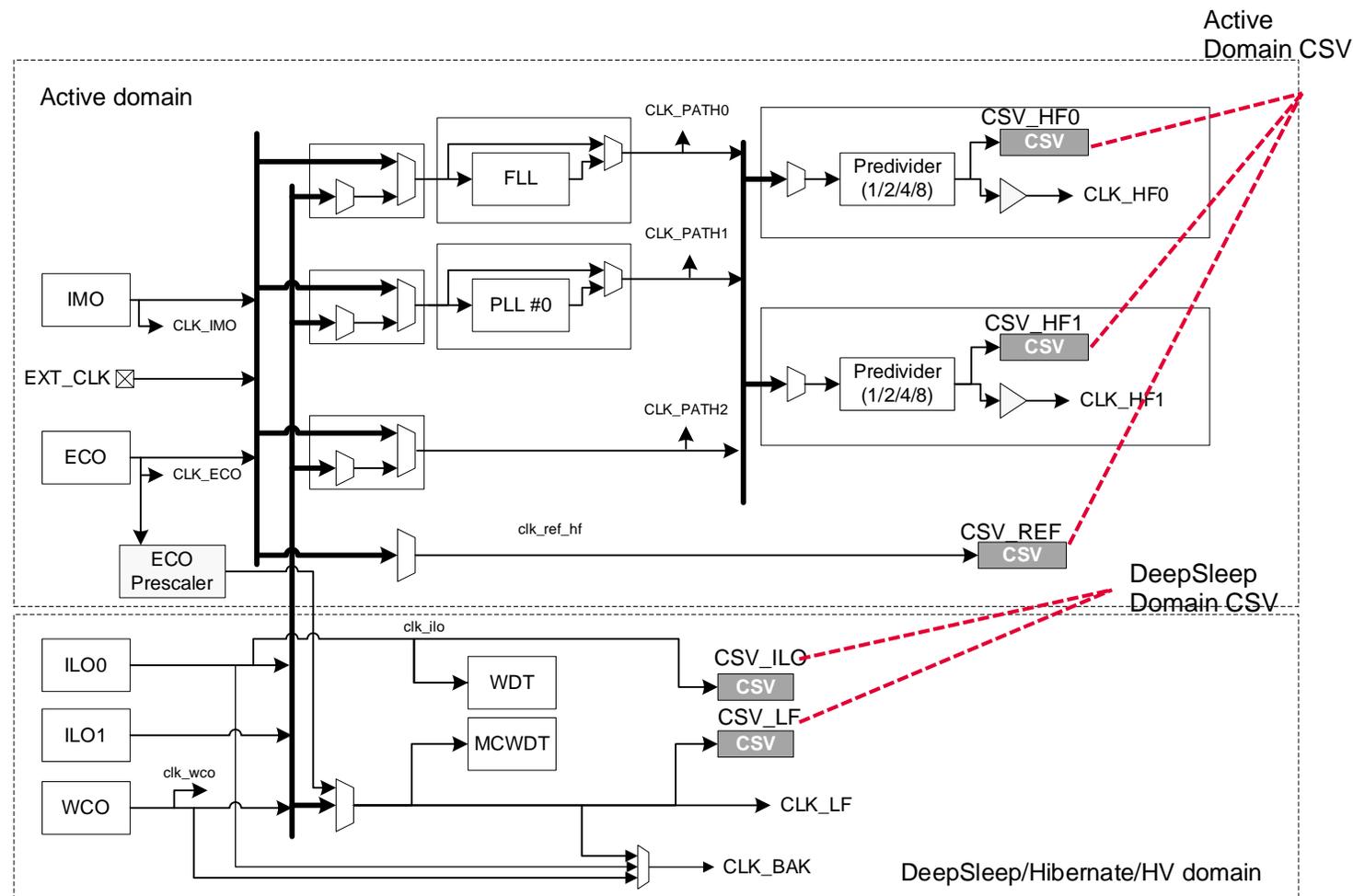
**Clock Enable multiplexers can be configured through CLOCK\_CTL registers, which are assigned for each peripheral**

**Review Section 18.7 in the TRM for additional details on clock numbers, which are assigned for each peripheral**

<sup>1</sup> Not all dividers are supported

# Clock Supervision (CSV)

- > Clock supervision (CSV) allows one clock to be monitored with another clock (reference clock)
- > Monitored clock sources:
  - CLK\_HF0
  - CLK\_HF1
  - CLK\_REF\_HF
  - ILO0
  - CLK\_LF
- > CSV power domains:
  - Active domain CSV
  - DeepSleep domain CSV

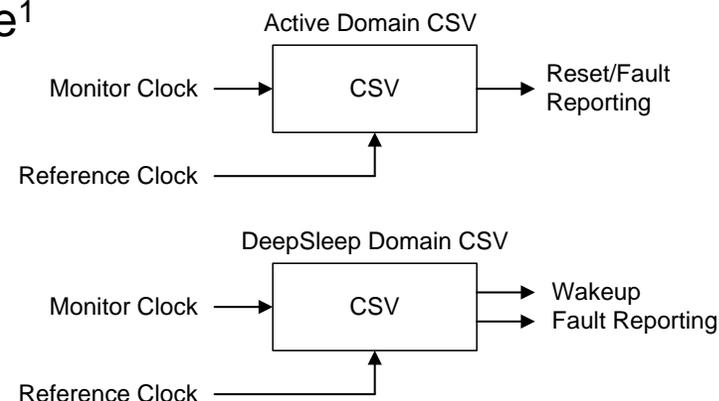


# Clock Supervision Features

- > Checks that the frequency of the monitored clock is within the allowed frequency window
  - Uses a reference clock to supervise the behavior of the monitor clock

CSV Components	Monitor Clock	Reference Clock	Note
CSV_HF0/1	CLK_HF0/1	clk_ref_hf	clk_ref_hf is typically selected the IMO (default)
CSV_REF	clk_ref_hf	ILO0	-
CSV_ILO	ILO0	CLK_LF	CLK_LF is selected WCO or ILO1
CSV_LF	CLK_LF	ILO0	-

- Active domain CSV: CSV\_HF0/1, CSV\_REF
  - Automatically stops during DeepSleep, and restarts by wakeup
  - Wait function of monitoring start for startup time<sup>1</sup>
  - Possible to generate a Reset or a Fault report
- DeepSleep domain CSV: CSV\_ILO, CSV\_LF
  - Operates during Active and DeepSleep
  - Generates Wakeup and Fault reports
- All CSVs are initially OFF



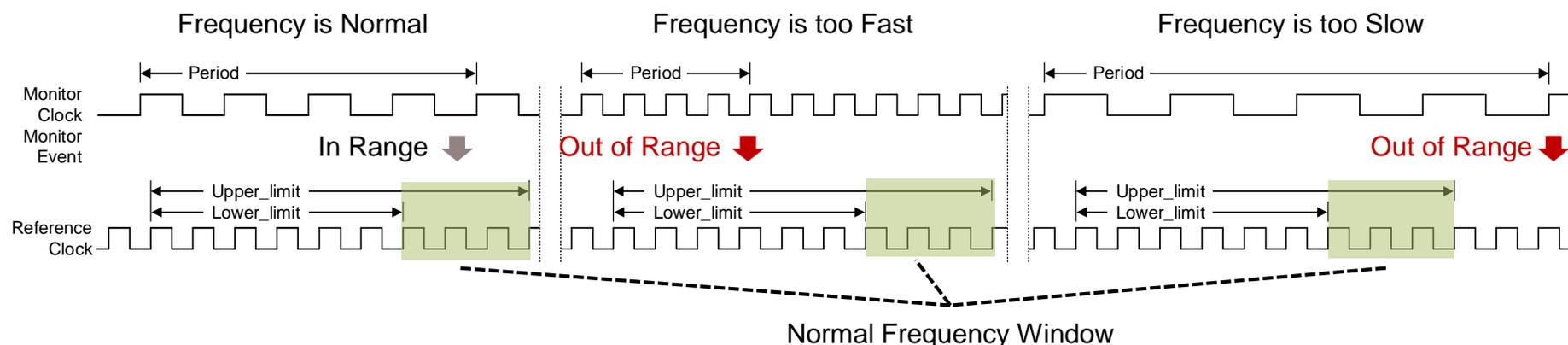
**Hint Bar**

**See the Register TRM for additional details**

<sup>1</sup> Need to prevent a false error detection at startup

# CSV Operation

- > The monitored clock generates a Monitor event (Period), and the reference clock generates a lower and upper limit
- > The Monitor event is compared against a lower limit/upper limit
- > An error is reported, if the Monitor event  $\leq$  lower limit, or the Monitor event  $>$  upper limit



- > Advantages
  - Detects whether the clock stops, runs too fast or runs too slow, and if the period is not within the frequency window
  - Monitors clock in each power mode such as Active, Sleep, and DeepSleep with Active domain CSV and DeepSleep domain CSV
  - Can achieve ASIL-B

## Hint Bar

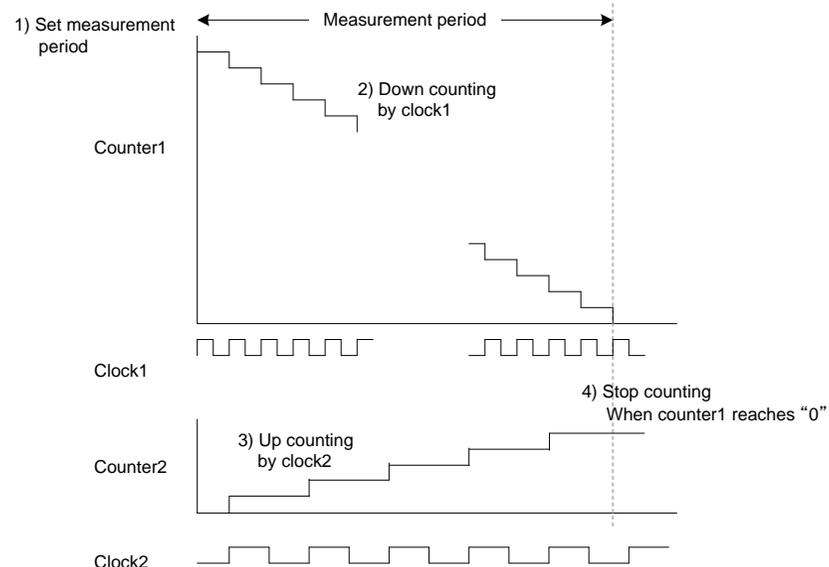
The monitor clock and the reference clock are asynchronous (typical). Therefore, the frequency window needs to account for maximum clock tolerance.

# Clock Calibration Counter

- > Clock Calibration Counter Operation
  - Two counters: Counter1 and Counter2
    - Counter1 is clocked by clock1: reference clock
    - Counter2 is clocked by clock2: measurement clock.
  - Counter1 sets the measurement period by the count number of clock1
  - Counter2 indicates the count number of clock2 during the measurement period
  - Clock2 frequency can be calculated from the following formula using two count numbers:

$$\text{clock2frequency} = \frac{\text{Counter2value}}{\text{Counter1value}} \times \text{clock1frequency}$$

- All clock sources are available as a source for these two clocks.
- > Use case
  - Measure a lower-accuracy clock, such as the ILO, using a higher-accuracy clock such as the ECO



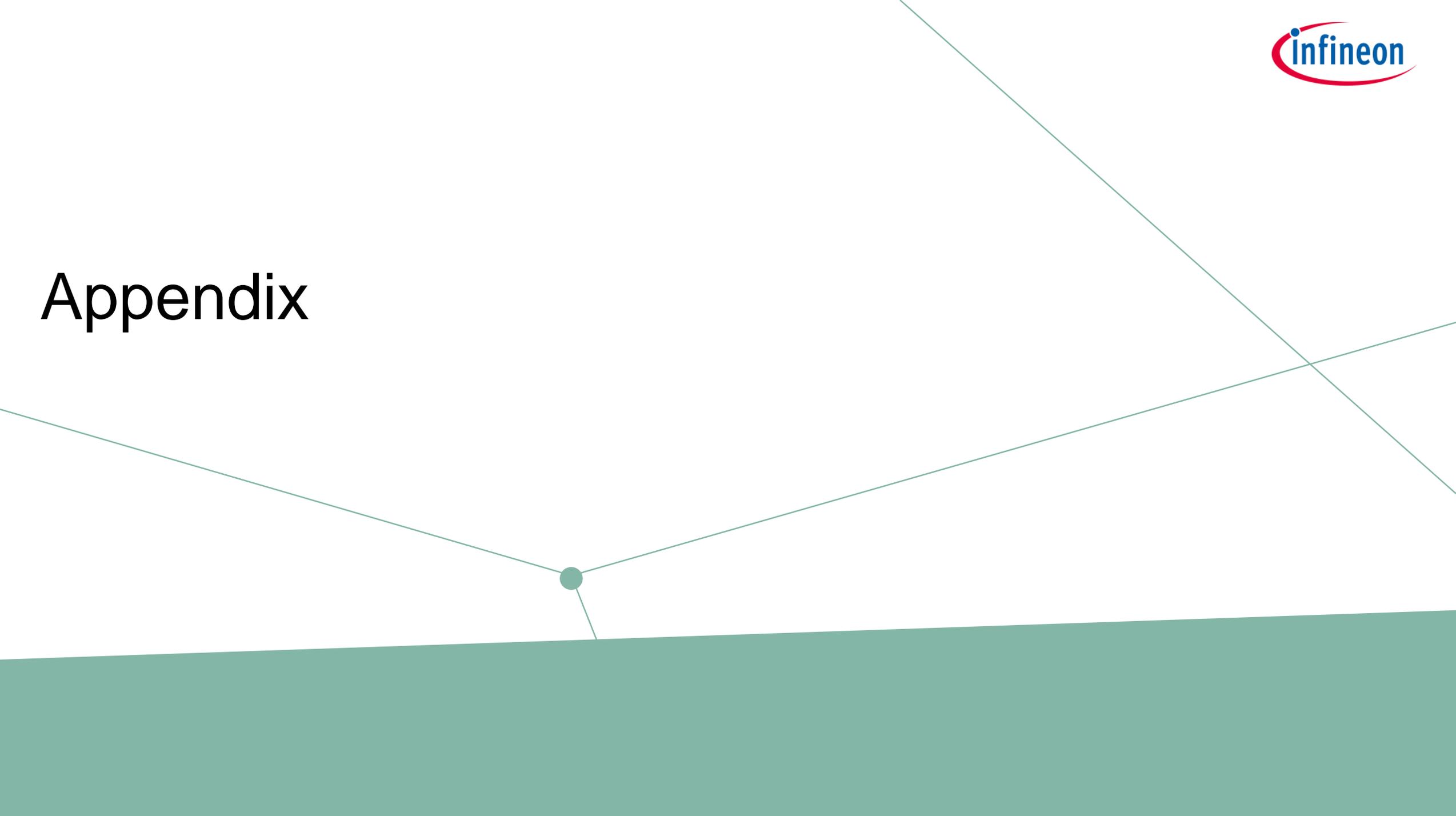
## Hint Bar

**Review Section 18.8 in the TRM for additional details**

**Count Clock1, 2 can be selected through registers:**

**CLK\_OUTPUT\_FAST**

# Appendix



# Comparison Between CYT2BL, CYT4BF, and CYT4DN (1/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
IMO			Supported		
ECO			Supported		
ILO 0			Supported		
ILO 1			Supported		
WCO			Supported		
LPECO		Not implemented		Supported	
FLL	Number of FLL	1			
	Input Range	0.25 to 80 MHz		0.25 to 100 MHz	
	Output Range	24 to 100 MHz			
PLL	Number of PLL	1	2	3	
	Input Range	3.988 to 33.34 MHz			
	Output Range	11 to 160 MHz	11 to 200 MHz		
PLL400	Number of PLL	Not implemented	2	5	
	Input Range	Not implemented	3.988 to 33.34 MHz		
	Output Range	Not implemented	25 to 350 MHz (*)	25 to 400 MHz	(*) Spreading off
	SSCG	Not implemented	Yes		
	Fractional Operation	Not implemented	Yes		

# Comparison Between CYT2BL, CYT4BF, and CYT4DN (2/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
CLK Trees Source Clock	CLK_PATH 0	FLL			
	CLK_PATH 1	PLL	PLL400		
	CLK_PATH 2	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL400		
	CLK_PATH 3	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL	PLL400	
	CLK_PATH 4	Not implemented	PLL	PLL400	
	CLK_PATH 5	Not implemented	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL400	
	CLK_PATH 6	Not implemented		PLL	
	CLK_PATH 7	Not implemented		PLL	
	CLK_PATH 8	Not implemented		PLL	
	CLK_PATH 9	Not implemented		ECO,IMO,EXT_CLK,WCO, ILO0/1,LPECO	
	CLK_REF_HF	ECO,IMO,EXT_CLK		ECO,IMO,EXT_CLK ,LPECO	
	CLK_TIMER	CLK_HF0, IMO	IMO		
	CLK_LF	ILO0/1, WCO, ECO		ILO0/1, WCO, ECO ,LPECO	
CLK_BAK	CLK_LF, ILO0, WCO		CLK_LF, ILO0, WCO ,LPECO		

# Comparison Between CYT2BL, CYT4BF, and CYT4DN (3/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
CLK Distribution	CLK_HF0	CPUSS clocks, PERI, and AHB infrastructure	CPUSS (Memories, CLK_SLOW, Peripherals)	CPUSS (Memories, CLK_SLOW, Peripherals)	
	CLK_HF1	Event Generator	CPUSS (Cortex-M7 CPU 0, 1)	CPUSS (Cortex-M7 CPU 0, 1)	
	CLK_HF2	Not connect	CAN FD, FlexRay, LIN, TCPWM, SCB, SAR	CAN FD, CXPI, LIN, SCB, SAR	
	CLK_HF3	Not implemented	Event Generator	Event Generator	
	CLK_HF4	Not implemented	Ethernet	Ethernet	
	CLK_HF5	Not implemented	Audio subsystem	Sound Subsystem #0	
	CLK_HF6	Not implemented	SDHC Interface, SMIF	Sound Subsystem #1	
	CLK_HF7	Not implemented	Not connect	Sound Subsystem #2	
	CLK_HF8	Not implemented	Not implemented	SMIF #0	
	CLK_HF9	Not implemented	Not implemented	SMIF #1	
	CLK_HF10	Not implemented	Not implemented	Video Subsystem	
	CLK_HF11	Not implemented	Not implemented	Video Display #0	
	CLK_HF12	Not implemented	Not implemented	Video Display #1	
	CLK_HF13	Not implemented	Not implemented	Not connect	

# Comparison Between CYT2BL, CYT4BF, and CYT4DN (4/4)

Features		CYT2BL	CYT4BF	CYT4DN	Note
Clock Divider	Number of Dividers	1	2		
	Fractional Clock Divider	24.5-bit dividers		16.5-bit dividers, 24.5-bit dividers	
	Phase Aligning	Supported			
Clock Supervision		Supported			
Calibration Counter		Supported			



Part of your life. Part of tomorrow.

# Revision History

Revision	ECN	Submission Date	Description of Change
**	6157641	04/29/2018	Initial release
*A	6364397	10/25/2018	Added slide 2 and the note descriptions of all pages. Updated slides 3-6, 9, 11, 14, 19. Added Clock Calibration Counter slide Updated the figures
*B	7060645	01/06/2021	Updated slide 2 - 4, 8, 10, 13, 16, 17, 18, 25-28 Deleted slide 4 Added slide 11