Customer Training Workshop

Traveo™ II Body Controller High Power Supply and Monitoring
### Target Products

**Target product list for this training material:**

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo™ II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384KB</td>
</tr>
</tbody>
</table>
Power supply monitoring functions are in System Resources

- Power-on reset (POR)
- Brownout detection (BOD)
- Over-voltage detection (OVD)
- Low-voltage detection (LVD)
- Low drop-out regulator (LDO)

System Resources

- Power
  - POR
  - LVD
  - PED
  - LDO

- Sleep Control

- Clock
  - 2xLO
  - WDT
  - IMO
  - ECO
  - 4xPLL

- Reset
  - Reset Control
  - XRES

- Test
  - Test Mode Entry
  - Digital DFT
  - Analog DFT

Power Modes

- Active/DeepSleep
- LowPower/Active/DeepSleep
- Hibernate

CPU Subsystem

- Cortex M7
  - 350 MHz

Peripheral Interconnect (MMIO, PPU)

- Prog.
  - Analog
  - ADC
  - ADC (12-bit)

IO Subsystem

- 1x 32-bit I/O Matrix, Smart I/O, Boundary Scan
- 5x Smart I/O

System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)

Introduction

Review TRM section 16.2 for additional details
Power Supply Overview

- 2.7 to 5.5-V power supply range
- Core regulators for High Current, Active, and DeepSleep modes
  - Digital power supply
  - External high-current regulator controller with load current up to 600 mA
  - Internal logic supply for device startup (boot process) and for applications with load current up to 300 mA
  - Core power supply
  - Internal logic power supply for DeepSleep mode
  - Analog power supply
  - I/O power supply

Review TRM section 16.2 for additional details

VDDD/VSSD: Digital power supply/ground
VDDIO_1/2/VSSD: I/O power supply/ground
VDDIO_3/4/VSSIO_3/4: I/O power supply/ground
VDDA/VSSA: Analog power supply/ground
VCCD/VSSD: Internal core supply/ground
## Power Pins and Rails

### Power/ground pins and voltage range

<table>
<thead>
<tr>
<th>Supply Pin</th>
<th>Ground Pin</th>
<th>Power Supply Voltage Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{DDD}}$</td>
<td>$V_{\text{SSD}}$</td>
<td>2.7 V to 5.5 V</td>
<td>Digital and I/O supply</td>
</tr>
<tr>
<td>$V_{\text{CCD}}$</td>
<td>$V_{\text{SSD}}$</td>
<td>1.1 V to 1.2 V</td>
<td>Core supply</td>
</tr>
<tr>
<td>$V_{\text{DDA}}$</td>
<td>$V_{\text{SSA}}$</td>
<td>2.7 V to 5.5 V</td>
<td>Analog supply, $V_{\text{DDA}} = V_{\text{DDIO}_2}$</td>
</tr>
<tr>
<td>$V_{\text{DDIO}_1}$</td>
<td>$V_{\text{SSD}}$</td>
<td>2.7 V to 5.5 V</td>
<td>I/O supply</td>
</tr>
<tr>
<td>$V_{\text{DDIO}_2}$</td>
<td>$V_{\text{SSD}}$</td>
<td>2.7 V to 5.5 V</td>
<td>I/O supply</td>
</tr>
<tr>
<td>$V_{\text{DDIO}_3}$</td>
<td>$V_{\text{SSIO}_3}$</td>
<td>2.7 V to 3.6 V</td>
<td>I/O supply</td>
</tr>
<tr>
<td>$V_{\text{DDIO}_4}$</td>
<td>$V_{\text{SSIO}_4}$</td>
<td>2.7 V to 3.6 V</td>
<td>I/O supply</td>
</tr>
</tbody>
</table>

Review TRM section 16.2.2 for additional details.
Power Supply

- **Power supply sources**
  - VDDD, VDDIO_1, VDDIO_3, and VDDIO_4 supplies are independent
  - VDDA1 and VDDIO_2 must be the same

- **Power sequencing requirements**
  - VDDD, VDDIO_1, VDDIO_3, and VDDIO_4 have no sequencing limitations
  - VDDA = VDDIO_2

- **Advantage**
  - Less effort and cost because no external power sequencing control is required for applications with load current up to 300 mA
Regulator Selection

› High-current regulator selection
  - Device starts up with Active regulator, which supports up to 300 mA supply current
  - Switches to high-current regulator if supply current of up to 600 mA is required

› Two types of external regulator configuration
  - External transistor
  - PMIC/LDO

Review datasheet and TRM section 16.2.5 for additional details
Sensing with the resistor controls the transistor and adjusts the supply voltage (VCCD)

- **DRV_VOUT**: Dedicated external supply control pin
- **EXT_PS_CTL0**: Sense input plus
- **EXT_PS_CTL1**: Sense input minus

Review datasheet and TRM section 16.2.5 for additional details
External Regulator: External Transistor Configuration (Software)

- Changing from Active regulator to high-current regulator controller with external transistor
  - Setup flow

Call `ConfigureRegulator` API:
- `PWR_REGHC_CTL.REGHC_MODE = 0` (Select external transistor mode)
- `PWR_REGHC_CTL.REGHC_TRANS_USE_OCD = 1`
- `PWR_REGHC_CTL.REGHC_CONFIGURED = 1`

Call `SwitchOverRegulators` API:
- `PWR_REGHC_CTL2.REGHC_EN = 1`
- Wait until `PWR_REGHC_STATUS.SEQ_BUSY == 0` and `PWR_REGHC_STATUS.REGHC_ENABLED == 1`
- This should occur within 15 μs
External Regulator:
PMIC Configuration (Hardware)

- High-current regulator controller provides adjustable reference and reset
  - EXT_PS_CTL0: Power good input from PMIC
  - EXT_PS_CTL1: Enable output for PMIC
  - EXT_PS_CTL2: Reset threshold adjustment for some PMIC (RADJ-pin\(^1\))

\(^1\) RADJ is optional and may not be present depending on the PMIC used

Recommended PMICs:
- Cypress S6BP501A
- Rohm BD9S200MUF-C

Review datasheet and TRM section 16.2.5 for additional details
External Regulator: PMIC Configuration (Software)

- Changing from active regulator to high-current regulator controller with external PMIC
  - Setup flow

  **Call ConfigureRegulator API:**
  - `PWR_REGHC_CTL.REGHC_MODE = 1` (PMIC mode)
  - `PWR_REGHC_CTL.REGHC_PMIC_STATUS_INEN = 1` to enable the input path for PMIC status
  - `PWR_REGHC_CTL.REGHC_PMIC_STATUS_POLARITY` to the setting that indicates an error condition (depending on the polarity of the PMIC status output)
  - `PWR_REGHC_CTL.REGHC_PMIC_CTL_OUTEN = 1` and `PWR_REGHC_CTL.REGHC_PMIC_CTL_POLARITY` to the setting that enables the PMIC (depending on polarity of PMIC enable input)
  - `PWR_REGHC_CTL.REGHC_VADJ` to the required feedback setting for the chosen PMIC

  **Call SwitchOverRegulators API:**
  - `PWR_REGHC_CTL2.REGHC_EN = 1`
  - Wait until `PWR_REGHC_STATUS.SEQ_BUSY == 0` and `PWR_REGHC_STATUS.REGHC_ENABLED == 1`

  This delay depends strongly on the startup time of the PMIC, based on its status output and the value in `PWR_REGHC_CTL2.REGHC_PMIC_STATUS_WAIT`
Voltage Monitoring Overview

- Supports multiple voltage monitoring and supply failure protection

Review datasheet and TRM section 16.3 for additional details.
Voltage Monitoring Overview

› Power-On Reset (POR)

Review datasheet and TRM section 16.3 for additional details
Power-On Reset (POR)

- Initializes the device at power-up
- Always on
  - POR on VDDD
  - Provide a reset pulse during the initial power ramp

Review datasheet and TRM section 16.3.1 for additional details
Brown-out Detection (BOD)

Review datasheet and TRM section 16.3 for additional details
BOD Overview

- Detects supply condition below a threshold and applies a reset to the device
- Always on except in Hibernate and XRES modes
  - **BOD on VDDD**
    - Generates a reset if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V\(^1\) (default) or < 3.0 V
  - **BOD on VDDA**
    - Generates a reset, a fault, or no action\(^2\) (default) if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V\(^1\) (default) or < 3.0 V
  - **BOD on VCCD**
    - Generates a reset if a voltage excursion dips below the falling trip point

\(^1\) If \(V_{DDD}/V_{DDA}\) falls below 2.7 V (minimum \(V_{CCD}/V_{DDA}\)), the device will operate out of specification. To prevent that, use the 3.0-V trip point.

\(^2\) Even if \(V_{DDA}\) is low, the MCU can boot because it does not generate a reset as default.
Low-Voltage Detection (LVD)

Review datasheet and TRM section 16.3 for additional details
LVD Overview

- Detects the warning voltage level to take preventive measures in the system
- Can be enabled or disabled (default) by software, except in Hibernate and XRES mode
- LVD on VDDD
  - Generates an interrupt or a fault if a voltage level meets the trip point
    - An interrupt or a fault and trip point are configurable by software
    - Supports up to 26 trip points to monitor between 2.8 V and 5.3 V (0.1-V step)
    - Can be configured as falling (low voltage), rising (high voltage), or both detection
- Use case for two LVD units
  - LVD1: Use the falling trip point (3.5 V) to detect the low-voltage warning
  - LVD2: Use the rising trip (5.3 V) to detect the over-voltage warning
POR, BOD, and LVD Use Cases (1/2)

- **Purpose:** Judge whether RAM contents have been retained by using voltage monitoring
- **Setting and condition**
  - MCU operation conditions:
    - LVD trip point can be in MCU operation range – RAM retention
    - LVD falling trip point (3.5 V): Warning LVD for safety system operation
    - LVD rising trip point (4.0 V): User program restart trigger
  - BOD reset (<3.0 V) is an asynchronous reset – No RAM retention
- **Use Case:** For RAM, contents are retained (no BOD reset generation)
POR, BOD, and LVD Use Cases (2/2)

› Purpose: Judge whether RAM contents have been retained by using voltage monitoring

› Setting and condition
  - MCU operation conditions:
    - LVD trip point can be in MCU operation range – RAM retention
    - LVD falling trip point (3.5 V): Warning LVD for safety system operation
    - LVD rising trip point (4.0 V): User program restart trigger

› BOD reset (<3.0 V) is an asynchronous reset – No RAM retention

› Use Case: For RAM, contents have not been retained (BOD reset generation)
Advantage for POR, BOD, and LVD

- Reduced BOM costs for low-cost applications using internal POR, BOD, and LVD¹

¹ Review TRM and datasheet to confirm if the POR, BOD, and LVD specifications meet the safety requirements of the system.
Voltage Monitoring Overview

› Over-Voltage Detection (OVD)

Legend:
- Regulation
- 2.7 V to 5.5 V power line
- 2.7 V to 3.3 V power line
- 1.1 V power line
- Control line
- External power pad

Review datasheet and TRM section 16.3 for additional details
OVD Overview

- Detects supply conditions above a threshold and applies a reset to the device
- Always on except in Hibernate and XRES mode
  - OVD on VDDD
    - Generates a reset if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VDDA
    - Generates a reset, a fault, or no action (default) if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VCCD
    - Generates a reset if a voltage excursion dips above the rising trip point

Hint Bar

Review datasheet and TRM section 16.3.3 for additional details
Voltage Monitoring Overview

› Over-Current Detection (OCD)

[Diagram]

Legend:
- Regulators
- 2.7 V to 3.6 V power line
- 2.7 V to 5.5 V power line
- Enable control
- Reset or Fault
- Internal or Fault

Review datasheet and TRM section 16.3 for additional details.
OCD Overview

› Detects if the device current is over the regulator limit
› Always on except in Hibernate and XRES modes
   – OCD on VCCD
     – Generates a reset by detecting if the load current of a regulator is higher than expected
   – OCD is not available when using PMIC

Hint Bar

Review datasheet and TRM section 16.3.5 for additional details
# Summary of Voltage Monitoring

<table>
<thead>
<tr>
<th>Monitored Supply</th>
<th>Monitor</th>
<th>Trip Point</th>
<th>Output</th>
<th>Available Power Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DDD}$</td>
<td>POR</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td>All power modes</td>
</tr>
<tr>
<td></td>
<td>BOD</td>
<td>2 (Programmable)</td>
<td>Reset</td>
<td>All power modes except Hibernate and XRES modes</td>
</tr>
<tr>
<td></td>
<td>OVD</td>
<td>2 (Programmable)</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LVD</td>
<td>26 (Programmable)</td>
<td>Interrupt, Fault, or No action</td>
<td></td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>BOD</td>
<td>2 (Programmable)</td>
<td>Reset, Fault, or No action</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OVD</td>
<td>2 (Programmable)</td>
<td>Reset, Fault, or No action</td>
<td></td>
</tr>
<tr>
<td>$V_{CCD}$</td>
<td>BOD</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OVD</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OCD¹</td>
<td>1 (Fixed)</td>
<td>Reset</td>
<td></td>
</tr>
</tbody>
</table>
Voltage Monitoring by ADC

- ADC is used for all other power supplies
- A monitor switch is provided between power/ground pad and AMUXBUS_A/B by the HSIOM_MONITOR_CTL register
- Midpoint of the signal (AMUXBUS_A/B) is connected to the SARMUX (internal signals) and can be selected for ADC by a channel
- Use case
  - VDDIO monitoring

Review TRM section 16.3.7 for additional details.
Power Supply Monitoring by ADC

Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

<table>
<thead>
<tr>
<th>HSIOM_MONITOR_CTL_0</th>
<th>Power/Ground Pins</th>
<th>AMUXBUS</th>
<th>BGA-320</th>
<th>BGA-272 for CYT4BF</th>
<th>BGA-272 for CYT3BB/4BB</th>
<th>TEQFP-176</th>
<th>TEQFP-144</th>
<th>TEQFP-100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 0</td>
<td>V&lt;sub&gt;PPP&lt;/sub&gt;</td>
<td>A</td>
<td>F8, F9, H15, J15, K15, L15, M15, N15, R12, R13</td>
<td>F8, H13, J13, K13, L13, N11</td>
<td>F8, H13, J13, K13, L13, N11</td>
<td>176</td>
<td>144</td>
<td>100</td>
</tr>
<tr>
<td>Bit 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>22</td>
<td>18</td>
<td>12</td>
</tr>
<tr>
<td>Bit 4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>43</td>
<td>35</td>
<td>24</td>
</tr>
<tr>
<td>Bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110</td>
<td>90</td>
<td>62</td>
</tr>
<tr>
<td>Bit 15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>132</td>
<td>108</td>
<td>75</td>
</tr>
<tr>
<td>Bit 17</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>153</td>
<td>124</td>
<td>86</td>
</tr>
<tr>
<td>Bit 1</td>
<td>V&lt;sub&gt;SSS&lt;/sub&gt;</td>
<td>B</td>
<td>A1, A20, C3, C10, C18, H9, H10, H11, H12, H13, J9, J10, J11, J12, J13, J18, K9, K10, K11, K12, K13, K18, L9, L10, L11, L12, L13, M9, M10, M11, M12, M13, N12, V3, V4, V15, Y1, Y20</td>
<td>A1, A18, D9, G7, G12, H9, H10, H11, J9, J10, J11, J15, K9, K10, K11, K12, K13, M7, M12, R5, R14, V1, V18</td>
<td>A1, A18, D9, G7, G12, H9, H10, H11, J9, J10, J11, J15, K9, K10, K11, M7, M12, R5, R14, V1, V18</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Bit 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>23</td>
<td>19</td>
<td>13</td>
</tr>
<tr>
<td>Bit 6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>45</td>
<td>37</td>
<td>26</td>
</tr>
<tr>
<td>Bit 12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>46</td>
<td>73</td>
<td>51</td>
</tr>
<tr>
<td>Bit 14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>89</td>
<td>94</td>
<td>66</td>
</tr>
<tr>
<td>Bit 16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111</td>
<td>109</td>
<td>76</td>
</tr>
<tr>
<td>Bit 19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>133</td>
<td>126</td>
<td>88</td>
</tr>
</tbody>
</table>

Review TRM sections 16.3.6 and 30.10 for additional details.
## Power Supply Monitoring by ADC

### Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

<table>
<thead>
<tr>
<th>HSIOM_MONITOR_CTL_0</th>
<th>Power/Ground Pins</th>
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<th>TEQFP-144</th>
<th>TEQFP-100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 5</td>
<td>V_{DDIO_1}</td>
<td>A</td>
<td>F10, F11, F12, F13</td>
<td>F9, F10, F11</td>
<td>F9, F10, F11</td>
<td>44</td>
<td>36</td>
<td>25</td>
</tr>
<tr>
<td>Bit 18</td>
<td>V_{SSD_1} (BGA)</td>
<td>B</td>
<td>N13</td>
<td>L11</td>
<td>L11</td>
<td>154</td>
<td>125</td>
<td>87</td>
</tr>
<tr>
<td>Bit 7</td>
<td>V_{REFL}</td>
<td>B</td>
<td>M8</td>
<td>K8</td>
<td>K8</td>
<td>76</td>
<td>62</td>
<td>41</td>
</tr>
<tr>
<td>Bit 8</td>
<td>V_{SSA}</td>
<td>B</td>
<td>N8</td>
<td>L8</td>
<td>L8</td>
<td>77</td>
<td>63</td>
<td>42</td>
</tr>
<tr>
<td>Bit 9</td>
<td>V_{DDA}</td>
<td>A</td>
<td>N6</td>
<td>L6</td>
<td>L6</td>
<td>78</td>
<td>64</td>
<td>43</td>
</tr>
<tr>
<td>Bit 10</td>
<td>V_{REFH}</td>
<td>A</td>
<td>M6</td>
<td>K6</td>
<td>K6</td>
<td>79</td>
<td>65</td>
<td>44</td>
</tr>
<tr>
<td>Bit 11</td>
<td>V_{DDIO_2}</td>
<td>A</td>
<td>R8</td>
<td>N8</td>
<td>N8</td>
<td>88</td>
<td>72</td>
<td>50</td>
</tr>
<tr>
<td>Bit 20</td>
<td>V_{DDIO_3}</td>
<td>A</td>
<td>H6, J6, K6, L6</td>
<td>H6, J6</td>
<td>H6, J6</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Bit 21</td>
<td>V_{SSIO_3}</td>
<td>B</td>
<td>H8, J8, K8, L8</td>
<td>H8, J8</td>
<td>H8, J8</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Bit 22</td>
<td>V_{DDIO_4}</td>
<td>A</td>
<td>R9, R10, R11</td>
<td>N9, N10</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Bit 24</td>
<td>V_{DDIO_4}</td>
<td>A</td>
<td>R9, R10, R11</td>
<td>N9, N10</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Bit 25</td>
<td>V_{SSIO_4}</td>
<td>B</td>
<td>N9, N10, N11</td>
<td>L9, L10</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Bit 5</td>
<td>V_{DDIO_1}</td>
<td>A</td>
<td>F10, F11, F12, F13</td>
<td>F9, F10, F11</td>
<td>F9, F10, F11</td>
<td>44</td>
<td>36</td>
<td>25</td>
</tr>
<tr>
<td>Bit 18</td>
<td>V_{SSD_1} (BGA)</td>
<td>B</td>
<td>N13</td>
<td>L11</td>
<td>L11</td>
<td>154</td>
<td>125</td>
<td>87</td>
</tr>
</tbody>
</table>

**Hint Bar**

Review TRM sections 16.3.6 and 30.10 for additional details.
Appendix
Comparison between CYT2B, CYT3B/4B, and CYT3D/4D

- Maximum number of system interrupts and wakeup interrupts varies by device.

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2B</th>
<th>CYT3B/4B</th>
<th>CYT3D/4D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply and Monitoring</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply</td>
<td>$V_{DD} = 2.7$ V to 5.5 V, $V_{DD} = 2.7$ V to 5.5 V (up to 300 mA)</td>
<td>$V_{DD} = 2.7$ V to 5.5 V and $V_{CCG} = 1.15$ V (exceeds 300 mA)</td>
<td></td>
</tr>
<tr>
<td>5.0 V I/O power supply</td>
<td>$V_{DDIO_1}$, $V_{DDIO_2}$</td>
<td>$V_{DDIO.GPIO}$, $V_{DDIO.SMC}$</td>
<td></td>
</tr>
<tr>
<td>3.3 V I/O power supply</td>
<td>N/A</td>
<td>$V_{DDIO.GPIO}$</td>
<td>$V_{DDIO.GPIO}$</td>
</tr>
<tr>
<td>1.8 V I/O power supply</td>
<td>N/A</td>
<td>$V_{DDIO.GPIO}$</td>
<td></td>
</tr>
<tr>
<td>Analog power supply</td>
<td>$V_{DDA}$</td>
<td>$V_{DDA_ADC}$, $V_{DDA_DAC}$, $V_{DDA_MIPI}$, $V_{DDA_FPD0}$</td>
<td>$V_{DDA_FPD0}$, $V_{DDA_FPD1}$, $V_{DDPLL_FPD0}$, $V_{DDPLL_FPD1}$</td>
</tr>
<tr>
<td>Active/DeepSleep regulator</td>
<td>Same</td>
<td></td>
<td></td>
</tr>
<tr>
<td>External transistor control</td>
<td>N/A</td>
<td>Available</td>
<td>N/A</td>
</tr>
<tr>
<td>External PMIC control</td>
<td>N/A</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>POR/BOD/OVD/LVD</td>
<td></td>
<td></td>
<td>Same</td>
</tr>
</tbody>
</table>
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## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>6402061</td>
<td>03/12/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>7053306</td>
<td>12/14/2020</td>
<td>Updated page 2, 3, 6, 8 to 11, 28, 29, 31.</td>
</tr>
</tbody>
</table>