Customer Training Workshop

Traveo™ II Body Controller High Power Supply and Monitoring

Q4 2020

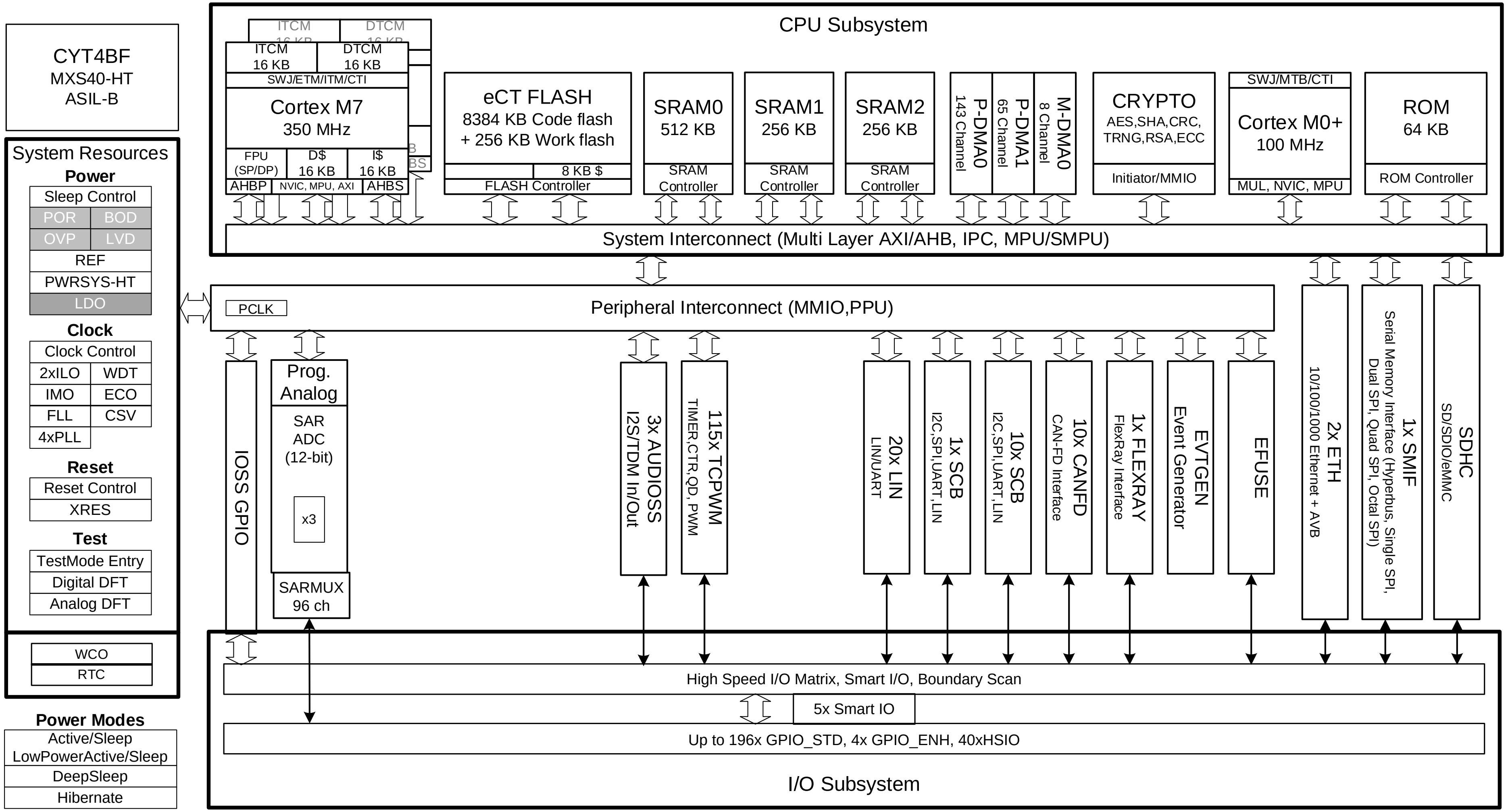
Target Products

- Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller High	CYT3BB/4BB	Up to 4160 KB
Traveo™ II Automotive Body Controller High	CYT4BF	Up to 8384KB

Introduction

› Power supply monitoring functions are in System Resources



Hint Bar

Review TRM section 16.2 for additional details

Power-on reset (POR)

Brownout detection (BOD)

Over-voltage detection (OVD)

Low-voltage detection (LVD)

Low drop-out regulator (LDO)

Power Supply Overview

- 2.7 to 5.5-V power supply range
- Core regulators for High Current, Active, and DeepSleep modes

Digital power supply

External high-current regulator controller with load current up to 600 mA

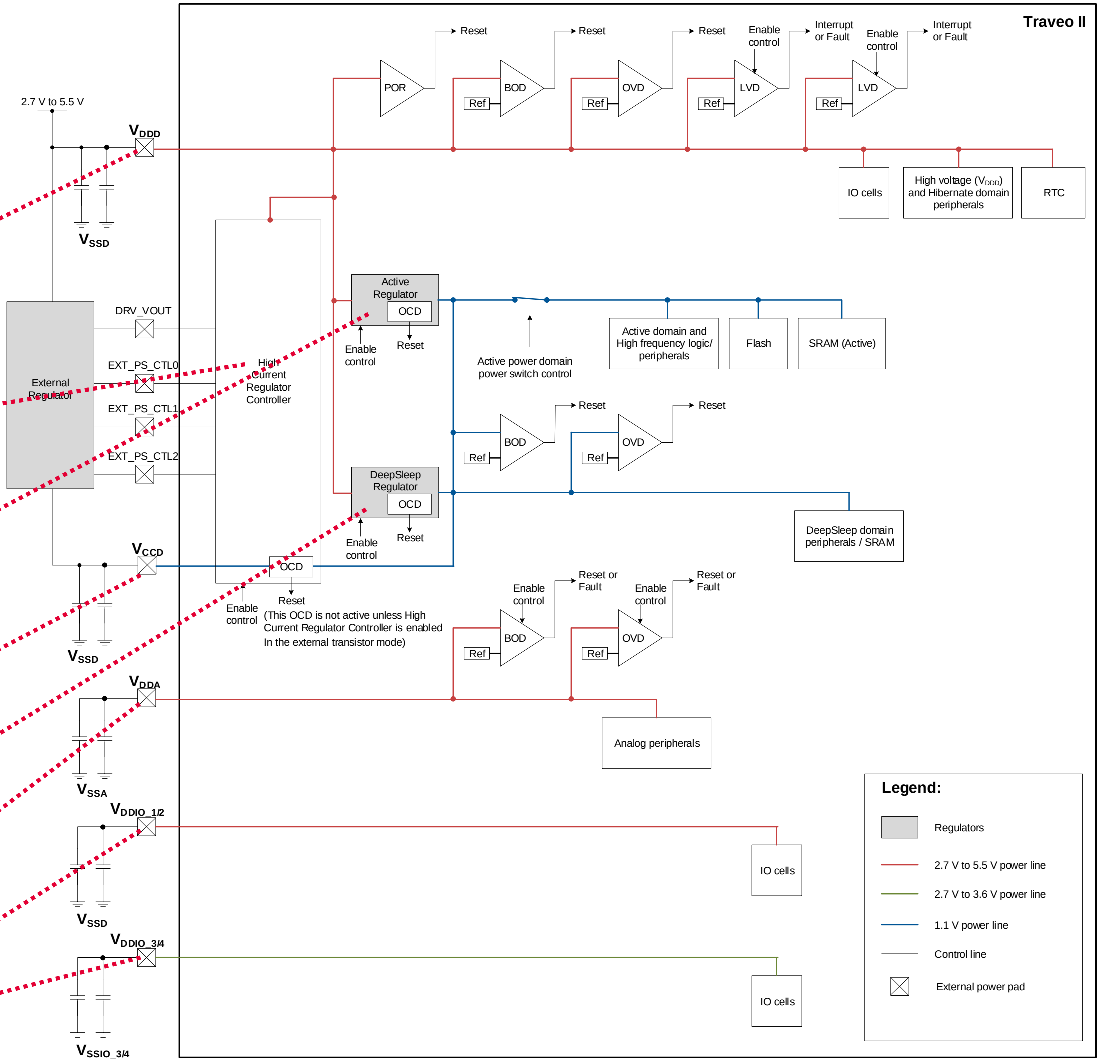
Internal logic supply for device startup (boot process) and for applications with load current up to 300 mA

Core power supply

Internal logic power supply for DeepSleep mode

Analog power supply

I/O power supply



Hint Bar

Review TRM section 16.2 for additional details

VDDD/VSSD:
Digital power supply/ ground

VDDIO_1/2/VSSD:
I/O power supply/ ground

VDDIO_3/4/VSSIO_3/4:
I/O power supply/ ground

VDDA/VSSA:
Analog power supply/ ground

VCCD/VSSD:
Internal core supply/ ground

Power Pins and Rails

› Power/ground pins and voltage range

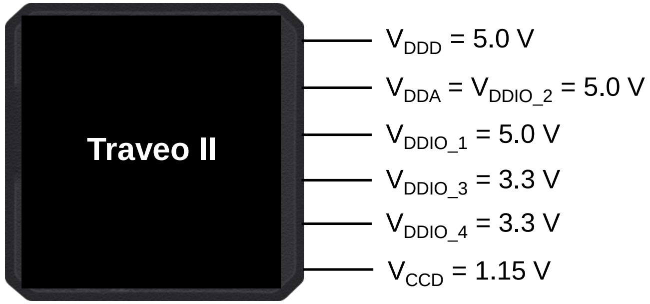
Supply Pin	Ground Pin	Power Supply Voltage Range	Description
V_{DDD}	V_{SSD}	2.7 V to 5.5 V	Digital and I/O supply
V_{CCD}	V_{SSD}	1.1 V to 1.2 V	Core supply
V_{DDA}	V_{SSA}	2.7 V to 5.5 V	Analog supply, $V_{DDA} = V_{DDIO\_2}$
V_{DDIO_1}	V_{SSD}	2.7 V to 5.5 V	I/O supply
V_{DDIO_2}	V_{SSD}	2.7 V to 5.5 V	I/O supply
V_{DDIO_3}	V_{SSIO_3}	2.7 V to 3.6 V	I/O supply
V_{DDIO_4}	V_{SSIO_4}	2.7 V to 3.6 V	I/O supply

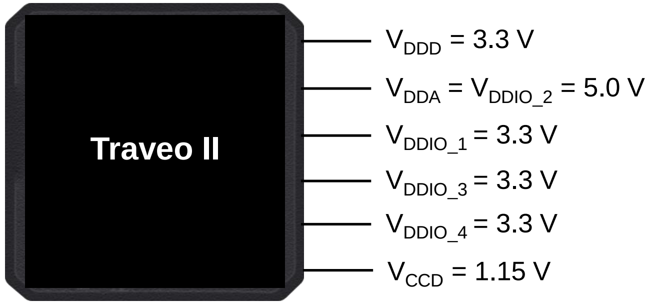
Hint Bar

Review TRM section 16.2.2 for additional details

Power Supply

- Power supply sources
  - VDDD, VDDIO_1, VDDIO_3, and VDDIO_4 supplies are independent
  - VDDA1 and VDDIO_2 must be the same





- Power sequencing requirements
  - VDDD, VDDIO_1, VDDIO_3, and VDDIO_4 have no sequencing limitations
  - VDDA = VDDIO_2
- Advantage
  - Less effort and cost because no external power sequencing control is required for applications with load current up to 300 mA

Hint Bar

Review the datasheet

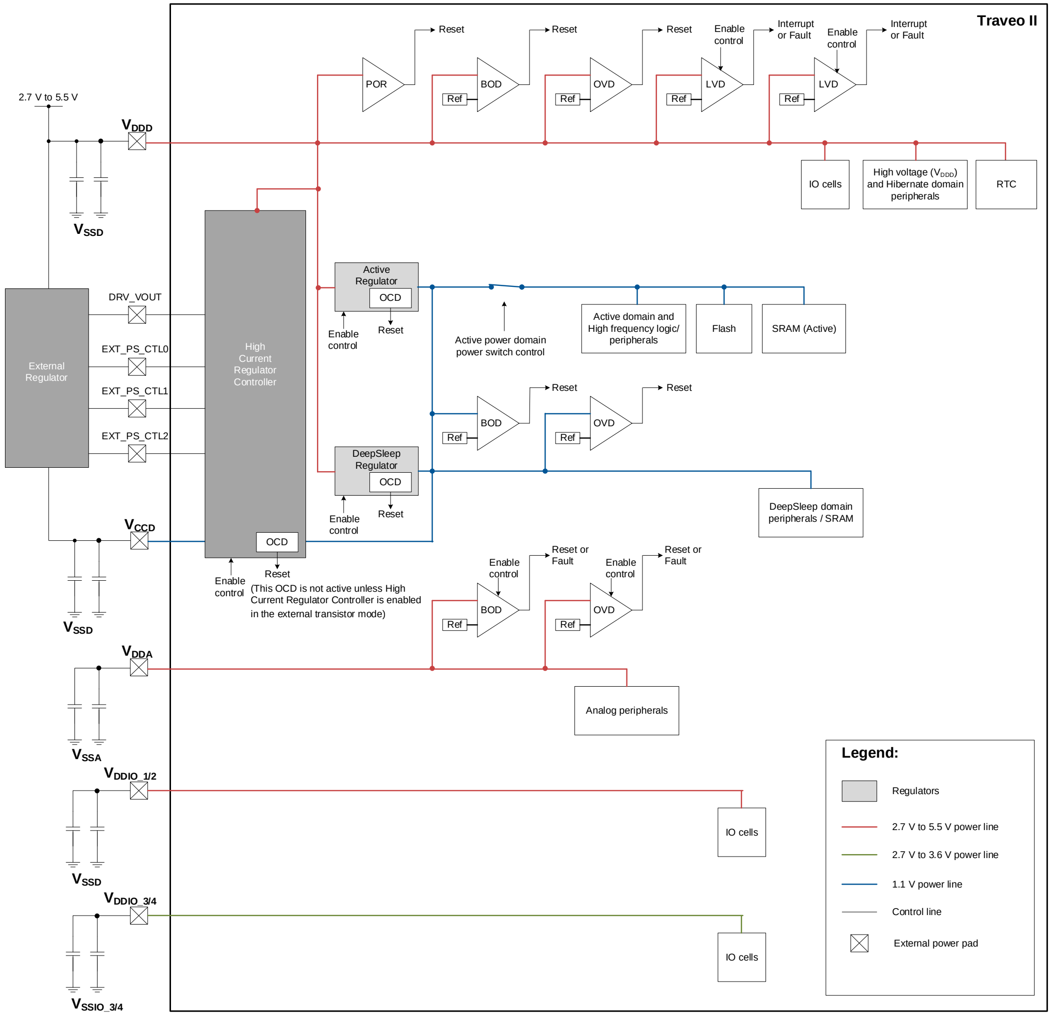
- Recommended Operating Conditions

- 12-Bit SAR ADC DC Specifications when using ADC units

Review TRM sections 16.2.3 and 16.2.4 for additional details

Regulator Selection

- High-current regulator selection
  - Device starts up with Active regulator, which supports up to 300 mA supply current
  - Switches to high-current regulator if supply current of up to 600 mA is required
- Two types of external regulator configuration
  - External transistor
  - PMIC/LDO

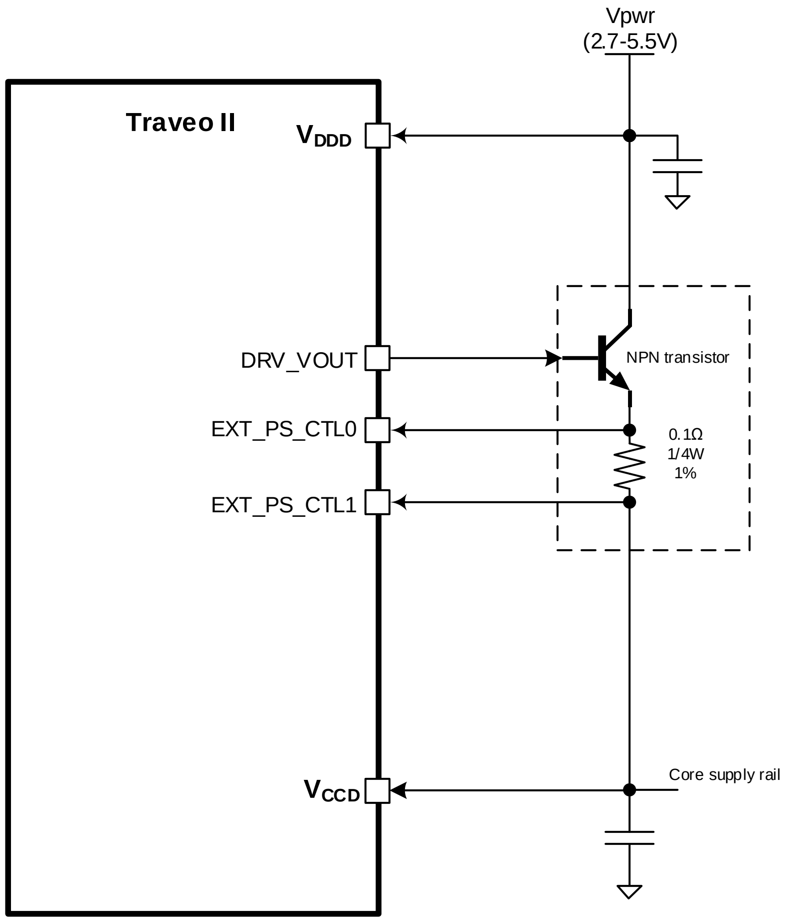


Hint Bar

Review datasheet and TRM section 16.2.5 for additional details

External Regulator:
External Transistor Configuration (Hardware)

- Sensing with the resistor controls the transistor and adjusts the supply voltage (VCCD)
  - DRV_VOUT: Dedicated external supply control pin
  - EXT_PS_CTL0: Sense input plus
  - EXT_PS_CTL1: Sense input minus

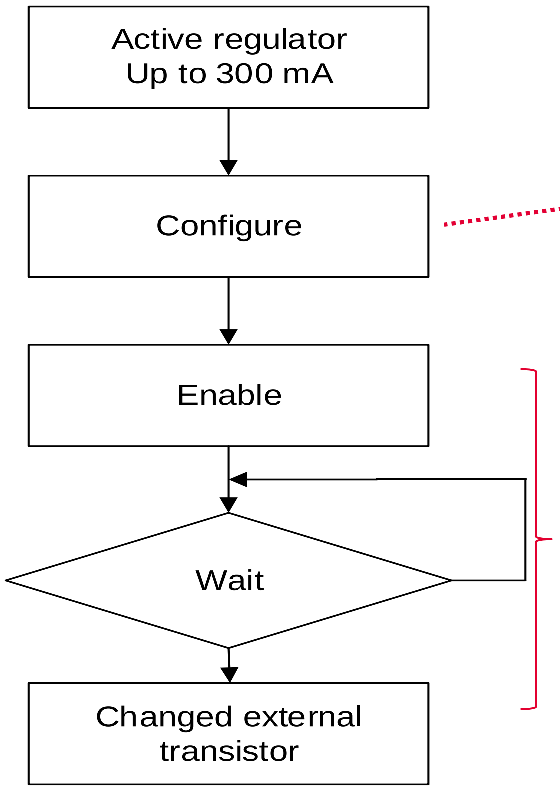


Hint Bar

Review datasheet and TRM section 16.2.5 for additional details

External Regulator:
External Transistor Configuration (Software)

- Changing from Active regulator to high-current regulator controller with external transistor
  - Setup flow



Call ConfigureRegulator API:

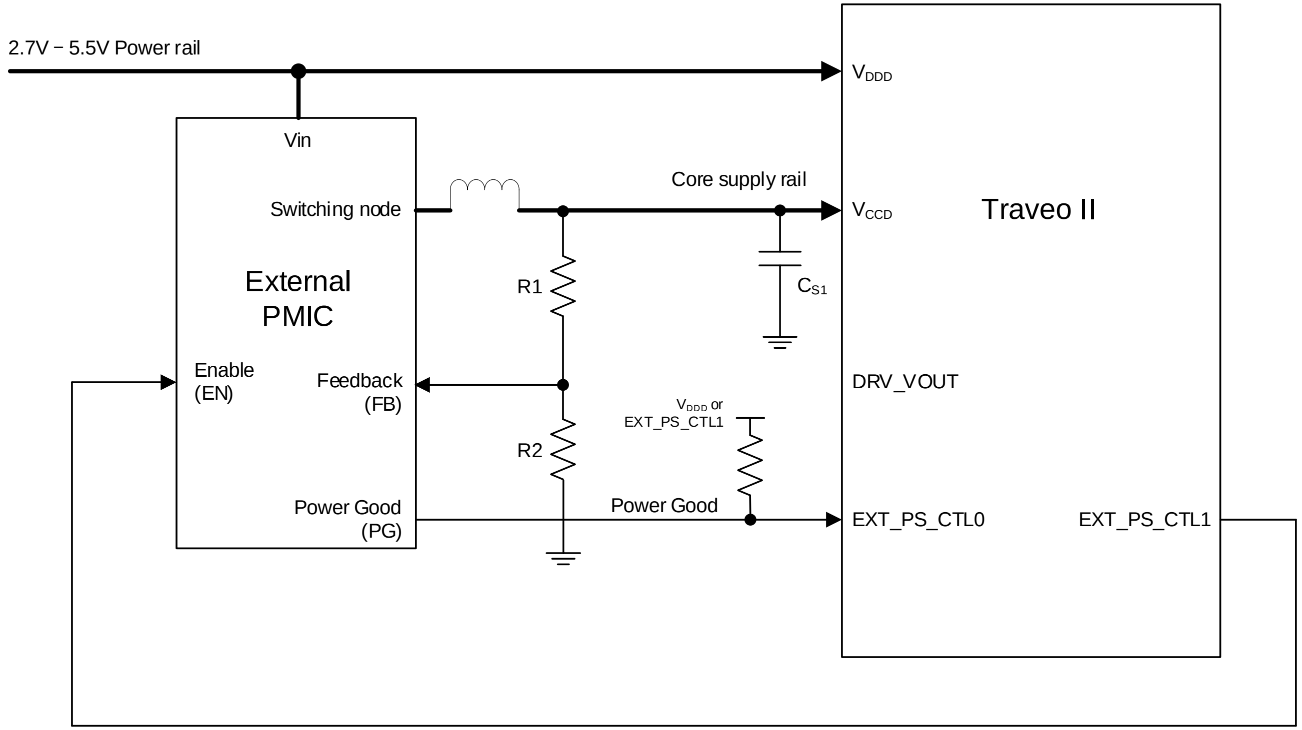
- PWR_REGHC_CTL.REGHC_MODE = 0 (Select external transistor mode)
- PWR_REGHC_CTL.REGHC_TRANS_USE_OCD = 1
- PWR_REGHC_CTL.REGHC_CONFIGURED = 1

Call SwitchOverRegulators API:

- PWR_REGHC_CTL2.REGHC_EN = 1
- Wait until PWR_REGHC_STATUS.SEQ_BUSY == 0 and PWR_REGHC_STATUS.REGHC_ENABLED == 1
- This should occur within 15 µs

External Regulator: PMIC Configuration (Hardware)

- High-current regulator controller provides adjustable reference and reset
  - EXT_PS_CTL0: Power good input from PMIC
  - EXT_PS_CTL1: Enable output for PMIC
  - EXT_PS_CTL2: Reset threshold adjustment for some PMIC (RADJ-pin[1])



[1] RADJ is optional and may not be present depending on the PMIC used

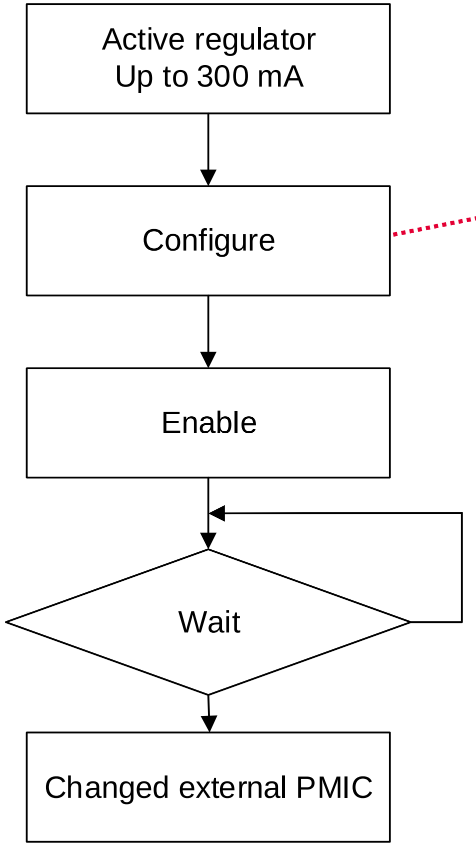
Hint Bar

Review datasheet and TRM section 16.2.5 for additional details

Recommended PMICs: Cypress S6BP501A and Rohm BD9S200MUF-C

External Regulator: PMIC Configuration (Software)

- Changing from active regulator to high-current regulator controller with external PMIC
  - Setup flow



Call ConfigureRegulator API:

- PWR_REGHC_CTL.REGHC_MODE = 1 (PMIC mode)
- PWR_REGHC_CTL.REGHC_PMIC_STATUS_INEN = 1 to enable the input path for PMIC status
- PWR_REGHC_CTL.REGHC_PMIC_STATUS_POLARITY to the setting that indicates an error condition (depending on the polarity of the PMIC status output)
- PWR_REGHC_CTL.REGHC_PMIC_CTL_OUTEN = 1 and PWR_REGHC_CTL.REGHC_PMIC_CTL_POLARITY to the setting that enables the PMIC (depending on polarity of PMIC enable input)
- PWR_REGHC_CTL.REGHC_VADJ to the required feedback setting for the chosen PMIC

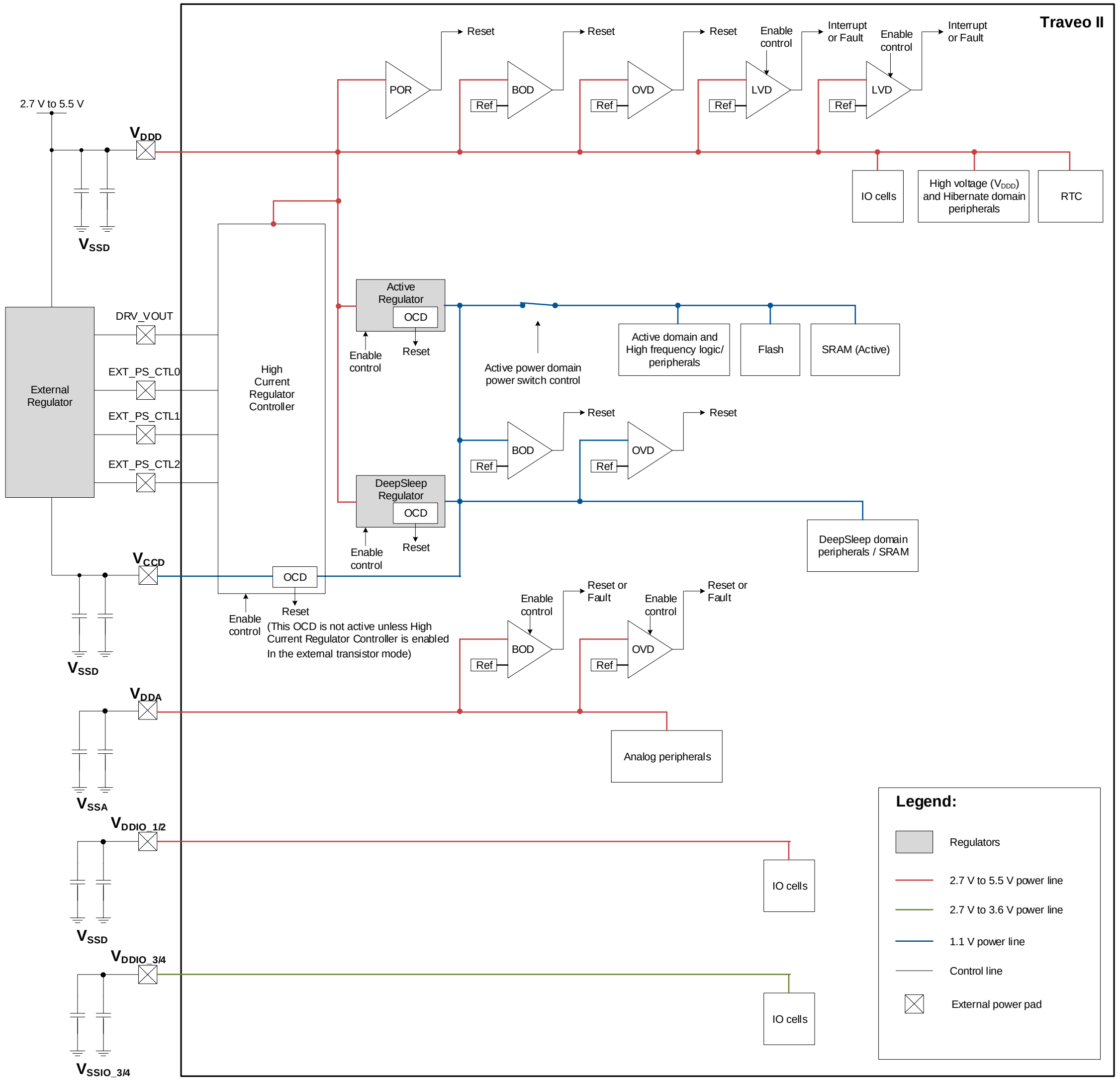
Call SwitchOverRegulators API:

- PWR_REGHC_CTL2.REGHC_EN = 1
- Wait until PWR_REGHC_STATUS.SEQ_BUSY == 0 and PWR_REGHC_STATUS.REGHC_ENABLED == 1

This delay depends strongly on the startup time of the PMIC, based on its status output and the value in PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT

Voltage Monitoring Overview

› Supports multiple voltage monitoring and supply failure protection



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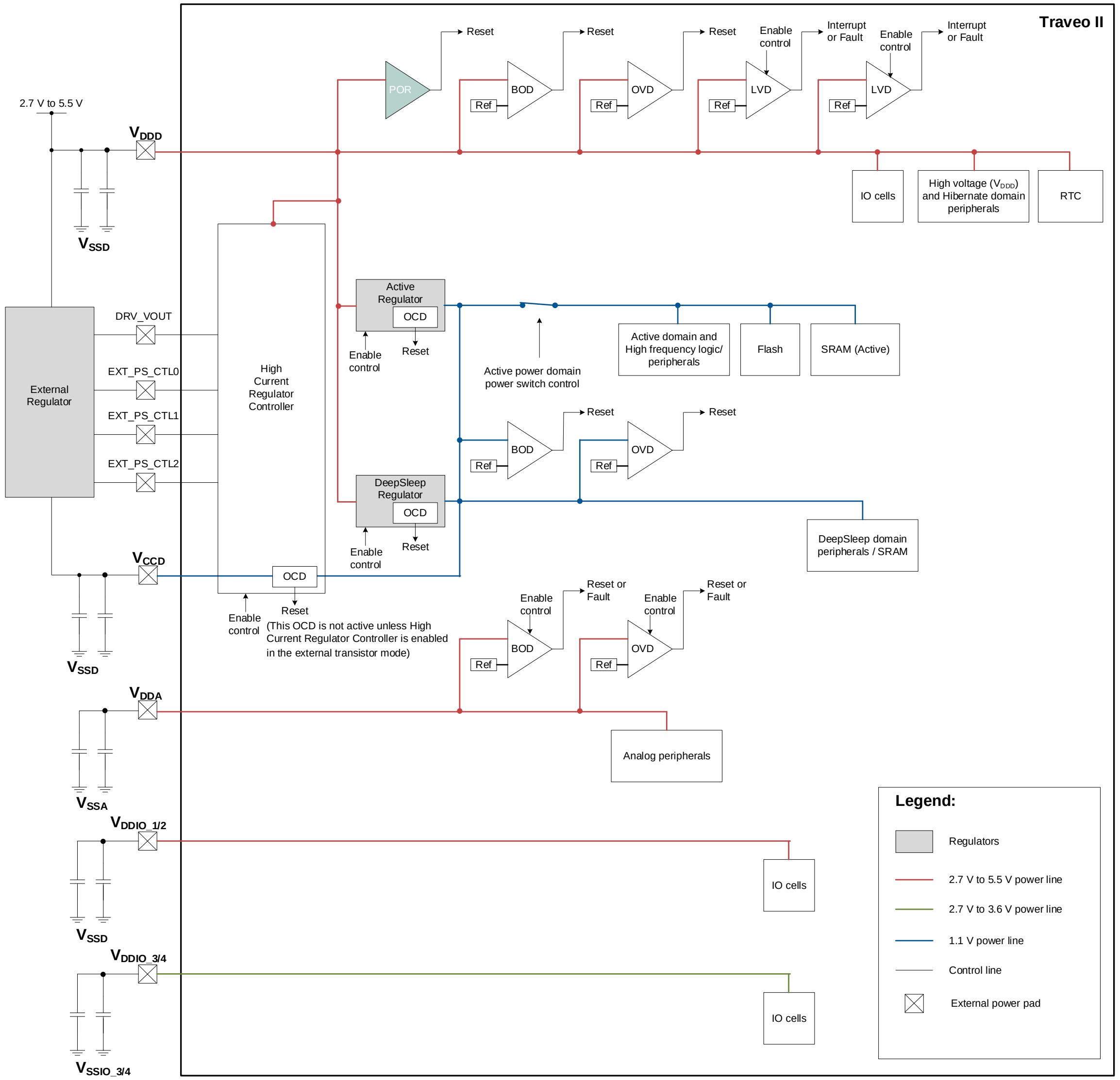
Review datasheet and TRM section 16.3 for additional details.

Voltage Monitoring Overview

› **Power-On Reset (POR)**

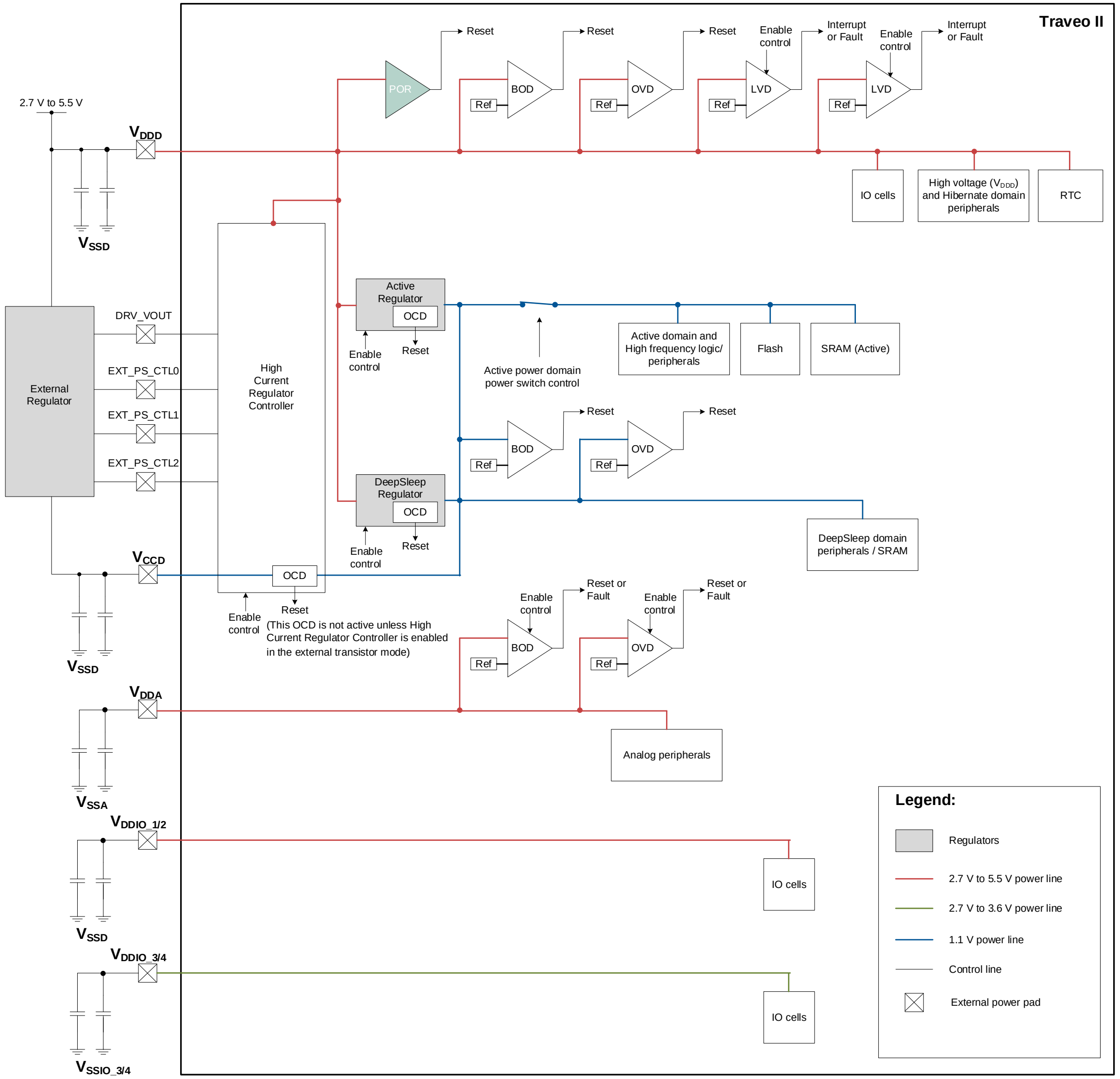


Hint Bar

Review datasheet and TRM section 16.3 for additional details

Power-On Reset (POR)

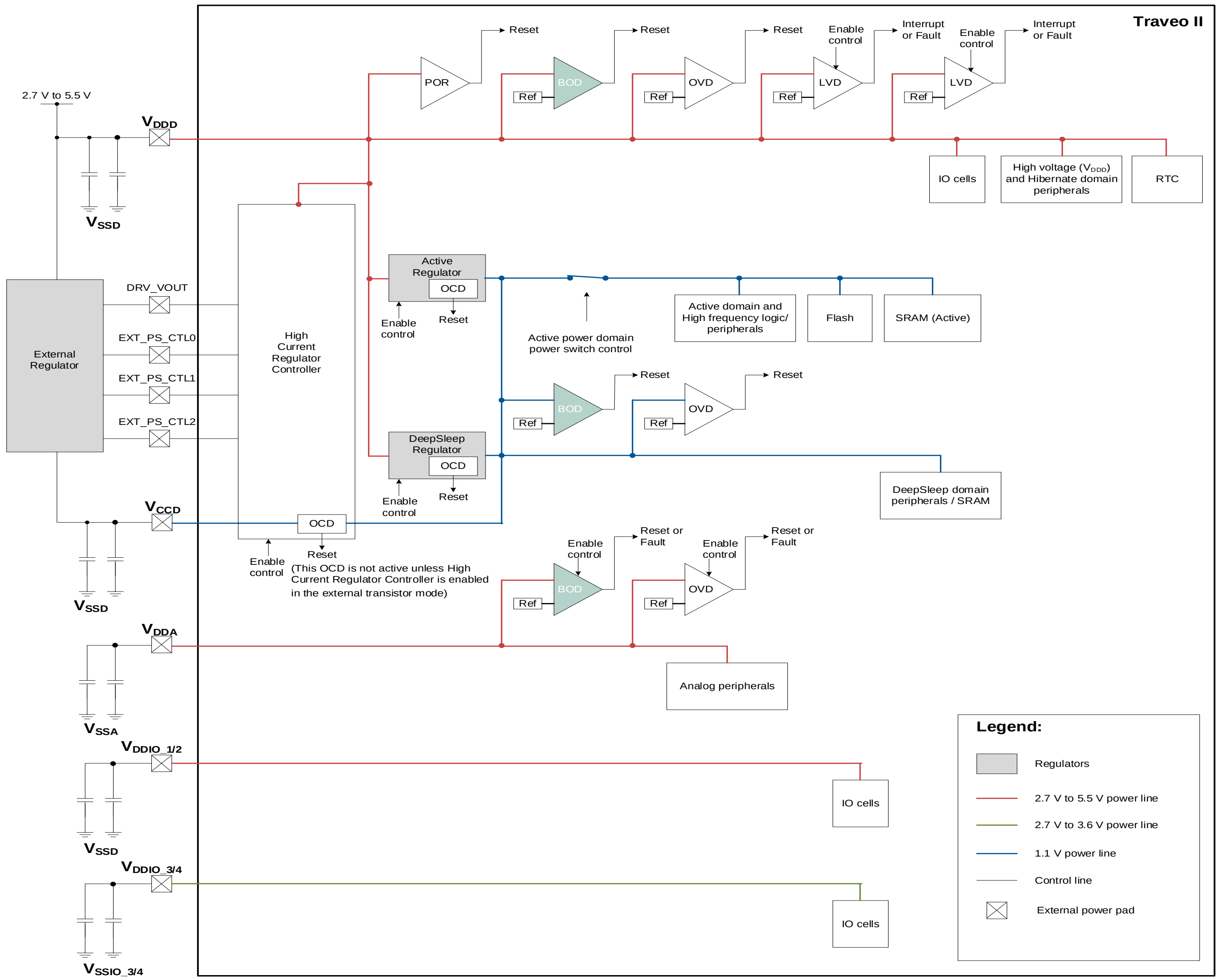
- Initializes the device at power-up
- Always on
  - POR on VDDD
    - Provide a reset pulse during the initial power ramp



Hint Bar

Review datasheet and TRM section 16.3.1 for additional details

Brown-out Detection (BOD)

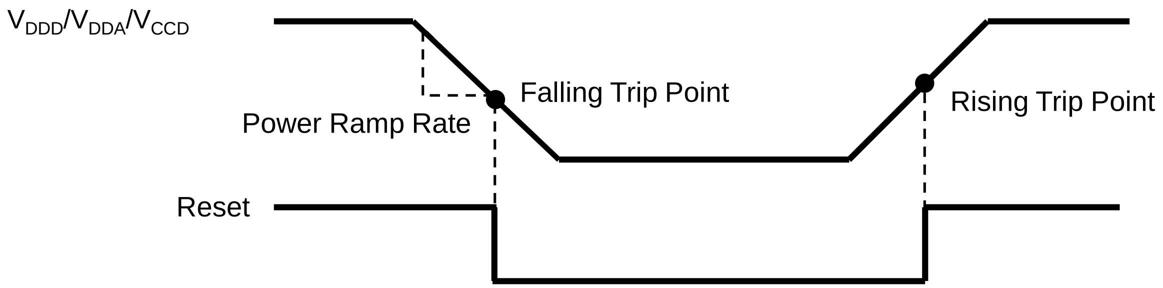


Hint Bar

Review datasheet and TRM section 16.3 for additional details

BOD Overview

- Detects supply condition below a threshold and applies a reset to the device
- Always on except in Hibernate and XRES modes
  - BOD on VDDD
    - Generates a reset if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V[1] (default) or < 3.0 V
  - BOD on VDDA
    - Generates a reset, a fault, or no action[2] (default) if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V[1] (default) or < 3.0 V
  - BOD on VCCD
    - Generates a reset if a voltage excursion dips below the falling trip point

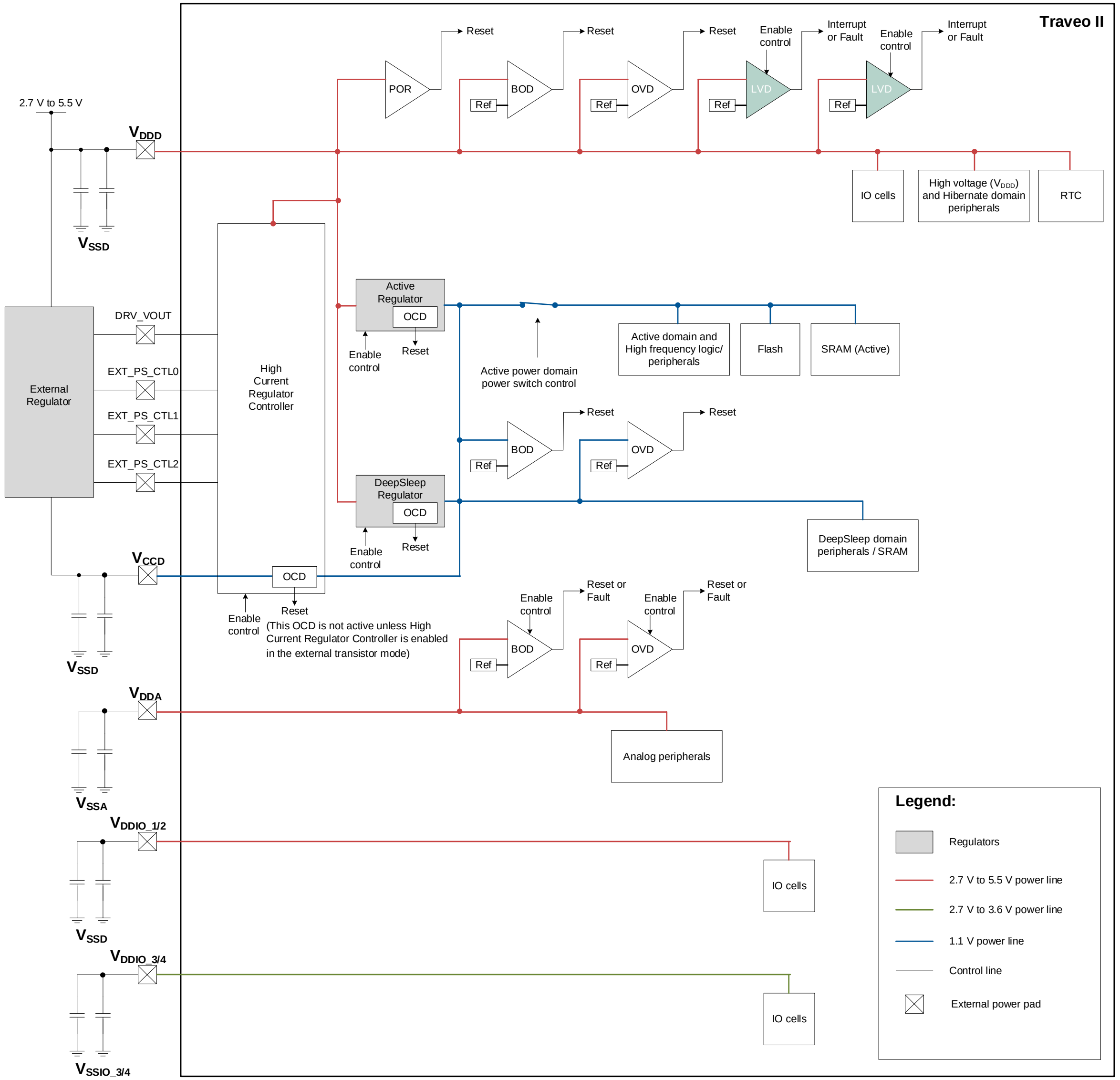


[1] If V_{DDD}/V_{DDA} falls below 2.7 V (minimum V_{DDD}/V_{DDA}), the device will operate out of specification. To prevent that, use the 3.0-V trip point
[2] Even if V_{DDA} is low, the MCU can boot because it does not generate a reset as default

Hint Bar

Review datasheet and TRM section 16.3.1 for additional details

Low-Voltage Detection (LVD)

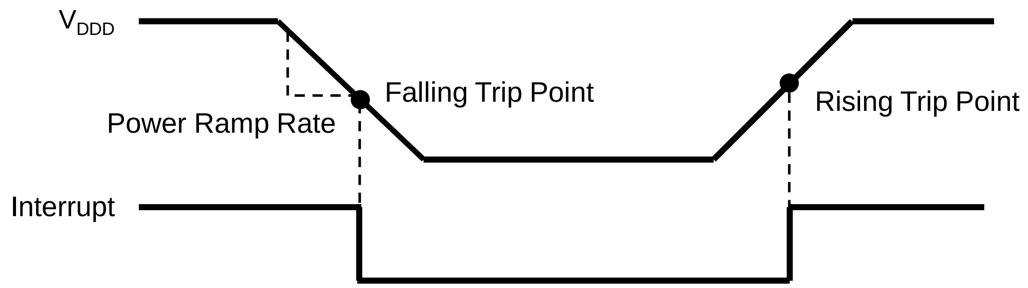


Hint Bar

Review datasheet and TRM section 16.3 for additional details

LVD Overview

- Detects the warning voltage level to take preventive measures in the system
- Can be enabled or disabled (default) by software, except in Hibernate and XRES mode
- LVD on VDDD
  - Generates an interrupt or a fault if a voltage level meets the trip point
    - An interrupt or a fault and trip point are configurable by software
  - Supports up to 26 trip points to monitor between 2.8 V and 5.3 V (0.1-V step)
  - Can be configured as falling (low voltage), rising (high voltage), or both detection
- Use case for two LVD units
  - LVD1: Use the falling trip point (3.5 V) to detect the low-voltage warning
  - LVD2: Use the rising trip (5.3 V) to detect the over-voltage warning

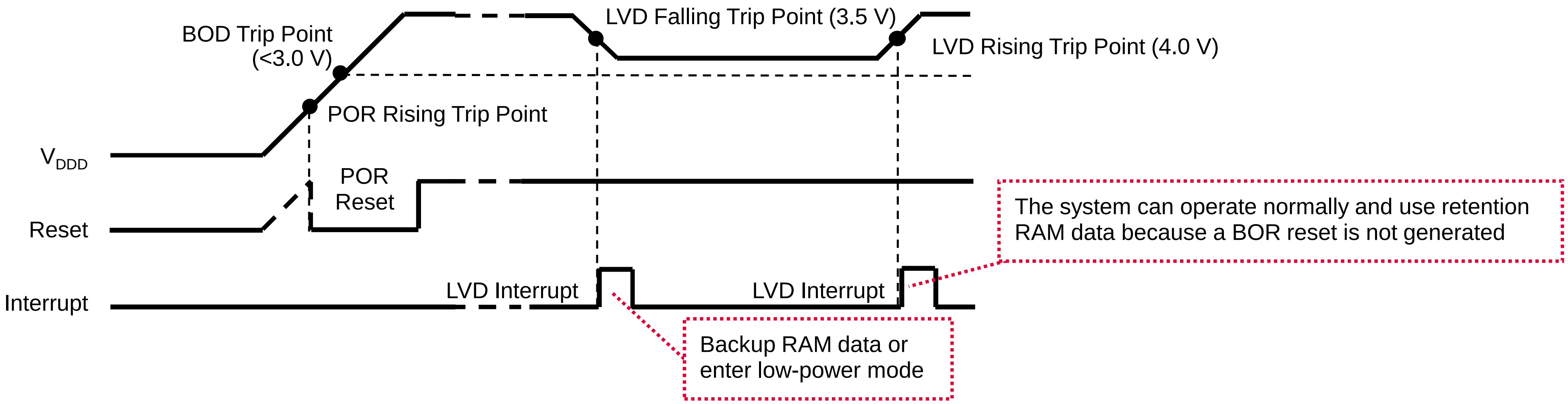


Hint Bar

Review datasheet and TRM section 16.3.4 for additional details

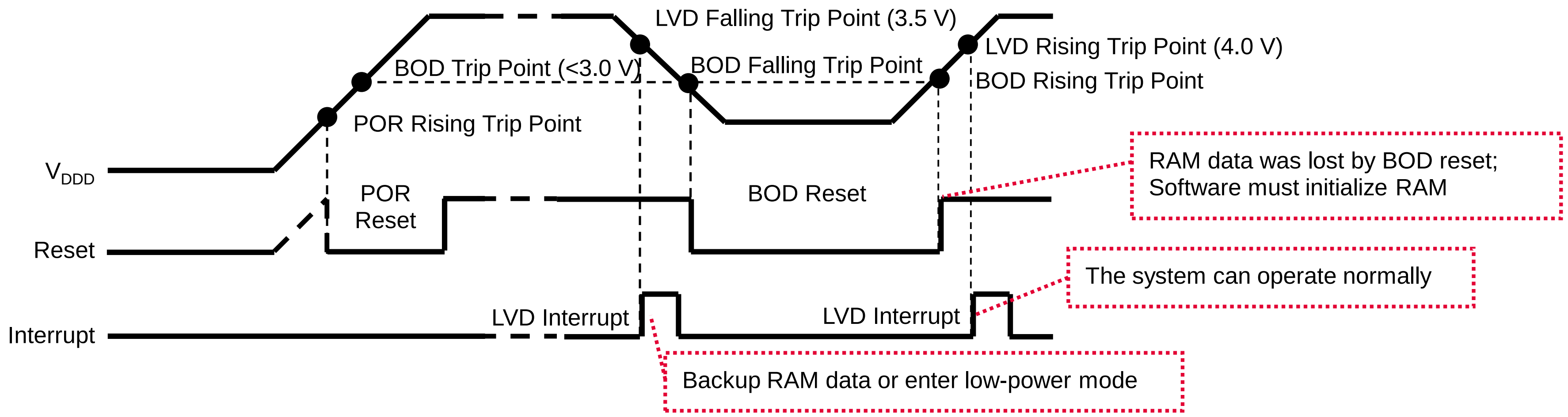
POR, BOD, and LVD Use Cases (1/2)

- Purpose: Judge whether RAM contents have been retained by using voltage monitoring
- Setting and condition
  - MCU operation conditions:
    - LVD trip point can be in MCU operation range − RAM retention
    - LVD falling trip point (3.5 V): Warning LVD for safety system operation
    - LVD rising trip point (4.0 V): User program restart trigger
  - BOD reset (<3.0 V) is an asynchronous reset − No RAM retention
- Use Case: For RAM, contents are retained (no BOD reset generation)



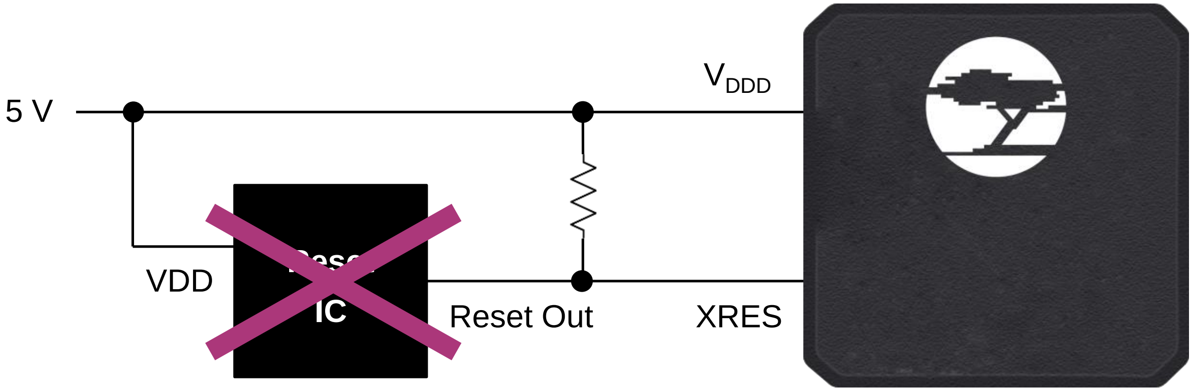
POR, BOD, and LVD Use Cases (2/2)

- Purpose: Judge whether RAM contents have been retained by using voltage monitoring
- Setting and condition
  - MCU operation conditions:
    - LVD trip point can be in MCU operation range − RAM retention
    - LVD falling trip point (3.5 V): Warning LVD for safety system operation
    - LVD rising trip point (4.0 V): User program restart trigger
- BOD reset (<3.0 V) is an asynchronous reset − No RAM retention
- Use Case: For RAM, contents have not been retained (BOD reset generation)



Advantage for POR, BOD, and LVD

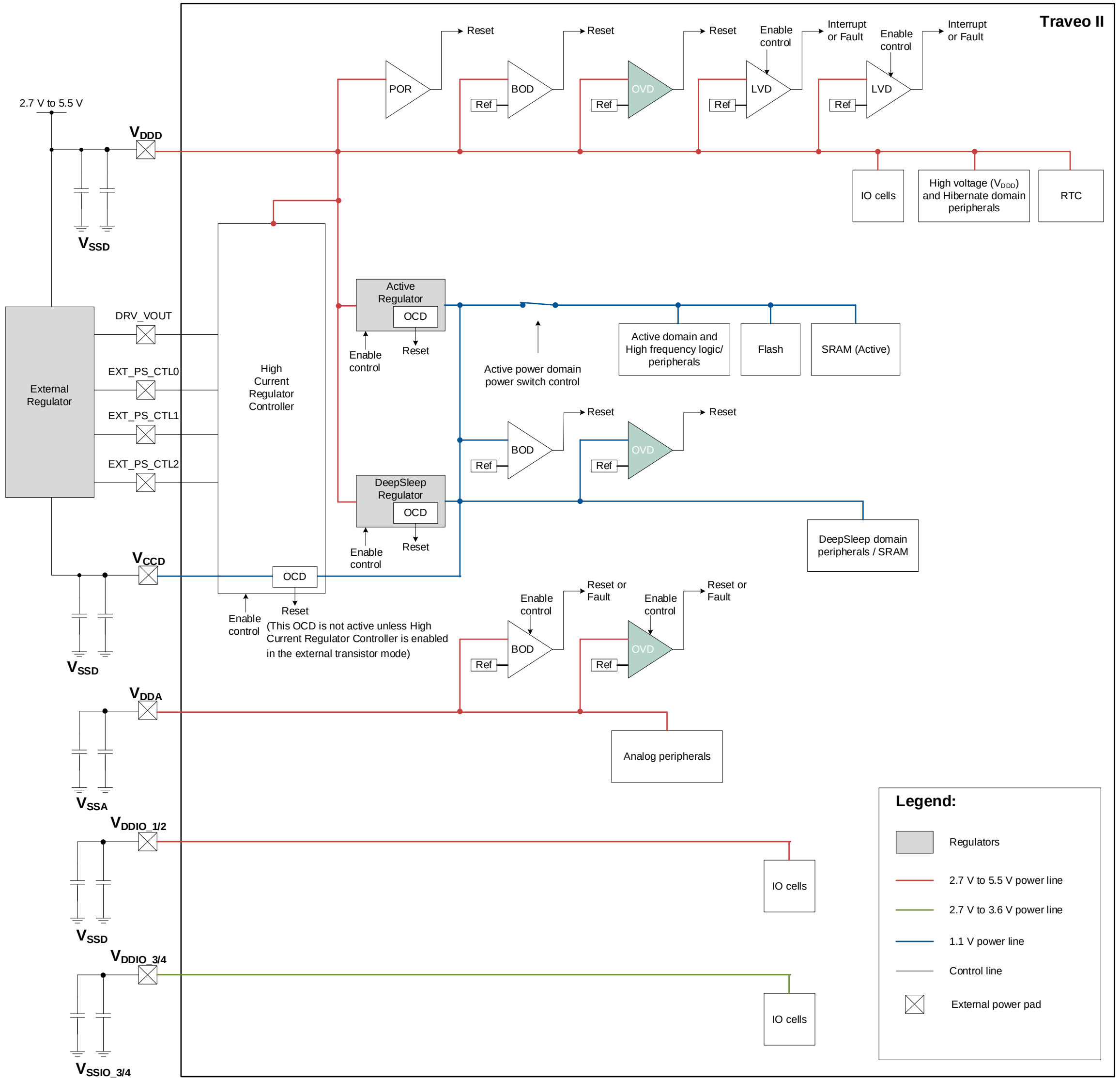
› Reduced BOM costs for low-cost applications using internal POR, BOD, and LVD[1]



[1] Review TRM and datasheet to confirm if the POR, BOD, and LVD specifications meet the safety requirements of the system

Voltage Monitoring Overview

› Over-Voltage Detection (OVD)

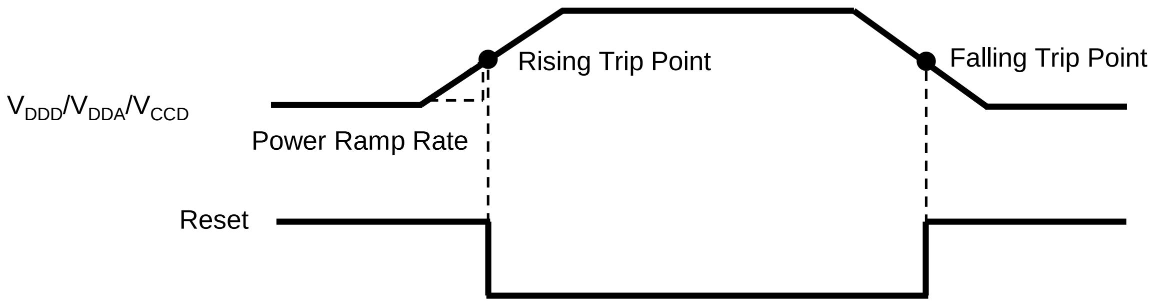


Hint Bar

Review datasheet and TRM section 16.3 for additional details

OVD Overview

- Detects supply conditions above a threshold and applies a reset to the device
- Always on except in Hibernate and XRES mode
  - OVD on VDDD
    - Generates a reset if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VDDA
    - Generates a reset, a fault, or no action (default) if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on VCCD
    - Generates a reset if a voltage excursion dips above the rising trip point

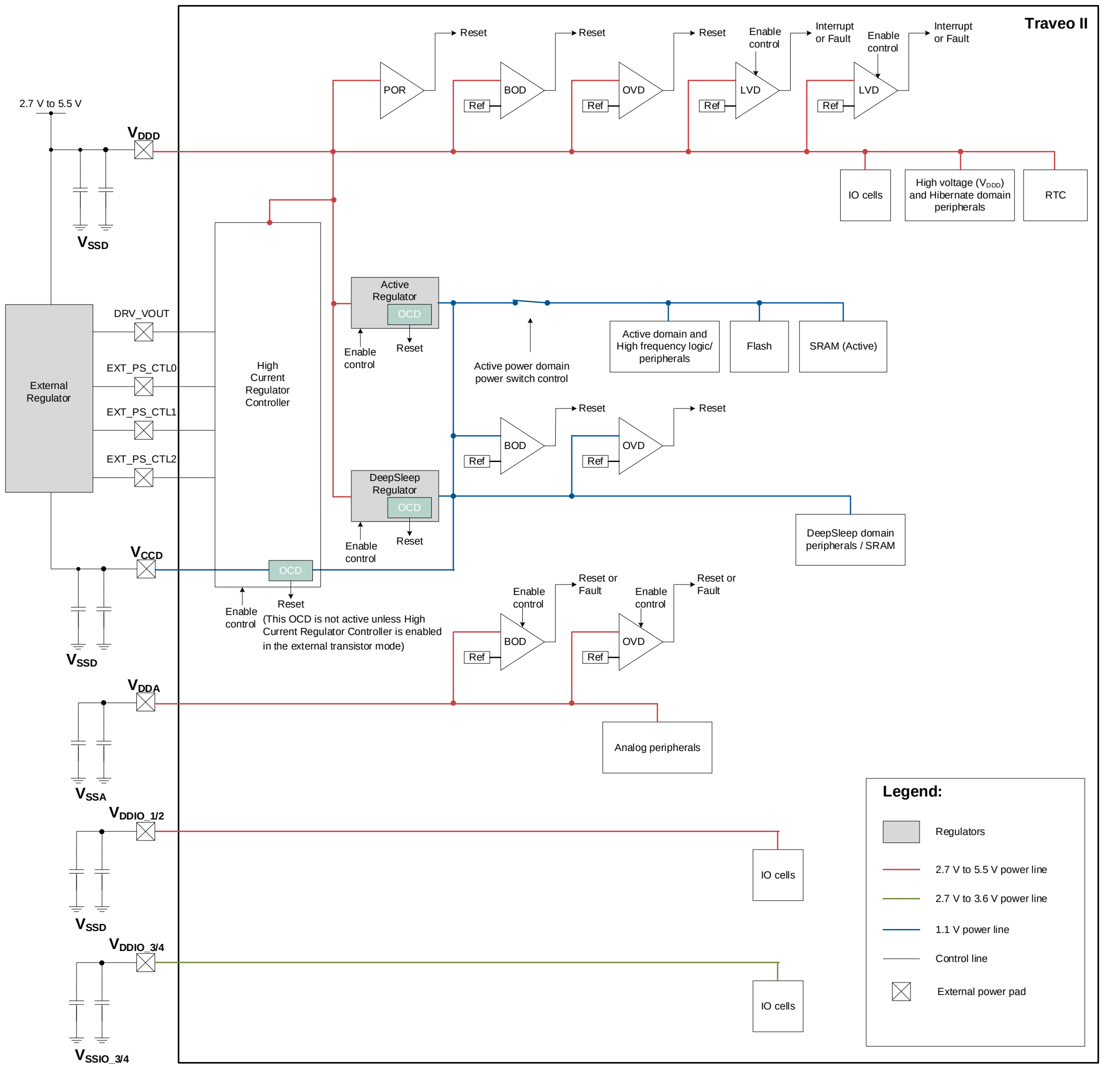


Hint Bar

Review datasheet and TRM section 16.3.3 for additional details

Voltage Monitoring Overview

- Over-Current Detection (OCD)



Hint Bar

Review datasheet and TRM section 16.3 for additional details

OCD Overview

- Detects if the device current is over the regulator limit
- Always on except in Hibernate and XRES modes
  - OCD on VCCD
    - Generates a reset by detecting if the load current of a regulator is higher than expected
  - OCD is not available when using PMIC

Hint Bar

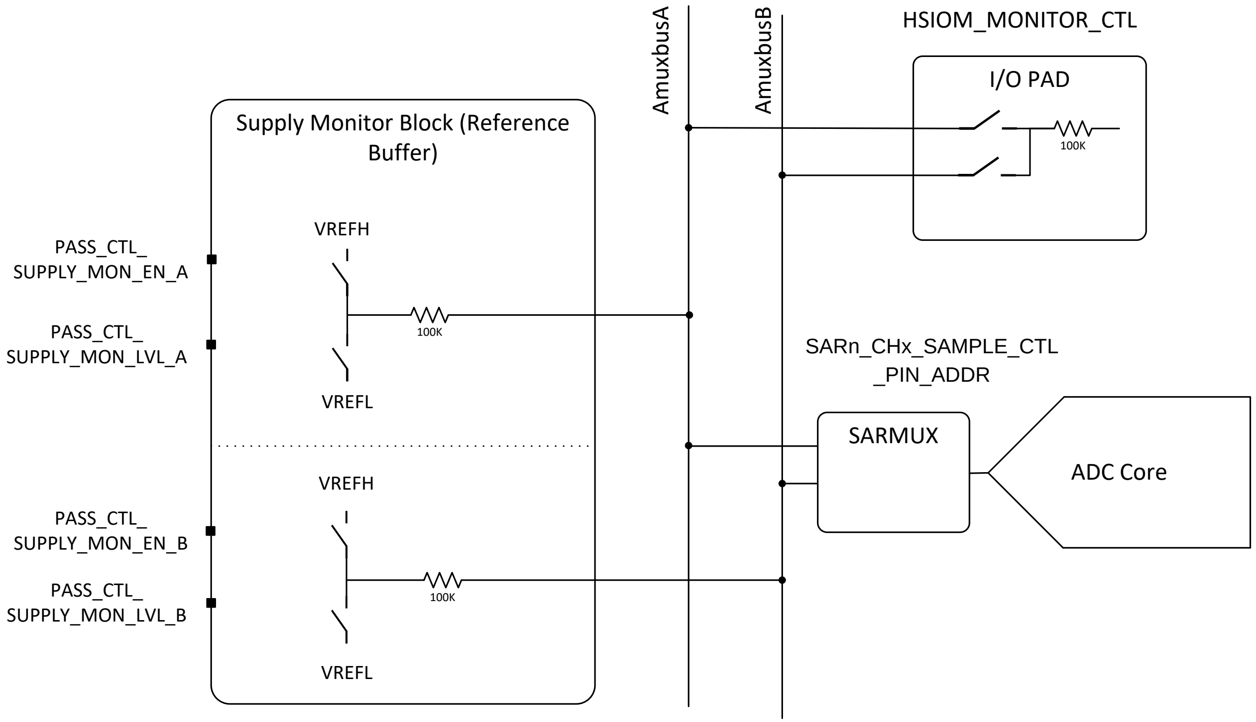
Review datasheet and TRM section 16.3.5 for additional details

Summary of Voltage Monitoring

Monitored Supply	Monitor	Trip Point	Output	Available Power Mode
V_{DDD}	POR	1 (Fixed)	Reset	All power modes
	BOD	2 (Programmable)	Reset	All power modes except Hibernate and XRES modes
	OVD	2 (Programmable)	Reset	
	LVD	26 (Programmable)	Interrupt, Fault, or No action	
V_{DDA}	BOD	2 (Programmable)	Reset, Fault, or No action	
	OVD	2 (Programmable)	Reset, Fault, or No action	
V_{CCD}	BOD	1 (Fixed)	Reset	
	OVD	1 (Fixed)	Reset	
	OCD[1]	1 (Fixed)	Reset	

Voltage Monitoring by ADC

- ADC is used for all other power supplies
- A monitor switch is provided between power/ground pad and AMUXBUS_A/B by the HSIOM_MONITOR_CTL register
- Midpoint of the signal (AMUXBUS_A/B) is connected to the SARMUX (internal signals) and can be selected for ADC by a channel
- Use case
  - VDDIO monitoring



Hint Bar

Review TRM section 16.3.7 for additional details.

Power Supply Monitoring by ADC

› Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

HSIOM_MONITOR_CTL_0	Power/ Ground Pins	AMUXBUS	BGA-320	BGA-272 for CYT4BF	BGA-272 for CYT3BB/4BB	TEQFP-176	TEQFP-144	TEQFP-100
Bit 0	V_{DDD}	A	F8, F9, H15, J15, K15, L15, M15, N15, R12, R13	F8, H13, J13, K13, L13, N11	F8, H13, J13, K13, L13, N11	176	144	100
Bit 2						22	18	12
Bit 4						43	35	24
Bit 13						110	90	62
Bit 15						132	108	75
Bit 17						153	124	86
Bit 1	V_{SSD}	B	A1, A20, C3, C10, C18, H9, H10, H11, H12, H13, J9, J10, J11, J12, J13, J18, K9, K10, K11, K12, K13, K18, L9, L10, L11, L12, L13, M9, M10, M11, M12, M13, N12, V3, V4, V15, Y1, Y20	A1, A18, D9, G7, G12, H9, H10, H11, J9, J10, J11, J15, K9, K10, K11, M7, M12, R5, R14, V1,V18	A1,A18,D9,G7,G12,H9,H10,H11,J9,J10,J11,J15,K9,K10,K11,M7,M12,R5,R14,V1,V18,L9,L10	1	1	1
Bit 3						23	19	13
Bit 6						45	37	26
Bit 12						46	73	51
Bit 14						89	94	66
Bit 16						111	109	76
Bit 19						133	126	88

Hint Bar

Review TRM sections 16.3.6 and 30.10 for additional details.

Power Supply Monitoring by ADC

› Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

HSIOM_MONITOR_CTL_0	Power/ Ground Pins	AMUXBUS	BGA-320	BGA-272 for CYT4BF	BGA-272 for CYT3BB/4BB	TEQFP-176	TEQFP-144	TEQFP-100
Bit 5	V_{DDIO_1}	A	F10, F11, F12, F13	F9, F10, F11	F9, F10, F11	44	36	25
Bit 18	V_{SSD_1} (BGA) V_{SSD} (TEQFP)	B	N13	L11	L11	154	125	87
Bit 7	V_{REFL}	B	M8	K8	K8	76	62	41
Bit 8	V_{SSA}	B	N8	L8	L8	77	63	42
Bit 9	V_{DDA}	A	N6	L6	L6	78	64	43
Bit 10	V_{REFH}	A	M6	K6	K6	79	65	44
Bit 11	V_{DDIO_2}	A	R8	N8	N8	88	72	50
Bit 20	V_{DDIO_3}	A	H6, J6, K6, L6	H6, J6	H6, J6	-	-	-
Bit 21	V_{SSIO_3}	B	H8, J8, K8, L8	H8, J8	H8, J8	-	-	-
Bit 22 Bit 24	V_{DDIO_4}	A	R9, R10, R11	N9, N10	-	-	-	-
Bit 23 Bit 25	V_{SSIO_4}	B	N9, N10, N11	L9, L10	-	-	-	-
Bit 5	V_{DDIO_1}	A	F10, F11, F12, F13	F9, F10, F11	F9, F10, F11	44	36	25
Bit 18	V_{SSD_1} (BGA) V_{SSD} (TEQFP)	B	N13	L11	L11	154	125	87

Hint Bar

Review TRM sections 16.3.6 and 30.10 for additional details.

Appendix

Comparison between CYT2B, CYT3B/4B, and CYT3D/4D

› Maximum number of system interrupts and wakeup interrupts varies by device.

Features		CYT2B	CYT3B/4B		CYT3D/4D
Power Supply and Monitoring	Power supply	V_{DDD} = 2.7 V to 5.5 V	V_{DDD} = 2.7 V to 5.5 V (up to 300 mA) V_{DDD} = 2.7 V to 5.5 V and V_{CCD} = 1.15 V (exceeds 300 mA)		
	5.0 V I/O power supply	V_{DDIO_1}, V_{DDIO_2}			V_{DDIO_GPIO}, V_{DDIO_SMC}
	3.3 V I/O power supply	N/A	V_{DDIO_3}, V_{DDIO_4}		V_{DDIO_HSIO}, $V_{DDIO\_SMIF\_HV}$
	1.8 V I/O power supply	N/A			V_{DDIO_SMIF}
	Analog power supply	V_{DDA}			V_{DDA_ADC}, V_{DDA_DAC}, V_{DDA_MIPI}, V_{DDA_FPD0}, V_{DDA_FPD1}, V_{DDHA_FPD0}, V_{DDHA_FPD1}, V_{DDPLL_FPD0}, V_{DDPLL_FPD1}
	Active/DeepSleep regulator	Same			
	External transistor control	N/A	Available	N/A	
	External PMIC control	N/A	Available		
	POR/BOD/OVD/LVD	Same			

Part of your life. Part of tomorrow.

Revision History

Revision	ECN	Submission Date	Description of Change
**	6402061	03/12/2018	Initial release
*A	7053306	12/14/2020	Updated page 2, 3, 6, 8 to 11, 28, 29, 31.