# Customer Training Workshop

## Traveo™ II Automotive Body Controller Entry/High and Cluster 2D Family Overview

Q4 2020

# Target Products

› Target product list for this training material:

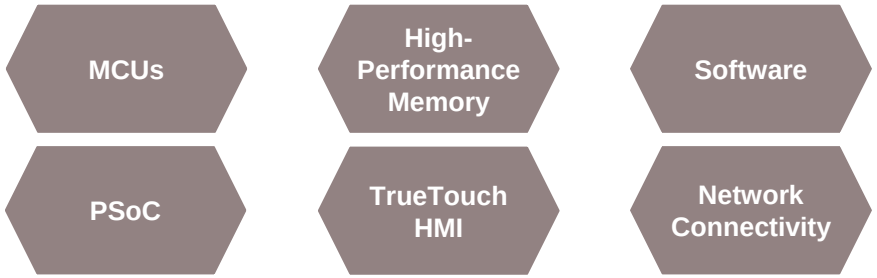
| Family Category | Series | Code Flash Memory Size |
|---|---|---|
| Traveo™ II Automotive Body Controller Entry | CYT2B6 | Up to 576 KB |
| Traveo II Automotive Body Controller Entry | CYT2B7 | Up to 1088 KB |
| Traveo II Automotive Body Controller Entry | CYT2B9 | Up to 2112 KB |
| Traveo II Automotive Body Controller Entry | CYT2BL | Up to 4160 KB |
| Traveo II Automotive Body Controller High | CYT3BB/4BB | Up to 4160 KB |
| Traveo II Automotive Body Controller High | CYT4BF | Up to 8384 KB |
| Traveo II Automotive Cluster | CYT3DL | Up to 4160 KB |
| Traveo II Automotive Cluster | CYT4DN | Up to 6336 KB |

# Cypress Embedded in Automotive Systems

- Instrument Cluster[1]
  - Virtual and Hybrid Clusters
  - Head-Up Display
- Infotainment
  - Navigation with Security
  - Central Information Display
  - Satellite/Audio Systems
  - Rear-Seat Entertainment
  - Touch/Character Recognition
- ADAS Safety
  - TPMS
  - Air Bag
  - Telematics
  - Surround Camera
  - Radar System
- Body Electronics
  - HVAC
  - Gateway
  - Body Control
  - Comfort
  - Lighting

**Cypress electronics solutions cover a wide variety of applications inside and outside the automobile cockpit**

**Cypress' Embedded Systems Product Portfolio**




- Cypress' Automotive Track Record
  - A comprehensive portfolio of AEC-Q100-qualified embedded system products
  - Over 30 years of experience supporting automotive quality requirements
  - Cypress is the third-largest supplier of automotive MCUs and memories Cypress has earned preferred supplier status from the Top 25 automotive OEMs
- Scalable MXS40 Technology Platform
  - High-performance 40-nm process
  - Based on single Arm® Cortex®-M4/-M7 and dual Cortex-M7
  - Pre-verified IP and core systems improve quality and constancy
  - Strong hardware-based security Crypto IP blocks
  - Flexible Smart I/O™ interfaces
  - Faster, cost-effective, and flexible derivatives
  - Script-driven chip implementations
  - Proven system software support

[1] Additional resources for Automotive applications and Cypress solutions are available at www.cypress.com/solutions

# Traveo II Body Controller Entry

# Overview

- Includes Arm® Cortex® -M4F and M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (such as body control units)
- Features
  - 32-bit CPU subsystem:
  - 160-MHz[1] 32-bit Cortex-M4F CPU with single-cycle multiply, floating-point units (FPU), and memory protection units (MPUs)
  - 100-MHz[2] 32-bit Cortex-M0+ CPU with MPU
- CYT2B6: Up to 576KB of Code Flash along with 64KB of Work Flash
- CYT2B7: Up to 1088KB of Code Flash along with 96KB of Work Flash
- CYT2B9: Up to 2112KB of Code Flash along with 128KB of Work Flash
- CYT2BL: Up to 4160KB of Code Flash along with 128KB of Work Flash
  - Dual Bank Mode support for Firmware Over-the-Air (FOTA) for CYT2B7/B9
- SRAM: CYT2B6: Up to 64KB, CYT2B7: Up to 128KB, CYT2B9: Up to 256KB, CYT2BL: Up to 512KB
- Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
- Low-power 2.7-5.5-V operation
- Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

[1] CYT2B6 up to 80-MHz
[2] CYT2B6 up to 80-MHz

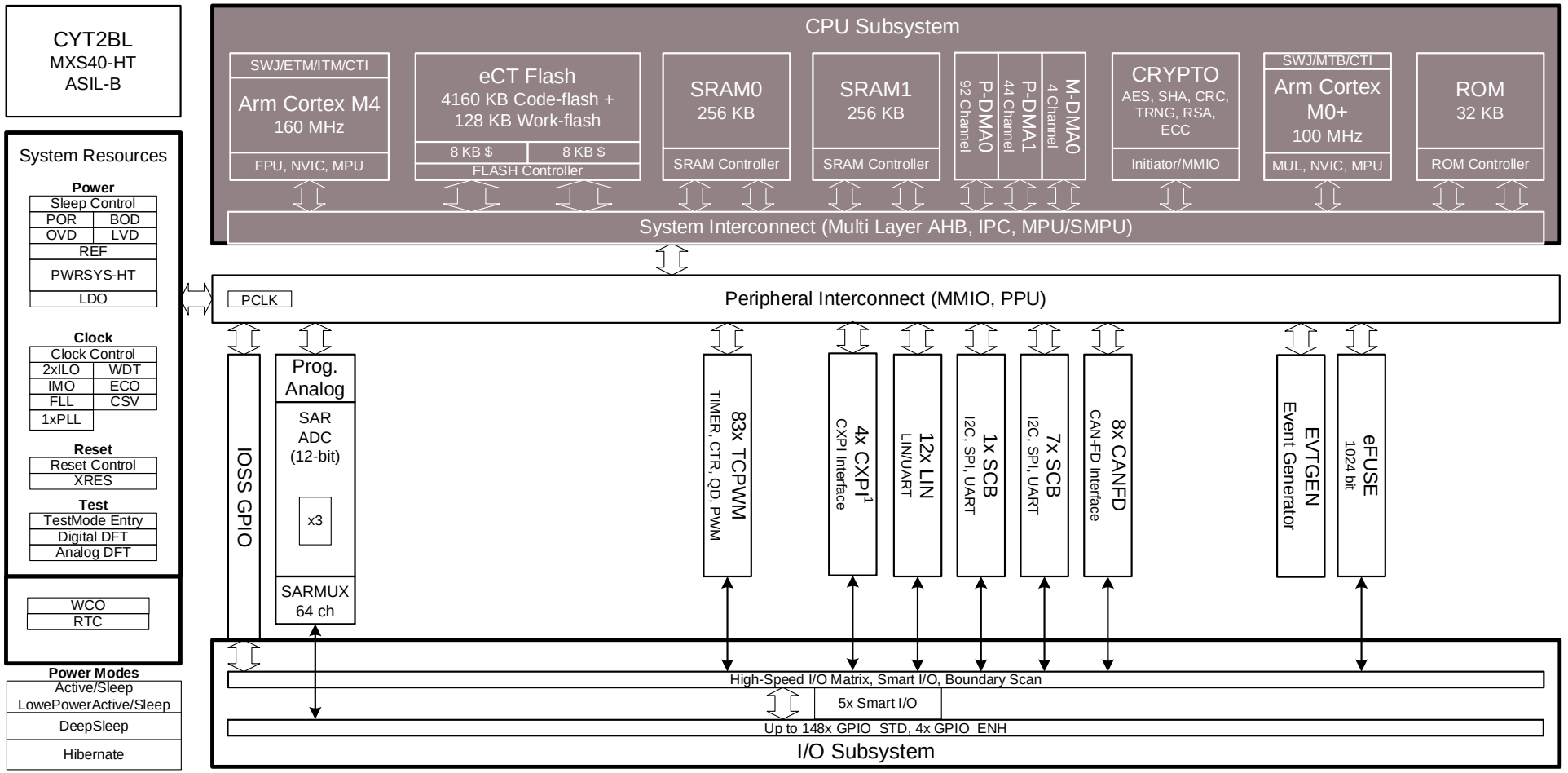
# Overview

- Features (continued)
- AEC-Q100 qualification and ASIL-B level functional safety
- Debugging via SWD/JTAG controller and interface-compliant IEEE-1149.1-2001, and Flash programming
  on the SWD/JTAG interface
- Packages:
  - 64-/80-/100-/144-/176-LQFP packages available for CYT2B7/B9/BL
  - 64-/80-/100-LQFP packages available for CYT2B6

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# CYT2BL Architecture Diagrams:
# CPU Subsystem

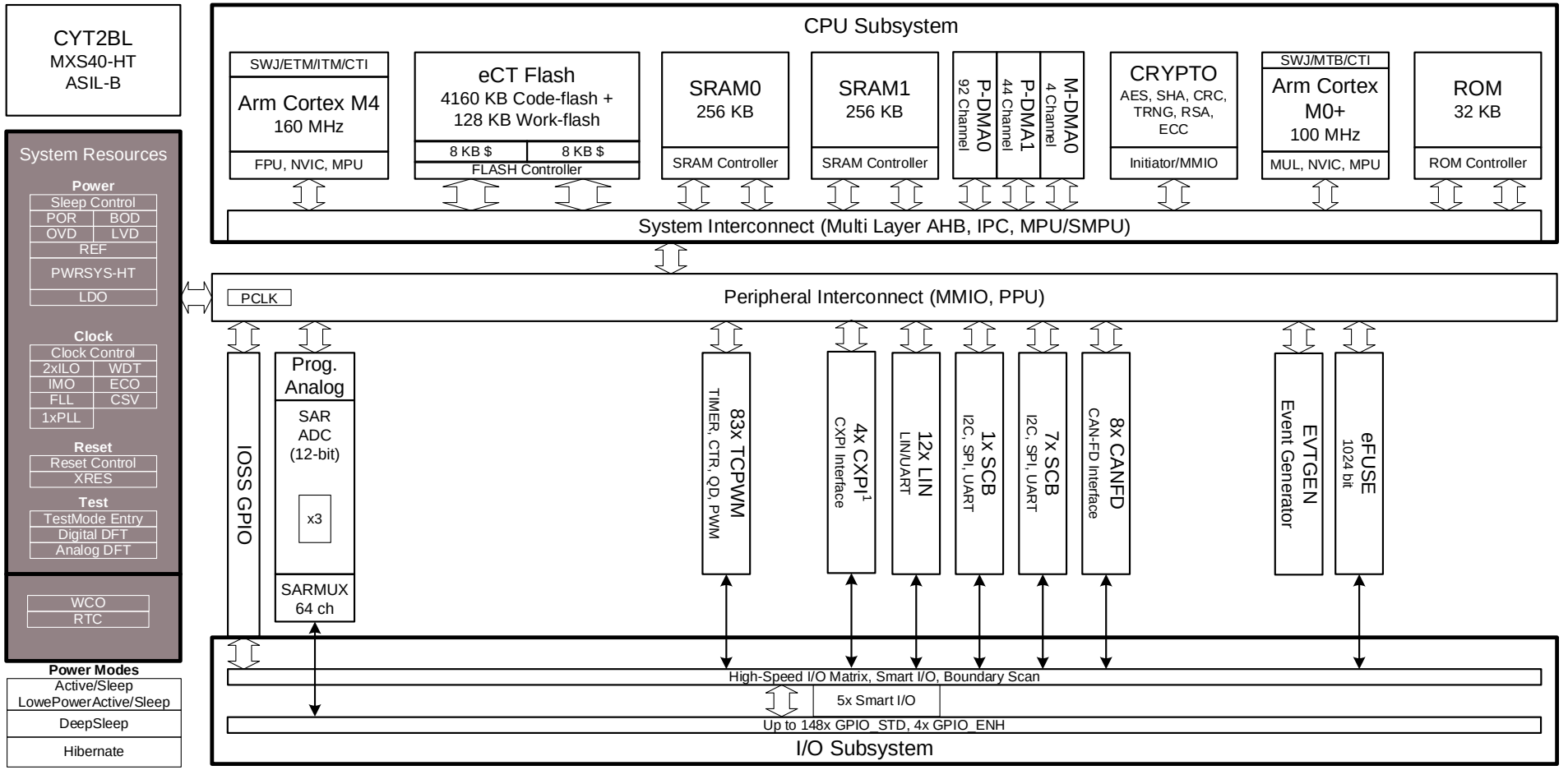



## Hint Bar

**Training section reference**

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

# CYT2BL Architecture Diagrams:
# System Resources




## Hint Bar

**Training section reference**

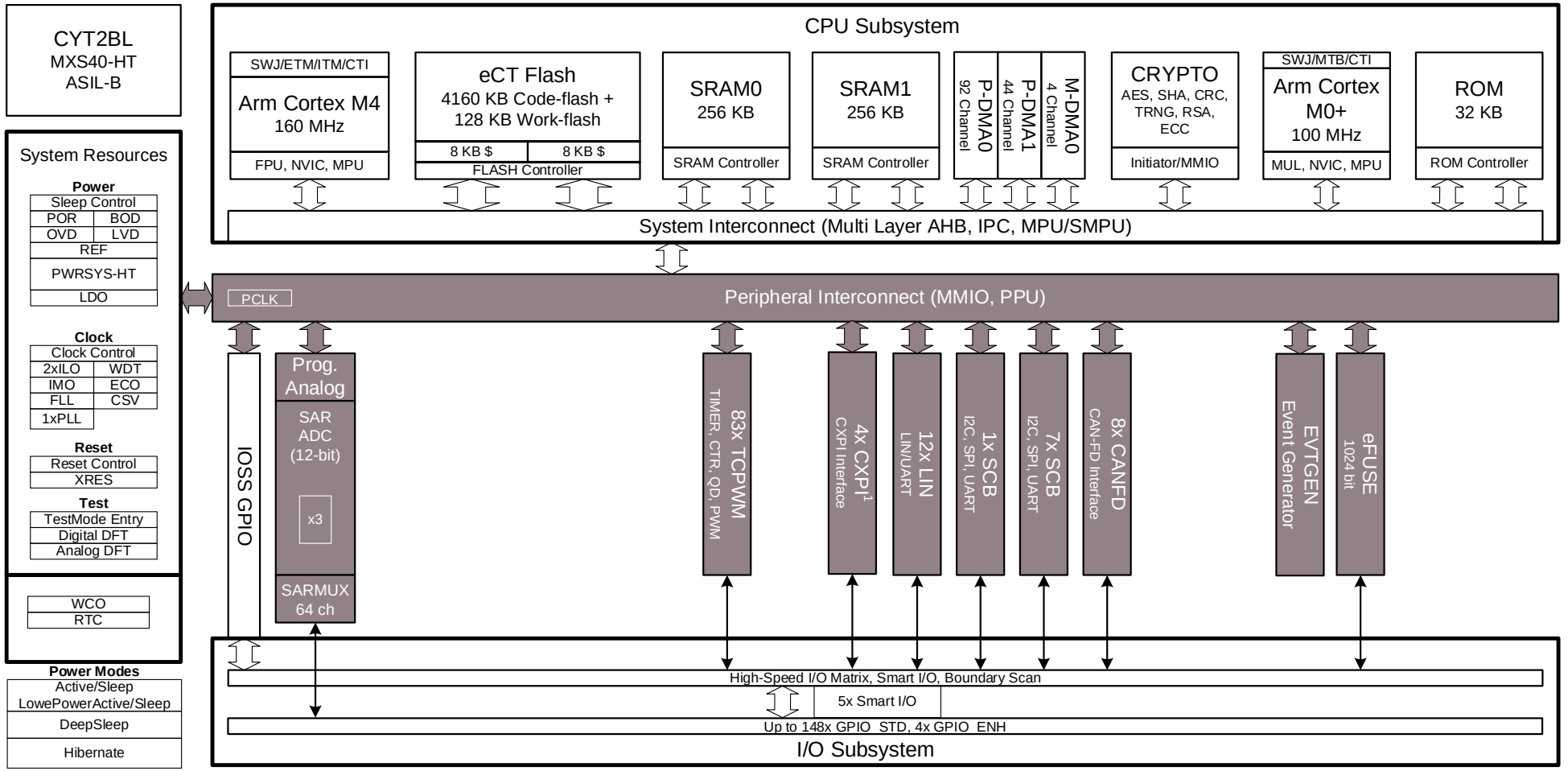
**- Power Supply and Monitoring**

**- Clock System**

**- Watchdog Timer**

**- Reset System**

# CYT2BL Architecture Diagrams:
# Peripheral Blocks




## Hint Bar

**Training section reference**

**- SAR ADC**

**- TCPWM (Timer/Counter/Pulse-Width Modulator)**

**- Serial Communication Blocks (SCB)**

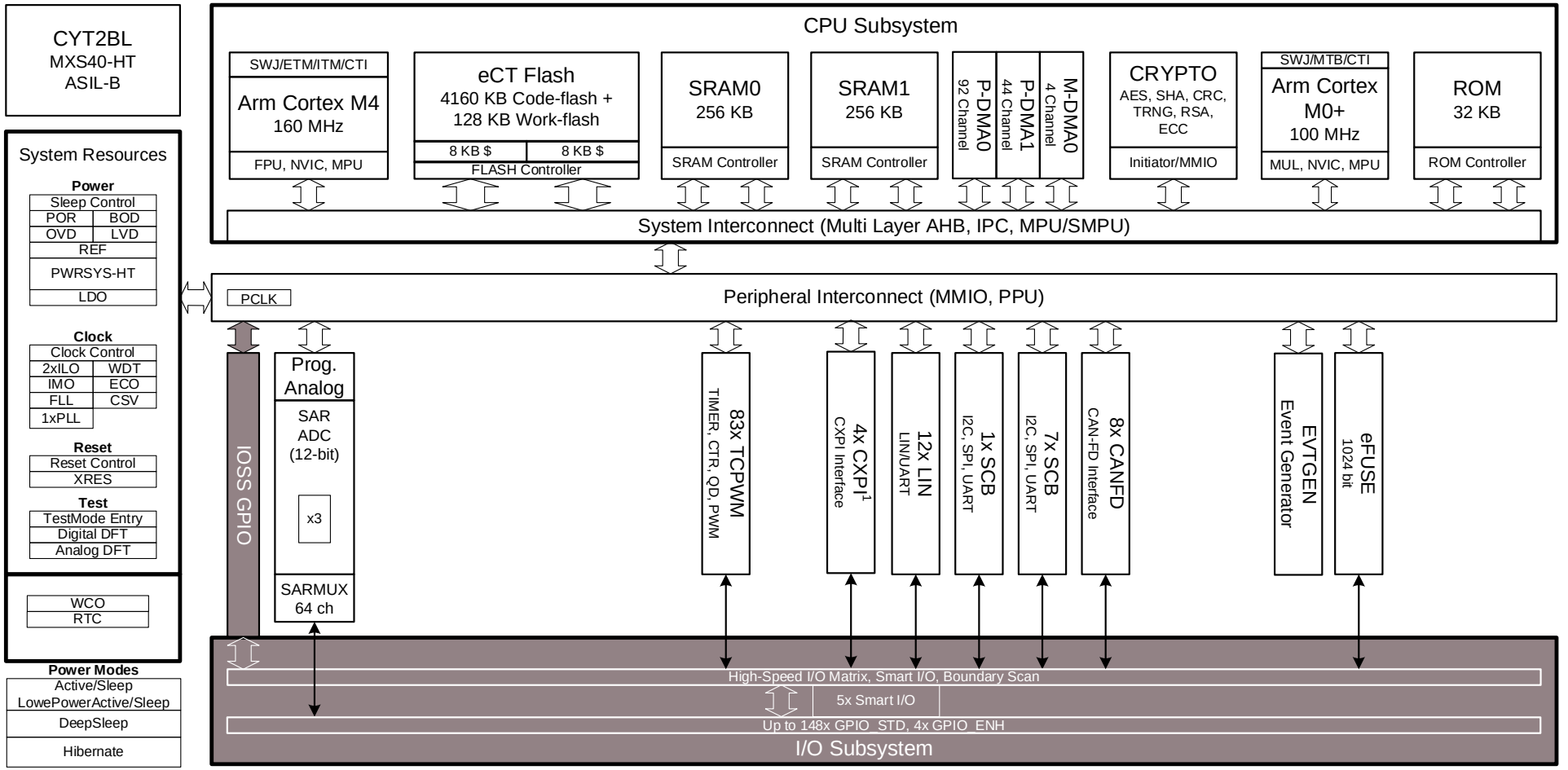
**- Local Interconnect Network (LIN)**

**- CAN FD**

**- Event Generator**

**- CXPI**

# CYT2BL Architecture Diagrams:
# I/O Subsystem




## Hint Bar

**Training section reference**
**- I/O Subsystem**

# Traveo II Body Controller High

# Overview

- Includes Arm® Dual Cortex®-M7 and M0+ CPUs, manufactured using a high-performance
  40-nm process
- Target applications
  - Automotive systems (gateway, high-end body-control units, etc.)
- Features
  - 32-bit CPU subsystem:
    - CYT3BB: One 250-MHz 32-bit Cortex-M7 CPU, with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    - CYT4BB: Two 250-MHz 32-bit Cortex-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    - CYT4BF: Two 350-MHz 32-bit Cortex-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    - 100-MHz 32-bit Cortex-M0+ CPU with MPU
  - CYT3BB/4BB: 4160KB of Code Flash along with 256KB of Work Flash:
  - CYT4BF: 8384KMB of Code Flash along with 256KB of Work Flash:
    - Dual Bank Mode support for Firmware Over-the-Air (FOTA)
  - SRAM: CYT3BB/4BB: 768KB, CYT4BF: 1024KB
  - Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  - Internal (up to 300 mA) power supply: VDDD = 2.7 V to 5.5 V
  - External (up to 600 mA) power supply: VDDD = 2.7 V to 5.5 V and VCCD = 1.15 V (1.1 V to 1.2 V)

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

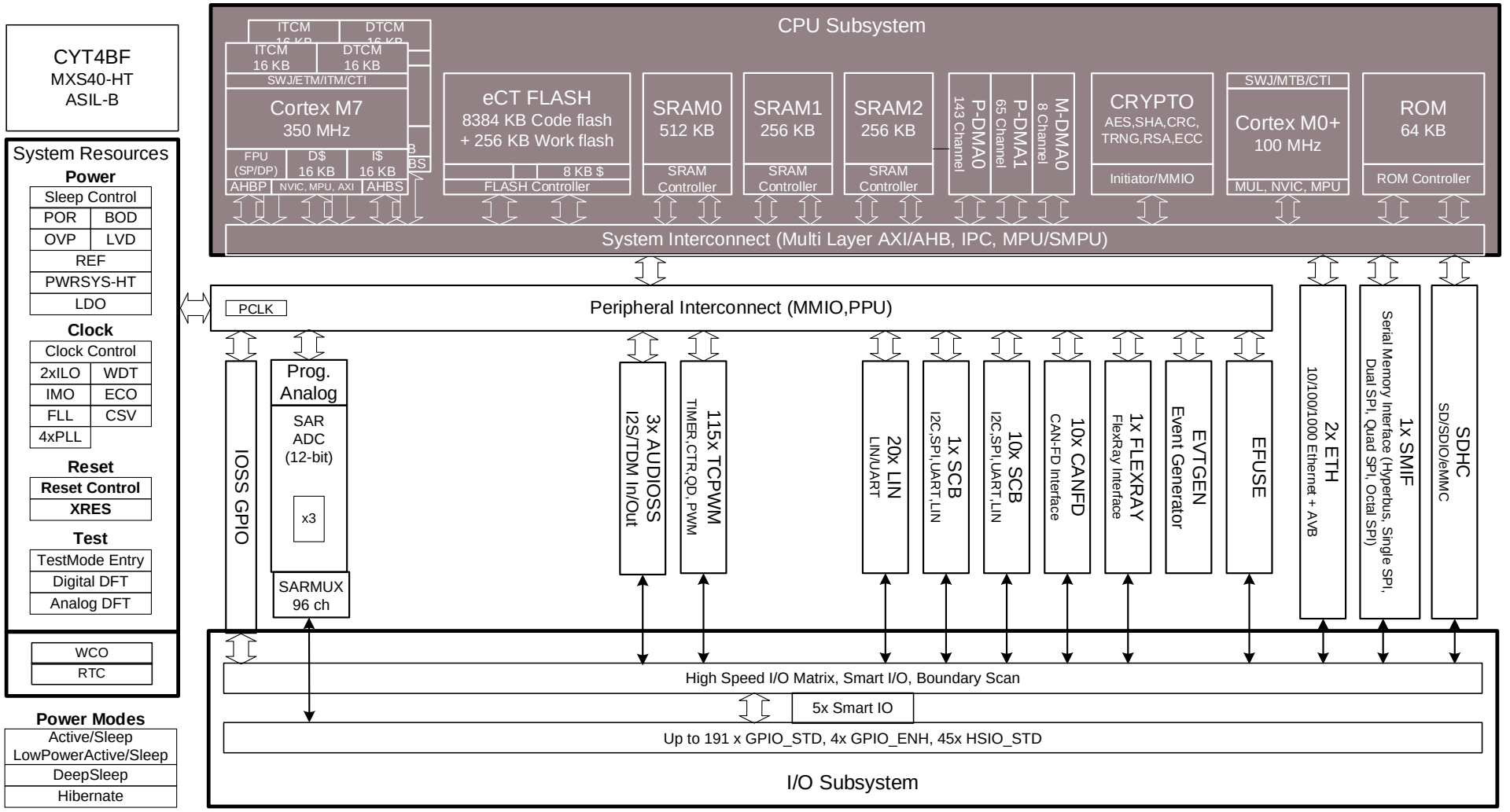
# Overview

- Features (continued)
  - Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support
  - AEC-Q100 qualification and ASIL-B level functional safety
  - Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001,
    and Flash programming through SWD/JTAG interface
  - Packages:
    - CYT3BB/4BB: 100-/144-/176-TEQFP, 272-FBGA packages available
    - CYT4BF: 176-TEQFP, 272-FBGA, 320-BGA packages available

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# CYT4BF Architecture Diagrams:
# CPU Subsystem

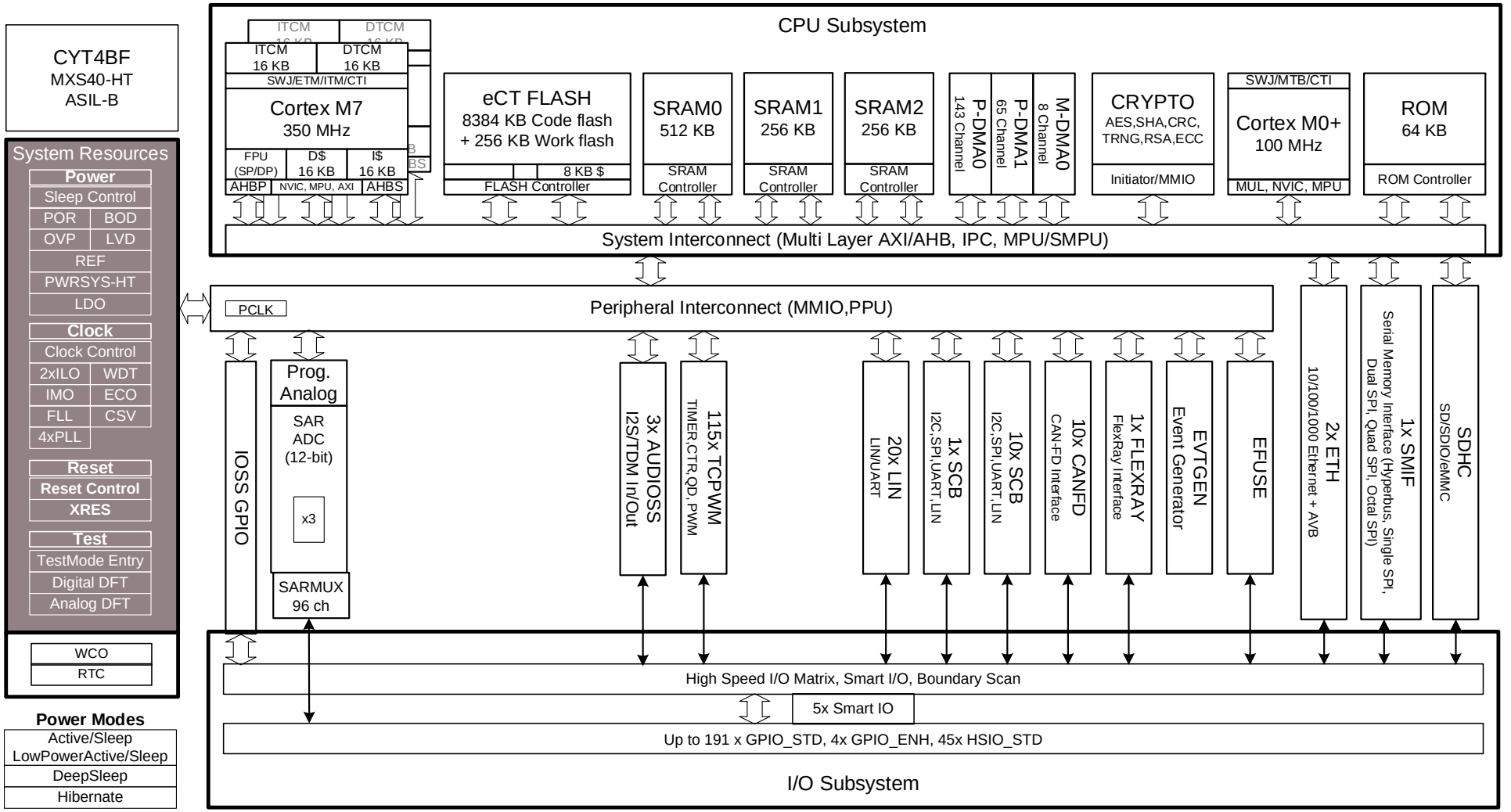



## Hint Bar

**Training section reference**

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

# CYT4BF Architecture Diagrams:
# System Resources

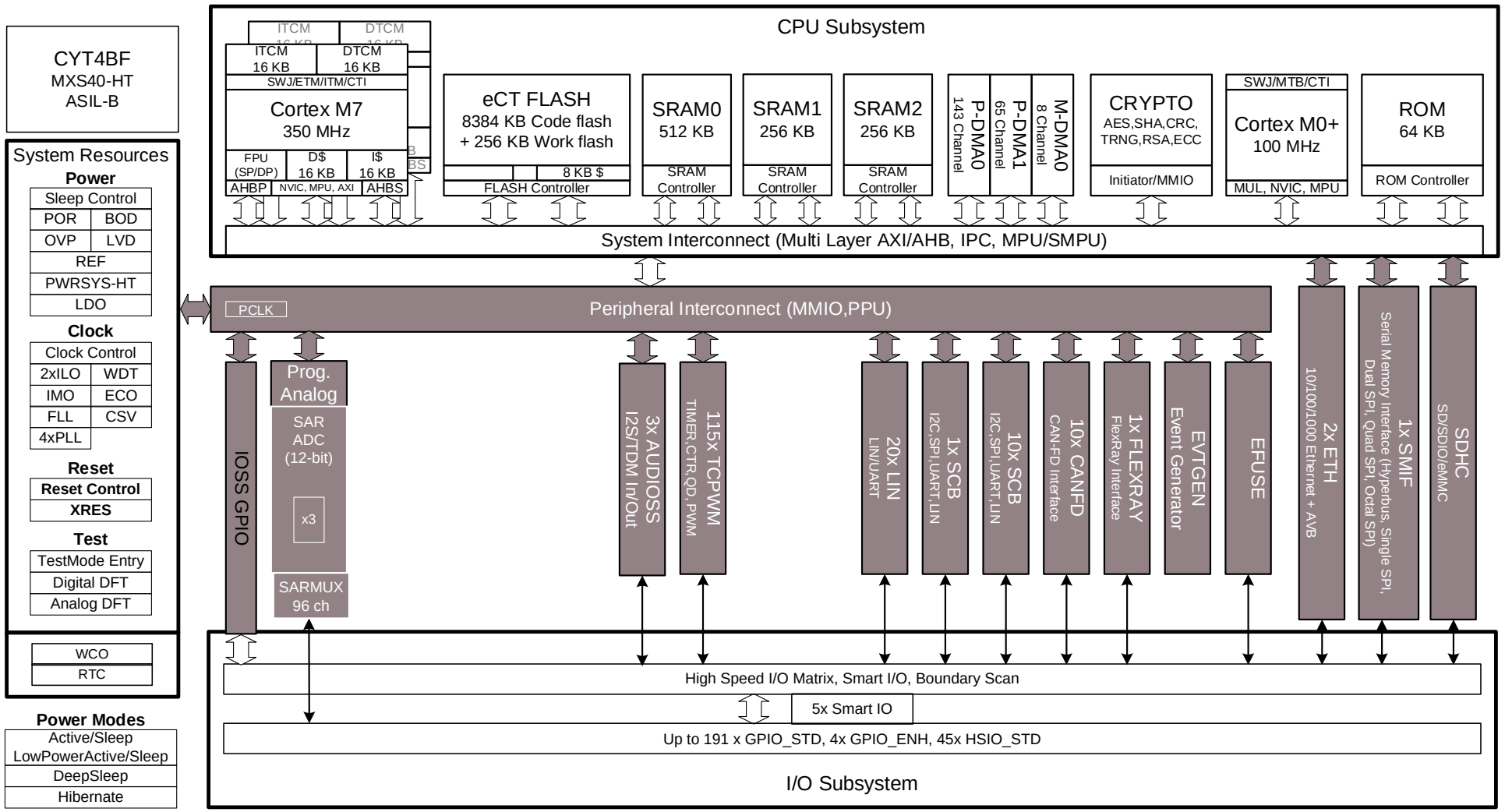



## Hint Bar

**Training section reference**

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

# CYT4BF Architecture Diagrams:
# Peripheral Blocks

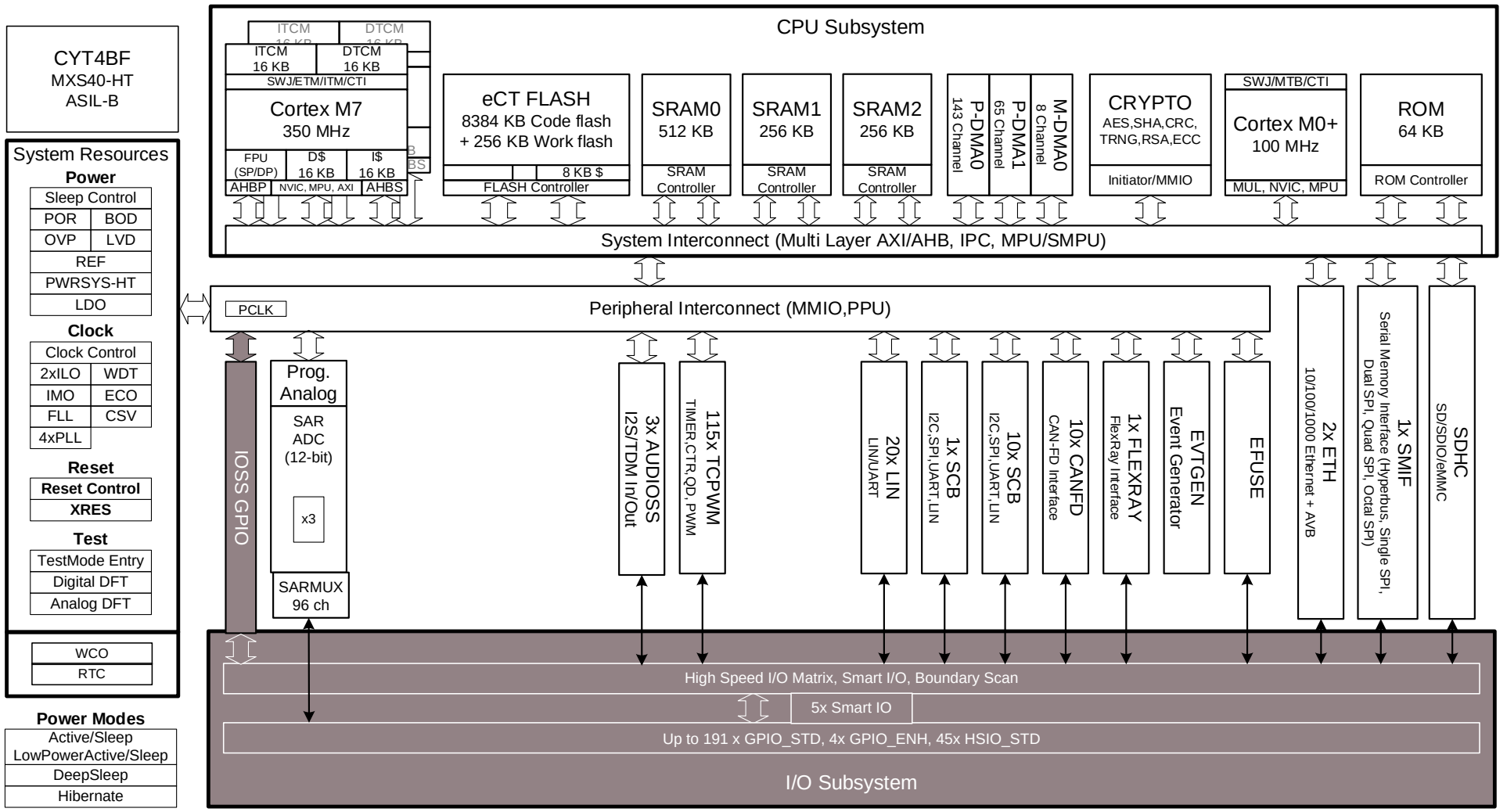



## Hint Bar

**Training section reference**

- **SAR ADC**
- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **CXPI**

# CYT4BF Architecture Diagrams:
# I/O Subsystem




## Hint Bar

**Training section reference**
**- I/O Subsystem**

# Traveo II Cluster

# Overview

- Includes Arm® Dual Cortex®-M7 and M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (instrument clusters, head-up displays, etc.)
- Features
  - Graphics Subsystem
    - Supports 2D and 2.5D (perspective warping, 3D effects) graphics rendering
    - Up to 30-bit color resolution (RGB)
    - Embedded video RAM memory (VRAM): CYT3DL: 2048KB,  CYT4DN: 4096 KB
    - Up to two video output interfaces supporting two displays
    - One capture engine for video input processing for ITU 656 or parallel RGB/YUV input
  - Audio Subsystem

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# Overview

**Features**

- 32-bit CPU subsystem:
  - CYT3DL: One 240-MHz 32-bit Cortex-M7 CPU, with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
  - CYT4DN: Two 320-MHz 32-bit Cortex-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
  - 100-MHz 32-bit Cortex-M0+ CPU with MPU
- CYT3DL: 4160KB of Code Flash along with 128KB of Work Flash:
- CYT4DN: 6336KB of Code Flash along with 128KB of Work Flash:
  - Dual Bank Mode support for Firmware Over-the-Air (FOTA)
- SRAM: CYT3DL: 384KB, CYT4DN: 640KB
- Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
- Power supply rails
  - Internal (up to 300 mA) power supply: VDDD = 2.7 V to 5.5 V
  - External (exceed 300 mA) power supply: VDDD = 2.7 V to 5.5 V and VCCD=1.15 V (1.1 V to 1.2 V)
  - 5.0 V I/O for VDDIO_GPIO, VDDIO_SMC = 2.7 V to 5.5 V
  - 3.3 V I/O for VDDIO_HSIO, VDDIO_SMIF_HV = 3.0 V to 3.6 V
  - 1.8 V I/O for VDDIO_SMIF = 1.7 V to 2.0 V
- Hardware Secure Module (HSM) support
- AEC-Q100 qualification and ASIL-B level functional safety

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# Overview

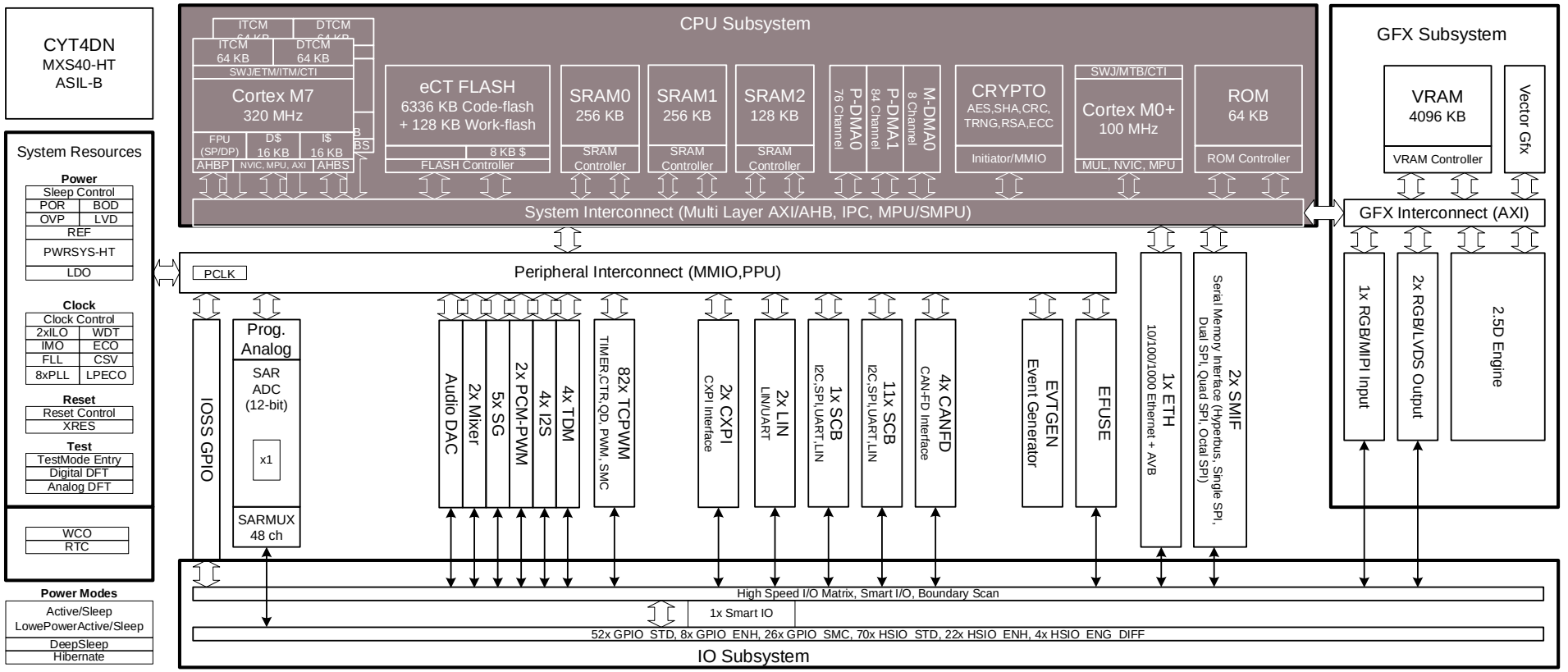
**Features (continued)**

- Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001,
  and Flash programming through SWD/JTAG interface
- Packages:
  - CYT3DL: 208-/216-TEQFP, 272-BGA packages available
  - CYT4DN: 327-/500-BGA packages available

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# CYT4DN Architecture Diagrams:
# CPU Subsystem

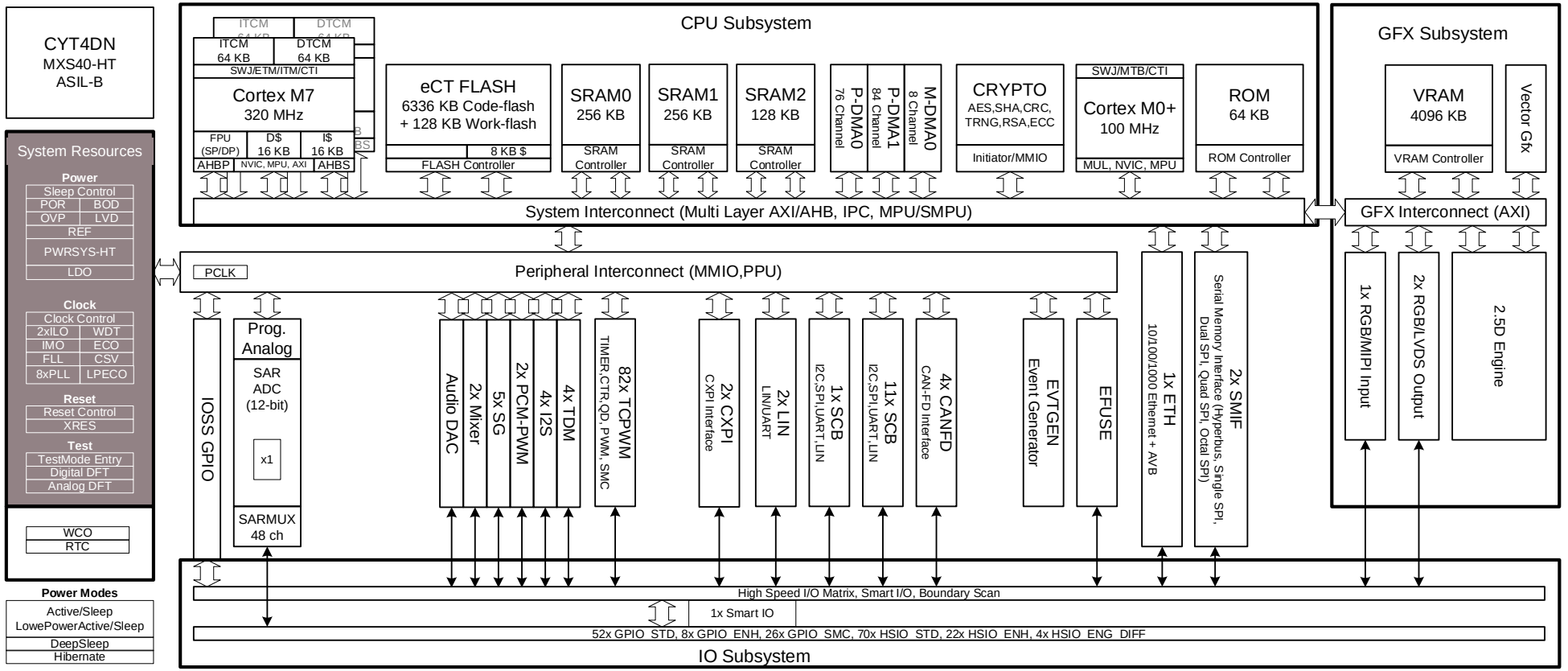



## Hint Bar

**Training section reference**

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

# CYT4DN Architecture Diagrams:
# System Resources

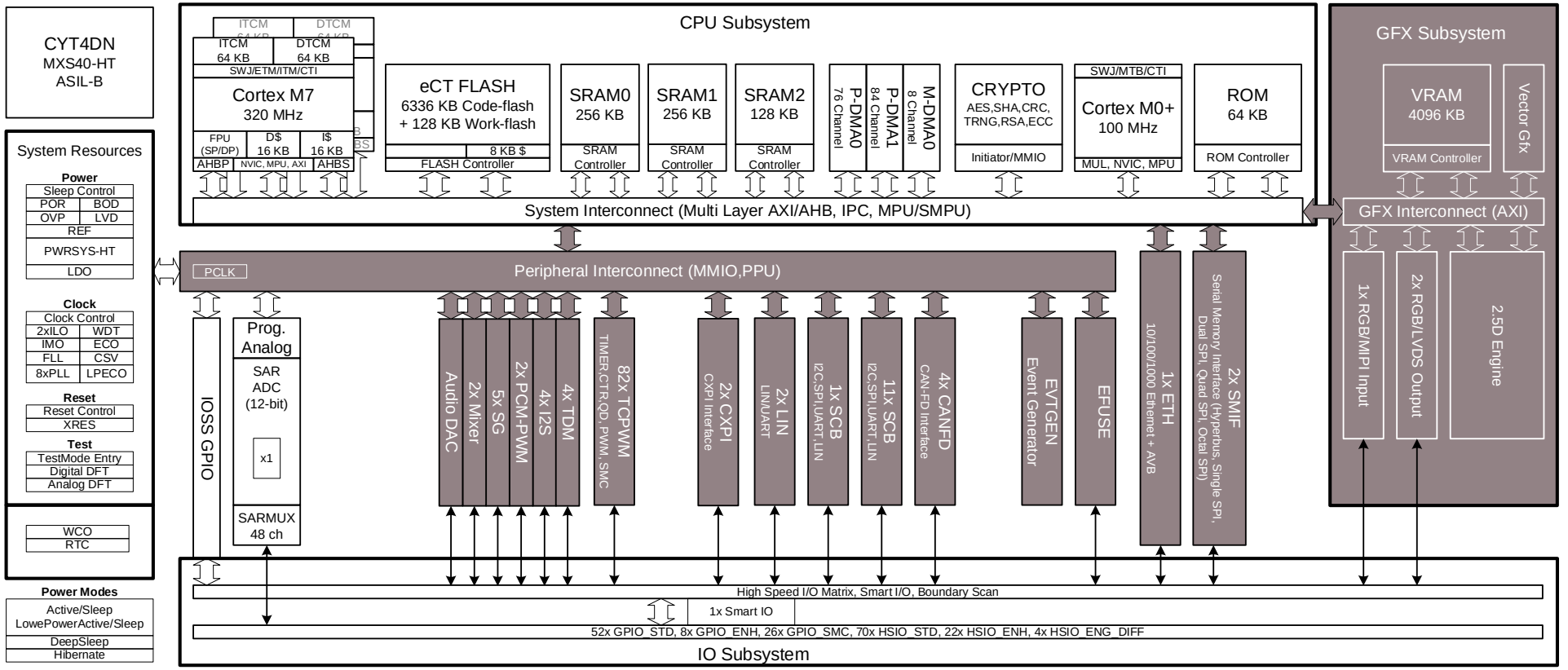



## Hint Bar

**Training section reference**

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

# CYT4DN Architecture Diagrams:
# Peripheral Blocks

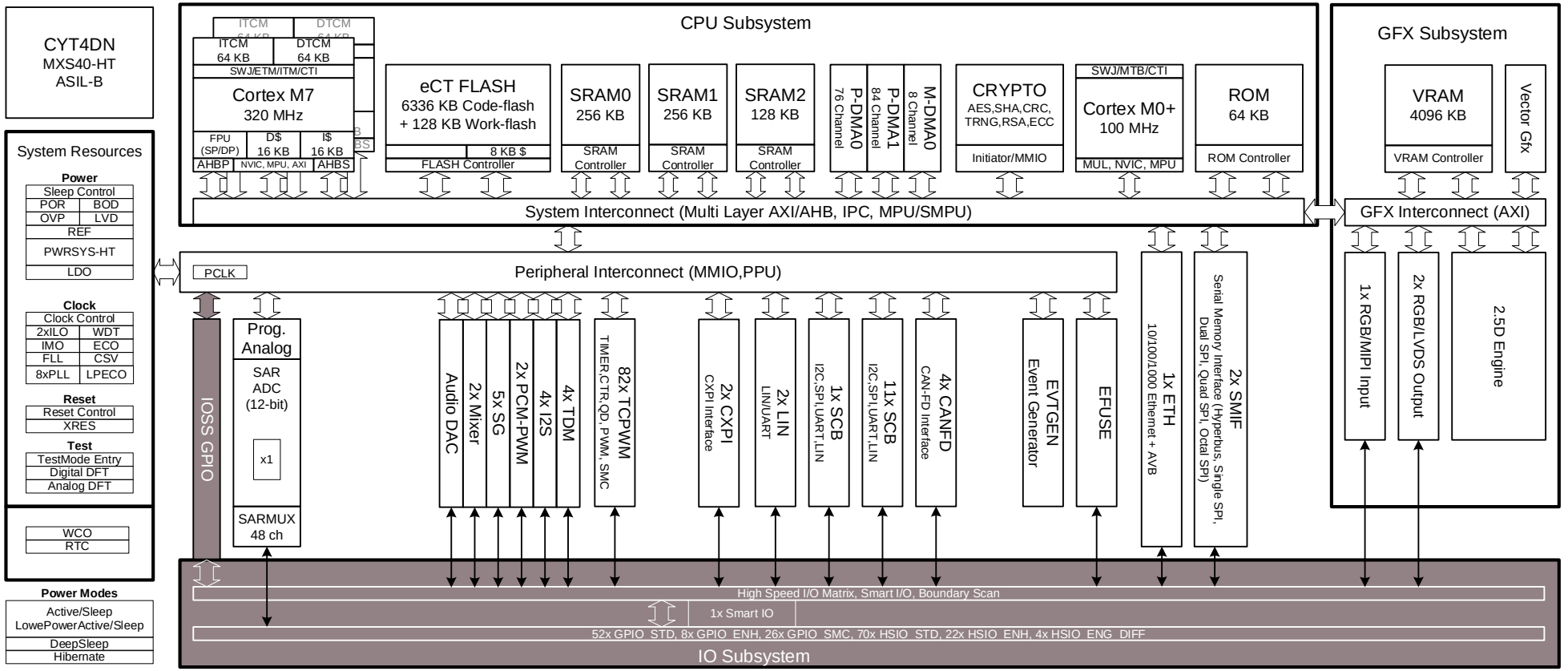



## Hint Bar

**Training section reference**

- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **Audio SS**
- **Ethernet**
- **SMIF**
- **Graphics**

# CYT4DN Architecture Diagrams:
# I/O Subsystem




## Hint Bar

**Training section reference**

- **I/O Subsystem**
- **SAR ADC**

# Appendix

## Comparison between CYT2B, CYT4B, and CYT4D

# Feature Comparison between CYT2B/CYT4B/CYT4D (1/4)

| Features | | CYT2B | CYT4B | CYT4D |
|---|---|---|---|---|
| CPU Subsystem | Main CPU | Cortex-M4 CPU | Two Cortex-M7 CPUs | |
| | FPU | Single-precision | Single/double-precision | |
| | Cache | - | 16 KB instruction, 16 KB data | |
| | MPU | Same | | |
| | System Tick Timer | Same | | |
| Inter-Processor Communication (IPC) | | Same | | |
| Protection Unit | | Same | | |
| Direct Memory Access | | Same | | |
| Flash | Bus interface | AHB-Lite | AXI, AHB-Lite | |
| | ECC (SEC/DED) | Same | | |
| | Bank modes | Same | | |
| SRAM Interface | Bus interface | AHB-Lite | AXI, AHB-Lite | |
| | ECC (SEC/DED) | Same | | |
| | TCM | N/A | 16 KB ITCM, 16 KB DTCM | 64 KB ITCM, 64 KB DTCM |
| Boot | | Same | | |
| Interrupts | | Same | | |
| Device Security with Crypto | | Same | | |
| Chip Operational Modes | | Same | | |
| Fault Subsystem | | Same | | |

# Feature Comparison between CYT2B/CYT4B/CYT4D (2/4)

| Features | | CYT2B | CYT4B | CYT4D |
|---|---|---|---|---|
| Power Supply and Monitoring | Power supply | $V_{DDD}$ = 2.7 V to 5.5 V | $V_{DDD}$ = 2.7 V to 5.5 V (up to 300 mA)<br>$V_{DDD}$ = 2.7 V to 5.5 V and $V_{CCD}$ = 1.15 V (exceeds 300 mA) | |
| | 5.0 V I/O power supply | $V_{DDIO\_1}$, $V_{DDIO\_2}$ | | $V_{DDIO\_GPIO}$, $V_{DDIO\_SMC}$ |
| | 3.3 V I/O power supply | N/A | $V_{DDIO\_3}$, $V_{DDIO\_4}$ | $V_{DDIO\_HSIO}$, $V_{DDIO\_SMIF\_HV}$ |
| | 1.8 V I/O power supply | N/A | | $V_{DDIO\_SMIF}$ |
| | Analog power supply | $V_{DDA}$ | | $V_{DDA\_ADC}$, $V_{DDA\_DAC}$, $V_{DDA\_MIPI}$, $V_{DDA\_FPD0}$, $V_{DDA\_FPD1}$, $V_{DDHA\_FPD0}$, $V_{DDHA\_FPD1}$, $V_{DDPLL\_FPD0}$, $V_{DDPLL\_FPD1}$ |
| | Active/DeepSleep regulator | Same | | |
| | External transistor control | N/A | Available | N/A |
| | External PMIC control | N/A | Available | |
| | BOD/OVD/LVD | Same | | |
| Device Power Modes | | Same | | |
| Clock System | Internal clock sources (IMO, ECO) | Same | | |
| | External clock sources (ECO, WCO, EXT_CLK) | Same | Support LPECO | |
| | FLL | Same | | |
| | PLL without SSCG and fractional operation | Same | | |
| | PLL with SSCG and fractional operation | N/A | Available | |
| | Clock supervision (CSV) | Same | | |
| | Clock calibration counter | Same | | |
| Reset System | | Same | | |

# Feature Comparison between CYT2B/CYT4B/CYT4D (3/4)

| Features | | CYT2B | CYT4B | CYT4D |
|---|---|---|---|---|
| Watchdog Timer | | Same | | |
| Real Time Clock | | Same | | |
| I/O System | GPIO input modes (CMOS/TTL/Automotive) | Same | | |
| | Eight output drive modes | Same | | |
| | Drive strength (Full, 1/2, 1/4) | Same | | |
| | Slew rate control (only for GPIO_ENH) | Same | | |
| | GPIO interrupt | Same | | |
| | Smart I/O | Same | | |
| | GPIO SMC | N/A | N/A | Available |
| | High-speed I/O | N/A | Available (HSIO_STD) | Available (HSIO_STD, HSIO_ENH, HSIO_ENH_DIFF) |
| CAN FD | | Same | | |
| Serial Communications Block | | Same | | |
| TCPWM | | Same | | |
| LIN | | Same | | |
| Event Generator | | Same | | |
| Trigger Multiplexer | | Same | | |
| FlexRay | | N/A | Available | N/A |
| Ethernet MAC | | N/A | Available | Available |

# Feature Comparison between CYT2B/CYT4B/CYT4D (4/4)

| Features | CYT2B | CYT4B | CYT4D |
|---|---|---|---|
| Serial Memory Interface | N/A | Available | Available |
| SDHC Host Controller | N/A | Available | - |
| Audio Subsystem | N/A | Available | N/A |
| Sound Subsystem | N/A | N/A | Available |
| Graphics Subsystem | N/A | N/A | Available |
| SAR ADC | Same | | |
| Program and Debug Interface | Same | | |
| Nonvolatile Memory Programming | Same | | |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# Revision History

| Revision | ECN | Submission Date | Description of Change |
|---|---|---|---|
| ** | 6097587 | 09/03/2018 | Initial release |
| *A | 6401071 | 12/04/2018 | Added CYT2B9 and CYT4BF<br>Updated the Block Diagram |
| *B | 6682714 | 09/26/2019 | Updated title to include cluster<br>Removed page 3<br>Updated CM0+ frequency from 80 MHz to 100 MHz<br>Added CYT4DN (page 17 to 23, 34 to 38)<br>Updated Functional Overview in Appendix |
| *C | 7053676 | 12/24/2020 | Updated page 2, 5 to 10, 12, 13, 19, 20, 21 |