Customer Training Workshop

Traveo™ II Automotive Body Controller Entry/High and Cluster 2D Family Overview

Q4 2020
### Target Products

Target product list for this training material:

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Body Controller Entry</td>
<td>CYT2B6</td>
<td>Up to 576 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B7</td>
<td>Up to 1088 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2B9</td>
<td>Up to 2112 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller Entry</td>
<td>CYT2BL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT3BB/4BB</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Body Controller High</td>
<td>CYT4BF</td>
<td>Up to 8384 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160 KB</td>
</tr>
<tr>
<td>Traveo II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336 KB</td>
</tr>
</tbody>
</table>
Cypress Embedded in Automotive Systems

› Instrument Cluster¹
  - Virtual and Hybrid Clusters
  - Head-Up Display
› Infotainment
  - Navigation with Security
  - Central Information Display
  - Satellite/Audio Systems
  - Rear-Seat Entertainment
  - Touch/Character Recognition
› ADAS Safety
  - TPMS
  - Air Bag
  - Telematics
  - Surround Camera
  - Radar System
› Body Electronics
  - HVAC
  - Gateway
  - Body Control
  - Comfort
  - Lighting

Cypress electronics solutions cover a wide variety of applications inside and outside the automobile cockpit

Cypress’ Automotive Track Record
- A comprehensive portfolio of AEC-Q100-qualified embedded system products
- Over 30 years of experience supporting automotive quality requirements
- Cypress is the third-largest supplier of automotive MCUs and memories
- Cypress has earned preferred supplier status from the Top 25 automotive OEMs

Scalable MXS40 Technology Platform
- High-performance 40-nm process
- Based on single Arm® Cortex®-M4/-M7 and dual Cortex-M7
- Pre-verified IP and core systems improve quality and constancy
- Strong hardware-based security Crypto IP blocks
- Flexible Smart I/O™ interfaces
- Faster, cost-effective, and flexible derivatives
- Script-driven chip implementations
- Proven system software support

¹ Additional resources for Automotive applications and Cypress solutions are available at www.cypress.com/solutions
Traveo II Body Controller Entry
Overview

- Includes Arm® Cortex ®-M4F and M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Automotive systems (such as body control units)
- Features
  - 32-bit CPU subsystem:
    - 160-MHz¹ 32-bit Cortex-M4F CPU with single-cycle multiply, floating-point units (FPU), and memory protection units (MPUs)
    - 100-MHz² 32-bit Cortex-M0+ CPU with MPU
  - CYT2B6: Up to 576KB of Code Flash along with 64KB of Work Flash
  - CYT2B7: Up to 1088KB of Code Flash along with 96KB of Work Flash
  - CYT2B9: Up to 2112KB of Code Flash along with 128KB of Work Flash
  - CYT2BL: Up to 4160KB of Code Flash along with 128KB of Work Flash
  - Dual Bank Mode support for Firmware Over-the-Air (FOTA) for CYT2B7/B9
  - SRAM: CYT2B6: Up to 64KB, CYT2B7: Up to 128KB, CYT2B9: Up to 256KB, CYT2BL: Up to 512KB
  - Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  - Low-power 2.7-5.5-V operation
  - Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support

¹ CYT2B6 up to 80-MHz
² CYT2B6 up to 80-MHz
Overview

› Features (continued)
› AEC-Q100 qualification and ASIL-B level functional safety
› Debugging via SWD/JTAG controller and interface-compliant IEEE-1149.1-2001, and Flash programming on the SWD/JTAG interface
› Packages:
  - 64-/80-/100-/144-/176-LQFP packages available for CYT2B7/B9/BL
  - 64-/80-/100-LQFP packages available for CYT2B6

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CYT2BL Architecture Diagrams:
CPU Subsystem

- CPU Subsystem
- Direct Memory Access (DMA)
- Flash
- SRAM Interface
- Boot (ROM)
- Device Security (Crypto)
CYT2BL Architecture Diagrams: System Resources

- **Power**
  - SWJ/TM/CTI
  - eCT Flash
  - SRAM0/1
  - CRYPTO
  - eFUSE
  - Flash Controller
  - SWJ/MTB/CTI
  - SWJ/ETM/ITM/CTI

- **Clock**
  - IMO
  - FLL
  - PLL
  - 1xPLL
  - 2xILO

- **Reset**
  - XRES
  - POR
  - BOD
  - LVD

- **I/O Subsystem**
  - 1024 bit eFUSE
  - I2C, SPI, UART
  - 1x SCB
  - 8x CANFD
  - 8x CAN
  - 8x LIN
  - 12x LIN

- **CPU Subsystem**
  - Arm Cortex M0+
  - Arm Cortex M4
  - 160 MHz
  - 100 MHz
  - 100 MHz
  - 160 MHz
  - M0+
  - M4
  - M3
  - M1

- **System Interconnect**
  - Multi Layer AHB, IPC, MPU/SMPU
  - initiator/MMIO
  - 8 KB
  - 8 KB

- **SRAM**
  - SRAM0
  - SRAM1
  - SRAM2
  - 256 KB
  - 256 KB
  - 256 KB

- **SRAM Controller**
  - 8 KB
  - 8 KB
  - 8 KB

- **DeepSleep**
  - Hibernate
  - LowPowerActive/Sleep
  - Active/Sleep

- **System Resources**
  - Power Supply and Monitoring
  - Clock System
  - Watchdog Timer
  - Reset System

**Digital DFT**

**Analog DFT**

**System Interconnect**

**Peripheral Interconnect (MMIO, PPU)**

**Power Modes**

002-22190 °C, 2020-12-24

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Traveo II Body Controller High
Overview

› Includes Arm® Dual Cortex®-M7 and M0+ CPUs, manufactured using a high-performance 40-nm process

› Target applications
  – Automotive systems (gateway, high-end body-control units, etc.)

› Features
  – 32-bit CPU subsystem:
    – CYT3BB: One 250-MHz 32-bit Cortex-M7 CPU, with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    – CYT4BB: Two 250-MHz 32-bit Cortex-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    – CYT4BF: Two 350-MHz 32-bit Cortex-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    – 100-MHz 32-bit Cortex-M0+ CPU with MPU
  – CYT3BB/4BB: 4160KB of Code Flash along with 256KB of Work Flash:
  – CYT4BF: 8384KMB of Code Flash along with 256KB of Work Flash:
  – Dual Bank Mode support for Firmware Over-the-Air (FOTA)
  – SRAM: CYT3BB/4BB: 768KB, CYT4BF: 1024KB
  – Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  – Internal (up to 300 mA) power supply: VDDD = 2.7 V to 5.5 V
  – External (up to 600 mA) power supply: VDDD = 2.7 V to 5.5 V and VCCD = 1.15 V (1.1 V to 1.2 V)
Overview

Features (continued)
- Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support
- AEC-Q100 qualification and ASIL-B level functional safety
- Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and Flash programming through SWD/JTAG interface
- Packages:
  - CYT3BB/4BB: 100-/144-/176-TEQFP, 272-FBGA packages available
  - CYT4BF: 176-TEQFP, 272-FBGA, 320-BGA packages available

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CYT4BF Architecture Diagrams:
System Resources

- Power Supply and Monitoring
- Clock System
- Watchdog Timer
- Reset System
CYT4BF Architecture Diagrams: Peripheral Blocks

- SAR ADC
- TCPWM (Timer/Counter/Pulse-Width Modulator)
- Serial Communication Blocks (SCB)
- Local Interconnect Network (LIN)
- CAN FD
- Event Generator
- CXPI
Traveo II Cluster
Overview

› Includes Arm® Dual Cortex®-M7 and M0+ CPUs, manufactured using a high-performance 40-nm process

› Target applications
  – Automotive systems (instrument clusters, head-up displays, etc.)

› Features
  – Graphics Subsystem
    – Supports 2D and 2.5D (perspective warping, 3D effects) graphics rendering
    – Up to 30-bit color resolution (RGB)
    – Embedded video RAM memory (VRAM): CYT3DL: 2048KB, CYT4DN: 4096 KB
    – Up to two video output interfaces supporting two displays
    – One capture engine for video input processing for ITU 656 or parallel RGB/YUV input
  – Audio Subsystem

Review datasheet and TRM chapter 1 for additional details
Overview

**Features**

› 32-bit CPU subsystem:
  - CYT3DL: One 240-MHz 32-bit Cortex-M7 CPU, with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
  - CYT4DN: Two 320-MHz 32-bit Cortex-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
  - 100-MHz 32-bit Cortex-M0+ CPU with MPU

› CYT3DL: 4160KB of Code Flash along with 128KB of Work Flash:
› CYT4DN: 6336KB of Code Flash along with 128KB of Work Flash:
  - Dual Bank Mode support for Firmware Over-the-Air (FOTA)

› SRAM: CYT3DL: 384KB, CYT4DN: 640KB

› Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)

› Power supply rails
  - Internal (up to 300 mA) power supply: VDDD = 2.7 V to 5.5 V
  - External (exceed 300 mA) power supply: VDDD = 2.7 V to 5.5 V and VCCD=1.15 V (1.1 V to 1.2 V)
  - 5.0 V I/O for VDDIO_GPIO, VDDIO_SMC = 2.7 V to 5.5 V
  - 3.3 V I/O for VDDIO_HSIO, VDDIO_SMIF_HV = 3.0 V to 3.6 V
  - 1.8 V I/O for VDDIO_SMIF = 1.7 V to 2.0 V

› Hardware Secure Module (HSM) support

› AEC-Q100 qualification and ASIL-B level functional safety

Review datasheet and TRM chapter 1 for additional details
Overview

Features (continued)

› Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and Flash programming through SWD/JTAG interface

› Packages:
  - CYT3DL: 208-/216-TEQFP, 272-BGA packages available
  - CYT4DN: 327-/500-BGA packages available
CYT4DN Architecture Diagrams:

CPU Subsystem

- CPU Subsystem
- Direct Memory Access (DMA)
- Flash
- SRAM Interface
- Boot (ROM)
- Device Security (Crypto)
CYT4DN Architecture Diagrams: System Resources

- Power Supply and Monitoring
- Clock System
- Watchdog Timer
- Reset System
CYT4DN Architecture Diagrams: Peripheral Blocks

- TCPWM (Timer/Counter/Pulse-Width Modulator)
- Serial Communication Blocks (SCB)
- Local Interconnect Network (LIN)
- CAN FD
- Event Generator
- Ethernet
- Audio SS
- SMIF
- Graphics
CYT4DN Architecture Diagrams:
I/O Subsystem

CPU Subsystem
- Cortex M7 320 MHz
- eCT FLASH 6336 KB Code-flash + 128 KB Work-flash
- SRAM0 256 KB
- SRAM1 256 KB
- SRAM2 128 KB
- PMU
- CRYPTO AES, SHA, CRC, TRNG, RSA, ECC
- Cortex M0+ 100 MHz
- ROM 64 KB

System Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPU)

Peripheral Interconnect (MMIO/PPU)
- Board Control
- Power
- Clock
- I2C
- SPI
- UART
- LIN

System Resources
- Power
- Clock
- Reset
- Test

Power Modes
- Active/Sleep
- Low Power
- Standby

GFX Subsystem
- GFX Interconnect (AXI)
- VRAM Interface

GFX Interconnect (AXI)
- 1x RGB/MIPI Input
- 2x RGB/LVDS Output
- 2x HDMI Outputs
- 4x DVI Outputs

GFX Subsystem
- AVR Interface
- EV Gen Interface
- Event Gen Interface
- ESC Interface
- SARMUX 48 ch
- 2.5D Engine
- 4096 KB VRAM
- 4096 KB VRAM Interface

I/O Subsystem
- High Speed I/O Matrix
- Smart I/O
- Boundary Scan
- DeepSleep
- Hibernate
- Power Modes
- 2x SARMUX 48 ch
- 2x SDIO
- 2x CAN
- 4x CANFD

System Resources
- Power
- Clock
- Reset
- Test

Power Modes
- Active/Sleep
- Low Power
- Standby
Appendix

Comparison between CYT2B, CYT4B, and CYT4D
## Feature Comparison between CYT2B/CYT4B/CYT4D (1/4)

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2B</th>
<th>CYT4B</th>
<th>CYT4D</th>
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<tbody>
<tr>
<td><strong>CPU Subsystem</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Main CPU</td>
<td>Cortex-M4 CPU</td>
<td>Two Cortex-M7 CPUs</td>
<td></td>
</tr>
<tr>
<td>FPU</td>
<td>Single-precision</td>
<td>Single/double-precision</td>
<td></td>
</tr>
<tr>
<td>Cache</td>
<td>-</td>
<td>16 KB instruction, 16 KB data</td>
<td></td>
</tr>
<tr>
<td>MPU</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>System Tick Timer</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Inter-Processor Communication (IPC)</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Protection Unit</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Direct Memory Access</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td><strong>Flash</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus interface</td>
<td>AHB-Lite</td>
<td>AXI, AHB-Lite</td>
<td></td>
</tr>
<tr>
<td>ECC (SEC/DED)</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Bank modes</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td><strong>SRAM Interface</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus interface</td>
<td>AHB-Lite</td>
<td>AXI, AHB-Lite</td>
<td></td>
</tr>
<tr>
<td>ECC (SEC/DED)</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>TCM</td>
<td>N/A</td>
<td>16 KB ITCM, 16 KB DTCM</td>
<td>64 KB ITCM, 64 KB DTCM</td>
</tr>
<tr>
<td>Boot</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Interrupts</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Device Security with Crypto</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Chip Operational Modes</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Fault Subsystem</td>
<td>Same</td>
<td>Same</td>
<td></td>
</tr>
</tbody>
</table>
## Feature Comparison between CYT2B/CYT4B/CYT4D (2/4)

<table>
<thead>
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<th>Features</th>
<th>CYT2B</th>
<th>CYT4B</th>
<th>CYT4D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Supply and Monitoring</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply</td>
<td>$V_{DDD} = 2.7 \text{ V to } 5.5 \text{ V}$</td>
<td>$V_{DDD} = 2.7 \text{ V to } 5.5 \text{ V (up to 300 mA)}$</td>
<td>$V_{DDD} = 2.7 \text{ V to } 5.5 \text{ V and } V_{CCD} = 1.15 \text{ V (exceeds 300 mA)}$</td>
</tr>
<tr>
<td>5.0 V I/O power supply</td>
<td>$V_{DDIO,1}, V_{DDIO,2}$</td>
<td></td>
<td>$V_{DDIO.GPIO}, V_{DDIO.SMC}$</td>
</tr>
<tr>
<td>3.3 V I/O power supply</td>
<td>N/A</td>
<td>$V_{DDIO,3}, V_{DDIO,4}$</td>
<td>$V_{DDIO.HBIO}, V_{DDIO.SMIC}, H/V$</td>
</tr>
<tr>
<td>1.8 V I/O power supply</td>
<td>N/A</td>
<td></td>
<td>$V_{DDIO.SMIC}$</td>
</tr>
<tr>
<td>Analog power supply</td>
<td>$V_{DDA}$</td>
<td></td>
<td>$V_{DDA.ADC}, V_{DDA.DAC}, V_{DDA.MPI}, V_{DDA.FPD0}, V_{DDA.FPD1}, V_{DDA.HSIO}, V_{DDA.SMIC}, H/V$</td>
</tr>
<tr>
<td>Active/DeepSleep regulator</td>
<td>Same</td>
<td></td>
<td>Same</td>
</tr>
<tr>
<td>External transistor control</td>
<td>N/A</td>
<td>Available</td>
<td>N/A</td>
</tr>
<tr>
<td>External PMIC control</td>
<td>N/A</td>
<td>Available</td>
<td></td>
</tr>
<tr>
<td>BOD/OVD/LVD</td>
<td>Same</td>
<td></td>
<td>Same</td>
</tr>
<tr>
<td><strong>Device Power Modes</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal clock sources (IMO, ECO)</td>
<td>Same</td>
<td></td>
<td>Support LPECO</td>
</tr>
<tr>
<td>External clock sources (ECO, WCO, EXT_CLK)</td>
<td>Same</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLL</td>
<td>Same</td>
<td></td>
<td>Same</td>
</tr>
<tr>
<td>PLL without SSCG and fractional operation</td>
<td>Same</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLL with SSCG and fractional operation</td>
<td>N/A</td>
<td>Available</td>
<td></td>
</tr>
<tr>
<td>Clock supervision (CSV)</td>
<td>Same</td>
<td></td>
<td>Same</td>
</tr>
<tr>
<td>Clock calibration counter</td>
<td>Same</td>
<td></td>
<td>Same</td>
</tr>
<tr>
<td><strong>Reset System</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Same</td>
</tr>
</tbody>
</table>
# Feature Comparison between CYT2B/CYT4B/CYT4D (3/4)

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2B</th>
<th>CYT4B</th>
<th>CYT4D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog Timer</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Real Time Clock</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td><strong>I/O System</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO input modes (CMOS/TTL/Automotive)</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Eight output drive modes</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Drive strength (Full, 1/2, 1/4)</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Slew rate control (only for GPIO_ENH)</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>GPIO interrupt</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>GPIO SMC</td>
<td>N/A</td>
<td>N/A</td>
<td>Available</td>
</tr>
<tr>
<td>High-speed I/O</td>
<td>N/A</td>
<td>Available (HSIO_STD)</td>
<td>Available (HSIO_STD, HSIO_ENH, HSIO_ENH_DIFF)</td>
</tr>
<tr>
<td><strong>CAN FD</strong></td>
<td></td>
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<tr>
<td>Serial Communications Block</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>TCPWM</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>LIN</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Event Generator</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>Trigger Multiplexer</td>
<td></td>
<td>Same</td>
<td></td>
</tr>
<tr>
<td>FlexRay</td>
<td>N/A</td>
<td>Available</td>
<td>N/A</td>
</tr>
<tr>
<td>Ethernet MAC</td>
<td>N/A</td>
<td>Available</td>
<td>Available</td>
</tr>
</tbody>
</table>
## Feature Comparison between CYT2B/CYT4B/CYT4D (4/4)

<table>
<thead>
<tr>
<th>Features</th>
<th>CYT2B</th>
<th>CYT4B</th>
<th>CYT4D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Memory Interface</td>
<td>N/A</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>SDHC Host Controller</td>
<td>N/A</td>
<td>Available</td>
<td>-</td>
</tr>
<tr>
<td>Audio Subsystem</td>
<td>N/A</td>
<td>Available</td>
<td>N/A</td>
</tr>
<tr>
<td>Sound Subsystem</td>
<td>N/A</td>
<td>N/A</td>
<td>Available</td>
</tr>
<tr>
<td>Graphics Subsystem</td>
<td>N/A</td>
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<td>SAR ADC</td>
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Part of your life. Part of tomorrow.
### Revision History

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<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<td>**</td>
<td>6097587</td>
<td>09/03/2018</td>
<td>Initial release</td>
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<td>*A</td>
<td>6401071</td>
<td>12/04/2018</td>
<td>Added CYT2B9 and CYT4BF</td>
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<td>Updated the Block Diagram</td>
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<td>*B</td>
<td>6682714</td>
<td>09/26/2019</td>
<td>Updated title to include cluster</td>
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<td>Updated CM0+ frequency from 80 MHz to 100 MHz</td>
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<td>Added CYT4DN (page 17 to 23, 34 to 38)</td>
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<td>Updated Functional Overview in Appendix</td>
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<td>7053676</td>
<td>12/24/2020</td>
<td>Updated page 2, 5 to 10, 12, 13, 19, 20, 21</td>
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