Customer Training Workshop Traveo™ II Audio Digital Analog Converter

Q4 2020

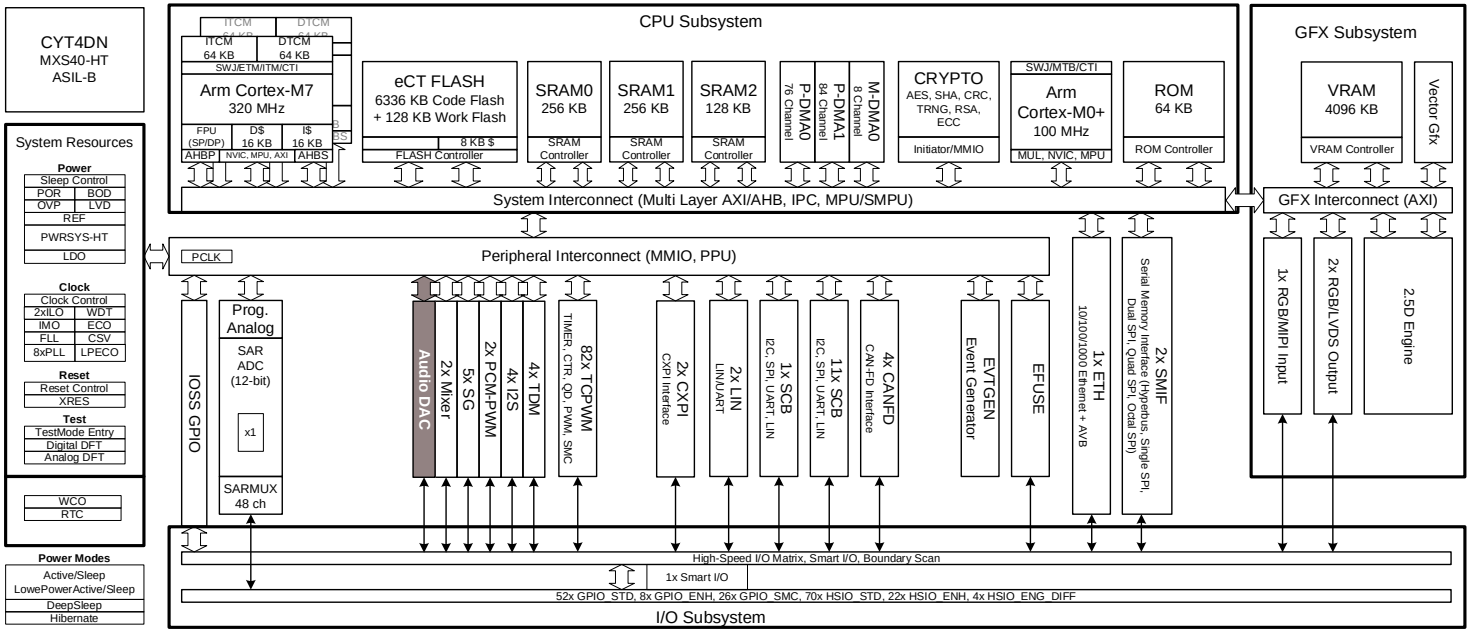
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo™ II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Cluster

The Audio DAC is part of Peripheral blocks



Hint Bar

Review TRM chapter 33 for additional details

Audio DAC Overview

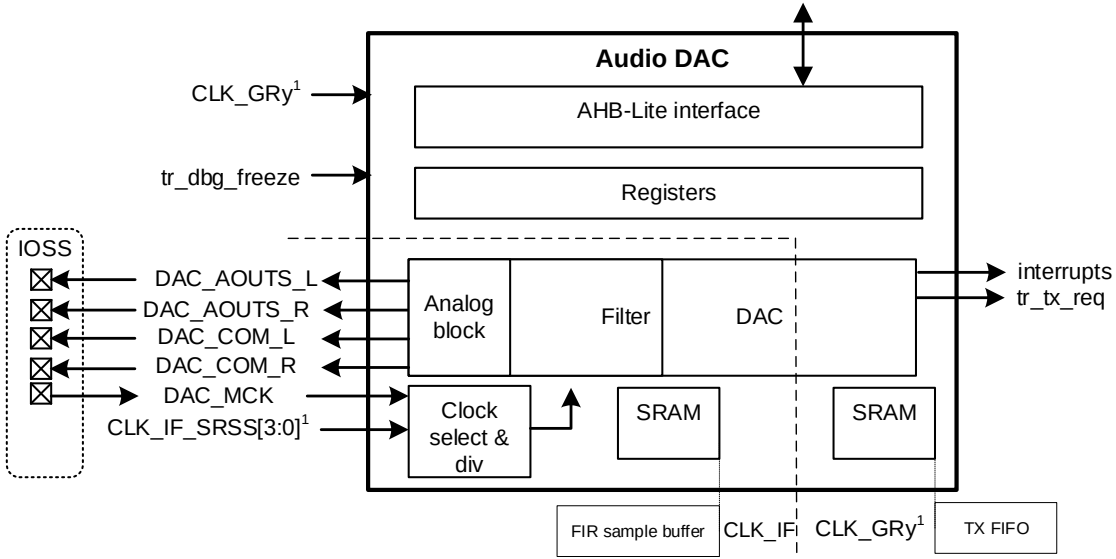
- Audio digital-to-analog converter (DAC) converts the PCM data to analog and drives to both left and right pins respectively
- Features
  - Programmable sampling rate (from 8 kHz to up to 48 kHz) and frequency control
  - 64 entry TX FIFOs with interrupt and trigger support
  - Two 16-bit PCM data each for left and right to form a stereo
  - Cascaded Integrated-Comb (CIC) filter, Finite Impulse Response (FIR) filter, Interpolation filter, and delta-sigma modulator (DSM)
  - Test mode for analog block

Hint Bar

Review TRM section 33.6 for additional details

Audio DAC Block Diagram

- Audio DAC components
  - Clock
  - TX FIFO
  - DAC core



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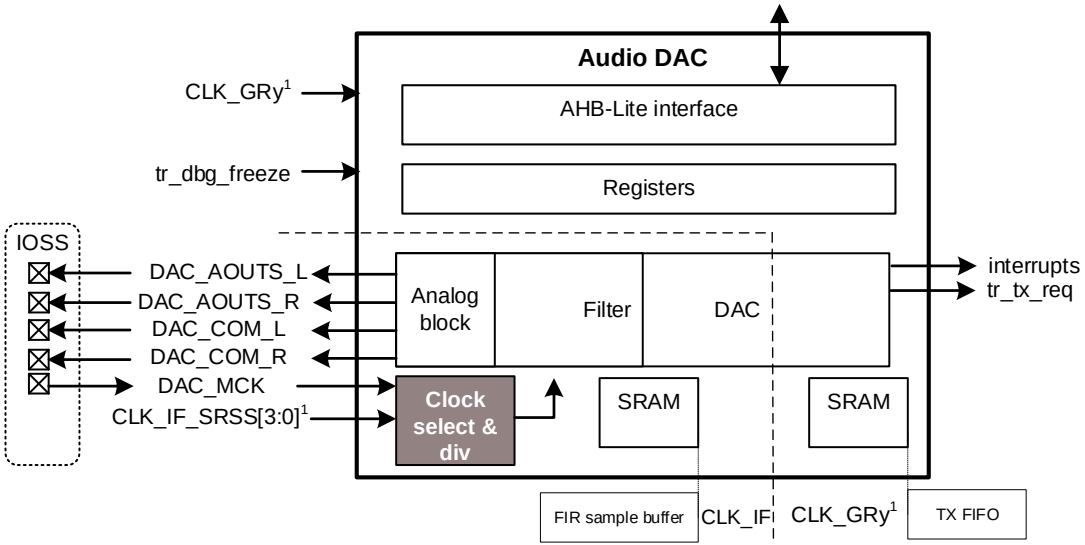
Review TRM section 33.6.2 for additional details

[1] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

Audio DAC Components - Clock

- Clock
  - Clock Selection and Divider
  - Oversampling Rate



Hint Bar

Review TRM section 33.6.3 for additional details

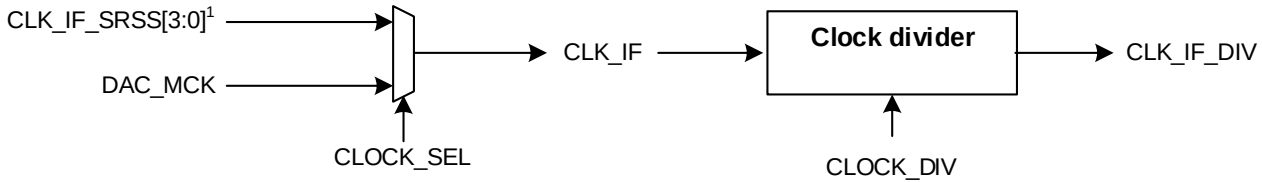
[1] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

Clock Selection and Divider

- PWM interface clock can be derived from one of these clock signals

Signal	Description
CLK_IF_SRSS[3:0][1]	One of the SRSS clocks
DAC_MCK	External master clock

- The divided clock will be used as the DAC core system clock



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Review TRM section 33.6.3 for additional details

Review the Clock System Training section for additional details about high-frequency clocks

DAC core system clock frequency is the function of CLK_IF/(CLOCK_DIV+1)

[1] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0]

Oversampling Rate

- System clock frequency can be used to perform oversampling on the DAC components to achieve the required sampling rate (Fs)
- Recommended Fs with system clock frequency configuration

FS_SEL	OSR	System Clock Frequency	Fs (kHz)
01	128	256 x Fs	32, 44.1, 48
10	256	256 x Fs	16, 22.05, 24
11	512	512 x Fs	8, 11.05, 12, 12.8

Hint Bar

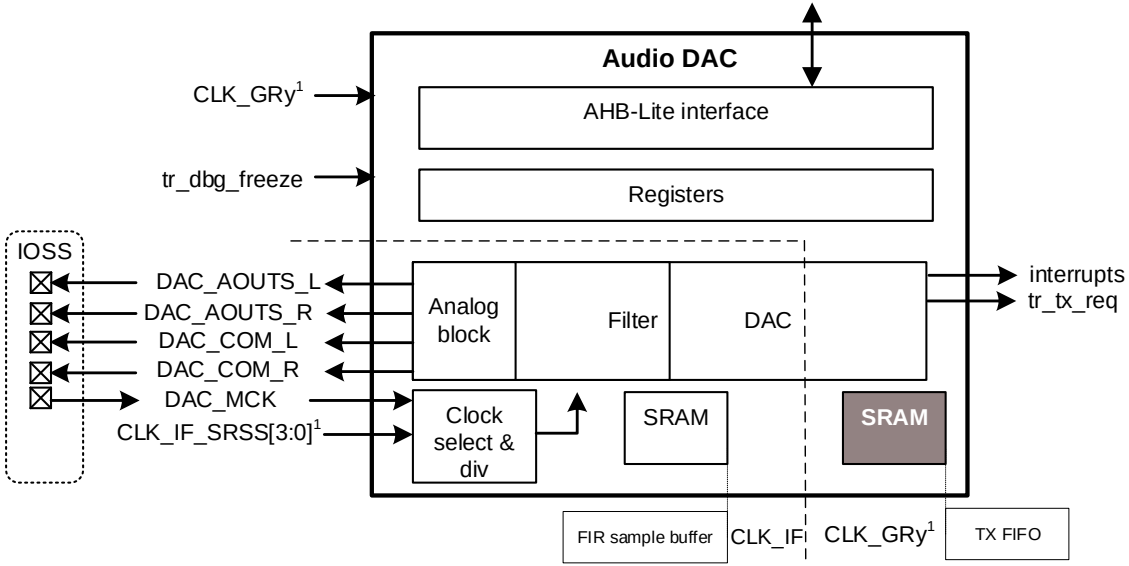
Review TRM section 33.6.3 for additional details

Fs and system clock can only be configured when there is no in-flight PCM data, and DAC_BUSY = 0 before the start of DAC use

FS_SEL: Sample frequency select

Audio DAC Components – TX FIFO

- Audio DAC components
  - TX FIFO



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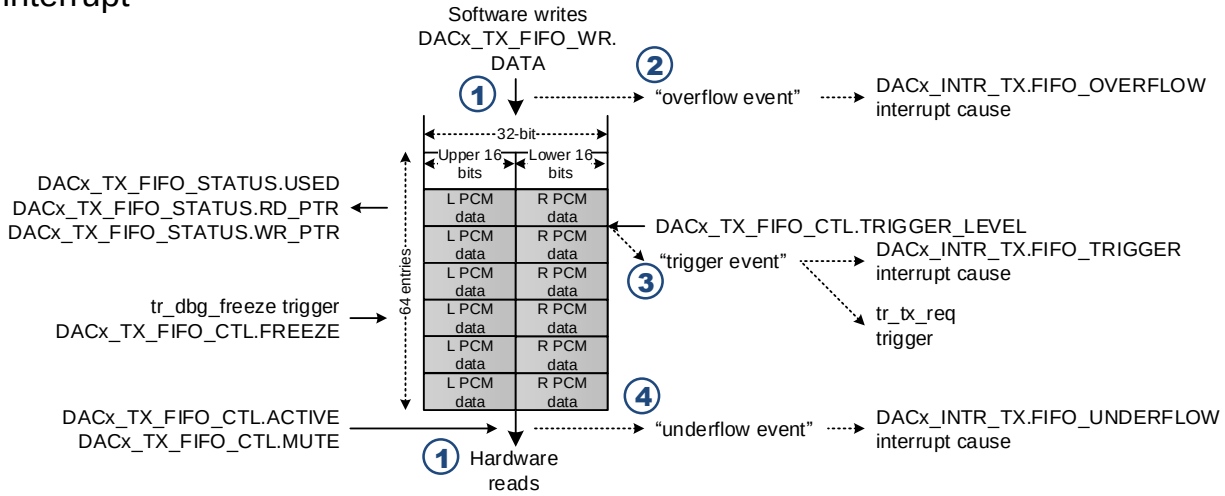
Review TRM section 33.6.5 for additional details

[1] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

TX FIFO Operation

- TX FIFO operation follows these steps:
  1. SW writes to TX FIFO and HW reads from TX FIFO to transfer PCM data to DAC core
  2. When SW writes to a full TX FIFO, HW sets INTR_TX.FIFO_OVERFLOW interrupt
  3. When TX_FIFO_STATUS.USED < TX_FIFO_CTL.TRIGGER_LEVEL, HW sets tx_tx_req trigger and INTR_TX.FIFO_TRIGGER interrupt
  4. When HW reads from an empty FIFO, HW sets INTR_TX.FIFO_UNDERFLOW interrupt



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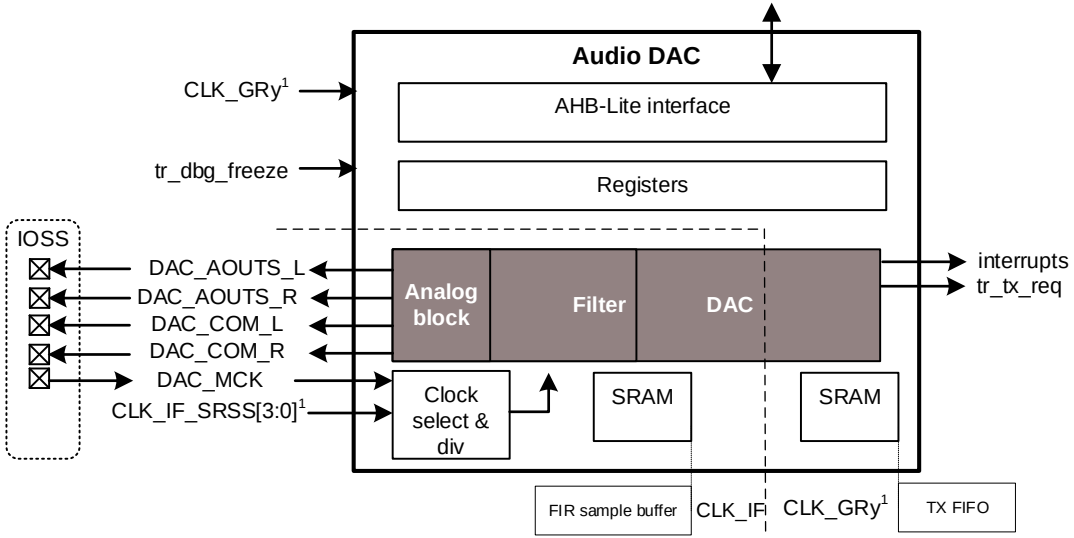
Review TRM section 33.6.5 for additional details

Review the Registers TRM for additional details

Audio DAC Components – DAC Core

- DAC Core
  - Test mode



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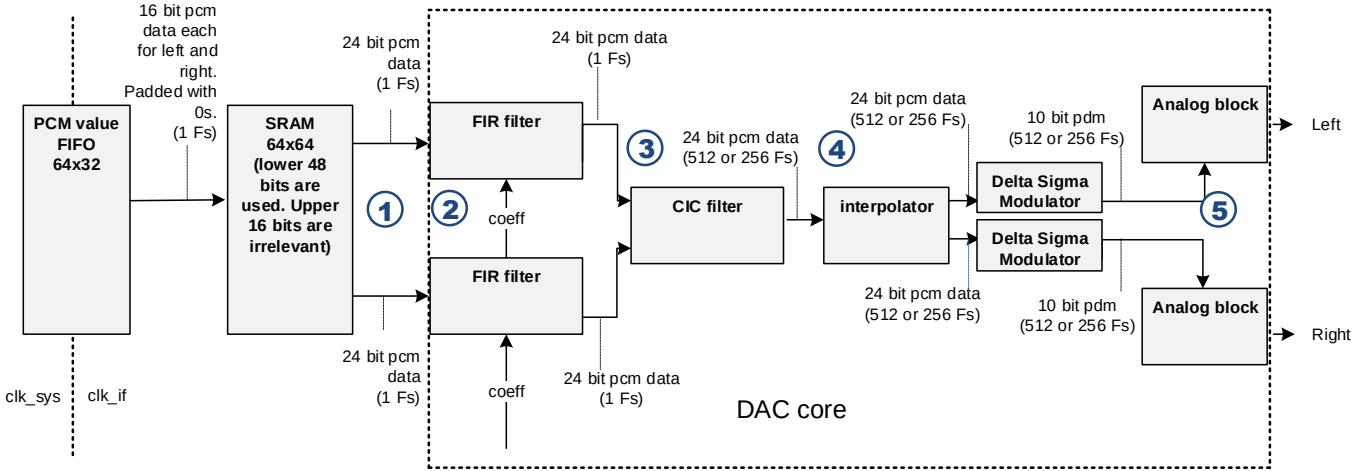
Review TRM section 33.6.4 for additional details

[1] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

DAC Core Process

DAC processing path

1. Audio DAC receives the processed two-channel data from TX FIFO
2. The data goes through the FIR filter with a series of delays, multiplier, and adder
3. The data is fed through the CIC filter with comb-type filters and integral filters
4. The interpolator converts PCM data to PDM bitstream and feeds it to DSM for noise shaping
5. Output of the DSM drives the multi-level DAC after synchronization and level shifting



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Review TRM section 33.6.4 for additional details

The processing of the FIR filter, CIC filter, interpolator, and DSM cannot be configured by the user

Review the Appendix section for additional details about FIR filter, CIC filter, and Delta-Sigma Modulator (DSM)

Noise shaping increases the apparent S/N ratio of the resultant signal by lowering the noise present in the audible range and increasing the noise above the audible range

Test Mode

- Test mode for analog block (TEST_CTL.TEST_MODE_EN = 1)
  - Analog block's input is connected to TEST_ANALOG_DATA.TEST_ANALOG_DATAIN

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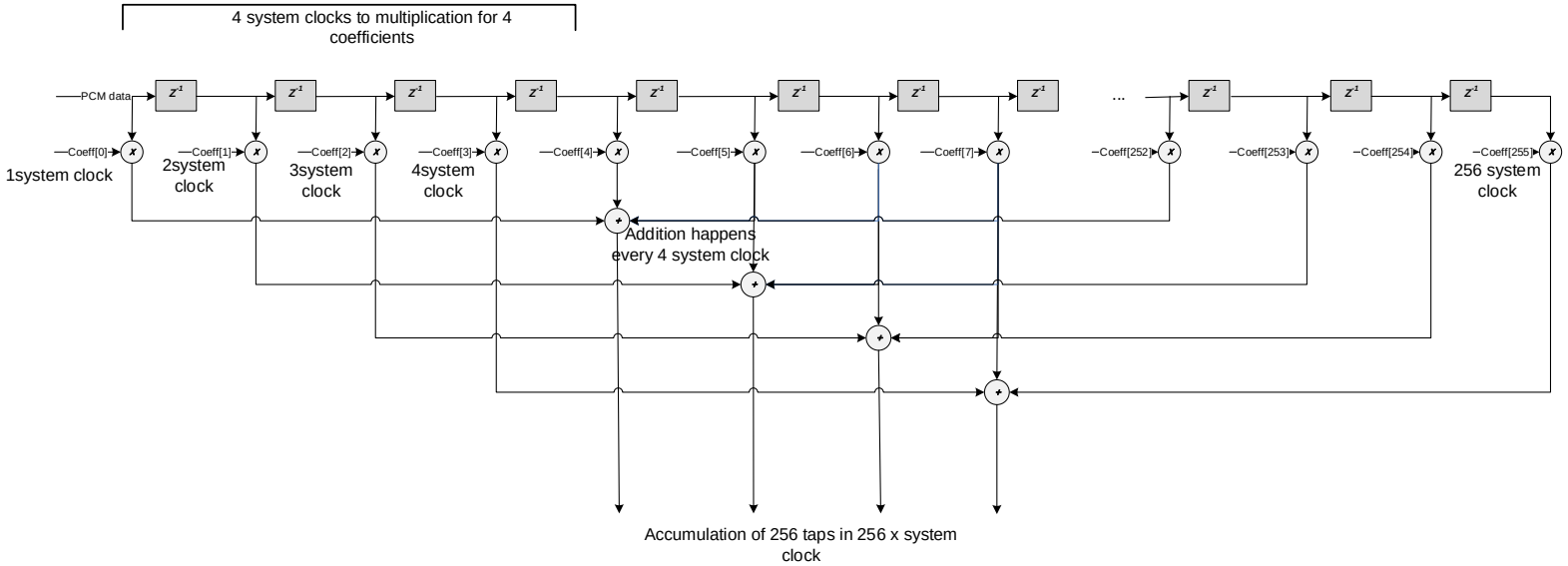
Review TRM section 33.6.8 for additional details

Review the Appendix section for additional details about the analog block

Appendix

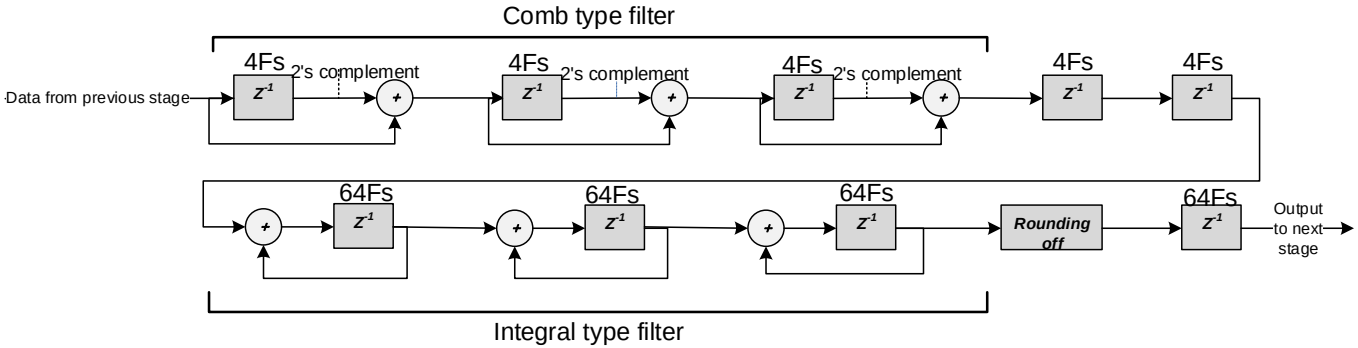
FIR Filter

- FIR filter in DAC core
  - Coefficient multiplication of 256 TAPs is carried with one multiplier
  - Four multiplications are performed for one sample value with system clock/4 frequency (64 Fs)
  - Result of the multiplication is accumulated in every system clock/4 frequency (64 Fs), which equals to 64 TAP multiplications of 4 (4 x 64) = 256 TAPs being executed



CIC Filter

- CIC filter in DAC core
  - First three stages: Comb-type filter
    - Operates at system clock/64 (4 Fs)
  - Last three stages: Integral-type filter
    - Operates at system clock/4 (64 Fs)
  - CIC-Interpolation is sequentially connected and outputs in 256 Fs rate



- Advantage
  - Has anti-aliasing and oversampling role

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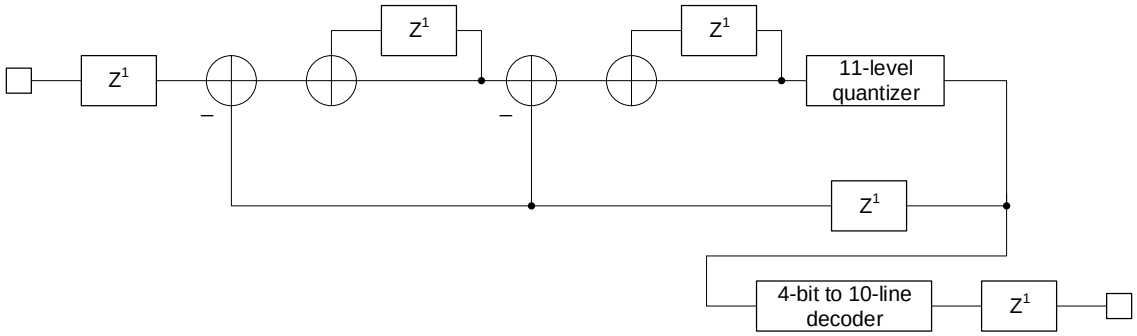
Review TRM section 33.6.4 for additional details

Cascaded Integrated-Comb (CIC)

Delta-Sigma Modulator (1/2)

- CIDF delta-sigma modulation circuit
  - Set the quantizer to 11-level
    - Quantization noise in passband is reduced by more than 1-bit delta-sigma configuration
  - Decode 11-level (4-bit) to 10-line (weight is equal to 1)
  - Drive analog DAC block with PDM waveform



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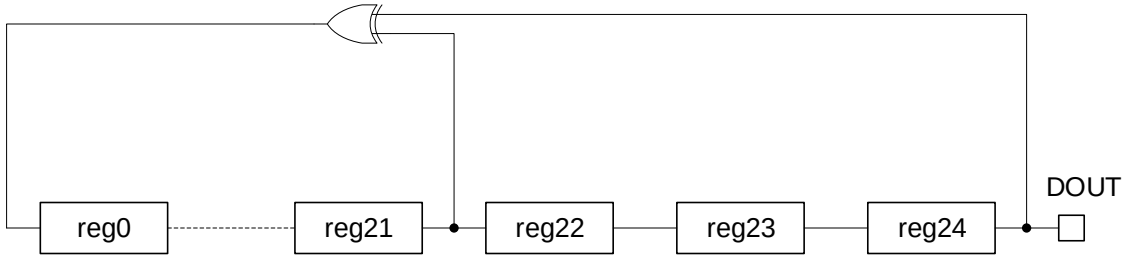
Review TRM section 33.6.4 for additional details

Pulse density modulation (PDM)

Delta-Sigma Modulator (2/2)

- Dynamic Element Matching
  - Averages the output voltage by sequentially changing the elements at the “High” level
    - To reduce the influence of the relative error that can increase noise and distortion
- Dithering
  - Suppresses idle tone generation
  - Is added before DSM to improve S/N ratio



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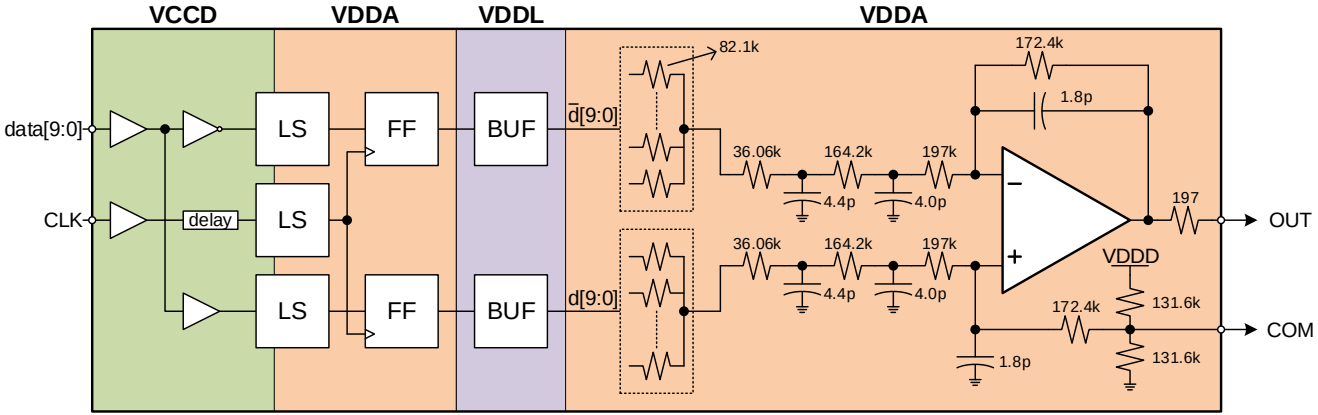
Review TRM section 33.6.4 for additional details

Signal-to-noise ratio (S/N ratio)

Analog Block

- Output of the DSM passes through LSs, FFs, and BUFs, and finally drives the DAC input resistors
- DAC resistors are summed at the input of opamp
- An active third-order LPF with cut-off frequency of 90 kHz is used
  - To filter high-frequency quantization noise
  - To provide low-impedance drive



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Review TRM section 33.6.4 for additional details

Level-shifter (LS)

Flip-flop (FF)

Logic buffer (BUF)

Low-pass filter (LPF)

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6638977	07/29/2019	Initial release
*A	6805412	02/12/2020	Added note descriptions in each slide
*B	7052598	12/21/2020	Updated 2, 5, 6, 7, 9, 11