Customer training workshop
TRAVEO™ T2G audio digital-analog converter
Target products

- Target product list for this training material

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRAVEO™ T2G Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
<tr>
<td>TRAVEO™ T2G Automotive Cluster</td>
<td>CYT4EN</td>
<td>Up to 6336 KB</td>
</tr>
</tbody>
</table>
Introduction to TRAVEO™ T2G Cluster

› The Audio DAC is part of peripheral blocks
Audio DAC overview

- Audio digital-to-analog converter (DAC) converts the PCM data to analog and drives to both left and right pins respectively.

- Features
  - Programmable sampling rate (from 8 kHz to up to 48 kHz) and frequency control
  - 64 entry TX FIFOs with interrupt and trigger support
  - Two 16-bit PCM data each for left and right to form a stereo
  - Cascaded Integrated-Comb (CIC) filter, Finite Impulse Response (FIR) filter, Interpolation filter, and delta-sigma modulator (DSM)

Hint Bar

Review TRM section 34.6 for additional details
Audio DAC block diagram

Audio DAC components
- Clock
- TX FIFO
- DAC core

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

Review TRM section 34.6.2 for additional details
Audio DAC components - Clock

- Clock selection and divider
- Oversampling rate

Hint Bar

Review TRM section 34.6.3 for additional details

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

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Clock selection and divider

- PWM interface clock can be derived from one of these clock signals
  - CLK_IF_SRSS[3:0]: One of the SRSS clocks
  - DAC_MCK: External master clock

- The divided clock will be used as the DAC core system clock

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**Signal Description**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_IF_SRSS[3:0]</td>
<td>One of the SRSS clocks</td>
</tr>
<tr>
<td>DAC_MCK</td>
<td>External master clock</td>
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</tbody>
</table>

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0]
Oversampling rate

- System clock frequency can be used to perform oversampling on the DAC components to achieve the required sampling rate \((F_s)\).
- Recommended \(F_s\) with system clock frequency configuration

<table>
<thead>
<tr>
<th>FS_SEL</th>
<th>OSR</th>
<th>System Clock Frequency</th>
<th>(F_s) (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>128</td>
<td>256 (\times F_s)</td>
<td>32, 44.1, 48</td>
</tr>
<tr>
<td>10</td>
<td>256</td>
<td>256 (\times F_s)</td>
<td>16, 22.05, 24</td>
</tr>
<tr>
<td>11</td>
<td>512</td>
<td>512 (\times F_s)</td>
<td>8, 11.05, 12, 12.8</td>
</tr>
</tbody>
</table>

Hint Bar

Review TRM section 34.6.3 for additional details.

\(F_s\) and system clock can only be configured when there is no in-flight PCM data, and \(DAC\_BUSY = 0\) before the start of DAC use.

FS_SEL: Sample frequency select
Audio DAC components – TX FIFO

Audio DAC components
- TX FIFO

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy
TX FIFO operation

TX FIFO operation follows these steps:

1. SW writes to TX FIFO and HW reads from TX FIFO to transfer PCM data to DAC core
2. When SW writes to a full TX FIFO, HW sets INTR_TX.FIFO_OVERFLOW interrupt
3. When TX_FIFO_STATUS.USED < TX_FIFO_CTL.TRIGGER_LEVEL, HW sets tx_tx_req trigger and INTR_TX.FIFO_TRIGGER interrupt
4. When HW reads from an empty FIFO, HW sets INTR_TX.FIFO_UNDERFLOW interrupt

Review TRM section 34.6.6 for additional details
Review the Registers TRM for additional details
Audio DAC components – DAC core

Audio DAC components
  - DAC core

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_Gry

Hint Bar
Review TRM section 34.6.5 for additional details
DAC core process

DAC processing path

1. Audio DAC receives the processed two-channel data from TX FIFO
2. The data goes through the FIR filter with a series of delays, multiplier, and adder
3. The data is fed through the CIC filter with comb-type filters and integral filters
4. The interpolator converts PCM data to PDM bitstream and feeds it to DSM for noise shaping
5. Output of the DSM drives the multi-level DAC after synchronization and level shifting

Noise shaping increases the apparent S/N ratio of the resultant signal by lowering the noise present in the audible range and increasing the noise above the audible range
Appendix
FIR filter in DAC core
- Coefficient multiplication of 256 TAPs is carried with one multiplier
- Four multiplications are performed for one sample value with system clock/4 frequency (64 Fs)
- Result of the multiplication is accumulated in every system clock/4 frequency (64 Fs), which equals to 64 TAP multiplications of 4 (4 x 64) = 256 TAPs being executed
CIC Filter

- **CIC filter in DAC core**
  - First three stages: Comb-type filter
    - Operates at system clock/64 (4 Fs)
  - Last three stages: Integral-type filter
    - Operates at system clock/4 (64 Fs)
  - CIC-Interpolation is sequentially connected and outputs in 256 Fs rate

- **Advantage**
  - Has anti-aliasing and oversampling role

**Diagram**

Comb type filter:
- Data from previous stage
- 4Fs 2's complement
- 4Fs 2's complement
- 4Fs 2's complement
- 4Fs 2's complement
- Output to next stage

Integral type filter:
- 64Fs
- 64Fs
- 64Fs
- Rounding
- 64Fs

**Hint Bar**

Review TRM section 34.6.5 for additional details

Cascaded Integrated-Comb (CIC)
Delta-sigma modulator (1/2)

- CIDF delta-sigma modulation circuit
  - Set the quantizer to 11-level
    - Quantization noise in passband is reduced by more than 1-bit delta-sigma configuration
  - Decode 11-level (4-bit) to 10-line (weight is equal to 1)
  - Drive analog DAC block with PDM waveform

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Z^1
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Review TRM section 34.6.5 for additional details

Pulse density modulation (PDM)
Delta-Sigma Modulator (2/2)

› Dynamic Element Matching
  − Averages the output voltage by sequentially changing the elements at the “High” level
    − To reduce the influence of the relative error that can increase noise and distortion

› Dithering
  − Suppresses idle tone generation
  − Is added before DSM to improve S/N ratio

DOUT

Hint Bar
Review TRM section 34.6.5 for additional details
Signal-to-noise ratio (S/N ratio)
Analog block

- Output of the DSM passes through LSs, FFs, and BUFs, and finally drives the DAC input resistors
- DAC resistors are summed at the input of opamp
- An active third-order LPF with cut-off frequency of 90 kHz is used
  - To filter high-frequency quantization noise
  - To provide low-impedance drive

Hint Bar

- Review TRM section 34.6.5 for additional details
- Level-shifter (LS)
- Flip-flop (FF)
- Logic buffer (BUF)
- Low-pass filter (LPF)
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## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<tbody>
<tr>
<td>**</td>
<td>6638977</td>
<td>2019/07/29</td>
<td>Initial release</td>
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<tr>
<td>*A</td>
<td>6805412</td>
<td>2020/02/12</td>
<td>Added note descriptions in each slide</td>
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<tr>
<td>*B</td>
<td>7052598</td>
<td>2020/12/21</td>
<td>Updated 2, 5, 6, 7, 9, 11</td>
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<tr>
<td>*C</td>
<td>7799385</td>
<td>2022/08/17</td>
<td>Updated 1 to 6, 9, 11. Removes the Test mode.</td>
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