Target Products

Target product list for this training material

<table>
<thead>
<tr>
<th>Family Category</th>
<th>Series</th>
<th>Code Flash Memory Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traveo™ II Automotive Cluster</td>
<td>CYT3DL</td>
<td>Up to 4160KB</td>
</tr>
<tr>
<td>Traveo™ II Automotive Cluster</td>
<td>CYT4DN</td>
<td>Up to 6336KB</td>
</tr>
</tbody>
</table>
Introduction to Traveo II Cluster

The Audio DAC is part of Peripheral blocks

CPU Subsystem

- Arm Cortex-M7
- 320 MHz
- 636 KB Code Flash
- 128 KB Work Flash
- SRAM0: 256 KB
- SRAM1: 256 KB
- SRAM2: 128 KB
- PRAM: 512 KB
- P-RAM: 256 KB
- PRAM: 256 KB
- M-RAM: 512 KB
- P-Daim
- M-Daim
- CRYPTO: AES, SHA, CRC, TRNG, RSA, ECC
- INIT: MMIO
- ROM: 64 KB
- Battery Backup

Peripheral Interconnect (MMIO, PPU)

- PCLK
- 52x GPIO_STD, 8x GPIO_ENH, 26x GPIO_SMC, 70x HSIO_STD, 22x HSIO_ENH, 4x HSIO_ENG_DIFF

GFX Subsystem

- eCT FLASH
- 636 KB Code Flash
- 128 KB Work Flash
- SRAM0: 256 KB
- SRAM1: 256 KB
- SRAM2: 128 KB
- PRAM: 512 KB
- P-RAM: 256 KB
- PRAM: 256 KB
- M-RAM: 512 KB
- P-Daim
- M-Daim
- CRYPTO: AES, SHA, CRC, TRNG, RSA, ECC
- INIT: MMIO
- ROM: 64 KB
- Battery Backup

Peripheral Interconnect (Multi Layer AXI/AHB, IPC, MPU/SMPI)

- SRAM
- Init MMIO
- Battery Backup

Review TRM chapter 33 for additional details
Audio DAC Overview

› Audio digital-to-analog converter (DAC) converts the PCM data to analog and drives to both left and right pins respectively

› Features
  – Programmable sampling rate (from 8 kHz to up to 48 kHz) and frequency control
  – 64 entry TX FIFOs with interrupt and trigger support
  – Two 16-bit PCM data each for left and right to form a stereo
  – Cascaded Integrated-Comb (CIC) filter, Finite Impulse Response (FIR) filter, Interpolation filter, and delta-sigma modulator (DSM)
  – Test mode for analog block
Audio DAC Block Diagram

- Audio DAC components
  - Clock
  - TX FIFO
  - DAC core

¹ See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy
Audio DAC Components - Clock

- Clock
  - Clock Selection and Divider
  - Oversampling Rate

See the device datasheet for assigned clocks to \( \text{CLK}_{\text{IF}} \text{SRSS}[3:0] \) and \( \text{CLK}_{\text{GRy}} \)

1 See the device datasheet for assigned clocks to \( \text{CLK}_{\text{IF}} \text{SRSS}[3:0] \) and \( \text{CLK}_{\text{GRy}} \)
Clock Selection and Divider

- PWM interface clock can be derived from one of these clock signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_IF_SRSS[3:0]</td>
<td>One of the SRSS clocks</td>
</tr>
<tr>
<td>DAC_MCK</td>
<td>External master clock</td>
</tr>
</tbody>
</table>

- The divided clock will be used as the DAC core system clock

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0]

Hint Bar

Review TRM section 33.6.3 for additional details

Review the Clock System Training section for additional details about high-frequency clocks

DAC core system clock frequency is the function of \( \frac{\text{CLK}_{\text{IF}}}{(\text{CLOCK}_{\text{DIV}}+1)} \)
Oversampling Rate

- System clock frequency can be used to perform oversampling on the DAC components to achieve the required sampling rate (Fs).
- Recommended Fs with system clock frequency configuration

<table>
<thead>
<tr>
<th>FS_SEL</th>
<th>OSR</th>
<th>System Clock Frequency</th>
<th>Fs (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>128</td>
<td>256 x Fs</td>
<td>32, 44.1, 48</td>
</tr>
<tr>
<td>10</td>
<td>256</td>
<td>256 x Fs</td>
<td>16, 22.05, 24</td>
</tr>
<tr>
<td>11</td>
<td>512</td>
<td>512 x Fs</td>
<td>8, 11.05, 12, 12.8</td>
</tr>
</tbody>
</table>

FS_SEL: Sample frequency select

Review TRM section 33.6.3 for additional details

Fs and system clock can only be configured when there is no in-flight PCM data, and DAC_BUSY = 0 before the start of DAC use.
Audio DAC Components – TX FIFO

Audio DAC components
- TX FIFO

See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy.
TX FIFO Operation

TX FIFO operation follows these steps:

1. SW writes to TX FIFO and HW reads from TX FIFO to transfer PCM data to DAC core
2. When SW writes to a full TX FIFO, HW sets INTR_TX.FIFO_OVERFLOW interrupt
3. When TX_FIFO_STATUS.USED < TX_FIFO_CTL.TRIGGER_LEVEL, HW sets tx_tx_req trigger and INTR_TX.FIFO_TRIGGER interrupt
4. When HW reads from an empty FIFO, HW sets INTR_TX.FIFO_UNDERFLOW interrupt

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Hint Bar

Review TRM section 33.6.5 for additional details
Review the Registers TRM for additional details
Audio DAC Components – DAC Core

› DAC Core
  – Test mode

1 See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy
DAC Core Process

DAC processing path

1. Audio DAC receives the processed two-channel data from TX FIFO.
2. The data goes through the FIR filter with a series of delays, multiplier, and adder.
3. The data is fed through the CIC filter with comb-type filters and integral filters.
4. The interpolator converts PCM data to PDM bitstream and feeds it to DSM for noise shaping.
5. Output of the DSM drives the multi-level DAC after synchronization and level shifting.

Hint Bar

Review TRM section 33.6.4 for additional details.

The processing of the FIR filter, CIC filter, interpolator, and DSM cannot be configured by the user.

Review the Appendix section for additional details about FIR filter, CIC filter, and Delta-Sigma Modulator (DSM).

Noise shaping increases the apparent S/N ratio of the resultant signal by lowering the noise present in the audible range and increasing the noise above the audible range.
Test Mode

- Test mode for analog block (TEST_CTL.TEST_MODE_EN = 1)
  - Analog block's input is connected to TEST_ANALOG_DATA.TEST_ANALOG_DATAIN

Hint Bar

Review TRM section 33.6.8 for additional details.

Review the Appendix section for additional details about the analog block.
Appendix
FIR Filter

FIR filter in DAC core
- Coefficient multiplication of 256 TAPS is carried with one multiplier
- Four multiplications are performed for one sample value with system clock/4 frequency (64 Fs)
- Result of the multiplication is accumulated in every system clock/4 frequency (64 Fs), which equals to 64 TAP multiplications of 4 (4 x 64) = 256 TAPS being executed
CIC Filter

- **CIC filter in DAC core**
  - First three stages: Comb-type filter
    - Operates at system clock/64 (4 Fs)
  - Last three stages: Integral-type filter
    - Operates at system clock/4 (64 Fs)
  - **CIC-Interpolation** is sequentially connected and outputs in 256 Fs rate

- **Advantage**
  - Has anti-aliasing and oversampling role
Delta-Sigma Modulator (1/2)

- CIDF delta-sigma modulation circuit
  - Set the quantizer to 11-level
    - Quantization noise in passband is reduced by more than 1-bit delta-sigma configuration
  - Decode 11-level (4-bit) to 10-line (weight is equal to 1)
  - Drive analog DAC block with PDM waveform

```
\begin{align*}
\text{Z} & \quad \text{Z}^1 \\
\text{Z}^1 & \quad \text{Z}^1 \\
\text{11-level quantizer} & \\
\text{4-bit to 10-line decoder} & \\
\text{Z}^1 & \quad \text{Z}^1
\end{align*}
```
Delta-Sigma Modulator (2/2)

› Dynamic Element Matching
  - Averages the output voltage by sequentially changing the elements at the “High” level
  - To reduce the influence of the relative error that can increase noise and distortion

› Dithering
  - Suppresses idle tone generation
  - Is added before DSM to improve S/N ratio

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*Hint Bar*

Review TRM section 33.6.4 for additional details

Signal-to-noise ratio (S/N ratio)
Analog Block

- Output of the DSM passes through LSs, FFs, and BUFs, and finally drives the DAC input resistors
- DAC resistors are summed at the input of the opamp
- An active third-order LPF with cut-off frequency of 90 kHz is used
  - To filter high-frequency quantization noise
  - To provide low-impedance drive

![Analog Block Diagram](image)
Part of your life. Part of tomorrow.
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>ECN</th>
<th>Submission Date</th>
<th>Description of Change</th>
</tr>
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<tbody>
<tr>
<td>**</td>
<td>6638977</td>
<td>07/29/2019</td>
<td>Initial release</td>
</tr>
<tr>
<td>*A</td>
<td>6805412</td>
<td>02/12/2020</td>
<td>Added note descriptions in each slide</td>
</tr>
<tr>
<td>*B</td>
<td>7052598</td>
<td>12/21/2020</td>
<td>Updated 2, 5, 6, 7, 9, 11</td>
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