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CYTVII-B-H-4M-272-CPU

Evaluation Board User Guide

Document Number: 002-29936 Rev. **

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Safety Information

Regulatory Compliance

This Evaluation Board is intended for use as a development platform for hardware in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. This may cause interference to other electrical or electronic devices in close proximity.

In a domestic environment, this product may cause radio interference. The user may then be required to take adequate prevention measures. Also, the board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

	This Evaluation Board contains electrostatic discharge (ESD) sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused this board in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If an ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to chassis ground (any unpainted metal surface) on your board when handling parts.

Handling Boards

This board is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad if available. Do not slide board over any surface.

1. Introduction

This user guide provides instructions to handle the CYTVII-B-H-4M-272-CPU board. This is an evaluation platform for the CYT4BB Traveo™ II device. The board can be used as a standalone board for basic validation or in combination with the CYTVII-B-E-BB Traveo II base board (available separately from Cypress). This document assumes that you will work with the combination (CPU board + base board), and provides guidance on how to use the features of the evaluation platform.

1.1 Precautions and Warnings

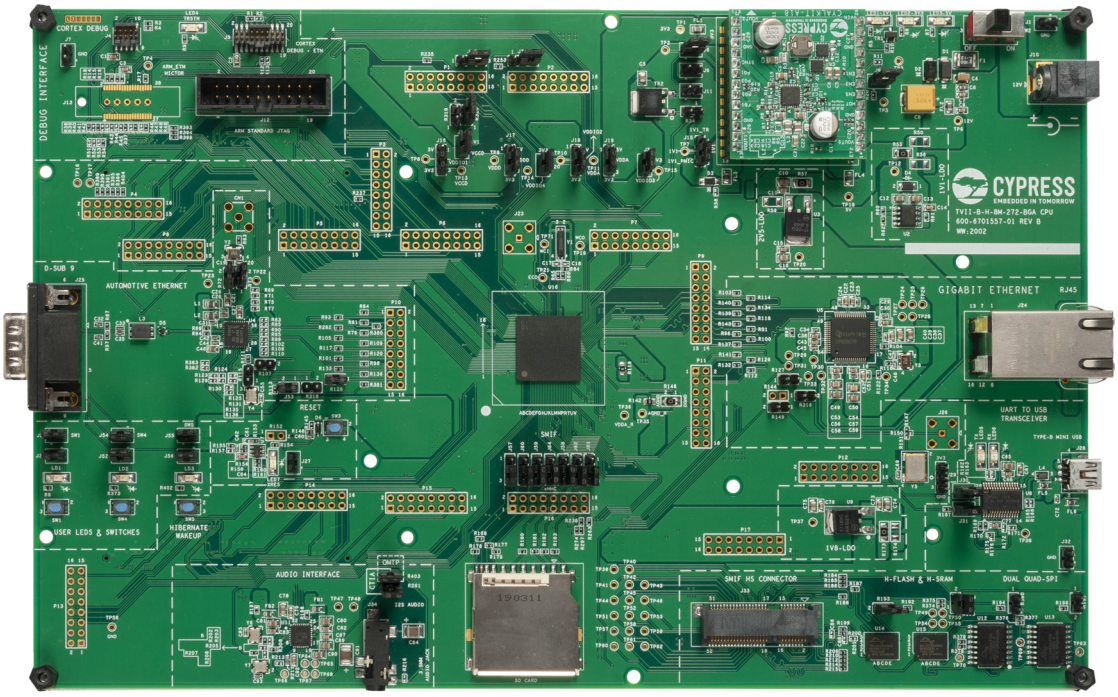
The board is a delicate PCB; make sure that the evaluation board is handled by qualified personnel who are aware of the capabilities of the board. Handle the board carefully and make sure it is not bent or subjected to stress. Ensure your own safety arising from electrical hazards and other sources.

The CPU board is shipped with a 12 V DC power adapter. This adapter can be plugged into the AC mains supply anywhere in the world and is designed to receive 100-240 V AC V @ 50/60 Hz. While powering the board, you must connect only the power adapter supplied with the evaluation board and not any other part.

2. Overview

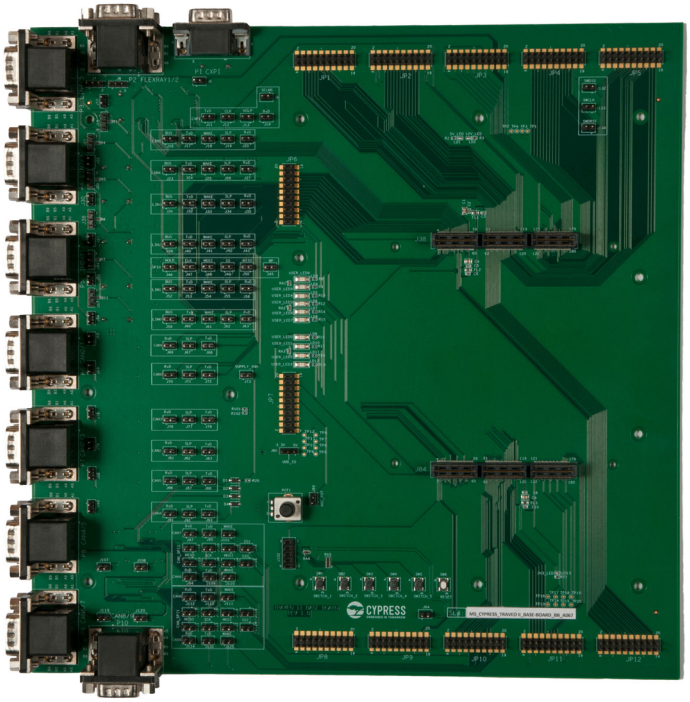
Figure 2-1 shows the CYTVII-B-H-4M-272-CPU board.

Figure 2-1. CYTVII-B-H-4M-272-CPU Board



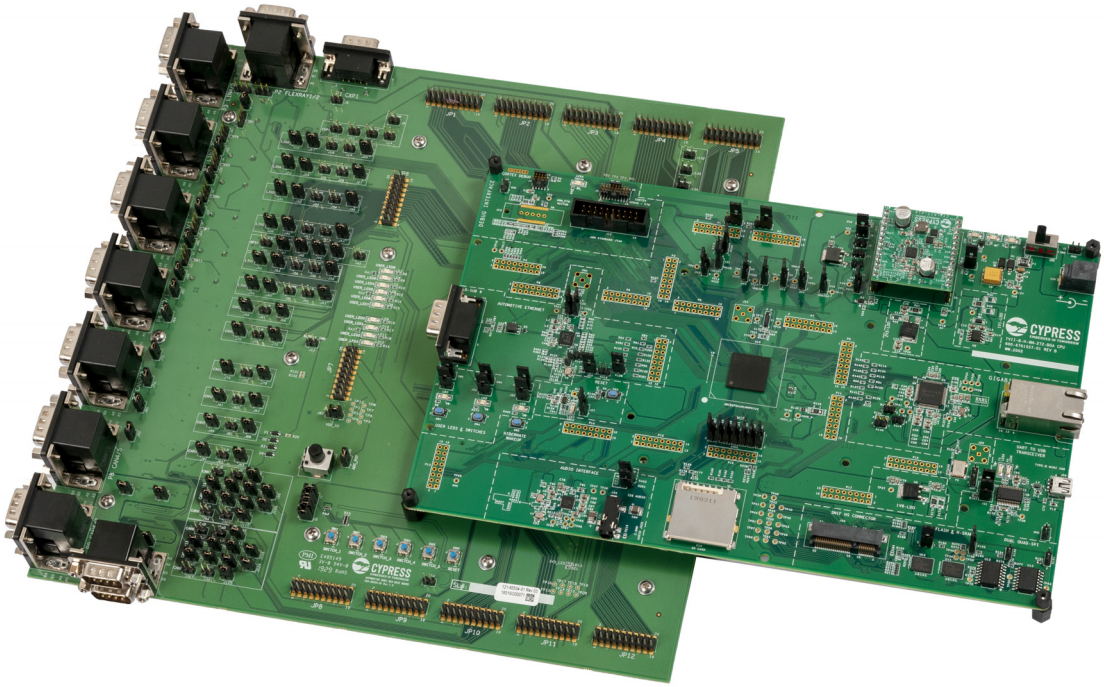
The CPU board is meant to be used along with a Traveo II base board (CYTVII-B-E-BB). The base board brings out all important interface connections such as CAN, LIN, SPI EEPROM and can be used in conjunction with several CPU boards of the Traveo II family. Figure 2-2 shows the base board.

Figure 2-2. Traveo II Base Board (CYTVII-B-E-BB)



Two Samtec connectors on the CPU board and corresponding mating connectors on the base board are used to connect signals across the two boards. When put together, the boards appear as shown in Figure 2-3.

Figure 2-3. Combination of CPU Board and Traveo II Base Board



2.1 Functional Overview

The CPU board has the following components:

1. One Traveo II device, which is soldered on board (U16).
2. PMIC to generate the 5-V, 3.3-V, and 1.1-V outputs, which power the CPU board and the base board (if connected).
3. Programming interface (Arm® Standard JTAG, Cortex® Debug, Cortex Debug + ETM and Arm ETM Mictor) to connect several programming tools such as IAR I-jet, Green Hills MULTI, also Cypress MiniProg.
4. USB-UART interface for terminal logging (J28).
5. Three user switch (SW1, SW4, SW5) and three user LED (LD1, LD2, LD3) for standalone operation without the base board.
6. Reset controller with manual reset switch (SW3) and voltage supervision.
7. Measurement of device current on VCCD using jumper J14, VDDD using jumper J17, VDDIO_1 using jumper J16, VDDIO_2 using jumper J18, VDDIO_3 using jumper J21, VDDIO_4 using jumper J20, and VDDA using jumper J19 respectively.
8. Samtec connector interface (J35 and J36) for connecting to the base board CYTVII-B-E-BB.
9. Automotive Ethernet(J25)
10. I^2S Audio Codec (J34)
11. SD Card Connector (U10)
12. HyperFlash and HyperRAM (U15, U14)
13. Dual Quad SPI Flash (U13, U12)
14. 0.10-inch Through-Hole Test Points

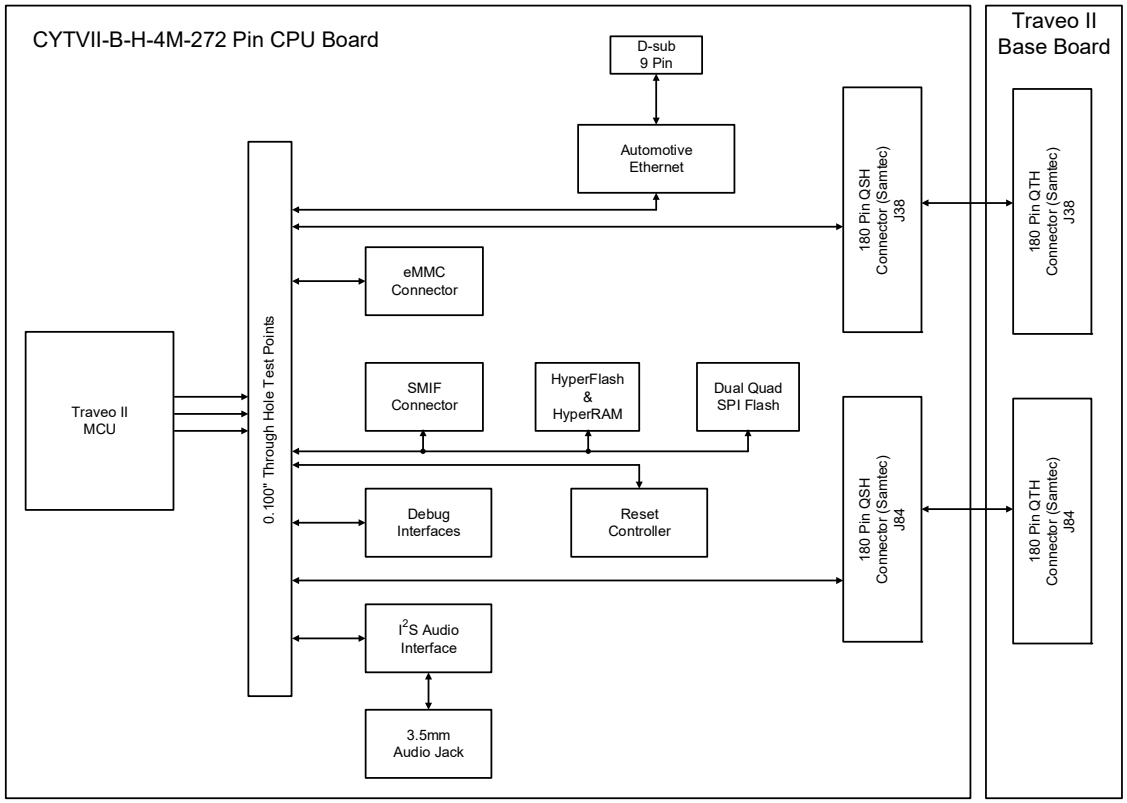
The Traveo II base board has the following components:

1. Six TJA1057GT - CAN-FD Transceivers (Dual connectors P6, P7, P8).
2. Four TJA1145T - SPI based CAN-FD transceivers (Dual connectors P9, P10).
3. Six TJA1021T - LIN transceivers (Dual connectors P3, P4, P5).
4. Two TJA1081TS - FlexRay transceivers (Dual connector P2).
5. One S6BT112A01 - CXPI transceiver (Connector P1).
6. One SPI EEPROM 25LC320A (U9).
7. Five user switches (SW1 through SW5), 10 user LEDs (USER_LED0 through USER_LED9), and one potentiometer (POT1) for analog input.
8. Pin headers to access all I/Os of the Traveo II device (when a CPU board is connected to the base board).
9. Samtec connector interface (J38 and J84) for connecting to a CPU board.

2.1.1 Block Diagram

The block diagram is shown in Figure 2-4.

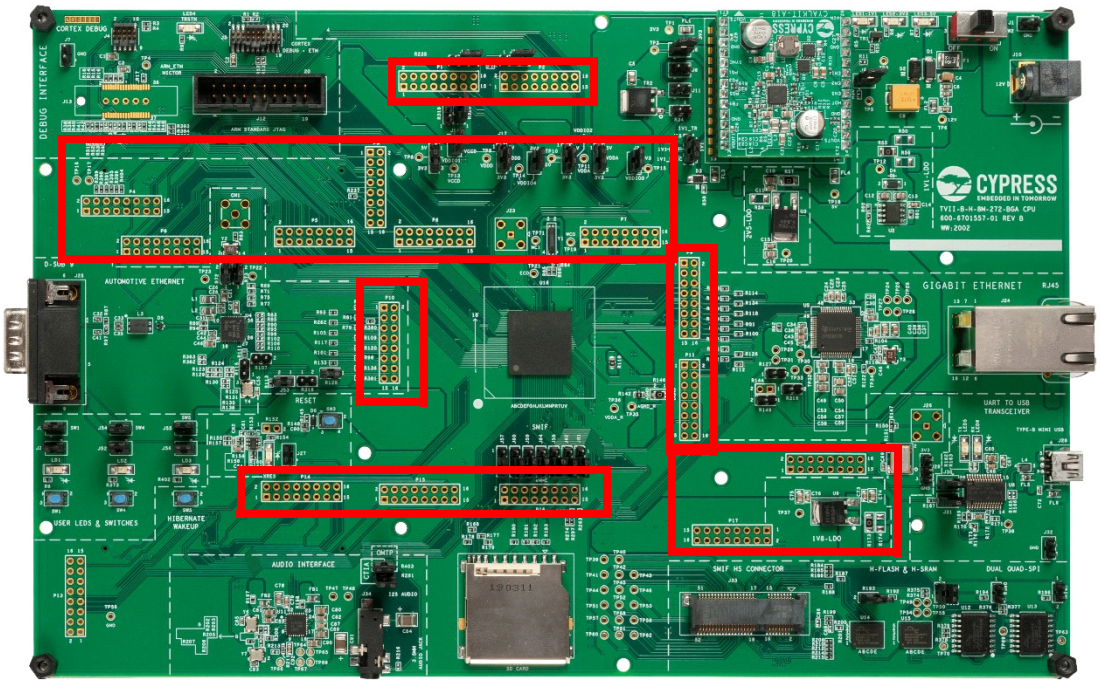
Figure 2-4. Block Diagram



2.1.2 The 0.10-inch Through-Hole Test Points

The location of the 0.10-inch Through-Hole Test Points is shown in Figure 2-5.

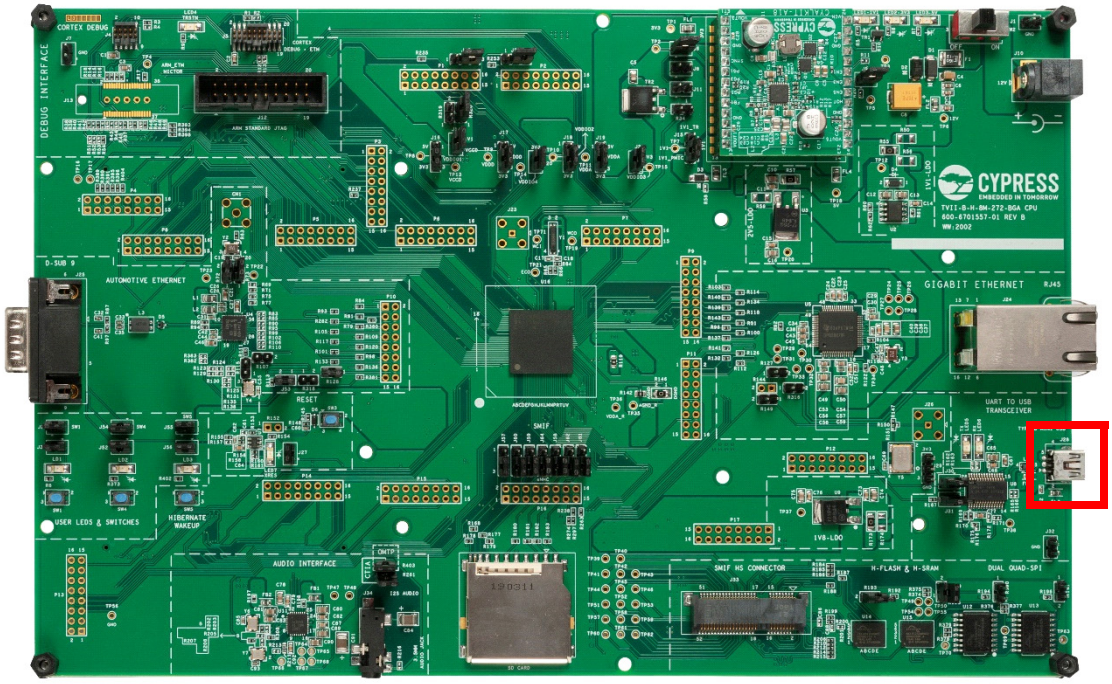
Figure 2-5. 0.10-inch Through-Hole Test Points



2.1.3 USB Connector

The location of the USB connector is shown in Figure 2-6.

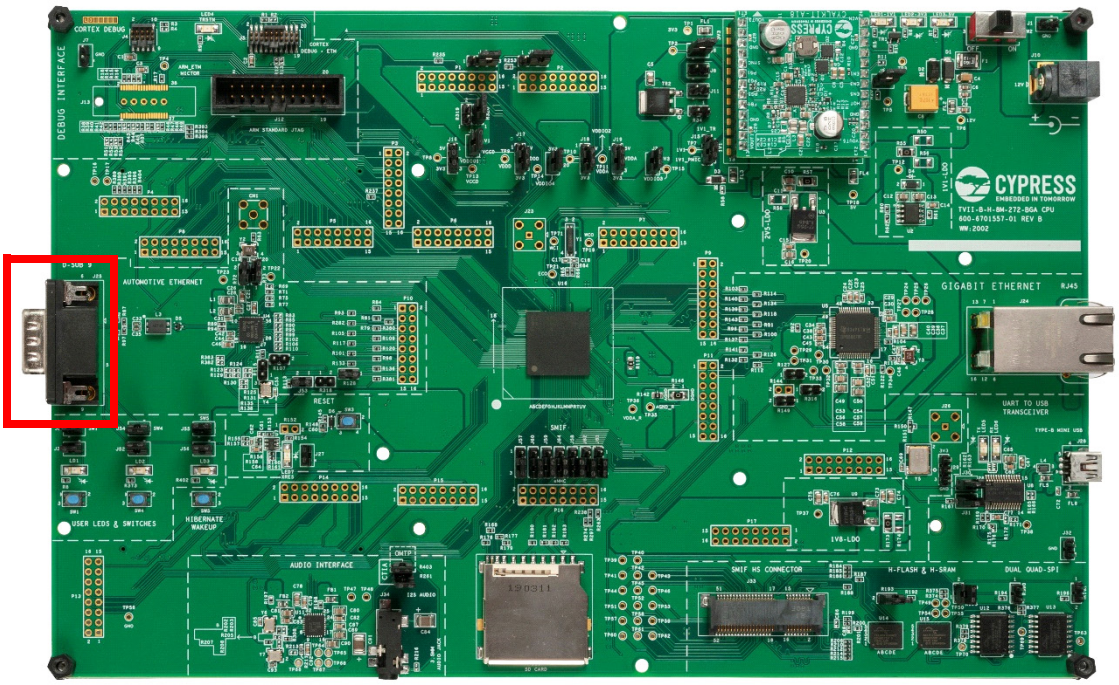
Figure 2-6. USB Connector



2.1.4 Ethernet Connector (Automotive Ethernet)

The location of the Ethernet connector (Automotive Ethernet) is shown in Figure 2-7.

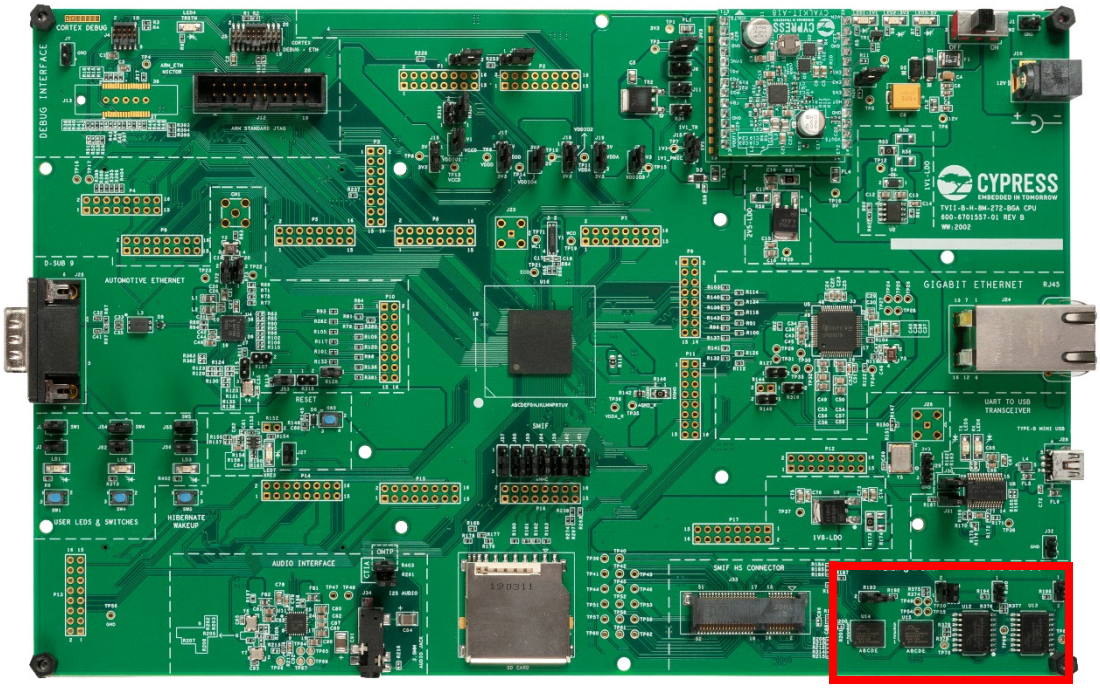
Figure 2-7. Ethernet Connector (Automotive Ethernet)



2.1.5 On-board SMIF Devices

The location of the onboard SMIF devices in shown in Figure 2-8.

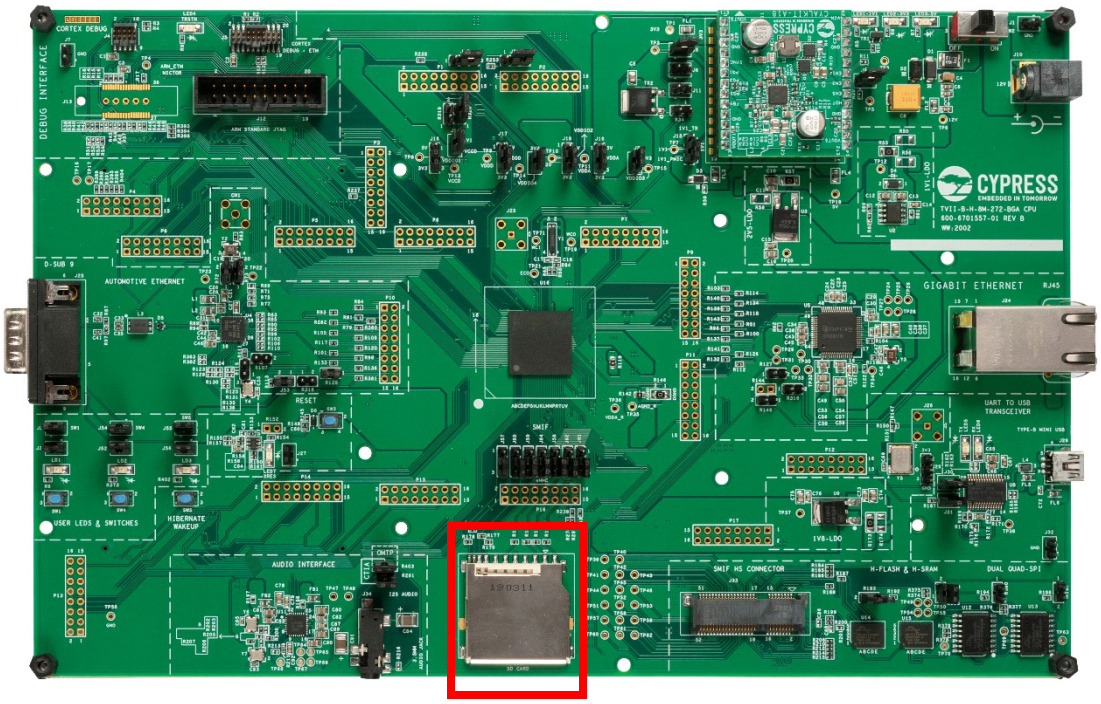
Figure 2-8. SMIF Devices



2.1.6 SD Card Connector

The location of the SD Card connector is shown in Figure 2-9.

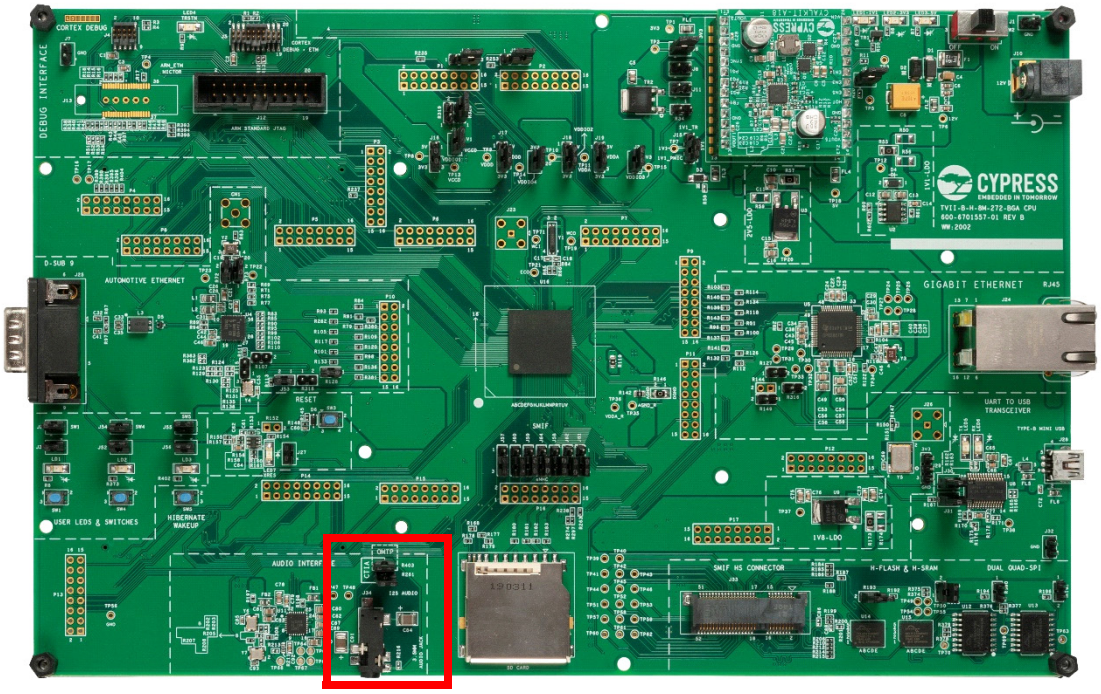
Figure 2-9. eMMC Connector



2.1.7 Audio Connector

The location of the audio connector is shown in Figure 2-10.

Figure 2-10. Audio Connector



3. Operation

This section describes the operation of the CPU board and the base board. It is assumed that you have connected the CPU board to the base board using the Samtec interface. Follow these steps to operate the CPU board and the base board:

1. A 12 V wall adapter board is supplied along with the CPU board. Connect the 12 V wall adapter to the barrel connector marked “12V DC” on the CPU board. Connect its plug to a mains socket using one of the four plug adapters provided in the white box (depending on the geographical location and the socket type available).
2. Ensure that jumpers J16, J17, J18, J19 (position “1-2”), J14, J20, J21 (current measurement jumpers) are inserted on the CPU board.
3. Turn on the mains supply to the wall adapter. Turn on the switch SW2 on the CPU board. The LED labeled PWR should light up.
4. Connect an appropriate programming tool to one of the programming interfaces (J13, J4, J12, J5). Programming tool options are:
   - Arm ETM MICTOR on J13
   - Cortex DEBUG on J4
   - Arm Standard JTAG on J12
   - Cortex DEBUG and ETM on J5
8. Install the appropriate programming integrated development environment (IDE) on a PC. The programming IDE (GHS MULTI, IAR Embedded Workbench, Cypress Programmer, etc.) should be able to detect a device (read the device ID) and to load a firmware HEX file (*.srec*) into the device flash successfully.
   As part of the release package, various firmware examples compiled in *.srec* programming IDEs are available. Some examples use specific transceivers on the base board.
9. To start with, use the LED blink example provided with the release package to test the functioning of the board.
10. Connect a USB-mini cable to J28 and the other end to a PC. Open Tera Term or your preferred terminal logging application and set the appropriate port and baud rate (typically 115,200 baud, 8, N, 1). Ensure that jumpers J30 and J31 are inserted on the CPU board. Some firmware examples provide data logs from the device or ask for user inputs over the terminal.

4. Connections and Settings

4.1 Evaluation Board Connections

4.1.1 Base Board and CPU Board Connections

Make sure that the following jumpers are inserted on the base board, so that each transceiver on the base board can be used with the respective firmware example that activate each functionality of the device:

- CAN0.1 from the device uses the CAN0 transceiver on the base board (connect jumpers J70, J71, J72).
- CAN1.1 from the device uses the CAN2 transceiver on the base board (connect jumpers J81, J82, J83).
- CAN1.2 from the device uses the CAN3 transceiver on the base board (connect jumpers J76, J77, J78).
- CAN1.3 from the device uses the CAN4 transceiver on the base board (connect jumpers J91, J92, J93).
- CAN1.0 from the device uses the CAN6 transceiver on the base board (connect jumpers J86, J87, J88).
- LIN0 from the device uses the LIN0 transceiver on the base board (connect jumpers J58, J59, J60, J63).
- LIN6 from the device uses the LIN1 transceiver on the base board (connect jumpers J51, J52, J53, J56).
- LIN8 from the device uses the LIN2 transceiver on the base board (connect jumpers J37, J39, J40, J43).
- LIN7 from the device uses the LIN3 transceiver on the base board (connect jumpers J30, J31, J32, J35).
- LIN10 from the device uses the LIN4 transceiver on the base board (connect jumpers J22, J23, J24, J27).
- LIN5 from the device uses the LIN5 transceiver on the base board (connect jumpers J10, J16, J17, J20).
- EEPROM on the base board is enabled by connecting jumpers J47, J48, J49, J50.
- The user switch functionality is enabled by connecting jumper J102.
- The potentiometer functionality is enabled by connecting jumper J89.
- Automotive Ethernet on the CPU Board is enabled for RMII mode by shorting jumper J53, R128, R72, R73, R107, R115. MII Mode is enabled by shorting J53, R128, R72, R73 and opening R115 and R107.
- SMIF - Dual Quad SPI on the CPU Board is enabled by shorting jumpers R190, R191, J57(1-2), J60(1-2), J59(1-2), J64(1-2), J58(1-2), J62(1-2), J61(1-2)
- SMIF - HyperFlash and HyperRAM on the CPU Board is enabled by shorting jumpers R189, R193, J57(1-2), J60(1-2), J59(1-2), J64(1-2), J58(1-2), J62(1-2), J61(1-2).

- SD Card Connector on the CPU board is enabled by connecting jumpers J57(2-3), J60(2-3), J59(2-3), J64(2-3), J58(2-3), J62(2-3), J61(2-3).
- I2S Audio Codec on the CPU board is always enabled.

In addition, power is supplied to the base board by connecting jumper J80 to the 3 V or 5 V select jumper pin in the ‘5 V’ position. Make sure that jumper J80 is always connected. Once a specific functionality is chosen by connecting the jumpers listed above, ensure that the appropriate firmware is loaded onto the device. Incorrect firmware can result in port pins being configured incorrectly leading to bus contention and damage to hardware. For example, if you connect jumpers related to CAN0.0, you must ensure that firmware configures the related ports as CAN pins. Contact Cypress technical support for firmware examples.

Apart from these interface transceivers that can be used for specific functions, all pins of the device are also accessible on the base board using pin headers JP1 through JP12.

The device port pins are connected to pin headers on the base board as listed in Table 4-1.

Table 4-1. Device Port Pin Connections on Base Board

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
J18	DRV_VOUT			DRV_VOUT		
B18	P0_0/PWM_18/PWM_22_N/TC_18_TR0/TC_22_TR1/ SCB0_RX/SCB7_SDA/SCB0_MISO/LIN1_RX	P5.16	JP2.18	BB_I2C1_SDA		
B17	P0_1/PWM_17/PWM_18_N/TC_17_TR0/TC_18_TR1/ SCB0_TX/SCB7_SCL/SCB0_MOSI/LIN1_TX	P5.8	JP2.17	BB_I2C1_SCL		
A17	P0_2/PWM_14/PWM_17_N/TC_14_TR0/TC_17_TR1/ SCB0_RTS/SCB0_SCL/SCB0_CLK/SCB4_MISO/LIN1_EN/ CAN0_1_TX	P5.7	JP6.12	BB_CAN0_TXD		
B16	P0_3/PWM_13/PWM_14_N/TC_13_TR0/TC_14_TR1/ SCB0_CTS/SCB0_SDA/SCB0_SEL0/SCB4_MOSI/ CAN0_1_RX	P5.6	JP6.11	BB_CAN0_RXD		
A16	P1_0/PWM_12/PWM_13_N/TC_12_TR0/TC_13_TR1/ PWM_H_4/SCB0_SCL/SCB0_MISO/SCB4_CLK	P5.5	JP6.5	BB_CAN0_S		
A15	P1_1/PWM_11/PWM_12_N/TC_11_TR0/TC_12_TR1/ PWM_H_5/SCB0_SDA/SCB0_MOSI/SCB4_SEL0	P5.3		GPIO_P1_1		
B15	P1_2/PWM_10/PWM_11_N/TC_10_TR0/TC_11_TR1/ PWM_H_6/SCB0_CLK/LIN0_RX/TRIG_IN[0]	P5.4	JP1.3	BB_LIN0_RXD		
C15	P1_3/PWM_8/PWM_10_N/TC_8_TR0/TC_10_TR1/ PWM_H_7/SCB0_SEL0/LIN0_TX/TRIG_IN[1]	P6.13	JP1.5	BB_LIN0_WAKE		
D15	P1_4/LIN8_RX/SCB8_RX/SCB8_MISO	P15.6		GPIO_P1_4		
M1	P10_0/PWM_28/PWM_27_N/TC_28_TR0/TC_27_TR1/ SCB4_RX/SCB4_MISO/LIN7_RX/TRIG_IN[18]	P17.8		GPIO_P10_0		
N1	P10_1/PWM_29/PWM_28_N/TC_29_TR0/TC_28_TR1/ SCB4_TX/SCB4_SDA/SCB4_MOSI/LIN7_TX/TRIG_IN[19]	P11.12		GPIO_P10_1		
N2	P10_2/PWM_30/PWM_29_N/TC_30_TR0/TC_29_TR1/ LIN8_RX/SCB4_RTS/SCB4_SCL/SCB4_CLK	P4.4		BB_FRA_RXD		
N3	P10_3/PWM_31/PWM_30_N/TC_31_TR0/TC_30_TR1/ LIN8_TX/SCB4_CTS/SCB4_SEL0	P4.5		BB_FRA_TXD		
N4	P10_4/PWM_32/PWM_31_N/TC_32_TR0/TC_31_TR1/ LIN8_EN/SCB4_SEL1/ADC[1]_0	P4.6		BB_FRA_TXEN		
P1	P10_5/PWM_33/PWM_32_N/TC_33_TR0/TC_32_TR1/ SCB4_SEL2/LIN13_RX/ADC[1]_1	P4.7		BB_FRB_RXD		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
P2	P10_6/PWM_33_N/TC_33_TR1/PWM_34/LIN13_TX/ ADC[1]_2	P4.8		BB_FRB_TXD		
P3	P10_7/PWM_35/PWM_34_N/TC_35_TR0/TC_34_TR1/ LIN13_EN/ADC[1]_3	P4.9		BB_FRB_TXEN		
M6	P11_0/PWM_61/PWM_62_N/TC_61_TR0/TC_62_TR1/ AUDIOSS0_MCLK/ADC[0]_M	P16.10		AUDIO_0_I2S_MCLK	AUDIO_I2S_MCLK	
P4	P11_1/PWM_60/PWM_61_N/TC_60_TR0/TC_61_TR1/ AUDIOSS0_TX_SCK/ADC[1]_M	P16.11		AUDIO_0_I2S_TX-_SCK	AUDIO_I2S_TX-_SCK	
R4	P11_2/PWM_59/PWM_60_N/TC_59_TR0/TC_60_TR1/ AUDIOSS0_TX_WS/ADC[2]_M	P16.14		AUDIO_0_I2S_TX-_WS	AUDIO_I2S_TX-_WS	
R1	P12_0/PWM_36/TC_36_TR0/PWM_35_N/AUDIOSS0_TX-_SDO/SCB8_RX/SCB8_MISO/CAN0_2_TX/TRIG_IN[20]/ ADC[1]_4	P16.9		AUDIO_0_I2S_TX-_SDO	AUDIO_I2S_TX-_SDO	
R2	P12_1/PWM_37/PWM_36_N/TC_37_TR0/TC_36_TR1/ AUDIOSS0_CLK_I2S_IF/SCB8_TX/SCB8_SDA/SCB8_-MOSI/LIN6_EN/CAN0_2_RX/TRIG_IN[21]/ADC[1]_5	P16.12		AUDIO_0_-CLK_I2S_IF	AUDIO_CLK_I2S_IF	
R3	P12_2/PWM_38/PWM_37_N/TC_38_TR0/TC_37_TR1/ AUDIOSS0_RX_SCK/EXT_MUX[1]_EN/SCB8_RTS/ SCB8_SCL/SCB8_CLK/LIN6_RX/ADC[1]_6	P16.13		AUDIO_0_I2S_RX-_SCK	AUDIO_I2S_RX-_SCK	
T1	P12_3/PWM_39/PWM_38_N/TC_39_TR0/TC_38_TR1/ AUDIOSS0_RX_WS/EXT_MUX[1]_0/SCB8_CTS/SCB8_-SEL0/LIN6_TX/ADC[1]_7	P16.15		AUDIO_0_I2S_RX-_WS	AUDIO_I2S_RX-_WS	
T2	P12_4/PWM_40/PWM_39_N/TC_40_TR0/TC_39_TR1/ AUDIOSS0_RX_SDI/EXT_MUX[1]_1/SCB8_SEL1/ CAN1_1_TX/ADC[1]_8	P16.16		AUDIO_0_I2S_RX-_SDI	AUDIO_I2S_RX-_SDI	
T3	P12_5/PWM_41/PWM_40_N/TC_41_TR0/TC_40_TR1/ EXT_MUX[1]_2/CAN1_1_RX/ADC[1]_9	P14.7		GPIO_P12_5		
U1	P12_6/PWM_42/PWM_41_N/TC_42_TR0/TC_41_TR1/ ADC[1]_10	P13.12	JP11.14	BB_USER_BUT-TON_1		
U2	P12_7/PWM_43/PWM_42_N/TC_43_TR0/TC_42_TR1/ ADC[1]_11	P13.9	JP11.13	BB_USER_BUT-TON_2		
V2	P13_0/PWM_M_8/PWM_43_N/TC_M_8_TR0/TC_43_TR1/ AUDIOSS1_MCLK/EXT_MUX[2]_0/SCB3_RX/LIN3_RX/ SCB3_MISO/ADC[1]_12	P12.11		UART_RX		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
V3	P13_1/PWM_44/PWM_M_8_N/TC_44_TR0/TC_M_8_TR1/ AUDIOSS1_TX_SCK/EXT_MUX[2]_1/SCB3_TX/SCB3_SDA/ LIN3_TX/SCB3_MOSI/ADC[1]_13	J30.2		UART_TX		
U3	P13_2/PWM_M_9/PWM_44_N/TC_M_9_TR0/TC_44_TR1/ AUDIOSS1_TX_WS/EXT_MUX[2]_2/SCB3_RTS/SCB3_SCL/ LIN3_EN/SCB3_CLK/ADC[1]_14	P12.7	JP11.16	BB_USER_BUT-TON_3		
V4	P13_3/PWM_45/PWM_M_9_N/TC_45_TR0/TC_M_9_TR1/ AUDIOSS1_TX_SDO/EXT_MUX[2]_EN/SCB3_CTS/ LIN2_RX/SCB3_SEL0/ADC[1]_15	P11.7		GPIO_P13_3		
U4	P13_4/PWM_M_10/PWM_45_N/TC_M_10_TR0/ TC_45_TR1/LIN8_RX/AUDIOSS1_CLK_I2S_IF/PWM_H_4/ LIN2_TX/SCB3_SEL1/ADC[1]_16	P14.16	JP11.17	BB_USER_BUT-TON_4		
T4	P13_5/PWM_46/PWM_M_10_N/TC_46_TR0/ TC_M_10_TR1/LIN8_TX/AUDIOSS1_RX_SCK/ PWM_H_4_N/SCB3_SEL2/ADC[1]_17	P11.8		GPIO_P13_5		
U5	P13_6/PWM_M_11/PWM_46_N/TC_M_11_TR0/TC_46_TR1/ LIN8_EN/AUDIOSS1_RX_WS/PWM_H_5/SCB3_SEL3/ TRIG_IN[22]/ADC[1]_18	P4.14	JP11.15	BB_USER_BUT-TON_5		
T5	P13_7/PWM_47/PWM_M_11_N/TC_47_TR0/TC_M_11_TR1/ AUDIOSS1_RX_SDI/PWM_H_5_N/TRIG_IN[23]/ADC[1]_19	P14.15	JP11.4	BB_CAN6_WAKE		
V5	P14_0/PWM_48/PWM_47_N/TC_48_TR0/TC_47_TR1/ AUDIOSS2_MCLK/PWM_H_6/SCB2_MISO/SCB2_RX/ CAN1_0_TX/ADC[1]_20	P14.13		BB_CAN6_TXD		
V6	P14_1/PWM_49/PWM_48_N/TC_49_TR0/TC_48_TR1/ AUDIOSS2_TX_SCK/PWM_H_6_N/SCB2_MOSI/ SCB2_SDA/SCB2_TX/CAN1_0_RX/ADC[1]_21	P14.14		BB_CAN6_RXD		
U6	P14_2/PWM_50/PWM_49_N/TC_50_TR0/TC_49_TR1/ PWM_H_7/SCB2_CLK/SCB2_SCL/SCB2_RTS/LIN6_RX/ ADC[1]_22	P4.16	JP2.13	BB_LIN4_RXD		
T6	P14_3/PWM_51/PWM_50_N/TC_51_TR0/TC_50_TR1/ PWM_H_7_N/SCB2_SEL0/SCB2_CTS/LIN6_TX/ADC[1]_23	P4.13	JP2.14	BB_LIN4_TXD		
R6	P14_4/PWM_52/PWM_51_N/TC_52_TR0/TC_51_TR1/ AUDIOSS2_TX_WS/TC_H_4_TR0/SCB2_SEL1/LIN6_EN/ ADC[1]_24	P4.15	JP2.16	BB_LIN4_SLP		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
N7	P14_5/PWM_53/PWM_52_N/TC_53_TR0/TC_52_TR1/ AUDIOSS2_TX_SDO/TC_H_4_TR1/SCB2_SEL2/LIN14_RX/ ADC[1]_25	P6.5	JP2.15	BB_LIN4_WAKE		
T7	P14_6/PWM_54/PWM_53_N/TC_54_TR0/TC_53_TR1/ TC_H_5_TR0/LIN14_TX/TRIG_IN[24]/ADC[1]_26	P11.15		GPIO_P14_6		
R7	P14_7/PWM_55/PWM_54_N/TC_55_TR0/TC_54_TR1/ TC_H_5_TR1/LIN14_EN/TRIG_IN[25]/ADC[1]_27	P11.6		GPIO_P14_7		
V7	P15_0/PWM_56/PWM_55_N/TC_56_TR0/TC_55_TR1/ AUDIOSS2_CLK_I2S_IF/TC_H_6_TR0/SCB9_RX/ SCB9_MISO/CAN1_3_TX/ADC[1]_28	P14.11	JP11.8	BB_CAN4_TXD		
U7	P15_1/PWM_57/PWM_56_N/TC_57_TR0/TC_56_TR1/ AUDIOSS2_RX_SCK/TC_H_6_TR1/SCB9_TX/SCB9_SDA/ SCB9_MOSI/CAN1_3_RX/ADC[1]_29	P14.12	JP11.7	BB_CAN4_RXD		
V8	P15_2/PWM_58/PWM_57_N/TC_58_TR0/TC_57_TR1/ AUDIOSS2_RX_WS/TC_H_7_TR0/SCB9_RTS/SCB9_SCL/ SCB9_CLK/ADC[1]_30	P13.15	JP10.13	BB_CAN4_S		
U8	P15_3/PWM_59/PWM_58_N/TC_59_TR0/TC_58_TR1/ AUDIOSS2_RX_SDI/TC_H_7_TR1/SCB9_CTS/SCB9_SEL0/ ADC[1]_31	P14.3		GPIO_P15_3		
V12	P16_0/PWM_60/PWM_59_N/TC_60_TR0/TC_59_TR1/ PWM_H_0/SCB9_SEL1/LIN11_RX	P11.16		GPIO_P16_0		
U12	P16_1/PWM_61/PWM_60_N/TC_61_TR0/TC_60_TR1/ PWM_H_0_N/SCB9_SEL2/LIN11_TX	P11.13		GPIO_P16_1		
V13	P16_2/PWM_62/PWM_61_N/TC_62_TR0/TC_61_TR1/ PWM_H_1/SCB9_SEL3/LIN11_EN	P9.5		GPIO_P16_2		
U13	P16_3/PWM_62/PWM_62_N/TC_62_TR0/TC_62_TR1/ PWM_H_1_N	P7.15		GPIO_P16_3		
T13	P16_4	J3.2		CB_LED_P16_4		
R13	P16_5	J52.2		CB_LED_P16_5		
T14	P16_6	J2.1		CB_BUTTON_P16_6		
N12	P16_7	J56.2		GPIO_P16_7		
V14	P17_0/PWM_61/PWM_62_N/TC_61_TR0/TC_62_TR1/ LIN11_RX/CAN1_1_TX	P7.10	JP10.8	BB_CAN2_TXD		
U14	P17_1/PWM_60/PWM_61_N/TC_60_TR0/TC_61_TR1/ SCB3_RX/LIN11_TX/CAN1_1_RX	P7.7	JP10.7	BB_CAN2_RXD		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
V15	P17_2/PWM_59/PWM_60_N/TC_59_TR0/TC_60_TR1/ SCB3_TX/SCB3_SDA/LIN11_EN	P7.8	JP10.11	BB_CAN2_S		
U15	P17_3/PWM_58/PWM_59_N/TC_58_TR0/TC_59_TR1/ PWM_H_3/SCB3_RTS/SCB3_SCL/SCB3_CLK/TRIG_IN[26]	J54.1		GPIO_P17_3		
T15	P17_4/PWM_57/PWM_58_N/TC_57_TR0/TC_58_TR1/ PWM_H_3_N/SCB3_CTS/SCB3_SEL0/TRIG_IN[27]	P7.3		GPIO_P17_4		
V16	P17_5/PWM_56/PWM_57_N/TC_56_TR0/TC_57_TR1/ PWM_H_2/LIN15_RX/SCB3_SEL1	P7.4		GPIO_P17_5		
U16	P17_6/PWM_M_4/PWM_56_N/TC_M_4_TR0/TC_56_TR1/ PWM_H_2_N/LIN15_TX/SCB3_SEL2	P7.1		GPIO_P17_6		
V17	P17_7/PWM_M_5/PWM_M_4_N/TC_M_5_TR0/ TC_M_4_TR1/LIN15_EN/LIN12_RX	P7.2		GPIO_P17_7		
U18	P18_0/PWM_M_6/PWM_M_5_N/TC_M_6_TR0/ TC_M_5_TR1/ETH0_REF_CLK/PWM_H_0/SCB1_RX/ SCB1_MISO/LIN12_TX/FAULT_OUT_0/ADC[2]_0	P10.4		AUTO_ETH_REF_-CLK_R	AUTO_ETH_REF_-CLK	AUTO_PHY_REF_-CLK
U17	P18_1/PWM_M_7/PWM_M_6_N/TC_M_7_TR0/ TC_M_6_TR1/ETH0_TX_CTL/PWM_H_0_N/SCB1_TX/ SCB1_SDA/SCB1_MOSI/SCB3_MISO/FAULT_OUT_1/ ADC[2]_1	P10.3		AUTO_ETH_TXEN_R	AUTO_ETH_TXEN	
T18	P18_2/PWM_55/PWM_M_7_N/TC_55_TR0/TC_M_7_TR1/ ETH0_TX_ER/PWM_H_1/SCB1_RTS/SCB1_SCL/SCB1_-CLK/SCB3_MOSI/ADC[2]_2	P10.6		AUTO_ETH_TXER_R	AUTO_ETH_TXER	
T17	P18_3/PWM_54/PWM_55_N/TC_54_TR0/TC_55_TR1/ ETH0_TX_CLK/PWM_H_1_N/SCB1_CTS/SCB1_SEL0/ SCB3_CLK/TRACE_CLOCK/ADC[2]_3	P10.5		AUTO_ETH_TXC_R	AUTO_ETH_TXC	
T16	P18_4/PWM_53/PWM_54_N/TC_53_TR0/TC_54_TR1/ ETH0_TXD_0/PWM_H_2/SCB1_SEL1/SCB3_SEL0/ TRACE_DATA_0/ADC[2]_4	P10.1		AUTO_ETH_TXD0_R	AUTO_ETH_TXD0	
R16	P18_5/PWM_52/PWM_53_N/TC_52_TR0/TC_53_TR1/ ETH0_TXD_1/PWM_H_2_N/SCB1_SEL2/TRACE_DATA_1/ ADC[2]_5	P10.2		AUTO_ETH_TXD1_R	AUTO_ETH_TXD1	
R15	P18_6/PWM_51/PWM_52_N/TC_51_TR0/TC_52_TR1/ ETH0_TXD_2/PWM_H_3/SCB1_SEL3/CAN1_2_TX/ TRACE_DATA_2/ADC[2]_6	P10.11		AUTO_ETH_TXD2_R	AUTO_ETH_TXD2	

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
P15	P18_7/PWM_50/PWM_51_N/TC_50_TR0/TC_51_TR1/ ETH0_TXD_3/PWM_H_3_N/CAN1_2_RX/TRACE_DATA_3/ ADC[2]_7	P10.12		AUTO_ETH_TXD3_R	AUTO_ETH_TXD3	
R18	P19_0/PWM_M_3/PWM_50_N/TC_M_3_TR0/TC_50_TR1/ ETH0_RXD_0/TC_H_0_TR0/SCB2_MISO/SCB2_RX/ CAN1_3_TX/FAULT_OUT_2	P10.8		AUTO_ETH_RXD0_R	AUTO_ETH_RXD0	
R17	P19_1/PWM_26/PWM_M_3_N/TC_26_TR0/TC_M_3_TR1/ ETH0_RXD_1/TC_H_0_TR1/SCB2_MOSI/SCB2_SDA/ SCB2_TX/CAN1_3_RX/FAULT_OUT_3	P10.7		AUTO_ETH_RXD1_R	AUTO_ETH_RXD1	
P17	P19_2/PWM_27/PWM_26_N/TC_27_TR0/TC_26_TR1/ ETH0_RXD_2/TC_H_1_TR0/SCB2_CLK/SCB2_SCL/ SCB2_RTS/TRIG_IN[28]	P10.10		AUTO_ETH_RXD2_R	AUTO_ETH_RXD2	
P16	P19_3/PWM_28/PWM_27_N/TC_28_TR0/TC_27_TR1/ ETH0_RXD_3/TC_H_1_TR1/SCB2_SEL0/SCB2_CTS/ TRIG_IN[29]	P10.9		AUTO_ETH_RXD3_R	AUTO_ETH_RXD3	
N15	P19_4/PWM_29/PWM_28_N/TC_29_TR0/TC_28_TR1/ TC_H_2_TR0/SCB2_SEL1	P7.9		GPIO_P19_4		
A14	P2_0/PWM_7/PWM_8_N/TC_7_TR0/TC_8_TR1/ TC_H_4_TR0/SCB7_RX/SCB0_SEL1/SCB7_MISO/ LIN0_RX/CAN0_0_TX/SWJ_TRSTN/TRIG_IN[2]	P5.1		TRSTN_PRM	TRSTN	
B14	P2_1/PWM_6/PWM_7_N/TC_6_TR0/TC_7_TR1/ TC_H_5_TR0/SCB7_TX/SCB7_SDA/SCB0_SEL2/SCB7_- MOSI/LIN0_TX/CAN0_0_RX/TRIG_IN[3]	P5.2	JP1.4	BB_LIN0_TXD		
C14	P2_2/PWM_5/PWM_6_N/TC_5_TR0/TC_6_TR1/ETH0_RX- _ER/TC_H_6_TR0/SCB7_RTS/SCB7_SCL/SCB0_SEL3/ SCB7_CLK/LIN0_EN/TRIG_IN[4]	P10.15		AUTO_ETH_RXER_R	AUTO_ETH_RXER	
D14	P2_3/PWM_4/PWM_5_N/TC_4_TR0/TC_5_TR1/ ETH0_ETH_TSU_TIMER_CMP_VAL/TC_H_7_TR0/ SCB7_CTS/SCB7_SEL0/LIN5_RX/TRIG_IN[5]	P15.5		GPIO_P2_3		
B13	P2_4/PWM_3/PWM_4_N/TC_3_TR0/TC_4_TR1/ PWM_H_4_N/SCB7_SEL1/LIN5_TX/TRIG_IN[6]	P15.9		GPIO_P2_4		
C13	P2_5/PWM_2/PWM_3_N/TC_2_TR0/TC_3_TR1/ PWM_H_5_N/SCB7_SEL2/LIN5_EN/TRIG_IN[7]	P15.8		GPIO_P2_5		
D13	P2_6/SCB8_CTS/SCB8_SEL0	P6.12	JP1.11	BB_LIN5_WAKE		
F12	P2_7/SCB8_SEL1/LIN11_RX	P6.11	JP6.10	BB_CAN1_S		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
N16	P20_0/PWM_30/PWM_29_N/TC_30_TR0/TC_29_TR1/ TC_H_2_TR1/SCB2_SEL2/LIN5_RX	P3.6	JP1.9	BB_LIN5_RXD		
M16	P20_1/PWM_49/PWM_30_N/TC_49_TR0/TC_30_TR1/ TC_H_3_TR0/LIN5_TX	P3.5	JP1.10	BB_LIN5_TXD		
M15	P20_2/PWM_48/PWM_49_N/TC_48_TR0/TC_49_TR1/ TC_H_3_TR1/LIN5_EN	P3.8	JP1.12	BB_LIN5_SLP		
M13	P20_3/PWM_47/PWM_48_N/TC_47_TR0/TC_48_TR1/ SCB1_RX/SCB1_MISO/CAN1_2_TX	P1.9	JP3.12	BB_CAN3_TXD		
L16	P20_4/PWM_46/PWM_47_N/TC_46_TR0/TC_47_TR1/ SCB1_TX/SCB1_SDA/SCB1_MOSI/CAN1_2_RX	P1.7	JP3.14	BB_CAN3_RXD		
L15	P20_5/PWM_45/PWM_46_N/TC_45_TR0/TC_46_TR1/ SCB1_RTS/SCB1_SCL/SCB1_CLK	P7.16	JP10.14	BB_CAN3_S		
K16	P20_6/PWM_44/PWM_45_N/TC_44_TR0/TC_45_TR1/ SCB1_CTS/SCB1_SEL0	P3.7	JP6.9	BB_CAN1_TXD		
K15	P20_7/PWM_43/PWM_44_N/TC_43_TR0/TC_44_TR1/ SCB1_SEL1	P1.10	JP6.8	BB_CAN1_RXD		
N17	P21_0/PWM_42/PWM_43_N/TC_42_TR0/TC_43_TR1/ SCB1_SEL2/WCO_IN			CPU_WCO_IN	WCI/BTB	
N18	P21_1/PWM_41/PWM_42_N/TC_41_TR0/TC_42_TR1/ WCO_OUT			CPU_WCO_OUT	WCO/BTB	WCO/BTB_R
M17	P21_2/PWM_40/PWM_41_N/TC_40_TR0/TC_41_TR1/ EXT_CLK/TRIG_DBG[1]/ECO_IN			CPU_ECO_IN	ECI/BTB	
M18	P21_3/PWM_39/PWM_40_N/TC_39_TR0/TC_40_TR1/ ECO_OUT			CPU_ECO_OUT	ECO/BTB	ECO/BTB_R
L17	P21_4/PWM_38/PWM_39_N/TC_38_TR0/TC_39_TR1/ HIBERNATE_WAKEUP[0]	J55.1		GPIO_P21_4		
K17	P21_5/PWM_37/PWM_38_N/TC_37_TR0/TC_38_TR1/ PWM_34/PWM_35_N/ETH0_RX_CTL/LIN0_RX/ CAN1_1_TX/TRACE_DATA_0	J53.1		GPIO_P21_5	TRACE_DATA_0_1	AUTO_ETH_RXD-V_R
J17	P21_6/PWM_36/PWM_37_N/TC_36_TR0/TC_37_TR1/ LIN0_TX/LIN13_RX	P7.13		GPIO_P21_6		
J16	P21_7/PWM_35/PWM_36_N/TC_35_TR0/TC_36_TR1/ SCB6_RX/SCB6_MISO/LIN0_EN/LIN13_TX/CAL_SUP_NZ/ RTC_CAL	P3.10	JP1.6	BB_LIN0_SLP		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
H18	P22_1/PWM_33/PWM_34_N/TC_33_TR0/TC_34_TR1/ SCB6_TX/SCB6_SDA/SCB6_MOSI/CAN1_1_RX/TRACE_- DATA_1/EXT_PS_CTL0	P3.12		GPIO_P22_1	TRACE_DATA_1_1	EXT_PS_CTL0
G18	P22_2/PWM_32/PWM_33_N/TC_32_TR0/TC_33_TR1/ SCB6_RTS/SCB6_SCL/SCB6_CLK/TRACE_DATA_2/ EXT_PS_CTL1	J22.2		GPIO_P22_2	TRACE_DATA_2_1	EXT_PS_CTL1
F18	P22_3/PWM_31/PWM_32_N/TC_31_TR0/TC_32_TR1/ SCB6_CTS/SCB6_SEL0/TRACE_DATA_3/EXT_PS_CTL2	J37.2		GPIO_P22_3	TRACE_DATA_3_1	EXT_PS_CTL2
H17	P22_4/PWM_30/PWM_31_N/TC_30_TR0/TC_31_TR1/ SCB6_SEL1/TRACE_CLOCK	P2.4		TRACE_CLOCK_1		
H16	P22_5/PWM_29/PWM_30_N/TC_29_TR0/TC_30_TR1/ SCB6_SEL2/LIN7_RX	P3.9	JP7.8	BB_USER_LED5		
H15	P22_6/PWM_28/PWM_29_N/TC_28_TR0/TC_29_TR1/ LIN7_TX	P6.9	JP7.15	BB_USER_LED6		
G17	P22_7/PWM_27/PWM_28_N/TC_27_TR0/TC_28_TR1/ LIN14_RX/LIN7_EN	P3.15	JP7.7	BB_USER_LED7		
G16	P23_0/PWM_M_8/PWM_27_N/TC_M_8_TR0/TC_27_TR1/ SCB7_RX/LIN14_TX/SCB7_MISO/CAN1_0_TX/ FAULT_OUT_0	P3.11	JP6.7	BB_USER_LED8		
G15	P23_1/PWM_M_9/PWM_M_8_N/TC_M_9_TR0/ TC_M_8_TR1/SCB7_TX/SCB7_SDA/SCB7_MOSI/ CAN1_0_RX/FAULT_OUT_1	P1.12	JP6.6	BB_USER_LED9		
G13	P23_2/PWM_M_10/PWM_M_9_N/TC_M_10_TR0/ TC_M_9_TR1/SCB7_RTS/SCB7_SCL/SCB7_CLK/LIN6_RX/ FAULT_OUT_2	P13.13		BB_USER_LED10		
F17	P23_3/PWM_M_11/PWM_M_10_N/TC_M_11_TR0/ TC_M_10_TR1/ETH0_RX_CLK/SCB7_CTS/SCB7_SEL0/ LIN6_TX/FAULT_OUT_3/TRIG_IN[30]	P10.16		AUTO_ETH_RXC_R	AUTO_ETH_RXC	
F16	P23_4/PWM_25/PWM_M_11_N/TC_25_TR0/TC_M_11_TR1/ SCB2_MISO/SCB7_SEL1/TRIG_DBG[0]/SWJ_SWO_TDO/ TRIG_IN[31]	P2.2		SWO_TDO_PRM	SWO_TDO	
F15	P23_5/PWM_24/PWM_25_N/TC_24_TR0/TC_25_TR1/ LIN9_RX/SCB2_MOSI/SCB7_SEL2/SWJ_SWCLK_TCLK	P2.1		SWCLK_TCLK_PRM	SWCLK_TCLK	
E18	P23_6/PWM_23/PWM_24_N/TC_23_TR0/TC_24_TR1/ LIN9_TX/SCB2_CLK/SWJ_SWDIO_TMS	P3.14		SWDIO_TMS_PRM	SWDIO_TMS	

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
E17	P23_7/PWM_22/PWM_23_N/TC_22_TR0/TC_23_TR1/ EXT_CLK/LIN9_EN/SCB2_SEL0/CAL_SUP_NZ/ SWJ_SWDOE_TDI/HIBERNATE_WAKEUP[1]	P1.11		SWDOE_TDI_PRM	SWDOE_TDI	
J3	P24_0/EXT_CLK/SDHC_CARD_DETECT_N	P16.1		EMMC_CD		
J4	P24_1/SPIHB_CLK/SDHC_CARD_MECH_WRITE_PROT	J57.2		GPIO_P24_1	GM_CK_R	EMMC_WP
K1	P24_2/SPIHB_RWDS/SDHC_CLK_CARD	J64.2		GPIO_P24_2	GM_RWDS_R	EMMC_CLK
K2	P24_3/SPIHB_SEL0/SDHC_CARD_CMD	J58.2		GPIO_P24_3	GM_CS#0_R	EMMC_CMD
K3	P24_4/SPIHB_SEL1/SDHC_CARD_IF_PWR_EN	P17.16		GM_CS#1_R		
K4	P25_0/SPIHB_DATA0/SDHC_CARD_DAT_3TO0_0	J59.2		GPIO_P25_0	GM_DQ0_R	EMMC_DATA0
L1	P25_1/SPIHB_DATA1/SDHC_CARD_DAT_3TO0_1	J60.2		GPIO_P25_1	GM_DQ1_R	EMMC_DATA1
L2	P25_2/SPIHB_DATA2/SDHC_CARD_DAT_3TO0_2	J61.2		GPIO_P25_2	GM_DQ2_R	EMMC_DATA2
L3	P25_3/SPIHB_DATA3/SDHC_CARD_DAT_3TO0_3	J62.2		GPIO_P25_3	GM_DQ3_R	EMMC_DATA3
L4	P25_4/SPIHB_DATA4/SDHC_CARD_DAT_7TO4_0	P17.15		GM_DQ4_R		
M2	P25_5/SPIHB_DATA5/SDHC_CARD_DAT_7TO4_1	P17.9		GM_DQ5_R		
M3	P25_6/SPIHB_DATA6/SDHC_CARD_DAT_7TO4_2	P17.13		GM_DQ6_R		
M4	P25_7/SPIHB_DATA7/SDHC_CARD_DAT_7TO4_3	P17.11		GM_DQ7_R		
T8	P26_0	P9.12		GIG_ETH_REF_-CLK_R	GIG_ETH_REF_-CLK	
R8	P26_1	P11.3		GIG_ETH_TX_EN_C-TRL_R	GIG_ETH_TX-_EN_CTRL	
V9	P26_2	P9.11		GIG_ETH_TX_CLK_R	GIG_ETH_TX_CLK	GIG_ETH_REF_-CLK
U9	P26_3	P9.10		GIG_ETH_TX_D0_R	GIG_ETH_TX_D0	
T9	P26_4	P11.1		GIG_ETH_TX_D1_R	GIG_ETH_TX_D1	
R9	P26_5	P11.4		GIG_ETH_TX_D2_R	GIG_ETH_TX_D2	
V10	P26_6	P9.9		GIG_ETH_TX_D3_R	GIG_ETH_TX_D3	
U10	P26_7	P9.8		GIG_ETH_RX_D0_R	GIG_ETH_RX_D0	
T10	P27_0	P9.16		GIG_ETH_RX_D1_R	GIG_ETH_RX_D1	
R10	P27_1	P11.2		GIG_ETH_RX_D2_R	GIG_ETH_RX_D2	
V11	P27_2	P9.7		GIG_ETH_RX_D3_R	GIG_ETH_RX_D3	

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
U11	P27_3	P9.6		GIG_ETH_RX_DV_C-TRL_R	GIG_ETH_RX_D-V_CTRL	
T11	P27_4	P9.14		GIG_ETH_RX_CLK_R	GIG_ETH_RX_CLK	
R11	P27_5	P9.15		GIG_ETH_MDIO_R	GIG_ETH_MDIO	
T12	P27_6	P9.13		GIG_ETH_MDC_R	GIG_ETH_MDC	
R12	P27_7	P7.5		GPIO_P27_7		
E16	P28_0/SCB10_RX/SCB10_MISO	P6.16	JP12.3	BB_CAN_SPI1_MISO		
E15	P28_1/SCB10_TX/SCB10_SDA/SCB10_MOSI	P6.14	JP12.6	BB_CAN_SPI1_MOSI		
D18	P28_2/SCB10_RTS/SCB10_SCL/SCB10_CLK	P3.13	JP12.5	BB_CAN_SPI1_SCK		
D17	P28_3/SCB10_CTS/SCB10_SEL0	P15.1	JP10.10	BB_CAN_SPI1_SS0		
D16	P28_4/SCB10_SEL1	P14.1	JP10.9	BB_CAN_SPI1_SS1		
C18	P28_5/SCB10_SEL2	P3.16		GPIO_P28_5		
C17	P28_6/SCB10_SEL3	P6.15		GPIO_P28_6		
C16	P28_7	P15.2		GPIO_P28_7		
A11	P29_0	P8.2		GPIO_P29_0		
A10	P29_1	P8.5		GPIO_P29_1		
B10	P29_2	P8.4		BB_FRA_STBN		
C10	P29_3	P6.7		BB_FRA_WAKE		
D10	P29_4	P6.8		BB_FRA_ERRN		
A9	P29_5	P8.7		BB_FRB_STBN		
B9	P29_6	P8.6		BB_FRB_WAKE		
C9	P29_7	P6.6		BB_FRB_ERRN		
A13	P3_0/PWM_1/PWM_2_N/TC_1_TR0/TC_2_TR1/ETH0_M-DIO/PWM_H_6_N/SCB6_RX/SCB6_MISO/CAN0_3_TX/ TRIG_DBG[0]	P10.14		AUTO_ETH_MDIO_R	AUTO_ETH_MDIO	
A12	P3_1/PWM_0/PWM_1_N/TC_0_TR0/TC_1_TR1/ ETH0_MDC/PWM_H_7_N/SCB6_TX/SCB6_SDA/SCB6_-MOSI/CAN0_3_RX/TRIG_DBG[1]	P10.13		AUTO_ETH_MDC_R	AUTO_ETH_MDC	
B12	P3_2/PWM_M_3/PWM_0_N/TC_M_3_TR0/TC_0_TR1/ TC_H_4_TR1/SCB6_RTS/SCB6_SCL/SCB6_CLK	P15.10		GPIO_P3_2		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
C12	P3_3/PWM_M_2/PWM_M_3_N/TC_M_2_TR0/ TC_M_3_TR1/TC_H_5_TR1/SCB6_CTS/SCB6_SEL0	P15.7		GPIO_P3_3		
D12	P3_4/PWM_M_1/PWM_M_2_N/TC_M_1_TR0/ TC_M_2_TR1/TC_H_6_TR1/SCB6_SEL1/LIN1_RX	P15.11		GPIO_P3_4		
B11	P3_5/PWM_M_0/PWM_M_1_N/TC_M_0_TR0/ TC_M_1_TR1/TC_H_7_TR1/SCB6_SEL2/LIN1_TX	P15.12		GPIO_P3_5		
C11	P3_6/SCB8_SEL2/LIN11_TX/CAN1_2_TX	P6.10		GPIO_P3_6		
D11	P3_7/LIN11_EN/CAN1_2_RX	P15.14		GPIO_P3_7		
B7	P30_0/SCB9_RTS/SCB9_CLK	P8.10		GPIO_P30_0		
C7	P30_1/SCB9_CTS/SCB9_SEL0	P6.2		GPIO_P30_1		
D7	P30_2/SCB9_SEL1/CAN1_3_TX	P15.16		GPIO_P30_2		
F7	P30_3/SCB9_SEL2/CAN1_3_RX	P14.8		GPIO_P30_3		
A5	P31_0	P8.15		GPIO_P31_0		
B5	P31_1	P8.14		GPIO_P31_1		
A4	P31_2	P8.11		GPIO_P31_2		
C1	P32_0/SCB10_RX/SCB10_MISO/ADC[0]_8	P15.15		GPIO_P32_0		
C2	P32_1/SCB10_TX/SCB10_SDA/SCB10_MOSI/ADC[0]_9	P14.9		GPIO_P32_1		
D1	P32_2/SCB10_RTS/SCB10_SCL/SCB10_CLK/ADC[0]_10	P14.4	JP12.16	BB_GPIO_56_RESET		
D2	P32_3/SCB10_CTS/SCB10_SEL0/ADC[0]_11	P14.6		BB_SPI0_WP		
D3	P32_4/LIN10_RX/SCB10_SEL1/ADC[0]_12	P5.9	JP12.4	BB_SPI0_HOLD		
D4	P32_5/LIN10_TX/SCB10_SEL2/ADC[0]_13	P5.11	JP2.11	BB_LIN3_WAKE		
E3	P32_6/LIN10_EN/SCB10_SEL3/ADC[0]_14	P6.3	JP2.7	BB_LIN2_WAKE		
E4	P32_7/ADC[0]_15	P6.1	JP6.4	BB_LIN1_WAKE		
A8	P4_0/PWM_4/PWM_M_0_N/TC_4_TR0/TC_M_0_TR1/ EXT_MUX[0]_0/SCB5_RX/SCB5_MISO/LIN1_RX/ TRIG_IN[10]	P8.9	JP3.18	BB_SPI0_MISO		
B8	P4_1/PWM_5/PWM_4_N/TC_5_TR0/TC_4_TR1/ EXT_MUX[0]_1/SCB5_TX/SCB5_SDA/SCB5_MOSI/ LIN1_TX/TRIG_IN[11]	P8.8	JP3.16	BB_SPI0_MOSI		
C8	P4_2/PWM_6/PWM_5_N/TC_6_TR0/TC_5_TR1/ EXT_MUX[0]_2/SCB5_RTS/SCB5_SCL/SCB5_CLK/ LIN1_EN/TRIG_IN[12]	P15.4	JP9.17	BB_SPI0_CLK		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
D8	P4_3/PWM_7/PWM_6_N/TC_7_TR0/TC_6_TR1/ EXT_MUX[0]_EN/SCB5_CTS/SCB5_SEL0/CAN0_1_TX/ TRIG_IN[13]	P15.13		BB_SPI0_SS0		
A7	P4_4/PWM_8/PWM_7_N/TC_8_TR0/TC_7_TR1/LIN15_RX/ SCB5_SEL1/CAN0_1_RX	P14.2		AUDIO_SPI0_SS		
A6	P5_0/PWM_9/PWM_8_N/TC_9_TR0/TC_8_TR1/LIN15_TX/ SCB5_SEL2/LIN7_RX	P8.13	JP6.15	BB_LIN1_RXD		
B6	P5_1/PWM_10/PWM_9_N/TC_10_TR0/TC_9_TR1/SCB9_- SEL3/LIN7_TX	P8.12	JP6.14	BB_LIN1_TXD		
C6	P5_2/PWM_11/PWM_10_N/TC_11_TR0/TC_10_TR1/ LIN10_RX/LIN7_EN	P5.14	JP6.3	BB_LIN1_SLP		
D6	P5_3/PWM_12/PWM_11_N/TC_12_TR0/TC_11_TR1/ LIN10_TX/LIN2_RX	P5.15	JP2.5	BB_LIN2_RXD		
C5	P5_4/PWM_13/PWM_12_N/TC_13_TR0/TC_12_TR1/ LIN9_RX/LIN2_TX	P5.12	JP2.6	BB_LIN2_TXD		
D5	P5_5/PWM_14/PWM_13_N/TC_14_TR0/TC_13_TR1/ LIN9_TX/LIN2_EN	P5.13	JP2.8	BB_LIN2_SLP		
B4	P6_0/PWM_M_0/PWM_14_N/TC_M_0_TR0/TC_14_TR1/ LIN9_EN/SCB4_RX/SCB4_MISO/LIN3_RX/ADC[0]_0	P8.16	JP2.9	BB_LIN3_RXD		
C4	P6_1/PWM_0/PWM_M_0_N/TC_0_TR0/TC_M_0_TR1/ SCB4_TX/SCB4_SDA/SCB4_MOSI/LIN3_TX/ADC[0]_1	P5.10	JP2.10	BB_LIN3_TXD		
A3	P6_2/PWM_M_1/PWM_0_N/TC_M_1_TR0/TC_0_TR1/SDH- C_CARD_MECH_WRITE_PROT/SCB4_RTS/SCB4_SCL/ SCB4_CLK/LIN3_EN/CAN0_2_TX/ADC[0]_2	P8.3	JP2.12	BB_LIN3_SLP		
B3	P6_3/PWM_1/PWM_M_1_N/TC_1_TR0/TC_M_1_TR1/SPIH- B_CLK/SDHC_CARD_CMD/SCB4_CTS/SCB4_SEL0/ LIN4_RX/CAN0_2_RX/CAL_SUP_NZ/ADC[0]_3	P16.7		GPIO_P6_3		
C3	P6_4/PWM_M_2/PWM_1_N/TC_M_2_TR0/TC_1_TR1/SPIH- B_RWDS/SDHC_CLK_CARD/SCB4_SEL1/LIN4_TX/ ADC[0]_4	P16.5		GPIO_P6_4		
A2	P6_5/PWM_2/PWM_M_2_N/TC_2_TR0/TC_M_2_TR1/SPIH- B_SEL0/SDHC_CARD_DETECT_N/SCB4_SEL2/LIN4_EN/ ADC[0]_5	P13.10		GPIO_P6_5		
B2	P6_6/PWM_M_3/PWM_2_N/TC_M_3_TR0/TC_2_TR1/ SCB4_SEL3/TRIG_IN[8]/ADC[0]_6	P8.1	JP7.11	BB_ADC_POT		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
B1	P6_7/PWM_3/PWM_M_3_N/TC_3_TR0/TC_M_3_TR1/ TRIG_IN[9]/ADC[0]_7	P14.10		GPIO_P6_7		
E1	P7_0/PWM_M_4/PWM_3_N/TC_M_4_TR0/TC_3_TR1/SPIH-B_SEL1/SDHC_CARD_IF_PWR_EN/SCB5_RX/ SCB5_MISO/LIN4_RX/ADC[0]_16	P13.7		GPIO_P7_0		
E2	P7_1/PWM_15/PWM_M_4_N/TC_15_TR0/TC_M_4_TR1/ SPIHB_DATA0/SDHC_CARD_DAT_3TO0_0/SCB5_TX/ SCB5_SDA/SCB5_MOSI/LIN4_TX/ADC[0]_17	P13.8		GPIO_P7_1		
F1	P7_2/PWM_M_5/PWM_15_N/TC_M_5_TR0/TC_15_TR1/ SPIHB_DATA1/SDHC_CARD_DAT_3TO0_1/SCB5_RTS/ SCB5_SCL/SCB5_CLK/LIN4_EN/ADC[0]_18	P13.5		GPIO_P7_2		
F2	P7_3/PWM_16/PWM_M_5_N/TC_16_TR0/TC_M_5_TR1/ SPIHB_DATA2/SDHC_CARD_DAT_3TO0_2/SCB5_CTS/ SCB5_SEL0/ADC[0]_19	P16.8		GPIO_P7_3		
F3	P7_4/PWM_M_6/PWM_16_N/TC_M_6_TR0/TC_16_TR1/ SPIHB_DATA3/SDHC_CARD_DAT_3TO0_3/SCB5_SEL1/ ADC[0]_20	P16.3		GPIO_P7_4		
F4	P7_5/PWM_17/PWM_M_6_N/TC_17_TR0/TC_M_6_TR1/ SPIHB_DATA4/SDHC_CARD_DAT_7TO4_0/LIN10_RX/ SCB5_SEL2/ADC[0]_21	P16.6		GPIO_P7_5		
G1	P7_6/PWM_M_7/PWM_17_N/TC_M_7_TR0/TC_17_TR1/ LIN10_TX/TRIG_IN[16]/ADC[0]_22	P17.6		GPIO_P7_6		
G2	P7_7/PWM_18/PWM_M_7_N/TC_18_TR0/TC_M_7_TR1/ LIN10_EN/TRIG_IN[17]/ADC[0]_23	P17.5		GPIO_P7_7		
G3	P8_0/PWM_19/PWM_18_N/TC_19_TR0/TC_18_TR1/SPIH-B_DATA5/SDHC_CARD_DAT_7TO4_1/LIN2_RX/ CAN0_0_TX	P16.2		GPIO_P8_0		
G4	P8_1/PWM_20/PWM_19_N/TC_20_TR0/TC_19_TR1/SPIH-B_DATA6/SDHC_CARD_DAT_7TO4_2/LIN2_TX/ CAN0_0_RX/TRIG_IN[14]/ADC[0]_24	P16.4		GPIO_P8_1		
G6	P8_2/PWM_21/PWM_20_N/TC_21_TR0/TC_20_TR1/SPIH-B_DATA7/SDHC_CARD_DAT_7TO4_3/LIN2_EN/ TRIG_IN[15]/ADC[0]_25	P13.11		GPIO_P8_2		
H3	P8_3/PWM_22/PWM_21_N/TC_22_TR0/TC_21_TR1/ TRIG_DBG[0]/ADC[0]_26	P13.6	JP7.18	BB_USER_LED0		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
H4	P8_4/PWM_23/PWM_22_N/TC_23_TR0/TC_22_TR1/ TRIG_DBG[1]/ADC[0]_27	P4.11	JP7.10	BB_USER_LED1		
H1	P9_0/PWM_24/PWM_23_N/TC_24_TR0/TC_23_TR1/ ADC[0]_28	P4.12	JP7.13	BB_USER_LED2		
H2	P9_1/PWM_25/PWM_24_N/TC_25_TR0/TC_24_TR1/ LIN12_RX/ADC[0]_29	P4.10	JP7.9	BB_USER_LED3		
J1	P9_2/PWM_26/PWM_25_N/TC_26_TR0/TC_25_TR1/ LIN12_TX/ADC[0]_30	P4.2	JP7.14	BB_USER_LED4		
J2	P9_3/PWM_27/PWM_26_N/TC_27_TR0/TC_26_TR1/ LIN12_EN/ADC[0]_31	P17.7		GPIO_P9_3		
F13	VCCD	J14.1		CPU_VCCD		
N6	VCCD	J14.1		CPU_VCCD		
N13	VCCD	J14.1		CPU_VCCD		
F6	VCCD	J14.1		CPU_VCCD		
L6	VDDA	J19.2		CPU_VDDA		
J13	VDDD	J17.2		CPU_VDDD		
K13	VDDD	J17.2		CPU_VDDD		
L13	VDDD	J17.2		CPU_VDDD		
N11	VDDD	J17.2		CPU_VDDD		
H13	VDDD	J17.2		CPU_VDDD		
F8	VDDD	J17.2		CPU_VDDD		
F10	VDDIO_1	J16.2		CPU_VDDIO1		
F9	VDDIO_1	J16.2		CPU_VDDIO1		
F11	VDDIO_1	J16.2		CPU_VDDIO1		
N8	VDDIO_2	J18.2		CPU_VDDIO2		
H6	VDDIO_3	J21.1		CPU_VDDIO3		
J6	VDDIO_3	J21.1		CPU_VDDIO3		
N9	VDDIO_4	J20.1		CPU_VDDIO4		
N10	VDDIO_4	J20.1		CPU_VDDIO4		
K6	VREFH	TP36.1		CPU_VDDA_R		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
K8	VREFL	TP35.1		AGND_R		
L8	VSSA	R146.2		AGND		
A18	VSSD	J1.1		DGND		
D9	VSSD	J1.1		DGND		
G7	VSSD	J1.1		DGND		
G12	VSSD	J1.1		DGND		
H9	VSSD	J1.1		DGND		
H10	VSSD	J1.1		DGND		
H11	VSSD	J1.1		DGND		
J9	VSSD	J1.1		DGND		
J10	VSSD	J1.1		DGND		
J11	VSSD	J1.1		DGND		
J15	VSSD	J1.1		DGND		
K9	VSSD	J1.1		DGND		
K10	VSSD	J1.1		DGND		
K11	VSSD	J1.1		DGND		
L18	VSSD	J1.1		DGND		
A1	VSSD	J1.1		DGND		
M7	VSSD	J1.1		DGND		
M12	VSSD	J1.1		DGND		
R5	VSSD	J1.1		DGND		
R14	VSSD	J1.1		DGND		
V1	VSSD	J1.1		DGND		
V18	VSSD	J1.1		DGND		
P18	VSSD	J1.1		DGND		
L11	VSSD	J1.1		DGND		
J8	VSSD	J1.1		DGND		

Table 4-1. Device Port Pin Connections on Base Board *(continued)*

MCU Pad No	Multiplexed Pin Functions	CPU Board Test Points	Base Board Test Points	Connection 1	Connection 2	Connection 3
H8	VSSD_1	J1.1		DGND		
L9	VSSIO_3	J1.1		DGND		
L10	VSSIO_3	J1.1		DGND		
K18	XRES	J27.1		CPU_XRES		

The first column in Table 4-1 lists the pin number on the MCU, followed by the port pin name.

For each pin, the connected peripheral or net on the base board is depicted by the depicted by Connection 1 column.

The Base Board Test Point column indicates the place where the signal can be probed on the base board. For example, JP6.15 refers to the 15th pin on the JP6 header.

A value of NA in the Test Point column indicates that the signal is unavailable on the JPx pin header on the base board. The signal might still be available on separate pin headers near the respective peripheral.

For details on the alternate functionality of each MCU pin, see the device datasheet.

Note: If there are pins with more than one connection to the base board, make sure that no two peripherals are driven at the same time. The unused peripheral jumpers must be disconnected before using the other connection.

4.1.2 Reset Switch

The correspondence between the Reset switch and port number is given in Table 4-2.

Table 4-2. Reset Switch

Switch	Part No.	Port Name
Reset Switch	SW3	XRES

4.1.3 User Switch

The correspondence between the User switch and port number is given in Table 4-3.

Table 4-3. User Switch

Push Button	Part No.	Port Name
User Button 1	SW1	P16.6
User Button 2	SW4	P17.3
User Button 3 / Hibernate Wakeup button	SW5	P21.4

4.1.4 User LED

The correspondence between the User LED and port number is given in Table 4-4.

Table 4-4. User LED

LED	Part No.	Port Name
User LED 1	LD1	P16.4
User LED 2	LD2	P16.5
User LED 3	LD3	P16.7

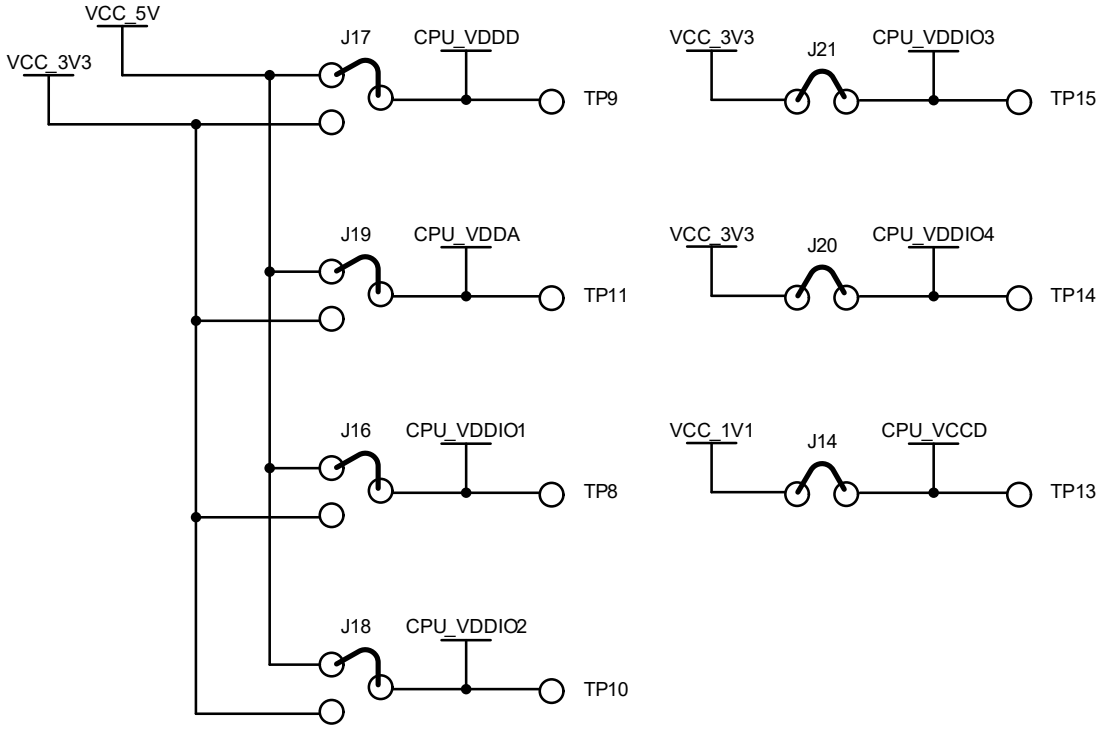
4.2 Power Supply Settings

Power supply settings are shown in Table 4-5 and Figure 4-1.

Table 4-5. Power Supply Jumpers Settings

Jumper	Pin	MCU Power	Remarks
J17	1-2 (default)	VDDD = +5.0 V	
	2-3	VDDD = +3.3 V	
J19	1-2 (default)	VDDA = +5.0 V	
	2-3	VDDA = +3.3 V	
J16	1-2 (default)	VDDIO_1 = +5.0 V	
	2-3	VDDIO_1 = +3.3 V	
J18	1-2 (default)	VDDIO_2 = +5.0 V	
	2-3	VDDIO_2 = +3.3 V	
J21	1-2 (default)	VDDIO_3 = +3.3 V	
J20	1-2 (default)	VDDIO_4 = +3.3 V	
J14	1-2 (default)	VCCD = +1.1 V	

Figure 4-1. Power Supply Jumpers Settings



4.3 External Power Supply Control Signals Settings

Jumper settings of the external power supply control signals from MCU are shown in Table 4-6.

Table 4-6. External Power Supply Control Signals Jumper Settings

Jumpers Name	PASS Transistor	S6BP501A	Remarks
EXT_PS_CTL0	J11	J6	J11 open (default)
			J6 closed (default)
EXT_PS_CTL1	J8	J9	J8 open (default)
			J9 closed (default)
EXT_PS_CTL2	-	R11	Connected a 0-ohm resistor (R11)
DRV_VOUT	R34	-	Close R34 only in Pass transistor mode
VCC_1V1_PMIC	J15(1-2)	J15(2-3)	J15(2-3) closed (default)

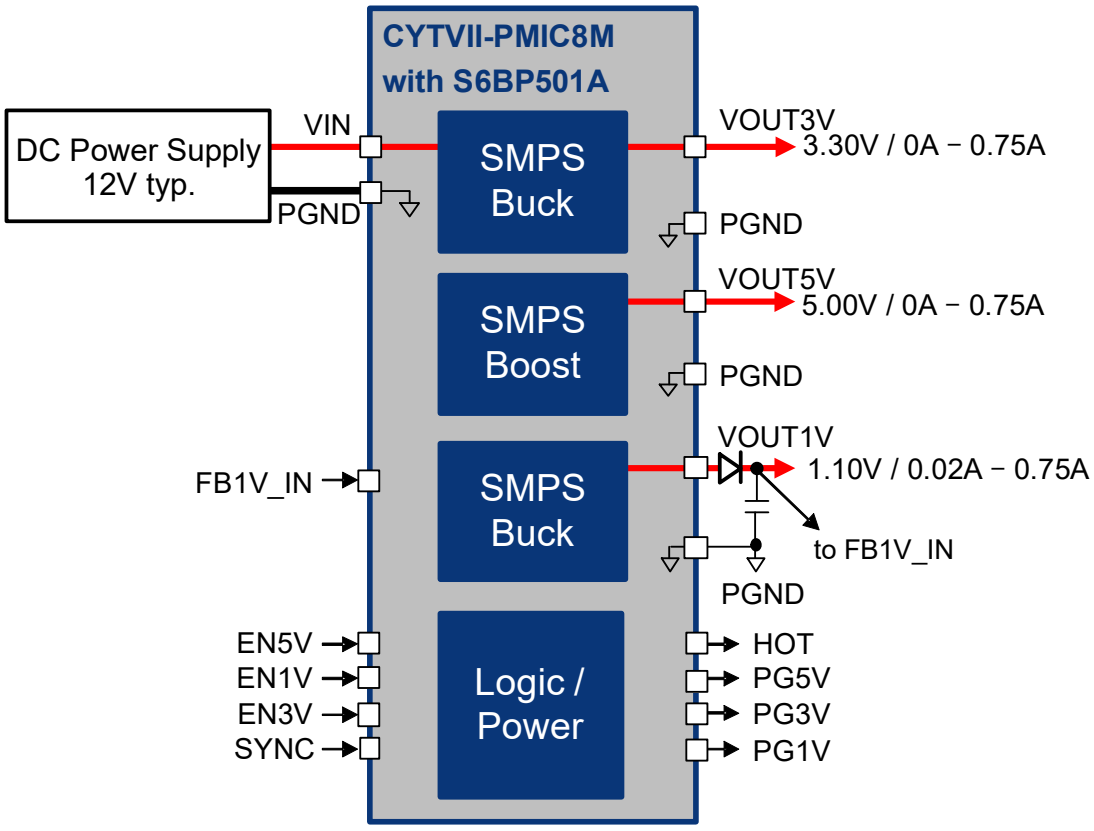
5. Power Management IC (PMIC)

5.1 Power Management IC (PMIC) Module

5.1.1 PMIC Module - CYTVII-PMIC8M

CYTVII-PMIC8M is the PMIC module for the power block of an automotive application with CYT4B Series MCU. The PMIC module implements the Cypress PMIC S6BP501A and is optimized for power supply of CYT4B Series MCU. 1.1-V output of the supply to VCCD of CYT4B Series MCU needs external schottky barrier diode (SBD), output capacitor, and constant load current no less than 20 mA.

Figure 5-1. Evaluation Board Block Diagram



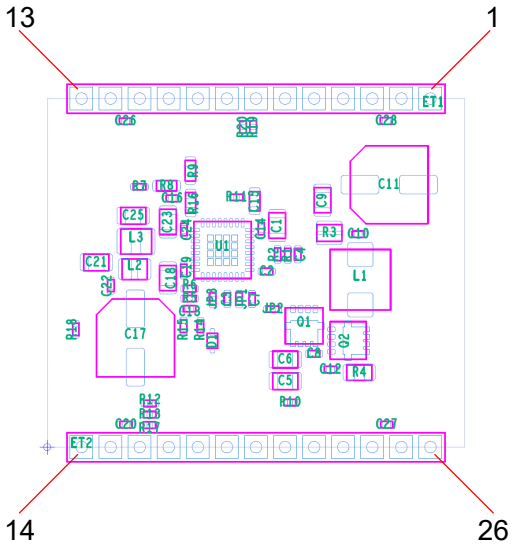
*SMPS: Switching Mode Power Supply

5.1.2 Input / Output Pin Descriptions

Table 5-1. Input / Output Pin Descriptions

Connector Symbol		I/O	Function Description
1, 2	VOUT3V	O	3.3 V power rail output terminal (0 A - 0.75 A)
3, 4	PGND	O	Ground terminal
5	SYNC	I	Mode setting or external clock input terminal Refer to the S6BP501A datasheet
6	PG1V	O	Power good terminal of 1.1 V power rail
7	PG3V	O	Power good terminal of 3.3 V power rail
8	PG5V	O	Power good terminal of 5 V power rail
9	FB1V_IN	I	Feed-back terminal for 1.1 V power rail
10, 11	PGND	–	Ground terminal
12, 13	VOUT1V	O	1.1 V output terminal (0 A - 0.75 A)
14, 15	VOUT5V	O	5 V output terminal (0 A - 0.75 A)
16, 17	PGND	–	Ground terminal
18	HOT	O	Thermal warning output terminal
19	EN5V	I	5 V power rail output enable terminal
20	EN3V	I	3.3 V power rail output enable terminal
21	EN1V	I	1.1 V power rail output enable terminal
22	N.C.	N.C.	No connection
23, 24	PGND	–	Ground terminal
25, 26	VIN	I	DC power supply terminal (4.5 V-42 V, 12 V typ.)

Figure 5-2. Pin Layout



A. Schematics of CPU Board

This appendix contains the schematics of CYTVII-B-H-4M-272-CPU board.

Figure A-1. Block Diagram

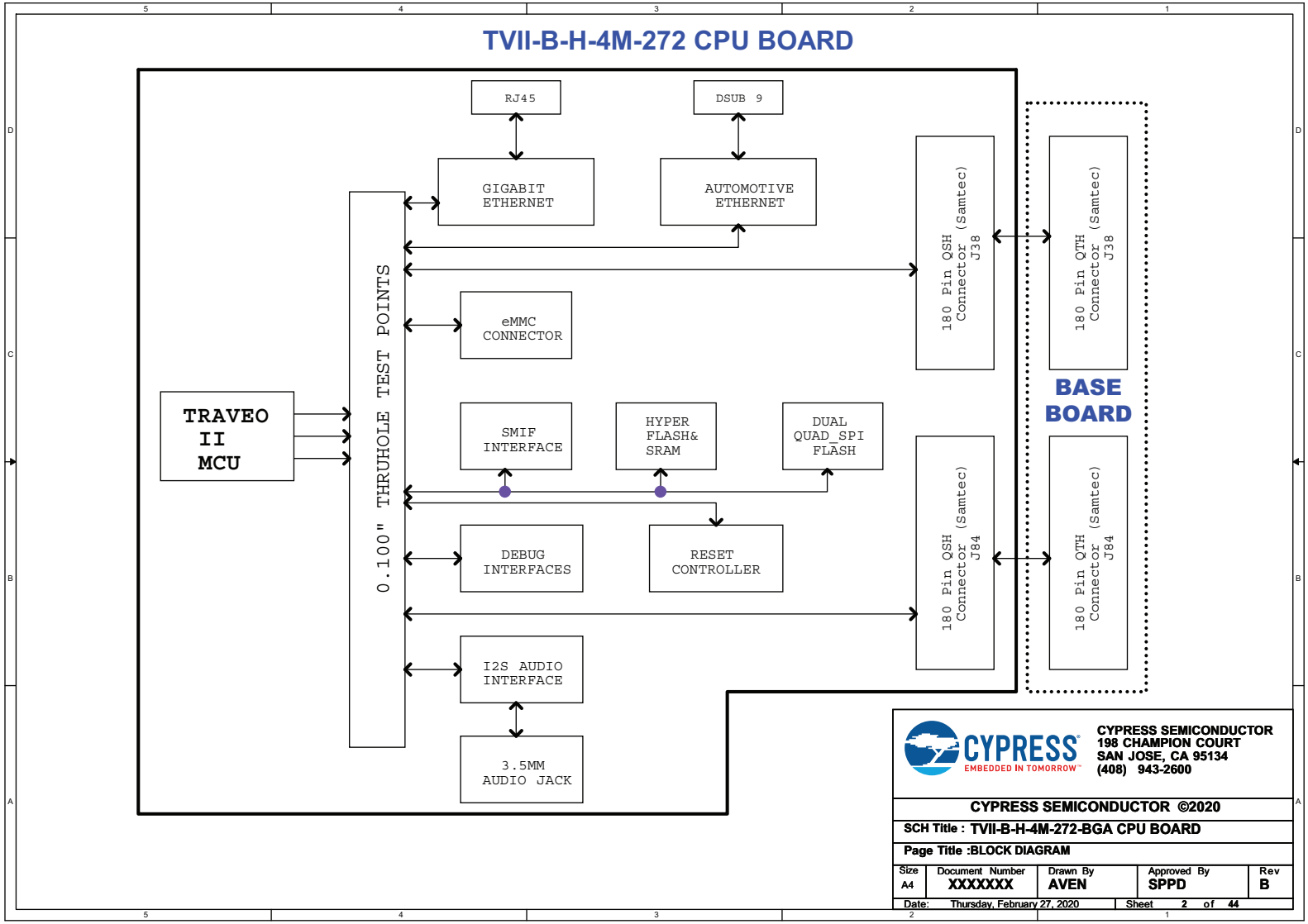


Figure A-2. Power Architecture

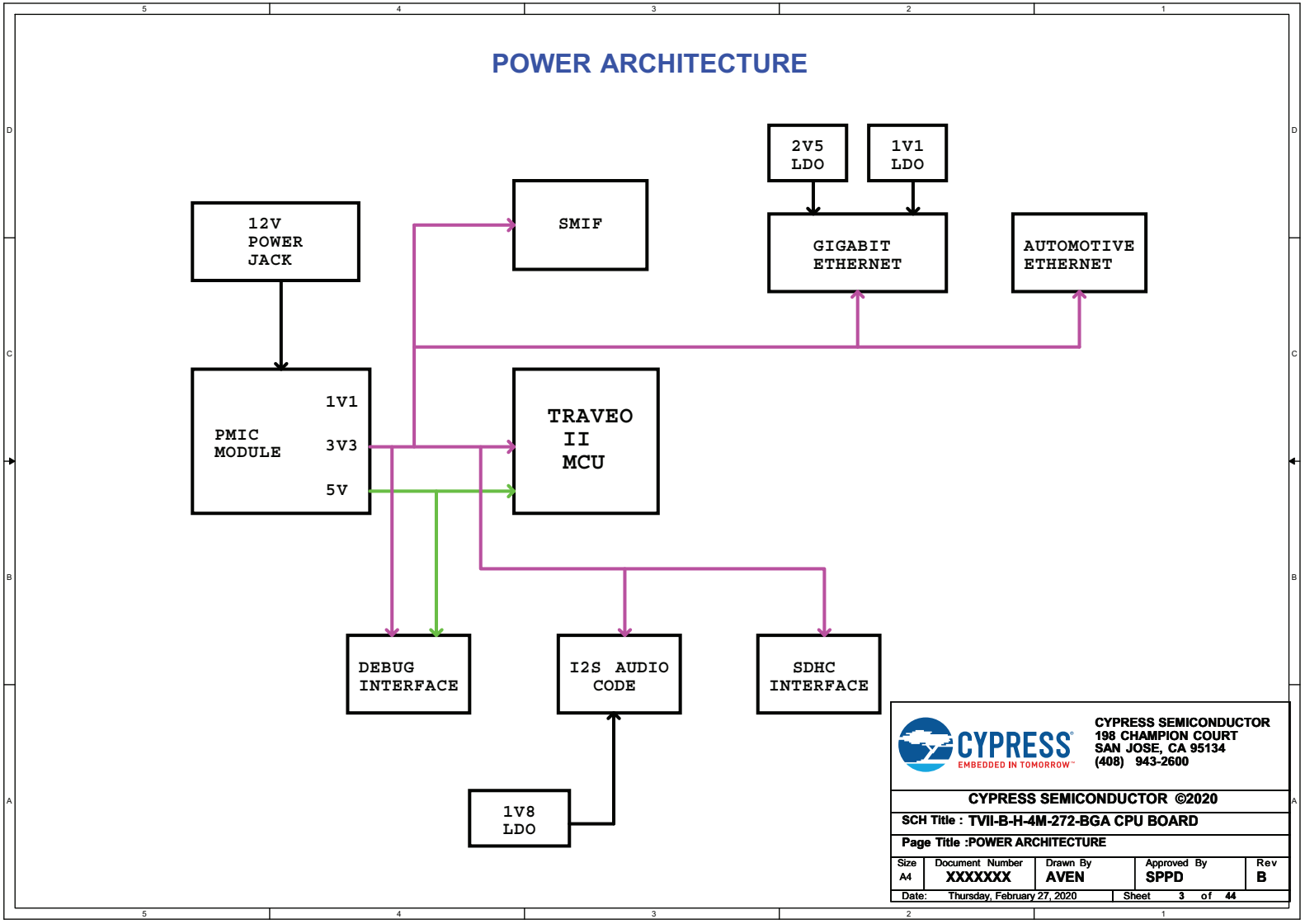


Figure A-3. Power Input-1

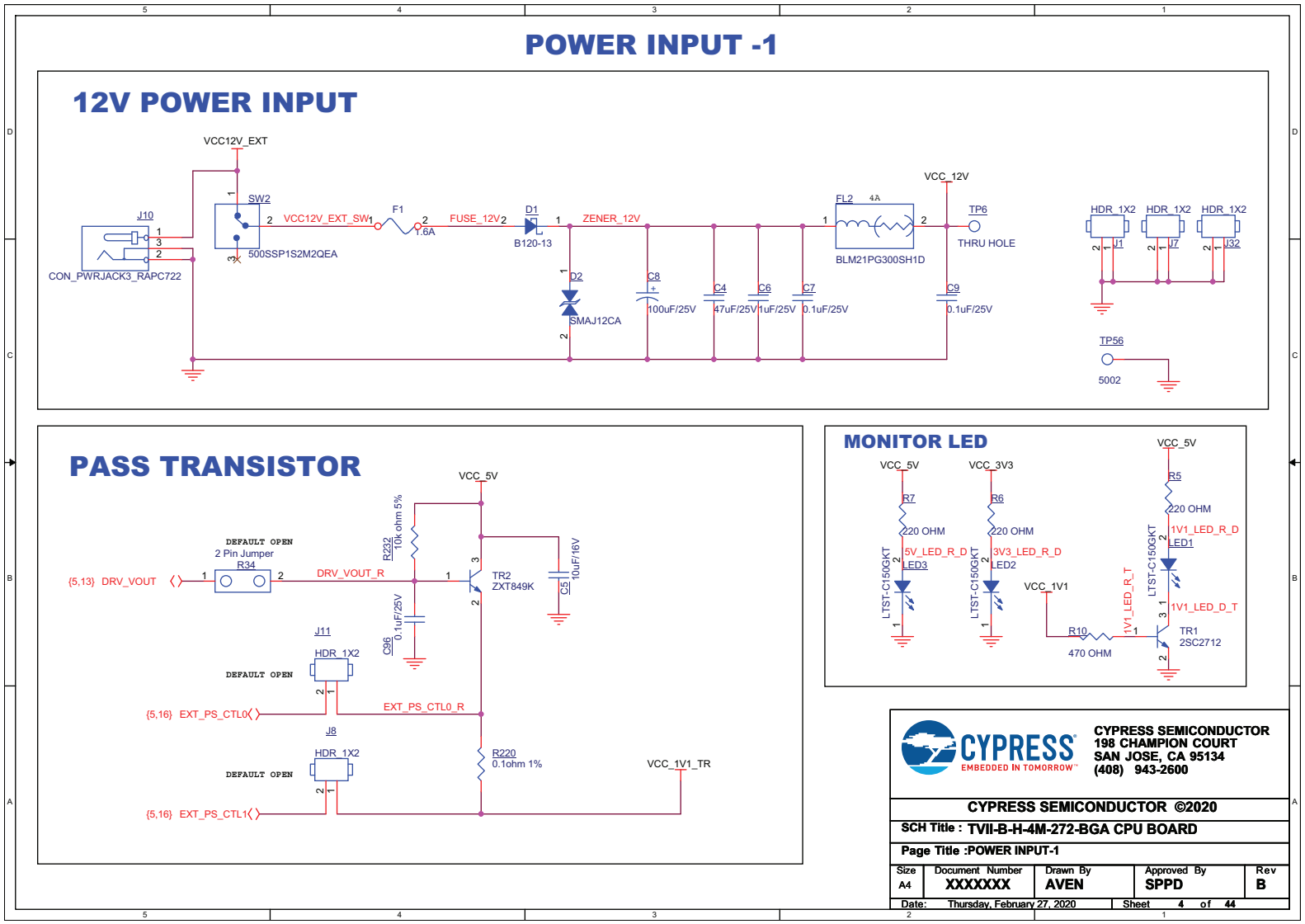


Figure A-4. Power Input-2

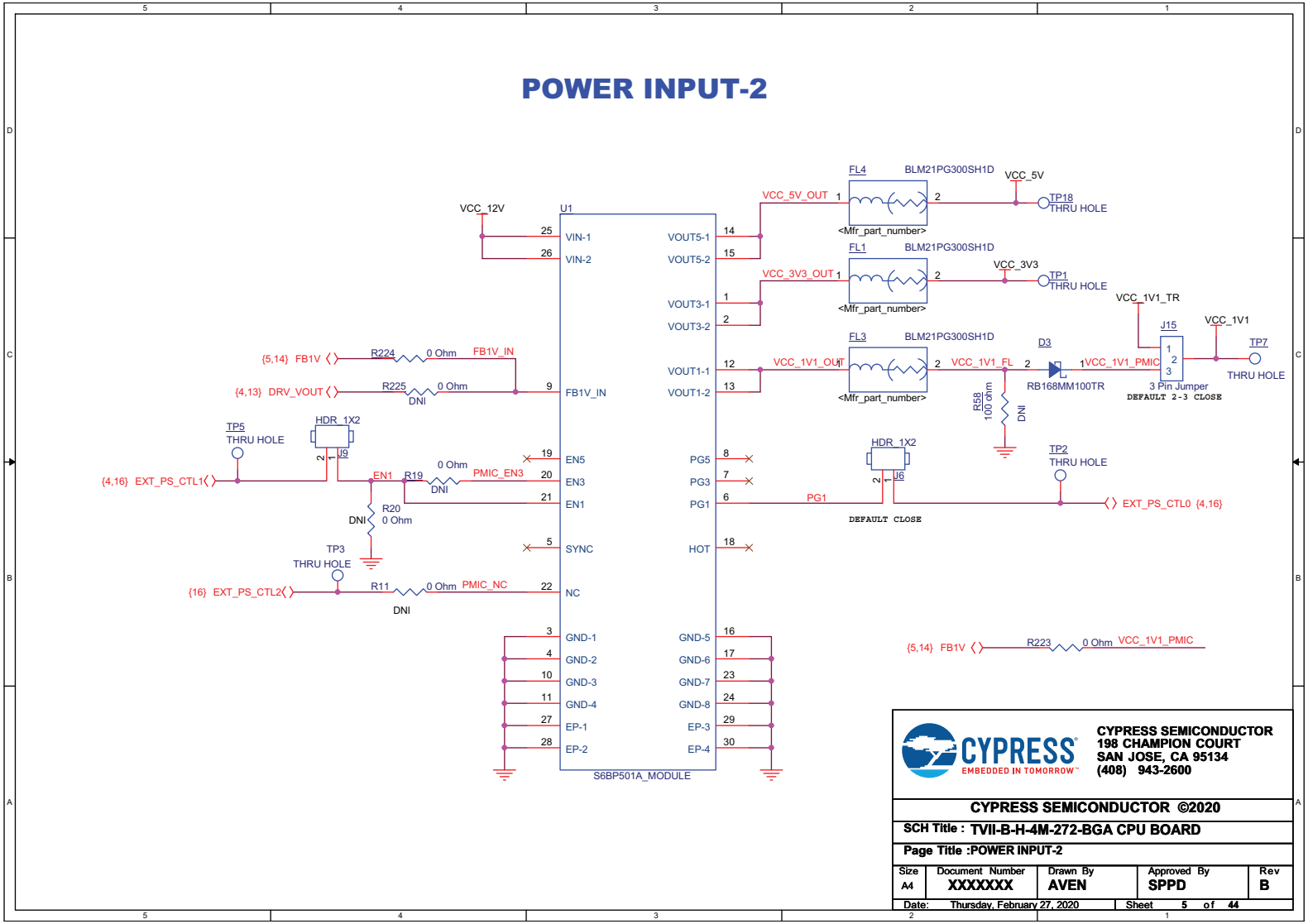


Figure A-5. Power Input-3

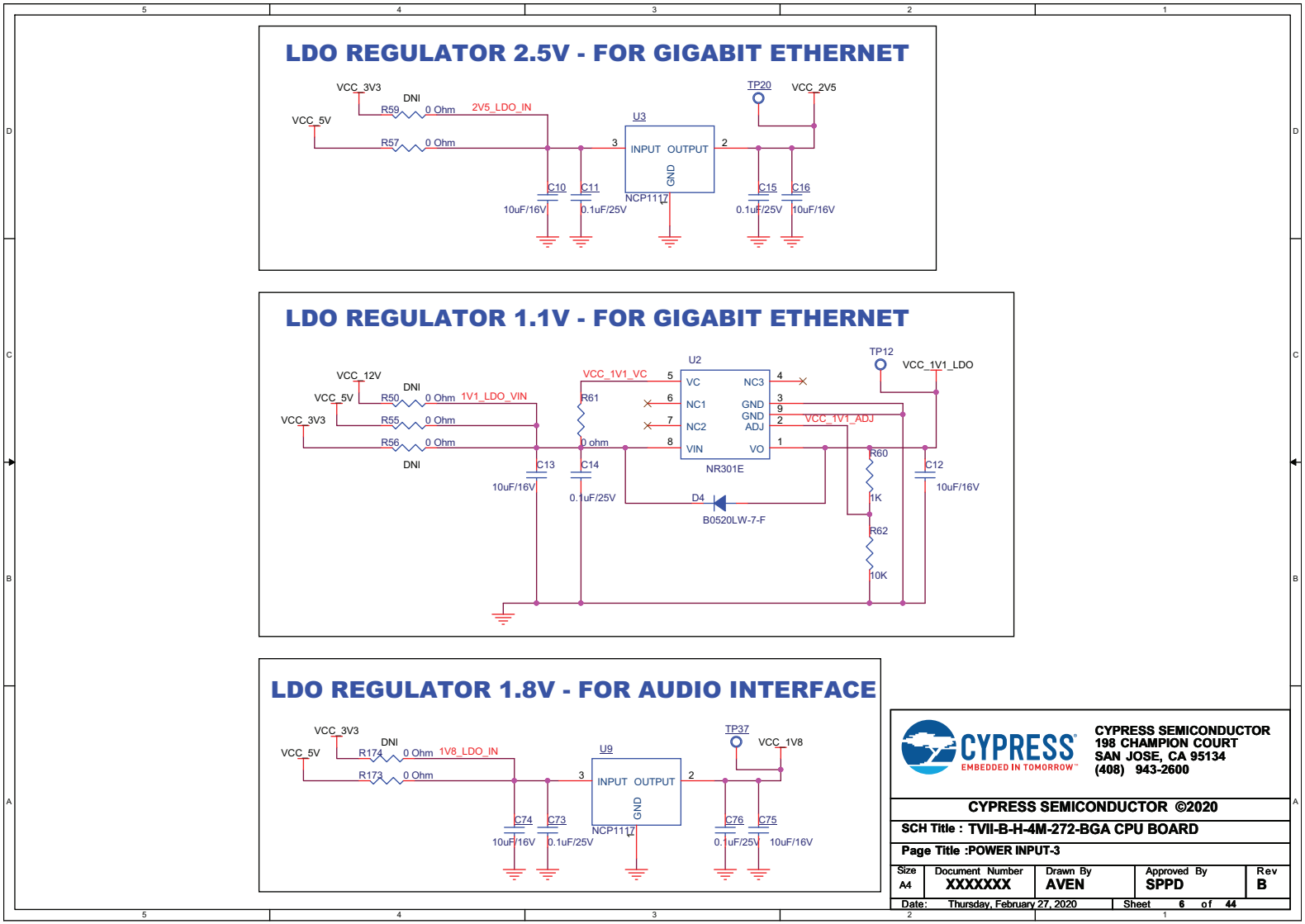


Figure A-6. MCU Power Rail-Supply Select

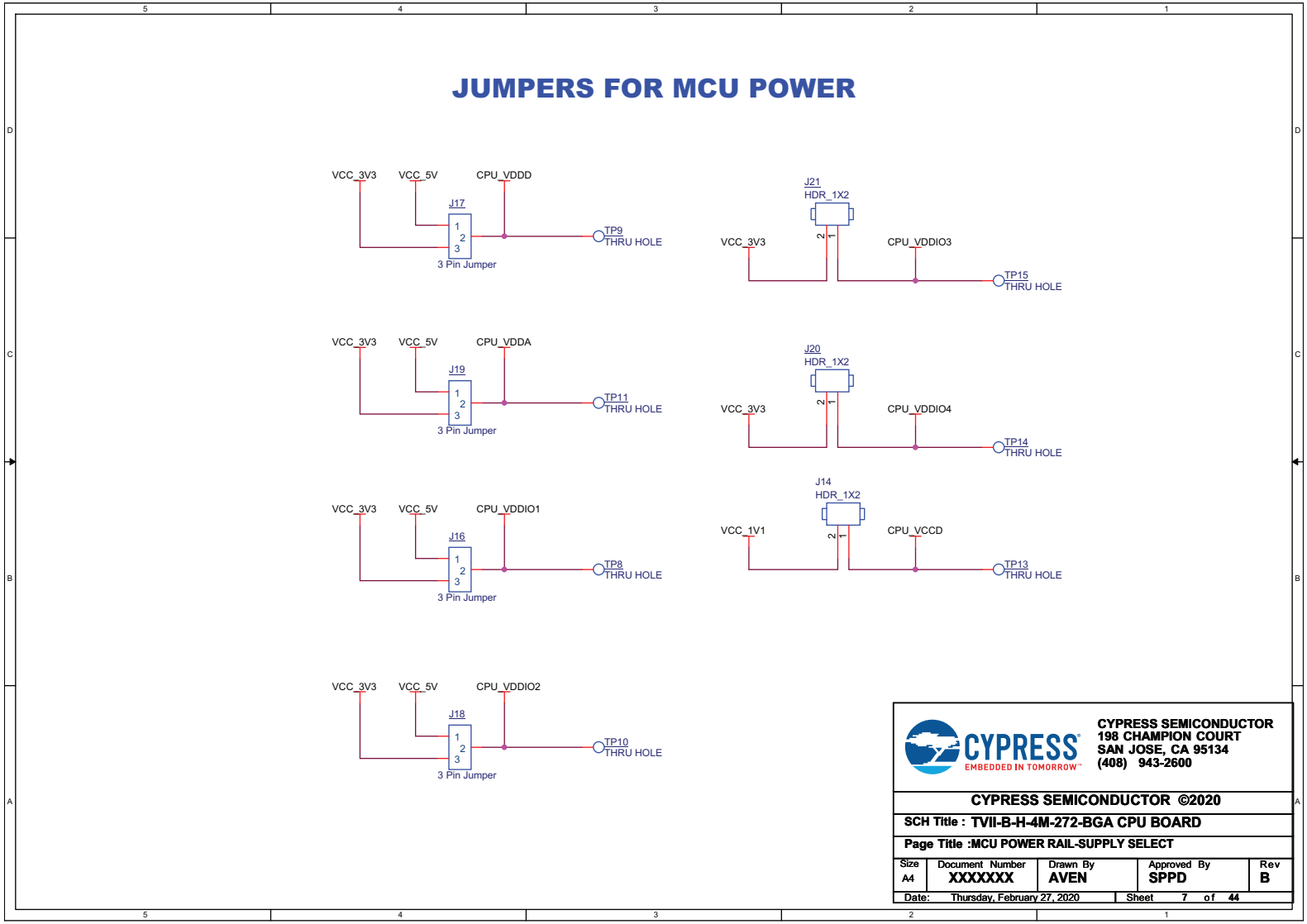


Figure A-7. TVII-B-H-4M-272-BGA

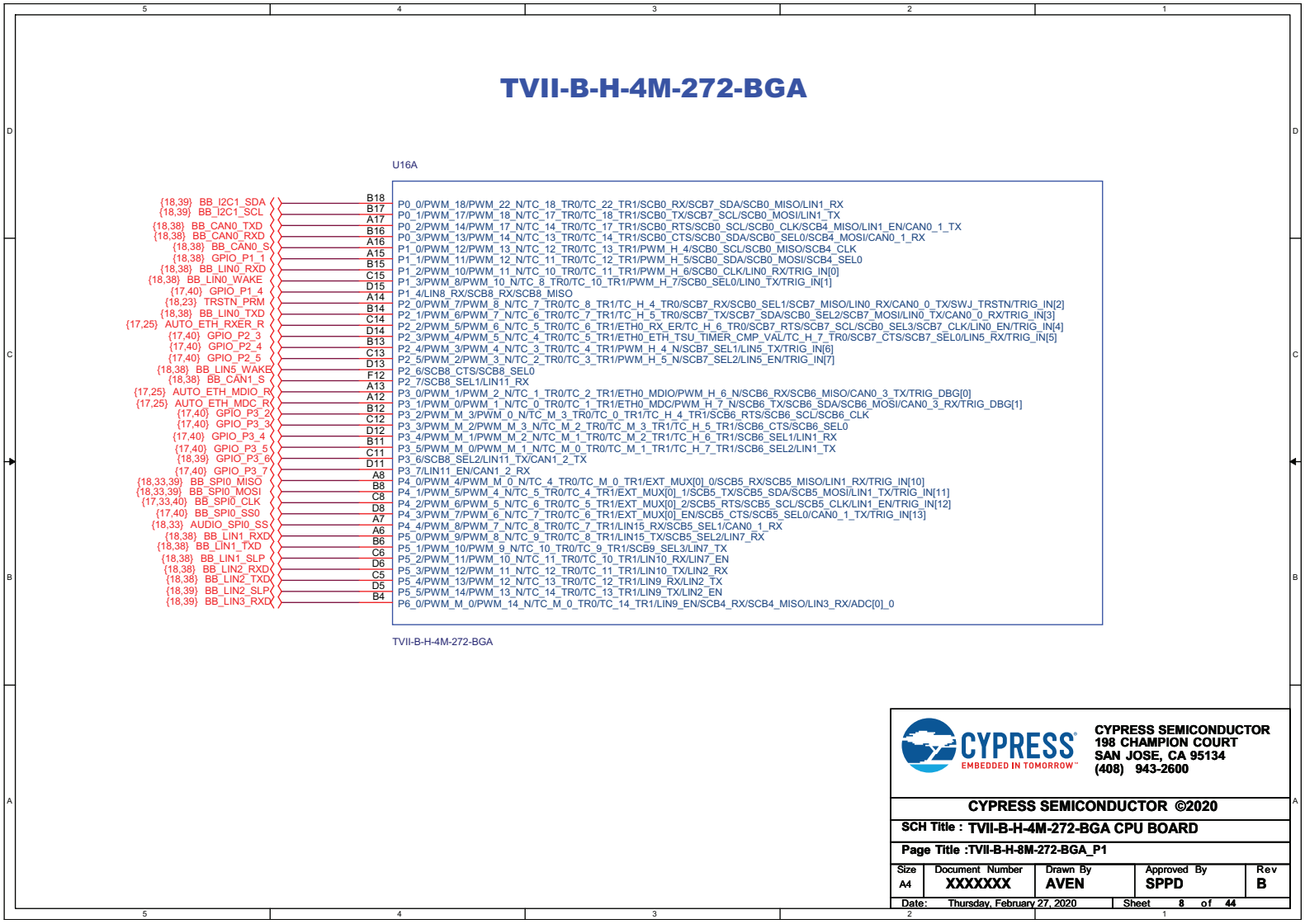


Figure A-8. TVII-B-H-4M-272-BGA

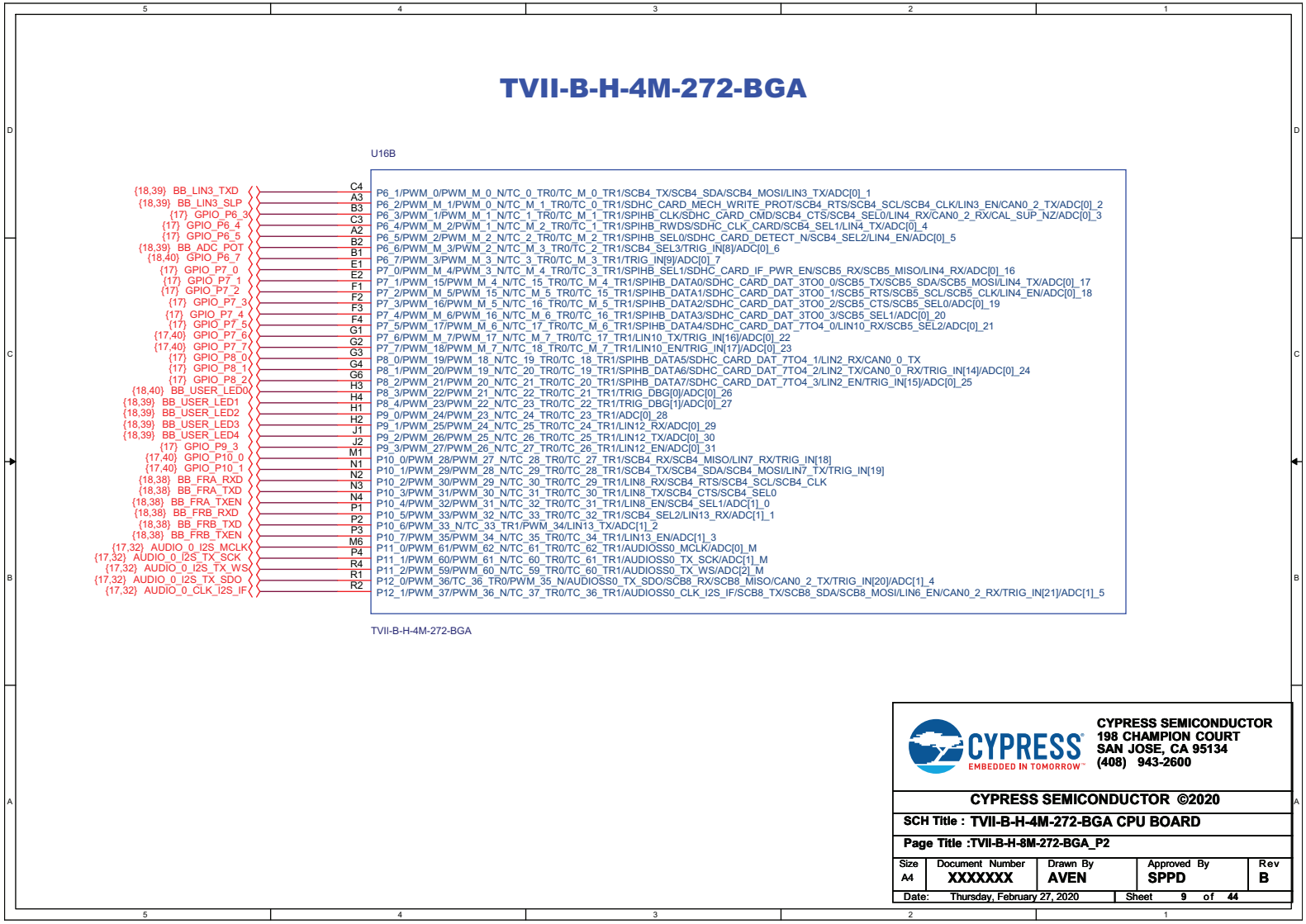


Figure A-9. TVII-B-H-4M-272-BGA

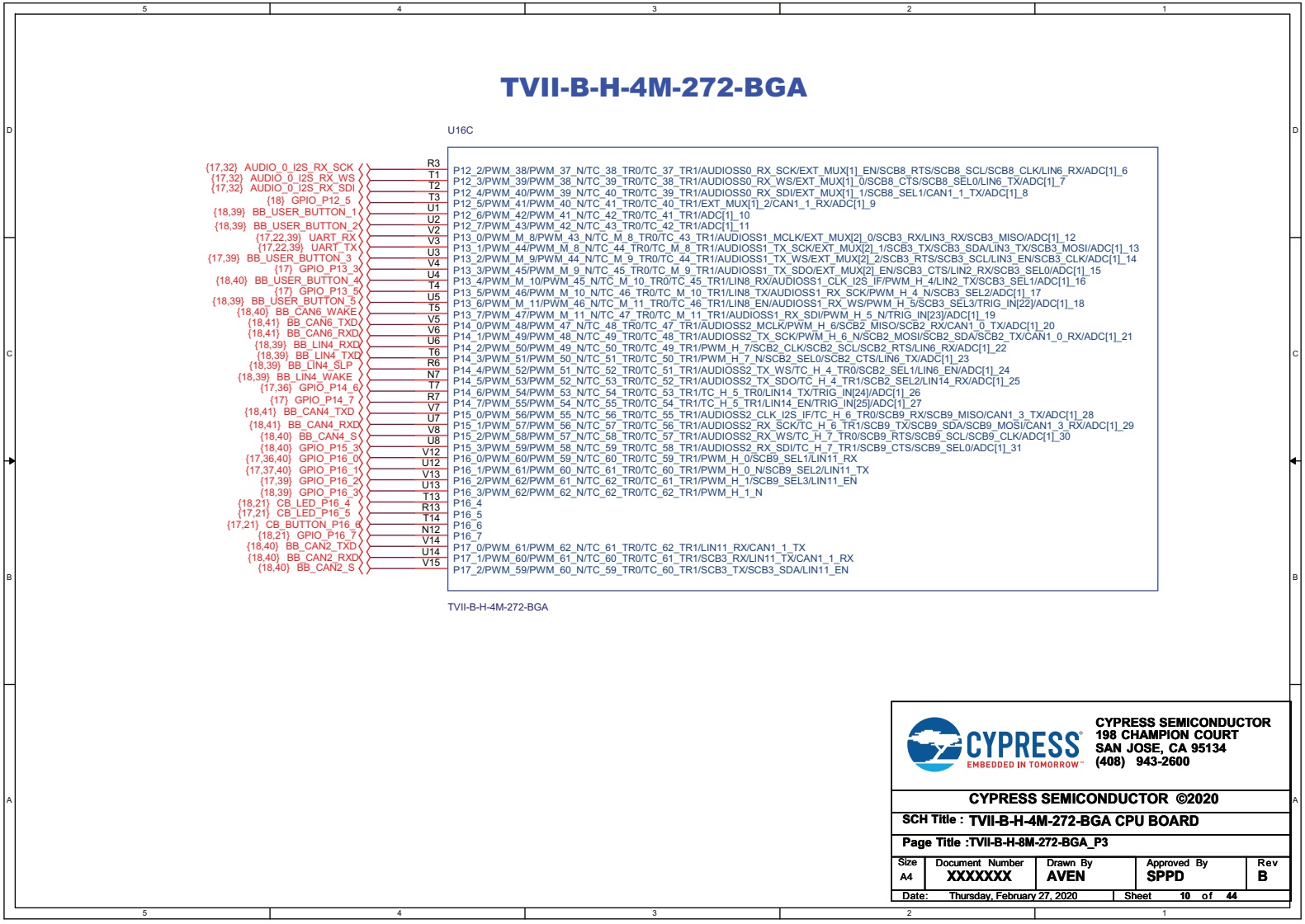


Figure A-10. TVII-B-H-4M-272-BGA

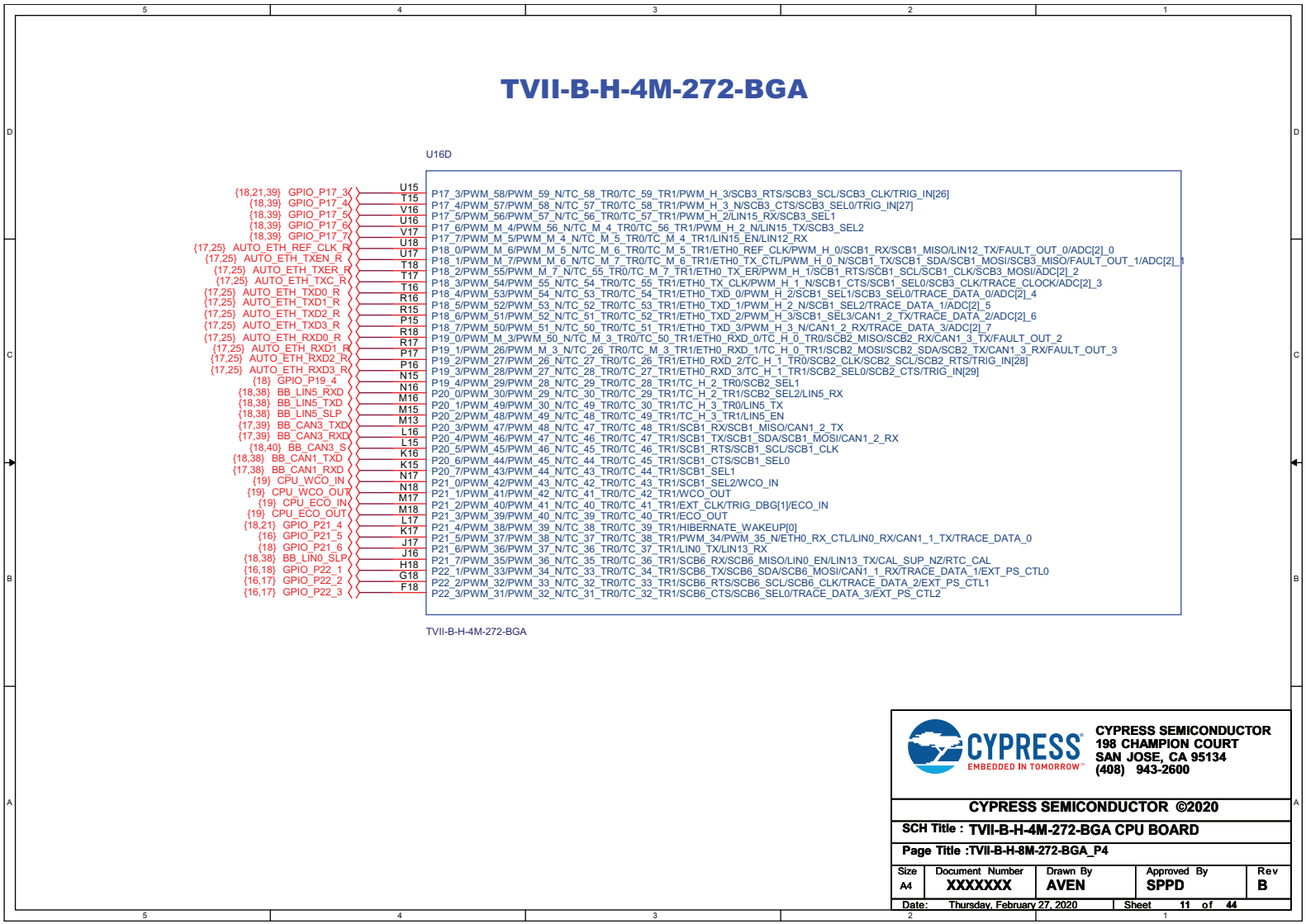


Figure A-11. TVII-B-H-4M-272-BGA

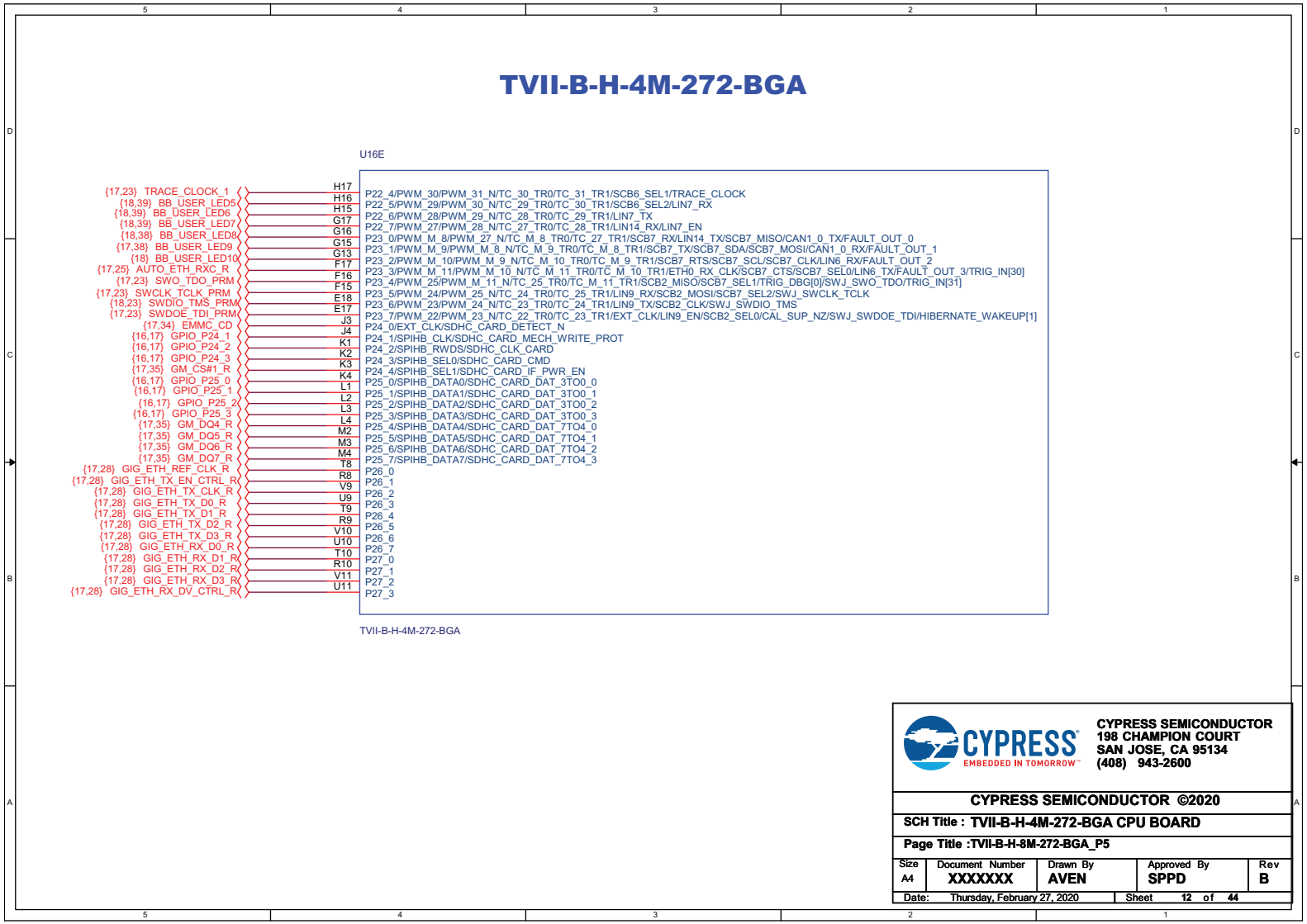


Figure A-12. TVII-B-H-4M-272-BGA

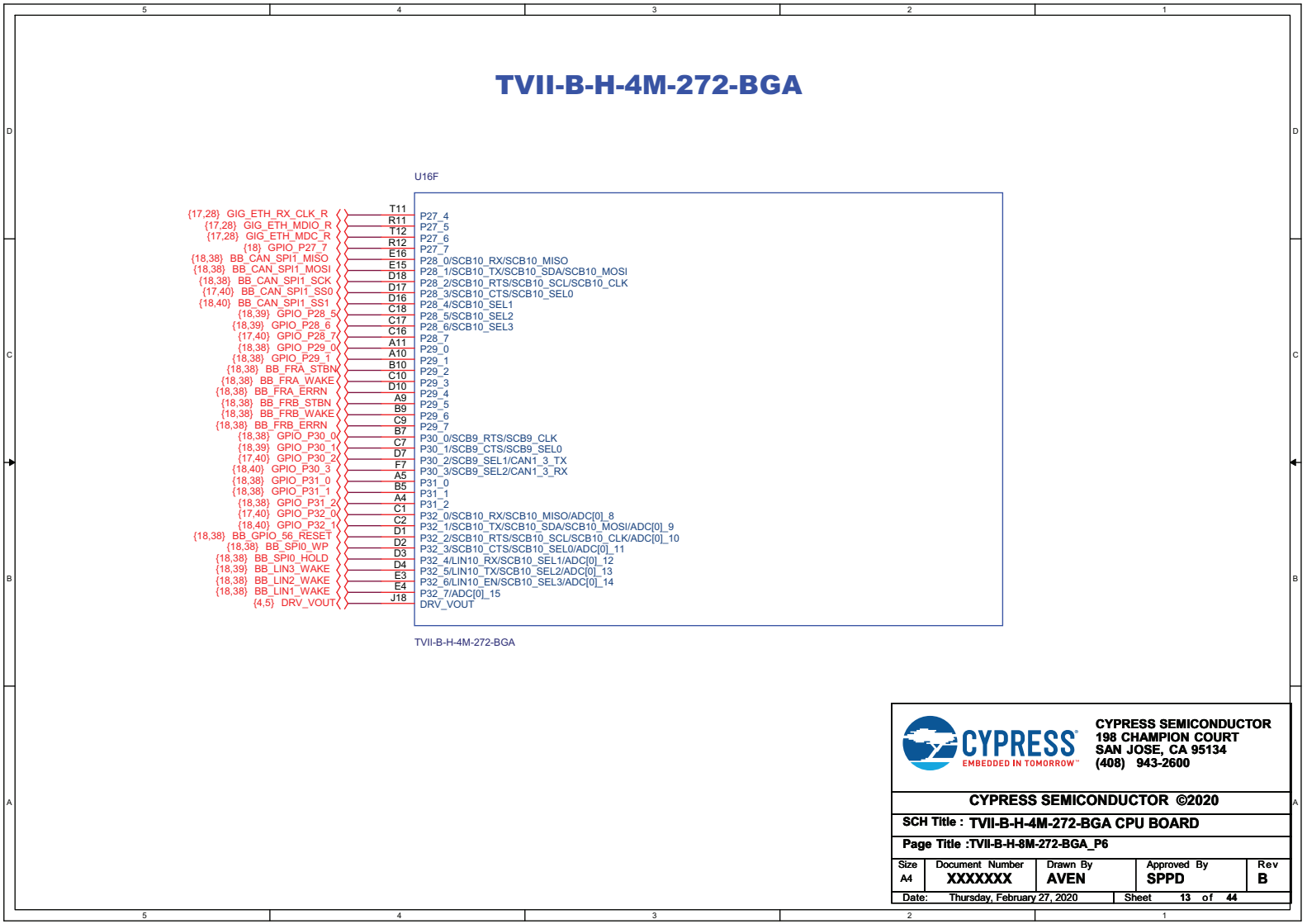


Figure A-13. TVII-B-H-4M-272-BGA

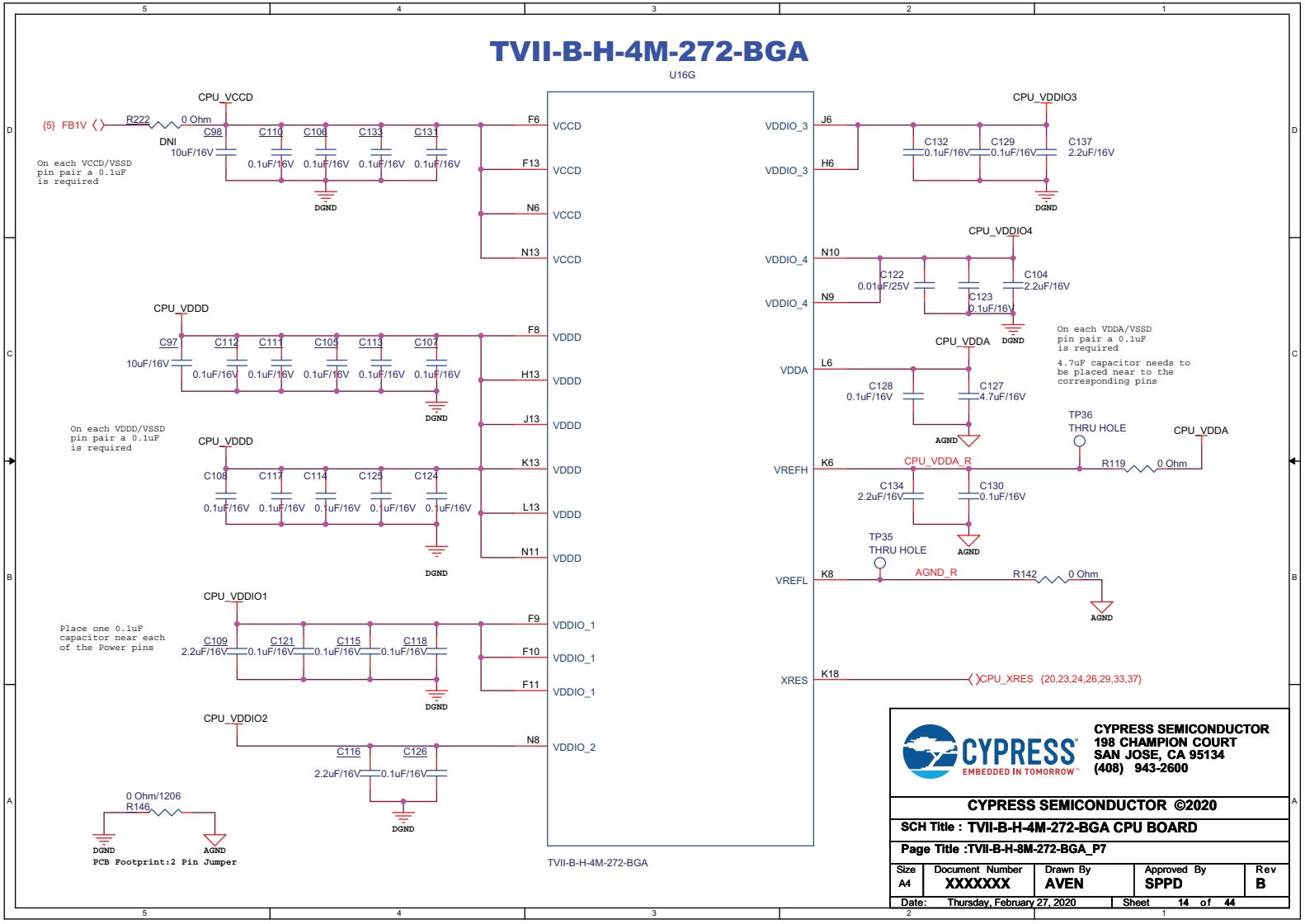


Figure A-14. TVII-B-H-4M-272-BGA

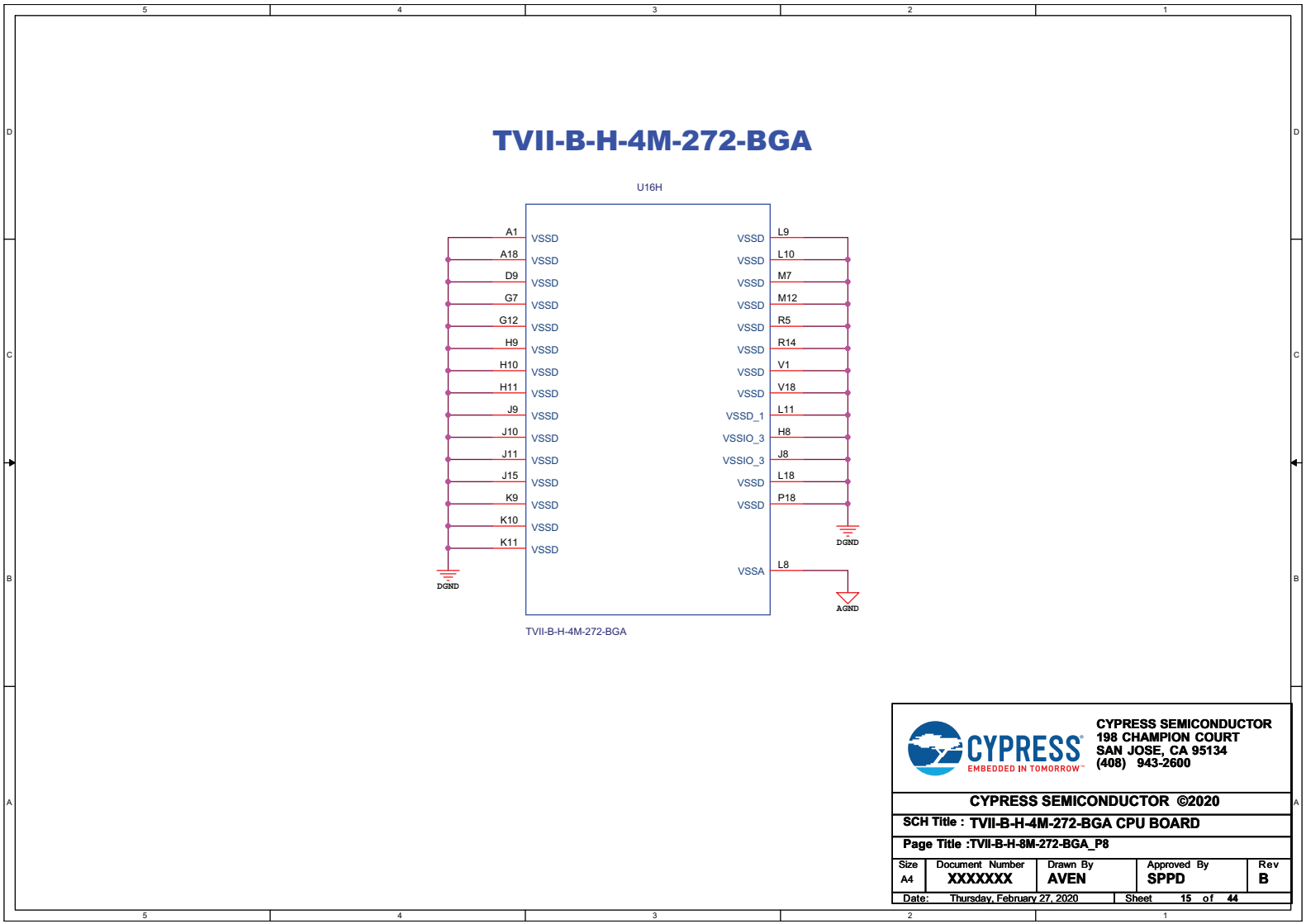


Figure A-15. MCU Port Pin Mux Options

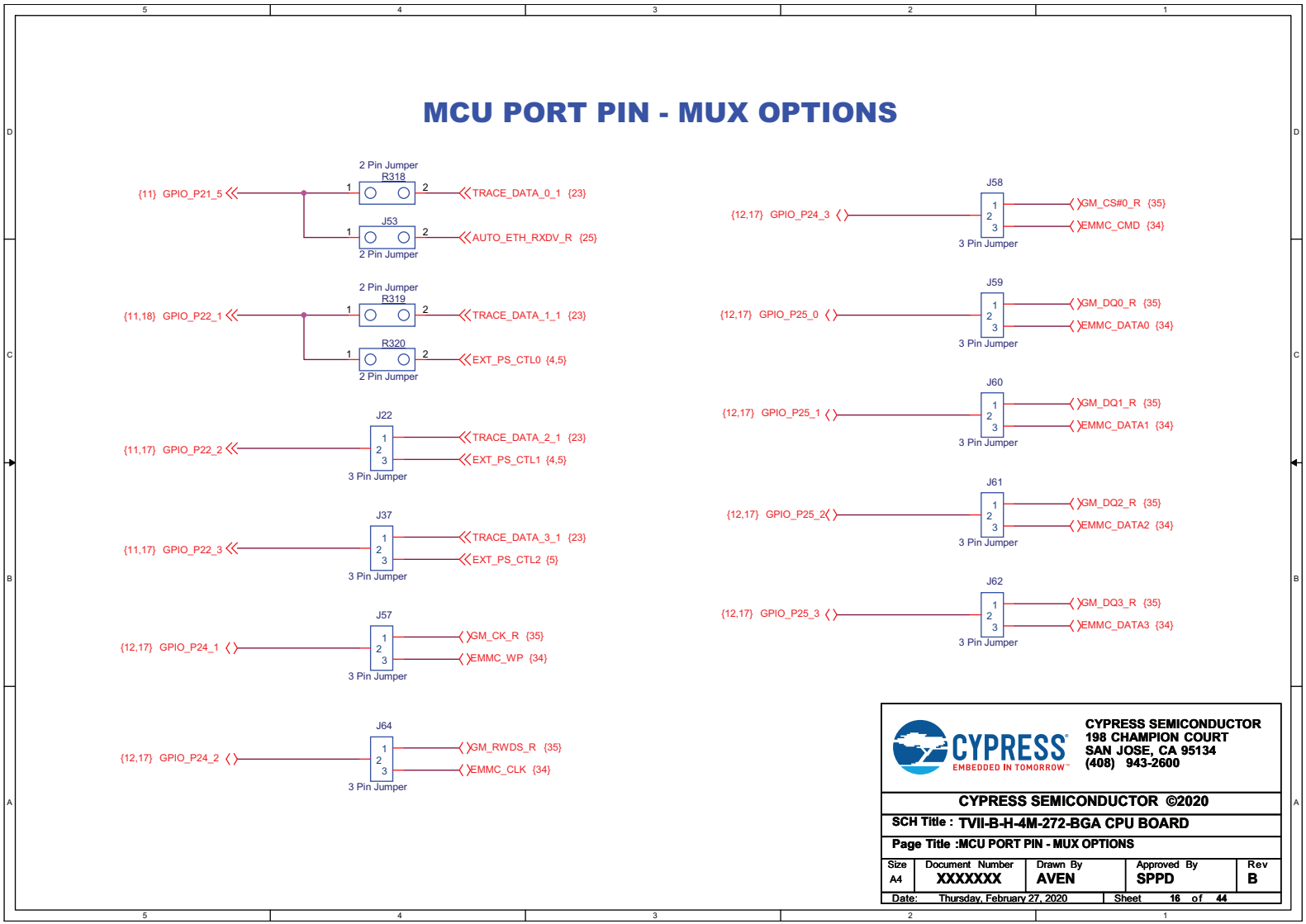


Figure A-16. Test Points-1

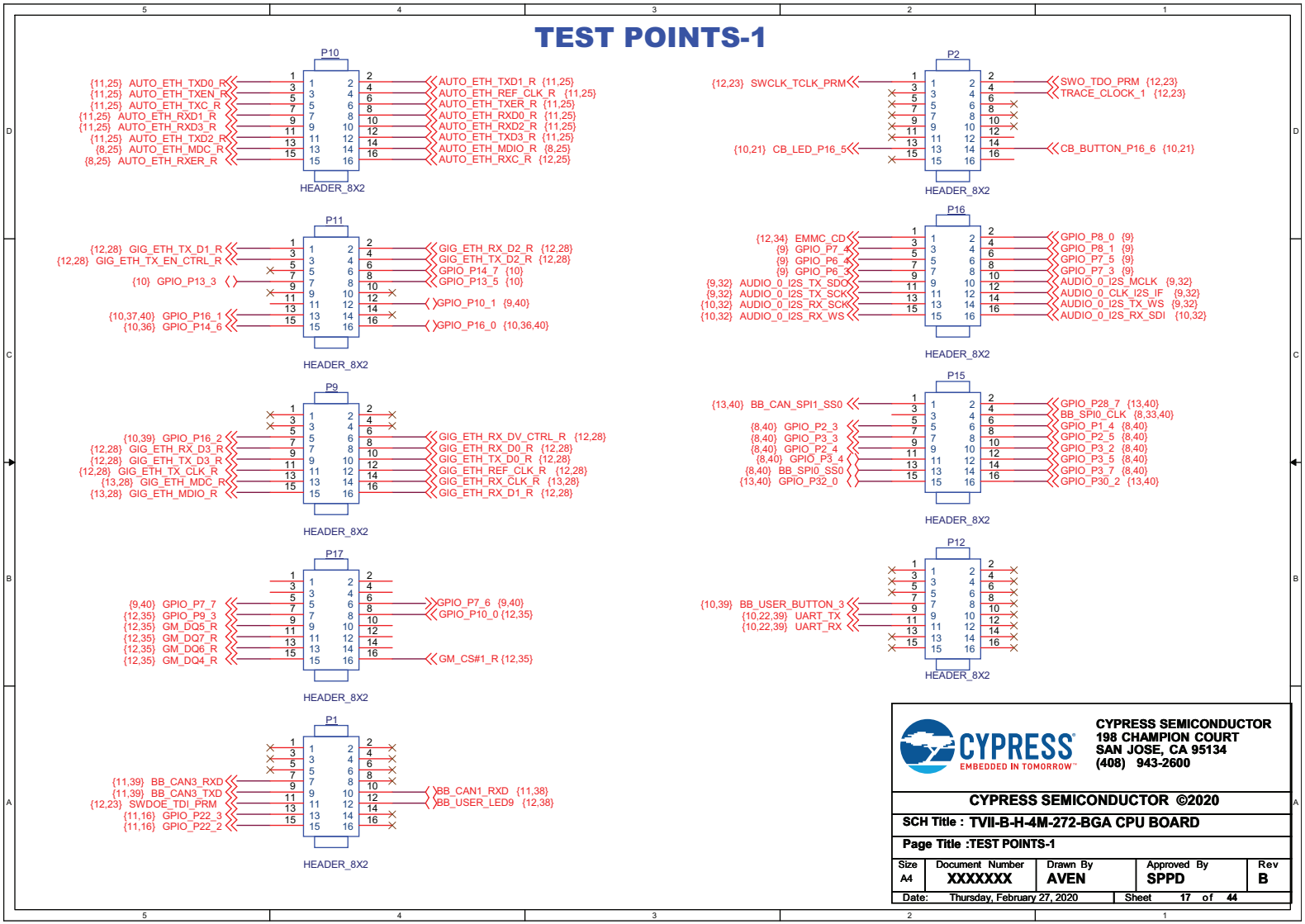


Figure A-17. Test Points-2

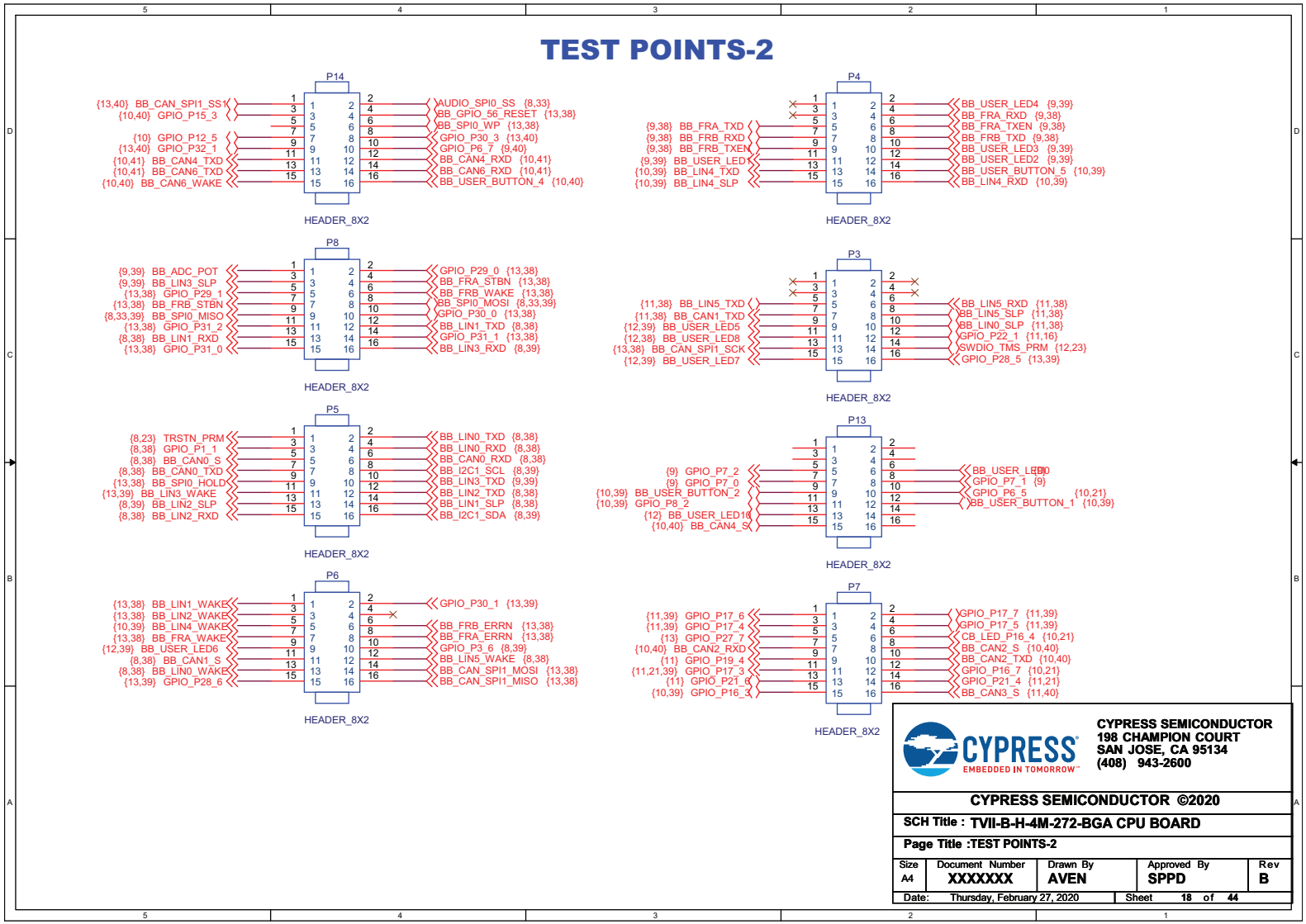


Figure A-18. Clock

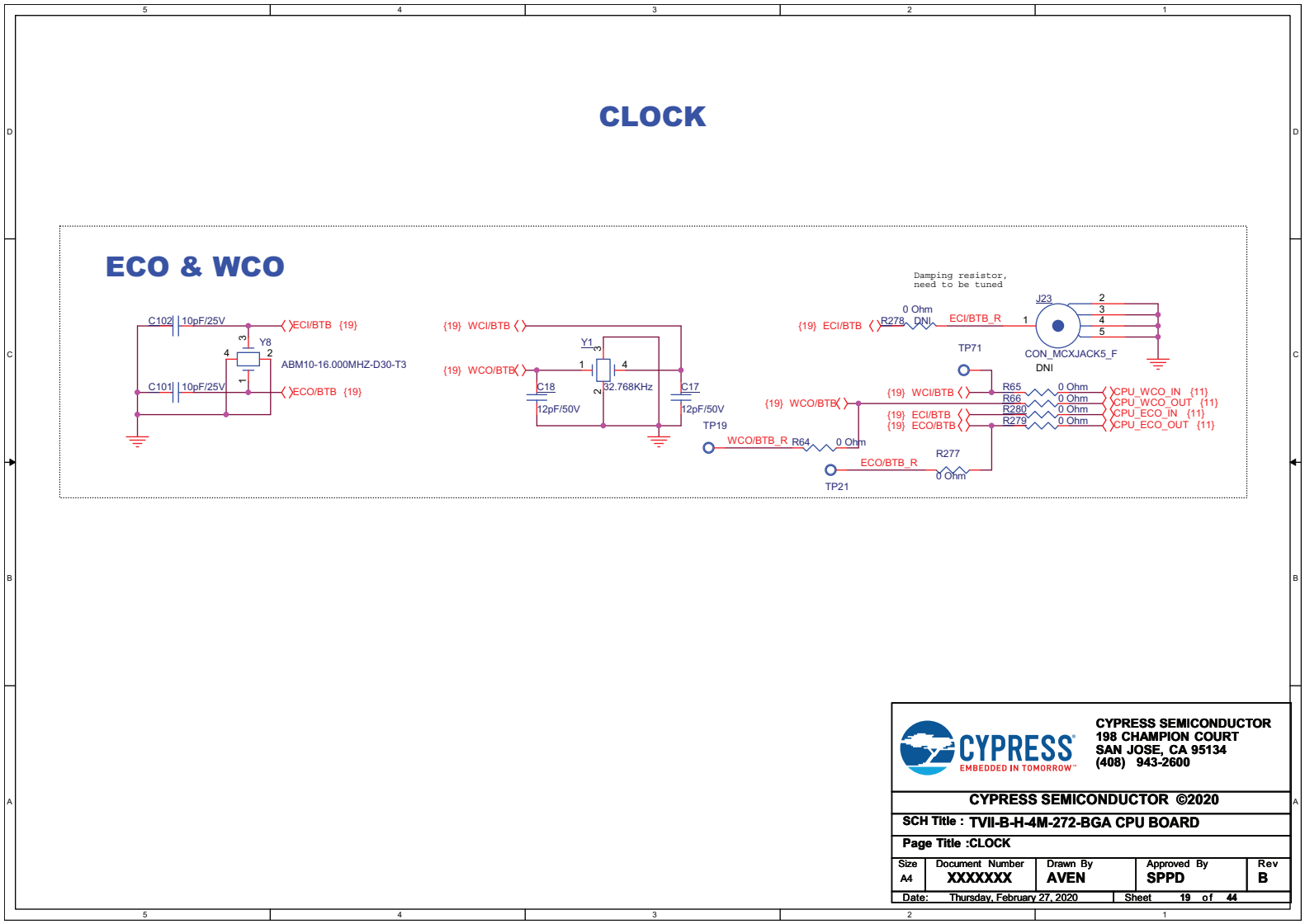


Figure A-19. Reset Controller

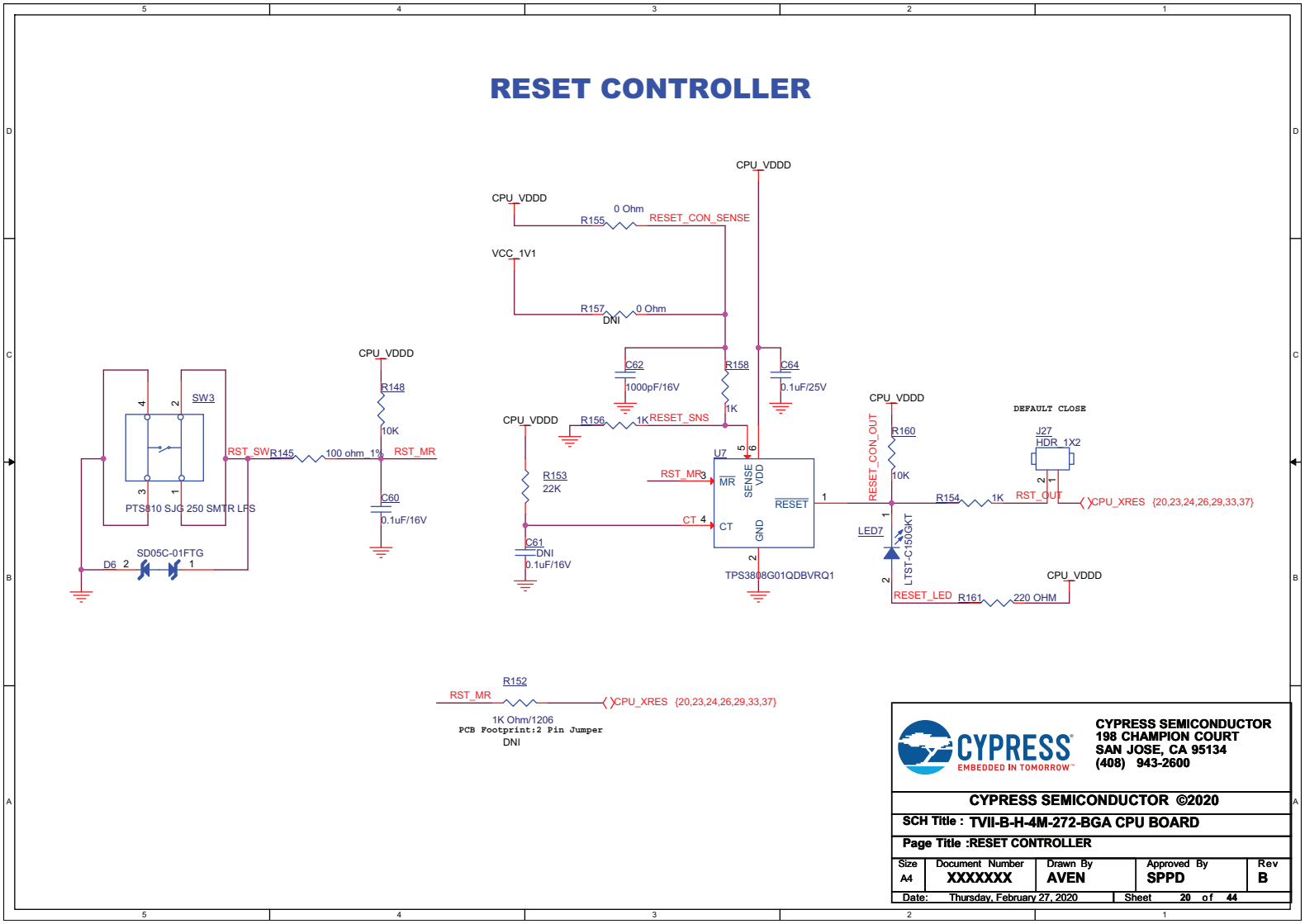


Figure A-20. GPIO - Button & Led

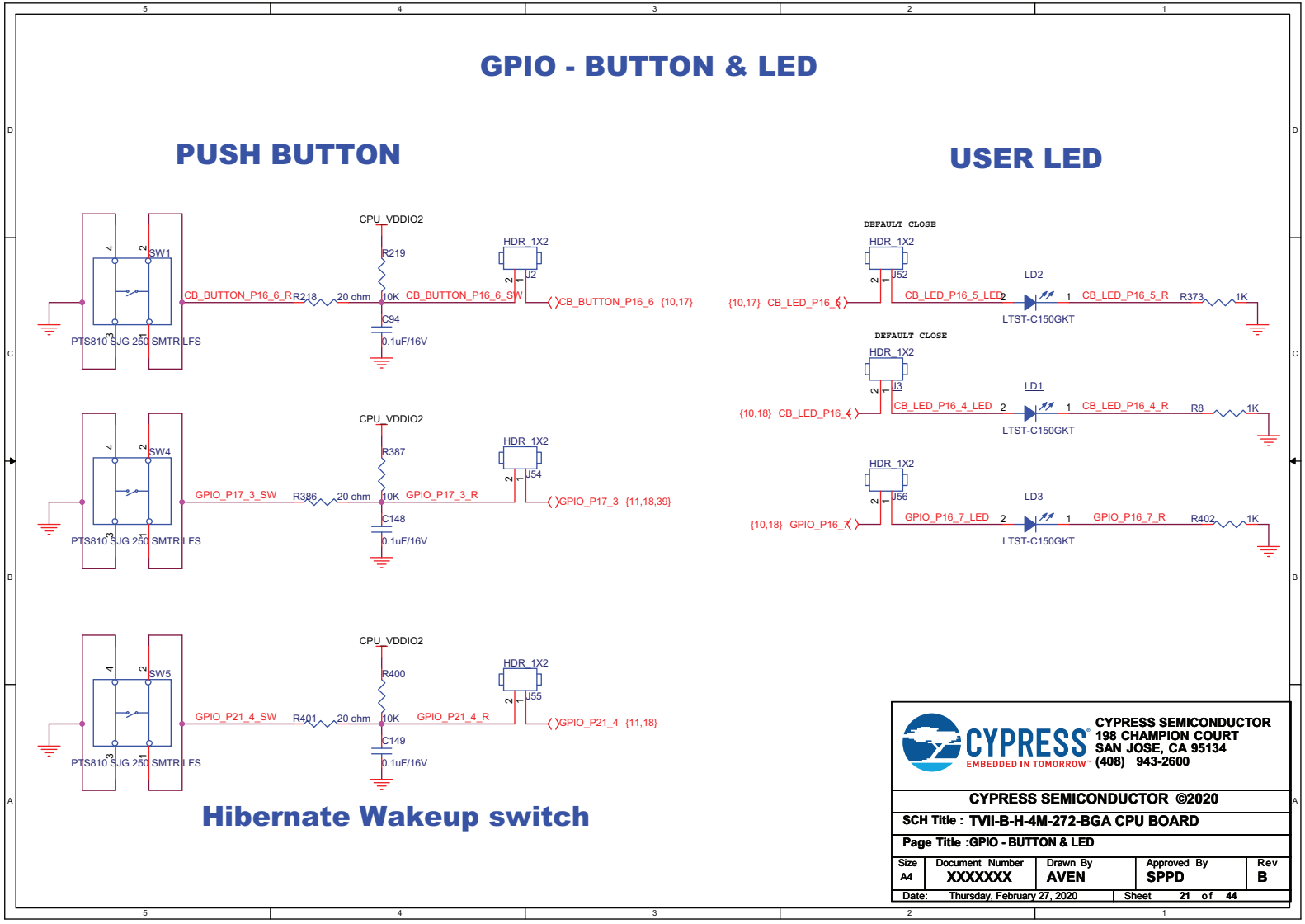


Figure A-21. UART - USB Transceiver

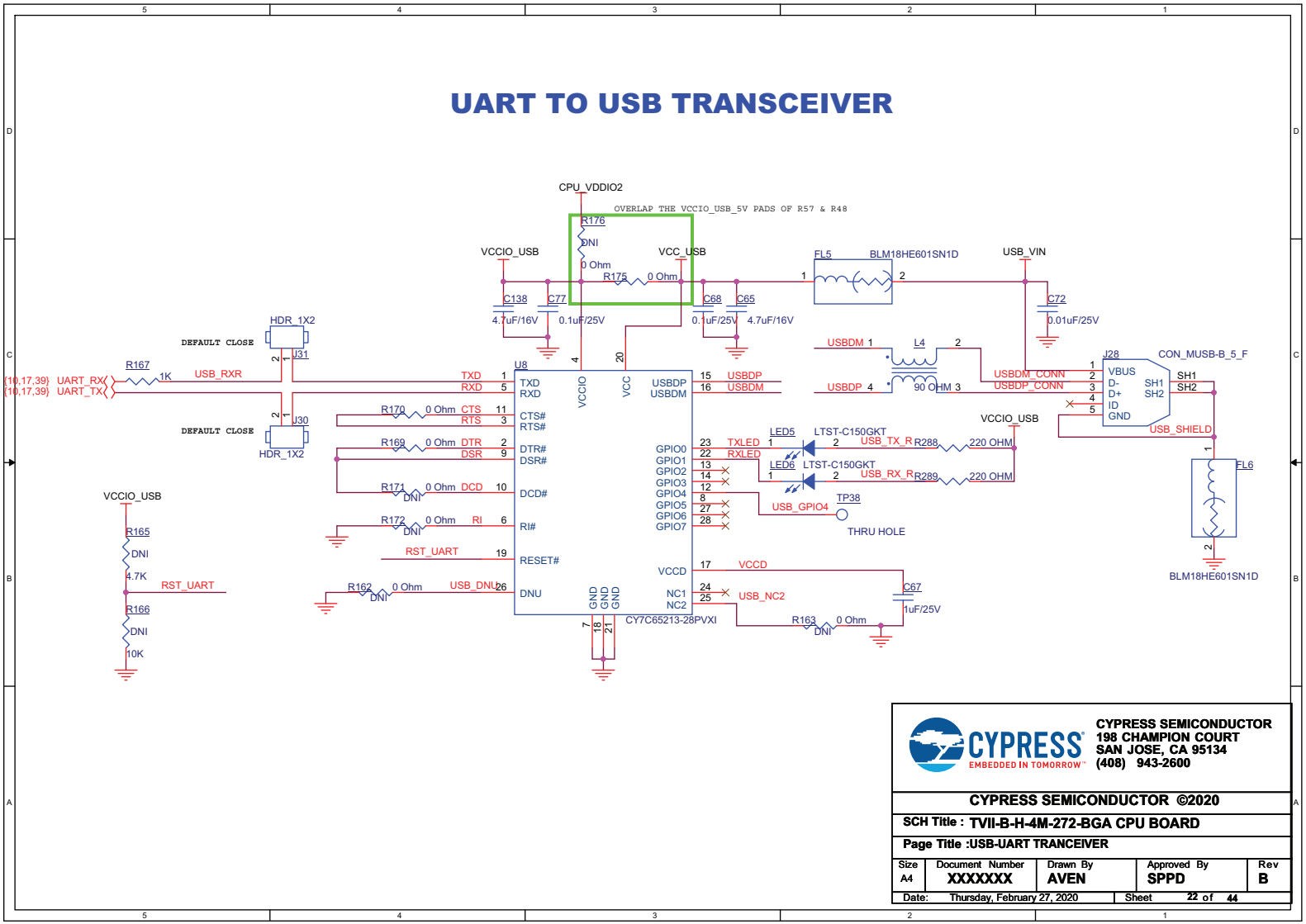


Figure A-22. Debug Interface-1

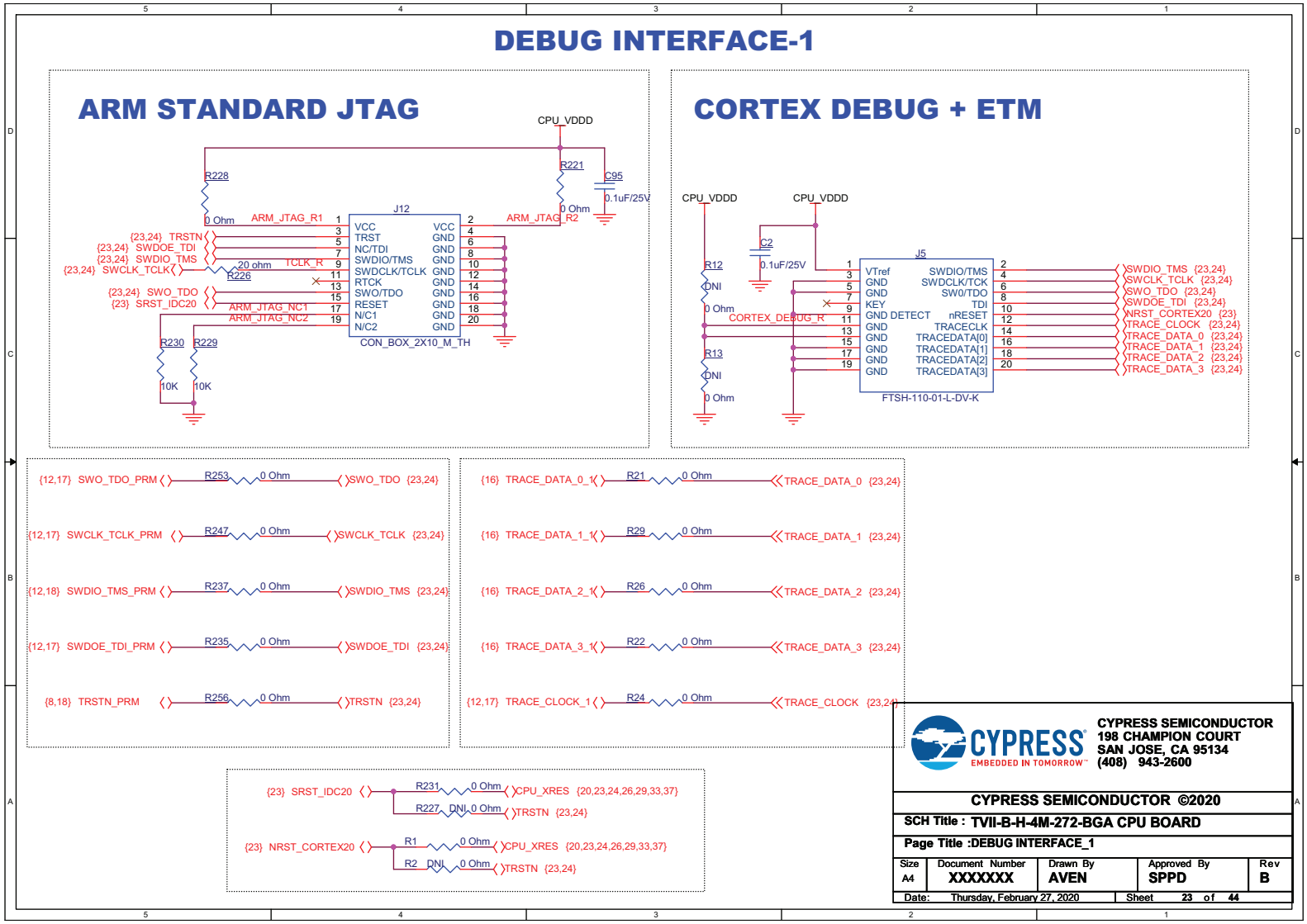


Figure A-23. Debug Interface-2

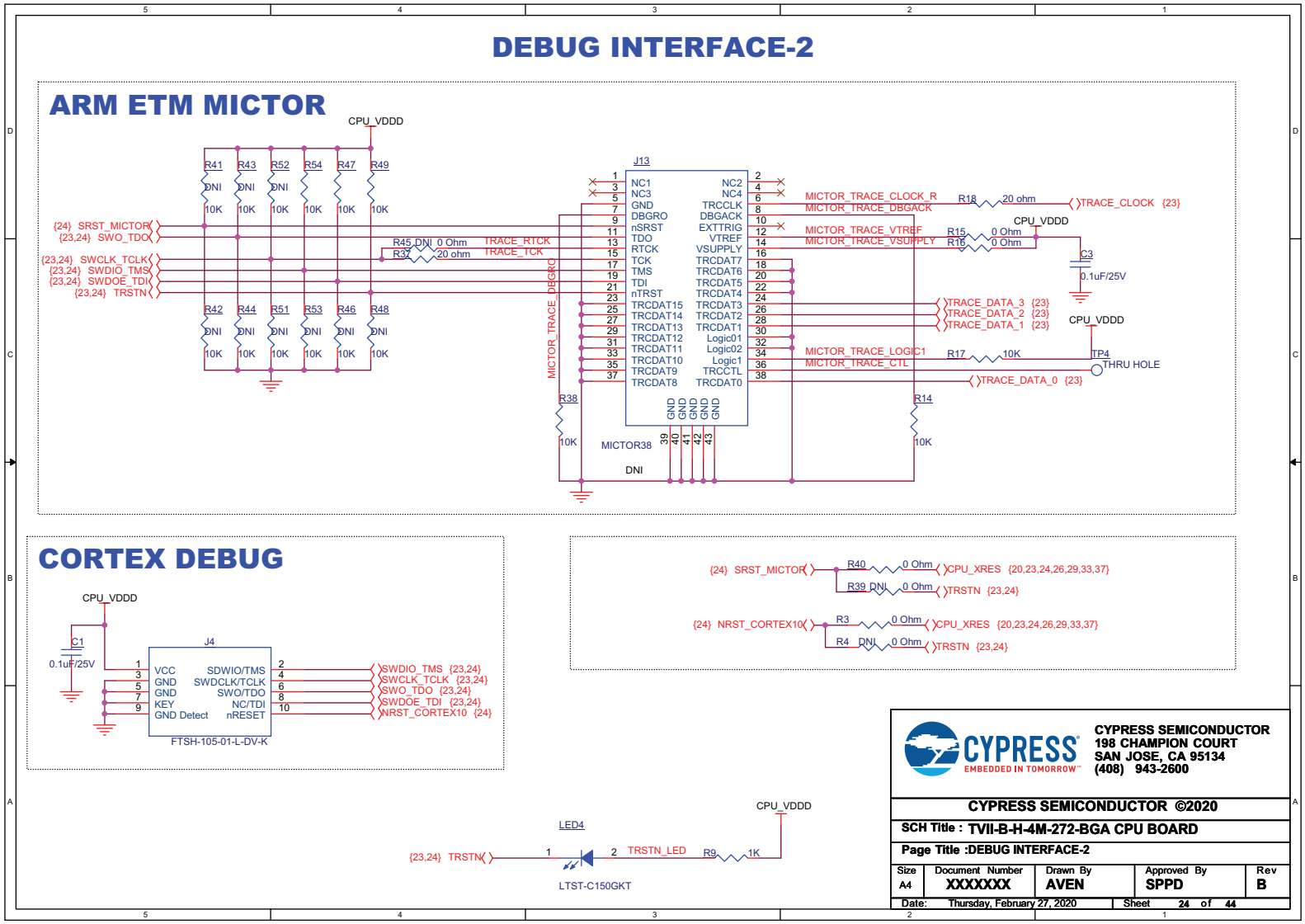


Figure A-24. Automotive Ethernet-1

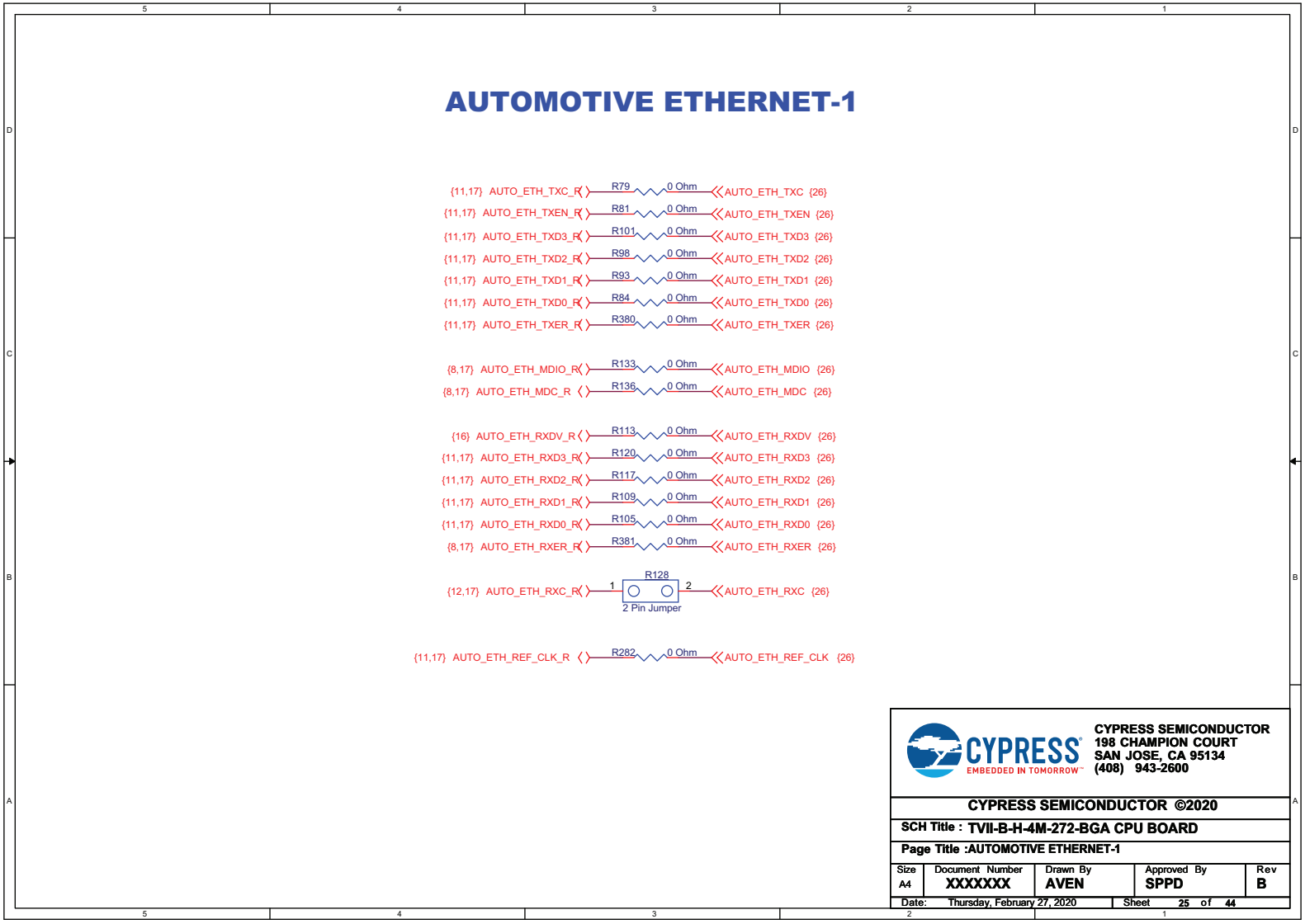


Figure A-25. Automotive Ethernet-2

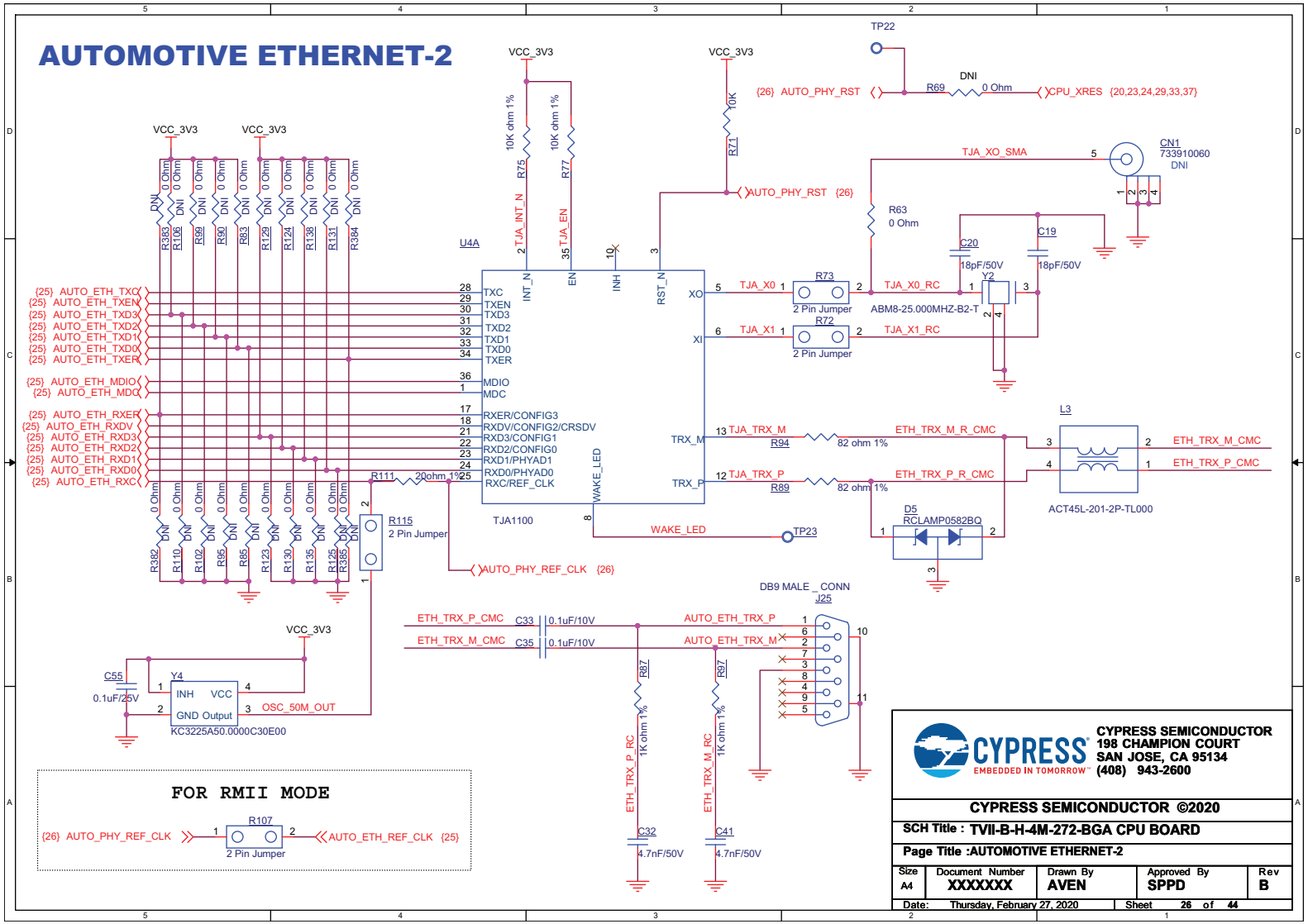


Figure A-26. Automotive Ethernet-3

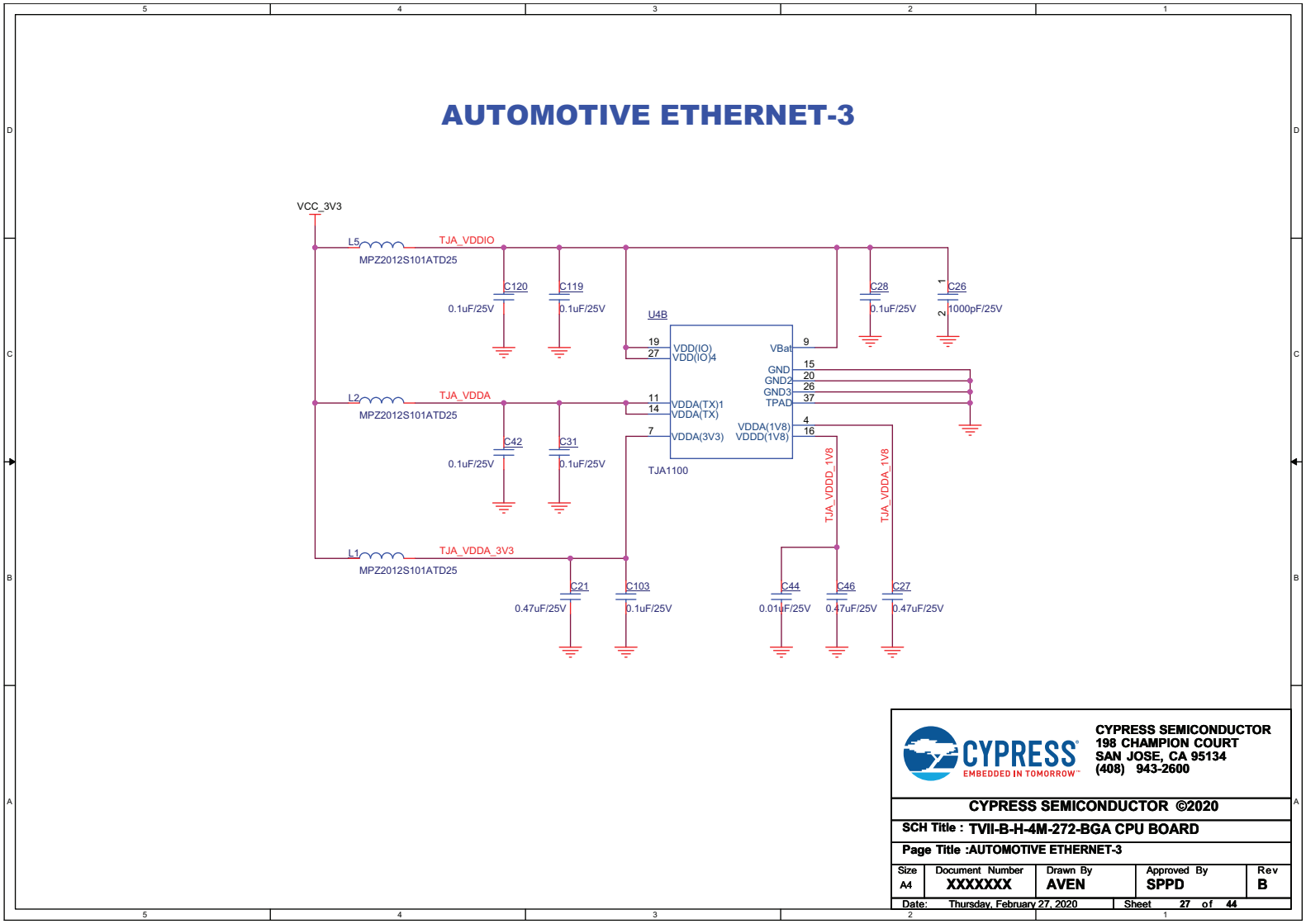


Figure A-27. Gigabit Ethernet-1

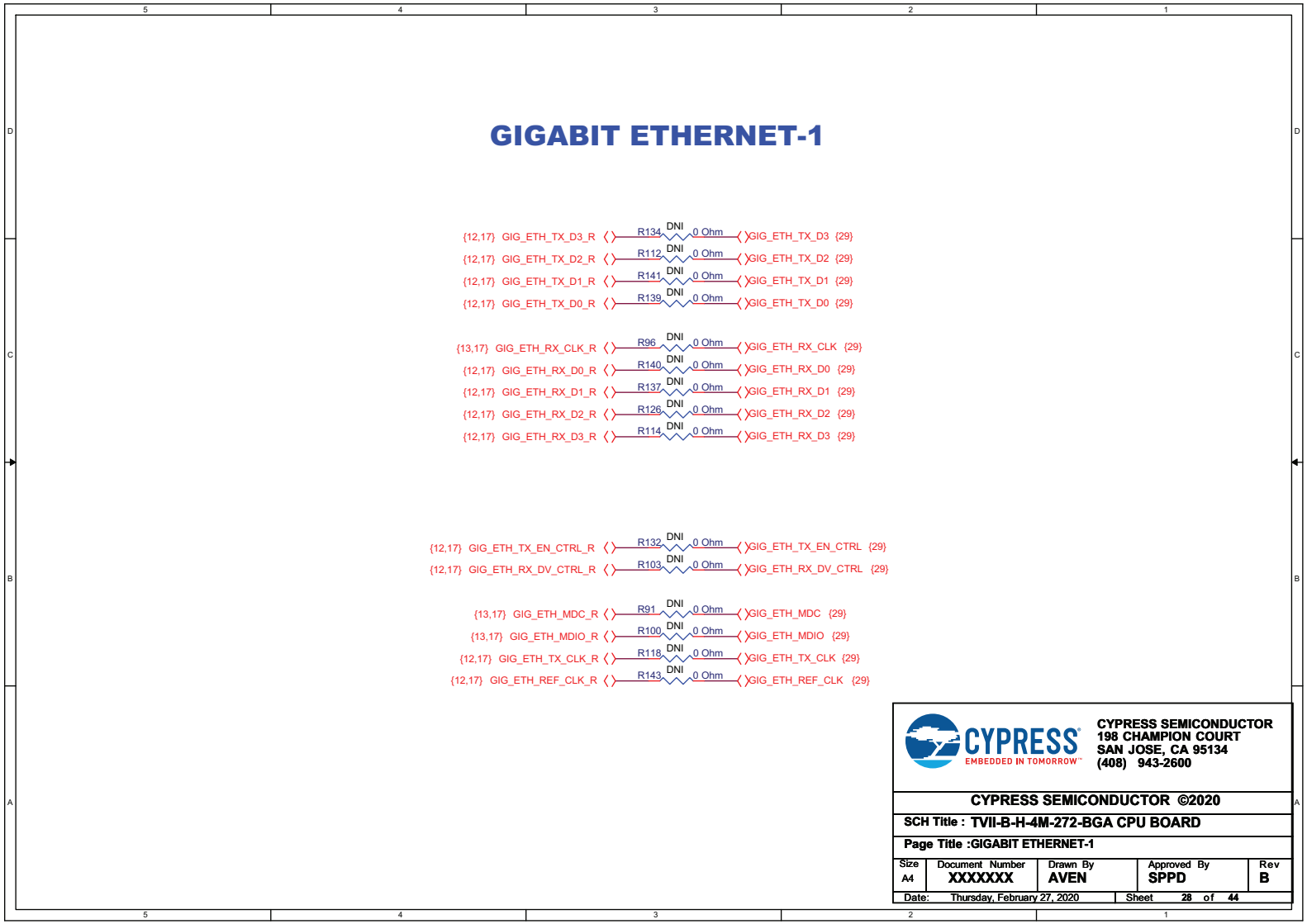


Figure A-28. Gigabit Ethernet-2

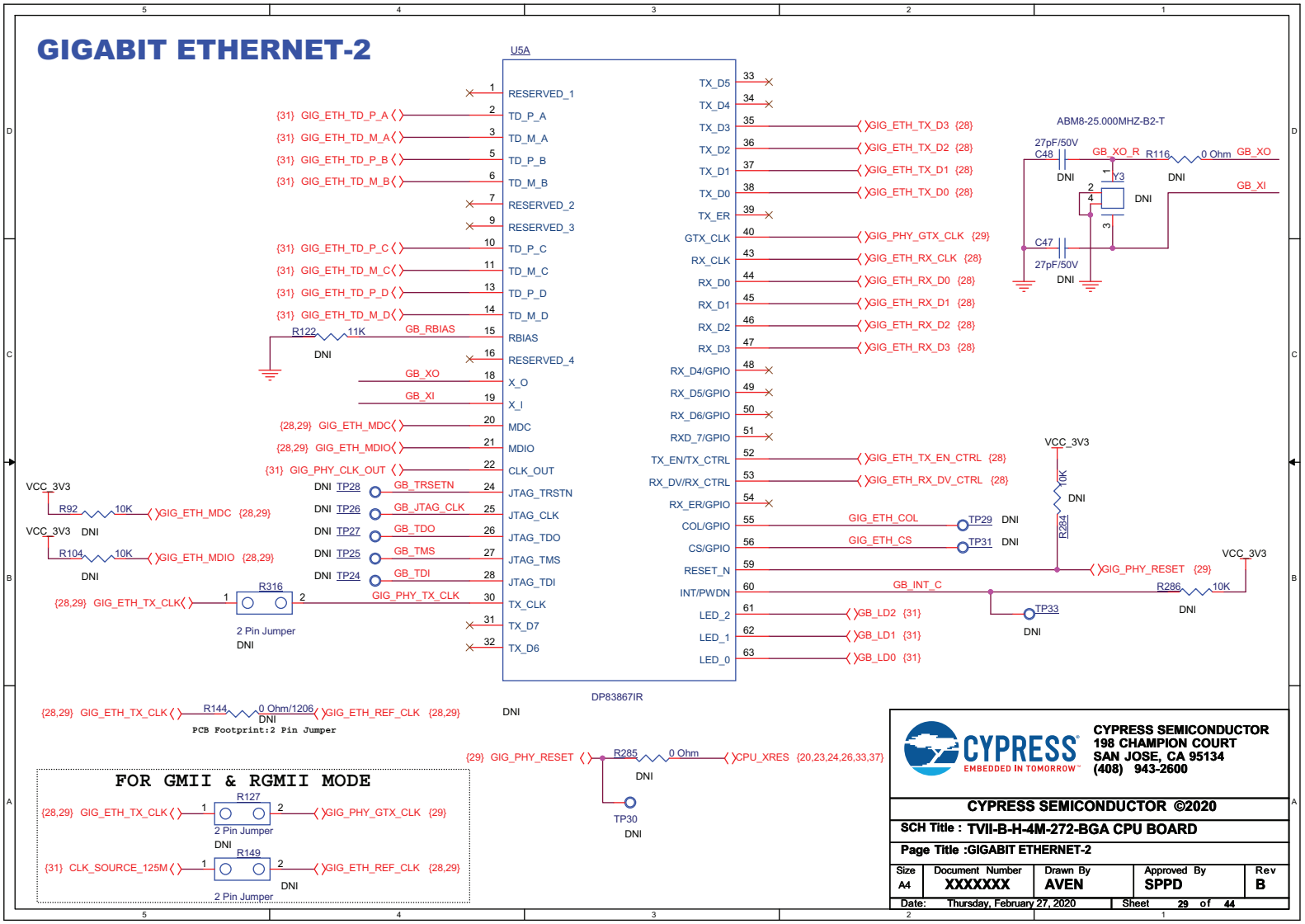


Figure A-29. Gigabit Ethernet-3

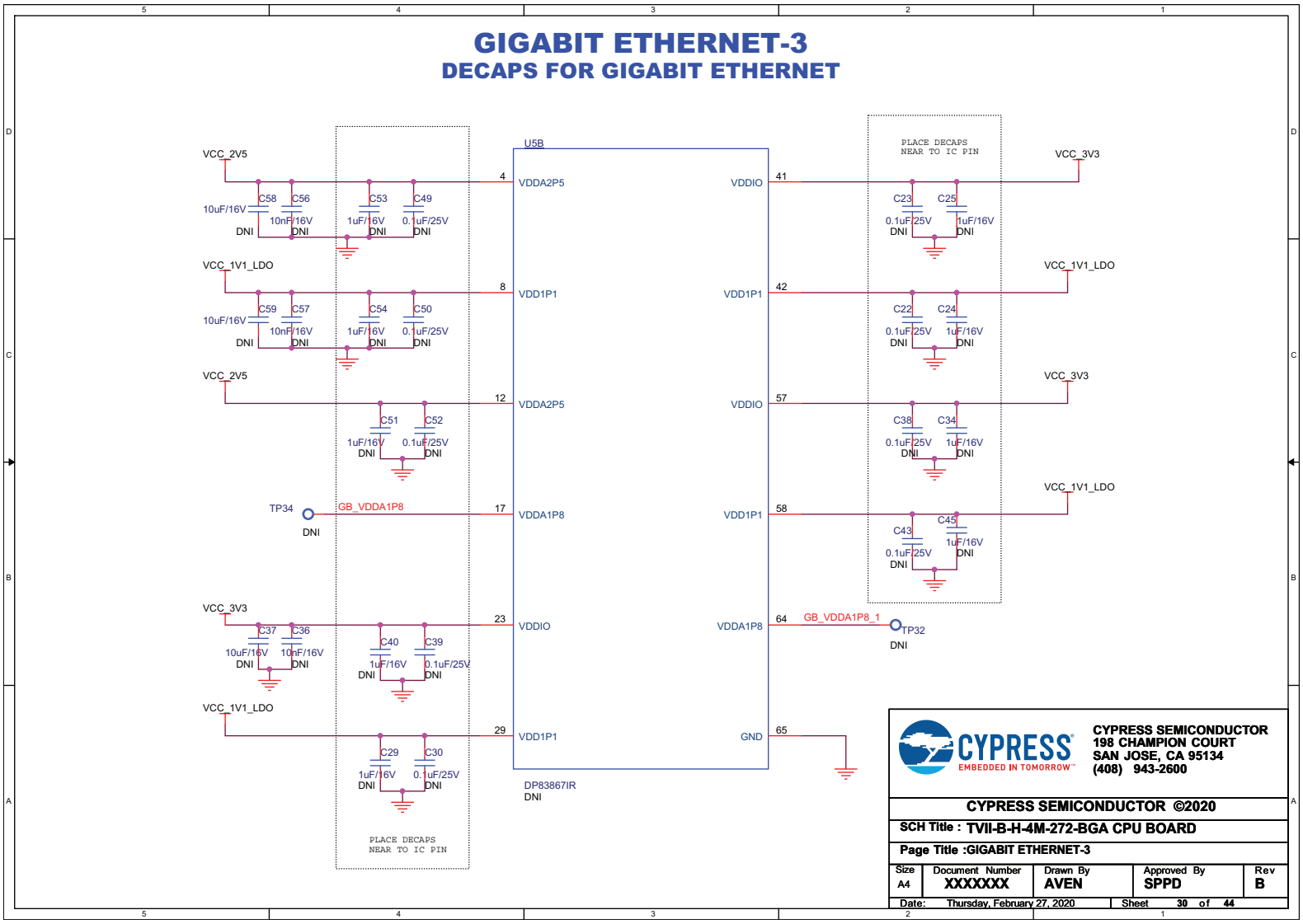


Figure A-30. Gigabit Ethernet-4

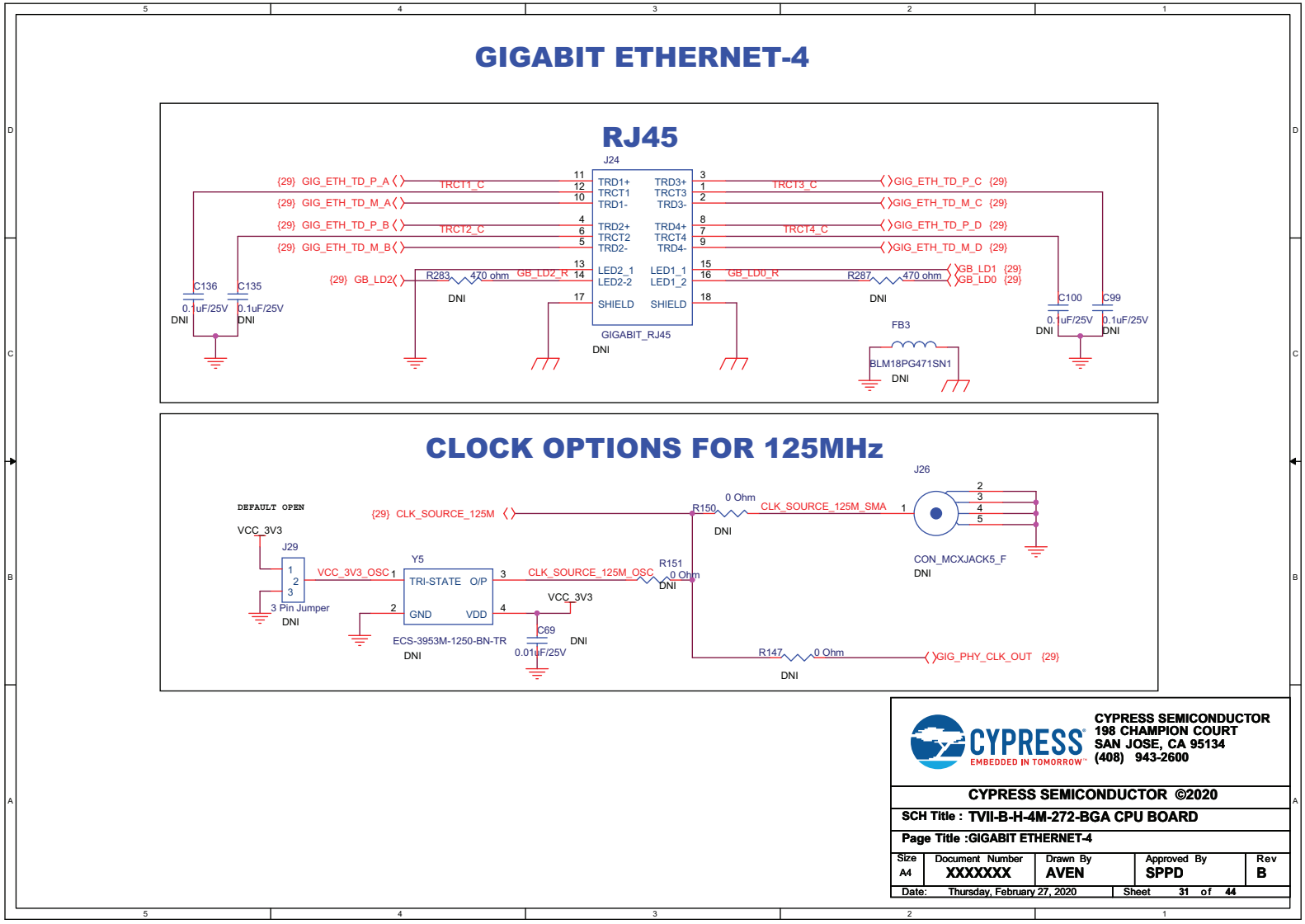


Figure A-31. Audio Interface-1

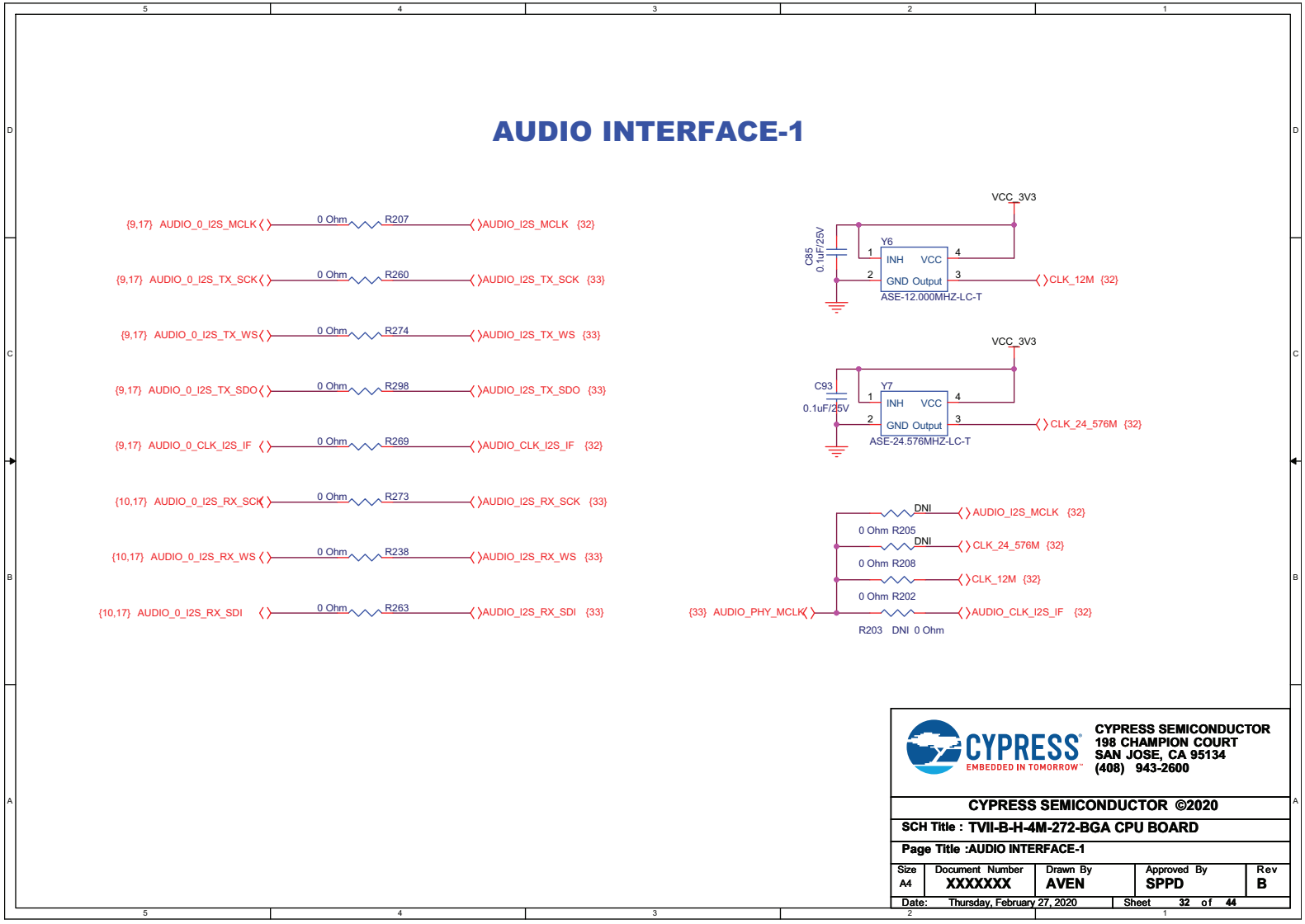


Figure A-32. Audio Interface-2

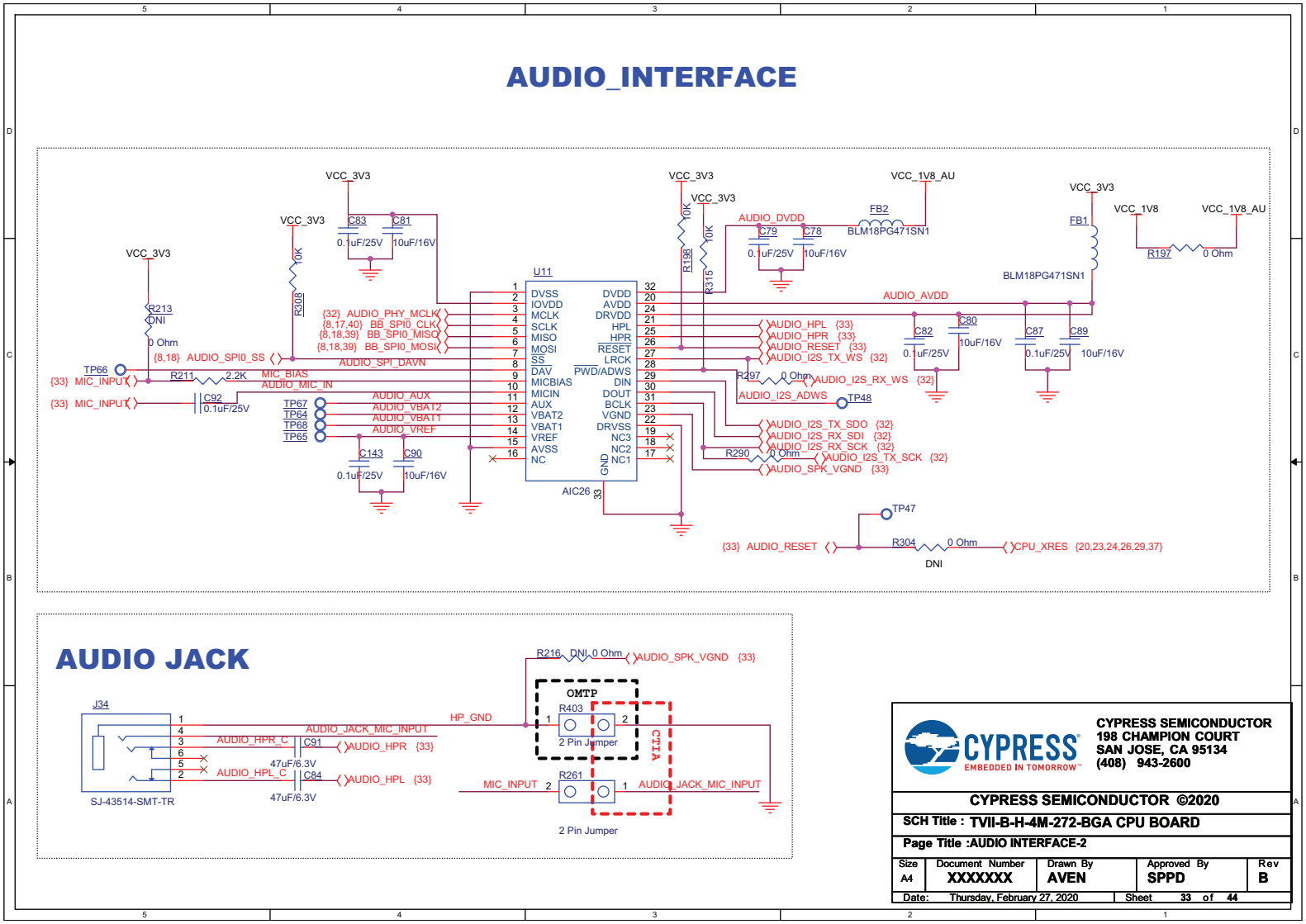


Figure A-33. eMMC Interface

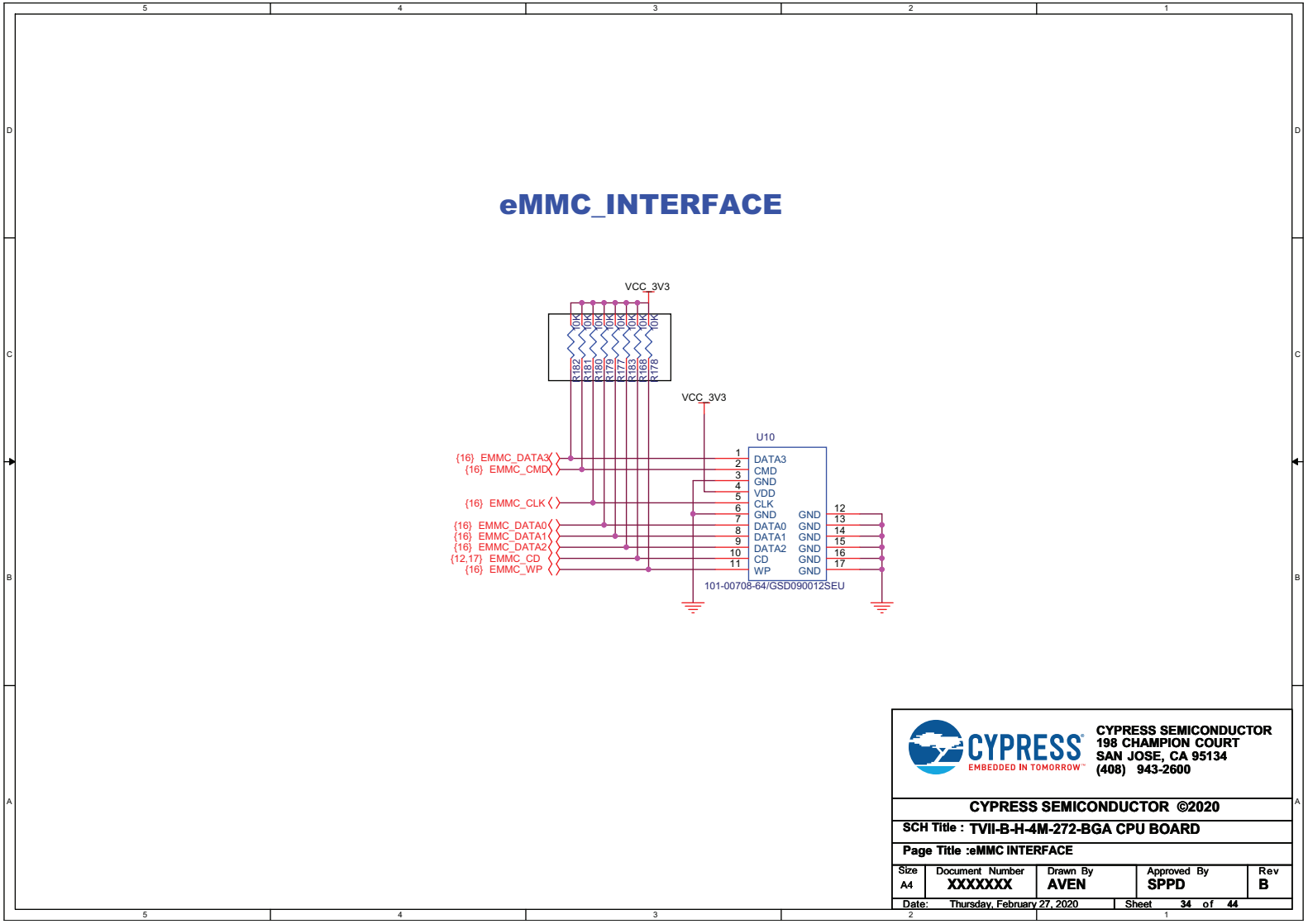


Figure A-34. SMIF HS Connector

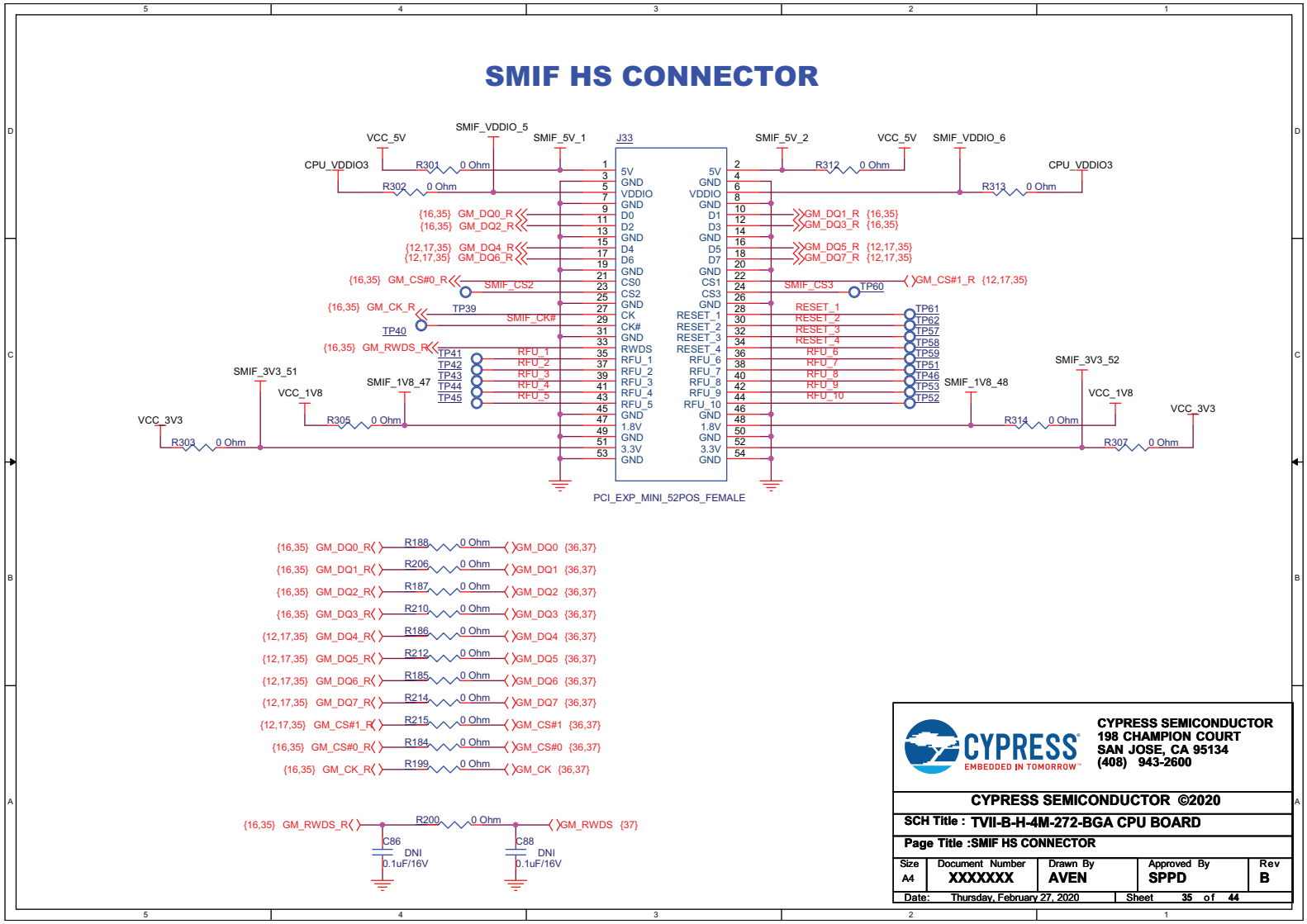


Figure A-35. Dual Quad-SPI

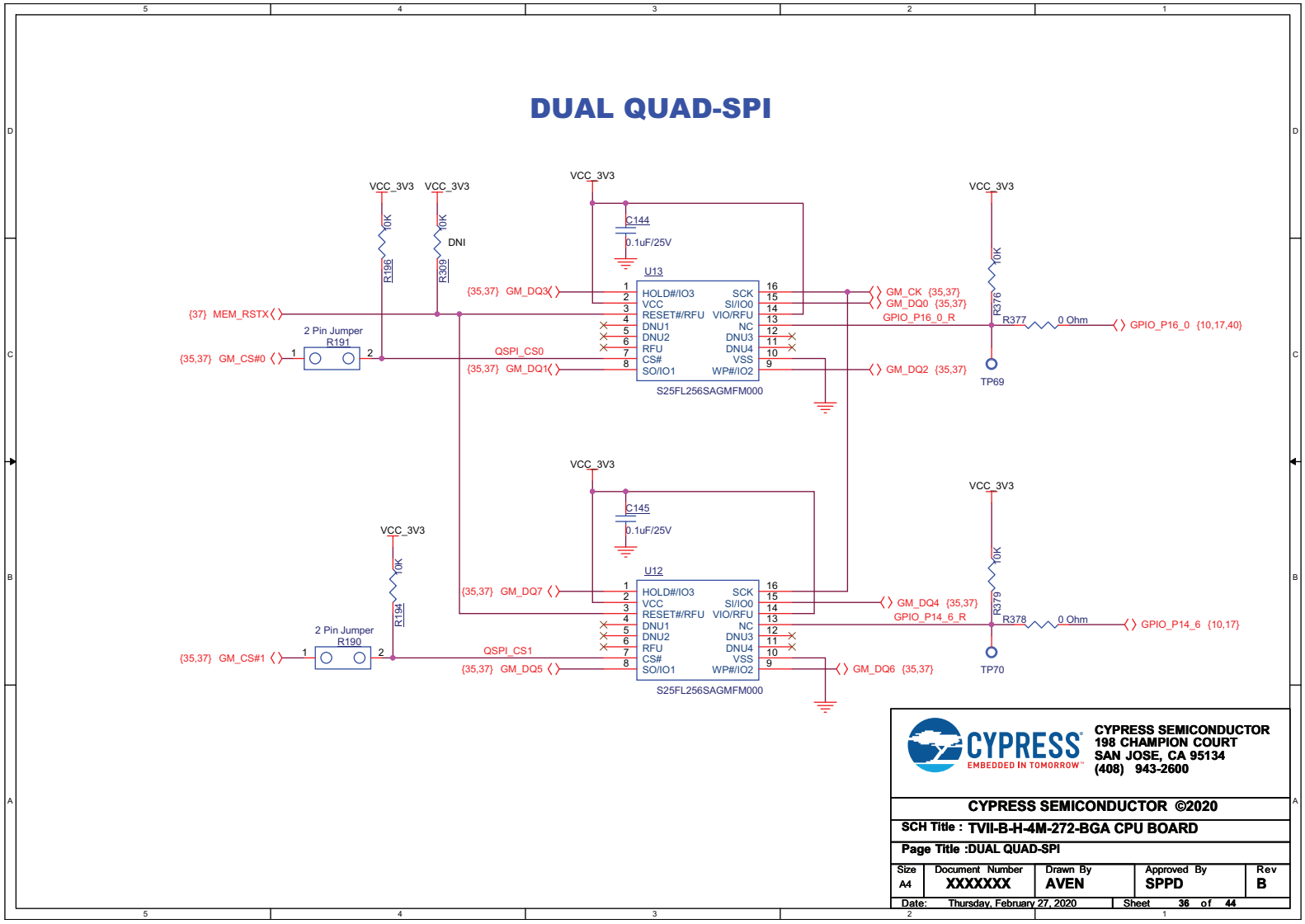


Figure A-36. H-Flash & H-SRAM

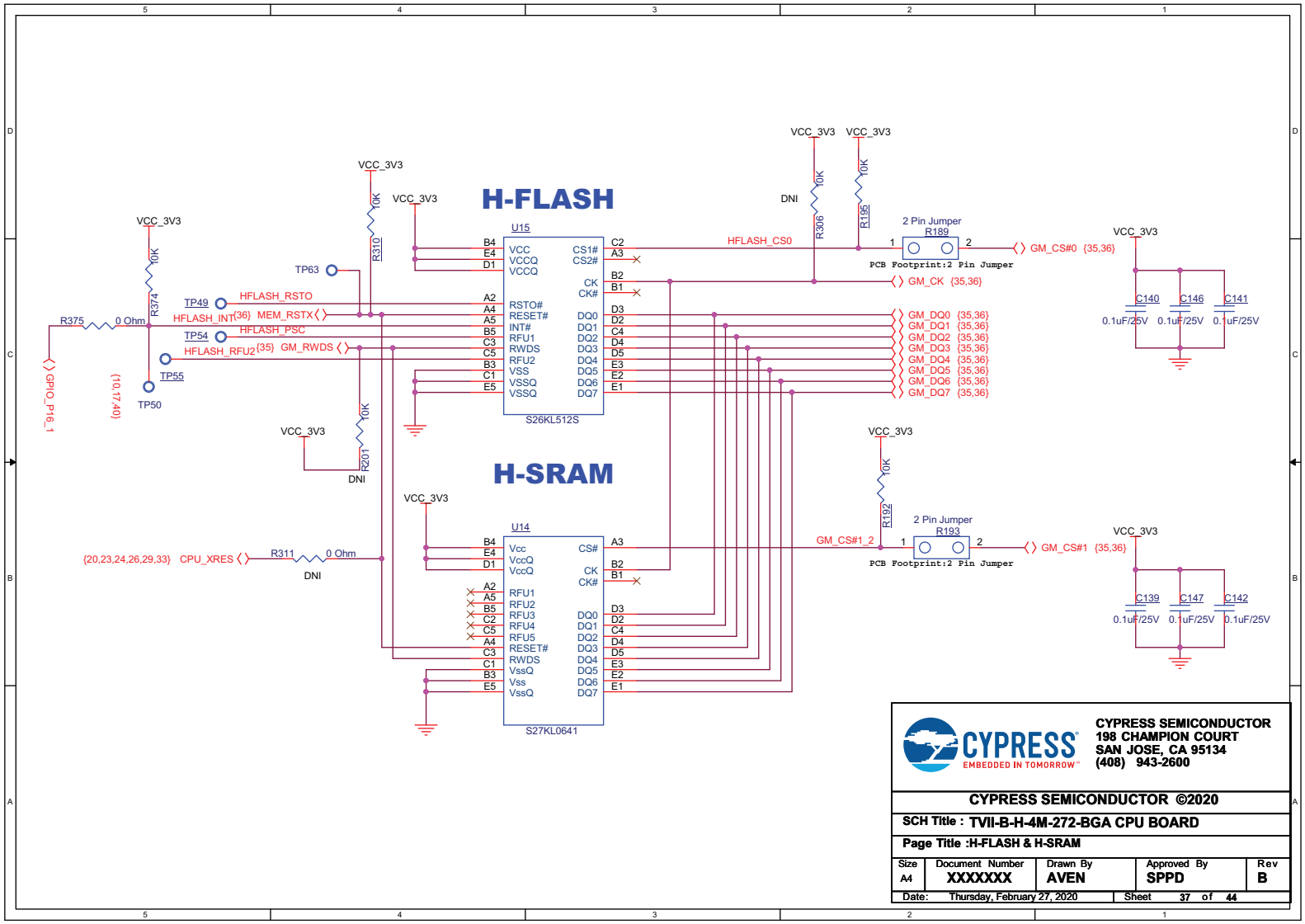


Figure A-37. Base Board Connector - J35A

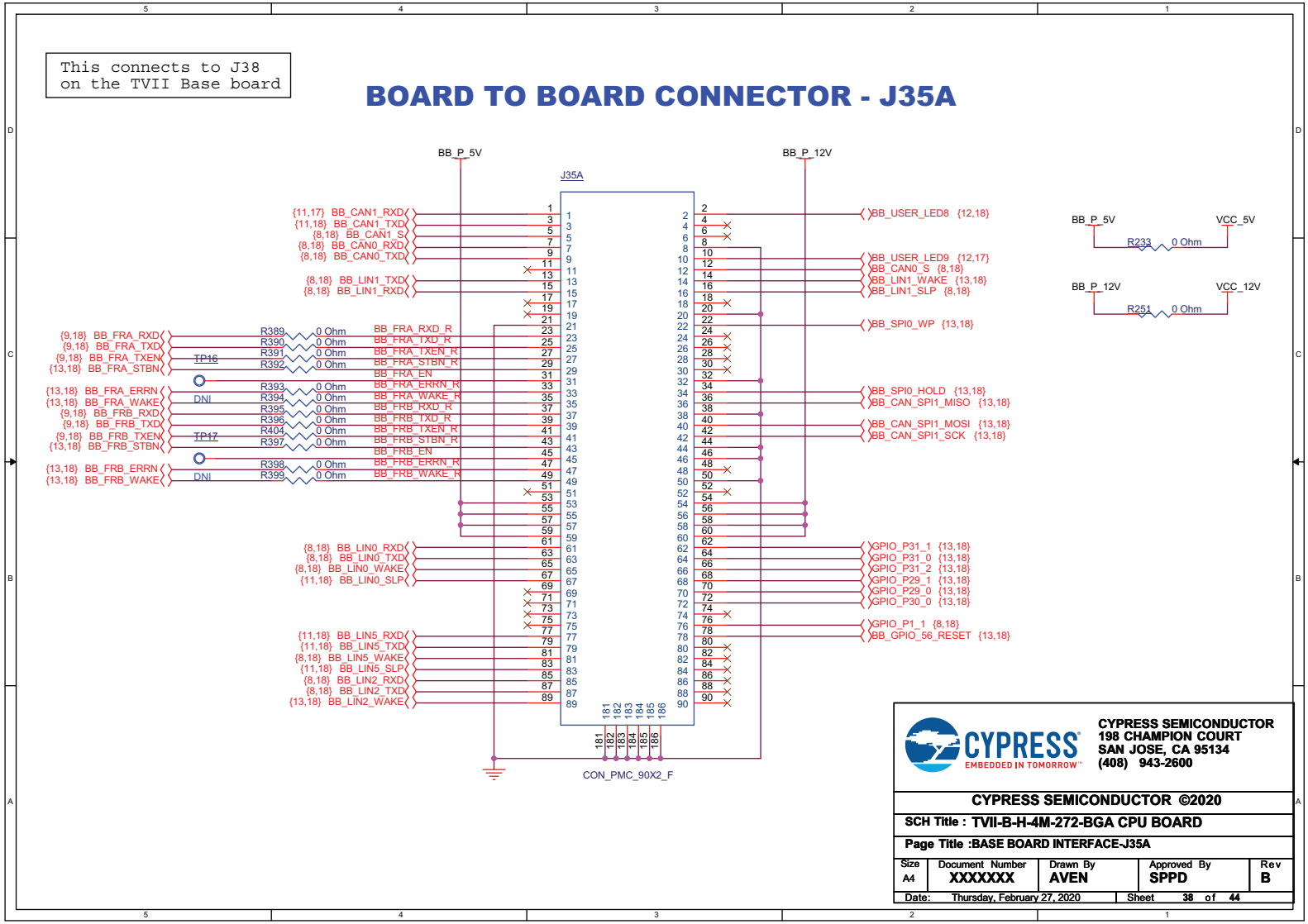


Figure A-38. Base Board Connector - J35B

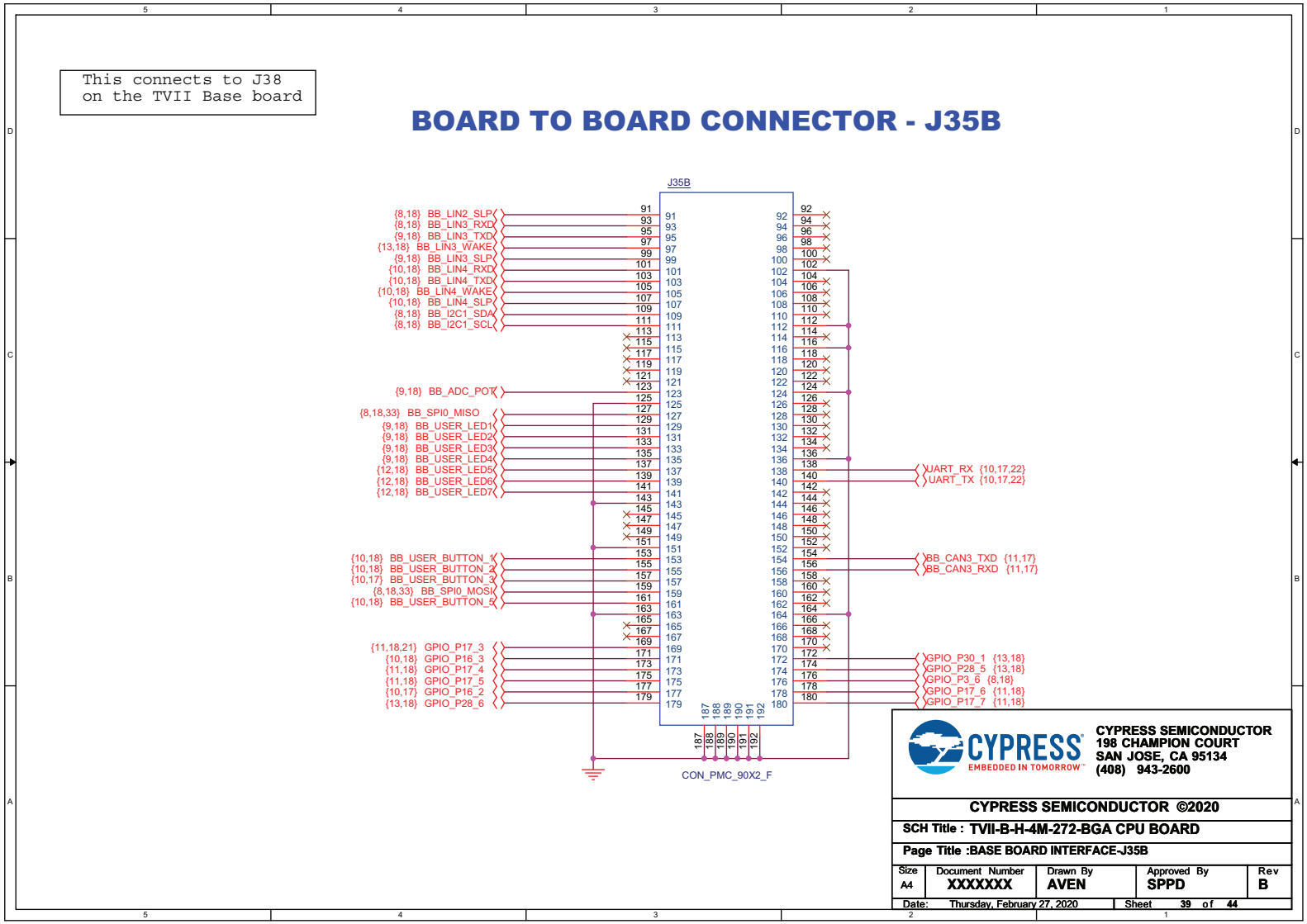


Figure A-39. Base Board Connector - J36A

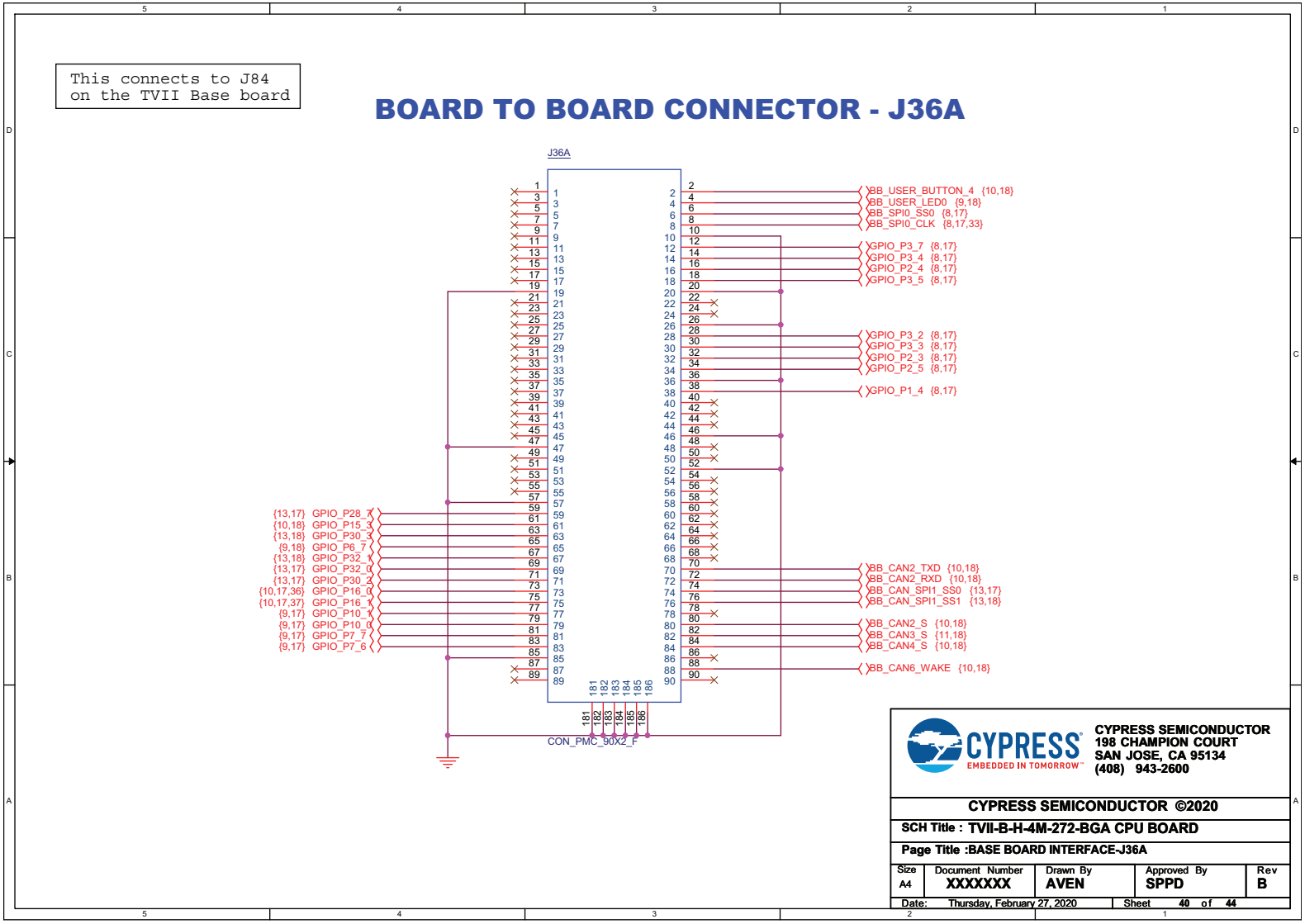
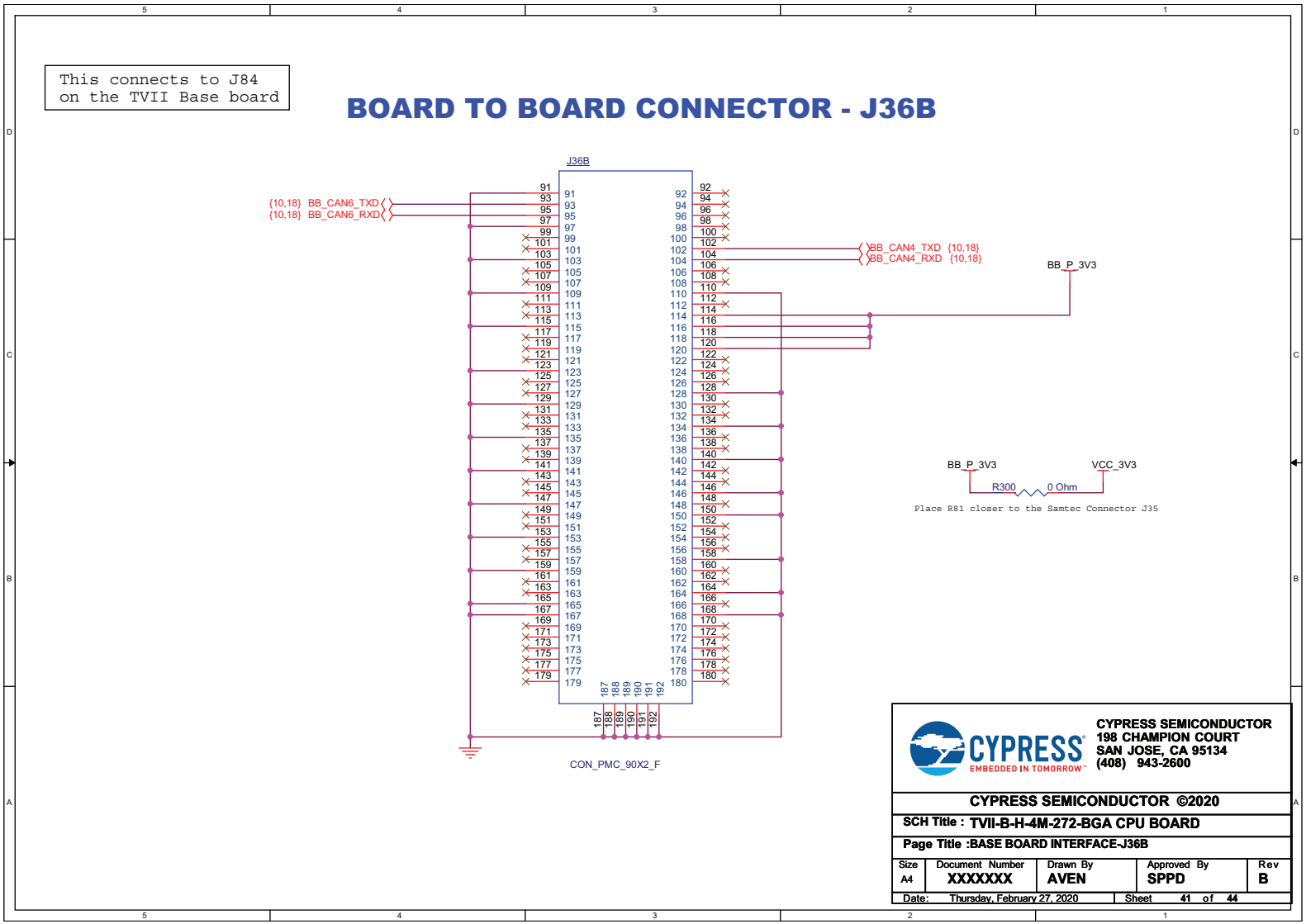


Figure A-40. Base Board Connector - J36B



B. Component Assembly on CPU Board

This appendix shows the top and bottom assembly of the CYTVII-B-H-4M-272-CPU board.

Figure B-1. Component Assembly (Top)

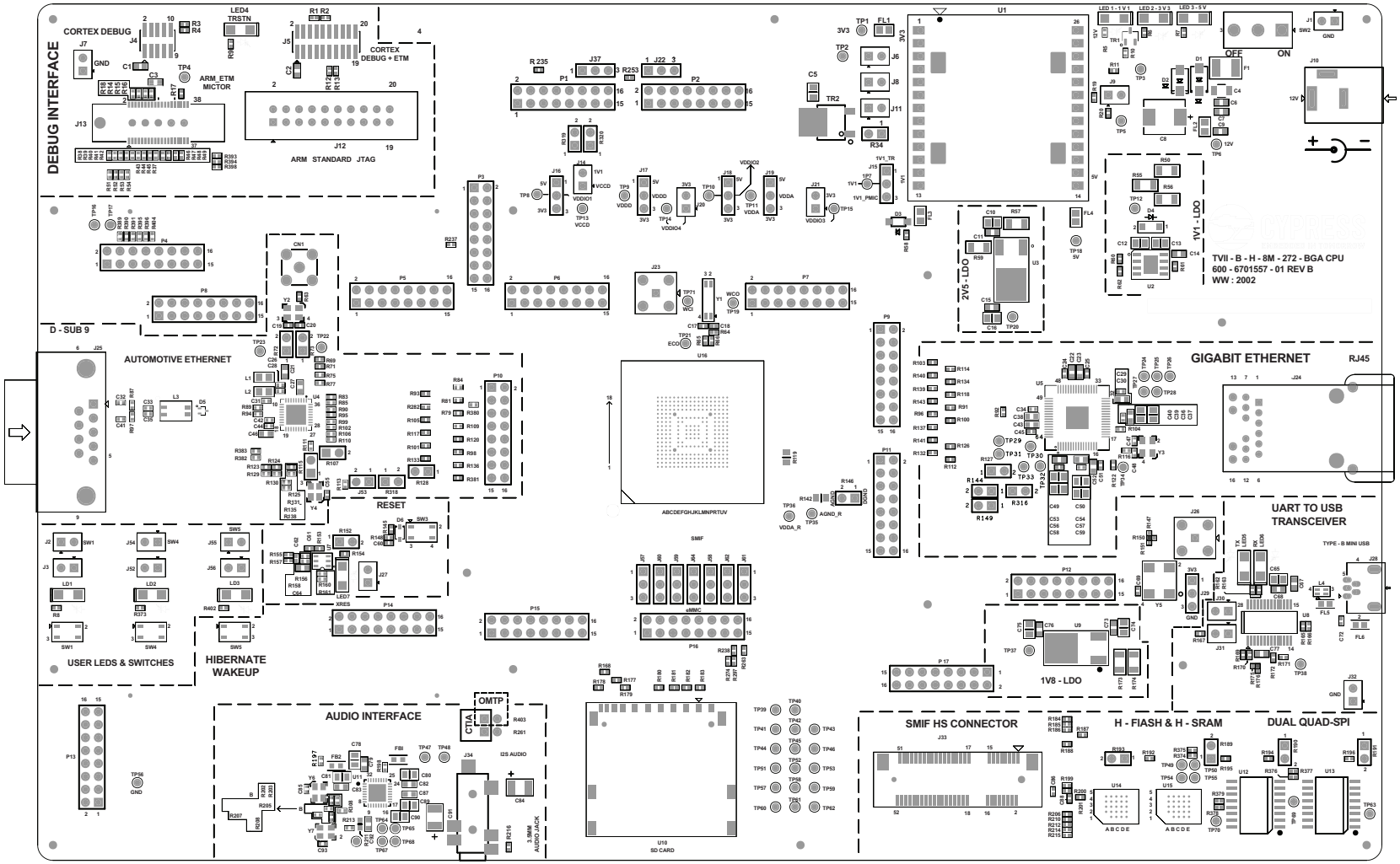
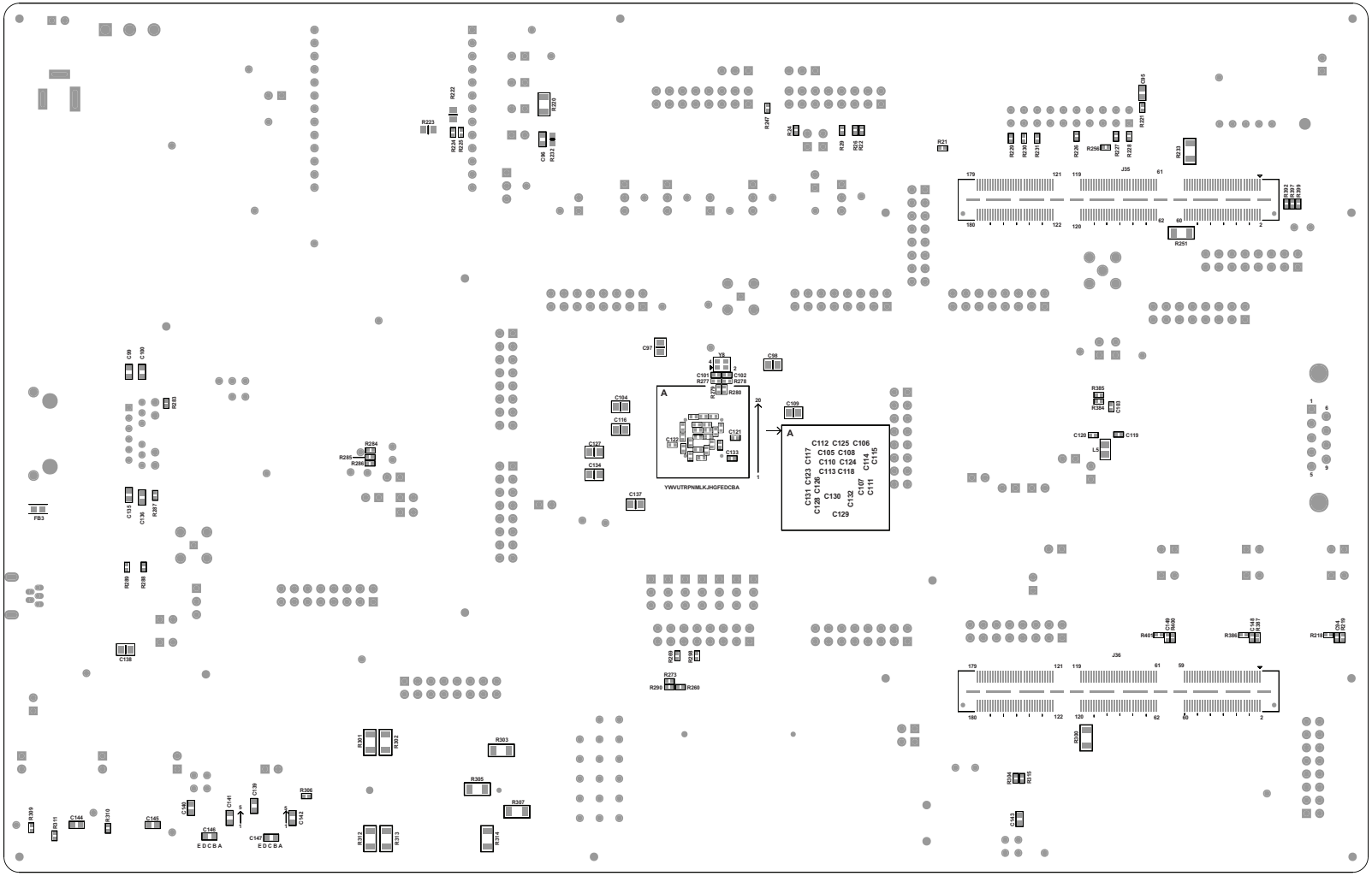


Figure B-2. Component Assembly (Bottom)



C. Schematics of Base Board

This appendix contains the schematics of Traveo II Base board (CYTVII-B-E-BB).

Figure C-1. Block Diagram

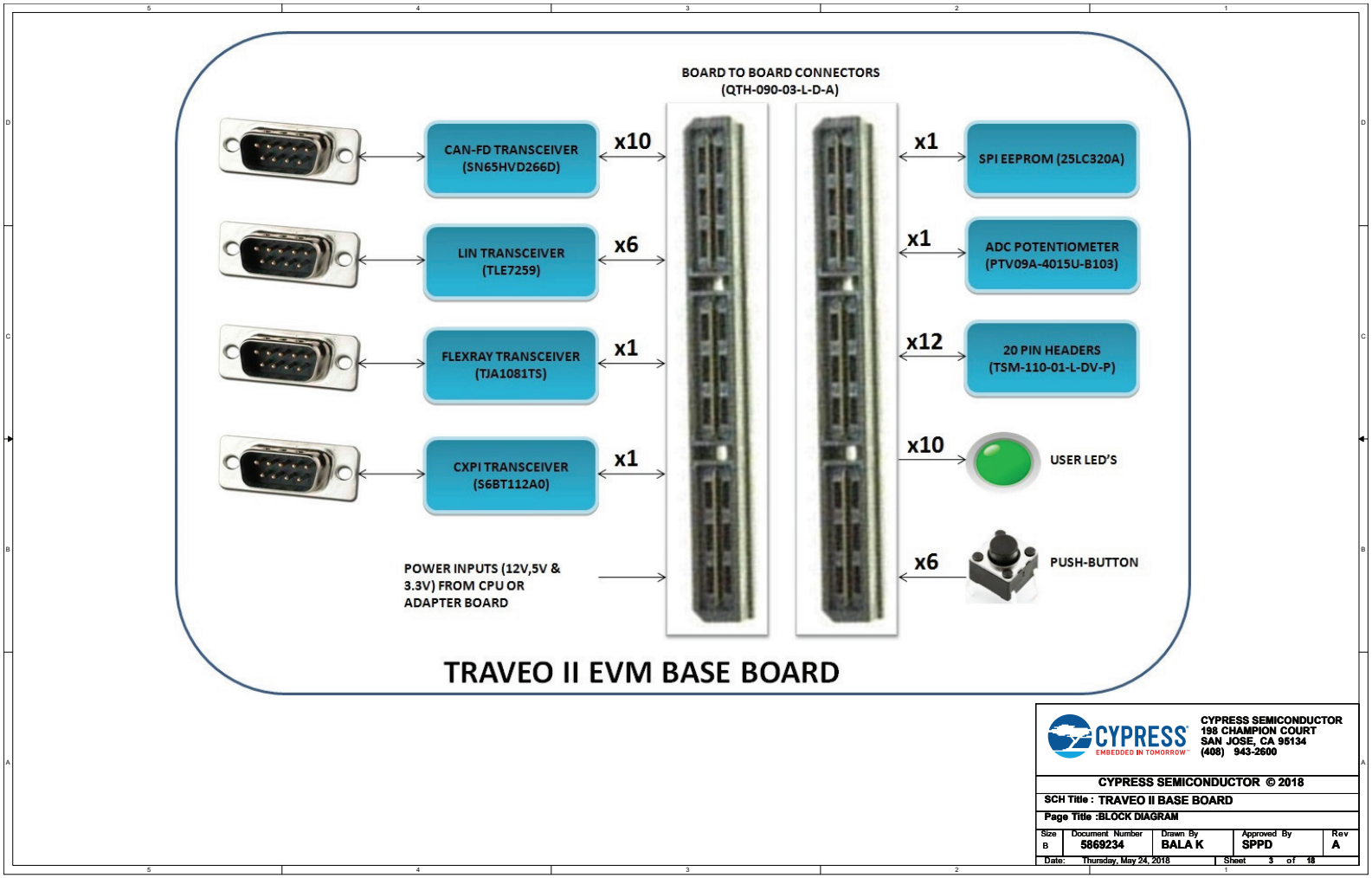


Figure C-2. BTOB Connector-01

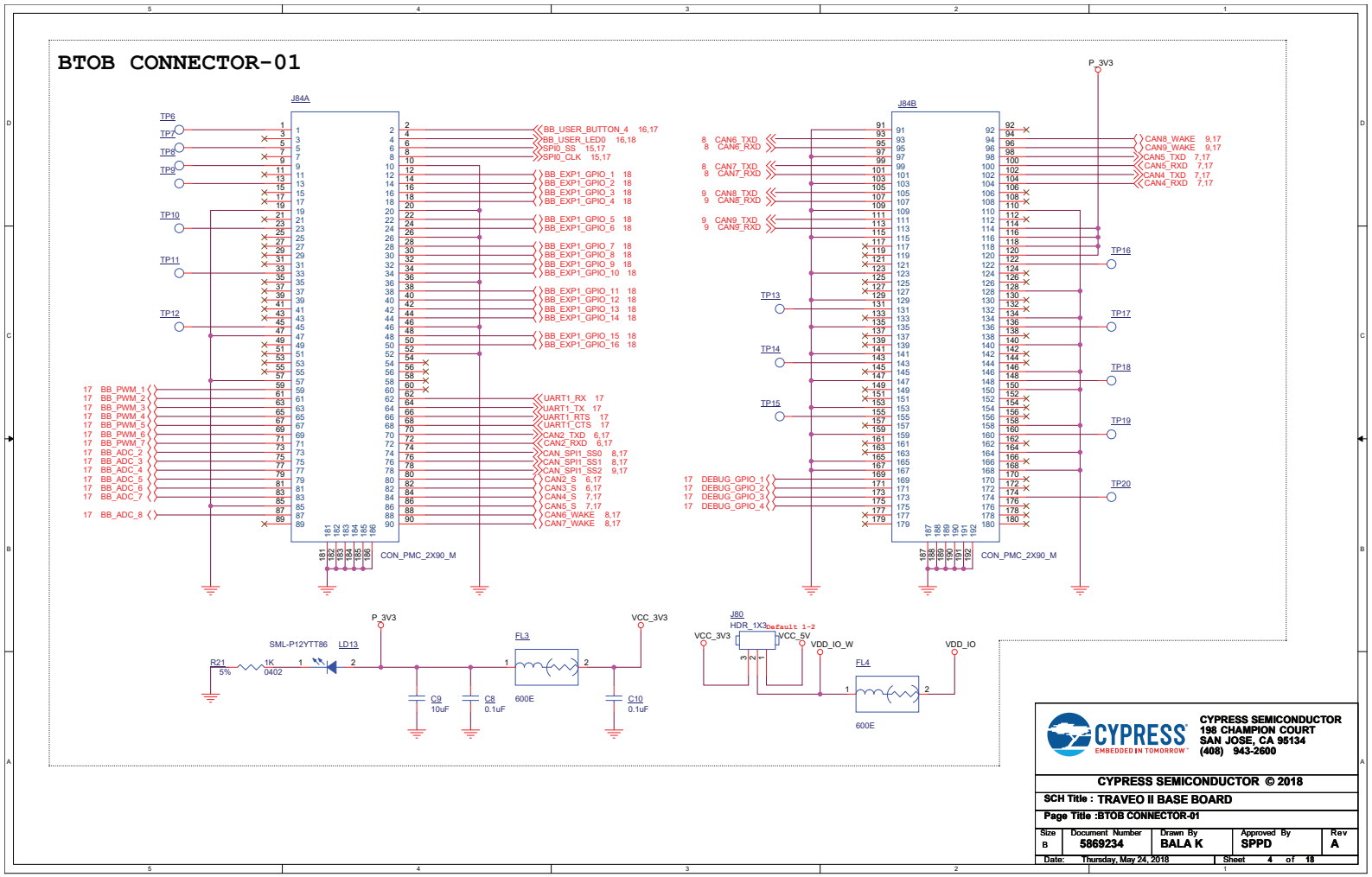


Figure C-3. BTOB Connector-02

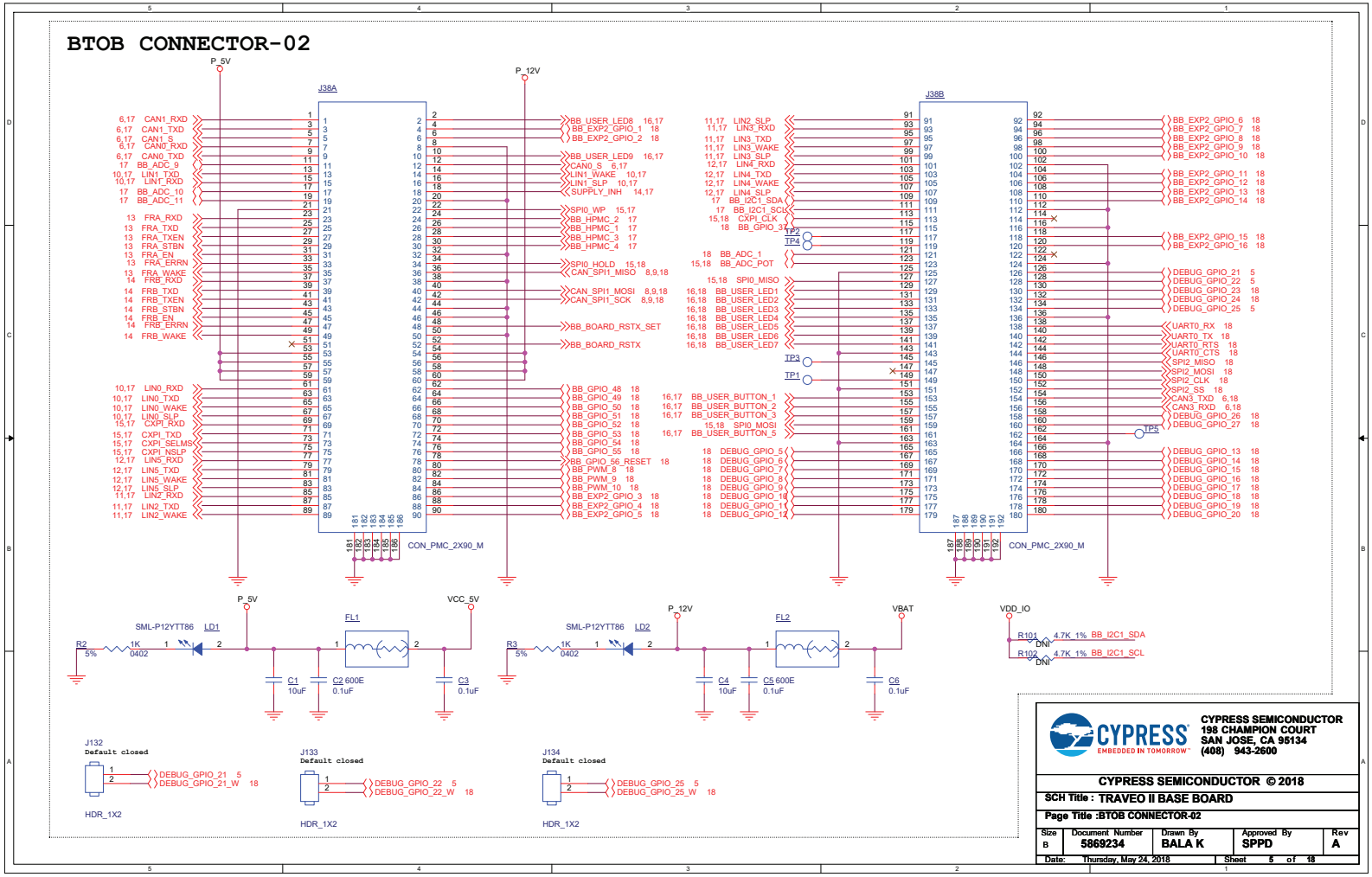


Figure C-4. CAN-FD_0 to 3

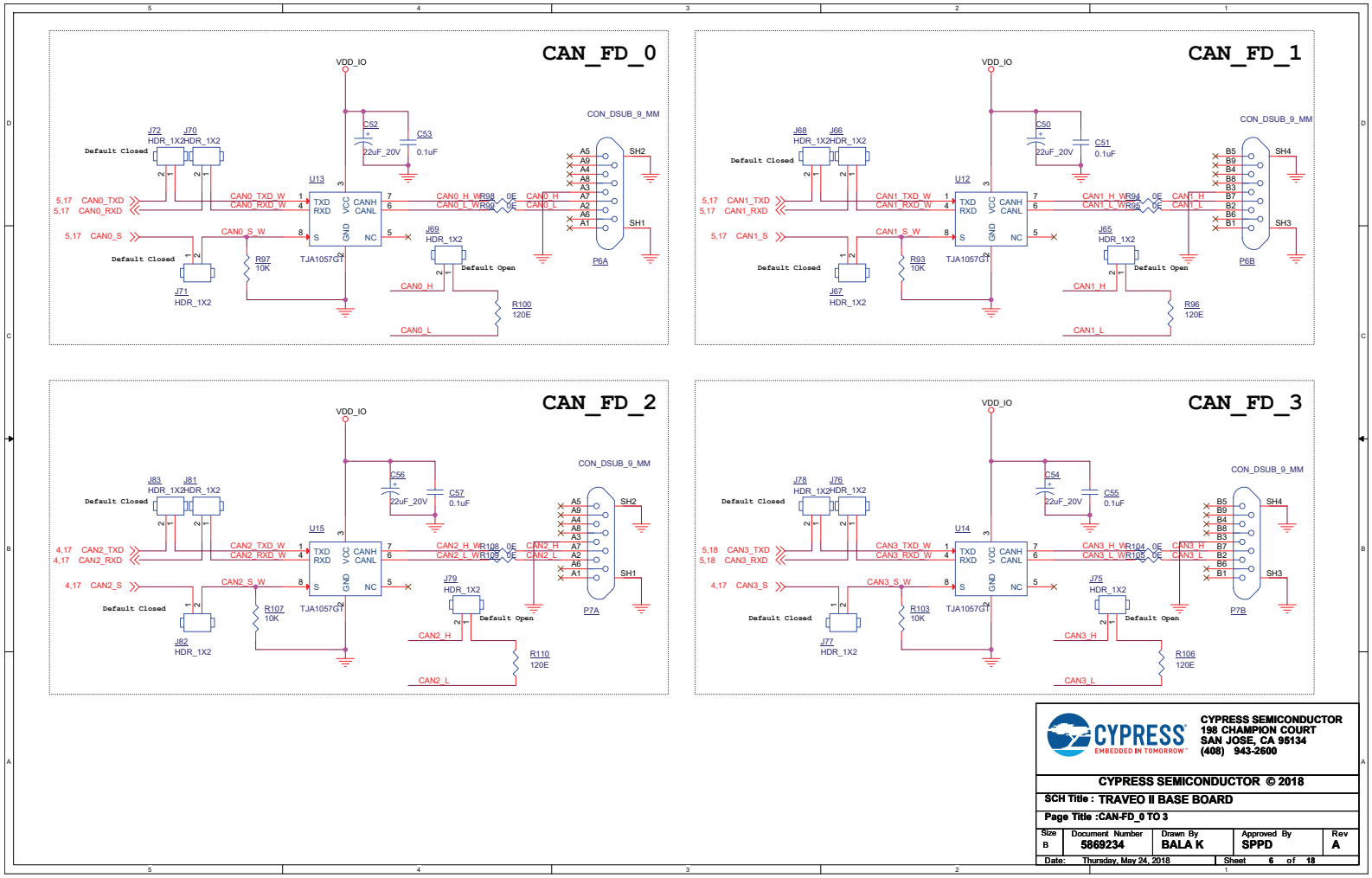


Figure C-5. CAN-FD_4 & 5

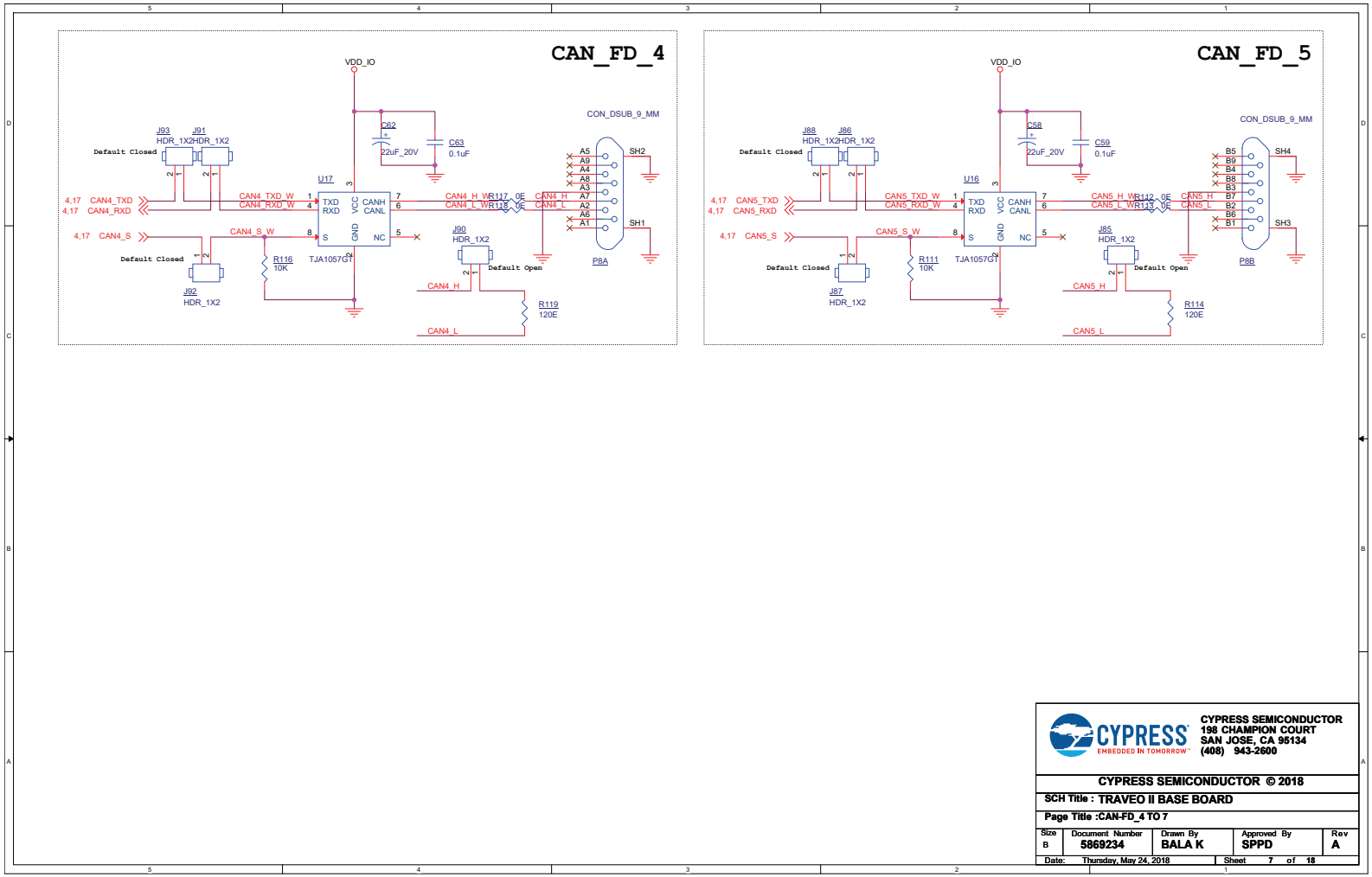


Figure C-6. CAN-FD_6 & 7

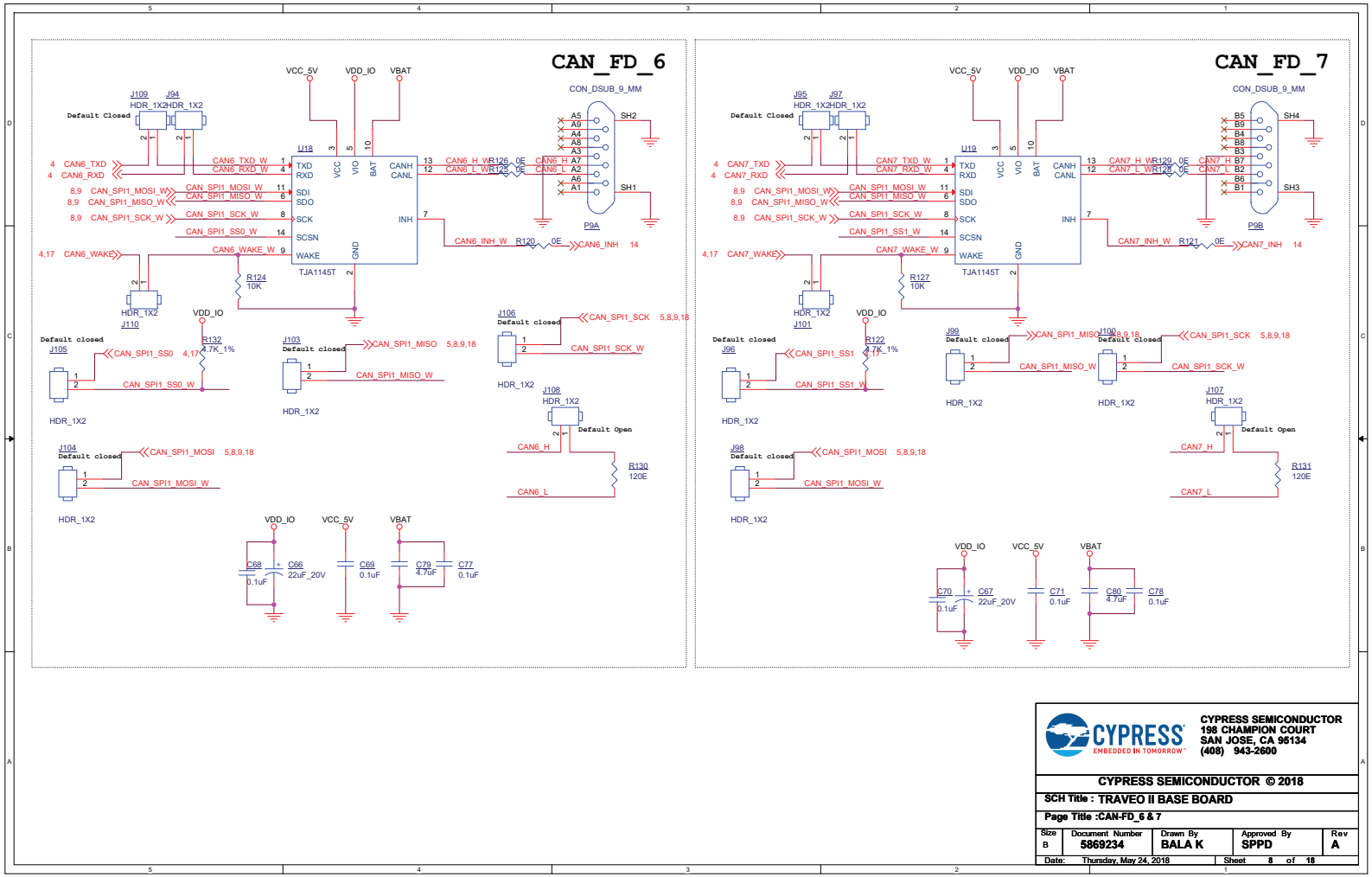


Figure C-7. CAN-FD_8 & 9

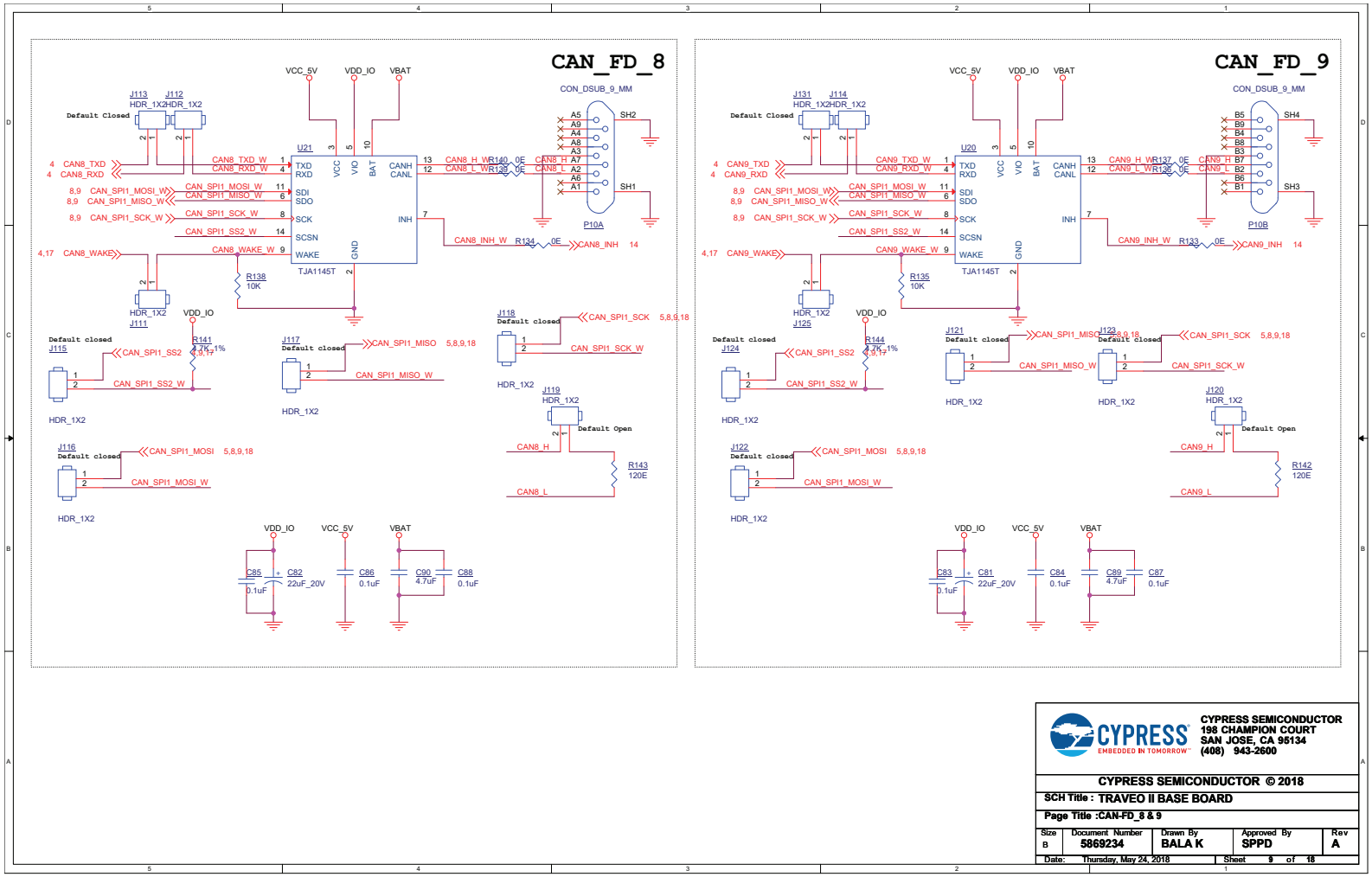


Figure C-8. LIN Interface_0 to 1

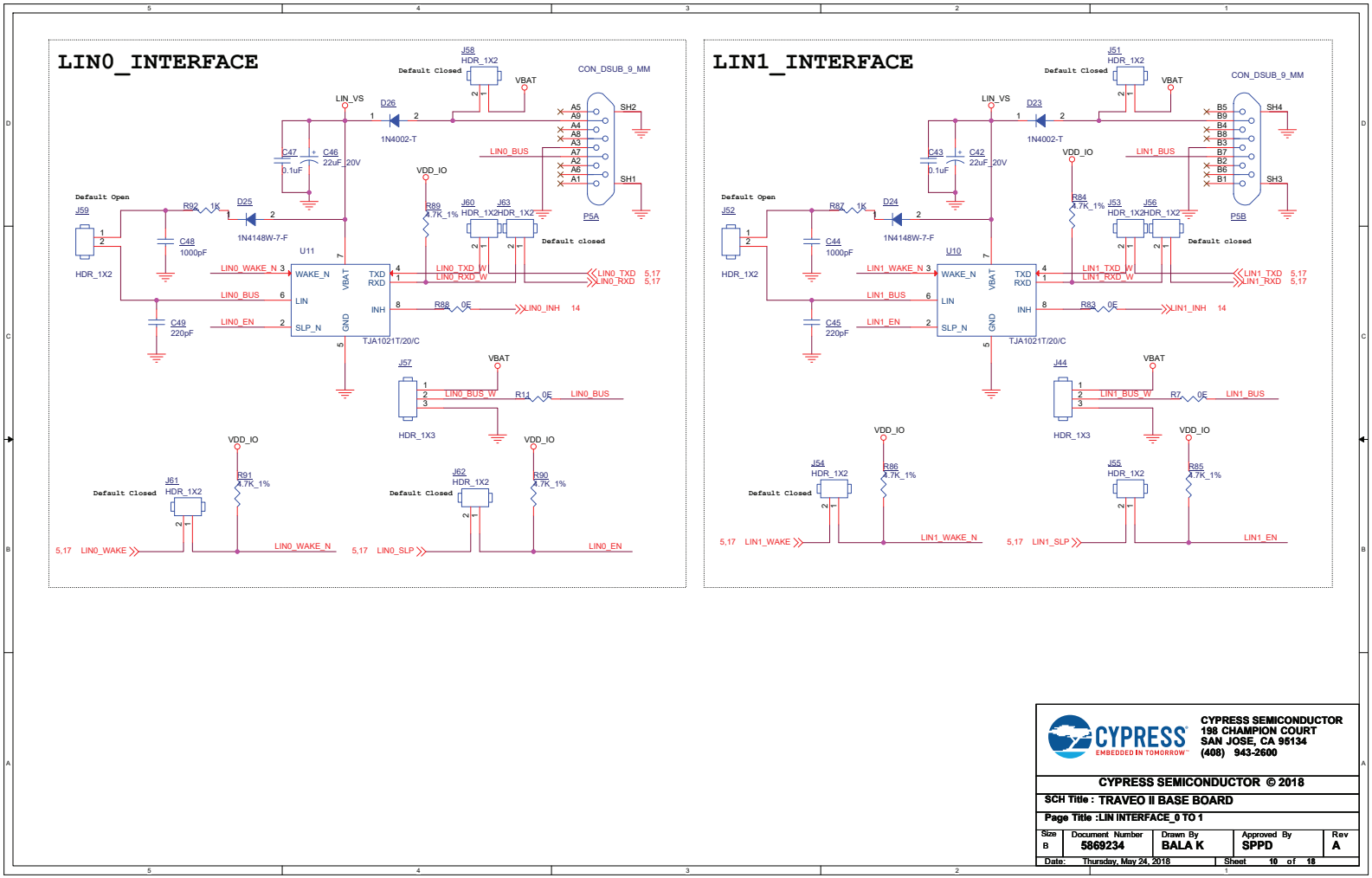


Figure C-9. LIN Interface_2 to 3

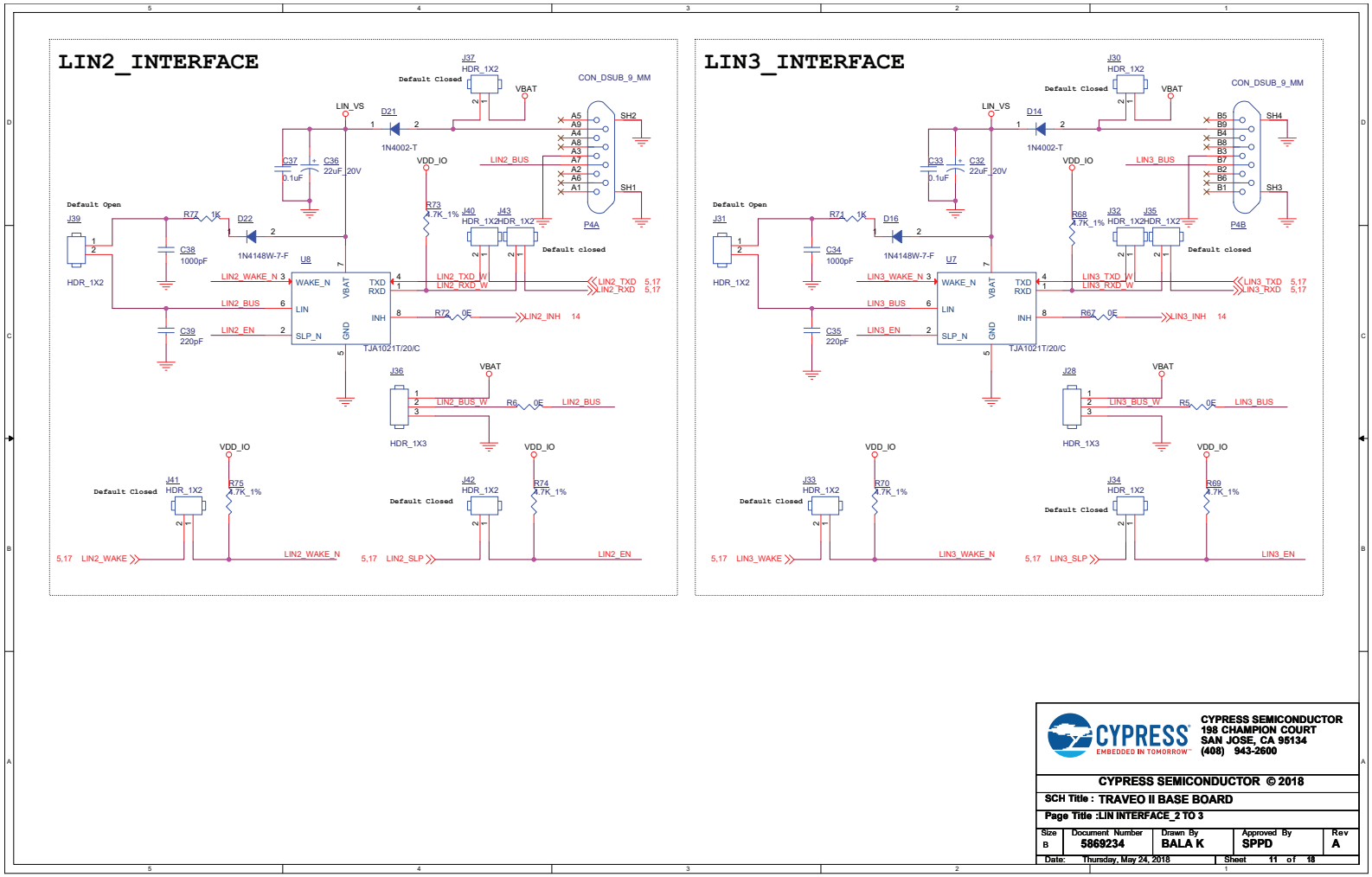


Figure C-10. LIN Interface_4 to 5

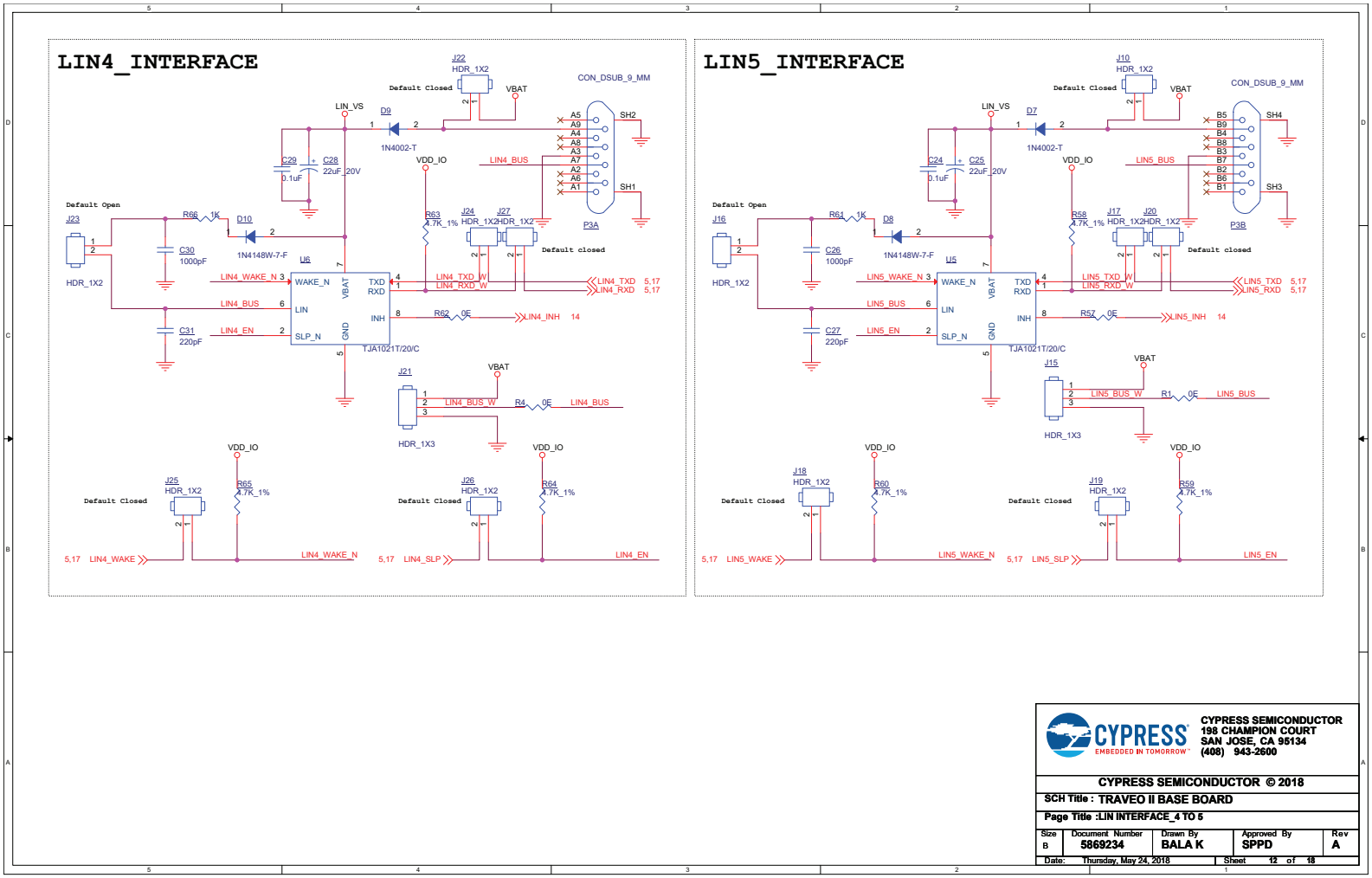


Figure C-11. FlexRay-01 & Reset

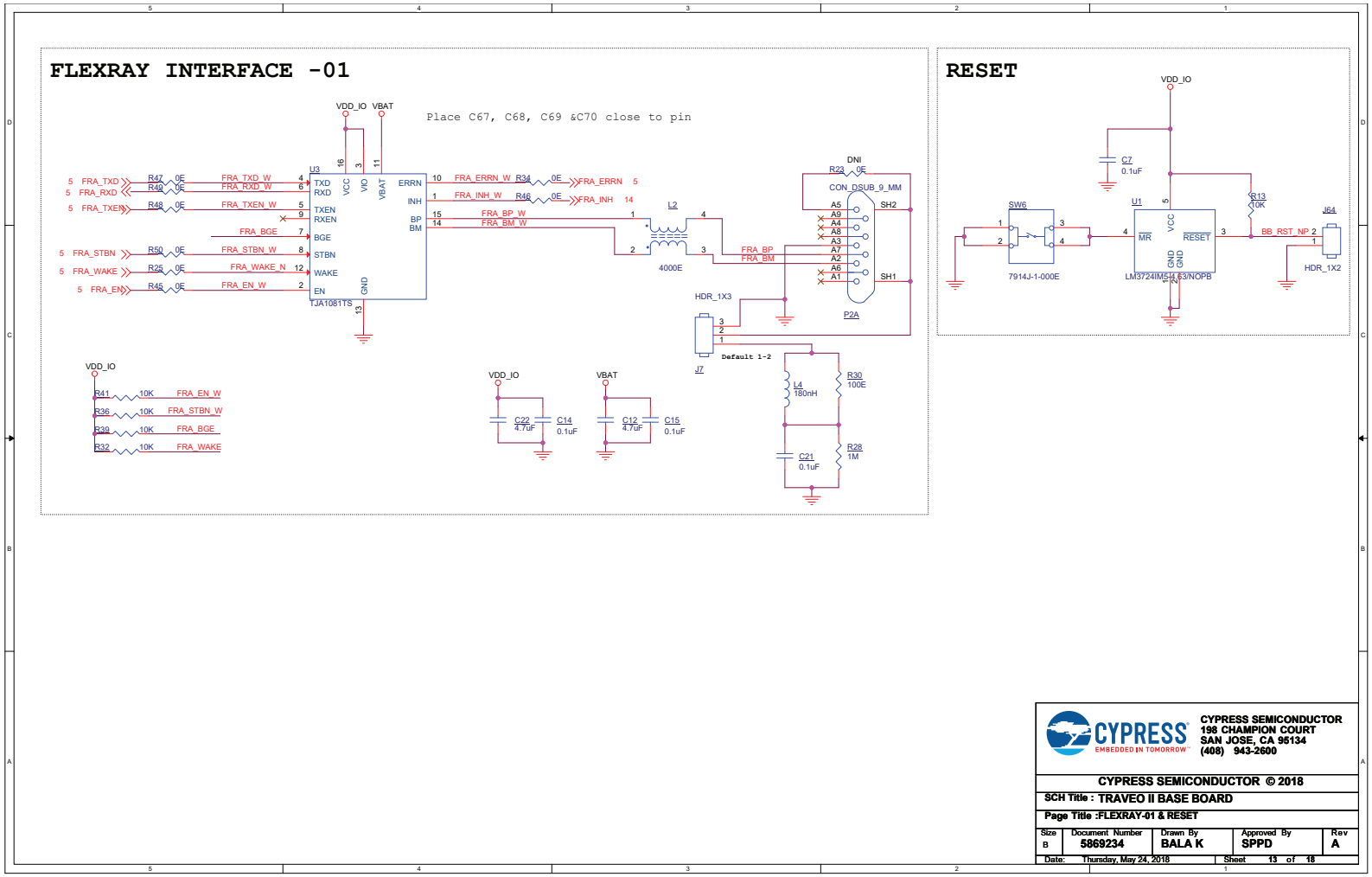


Figure C-12. FlexRay-02 & INH

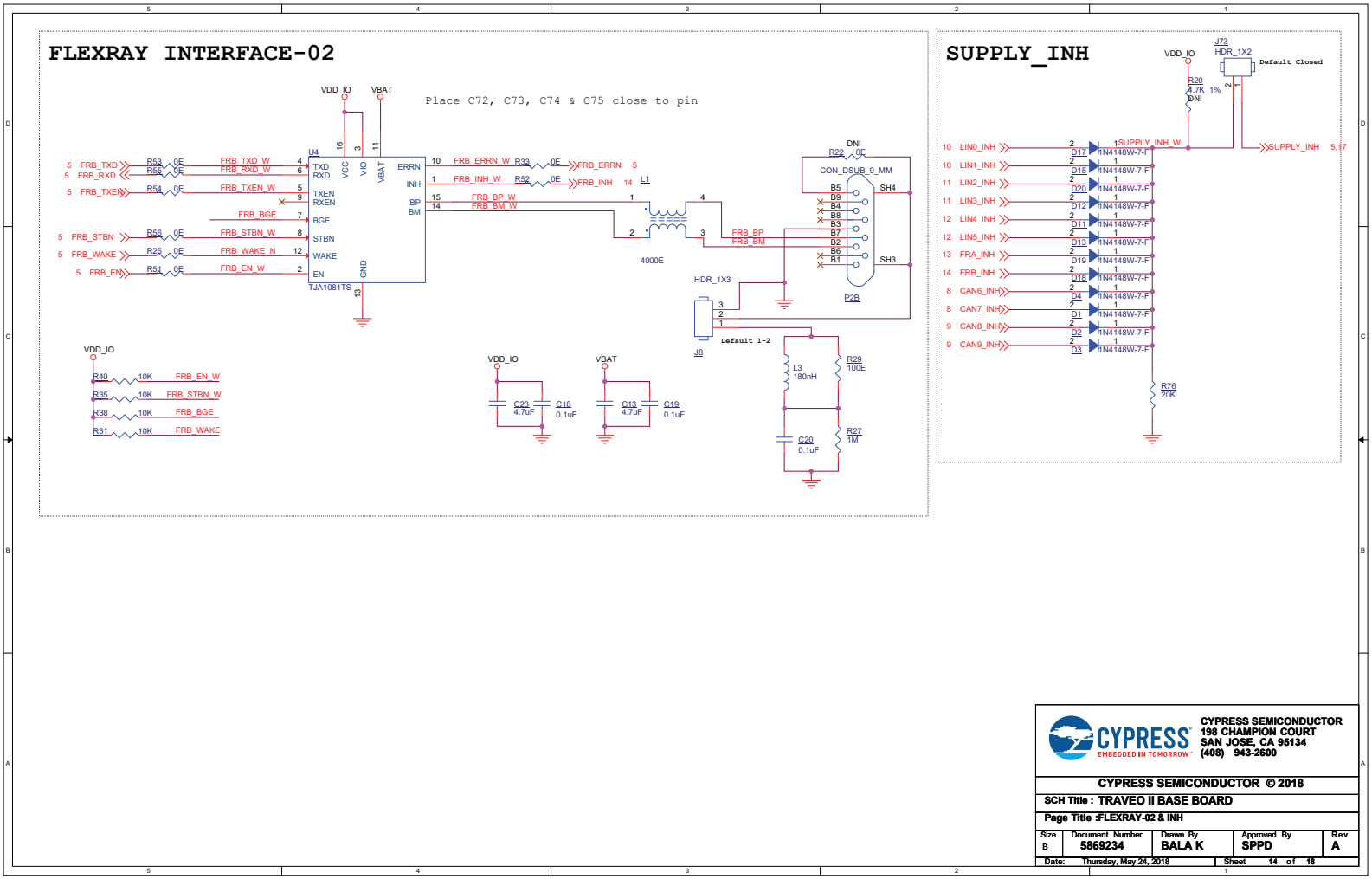


Figure C-13. CXPI, EEPROM & POT

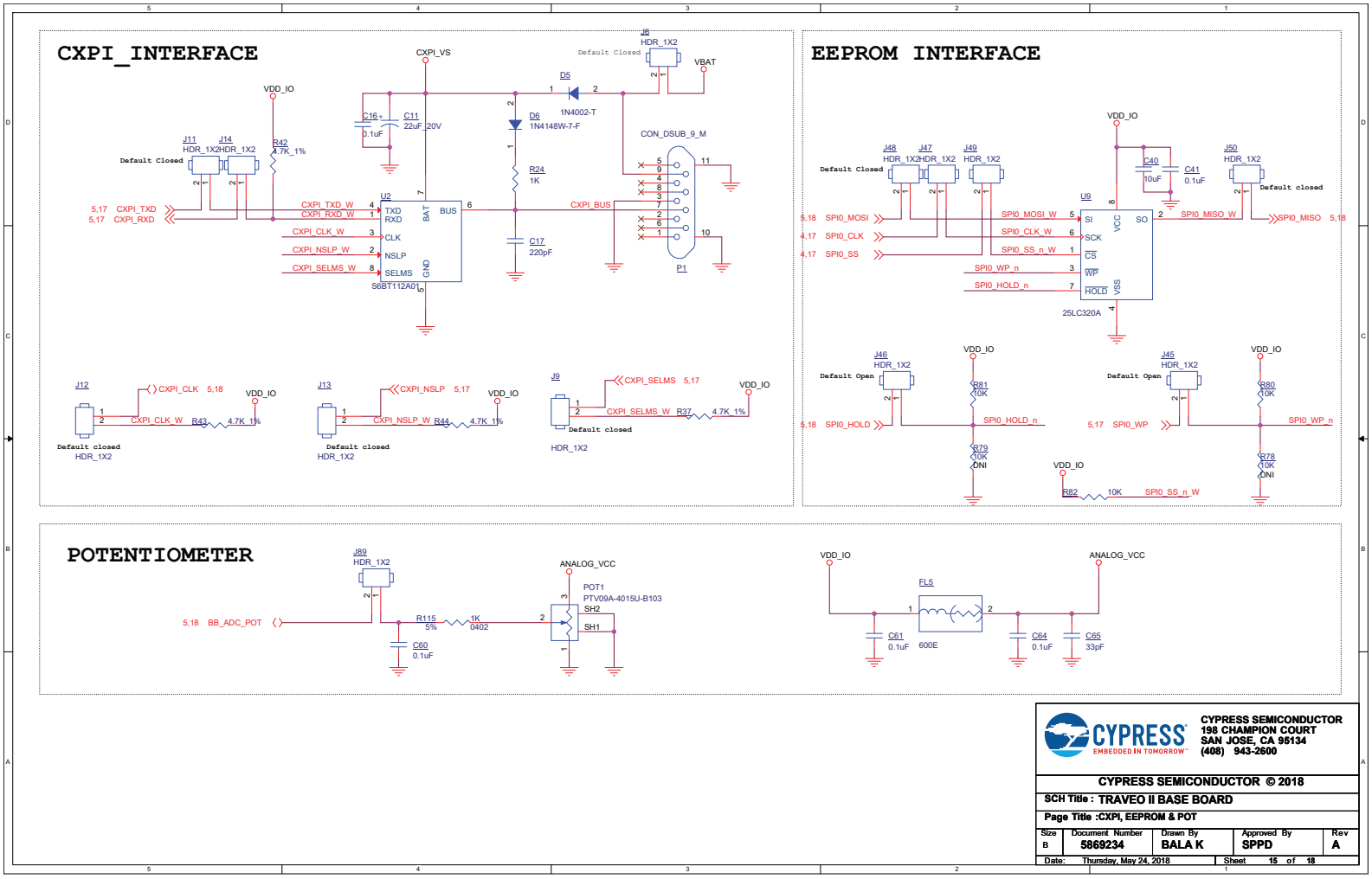


Figure C-14. User_Led & Pushbutton

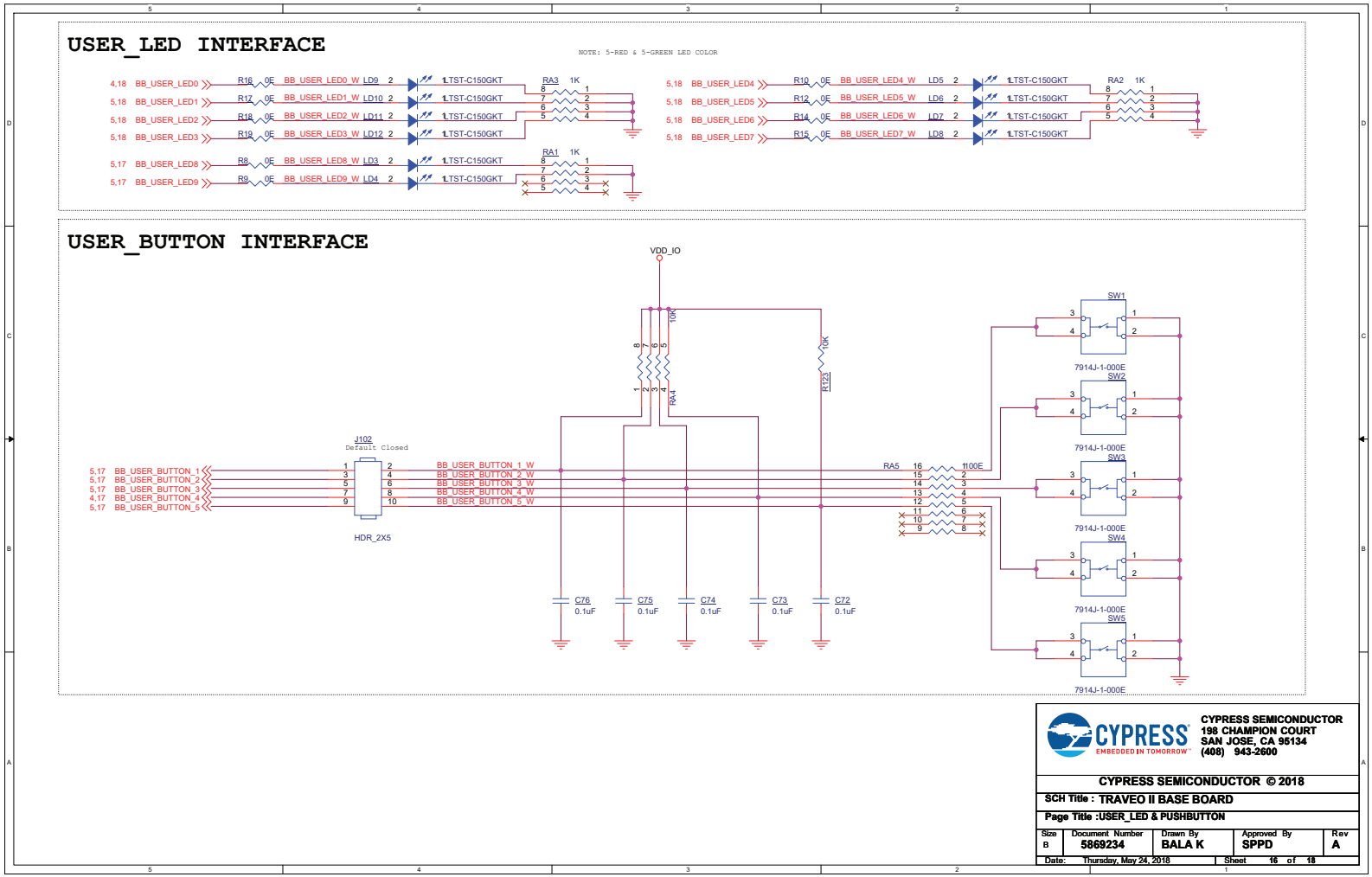


Figure C-15. Pin Header Section-01

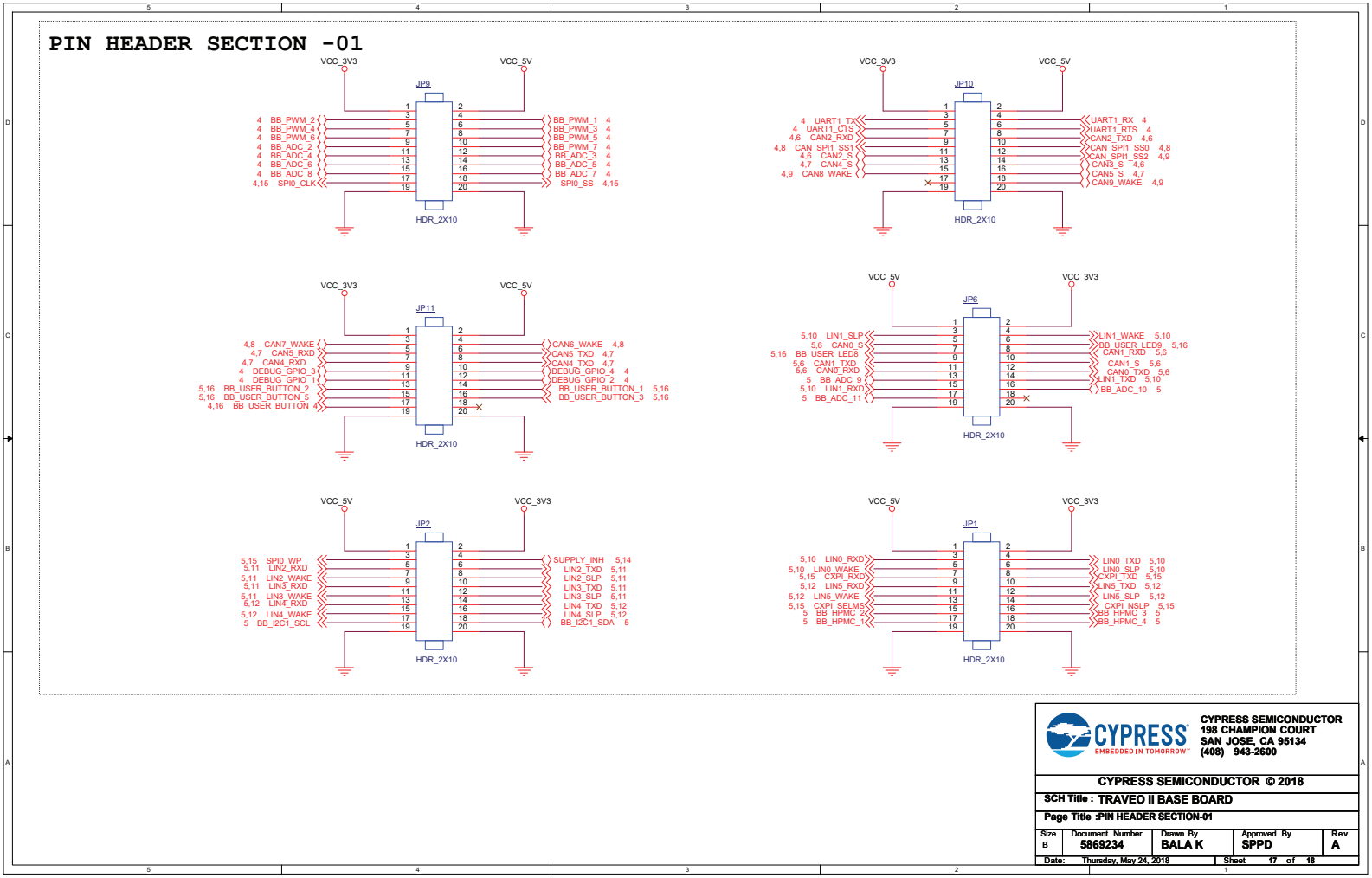
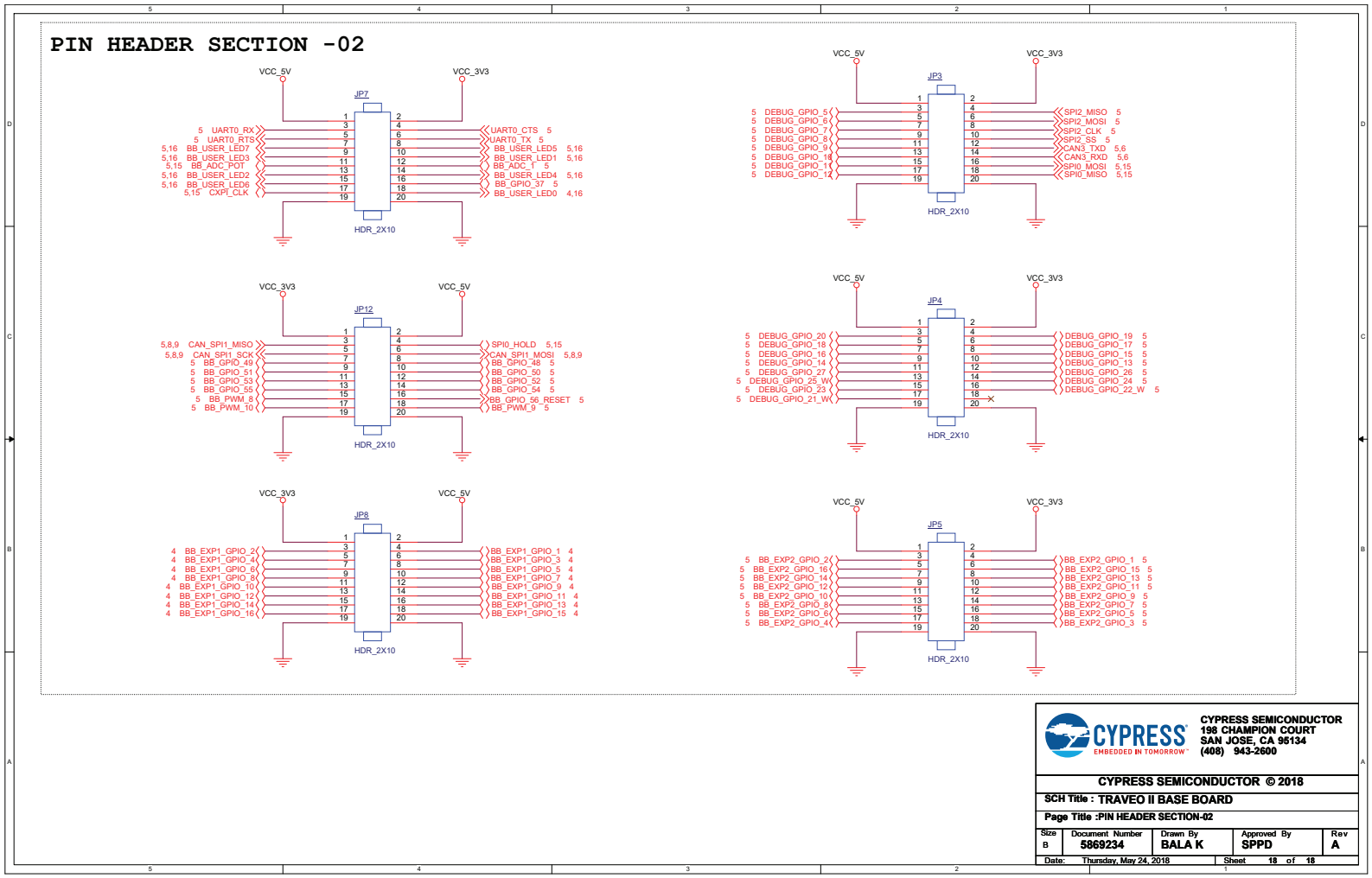


Figure C-16. Pin Header Section-02



D. Component Assembly on Base Board

This appendix shows the top and bottom assembly of the Traveo II Base board (CYTVII-B-E-BB).

Figure D-1. Component Assembly (Top)

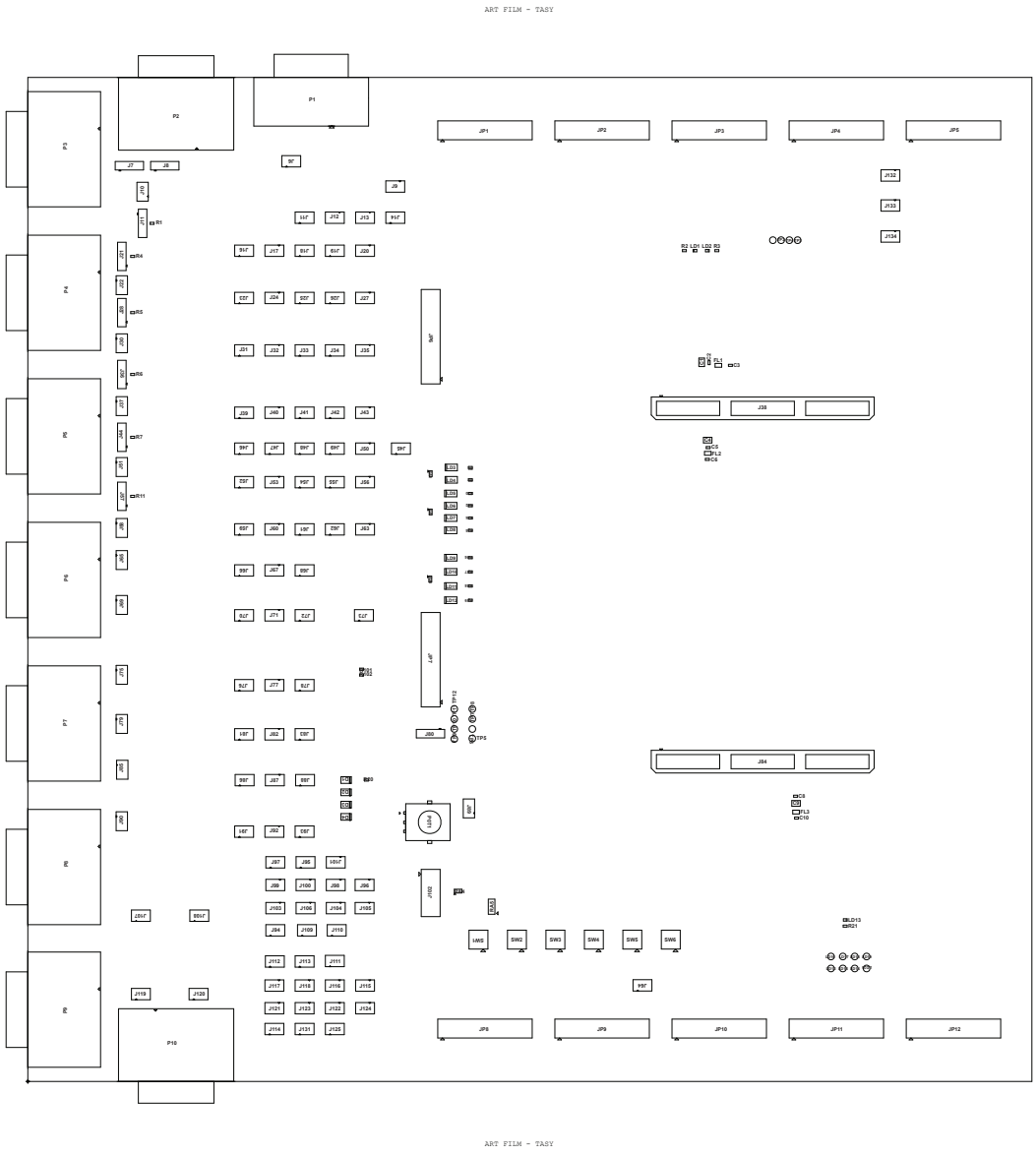
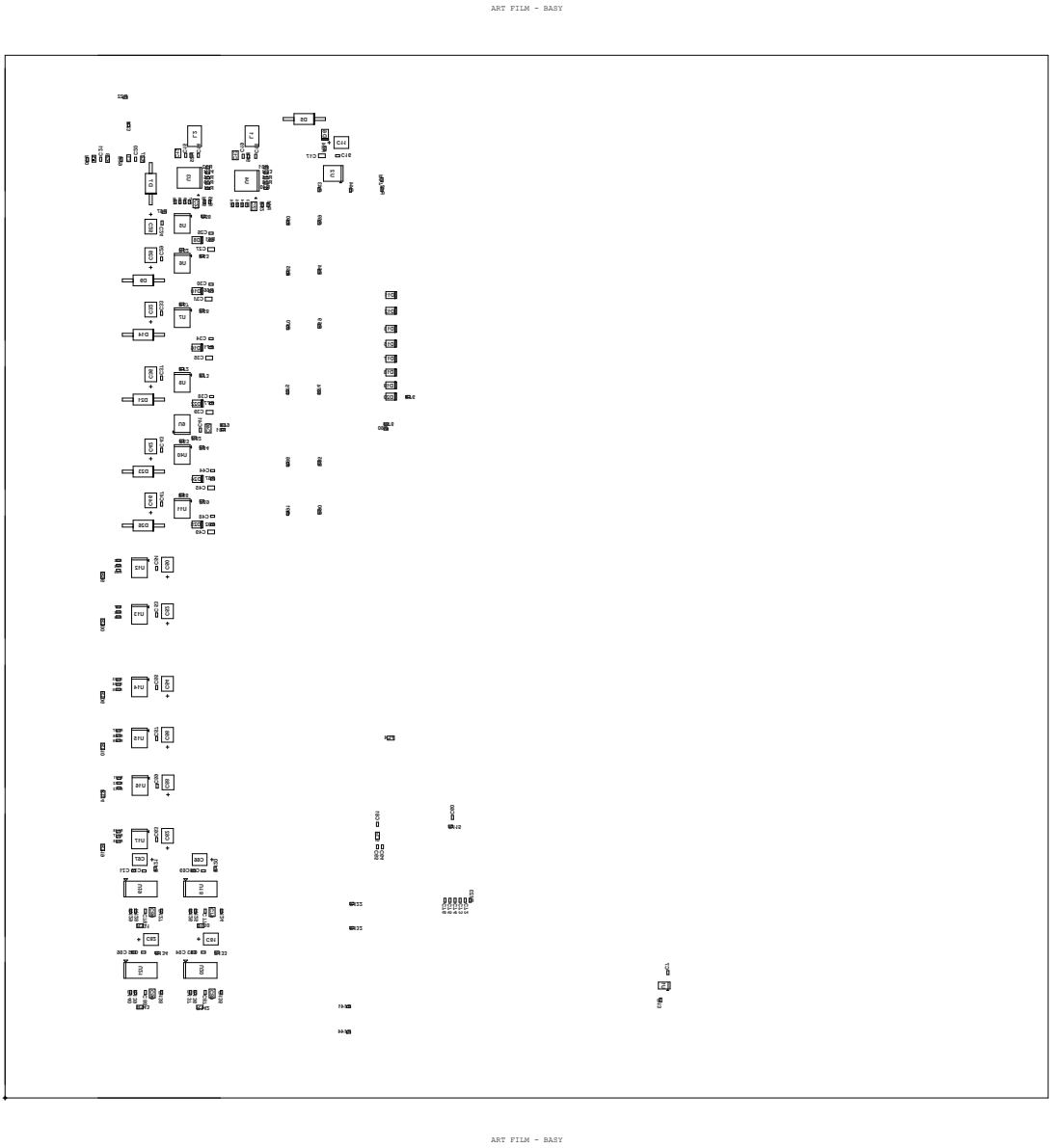


Figure D-2. Component Assembly (Bottom)



Revision History

Document Revision History

Document Title: CYTVII-B-H-4M-272-CPU Evaluation Board User Guide Document Number: 002-29936			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	6827146	03/17/2020	Initial release for CYTVII-B-H-4M-272-CPU Evaluation Board User Guide.