EiceDRIVER™

Tips & Tricks for RCIN and ITRIP

6EDL family - 2nd generation

Application Note AN2015-09

About this document

Scope and purpose

The RCIN and ITRIP functions strongly help to reduce the system cost. However, the functions as they are available do have limitations in some applications. This application note helps to understand the function more in detail and give application support how to overcome these limitations.

Intended audience

The application note addresses experienced hardware engineers who have already basic knowledge of the 6EDL family – 2nd generation.

Table of Contents

1 Introduction

The 6EDL family – 2nd generation is a family of versatile and robust driver ICs. This application note is related to the family's members given in Table 1

Table 1 Members of 6ED family – 2nd generation

Sales code	control input HIN1,2,3 and LIN1,2,3	UVLO threshold	Bootstrap diode	Package	Optimal for
6EDL04I06NT	negative logic	12.1V/10.2V	Yes	DSO28	IGBT
6EDL04I06PT	positive logic	12.1V/10.2V	Yes	DSO28	IGBT
6EDL04N06PT / 6EDL04N02PR	positive logic	8.9V/8.0V	Yes	DSO28 / TSSOP28	MOSFET
6ED003L06-F2 / 6ED003L02-F2	negative logic	12.1V/10.2V	No	DSO28 / TSSOP28	IGBT, replacement of 1st generation

The RCIN and ITRIP functions strongly help to reduce the system cost. However, the functions as they are available do have limitations in some applications. This application note helps to understand the functions in deep detail and gives application support on how to overcome the limitations.

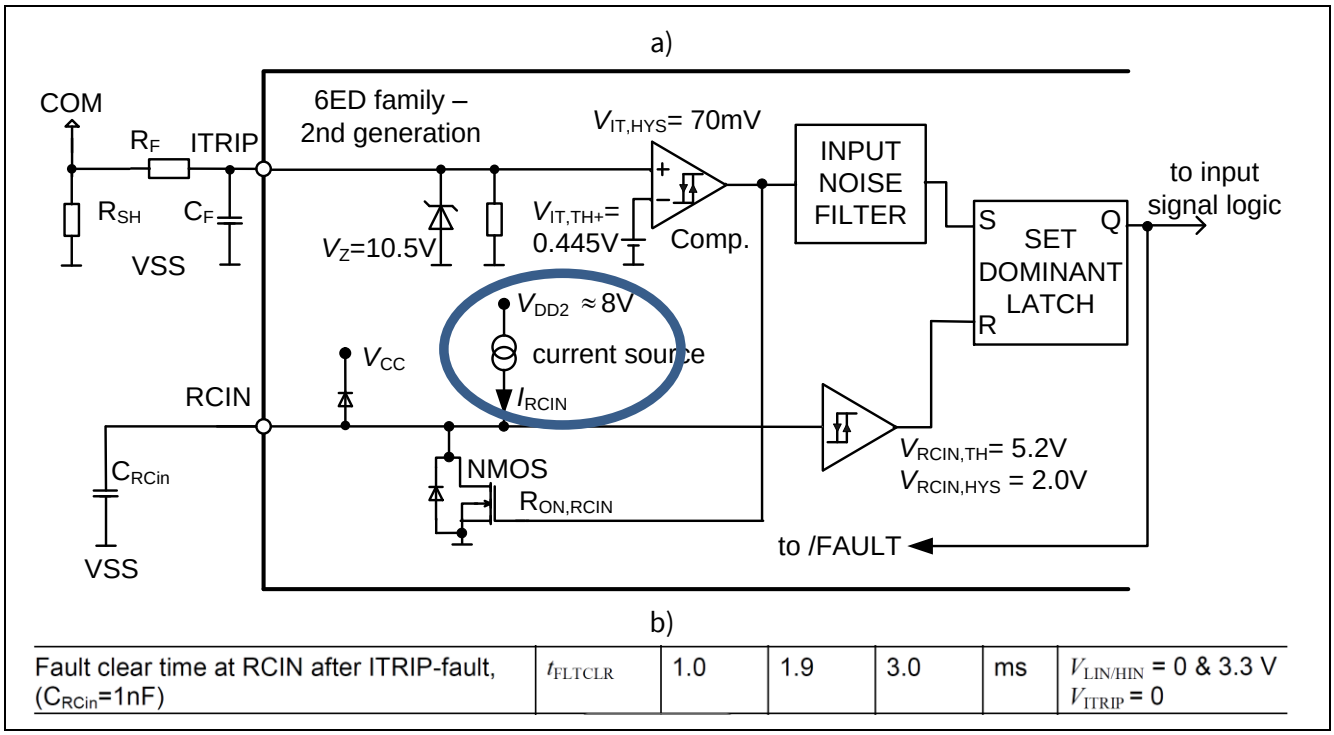
It is mandatory for the understanding of this document to carefully read the datasheet [1] and the 6EDL technical description [2].

2 Overcoming the large tolerance of the RCIN timing

This section describes how the rather large tolerance of the RCIN timing can be overcome.

2.1 Application problem

The RCIN function ([1], [2]) of the 6EDL family – 2nd generation provides an integrated current source as depicted in a) of Figure 1. It usually allows skipping an external pull-up resistor. The tolerance of this current source can be derived from a specific datasheet parameter according to b) in Figure 1.



b)

Fault clear time at RCIN after ITRIP-fault, (C_{RCin}=1nF)	t_{FLTCLR}	1.0	1.9	3.0	ms	$V_{LIN/HIN}$ = 0 & 3.3 V V_{ITRIP} = 0

Figure 1 a) RCIN circuit
b) Datasheet excerpt of the fault clear time t_{FLTCLR}

The fault clear time t_{FLTCLR} specifies the charging time of the RCIN capacitor C_{RCIN} in the datasheet. The RCIN capacitor is charged from the internal current source for this parameter. Therefore, the tolerance of the current source can be derived from the parameter tolerances. This means that the tolerance of the current source is approx. –52 % and + 58 %. Such tolerances may be not acceptable especially for fault clear times t_{FLTCLR} which are longer than 5 ms. For simplification, it is assumed in the following sections that the internal current source has a tolerance of ± 50%.

2.2 Application solution

The situation which is described in section 2.1 can be solved by applying an additional, highly accurate current source to charge the capacitor C_{RCIN} according to Figure 2. This can be implemented by a pull-up resistor R_{RCIN} to a voltage V_{pu}. The pull-up resistor must have a tolerance of 1%. The pull-up current needs to be large enough to tune the overall charging current into a suitable design window.

Overcoming the large tolerance of the RCIN timing

Two assumptions are made:

- The pull-up current I_{RRCIN} and the value I_{RCIN} of the integrated current source according to Figure 2 are small with respect to the initial current amplitude during discharge of the capacitor C_{RCIN}. Therefore, only the capacitor C_{RCIN} dominates the discharge process

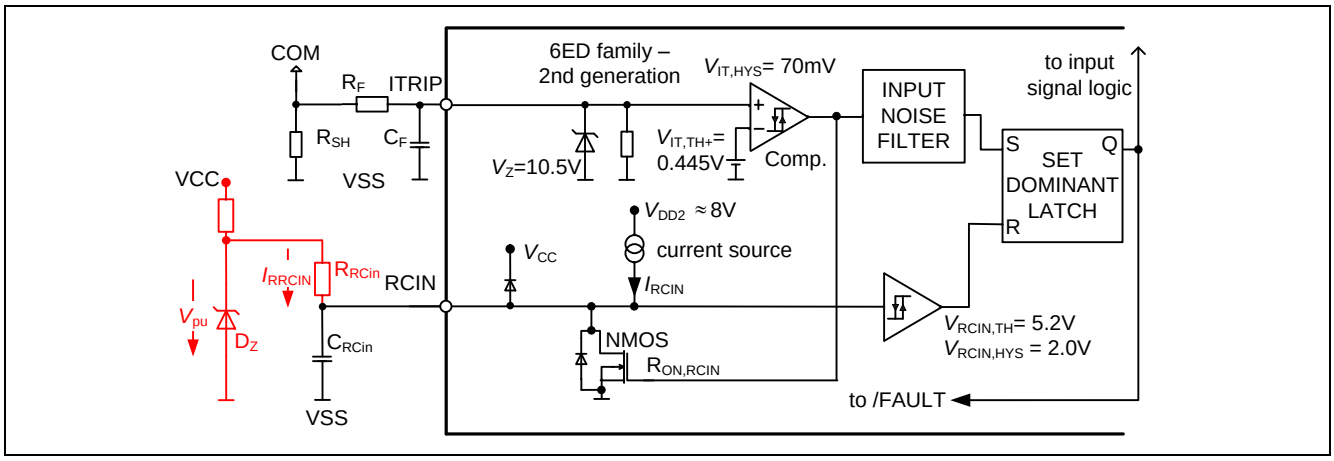


Figure 2 Improved RCIN circuit

- Target power transistor is a IKD06N60RF

It is described in [2] that the pull-up resistor bears the risk that the capacitor C_{RCIN} is not discharged fast enough, so that the IC also does not reach the ITRIP latch state. This is shown in the right part of Figure 3. It leads to an occurrence of multiple short circuit or overcurrent shut-down events without getting into the fault clear state. Therefore, the maximum discharge time must remain smaller than the minimum shut down propagation delay

$$t_{\text{discharge}} = -R_{\text{on,RCIN}} \cdot C_{\text{RCIN}} \quad ln\frac{V_{\text{th,RCIN-}}}{V_{\text{pu}}} < T_{\text{ITRIP,min}} + t_{\text{d(off),min}} \tag{1}$$

The evaluation of this equation shows that it can easily get critical to use the IC´s supply voltage V_{VCC} as the pull-up voltage:

$$t_{\text{discharge}}(C_{\text{RCIN}} = 10\ \text{nF}, V_{\text{pu}} = 15\ \text{V}) = 0.62\ \mu\text{s} < 400\ \text{ns} + 106\ \text{ns} = 506\ \text{ns} \tag{2}$$

This means that the shut down occurs earlier than the discharge reaches the latching level of 3.2 V. Thus, the IC does not reach the safe fault clear state and activates its outputs again. This is shown in the right part of Figure 3.

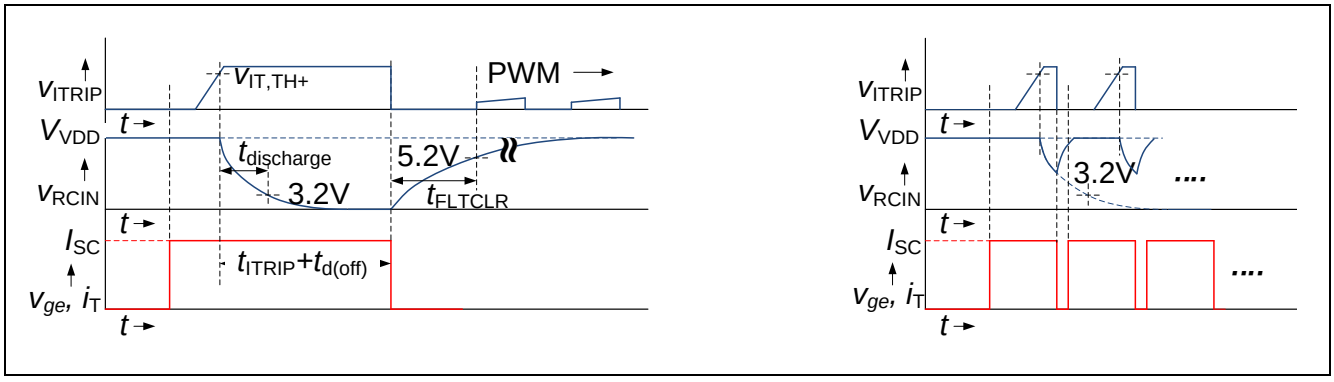


Figure 3 left: suitable RCIN timing with safe fault clear state
right: bad RCIN timing without reaching fault clear state

Overcoming the large tolerance of the RCIN timing

So both, charging and discharging of the capacitor C_{RCIN} must be carefully evaluated in order to achieve a suitable and precise RCIN timing according to the left part of Figure 3. A lower pull-up voltage can be necessary and can be achieved by implementing a stabilized voltage source by means of a biased zener diode according to the red parts in Figure 2. It is assumed that the current through R_{RCIN} is constant during the charging and discharging until the relevant thresholds are reached.

The pull-up current through resistor R_{RCIN} is superposed onto the current I_{RCIN} of the integrated current source. The integrated current source delivers I_{RCIN} = 2.8 µA with a tolerance of Tol_{intCS}. The total target tolerance of the charging current is *Tol*. The charging current through R_{RCIN} can be calculated to be

$$I_{\mathrm{RRCIN,charge}} = \left(\frac{Tol_{\mathrm{intCS}}}{Tol} - 1\right) \cdot I_{\mathrm{RCIN}} \tag{3}$$

The charging current through R_{RCIN} leads to the corresponding resistance value of

$$R_{\mathrm{RCIN}} = \frac{V_{\mathrm{pu}}}{I_{\mathrm{RRCIN,charge}}} \tag{4}$$

The calculated fault clear time including a pull-up resistor R_{RCIN} is depicted in Figure 4. The target capacitor value C^*_{RCIN} can be calculated by scaling with the ratio of a given fault clear time and the target fault clear time $t_{FLTCLR,target}$ using the calculated value of R_{RCIN} in equation (4). The application example in section 2.3 explains this procedure in detail. The scaling calculation is

$$C^*_{\mathrm{RCIN}} = \frac{t_{\mathrm{FLTCLR,target}}}{t_{\mathrm{RRCIN,CRCIN}}} \cdot C_{\mathrm{RCIN}} \tag{5}$$

Now, equation (1) can be executed and verified by using C^*_{RCIN} .

2.3 Application example

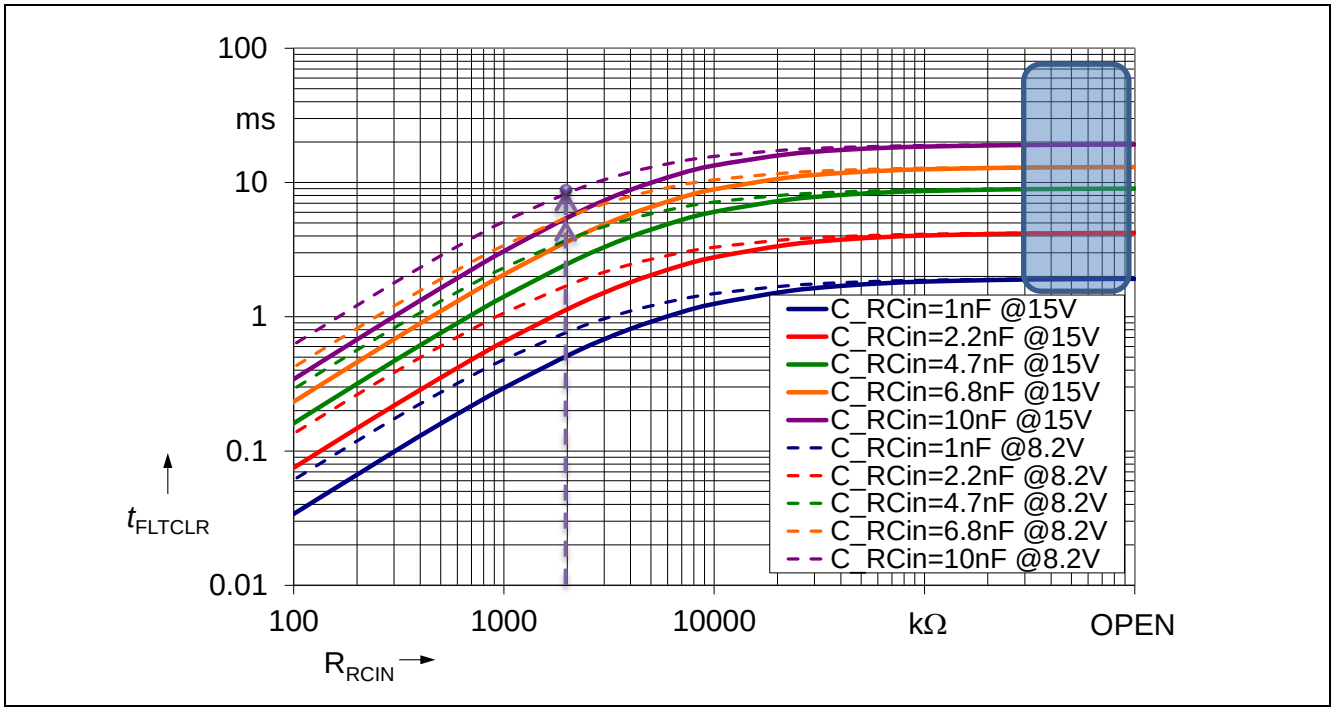


Figure 4 Resulting fault clear time of C_{RCIN} in combination with R_{RCIN}. The shadowed area shows the fault clear time without R_{RCIN}

Overcoming the large tolerance of the RCIN timing

The application example should achieve the target behavior including:

- Overall tolerance *Tol* < 20 %
- Fault clear time t_{FLTCLR} = 10 ms
- The pull-up voltage is V_{pu} = 8.2 V

Executing equation (3) with the target conditions results in

$$I_{\text{charge,RRCIN}} = \left(\frac{Tol_{\text{intCS}}}{Tol} - 1\right) \cdot I_{\text{RCIN}} = \left(\frac{50\%}{20\%} - 1\right) \cdot 2.8\ \mu\text{A} = 4.2\ \mu\text{A} \quad (6)$$

The related pull-up resistance is

$$R_{\text{RCIN}} = \frac{V_{\text{pu}}}{I_{\text{charge,RRCIN}}} = \frac{8.2\ \text{V}}{4.2\ \mu\text{A}} = 1.95\ \text{M}\Omega \quad (7)$$

The closest match of the E24 series of resistors is a value of 2.0 MΩ.

The scaling of the read out value in Figure 4 is now the next procedure step. The readout value of the dashed purple line at R_{RCIN} = 2.0 MΩ and C_{RCIN} = 10 nF is t_{FLTCLR} = 8.5 ms. The calculated capacitance C^*_{RCIN} is

$$C^*_{\text{RCIN}} = \frac{t_{\text{FLTCLR,target}}}{t_{\text{RRCIN,CRCIN}}} \cdot C_{\text{RCIN}} = \frac{10\ \text{ms}}{8.5\ \text{ms}} \cdot 10\ \text{nF} = 11.8\ \text{nF} \quad (8)$$

A close value is C_{RCIN} = 12nF. The last step in the design procedure is to verify the proper discharge of C_{RCIN} with the selected values for R_{RCIN} and C_{RCIN}

$$t_{\text{discharge}} = -R_{\text{on,RCIN}} \cdot C_{\text{RCIN}}\ \ ln\frac{V_{\text{th,RCIN-}}}{V_{\text{pu}}} = 40\ \Omega \cdot 12\ \text{nF}\ \cdot ln\frac{3.2\ \text{V}}{8.2\ \text{V}} = 0.452\ \mu\text{s} \quad (9)$$

The discharge time is short enough to ensure a safe shut down of the power transistor and a latch of the ITRIP event. Nevertheless, a practical verification by measurements in the system is required.

2.4 Limitations of the proposed solution

The limitation of this approach is the discharge condition according to equation (1). The concept of the proposed solution is based on the assumption that the discharge of capacitor C_{RCIN} is faster than the minimum total shut down delay time. This time includes the IC´s minimum shutdown propagation delay $t_{ITRIP,min}$ and the power transistor´s minimum turn-off propagation delay $t_{(off),min}$. This is difficult to achieve for power transistors with a very small current rating.

Further limitations are especially other component tolerances, such as the capacitance C_{RCIN}, the temperature influence on resistance R_{RCIN} or the zener voltage tolerances.

3 Overcome the high trigger level of the ITRIP function

This section describes how the high trigger level of the overcurrent shut down function can be adapted towards lower levels.

3.1 Application problem

The shunt, which is located in the emitter path of a low side IGBT, generates a voltage according to its bias point. This voltage is filtered by means of a R_F / C_F –combination according to Figure 5.

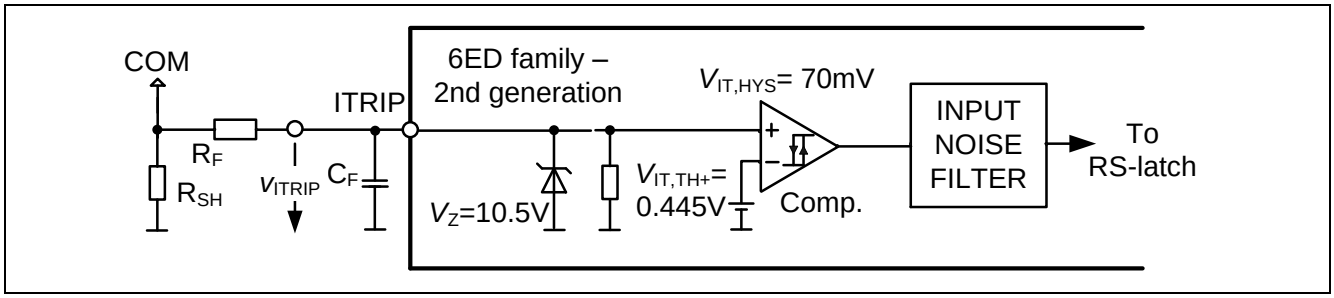


Figure 5 ITRIP function

The ITRIP trigger level of $V_{IT,th+}$ = 0.445 V is fixed for the 6EDL family – 2nd generation. The adjustment of the triggering current level is done by adjusting the shunt value, so that the shunt's voltage will trigger the ITRIP event. However, applications with high load currents will dissipate a considerable power in the shunt. For example, a current trigger level of 50 A would dissipate a power of 50 A · 0.445 V = 22.25 W. Therefore, the current trigger level should result in a low shunt voltage in the area of 100 mV to 200 mV in order to reduce the power dissipated in the shunt.

3.2 Application solution

The application solution is implemented by an additional voltage drop over the filter resistor R_F. The voltage drop is generated by a current added by a pull up-resistor R_{pu} according to Figure 6.

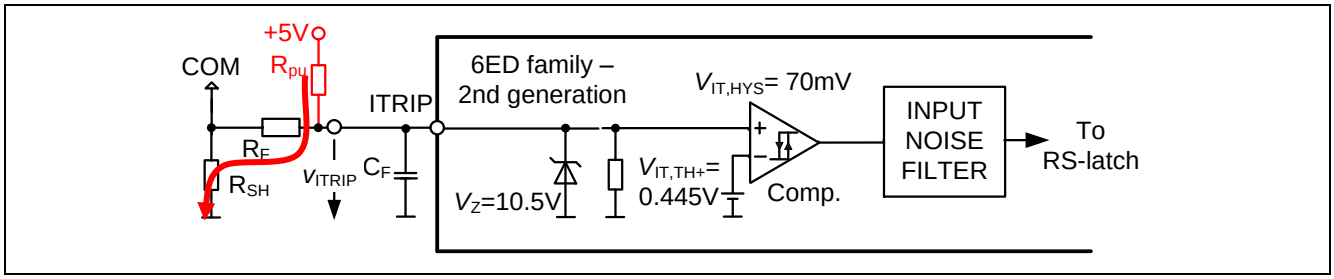


Figure 6 ITRIP function with pre-bias circuit

The required voltage drop of the resistor R_F is calculated with

$$V_{\mathrm{IT,th}} = V_{\mathrm{RF}} + V_{\mathrm{SH,max}} \implies V_{\mathrm{RF}} = V_{\mathrm{IT,th}} - V_{\mathrm{SH,max}} \tag{10}$$

This results in a required pull-up current of

$$I_{\mathrm{RF}} = \frac{V_{\mathrm{RF}}}{R_{\mathrm{F}}} \tag{11}$$

Now the pull-up resistor value which provides the current I_{RF} can be calculated

$$R_{pu} = \frac{V_{pu} - V_{IT,th}}{I_{RF}} \quad (12)$$

3.3 Application example

The example in this document is based on these conditions and assumptions:

- The triggering current of an ITRIP event should result in a shunt voltage of 200 mV
- The pull-up voltage is 5 V
- R_F = 1 kΩ ($\gg R_{SH}$)

The execution of equations (10) - (12) is

$$V_{RF} = V_{IT,th} - V_{SH,max} = 0.445\ V - 0.2\ V = 0.245\ V \quad (13)$$

The pull-up current will be

$$I_{RF} = \frac{V_{RF}}{R_F} = \frac{0.245\ V}{1\ k\Omega} = 0.245\ mA \quad (14)$$

Now the pull-up resistor value which provides the current I_{RF} can be calculated

$$R_{pu} = \frac{V_{pu} - V_{IT,th}}{I_{RF}} = \frac{5\ V - 0.445\ V}{0.245\ mA} \approx 18.6\ k\Omega \quad (15)$$

A selection of R_{pu} = 18 kΩ is possible. The design verification step executes the reworked equations (12) - (10) using the selected component values.

$$I_{RF} = \frac{V_{pu} - V_{IT,th}}{R_{pu}} = \frac{5\ V - 0.445\ V}{18\ k\Omega} = 0.253\ mA \quad (16)$$

This results in a voltage drop at the resistor R_F of

$$V_{RF} = I_{RF} \cdot R_F = 0.253\ mA \cdot 1\ k\Omega = 0.253\ V \quad (17)$$

The typical error is smaller than 5% and therefore acceptable with respect to the overall tolerance of the ITRIP function.

3.4 Limitations of the proposed solution

The most dominant limitation is the overall tolerance of the ITRIP function. It is of course possible to reduce the triggering shunt voltage of this function. However, the absolute tolerance of ± 65 mV remains. A very precise overcurrent shut down function can´t be achieved with this proposal. Nevertheless, the secure shut down of short circuit events is not jeopardized.

Additionally, the ITRIP hysteresis must be considered, so that the largest usable voltage drop over the resistor R_F is $V_{IT,th+,min} - V_{IT,hys,typ}$ = 380 mV – 70mV = 310 mV. Therefore, the resulting smallest shunt voltage is 65 mV + 70 mV = 135 mV. An additional margin of approximately 50 mV is recommended in order to ensure a proper power up.

Overcome the high trigger level of the ITRIP function

References

[1] Infineon Technologies: 6EDL family – 2nd generation; Datasheet; Infineon Technologies, Neubiberg, Germany.

[2] Infineon Technologies: 6EDL family – 2nd generation Technical description; Application Note AN-EICEDRIVER-6EDL04-1; Infineon Technologies, Neubiberg, Germany.

[3] Infineon Technologies: IKD06N60RF; Datasheet; Infineon Technologies, Neubiberg, Germany.

Revision History

Major changes since the last revision

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