EZ-PD™ CCG7D consumer cigarette lighter adapter (CLA) solution demo (SD2230) kit test report

About this document

Scope and purpose

This document provides test results of dual-port EZ-PD™ CCG7D consumer USB Type-C Power Delivery (PD) and buck-boost controller in cigarette lighter adapter (CLA) solution demo kit (SD2230).

Intended audience

This document is primarily intended for cigarette lighter adapter power electronics hardware designers using EZ-PD™ CCG7D consumer USB Type-C PD and buck-boost controller.

Abbreviations and definitions

Table 1 Abbreviations

Abbreviation	Description
AM	amplitude modulated wave
BCI	bulk current injection
CC-CV	constant current - constant voltage
CE	conducted emission
CH'x'	oscilloscope channel numbers
CW	unmodulated sine wave
DCM	discontinuous current mode
DP/DM	USB data positive / data negative lines
DUT/EUT	device under test / equipment under test
ESD	electrostatic discharge
FCCM	forced continuous conduction mode
FET	MOSFET (metal oxide semiconductor field effect transistor)
HCP	horizontal coupling pane
Io/I_{OUT}	output current of the DUT
NGDO	NFET gate driver output
OCP	overcurrent protection
OVP	overvoltage protection
P0/P1	Port #0/Port #1
PAT	power adaptor tester
PDO	power delivery output
P-P	peak-to-peak
PPS	programmable power supply

Abbreviation	Description
PSM	pulse skip mode
RE	radiated emission
SCP	short-circuit protection
SW1, SW2	buck converter switch node, boost converter switch node
UI	user interface
USB PD	universal serial bus power delivery
V_{BUS_C}	bus voltage at Type-C i.e., after provider/NGDO FET
V_{BUS_C}/V_{OUT}	output voltage of the DUT
V_{BUS_IN}	bus voltage before provider/NGDO FET
V_{IN}/V_{IN_DC}	input DC voltage to the DUT

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1 Introduction

The USB Power Delivery (USB PD) cigarette lighter adapter needs to deliver a wide range of configured positive output voltage and power from an automotive battery input ranging from 9 V – 24 V. A four-switch buck boost converter (FSBBC) is the suitable topology, which can support variable input voltages and configurable output voltage applications such as USB PD where high efficiency, power density is also required. The FSBBC configuration can act as buck, boost, or buck-boost converter to provide output voltage with the same polarity of the input voltage. Improved efficiency of the FSBBC is observed because of synchronous rectification. In similar lines buck only and boost-only operations can be achieved.

Constant-frequency peak current-mode control (PCMC) is a popular control technique for switched-mode power converters. PCMC offers built-in overcurrent protection, robust dynamic responses, simplified voltage-loop compensator design, and rejection of input voltage disturbances.

EZ-PD™ CCG7D consumer, a dual port USB Type-C Power Delivery controller with integrated buck - boost DC-DC controller is a single chip controller used for cigarette lighter adapter solution demo board.

EZ-PD™ CCG7D consumer is highly integrated dual-port USB Type-C PD solution with integrated buck-boost controllers. It complies to the latest USB Type-C and PD specifications, and is targeted for consumer multi-port power adapter applications. Integration offered by EZ-PD™ CCG7D-consumer not only reduces the bill of materials (BOM) but also provides a footprint optimized solution for power adapter charging needs. EZ-PD™ CCG7D-consumer has integrated gate drivers for VBUS NFET on the provider path. It also includes hardware-controlled protection features on the VBUS. EZ-PD™ CCG7D-consumer supports a wide input voltage range (4 V-24 V with 40-V tolerance) and programmable switching frequency (150 kHz – 600 kHz) in an integrated PD solution.

A high-level block diagram of the EZ-PD™ consumer-based dual-output USB PD cigarette lighter adapter is shown in **Figure 1**.

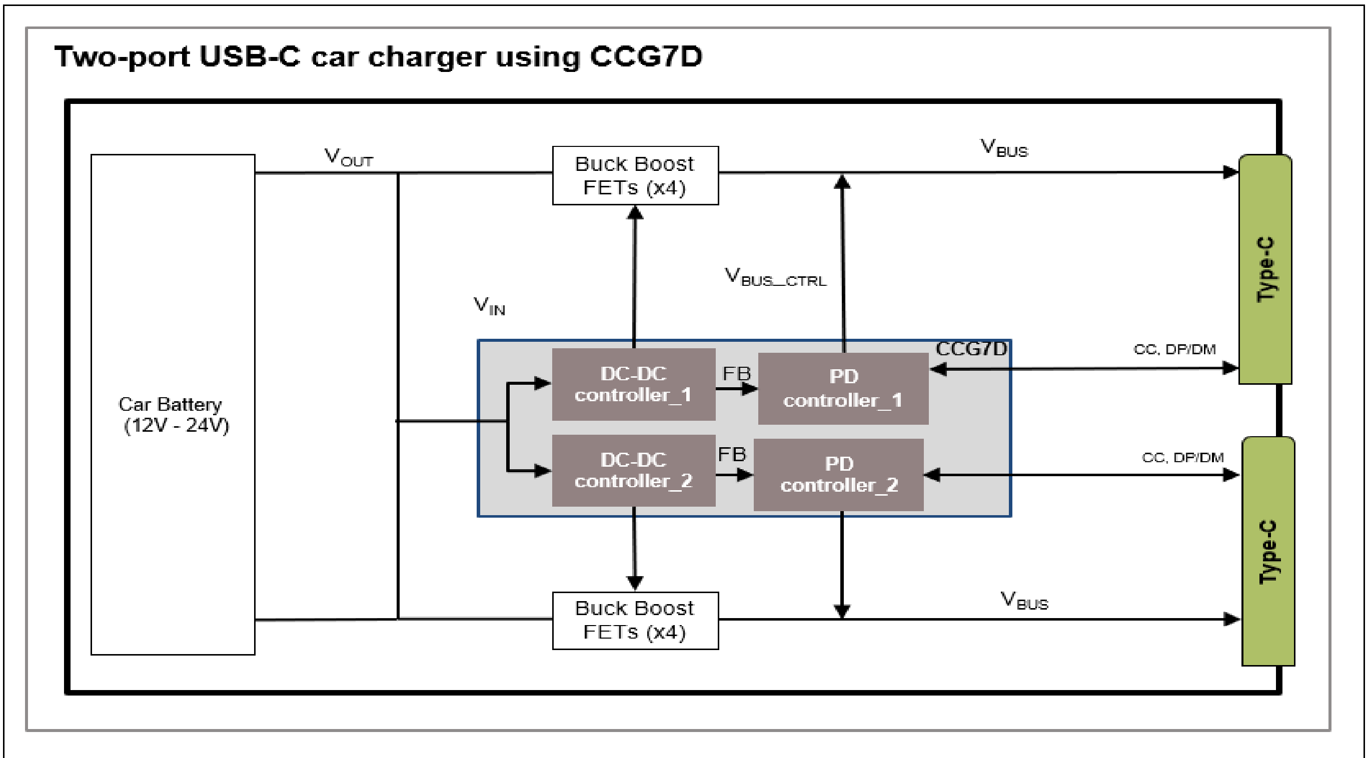


Figure 1 EZ-PD™ CCG7D consumer based dual output USB PD cigarette lighter adapter

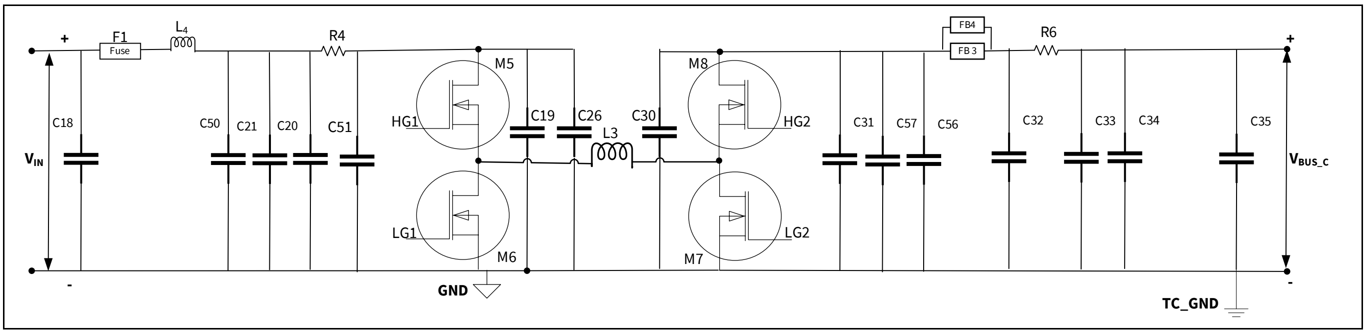


Figure 2 High-level block diagram of CLA solution board power stage

Table 2 Critical components BOM

Designator	Description	Part number	Manufacturer
U1	EZ-PD™ CCG7D consumer dual-port USB Type-C PD and buck-boost controller 68-pin QFN	CYPD7271-68LQXQES	Infineon Technologies
M5, M6, M7, M8	MOSFET N-CH 40 V 40 A 8TSDSON	IPZ40N04S5L4R8ATMA1	Infineon Technologies
F1	Fuse 15 A AC, 32 V DC, 1206	SF-1206SA1500W-2	Bourns
FB3, FB4	Ferrite bead 0805, 8.5 A 4 mΩ	BLM21SN300SH1D	Murata Electronics
L4	Inductor 0.45 µH 20% 5.8 A 5.9 mΩ	XGL3520-201MEC	CoilCraft
L3	Inductor 6.8 µH 20% 9.2 A 18.9 mΩ	XGL6060-682	CoilCraft
C18	CAP CER 10 µF 50 V X7S 1210	GCM32EC71H106KA03K	Murata Electronics
C20, C21, C57, C31, C32	CAP CER 10 µF 50 V X7R 1206	CGA5L1X7R1H106K160 AC	TDK Corporation
C19, C26, C30, C51	CAP CER 4.7 µF 50 V X7R 0805	CGA4J1X7R1H475K125AE	TDK Corporation
C50	CAP ALUM POL HY 47 µF 20% 35 V	GYC1V470MCQ1GS	Nichicon
C56	CAP ALUM POLY 220 µF 20% 25 V	GYC1E221MCQ1GS	Nichicon
C33	CAP CER 0.1 µF 50 V X7R 0603	GCM188R71H104KA57J	Murata Electronics
C34	CAP CER 1 µF 50 V X7R 0805	GCM21BR71H105KA03L	Murata Electronics
C35	CAP CER 4.7 µF 50 V X7R 1210	C1210C475K5RACAUTO	Kemet
R4	RES 0.005 Ω, 1%, 1.5 W, 1206	KRL3216E-C-R005-F-T1	Susumu
R6	RES 0.005 Ω, 1%, 1 W, 0805	KRL2012E-M-R005-F-T5	Susumu

CLA solution PCB details are shown in **Table 3**.

Table 3 Printed circuit board (PCB) details

PCB layer	Copper thickness	Details
Top layer	2 oz.	Components, power traces
2nd layer	2 oz.	High-frequency traces, control signal traces
3rd layer	2 oz.	Ground layer
Bottom layer	2 oz.	Components, power traces
Board size	-	73 mm (L) x 28 mm (W) x 24.5 mm(H)
Board thickness	-	1.6 mm

2 EZ-PD™ CCG7D consumer CLA solution demo (SD2230) kit specifications

Table 4 Test specification

Parameter	Value
Input voltage	9.0 V DC – 24 V DC
Max output power	65 W total with a max of 45 W on each port. When both the ports are connected dynamic power sharing of 65 W is enabled.
Output voltage	Fixed PDOs: 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 2.25 A PPS: 3.3 V – 11 V, 3 A; 3.3 V – 16 V, 3 A; 3.3 V – 21 V, 2.25 A with PPS power limit
Peak efficiency	See **4.1 Peak efficiency table** and **4.2 Full load efficiency table**
Protections	1. Input overvoltage protection 2. Input undervoltage protection 3. V_{BUS_C} Overvoltage protection (OVP) 4. V_{BUS_C} Undervoltage protection (UVP) 5. Overcurrent protection (OCP) 6. Short-circuit protection (SCP) 7. Overtemperature protection (OTP) 8. VBUS to CC short protection
Charging standards supported	1. USB-C PD v2.0 including programmable power supply (PPS) mode 2. Apple Charging 2.4 A 3. Qualcomm QC 2.0, 3.0, 4.0 4. Samsung AFC 5. USB BC 1.2

3 Test setup

- The CLA solution board, firmware version details, and EZ-PD™ CCG7D consumer configuration details are shown in **Table 5.**

Table 5 DUT hardware and software configurations

DUT contents	Description	Remarks
Hardware configuration		
EZ-PD™ CCG7D consumer cigarette lighter adaptor (CLA) solution demo (CY-SD2230) kit	Rev 3; A1 silicon FCCM	See **Circuit schematics, BOM, and PCB layout**
Firmware		
Firmware version	V4	CLA_ES100_v4.hex
EZ-PD™ CCG7D consumer configuration		
System clock	24 MHz	Default configuration
Gate drive strength Pull-up drive strength: LG1, LG2 – 2.9 Ω, HG1, HG2 – 3.3 Ω Pull-down drive strength: LG1, LG2 – 3.1 Ω, HG1, HG2 – 3.4 Ω	0x7	Default configuration
Spread spectrum – Triangle	15%	Default configuration (switching frequency 400 kHz)

Figure 3 EZ-PD™ CCG7D consumer CLA solution board

3.1 DUT setup

The DUT is connected to a power adapter tester (PAT) (CCPROG PAT) using a USB Type-C cable. Once a successful connection is established, the PAT UI does a PDO discovery and displays the results. The CLA solution demo kit is pre-configured with 7 PDOs:

Fixed PDOs: 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 2.25 A

PPS: 3.3 V – 11 V, 3 A; 3.3 V – 16 V, 3 A; 3.3 V – 21 V, 2.25 A (PPS power limited)

You can either choose the suitable pre-configured PDO or configure a new one using the EZ-PD™ Configuration Utility. Tests in the following sections use pre-configured PDOs.

To know more about PAT tester, visit: USBCEE: **https://www.usbcee.com/product-details/3**

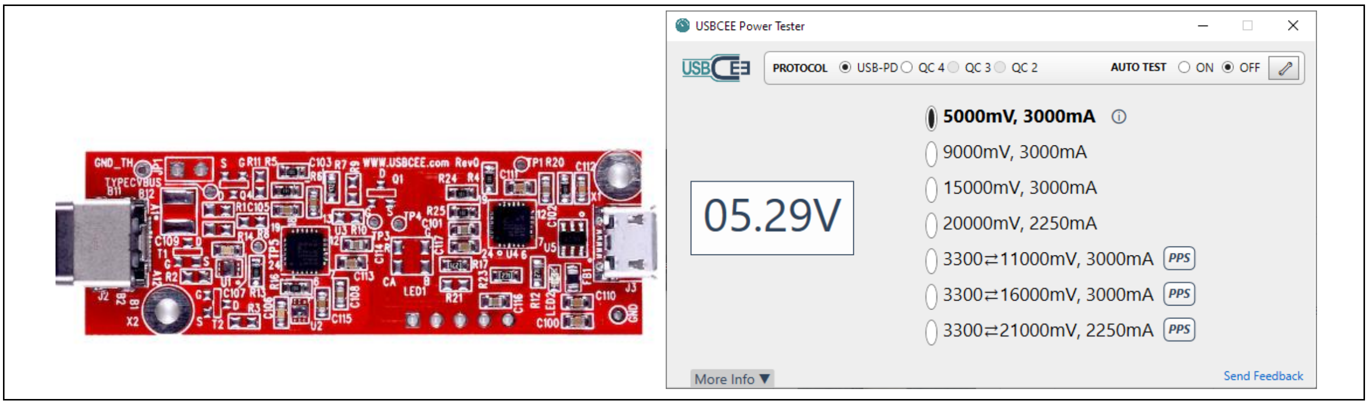


Figure 4 PAT tester and user interface

3.2 Test equipment

The test equipment used to measure the efficiency, ripple, regulation, and transient response are shown in **Table 6**.

Table 6 Test equipment details

Test setup	Description
Programmable DC source	Chroma 62024P-80-60
Oscilloscope	Tektronix MDO 3034
Digital multimeter (Port #0 I_{OUT}, Port #1 I_{OUT})	Keysight 34465 A
Data logger (Port #0 V_{BUS_C}, Port #1 V_{BUS_C}, I_{IN}, V_{IN})	Keysight 34970 A
Electronic load	Chroma 63102 A
Input current (I_{IN})measurement shunt	Murata 3020-01107-0
Thermal camera	FLIR E75
Automation software	SIVA 2.3.0 DCDC Automation Suite 2.0.0.2

4 Power management test results

4.1 Peak efficiency table

Peak efficiency results are in the (see test setup and conditions in the **Appendix – A: Efficiency measurement test setup** and full load efficiency results are in the **Table 7** and **Table 8**.

Table 7 Peak efficiency when Port #0 and Port #1 are loaded

V_{IN}	Port#0 V_{BUS_C}	Port#0 I_{OUT}	Port#1 V_{BUS_C}	Port#1 I_{OUT}	Peak efficiency (old silicon)
9.00 V	5.00 V	2.00 A	5.00 V	2.00 A	95.49 %
9.00 V	9.00 V	1.75 A	9.00 V	1.75 A	95.64 %
9.00 V	15.00 V	1.75 A	15.00 V	0.81 A	95.98 %
9.00 V	20.00 V	1.69 A	20.00 V	0.75 A	94.93 %
12.00 V	5.00 V	2.50 A	5.00 V	2.50 A	94.56 %
12.00 V	9.00 V	2.50 A	9.00 V	2.50 A	96.74 %
12.00 V	15.00 V	2.25 A	15.00 V	1.04 A	97.01 %
12.00 V	20.00 V	2.25 A	20.00 V	1.00 A	96.00 %
15.00 V	5.00 V	2.75 A	5.00 V	2.75 A	93.75 %
15.00 V	9.00 V	2.75 A	9.00 V	2.75 A	96.15 %
15.00 V	15.00 V	3.00 A	15.00 V	1.28 A	95.94 %
15.00 V	20.00 V	2.25 A	20.00 V	1.00 A	96.86 %
18.00 V	5.00 V	3.00 A	5.00 V	3.00 A	92.94 %
18.00 V	9.00 V	3.00 A	9.00 V	3.00 A	95.56 %
18.00 V	15.00 V	3.00 A	15.00 V	1.28 A	97.14 %
18.00 V	20.00 V	2.25 A	20.00 V	1.00 A	95.14 %
24.00 V	5.00 V	3.00 A	5.00 V	3.00 A	91.48 %
24.00 V	9.00 V	3.00 A	9.00 V	3.00 A	94.42 %
24.00 V	15.00 V	3.00 A	15.00 V	1.28 A	95.98 %
24.00 V	20.00 V	2.25 A	20.00 V	1.00 A	96.86 %

4.2 Full load efficiency table

Table 8 Full load efficiency when Port #0 and Port #1 are loaded

V_{IN}	Port #0 V_{BUS_C}	Port #0 I_{OUT}	Port #1 V_{BUS_C}	Port #1 I_{OUT}	Efficiency
9.0 V	5.0 V	3.00 A	5.0 V	3.00 A	95.22 %
12.0 V	5.0 V	3.00 A	5.0 V	3.00 A	94.49 %
15.0 V	5.0 V	3.00 A	5.0 V	3.00 A	93.75 %
18.0 V	5.0 V	3.00 A	5.0 V	3.00 A	92.94 %
24.0 V	5.0 V	3.00 A	5.0 V	3.00 A	91.48 %
9.0 V	9.0 V	3.00 A	9.0 V	3.00 A	94.93 %
12.0 V	9.0 V	3.00 A	9.0 V	3.00 A	96.59 %
15.0 V	9.0 V	3.00 A	9.0 V	3.00 A	96.15 %
18.0 V	9.0 V	3.00 A	9.0 V	3.00 A	95.56 %
24.0 V	9.0 V	3.00 A	9.0 V	3.00 A	94.42 %
9.0 V	15.0 V	3.00 A	15.0 V	1.34 A	95.47 %
12.0 V	15.0 V	3.00 A	15.0 V	1.34 A	96.88 %
15.0 V	15.0 V	3.00 A	15.0 V	1.34 A	95.94 %
18.0 V	15.0 V	3.00 A	15.0 V	1.34 A	97.22 %
24.0 V	15.0 V	3.00 A	15.0 V	1.34 A	95.98 %
9.0 V	20.0 V	2.25 A	20.0 V	1.00 A	94.65 %
12.0 V	20.0 V	2.25 A	20.0 V	1.00 A	96.00 %
15.0 V	20.0 V	2.25 A	20.0 V	1.00 A	96.86 %
18.0 V	20.0 V	2.25 A	20.0 V	1.00 A	95.14 %
24.0 V	20.0 V	2.25 A	20.0 V	1.00 A	96.86 %

Note:

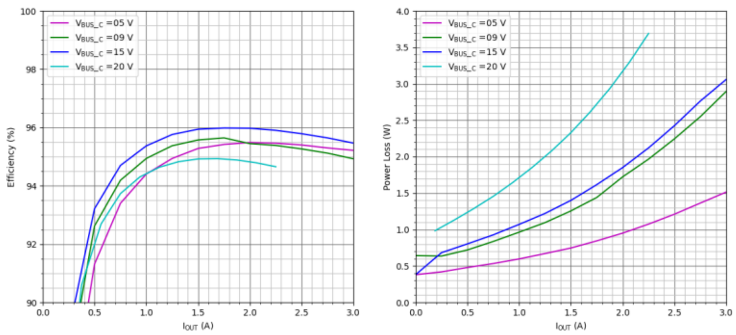
1. *Peak efficiency when both ports are loaded: 97.22% (At V_{IN}: 18 V, Port #0 V_{BUS_C}: 15 V, I_{OUT}: 3.0 A, Port #1 V_{BUS_C}: 15 V, I_{OUT}: 1.34 A)*
2. *For efficiency calculations V_{BUS_C} is measured across the output capacitors (C74, C96) with 30 minutes warmup.*
3. *Load sharing is disabled using the EZ-PD™ Configuration Utility.*
4. *Efficiency, ripple, Voltage regulation are tested for the following output combinations (also tested Port #1 loaded with 45 W and Port #0 loaded with 20 W):*
   a. *Port #0 V_{BUS_C} = 5 V, I_{OUT} = 0 A to 3 A; Port #1 V_{BUS_C} = 5 V, I_{OUT} = 0 A to 3 A;*
   b. *Port #0 V_{BUS_C} = 9 V, I_{OUT} = 0 A to 3 A; Port #1 V_{BUS_C} = 9 V, I_{OUT} = 0 A to 3 A;*
   c. *Port #0 V_{BUS_C} = 15 V, I_{OUT} = 0 A to 3 A; Port #1 V_{BUS_C} = 15 V, I_{OUT} = 0 A to 1.34 A;*
   d. *Port #0 V_{BUS_C} = 20 V, I_{OUT} = 0 A to 2.25 A; Port #1 V_{BUS_C} = 20 V, I_{OUT} = 0 A to 1 A;*

4.3 Efficiency graphs

Efficiency measurements are taken at 9 V, 12 V, 15 V, 18 V and 24 V DC input to the DUT; V_{BUS_C} contract voltages are 5 V, 9 V, 12 V, 15 V, and 20 V. Both ports are loaded from 0 A to the maximum rated output current of 3 A, with a maximum output power of 45 W per port. Maximum of 65 W output power on both ports together.

- Efficiency, losses at 9-V DC input, Port #0 and Port #1 V_{BUS_C} 5 V, 09 V, 15 V, 20 V are shown in **Figure 5**.
- Efficiency, losses at 12-V DC input, Port #0 and Port #1 V_{BUS_C} 5 V, 09 V, 15 V, 20 V are shown in **Figure 6**.
- Efficiency, losses at 15-V DC input, Port #0 and Port #1 V_{BUS_C} 5 V, 09 V, 15 V, 20 V are shown in **Figure 7**.
- Efficiency, losses at 18-V DC input, Port #0 and Port #1 V_{BUS_C} 5 V, 09 V, 15 V, 20 V are shown in **Figure 8**.
- Efficiency, losses at 24-V DC input, Port #0 and Port #1 V_{BUS_C} 5 V, 09 V, 15 V, 20 V are shown in **Figure 9**.

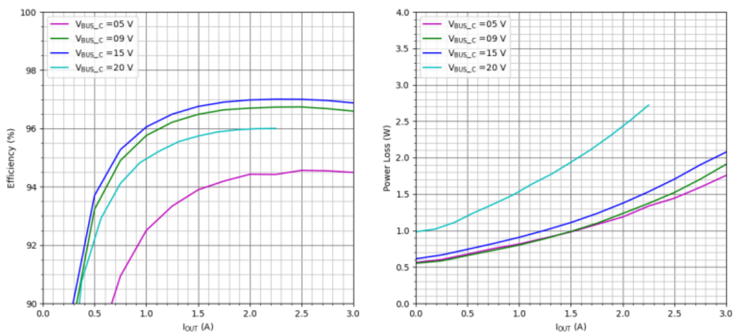
4.3.1 Efficiency and power losses at 9-V DC input



Efficiency at 9-V DC input   Power loss at 9-V DC input

Figure 5 Efficiency and power losses at 9-V DC input

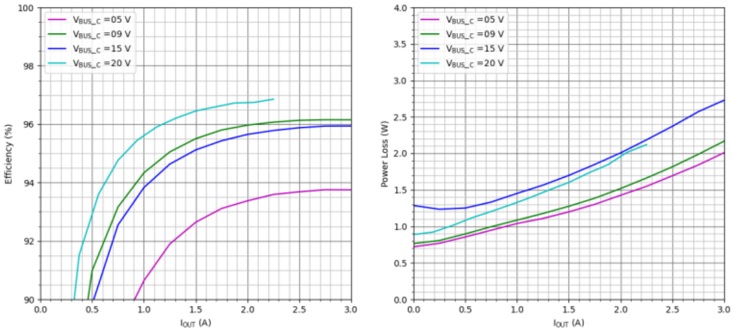
4.3.2 Efficiency and power losses at 12-V DC input



Efficiency at 12-V DC input   Power loss at 12-V DC input

Figure 6 Efficiency and power losses at 12-V DC input

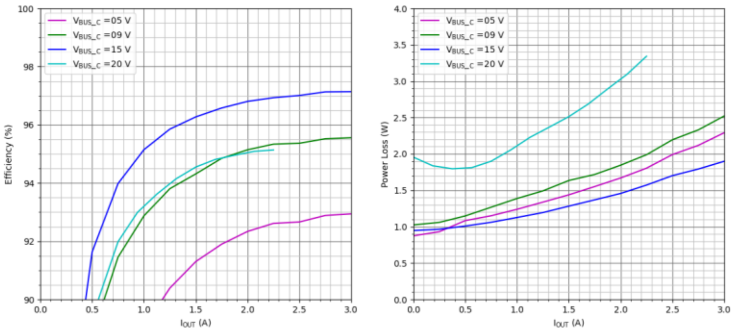
4.3.3 Efficiency and power losses at 15-V DC input



Efficiency at 15-V DC input   Power loss at 15-V DC input

Figure 7 Efficiency and power losses at 15-V DC input

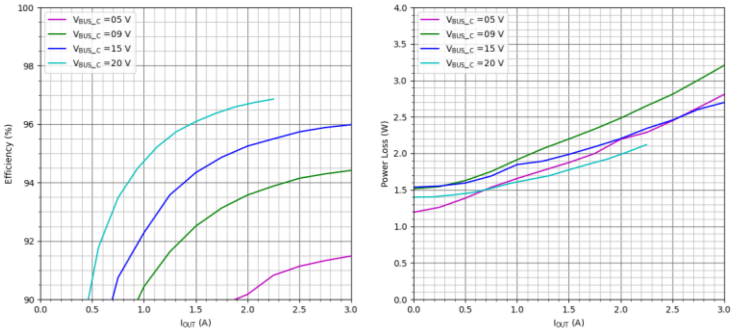
4.3.4 Efficiency and power losses at 18-V DC input



Efficiency at 18-V DC input   Power loss at 18-V DC input

Figure 8 Efficiency and power losses at 18-V DC input

4.3.5 Efficiency and power losses at 24-V DC input



Efficiency at 24-V DC input   Power loss at 24-V DC input

Figure 9 Efficiency and power losses at 24-V DC input

4.4 Output voltage and current regulation

Output voltage regulation is measured in the constant voltage (CV) mode.

4.4.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A and 3 A load currents are shown in **Figure 10** to **Figure 14**. Voltage regulation is measured for the following load combinations:

1. Port #0 V_{BUS_C} = 5 V, I_{OUT} = 0 A to 3 A; Port #1 V_{BUS_C} = 5 V, I_{OUT} = 0 A to 3 A;
2. Port #0 V_{BUS_C} = 9 V, I_{OUT} = 0 A to 3 A; Port #1 V_{BUS_C} = 9 V, I_{OUT} = 0 A to 3 A;
3. Port #0 V_{BUS_C} = 15 V, I_{OUT} = 0 A to 3 A; Port #1 V_{BUS_C} = 15 V, I_{OUT} = 0 A to 1.34 A;
4. Port #0 V_{BUS_C} = 20 V, I_{OUT} = 0 A to 1 A; Port #1 V_{BUS_C} = 20 V, I_{OUT} = 0 A to 2.25 A;

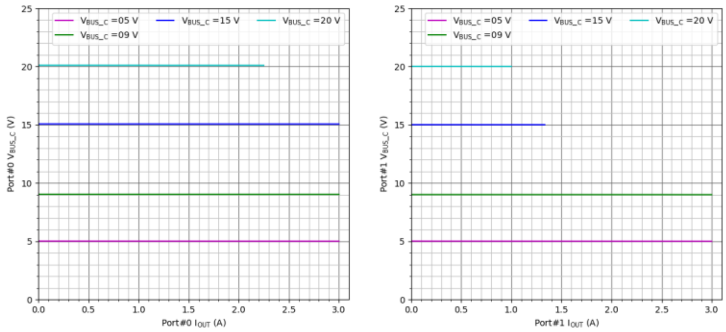


Figure 10 CV regulation V_{IN} = 9 V, Port #0 and Port #1

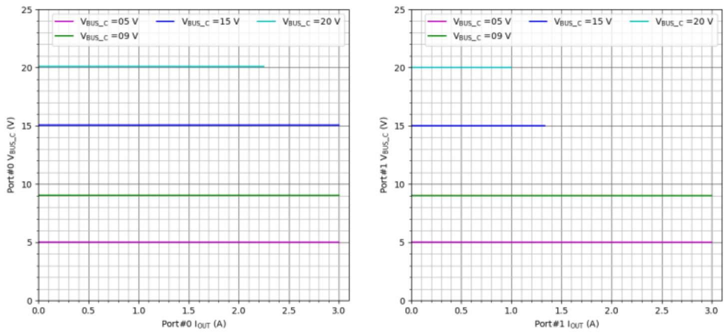


Figure 11 CV regulation V_{IN} = 12 V, Port #0 and Port #1

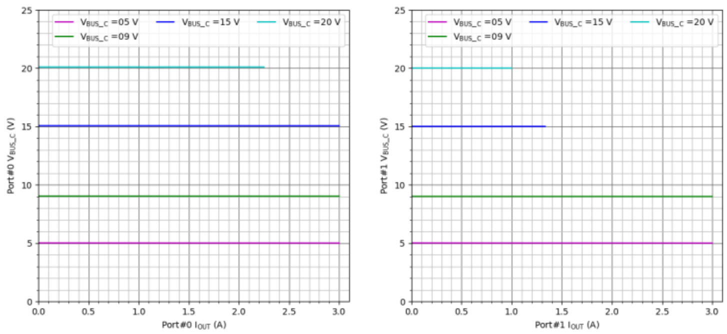


Figure 12 CV regulation V_{IN} = 15 V, Port #0 and Port #1

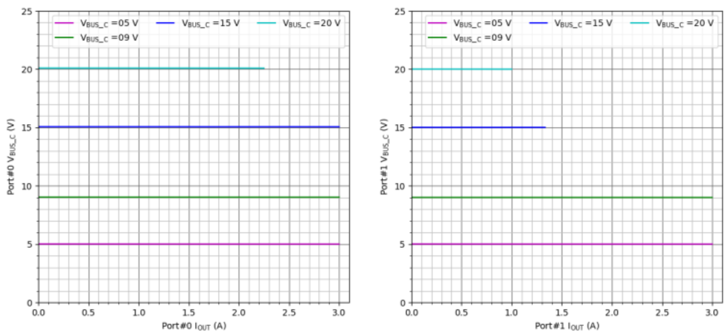


Figure 13 CV regulation V_{IN} = 18 V, Port #0 and Port #1

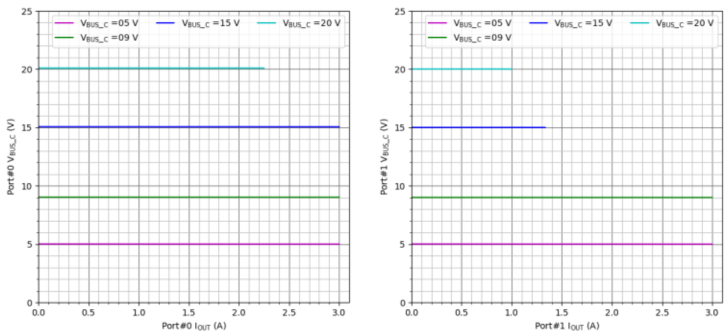


Figure 14 CV regulation V_{IN} = 24 V, Port #0 and Port #1

4.4.2 Output current regulation (CC mode)

The output constant current regulation measured at 1 A load current is shown in **Figure 15** to **Figure 19**.

4.4.3 CV-CC regulation curve at 9 V, 12 V, 15 V, 18 V, and 24 V input

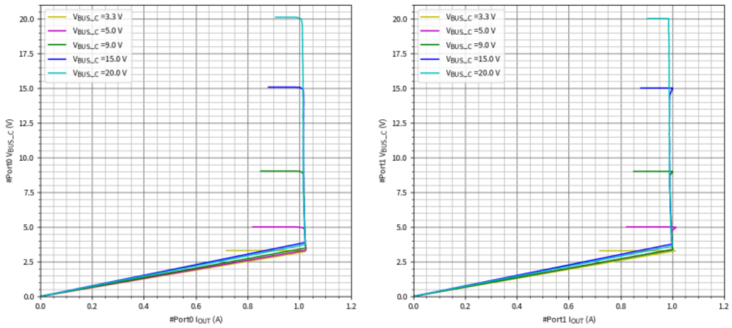


Figure 15 CV-CC regulation curve at 9 V input, Port #0 and Port #1

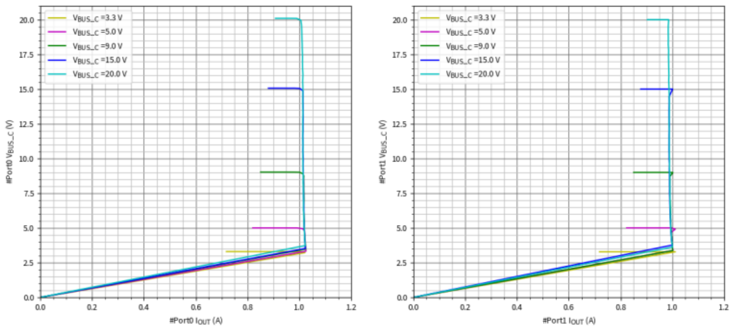


Figure 16 CV-CC regulation curve at 12 V input, Port #0 and Port #1

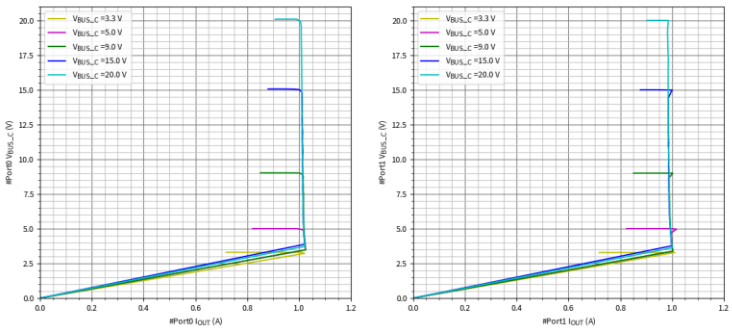


Figure 17 CV-CC regulation curve at 15 V input, Port #0 and Port #1

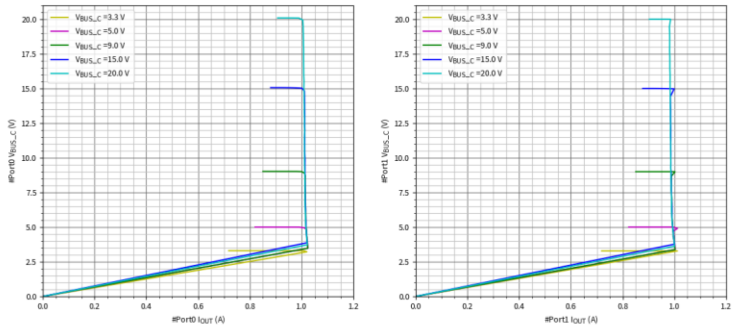


Figure 18 CV-CC regulation curve at 18 V input, Port #0 and Port #1

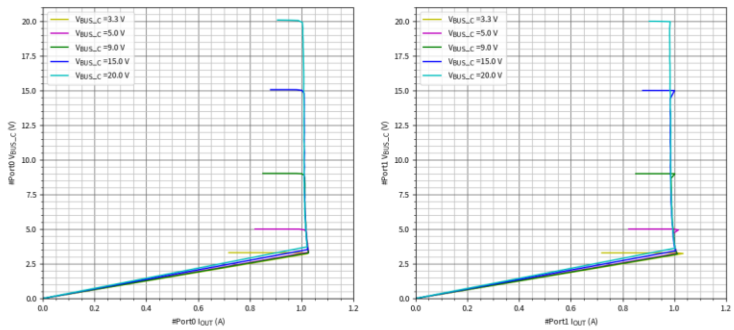


Figure 19 CV-CC regulation curve at 24 V input, Port #0 and Port #1

4.5 Output voltage regulation

Output voltage regulation measured on each Port at V_{IN}: 9 V, 12 V, 15 V, 18 V, 24 V when Port #0 V_{BUS_C}: 5 V, 9 V, 15 V, 20 V and Port #1 V_{BUS_C}: 5 V, 9 V, 15 V, 20 V are shown in **Table 9** to **Table 13**.

Table 9 Regulation: V_{IN} 09 V

V_{IN} (V)	Port #0 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 I_{OUT} (A)	Port #1 V_{BUS_C} (V)
09	0	5.009559	0	5.007784
09	3	4.999869	3	4.996173
09	0	9.029373	0	9.004355
09	3	9.021657	3	8.997255
09	0	15.07608	0	15.00908
09	3	15.06952	1.34	15.00543
09	0	20.11308	0	20.01607
09	2.25	20.10391	1	20.01096

Table 10 Regulation: V_{IN} 12 V

V_{IN} (V)	Port #0 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 I_{OUT} (A)	Port #1 V_{BUS_C} (V)
12	0	5.009371	0	5.007857
12	3	4.99988	3	4.995881
12	0	9.027577	0	9.004418
12	3	9.020895	3	8.998476
12	0	15.07192	0	15.00731
12	3	15.06733	1.34	15.00397
12	0	20.1061	0	20.00784
12	2.25	20.10048	1	20.00794

Table 11 Regulation: V_{IN}15 V

V_{IN} (V)	Port #0 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 I_{OUT} (A)	Port #1 V_{BUS_C} (V)
15	0	5.009945	0	5.008598
15	3	4.999838	3	4.997363
15	0	9.026543	0	9.002559
15	3	9.019788	3	8.995156
15	0	15.07035	0	15.01044
15	3	15.0642	1.34	15.00741
15	0	20.1011	0	20.00867
15	2.25	20.0987	1	20.0069

Table 12 Regulation: V_{IN} 18 V

V_{IN} (V)	Port #0 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 I_{OUT} (A)	Port #1 V_{BUS_C} (V)
18	0	5.009726	0	5.008317
18	3	4.999431	3	4.998303

V_{IN} (V)	Port #0 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 I_{OUT} (A)	Port #1 V_{BUS_C} (V)
18	0	9.026084	0	9.002078
18	3	9.019015	3	8.995458
18	0	15.07014	0	15.01096
18	3	15.06639	1.34	15.00898
18	0	20.10058	0	20.00784
18	2.25	20.09037	1	20.00284

Table 13 Regulation: V_{IN} 24 V

V_{IN} (V)	Port #0 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 I_{OUT} (A)	Port #1 V_{BUS_C} (V)
24	0	5.010509	0	5.009329
24	3	4.99966	3	4.997248
24	0	9.023839	0	9.001431
24	3	9.017198	3	8.995145
24	0	15.06837	0	15.00668
24	3	15.0615	1.34	15.00231
24	0	20.09964	0	20.01534
24	2.25	20.09891	1	20.00919

4.6 Output voltage cross regulation

Output voltage cross regulation measured at V_{IN}: 9 V_{DC}, 12 V_{DC}, 15 V_{DC}, 18 V_{DC} and 24 V_{DC} Port #0, Port #1 V_{BUS_C}: 5 V, 9 V, 15 V, 20 V are shown in **Table 14** to **Table 18**.

Table 14 Cross regulation: V_{IN} 9 V_{DC}

V_{IN} (V_{DC})	Port #0 I_{OUT} (A)	Port #1 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 V_{BUS_C} (V)
9	0	3	5.009	4.997
9	3	0	5.000	5.007
9	0	3	9.029	9.000
9	3	0	9.023	9.005
9	0	3	15.080	15.007
9	3	0	15.074	15.012
9	0	2.25	20.119	20.014
9	2.25	0	20.114	20.015

Table 15 Cross regulation: V_{IN} 12 V_{DC}

V_{IN} (V_{DC})	Port #0 I_{OUT} (A)	Port #1 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 V_{BUS_C} (V)
12	0	3	5.009	4.996
12	3	0	5.000	5.007
12	0	3	9.029	9.000
12	3	0	9.023	9.005
12	0	3	15.076	15.005

V_{IN} (V_{DC})	Port #0 I_{OUT} (A)	Port #1 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 V_{BUS_C} (V)
12	3	0	15.071	15.011
12	0	2.25	20.115	20.013
12	2.25	0	20.109	20.014

Table 16 Cross regulation: V_{IN} 15 V_{DC}

V_{IN} (V_{DC})	Port #0 I_{OUT} (A)	Port #1 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 V_{BUS_C} (V)
15	0	3	5.009	4.998
15	3	0	5.001	5.008
15	0	3	9.027	8.997
15	3	0	9.022	9.004
15	0	3	15.069	15.008
15	3	0	15.065	15.011
15	0	2.25	20.110	20.008
15	2.25	0	20.107	20.014

Table 17 Cross regulation: V_{IN} 18 V_{DC}

V_{IN} (V_{DC})	Port #0 I_{OUT} (A)	Port #1 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 V_{BUS_C} (V)
18	0	3	5.009	4.999
18	3	0	5.000	5.008
18	0	3	9.027	8.998
18	3	0	9.021	9.003
18	0	3	15.073	15.009
18	3	0	15.069	15.012
18	0	2.25	20.102	20.007
18	2.25	0	20.100	20.009

Table 18 Cross regulation: V_{IN} 24 V_{DC}

V_{IN} (V_{DC})	Port #0 I_{OUT} (A)	Port #1 I_{OUT} (A)	Port #0 V_{BUS_C} (V)	Port #1 V_{BUS_C} (V)
24	0	3	5.010	4.998
24	3	0	5.000	5.009
24	0	3	9.026	8.997
24	3	0	9.020	9.003
24	0	3	15.071	15.001
24	3	0	15.062	15.006
24	0	2.25	20.106	20.014
24	2.25	0	20.102	20.017

4.7 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors C74 and C96 of Port #0 and Port #1 using a short ground loop connected to the probe.

4.7.1 Output voltage ripple peak-peak (mV)

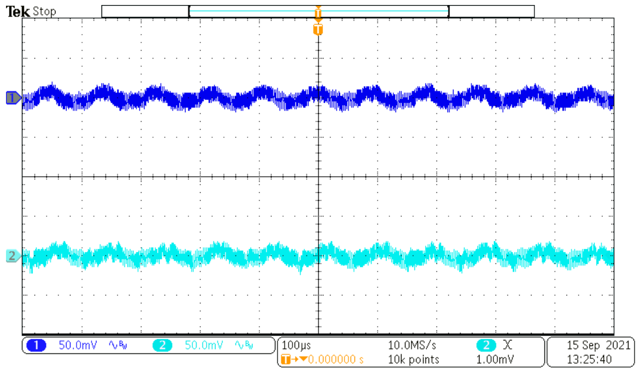
Port #0 and Port #1 output voltage peak-to-peak ripple measured by loading both ports at a time and are tabulated in **Table 19**.

Table 19 Peak-to-peak (mV) ripple

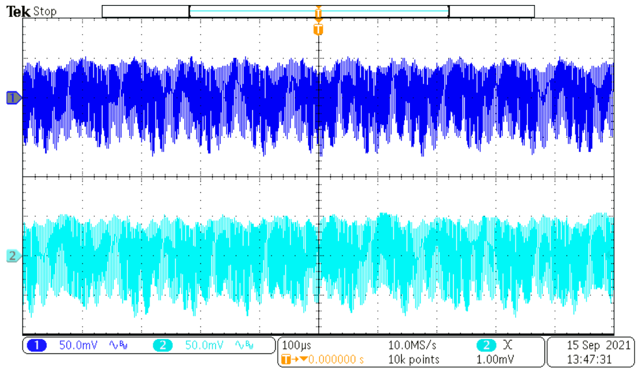
Port # 0; V_{BUS_C} ripple peak - peak (mV)						Port # 1; V_{BUS_C} ripple peak - peak (mV)					
V_{BUS_C} - I_{OUT}	V_{IN} 9 V	V_{IN} 12 V	V_{IN} 15 V	V_{IN} 18 V	V_{IN} 24 V	V_{BUS_C} - I_{OUT}	V_{IN} 9 V	V_{IN} 12 V	V_{IN} 15 V	V_{IN} 18 V	V_{IN} 24 V
5.0 V – 0 A	24	28	26	24	32	5.0 V – 0 A	24	26	26	22	36
5.0 V – 3 A	38	36	58	70	58	5.0 V – 3 A	42	44	64	70	64
9.0 V – 0 A	40	42	40	38	50	9.0 V – 0 A	44	46	40	40	50
9.0 V – 3 A	126	62	48	68	70	9.0 V – 3 A	132	68	54	74	74
15.0 V – 0 A	26	26	68	86	64	15.0 V – 0 A	30	30	70	92	64
15.0 V – 3 A	172	108	154	112	80	15.0 V – 1.34 A	108	64	114	112	88
20.0 V – 0 A	32	44	44	48	124	20.0 V – 0 A	36	44	44	48	132
20.0 V – 2.25 A	216	164	120	152	148	20.0 V – 1 A	132	112	88	100	156

4.7.2 Output voltage ripple peak-to-peak measurement graphs

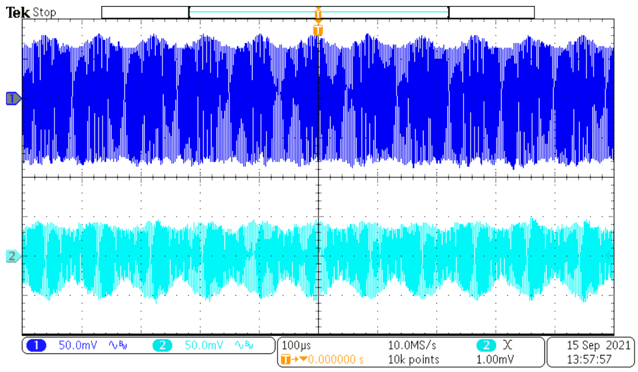
Port #0 and Port #1 output voltage peak-to-peak ripple waveforms at full load are shown in **Figure 20** to **Figure 24**.



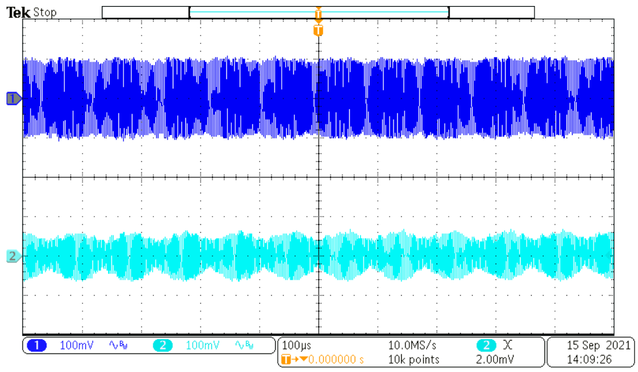
V_{IN}: 9 V; Port #0 V_{BUS_C}: 5 V/3 A;
Port #1 V_{BUS_C}: 5 V/ 3 A;



V_{IN}: 9 V; Port #0 V_{BUS_C}: 9 V/3 A;
Port #1 V_{BUS_C}: 9 V/3 A;

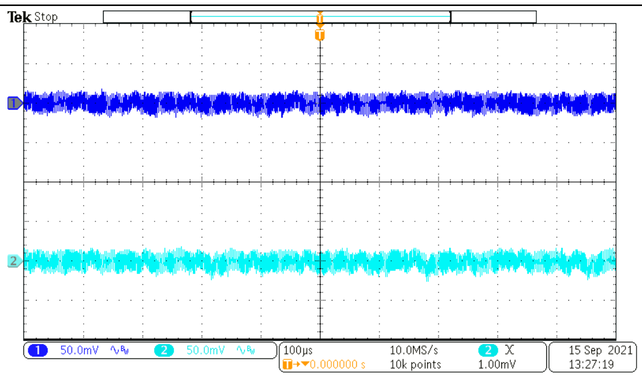


V_{IN}: 9 V; Port #0 V_{BUS_C}: 15 V/3 A;
Port #1 V_{BUS_C}: 15 V/1.34 A;

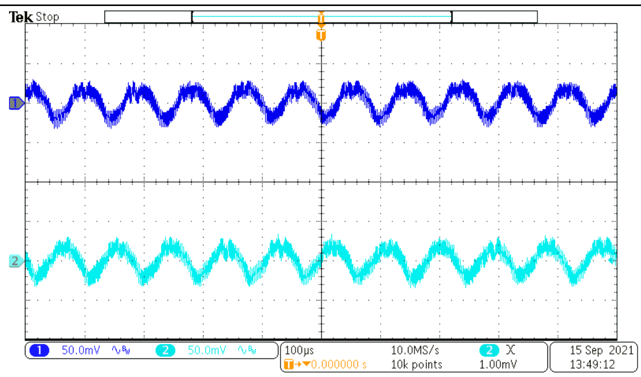


V_{IN}: 9 V; Port #0 V_{BUS_C}: 20 V/2.25 A;
Port #1 V_{BUS_C}: 20 V/1.0 A;

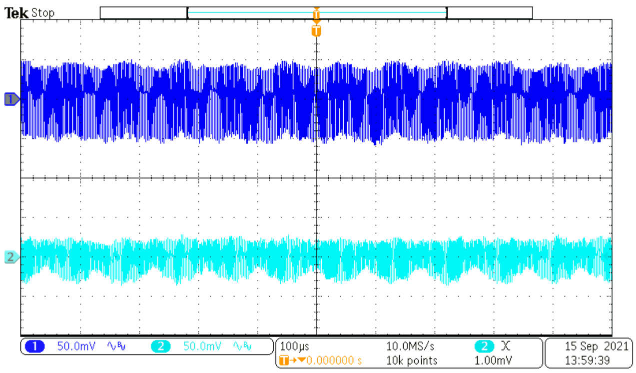
Figure 20 Ripple measurement – Input voltage: 9 V DC (CH1: Port #0 V_{BUS_C}, CH2: Port #1 V_{BUS_C})



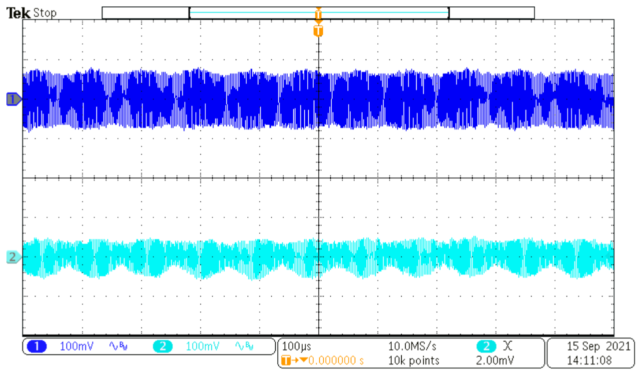
V_{IN}:12 V; Port #0 V_{BUS_C}: 5 V/3 A;
Port #1 V_{BUS_C}: 5 V/ 3 A;



V_{IN}: 12 V; Port #0 V_{BUS_C}: 9 V/3 A;
Port #1 V_{BUS_C}:9 V/3 A;

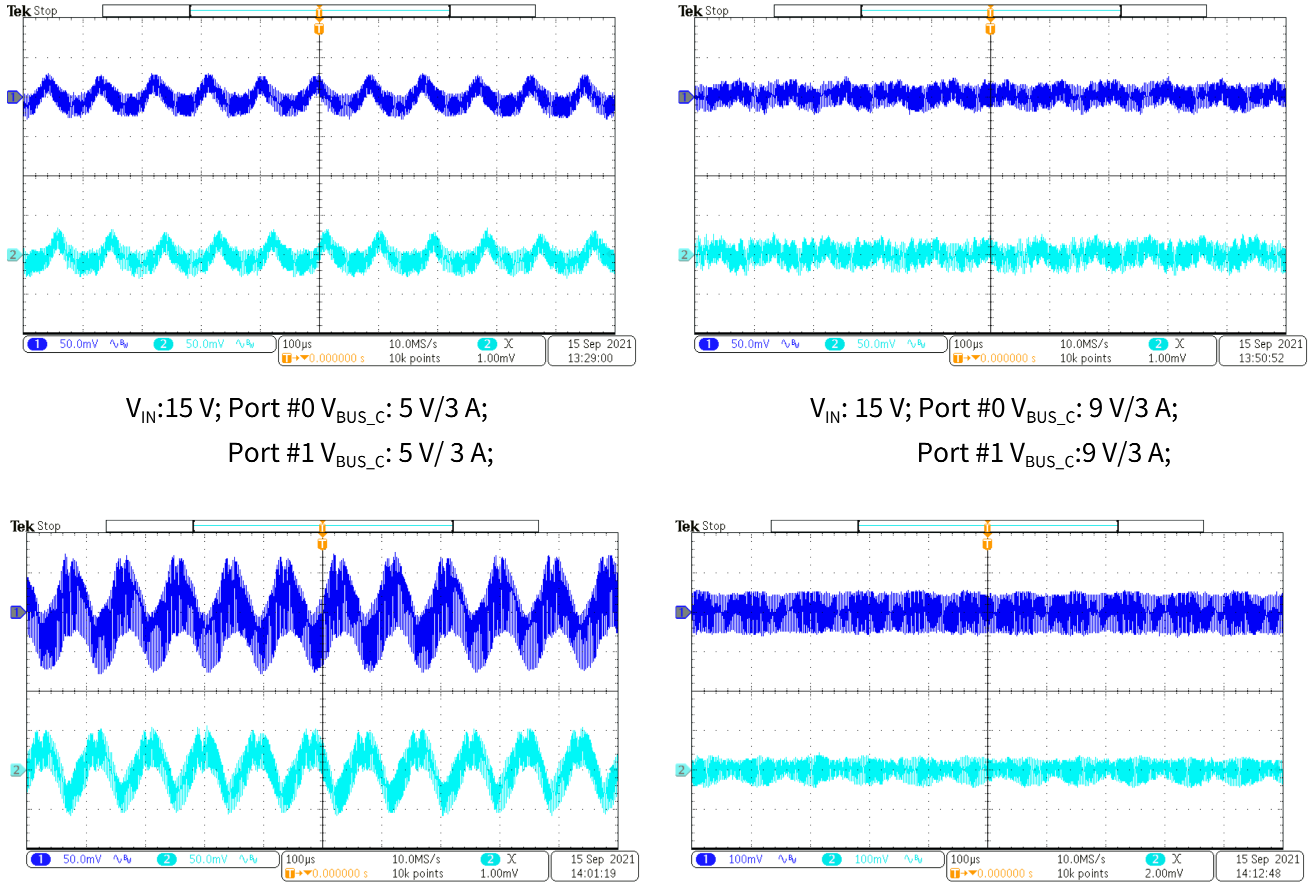


V_{IN}: 12 V; Port #0 V_{BUS_C}: 15 V/ 3 A;
Port #1 V_{BUS_C}: 15 V/1.34 A;



V_{IN}: 12 V; Port #0 V_{BUS_C}: 20 V/2.25 A;
Port #1 V_{BUS_C}: 20 V/1.0 A;

Figure 21 Ripple measurement – Input voltage: 12 VDC (CH1: Port #0 V_{BUS_C}, CH2: Port #1 V_{BUS_C})



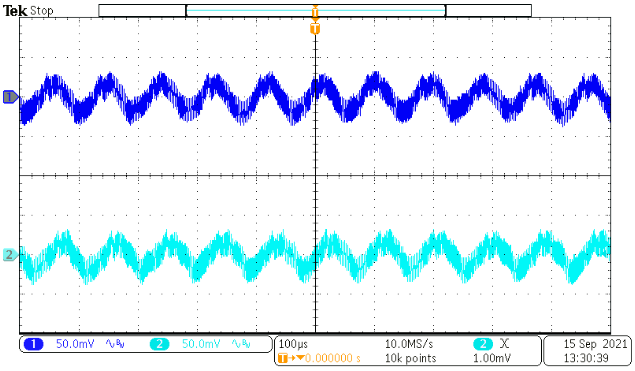
V_{IN}:15 V; Port #0 V_{BUS_C}: 5 V/3 A; Port #1 V_{BUS_C}: 5 V/ 3 A;

V_{IN}: 15 V; Port #0 V_{BUS_C}: 9 V/3 A; Port #1 V_{BUS_C}:9 V/3 A;

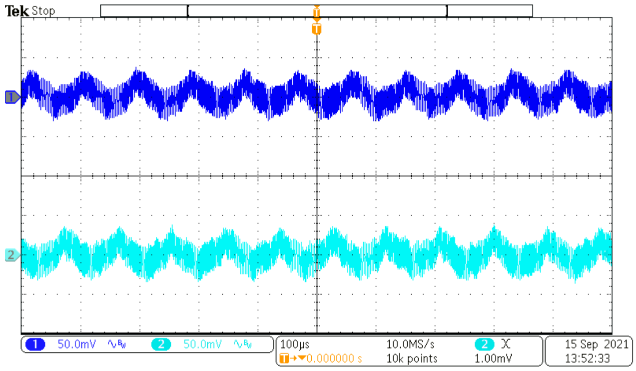
V_{IN}: 15 V; Port #0 V_{BUS_C}: 15 V/3 A; Port #1 V_{BUS_C}: 15 V/1.34 A;

V_{IN}: 15 V; Port #0 V_{BUS_C}: 20 V/2.25 A; Port #1 V_{BUS_C}: 20 V/1.0 A;

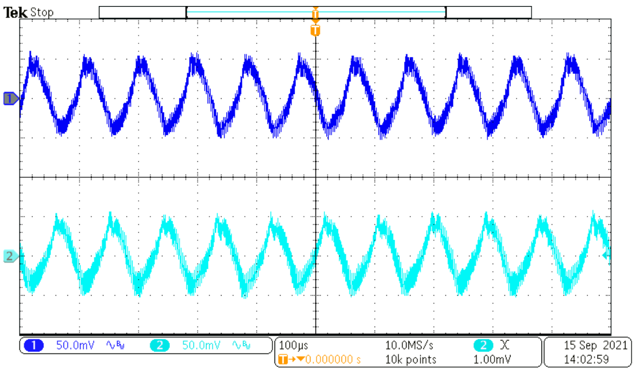
Figure 22 Ripple measurement – Input voltage: 15 Vdc (CH1: Port #0 V_{BUS_C}, CH2: Port #1 V_{BUS_C})



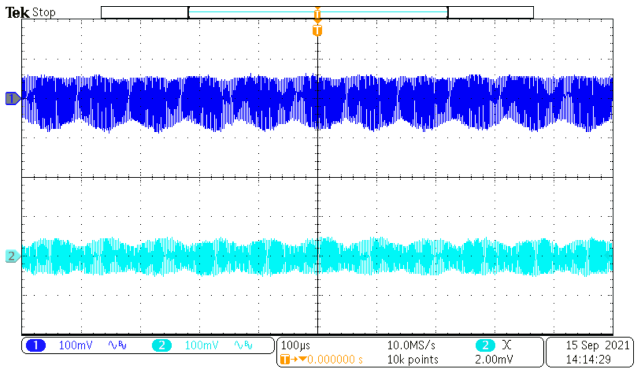
V_{IN}:18 V; Port #0 V_{BUS_C}: 05 V/3 A;
Port #1 V_{BUS_C}: 05 V/ 3 A;



V_{IN}: 18 V; Port #0 V_{BUS_C}: 09 V/3 A
Port #1 V_{BUS_C}:0 9 V/3 A;

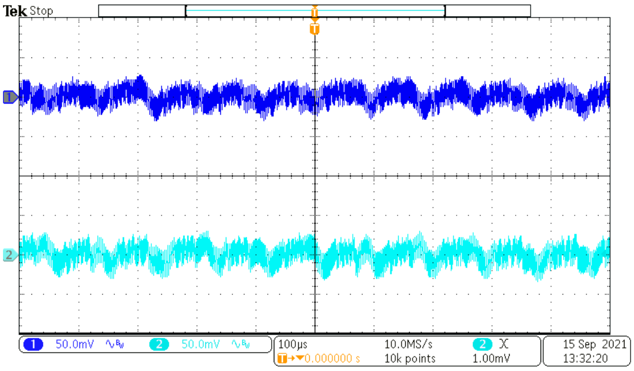


V_{IN}: 18 V; Port #0 V_{BUS_C}: 15 V/3 A;
Port #1 V_{BUS_C}: 15 V/1.34 A;

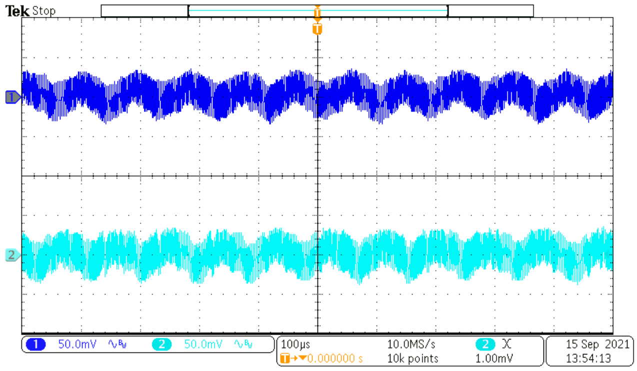


V_{IN}: 18 V; Port #0 V_{BUS_C}: 20 V/2.25 A;
Port #1 V_{BUS_C}: 20 V/1.0 A;

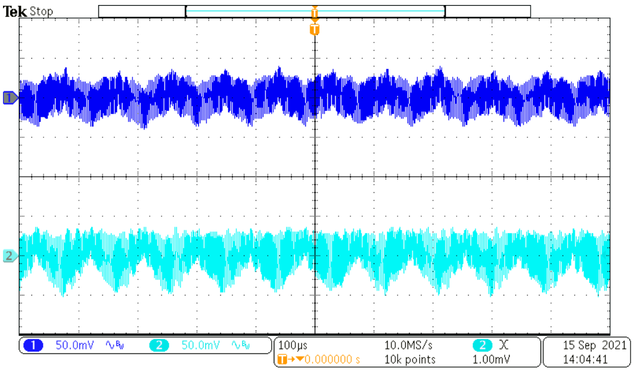
Figure 23 Ripple measurement – Input voltage: 18 Vdc (CH1: Port #0 V_{BUS_C}, CH2: Port #1 V_{BUS_C})



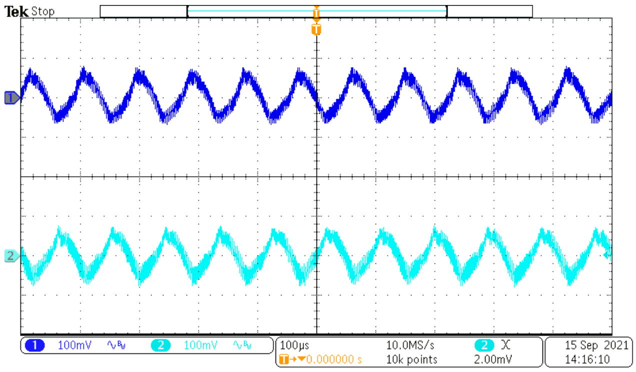
V_{IN}: 24 V; Port #0 V_{BUS_C}: 5 V/ 3 A;
Port #1 V_{BUS_C}: 5 V/ 3 A;



V_{IN}: 24 V; Port #0 V_{BUS_C}: 9 V/ 3 A
Port #1 V_{BUS_C}: 9 V/ 3 A;



V_{IN}: 24 V; Port #0 V_{BUS_C}: 15 V/3 A;
Port #1 V_{BUS_C}: 15 V/1.34 A;

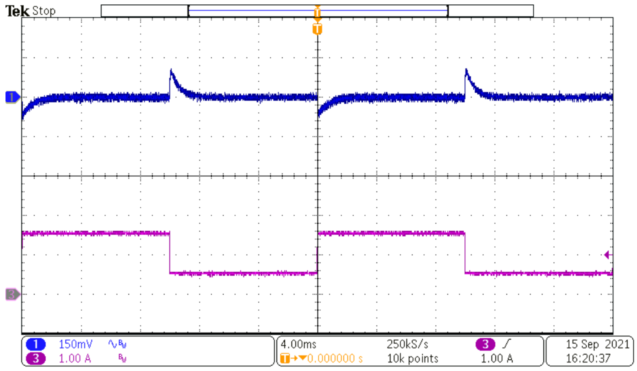


V_{IN}: 24 V; Port #0 V_{BUS_C}: 20 V/2.25 A;
Port #1 V_{BUS_C}: 20 V/1 A;

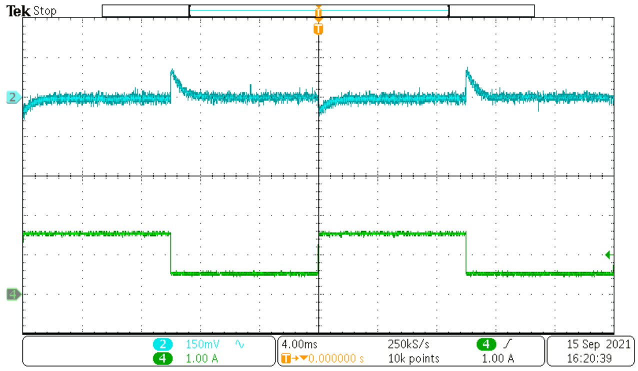
Figure 24 Ripple measurement – Input voltage: 24 V DC (CH1: Port #0 V_{BUS_C}, CH2: Port #1 V_{BUS_C})

4.8 Output dynamic response waveforms

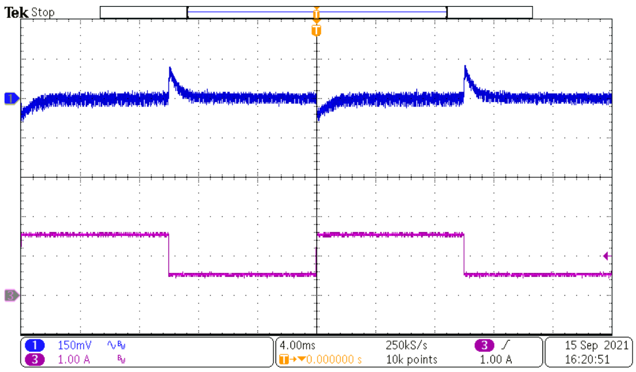
- V_{IN}:12 V, output voltage response when the output current is from 0.5 A – 1.5 A – 0.5 A is shown in **Figure 25**.
- V_{IN}:24 V, output voltage response when the output current is from 0.5 A – 1.5 A – 0.5 A is shown in **Figure 26**.



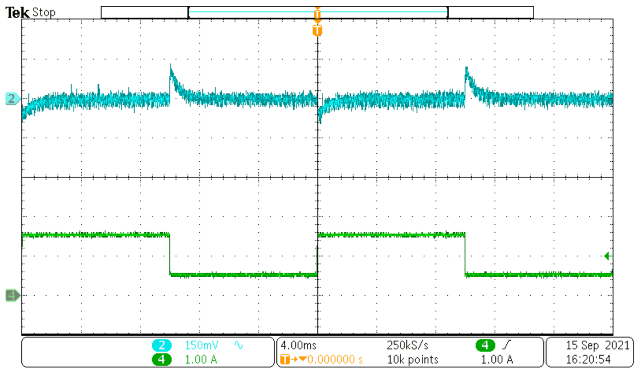
V_{BUS_C}: 5 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT})



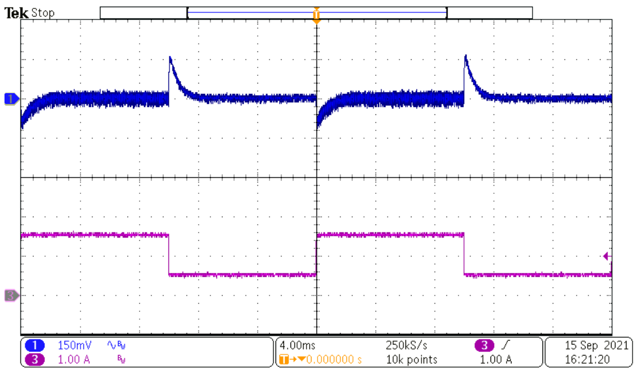
V_{BUS_C}: 5 V; (CH2: Port #1 V_{BUS_C}, CH4: Port #1 I_{OUT})



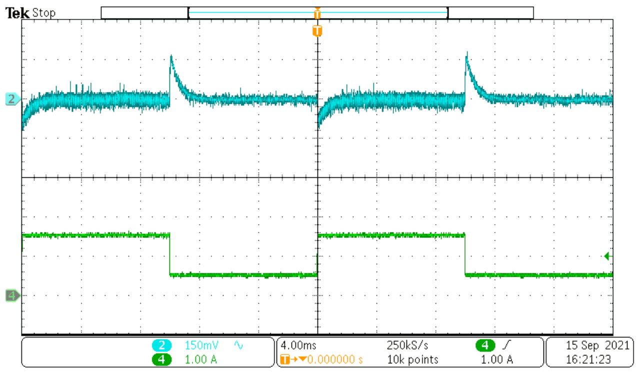
V_{BUS_C}: 9 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT})



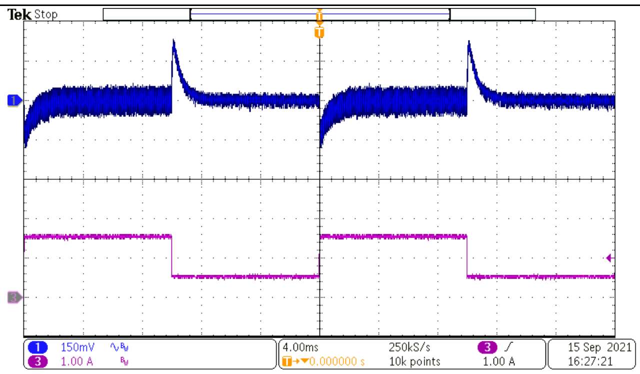
V_{BUS_C}: 9 V; (CH2: Port #1 V_{BUS_C}, CH4: Port #1 I_{OUT})



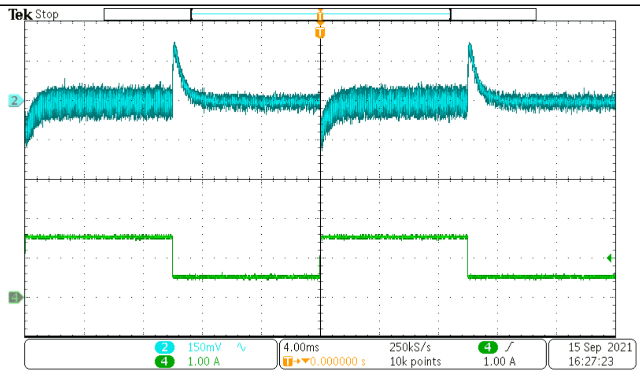
V_{BUS_C}: 15 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT})



V_{BUS_C}: 15 V; (CH2: Port #1 V_{BUS_C}, CH4: Port #1 I_{OUT})

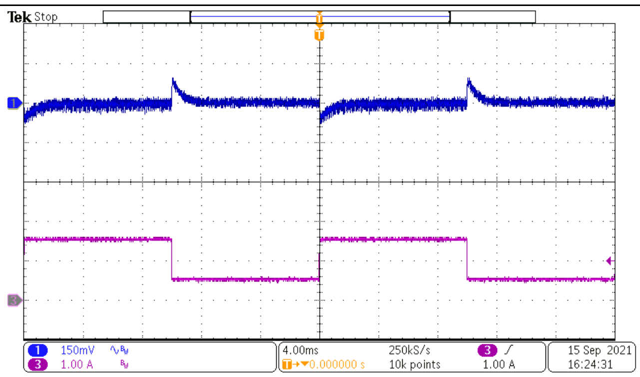


V_{BUS_C}: 20 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT})

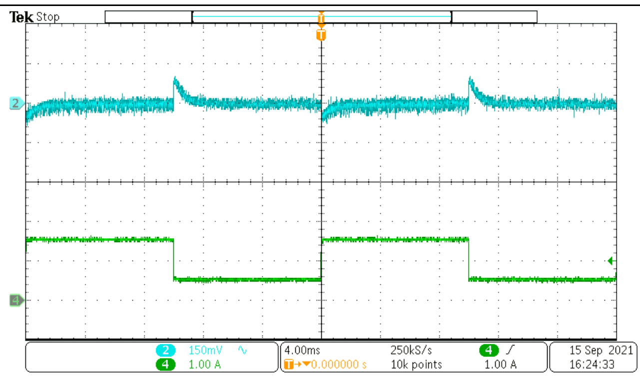


V_{BUS_C}: 20 V; (CH2: Port #1 V_{BUS_C}, CH4: Port #1 I_{OUT})

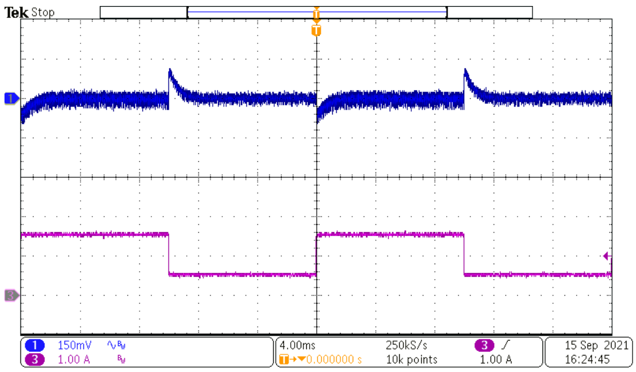
Figure 25 Output dynamic response waveforms - Input 12 V; load transition 0.5 A to 1.5 A to 0.5 A



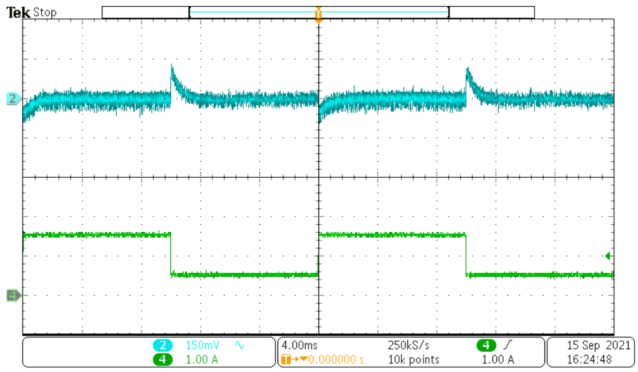
V_{BUS_C}: 5 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT})



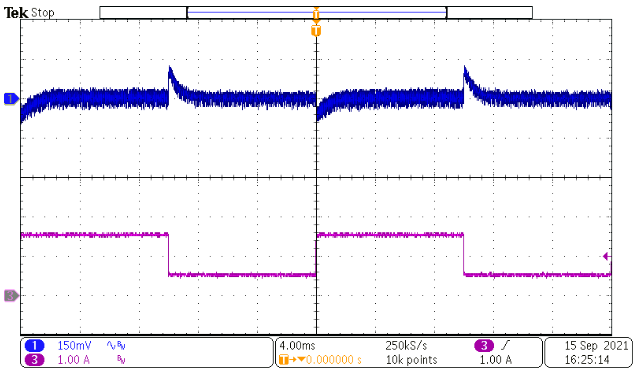
V_{BUS_C}: 5 V; (CH2: Port #1 V_{BUS_C}, CH3: Port #1 I_{OUT})

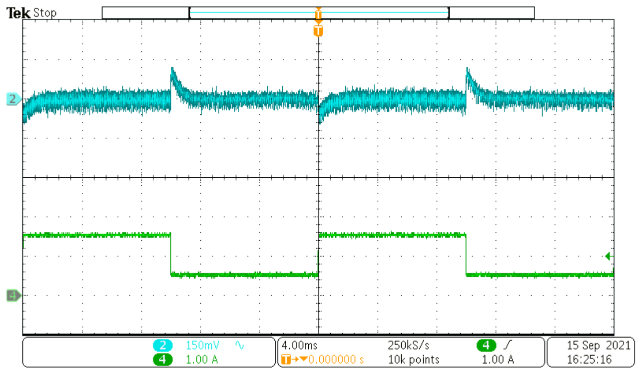


V_{BUS_C}: 9 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT})

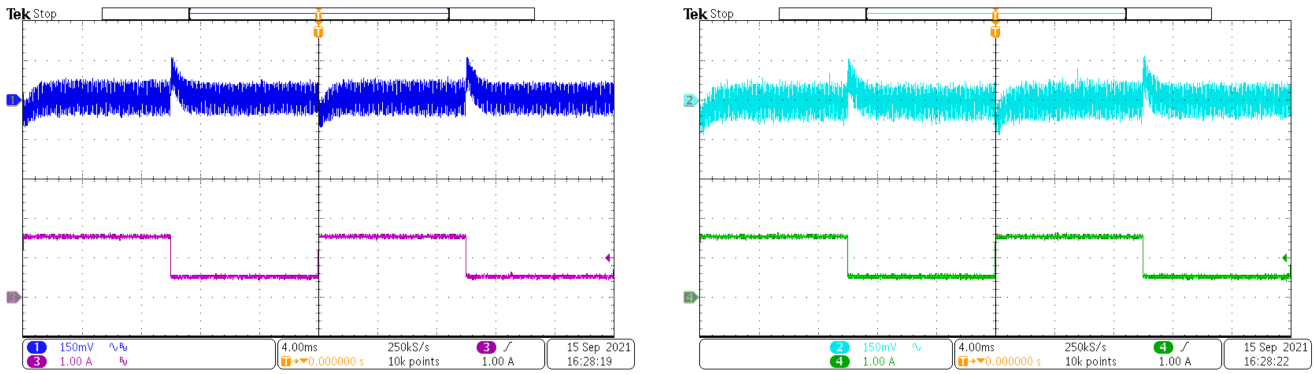


V_{BUS_C}: 9 V; (CH2: Port #1 V_{BUS_C}, CH3: Port #1 I_{OUT})





V_{BUS_C}: 15 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT}) — V_{BUS_C}: 15 V; (CH2: Port #1 V_{BUS_C}, CH3: Port #1 I_{OUT})

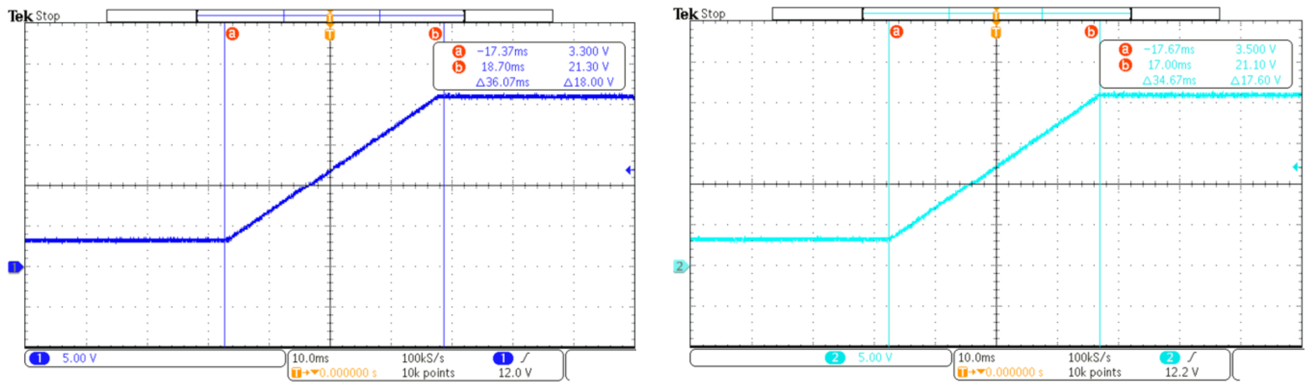


V_{BUS_C}: 20 V; (CH1: Port #0 V_{BUS_C}, CH3: Port #0 I_{OUT}) — V_{BUS_C}: 20 V; (CH2: Port #1 V_{BUS_C}, CH3: Port #1 I_{OUT})

Figure 26 Output dynamic response waveforms - Input 24 V; Load transition 0.5 A to 1.5 A to 0.5 A

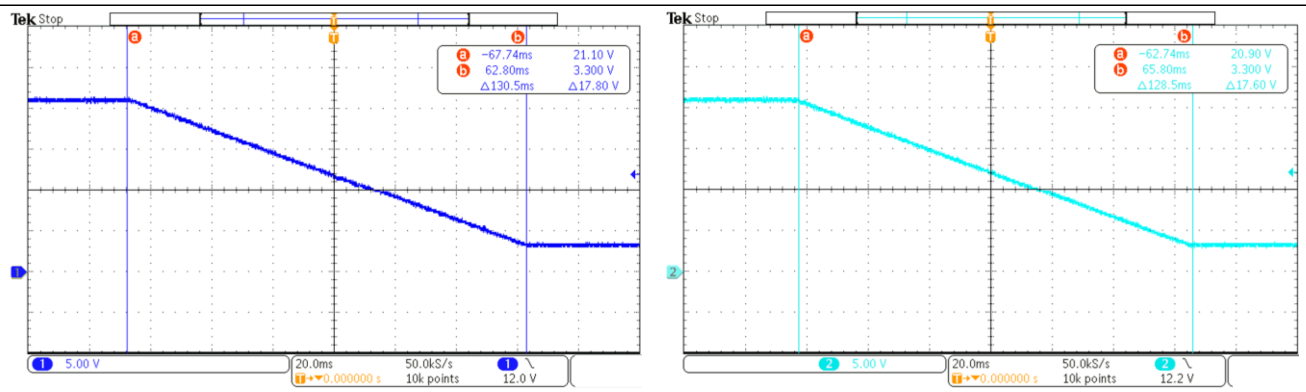
4.9 Output voltage transition

The output voltage transition at 12 V_{DC} input and load current (2.25 A) is measured and is shown in **Figure 27** and **Figure 28**.



Port #0 I_{OUT}: 2.25 A (CH1: Port #0 V_{BUS_C}) — Port #1 I_{OUT}: 2.25 A (CH2: Port #1 V_{BUS_C})

Figure 27 Input 12 V_{DC}; V_{BUS_C} transition from 3.3 V to 20 V

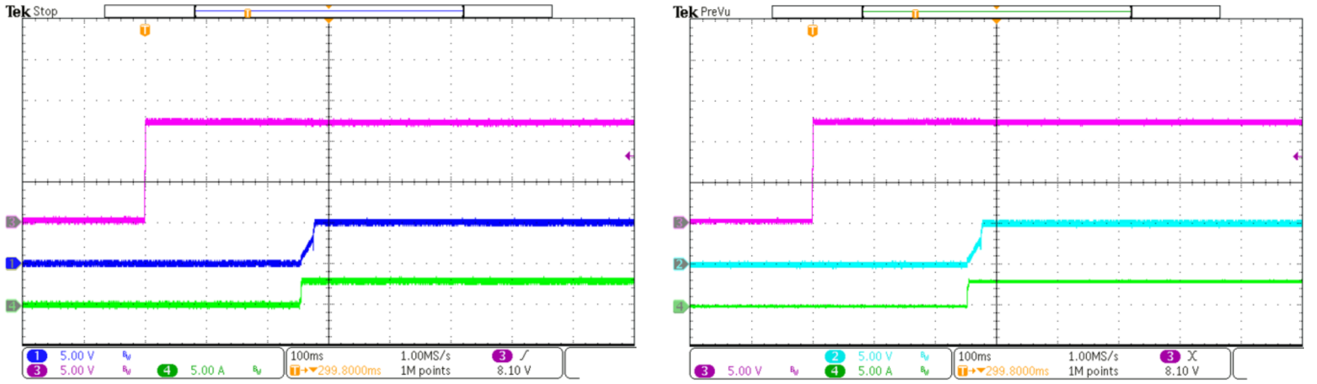


Port #0 I_{OUT}: 2.25 A (CH1: Port #0 V_{BUS_C}) — Port #1 I_{OUT} : 2.25 A (CH2: Port #1 V_{BUS_C})

Figure 28 Input 12 V_{DC}; V_{BUS_C} transition from 20.0 V to 3.3 V

4.10 Start-up turn-on delay

Turn-on delay w.r.t DUT input voltage and output voltage is measured at load current (3 A) and is shown in **Figure 29**.



Port #0: (CH1: V_{BUS_C}; CH3: V_{IN}; CH4: I_{OUT}) Port #1: (CH2: V_{BUS_C}; CH3: V_{IN}; CH4: I_{OUT})

Figure 29 Input 12 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 3 A

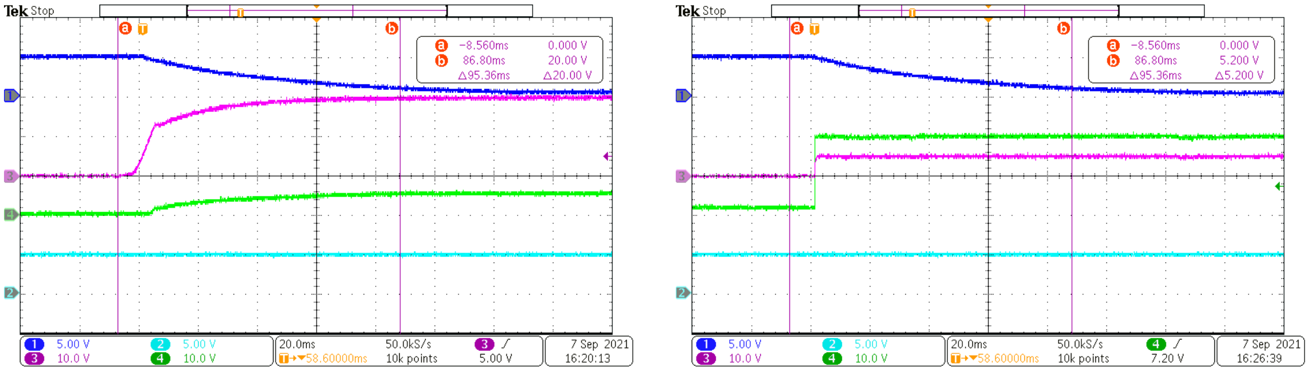
4.11 Faults test waveforms

CLA solution board was subjected to supported fault protections and is shown as follows:

4.11.1 VBus to CCx line faults test waveforms

V_{BUS_C} to Port #0 CCx lines fault on Port #0 is shown in **Figure 30**.

V_{IN} = 12 V, Port #0 V_{BUS_C}: 5 V; Port #1 V_{BUS_C}: 5 V



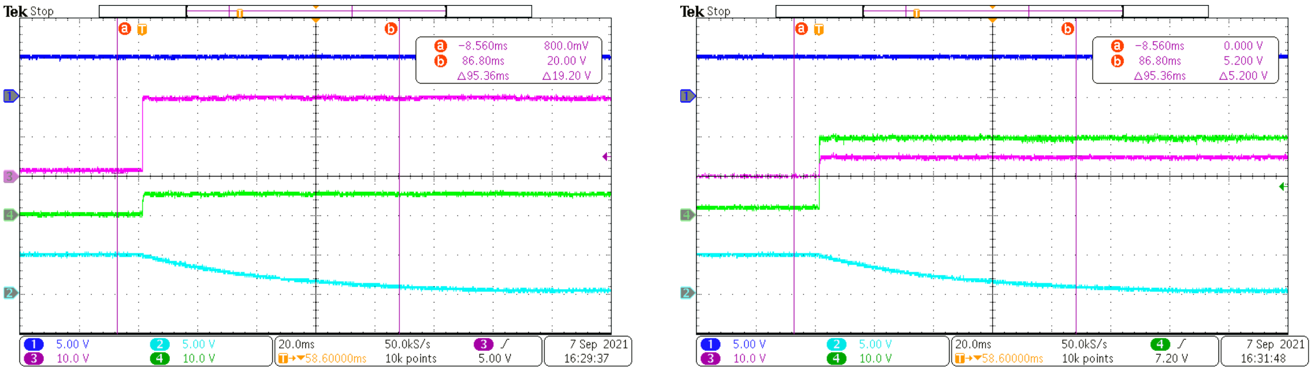
V_{BUS_C} to CC1 fault on Port #0 V_{BUS_C} to CC2 fault on Port #0

CH1: Port #0 V_{BUS_C}; CH2: Port #1 CC1; CH3: Port #0 CC1; CH4: Port #0 CC2

Figure 30 Port #0 V_{BUS_C} to CC line fault

V_{BUS_C} to Port #0 CCx lines fault on Port #1 is shown in **Figure 31**.

V_{IN} = 12 V, Port #0 V_{BUS_C}: 5 V; Port #1 V_{BUS_C}: 5 V



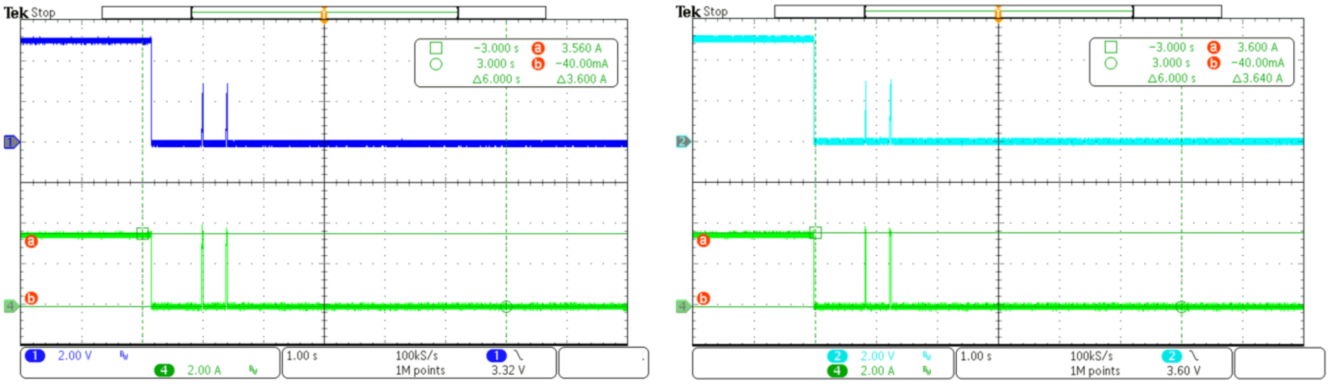
V_{BUS_C} to CC1 fault on Port #1 V_{BUS_C} to CC2 fault on Port #1

CH1: Port #0 V_{BUS_C}; CH2: Port #1 CC1; CH3: Port #1 CC1; CH4: Port #1 CC2

Figure 31 Port #1 V_{BUS_C} to CC line fault

4.11.2 Output overcurrent protection

DUT output overcurrent protection waveforms are shown in **Figure 32**.

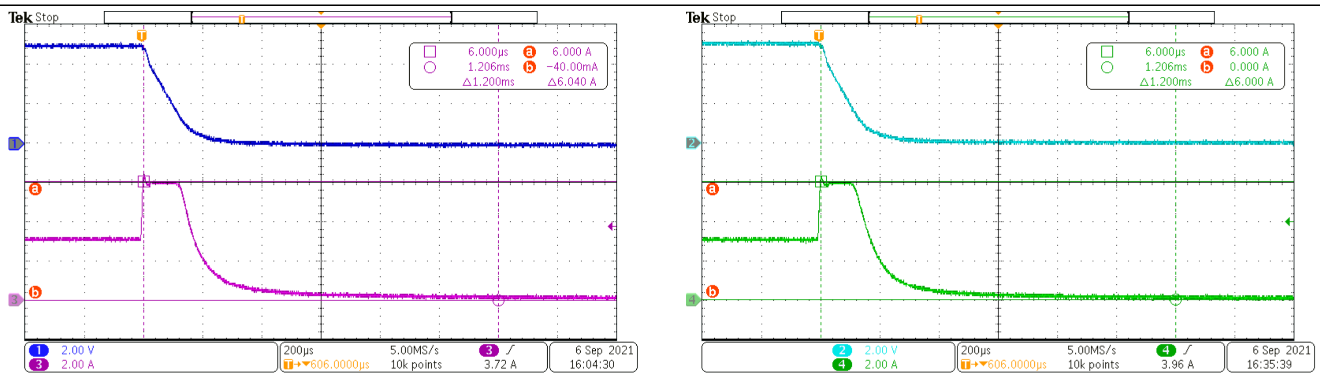


V_{IN}: 12 V; Port #0 V_{BUS_C}: 5 V, OCP at 3.6 A V_{IN}: 12 V; Port #1 V_{BUS_C}: 5 V, OCP at 3.64 A

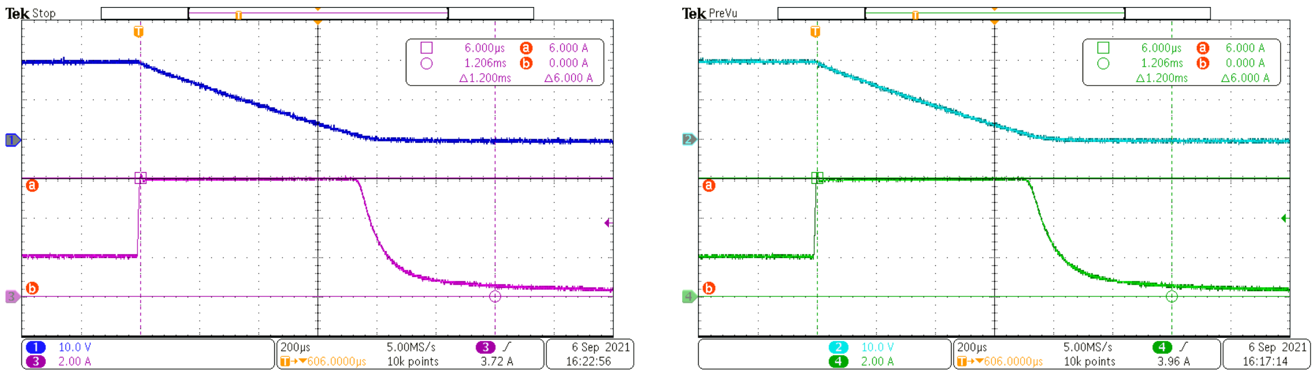
Figure 32 Output overcurrent protection

4.11.3 Output short-circuit protection

DUT output short-circuit protection waveforms are shown in **Figure 33**.



V_{IN}: 12 V; Port #0 V_{BUS_C}: 5 V, SCP at 6 A V_{IN}: 12 V; Port #1 V_{BUS_C}: 5 V, SCP at 6 A



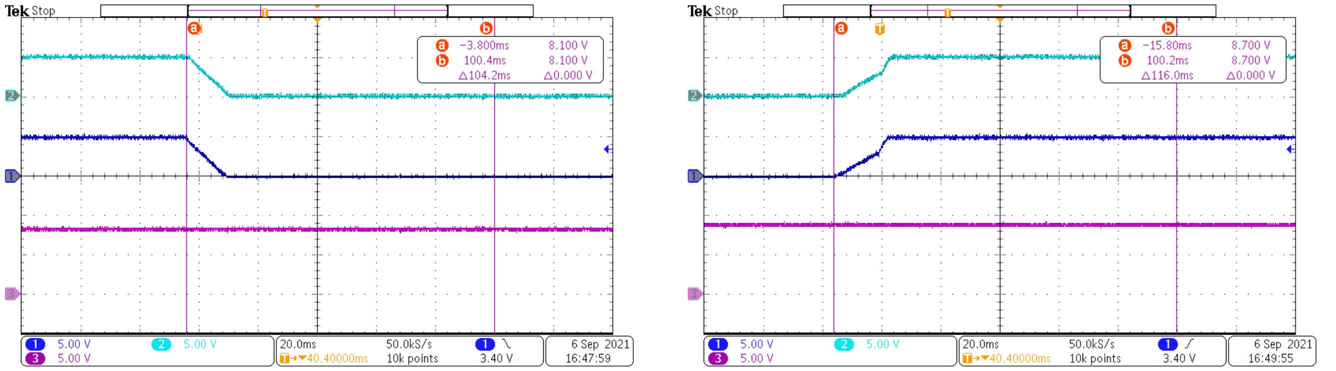
V_{IN}: 12 V; Port #0 V_{BUS_C}: 20 V, SCP at 6 A V_{IN}: 12 V; Port #1 V_{BUS_C}: 20 V, SCP at 6 A

Figure 33 Output short-circuit protection

4.11.4 Input under voltage protection

DUT input undervoltage protection waveforms are shown in **Figure 34**.

Test condition: Port #0, Port #1: V_{BUS_C}: 5.0 V, I_{OUT}: 1 A



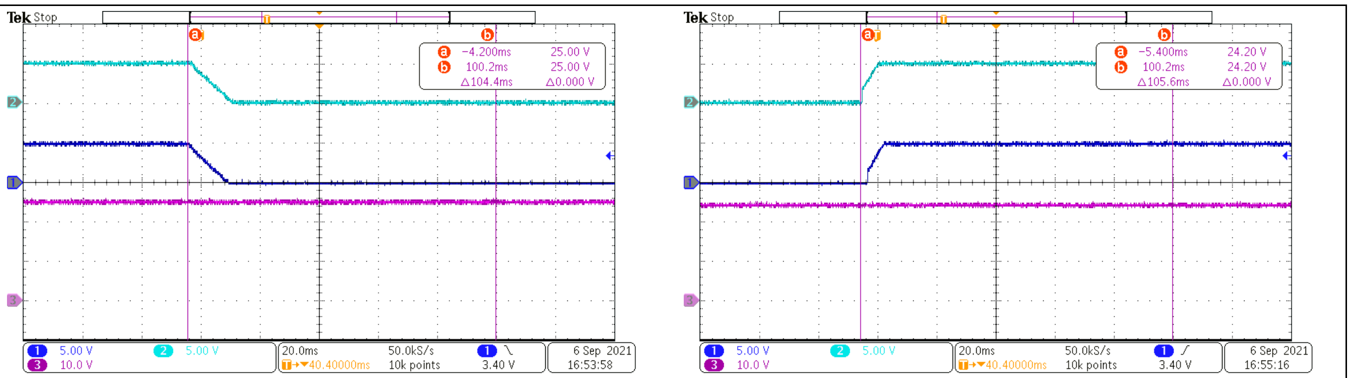
CH1: : Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN};

Figure 34 Input under voltage protection and recovery

4.11.5 Input over voltage protection

DUT input overvoltage protection waveforms are shown in **Figure 35**.

Test condition: Port #0, Port #1: V_{BUS_C}: 5.0 V, I_{OUT}: 1 A



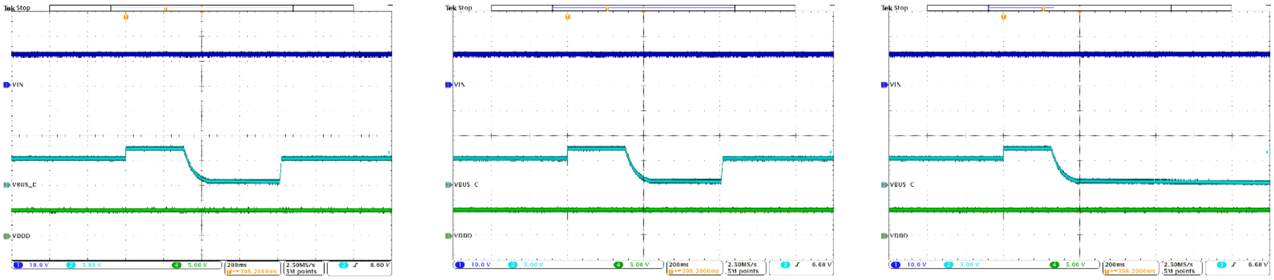
CH1: : Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN};

Figure 35 Input over voltage protection and recovery

4.11.6 Output overvoltage protection

DUT output overvoltage protection waveforms are shown in **Figure 36**.

Test condition: V_{IN}: 12.0 V_{DC}; Port #0, Port #1: V_{BUS_C}: 5.0 V, I_{OUT}: 0 A



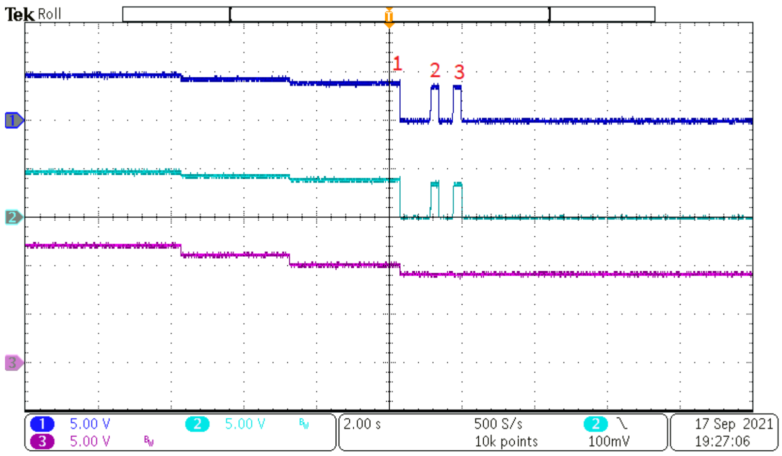
1st iteration 2nd iteration 3rd iteration

Figure 36 Output overvoltage protection

4.11.7 Output undervoltage protection

DUT output undervoltage protection waveforms are shown in **Figure 37**.

Test condition: V_{IN}: 12.0 V_{DC}; Port #0, Port #1: V_{BUS_C}: 5.0 V, I_{OUT}: 3 A



CH1: Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN}

Figure 37 Output under voltage protection

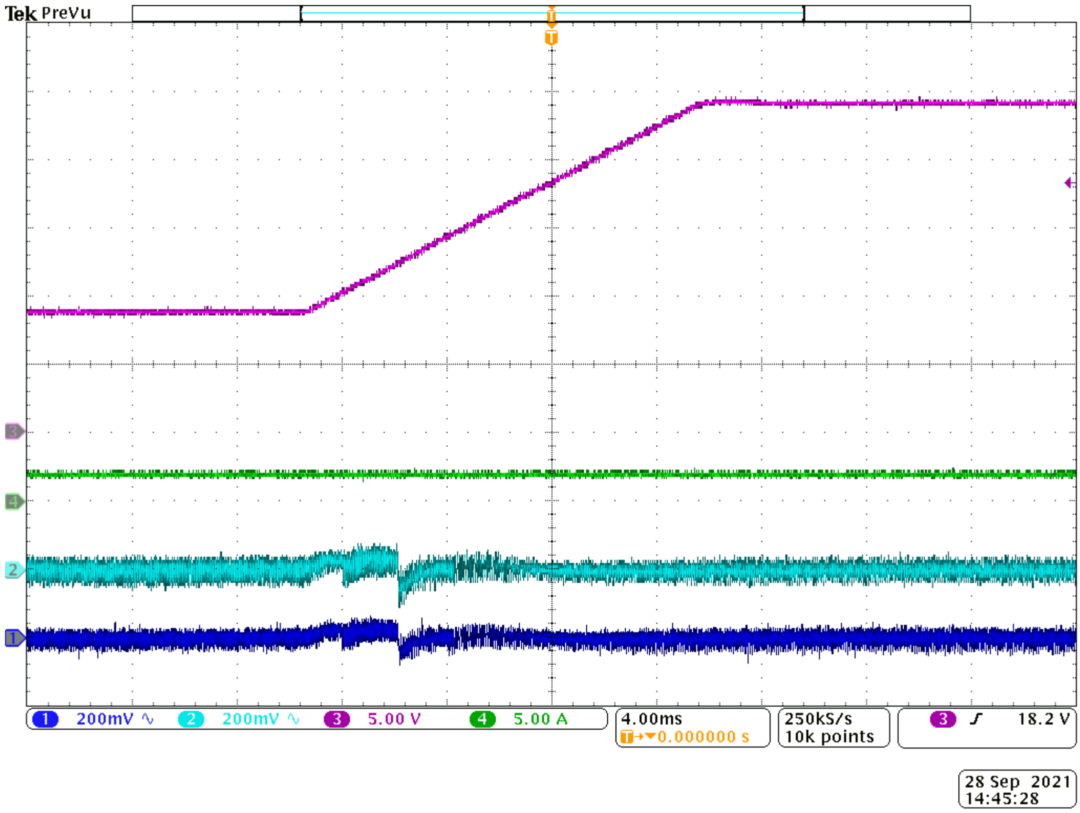
The above shown three itirations of under voltage(3.5 V), after 3rd iteration V_{BUS_C} is latched to 0 V.

4.11.8 PWM mode transition in FCCM

Based on the input voltage to the converter and the V_{BUS_C} contract, CCG7D-consumer delivers PWMs to the power MOSFETs. To change the converter mode (buck, boost, or buck-boost) dynamically, the input voltage is varied from 9 V_{DC} to 24 V_{DC} and V_{BUS_C} is maintained at 12 V_{DC}.

Mode transition in FCCM is shown in **Figure 38**.

Test condition: V_{IN}: 9.0 V_{DC} to 24.0 V_{DC}; Port #0 V_{BUS_C}: 12.0 V, Port #0 I_{OUT}: 2 A; Port #1 V_{BUS_C}: 12.0 V, Port #1 I_{OUT}: 2 A



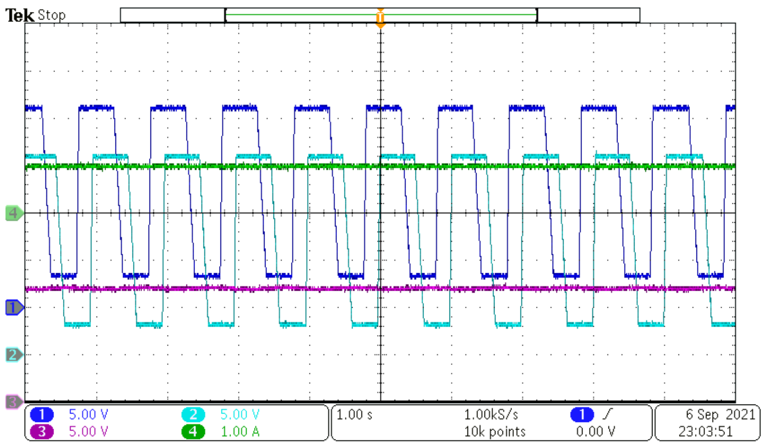
CH1: Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN}; CH4: Port#1 I_{OUT}

Figure 38 PWM mode transition in FCCM

4.12 Stress test waveforms

The CLA solution board was subjected to electrical stress conditions.

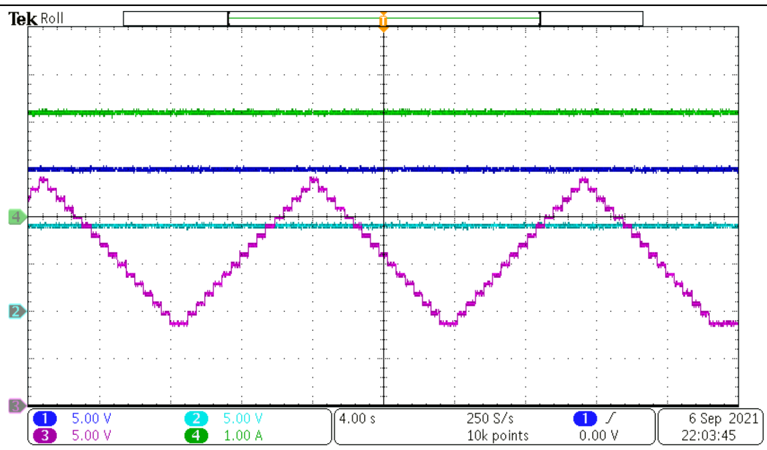
Electrical stress test #1: V_{IN}:12 V_{DC}; Port #0 V_{BUS_C} and Port #1 V_{BUS_C} are continuously changing from 3.3 V - 21 V vice versa; Port #0 V_{BUS_C} and Port #1 V_{BUS_C} I_{OUT}: 1 A for a duration of 15 min. Captured waveforms are shown in **Figure 39**.



CH1: Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN}; CH4: Port #1 I_{OUT}

Figure 39 **V_{IN}: 12 V_{DC}; V_{BUS_C}: Continuously changing from 3.3 V-21 V vice versa; I_{OUT}: 1 A on both the ports**

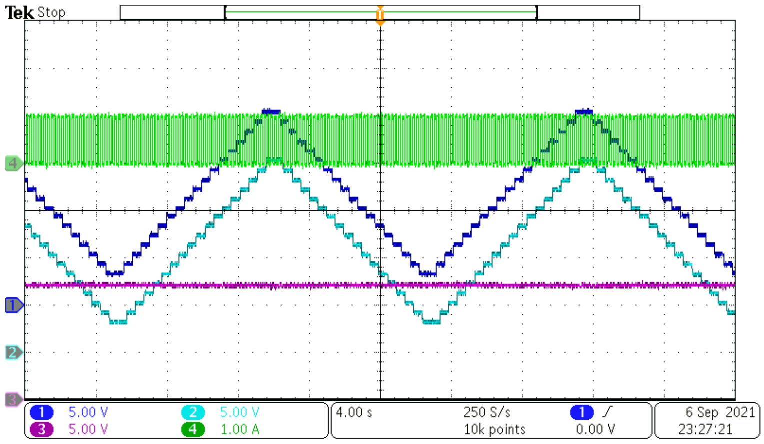
Electrical stress test #2: V_{IN}: Continuously changing from 9 V_{DC} to 24 V_{DC} and vice versa; Port #0 V_{BUS_C}: 15 V; Port #0 I_{OUT}: 3 A and Port #1 V_{BUS_C}: 9 V, Port #1 I_{OUT} : 2.22 A for a duration of 30 minutes. Captured waveforms are shown in **Figure 40**.



CH1: Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN}; CH4: Port #1 I_{OUT}

Figure 40 **V_{IN}: Continuously changing from 9 V_{DC} to 24 V_{DC} vice versa; Port #0 V_{BUS_C}: 15 V; Port #0 I_{OUT}: 3 A and Port #1 V_{BUS_C}: 9 V, Port #1 I_{OUT}: 2.22 A**

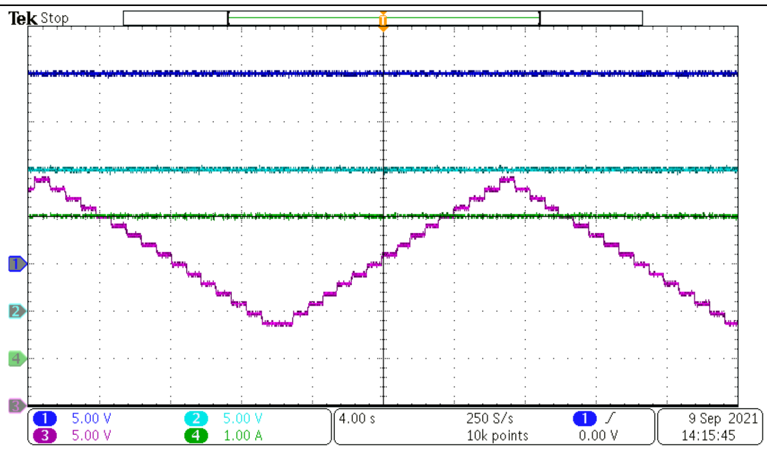
Electrical stress test #3: V_{IN}:12 V_{DC}; Port #0 V_{BUS_C} and Port #1 V_{BUS_C} are continuously changing from 3.3 V - 21 V vice versa; Port #0 I_{OUT} and Port #1 I_{OUT} are continuously changing from 0 A - 1 A and vice versa for a duration of 30 minutes. Captured waveforms are shown in **Figure 41**.



CH1: Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN}; CH4: Port #1 I_{OUT}

Figure 41 V_{IN}: 12 V_{DC}; V_{BUS_C}: continuously changing from 3.3 V-21 V vice versa; I_{OUT}: continuously changing from 0 A – 1 A and vice versa

Electrical stress test #4: V_{IN}: Continuously changing from 9 V – 24 V and vice versa; Port #0 V_{BUS_C}: 15 V; Port #0 I_{OUT}: 3 A and Port #1 V_{BUS_C}: 20 V; Port #1 I_{OUT} : 1 A for a duration of 30 min. Captured waveforms are shown in **Figure 42**.



CH1: Port #0 V_{BUS_C}; CH2: Port #1 V_{BUS_C}; CH3: V_{IN}; CH4: Port #1 I_{OUT}

Figure 42 V_{IN}: Continuously changing from 9 V – 24 V and vice versa; Port #0 V_{BUS_C}: 15 V; Port #0 I_{OUT}: 3 A and Port #1 V_{BUS_C}: 20 V; Port #1 I_{OUT} : 1 A

4.13 Current consumption

EZ-PD™ CCG7D-consumer solution board and silicon (CCG7D-consumer) currents are measured and tabulated in **Table 20**.

Table 20 Current consumption

Test condition	Current (mA)	Remarks
Full active – Silicon current (into the silicon, pin #61) Two ports attached	29.3 30.38 44.6	Buck mode operation (V_{IN}: 12 V_{DC}; Port #0, 1 V_{BUS_C}: 05 V) Boost mode operation (V_{IN}: 12 V_{DC}; Port #0, 1 V_{BUS_C}: 20 V) Buck-boost mode Operation (V_{IN}: 12 V_{DC}; Port #0, 1 V_{BUS_C}: 12 V)
Full active – Board current (measured at input connector) Two ports attached	44.9 78.3 76.8	Buck mode operation (V_{IN}: 12 V_{DC}; Port #0, 1 V_{BUS_C}: 05 V) Boost mode operation (V_{IN}: 12 V_{DC}; Port #0, 1 V_{BUS_C}: 20 V) Buck-boost mode operation (V_{IN}: 12 V_{DC}; Port #0, 1 V_{BUS_C}: 12 V)
Sleep current – Silicon current (into the silicon, pin #61)	0.44	Both ports detached condition: (V_{IN}: 12 V_{DC})
Sleep current – Board current (measured at input connector)	0.47	Both ports detached condition: (V_{IN}: 12 V_{DC})

Note:

1. *Silicon current is measured on the EZ-PD™ CCG7D-consumer validation board.*

5 Thermal scan

DUT temperature measurements are captured at ambient temperature on both sides of the PCB.

5.1 Temperature measurement using thermal camera at room temperature

5.1.1 Thermal image top view

- **Test condition:** V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 20 V, I_{OUT} = 2.25 A and Port #1: V_{BUS_C} = 9 V, I_{OUT} = 2.22 A
- Lab ambient temperature: 25°C and thermal scan captured in open-frame after 90 minutes (see **Figure 43**).

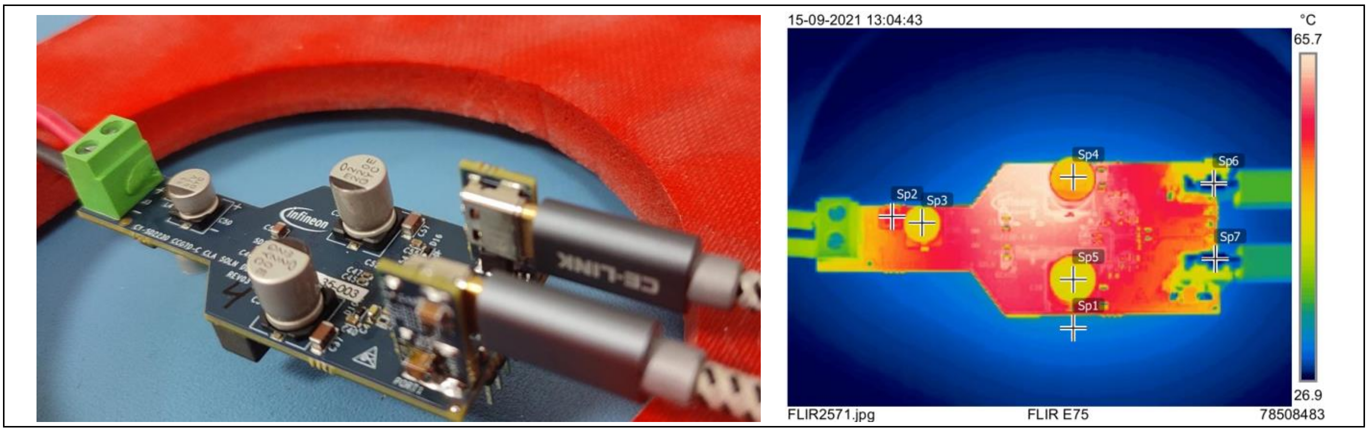


Figure 43 DUT (TOP) thermal image at ambient temperature, V_{IN}:12 V; Port #0: V_{BUS_C}: 20 V, I_{OUT}: 2.25 A; Port #1 V_{BUS_C}: 9 V, I_{OUT}: 2.22 A

Table 21 Temperature measurement

Marking	Designator	Component	Temperature
Sp2	L4	Port #0 EMI inductor	57.1°C
Sp3	C50	Port #0 input bulk capacitor	47.9°C
Sp4	C56	Port #0 output bulk capacitor	50.6°C
Sp5	C39	Port #1 output Bulk capacitor	46.3°C
Sp6	J4	Port #0 Type-C connector	27.8°C
Sp7	J1	Port #1 Type-C connector	27.5°C

5.2 Thermal image bottom view

- **Test condition:** V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 20 V, I_{OUT} = 2.25 A and Port #1: V_{BUS_C} = 9 V, I_{OUT} = 2.22 A
- Lab ambient temperature: 28°C and thermal scan captured in open-frame after 90 minutes (see **Figure 44**).

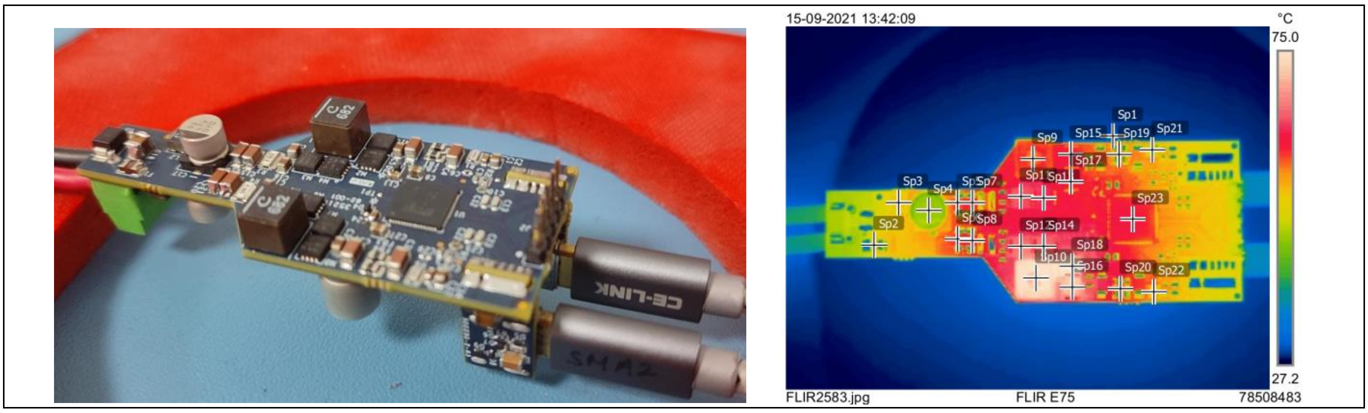


Figure 44 DUT (TOP) thermal image at ambient temperature, V_{IN}:12 V; Port #0: V_{BUS_C}: 20 V, I_{OUT}: 2.25 A; Port #1 V_{BUS_C}: 9 V, I_{OUT}: 2.22 A

Table 22 Temperature measurement

Marking	Designator	Component	Temperature
Sp1		Ambient temperature	29.3°C
Sp2	F1	Fuse	54.3°C
Sp3	L2	Port #1 EMI inductor	54.9°C
Sp4	C17	Port #1 input bulk capacitor	48.5°C
Sp5	C14, C15	Port #1 input MLCC	60.6°C
Sp6	C21, C20	Port #0 input MLCC	61.5°C
Sp7	R3	Port #1 input current sense resistor	61.6°C
Sp8	R4	Port #0 input current sense resistor	62.0°C
Sp9	L1	Port #1 power Inductor	59.6°C
Sp10	L3	Port #0 power Inductor	74.0°C
Sp11	M3	Port #1 M3 (HS1)	66.1°C
Sp12	M5	Port #0 M5 (HS1)	67.6°C
Sp13	M4	Port #1 M4 (LS1)	64.8°C
Sp14	M6	Port #0 M6 (LS1)	67.7°C
Sp15	M1	Port #1 M1 (HS2)	61.9°C
Sp16	M8	Port #0 M8 (HS2)	72.4°C
Sp17	M2	Port #1 M2 (LS2)	62.9°C
Sp18	M7	Port #0 M7 (LS2)	75.3°C
Sp19	FB1, FB2	Port #1 output ferrite beads	59.8°C
Sp20	FB3, FB4	Port #0 output ferrite beads	64.1°C
Sp23	U1	CCG7D-consumer	62.7°C

5.3 Temperature measurement using thermocouple at elevated ambient temperature

- Test condition: V_{IN} = 12 V_{DC}; Port #0 V_{BUS_C} = 20 V; Port#0 I_{OUT} = 2.25 A; Port #1 V_{BUS_C} = 9 V; Port#1 I_{OUT} = 2.22 A
- Ambient temperature: Temperature of individual components are measured and shown in **Figure 45** at ambient -20°C, 25°C, 45°C, and 70°C

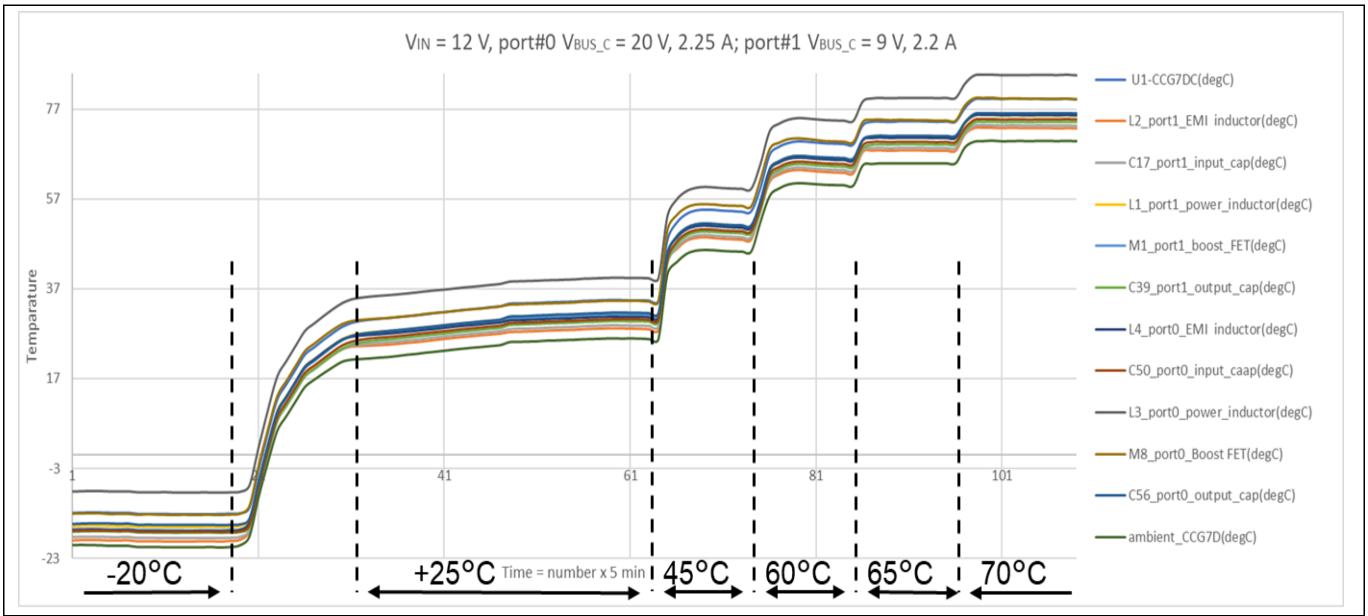


Figure 45 **Temperature of individual components at elevated temperature, V_{IN}:12 V; Port #0: V_{BUS_C}: 20 V, I_{OUT}: 2.25 A; Port #1 V_{BUS_C}: 9 V, I_{OUT}: 2.22 A**

Temperature of individual components are shown in the **Table 23**.

Table 23 **Temperature measurement of individual components at elevated temperature**

Component	Designator	At –20°C ambient (°C)	At 25°C ambient (°C)	At 45°C ambient (°C)	At 70°C ambient (°C)
Ambient temperature	-	–20.68	25.40	45.29	69.98
CCG7D-consumer	U1	–13.14	34.95	54.29	79.29
Port #1 EMI inductor	L2	–19.22	29.00	48.03	72.78
Port #1 input bulk capacitor	C17	–18.51	29.38	48.59	73.43
Port #1 power inductor	L1	–16.03	31.96	51.19	75.73
Port #1 M1 (HS2)	M1	–16.63	31.53	50.85	75.99
Port #1 output bulk capacitor	C39	–17.40	30.30	49.49	74.29
Port #0 EMI inductor	L4	–16.94	31.39	50.64	75.66
Port #0 input bulk capacitor	C50	–17.23	30.66	49.86	74.79
Port #0 power inductor	L3	–8.42	39.92	59.29	84.68
Port #0 M8 (HS2)	M8	–13.33	36.55	55.49	79.27

Component	Designator	At –20°C ambient (°C)	At 25°C ambient (°C)	At 45°C ambient (°C)	At 70°C ambient (°C)
Port #0 output bulk capacitor	C56	–15.54	32.07	51.25	76.20

Note:

1. *Over temperature protection is disabled to measure the temperature of components at an elevated ambient temperature.*

6 USB-IF pre-compliance tests

Note: USB PD source detailed test reports are available based on request.

6.1 Quadramax

6.1.1 Test setup

- Quad Draw version: 0.8.7779.
- Test Input voltage conditions: 09 V_{DC}, 12 V_{DC} and 16.5 V_{DC}.

Table 24 Quadramax - USB PD source test results

Test	Description	Result
TD SPT.1	Load test	Pass
TD SPT.2	Capabilities test	Pass
TD SPT.3	Hard reset test	Pass
TD SPT.5	OCP test	Pass
TD SPT.6	PPS voltage step test	Pass
TD SPT.7	PPS current limit test	Pass

6.2 Ellisys

6.2.1 Test setup

The test was run using the Ellisys USB Explorer 350 Examiner V3.1.7906 (**https://www.ellisys.com/products/usbex350/**).

Table 25 Ellisys - USB PD source test results

Test	Result
USB Type-C tests	Pass
USB PD physical tests	Pass
USB PD link tests	Pass
USB PD VDM	Pass
USB PD 3.0 tests	Pass
PD merged	Pass

6.3 MQP

6.3.1 Test setup

- The test was run using the packet-master USB-PDT Power Delivery compliance tester (**http://www.mqp.com/data_sheets/Packet-Master/Packet-Master%20USB-PDT%20Data%20Sheet%201_0d.pdf**).
- The graphic USB V6.38.00 software was used to run these tests.

Table 26 MQP - USB PD source test results

Test	Result
Physical tests	Pass
Rev 2 protocol tests	Pass
Power tests	Pass
Rev 3 link layer tests	Pass
Rev 3 protocols tests	Pass

6.4 GRL

- The test was run using USB PD and Type-C tester and analyzer (GRL-USB PD-C2) (**https://graniteriverlabs.com/usb-pd-c2/**).
- The GRL-PD-C2 browser software release version 1.5.63.0 was used to run these tests.

Table 27 GRL - USB PD source test results

Test	Result
PD 3.0 communication tests	Pass
PD 2.0 deterministic tests	Pass
USB Type-C functional tests	Pass
USB PD source power tests	Pass
PD 3.0 compliance tests	Pass
Qualcomm QC 5.0	Pass

6.5 Lecroy

- The test was run using Voyager M310P (**https://teledynelecroy.com/protocolanalyzer/usb/voyager-m310p**).
- The USB Compliance Suite V 5.26 build 959 software was used to run these tests.

Table 28 Lecroy - USB PD source test results

Test	Result
USB Type-C	Pass
Power Delivery 2.0 communication MOI	Pass
Power Delivery 3.0	Pass

7 Bode plots

Note: *R2 and R5 default values on the CLA solution board is 0 Ω, to capture the bode plots R2 and R5 are set as 10 Ω.*

Note: *Port #1 crossover frequency and phase margin is in similar lines with Port#0.*

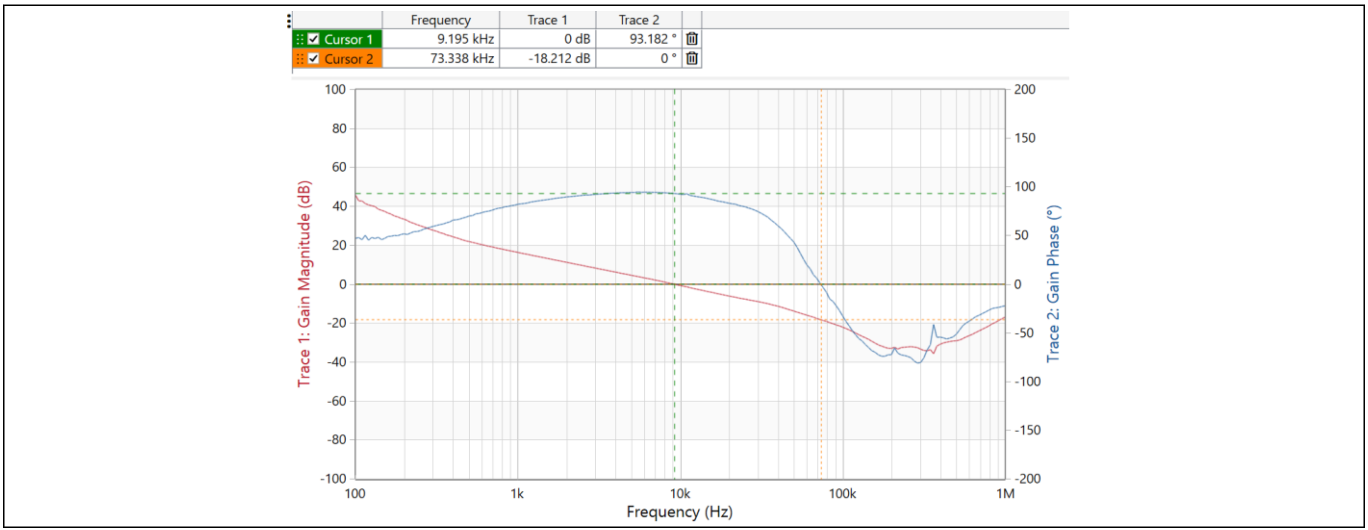


Figure 46 Bode plot: - V_{IN}:12 V_{DC} Port#0: V_{BUS_C}: 5 V; I_{OUT}:3 A

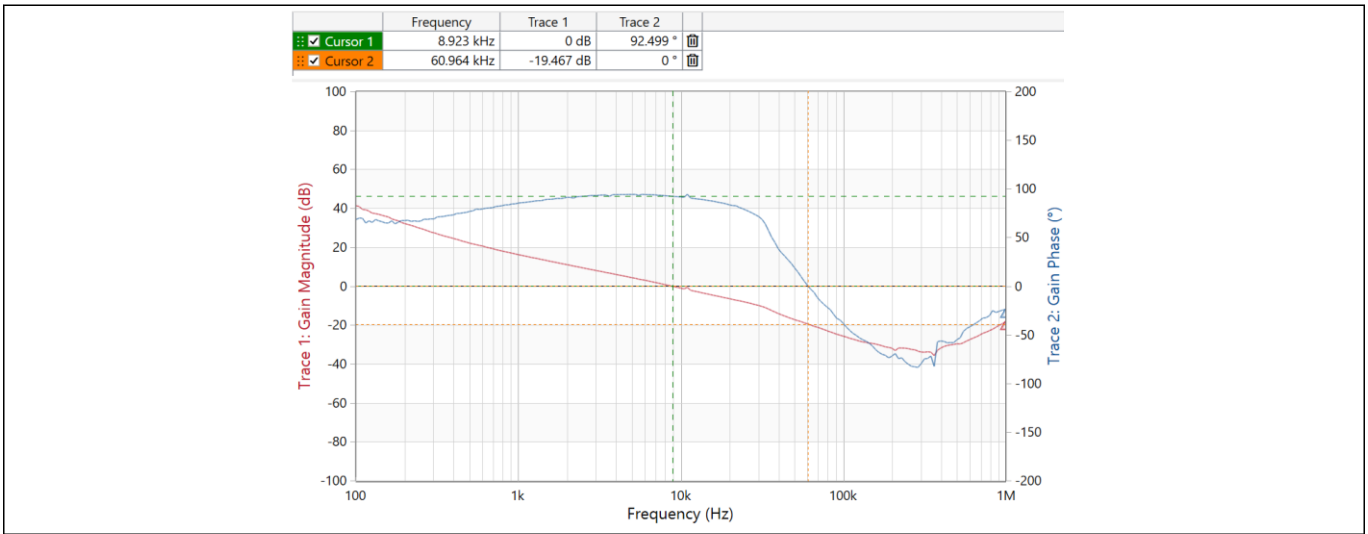


Figure 47 Bode plot: - V_{IN}:12 V_{DC} Port#0: V_{BUS_C}: 9 V; I_{OUT}:3 A

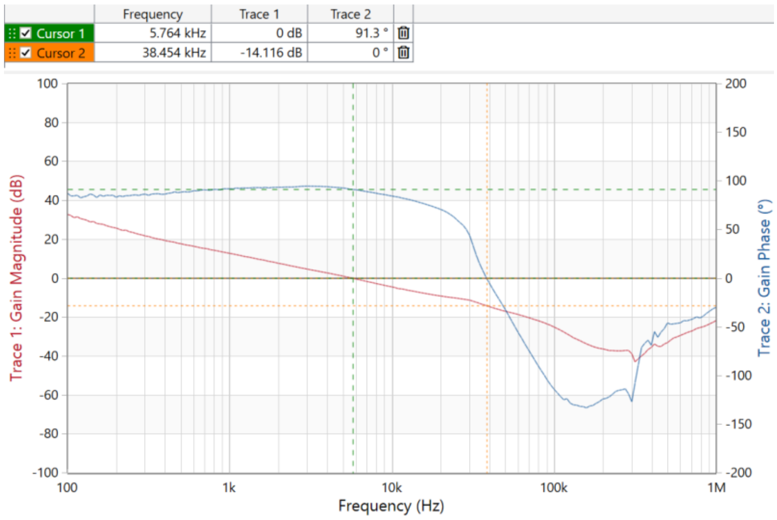


Figure 48 **Bode plot: - V_{IN}:12 V_{DC} Port#0: V_{BUS_C}: 15 V; I_{OUT}:3 A**

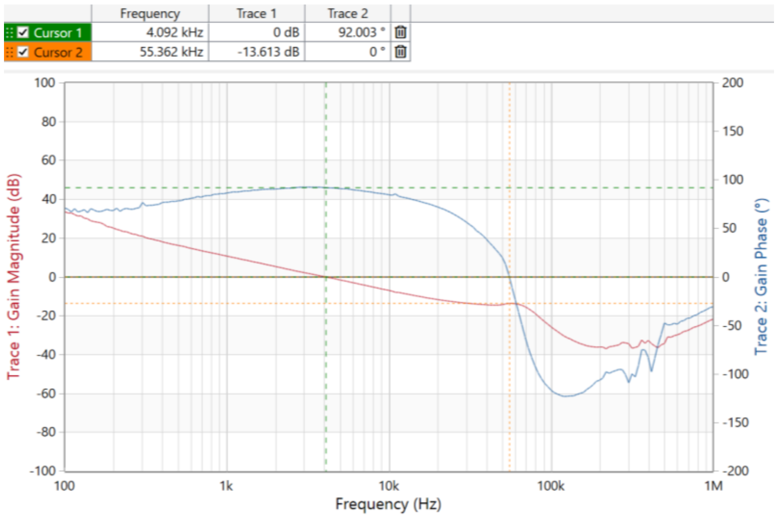


Figure 49 **Bode plot: - V_{IN}: 12 V_{DC} Port#0: V_{BUS_C}: 20 V; I_{OUT}: 2.25 A**

8 CE and RE scans

Note: To improve the conducted and radiated emission margins, consider adding MLCC at the input connector and also at the input bulk capacitors and change the gate drive strength as shown as follows.

Note: For example: Referring the "CCG7D_Consumer_45W_CLA SOLUTION_DEMO_BOARD" schematics add MLCC (CGA5L1X7R1H106K160AC) at C18, MLCC(CGA5L1X7R1H106K160AC) at C14, C15, C20, and C21.

Note: For example: Change the gate pull-up drive strength: LG2 – 5.9 Ω (0x5), HG1– 9.7 Ω (0x4), pull-down drive strength LG2 – 6.6 Ω (0x5), HG1– 10.1 Ω (0x4).

8.1 CE scans

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 5 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 5 V, I_{OUT} = 3.0 A. CE scan is shown in **Figure 50**.

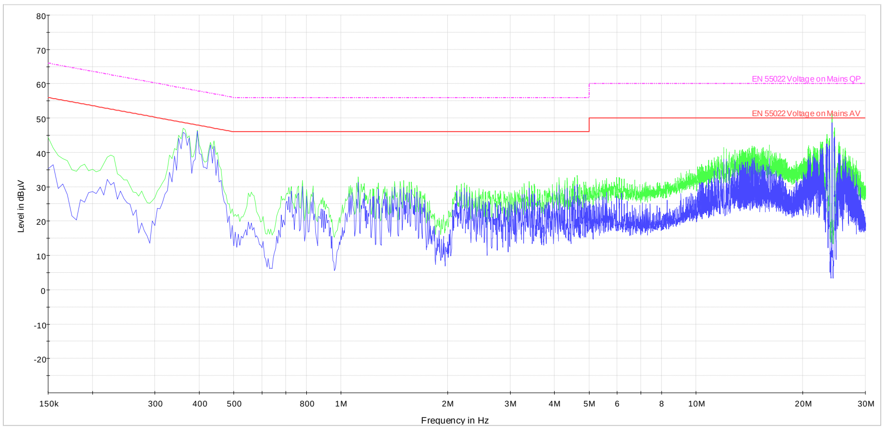


Figure 50 CE scan V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 5 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 5 V, I_{OUT} = 3.0 A

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 9 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 9 V, I_{OUT} = 3.0 A. CE scan is shown in **Figure 51**.

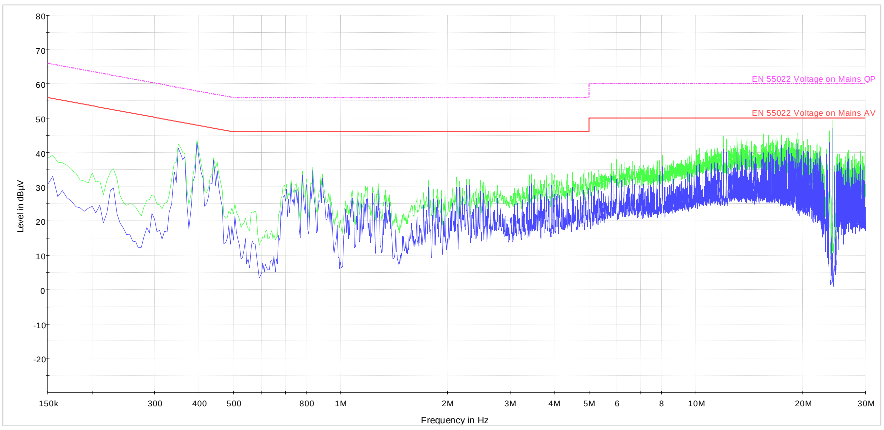


Figure 51 CE scan V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 9 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 9 V, I_{OUT} = 3.0 A

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 12 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 12 V, I_{OUT} = 2.4 A. CE scan is shown in **Figure 52**.

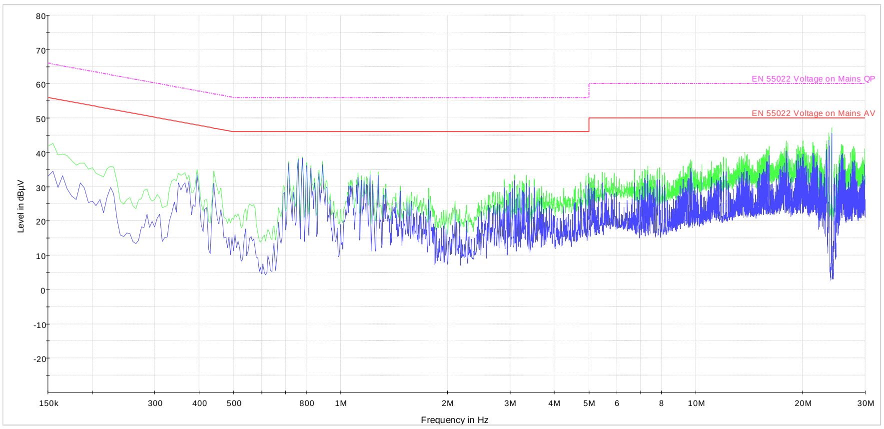


Figure 52 CE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 12 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 12 V, I_{OUT} = 2.6 A

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 15 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 15 V, I_{OUT} = 1.25 A. CE scan is shown in **Figure 53**.

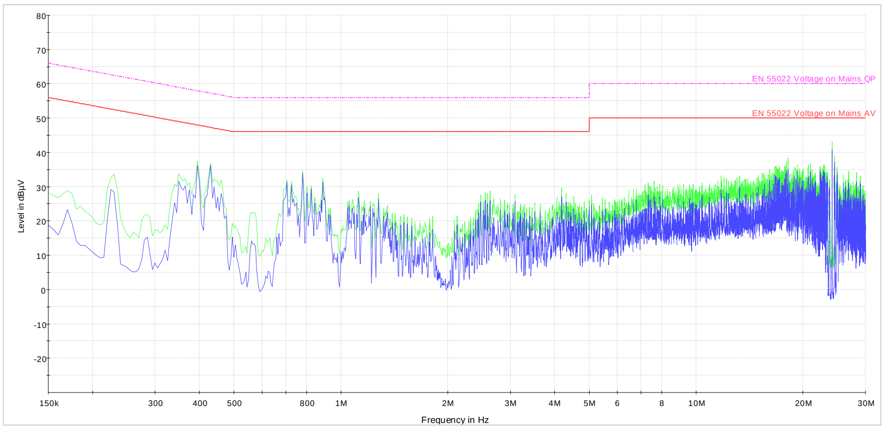


Figure 53 CE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 15 V, I_{OUT} = 3.0 A and Port #1: V_{BUS_C} = 15 V, I_{OUT} = 1.25 A

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 20 V, I_{OUT} = 2.25 A and Port #1: V_{BUS_C} = 20 V, I_{OUT} = 1 A. CE scan is shown in **Figure 54**.

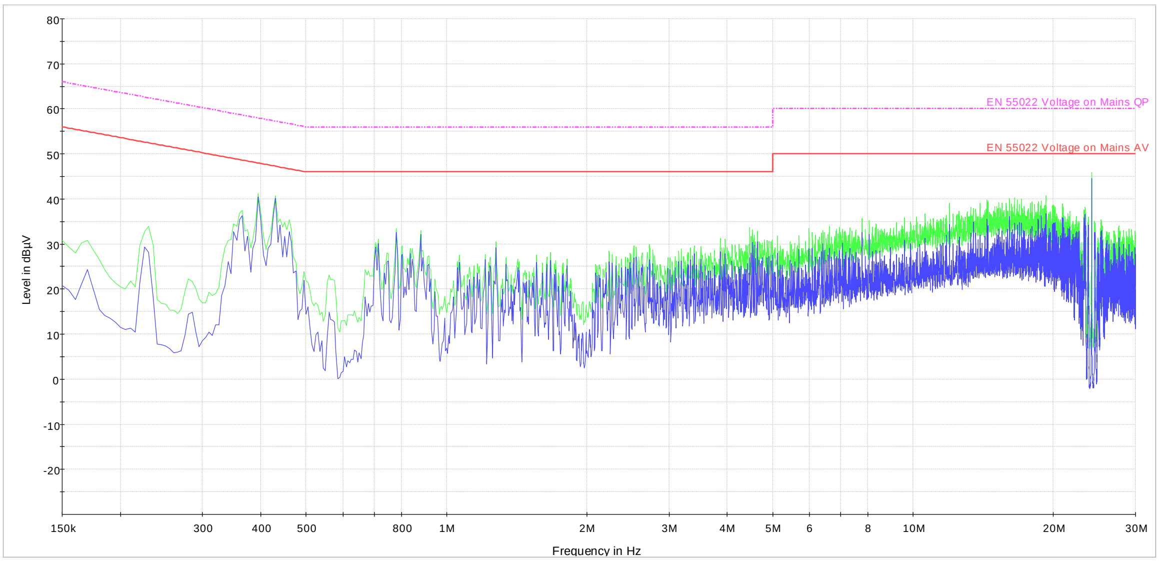


Figure 54 CE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 20 V, I_{OUT} = 2.25 A and Port #1: V_{BUS_C} = 20 V, I_{OUT} = 1 A

8.2 RE scans

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 5 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 5 V, I_{OUT} = 3 A. RE scan is shown in **Figure 55**. Antenna is positioned vertical and horizontal.

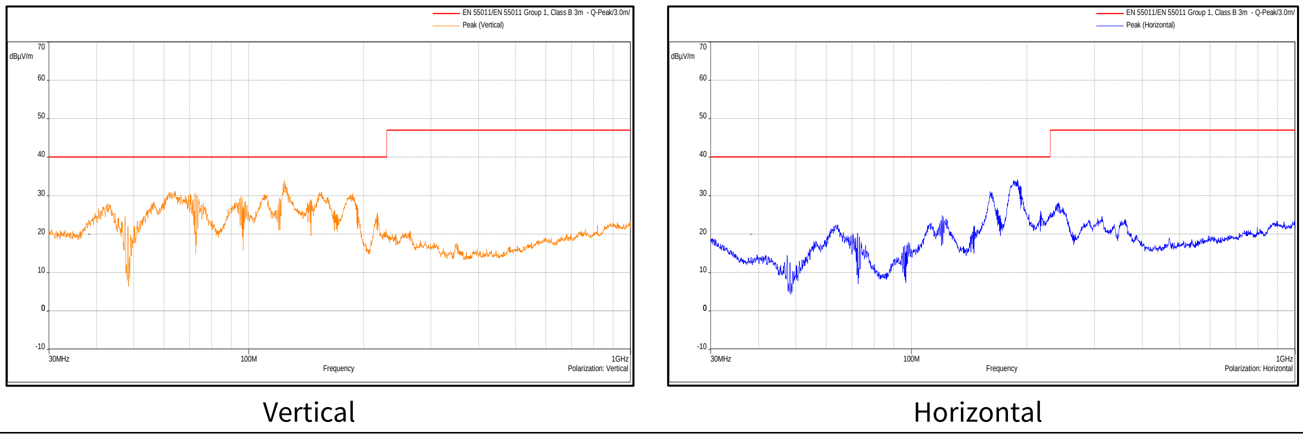


Figure 55 Vertical and horizontal RE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 5 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 5 V, I_{OUT} = 3 A

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 9 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 9 V, I_{OUT} = 3 A. RE scan is shown in **Figure 56**. Antenna is positioned vertical and horizontal.

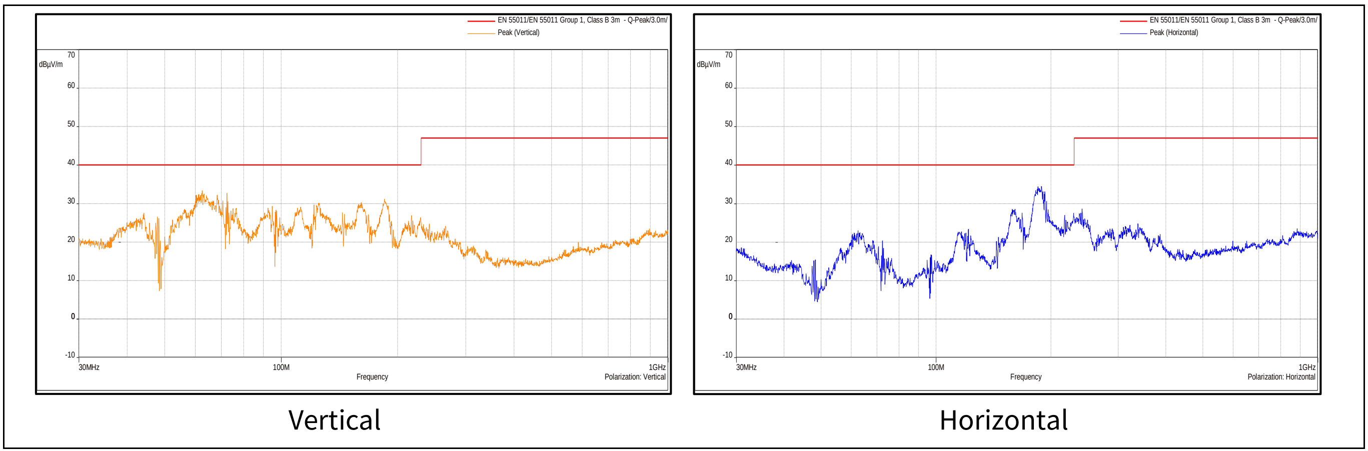


Figure 56 **Vertical and horizontal RE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 9 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 9 V, I_{OUT} = 3 A**

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 12 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 12 V, I_{OUT} = 2.4 A. RE scan is shown in **Figure 57**. Antenna is positioned vertical and horizontal.

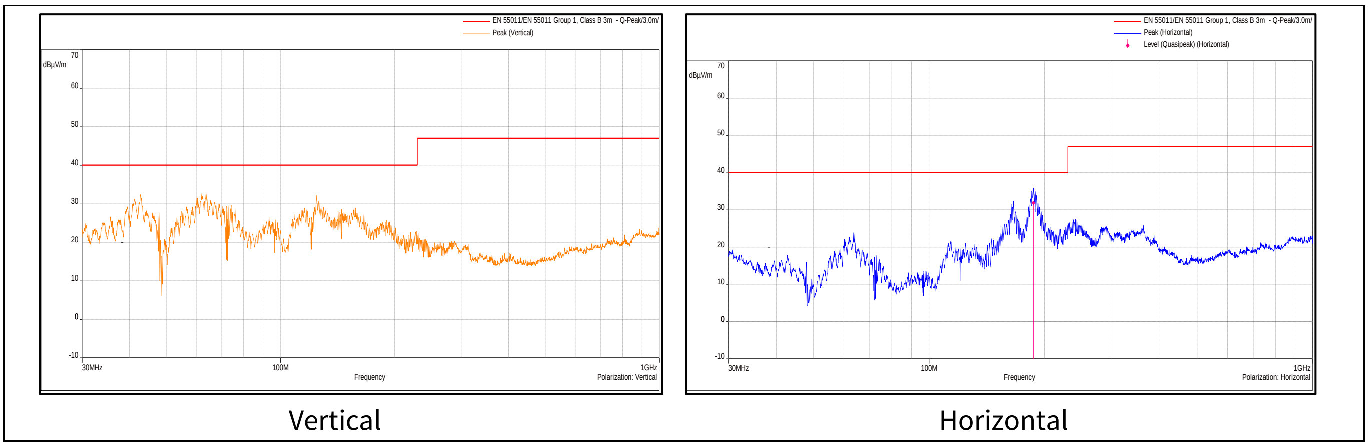
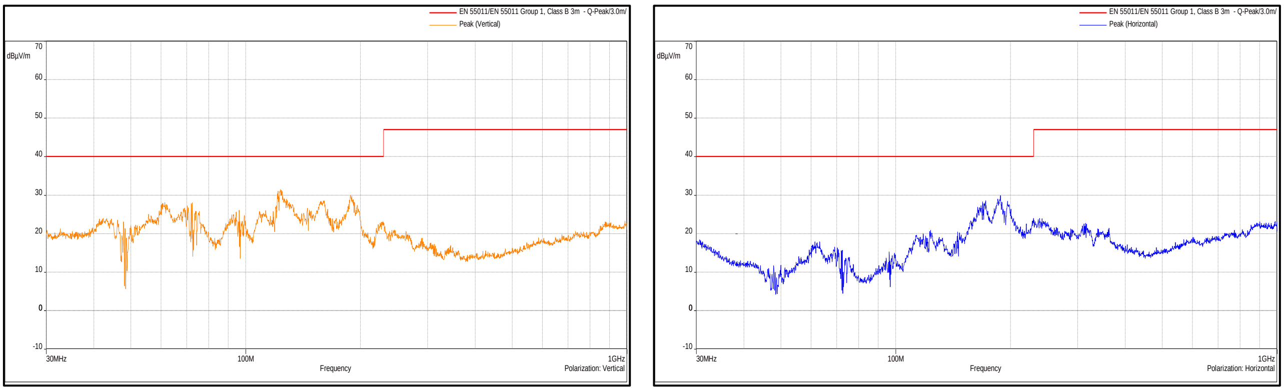


Figure 57 **Vertical and horizontal RE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 12 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 12 V, I_{OUT} = 2.4 A**

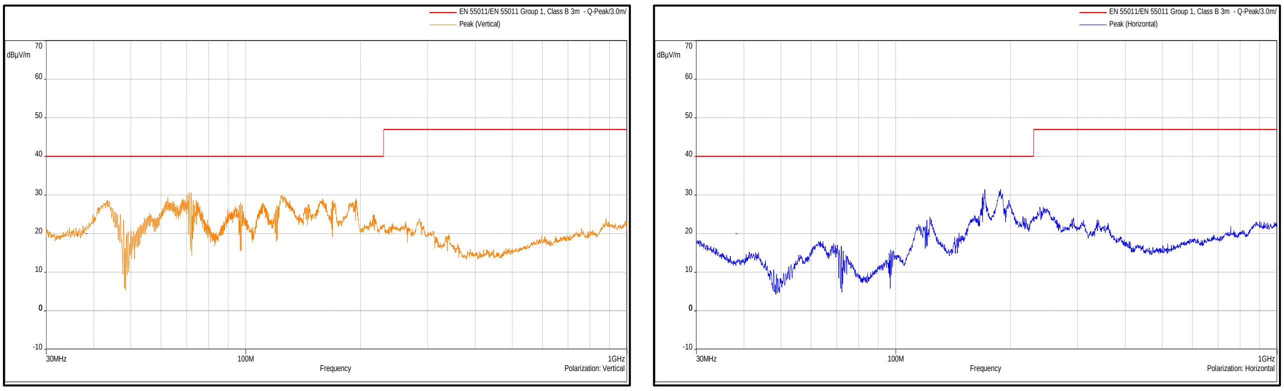
Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 15 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 15 V, I_{OUT} = 1.25 A. RE scan is shown in **Figure 58**. Antenna is positioned vertical and horizontal.



Vertical Horizontal

Figure 58 Vertical and horizontal RE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 15 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 15 V, I_{OUT} = 2.4 A

Test condition: V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 20 V, I_{OUT} = 2.25 A and Port #1: V_{BUS_C} = 20 V, I_{OUT} = 1 A. RE scan is shown in **Figure 59**. Antenna is positioned vertical and horizontal.



Vertical Horizontal

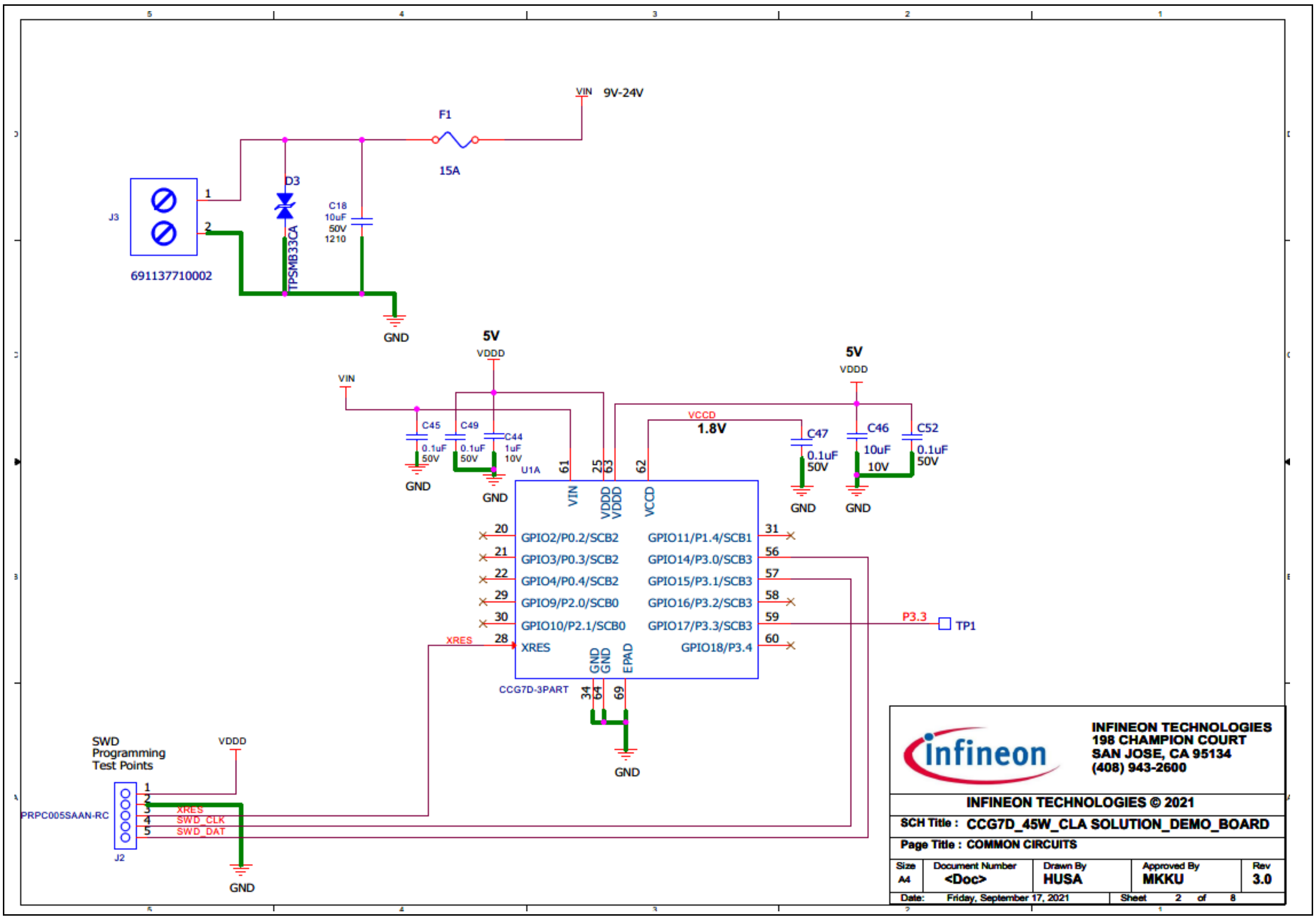
Figure 59 Vertical and horizontal RE scan for V_{IN} = 12 V_{DC}, Port #0: V_{BUS_C} = 15 V, I_{OUT} = 3 A and Port #1: V_{BUS_C} = 15 V, I_{OUT} = 2.4 A

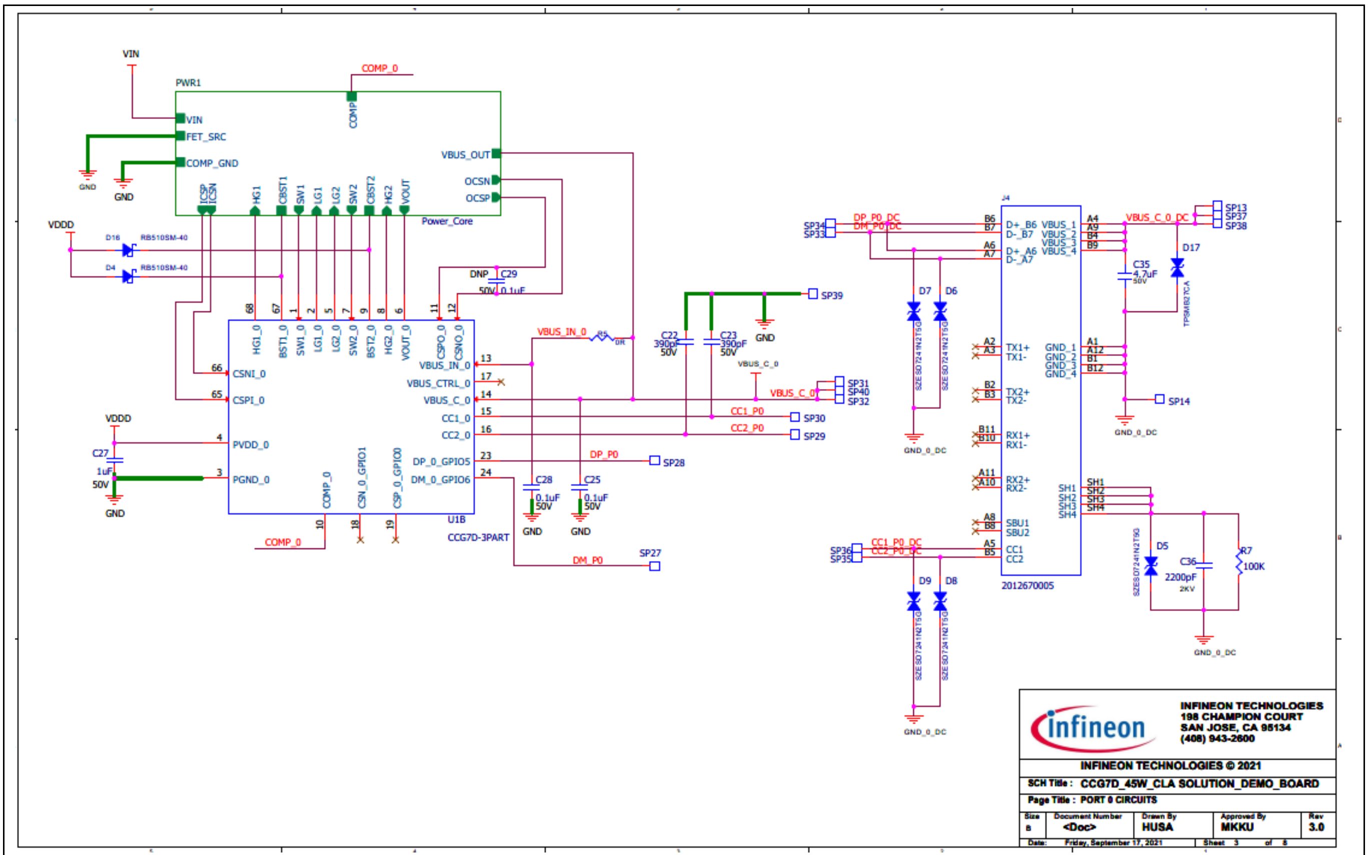
9 Circuit schematics, BOM, and PCB layout

See the following sections for cigarette lighter adapter solution demo board circuit schematics, BOM, and PCB layout:

- 9.1 CLA circuit schematics
- 9.2 CLA BOM
- 9.3 CLA PCB layout

9.1 CLA circuit schematics

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SAN JOSE, CA 95134
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Document Number <Doc>
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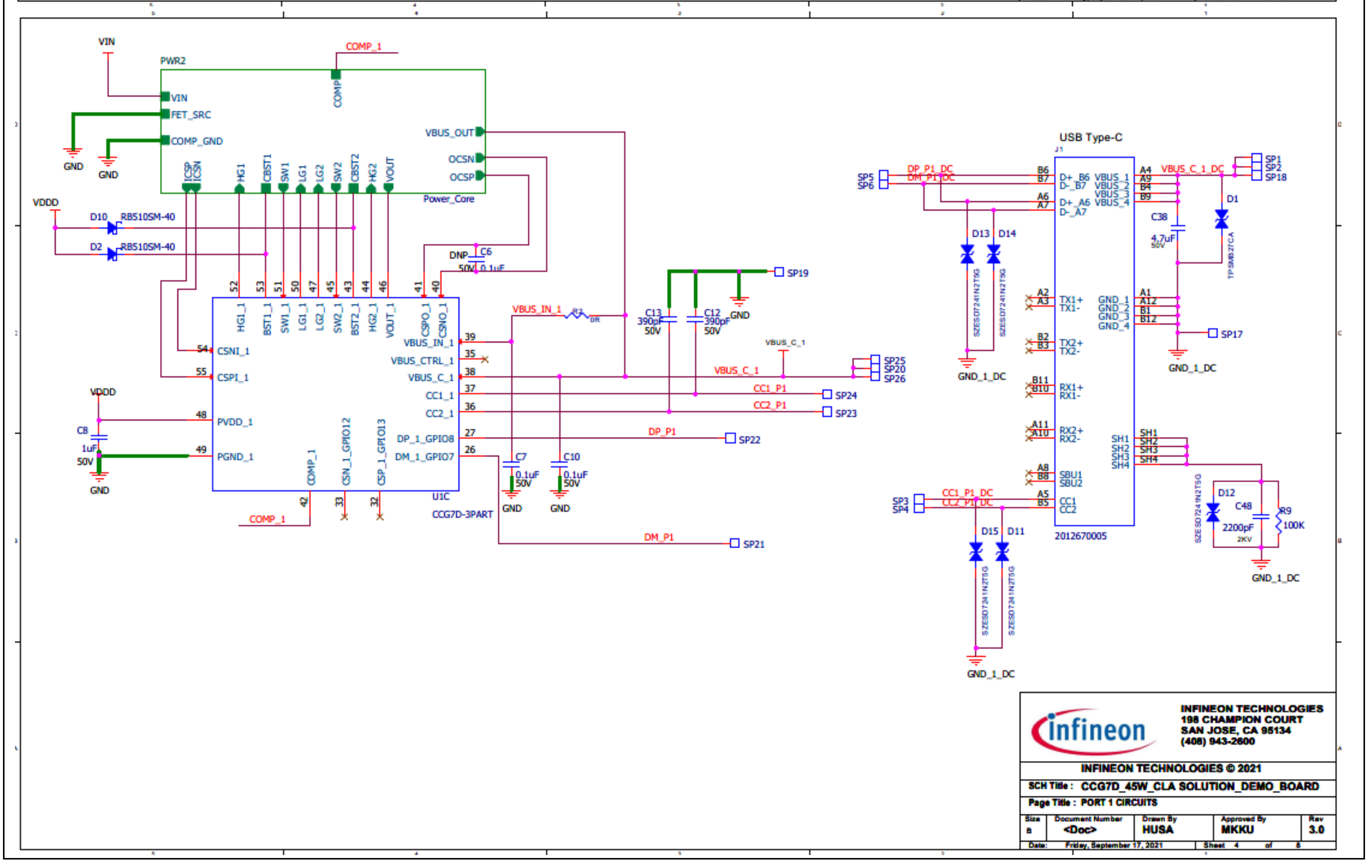
Approved By MKKU
Rev 3.0
Date: Friday, September 17, 2021
Sheet 3 of 8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SCH Title: CCG7D_45W_CLA SOLUTION_DEMO_BOARD
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Sheet 4 of 8

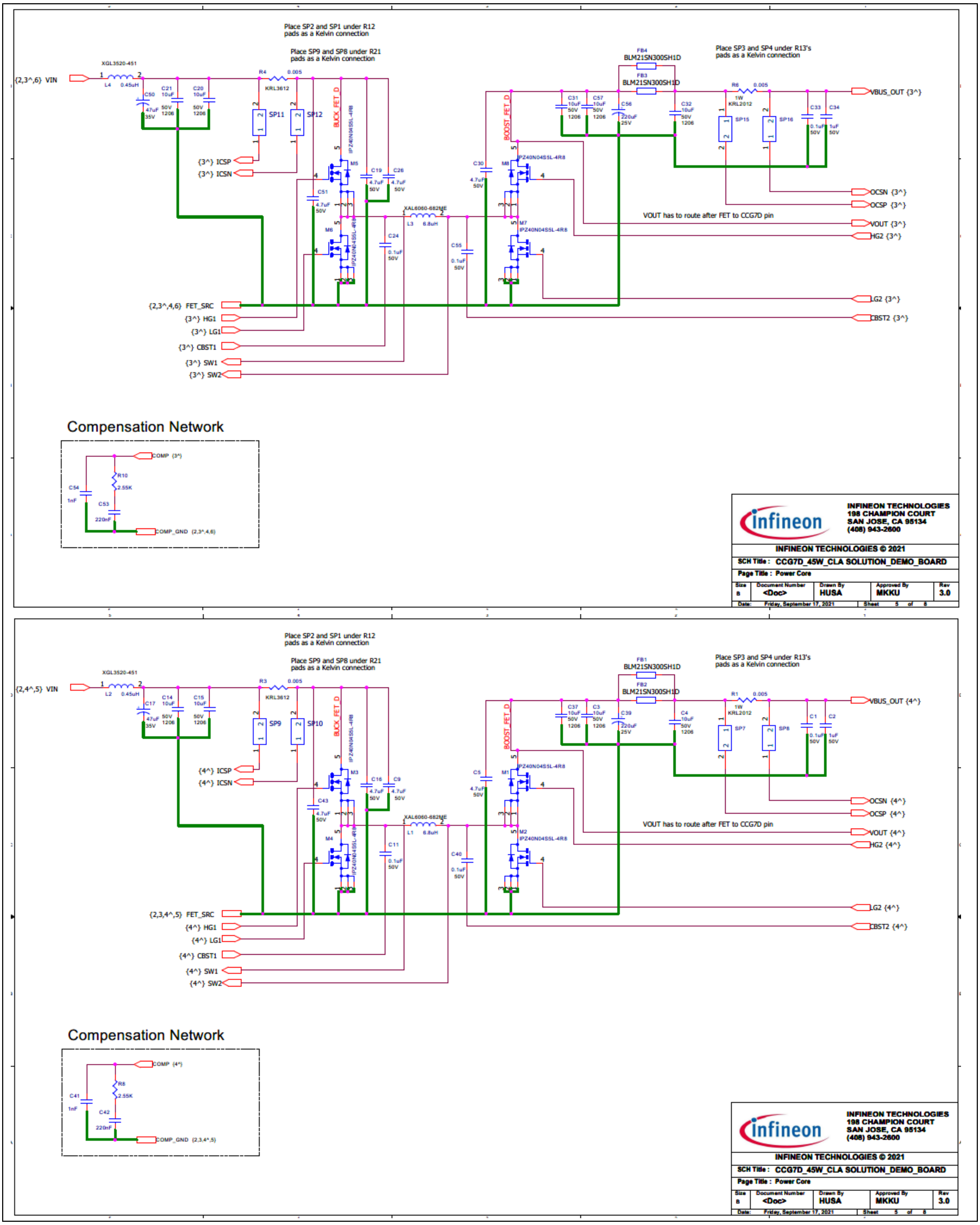


Figure 60 **CLA solution demo (SD2230) board circuit Rev3 schematics**

9.2 CLA BOM

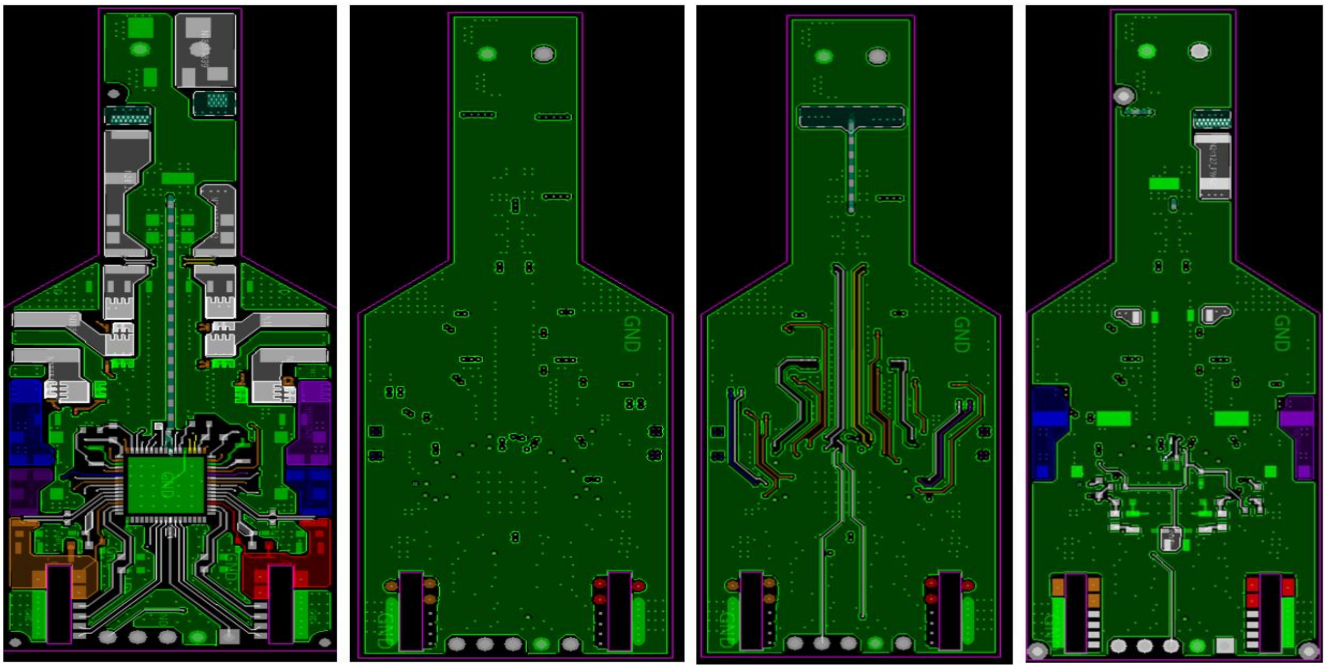
Table 29 CLA solution demo (SD2230) board bill of materials

S. No	Qty	Reference	Description	Part number	Manufacturer
1	6	C1, C11, C24, C33, C40, C55	CAP CER 0.1 µF 50 V X7R 0603	GCM188R71H104KA57J	Murata Electronics
2	8	C7, C10, C25, C28, C45, C47, C49, C52	CAP CER 0.1 µF 50 V X7R 0402	CGA2B3X7R1H104K050BB	TDK Corporation
3	10	C3, C4, C14, C15, C20, C21, C31, C32, C37, C57	CAP CER 10 µF 50 V X7R 1206	CGA5L1X7R1H106K160AC	TDK Corporation
4	1	C18	CAP CER 10 µF 50 V X7S 1210	GCM32EC71H106KA03K	Murata Electronics
5	1	C46	CAP CER 10 µF 10 V X7R 0805	C0805C106J8RACAUTO	KEMET
6	2	C41, C54	CAP CER 1000 pF 50 V C0G/NP0 0603	C0603C102F5GACAUTO	KEMET
7	4	C2, C8, C27, C34	CAP CER 1µF 50 V X7R 0805	GCM21BR71H105KA03L	Murata Electronics
8	1	C44	CAP CER 1µF 10 V X7S 0402	GCM155C71A105KE38D	Murata Electronics
9	2	C36, C48	CAP CER 1206 2.2 nF 2000 V X7R 10%	C1206C222KGRACAUTO	KEMET
10	2	C42, C53	CAP CER 0.22 µF 25 V X7R 0805	C0805C224K3RACAUTO	KEMET
11	2	C39, C56	CAP ALUM HYBRD 220 µF 20% 25 V SMD	GYC1E221MCQ1GS	Nichicon
12	4	C12, C13, C22, C23	CAP CER 390 pF 50 V C0G/NP0 0603	GCM1885C1H391JA16D	Murata Electronics
13	6	C5, C16, C19, C30, C43, C51	CAP CER 4.7 µF 50 V X7R 0805	CGA4J1X7R1H475K125AE	TDK Corporation
14	2	C35, C38	CAP CER 4.7 µF 50 V X7R 1210	C1210C475K5RACAUTO	KEMET
15	2	C17, C50	CAP ALUM POL HY 47 µF 20% 35 V SMD	GYC1V470MCQ1GS	Nichicon
16	2	D1, D17	TVS DIODE 23.1 V 37.5 V DO214AA	TPSMB27CA	Littelfuse Inc.
17	4	D2, D4, D10, D16	Diode Schottky 40 V 100 mA surface mount EMD2	RB510SM-40FHT2R	Rohm
18	1	D3	TVS diode 28.2 V 45.7 V DO214AA	TPSMB33CA	Littelfuse Inc.

S. No	Qty	Reference	Description	Part number	Manufacturer
19	10	D5, D6, D7, D8, D9, D11, D12, D13, D14, D15	TVS diode 24 V 48 V 2X2DFN	SZESD7241N2T5G	ON Semi
20	4	FB1, FB2, FB3, FB4	30 Ω @ 100 MHz 1 power line ferrite bead 0805 (2012 Metric) 8.5 A 4 mΩ	BLM21SN300SH1D	Murata Electronics
21	1	F1	Fuse board mount 15 A 32 V DC 1206	SF-1206SA1500W-2	Bourns Inc.
22	2	J1, J4	USB-C (USB Type-C) USB 3.1 (USB 3.1 Gen 2, Superspeed+) receptacle connector 24 position surface mount, right angle; through-hole	2012670005	Molex
23	1	J2	CONN HEADER VERT 5POS 2.54 mm	PRPC005SAAN-RC	Sullins Connector Solutions
24	1	J3	2 position wire to board terminal block horizontal with board 0.197" (5.00 mm) through-hole	691137710002	Würth Elektronik
25	2	L1, L3	Fixed inductors 6.8 µH 20% 8.9 A 12.7 mΩ	XGL6060-682	COILCRAFT
26	2	L2, L4	Fixed inductor 0.45 µH 20% 5.8 A 5.9 mΩ	XGL3520-201MEC	COILCRAFT
27	8	M1, M2, M3, M4, M5, M6, M7, M8	N-channel 40 V 40 A (Tc) 48 W (Tc) surface mount PG-TSDSON-8	IPZ40N04S5L4R8ATMA1	Infineon Technologies
28	2	R1, R6	5 mΩ ±1% 1 W chip resistor wide 0805 (2012 metric), 0508 automotive AEC-Q200, current sense metal foil	KRL2012E-M-R005-F-T5	SUSUMU
29	2	R2, R5	RES SMD 0Ω jumper 1/10 W 0603	ERJ-3GEY0R00V	Panasonic Electronic Components
30	2	R3, R4	RES.,0.005 Ω, 1%, 1.5 W, 1206, long-side term, KRL3216, metal, sense,	KRL3216E-C-R005-F-T1	SUSUMU
31	2	R7, R9	RES SMD 100 KΩ 5% 1/10 W 0603	ERJ-3GEYJ104V	Panasonic Electronic Components
32	2	R8, R10	RES SMD 2.55 KΩ 1% 1/10 W 0603	ERJ-3EKF2551V	Panasonic Electronic Components

S. No	Qty	Reference	Description	Part number	Manufacturer
33	1	U1	Dual-port USB-C PD AC-DC power adapter/cigarette lighter adapter (CLA)	CYPD7271-68LQXQES	Infineon Technologies
34	2	C6, C29	CAP CER 0.1 µF 50 V X7R 0402	CGA2B3X7R1H104K050BB	TDK Corporation
35	2	C9, C26	CAP CER 0.1 µF 50 V X7R 0603	GCM188R71H104KA57J	Murata Electronics
36	6	C1, C11, C24, C33, C40, C55	CAP CER 0.1 µF 50 V X7R 0402	CGA2B3X7R1H104K050BB	TDK Corporation
37	8	C7, C10, C25, C28, C45, C47, C49, C52	CAP CER 10 µF 50 V X7R 1206	CGA5L1X7R1H106K160AC	TDK Corporation
38	10	C3, C4, C14, C15, C20, C21, C31, C32, C37, C57	CAP CER 10 µF 50 V X7S 1210	GCM32EC71H106KA03K	Murata Electronics
39	1	C18	CAP CER 10 µF 10 V X7R 0805	C0805C106J8RACAUTO	KEMET

9.3 CLA PCB layout



Bottom layer　3rd layer　2nd layer　Top layer

Figure 61 CLA solution demo (SD2230-1-R3) board – main board PCB layout

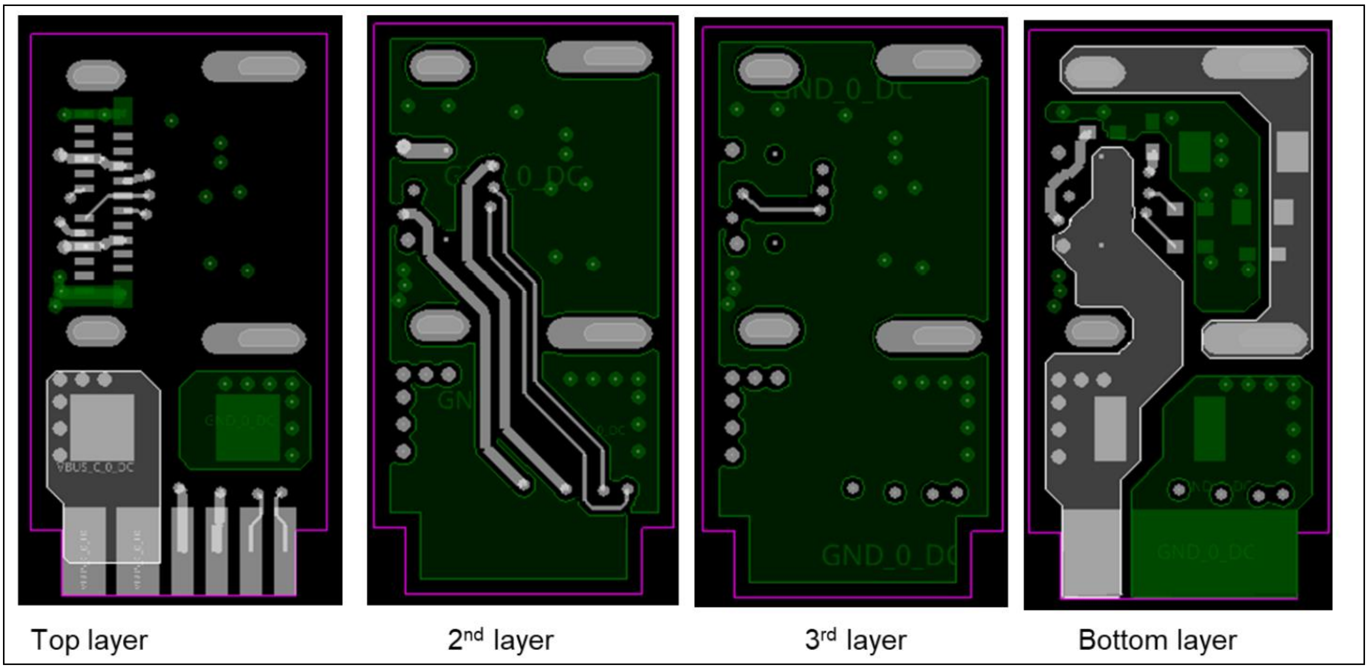


Figure 62 CLA solution demo (SD2230-2-R3) board – Port #0 Mushroom board PCB layout

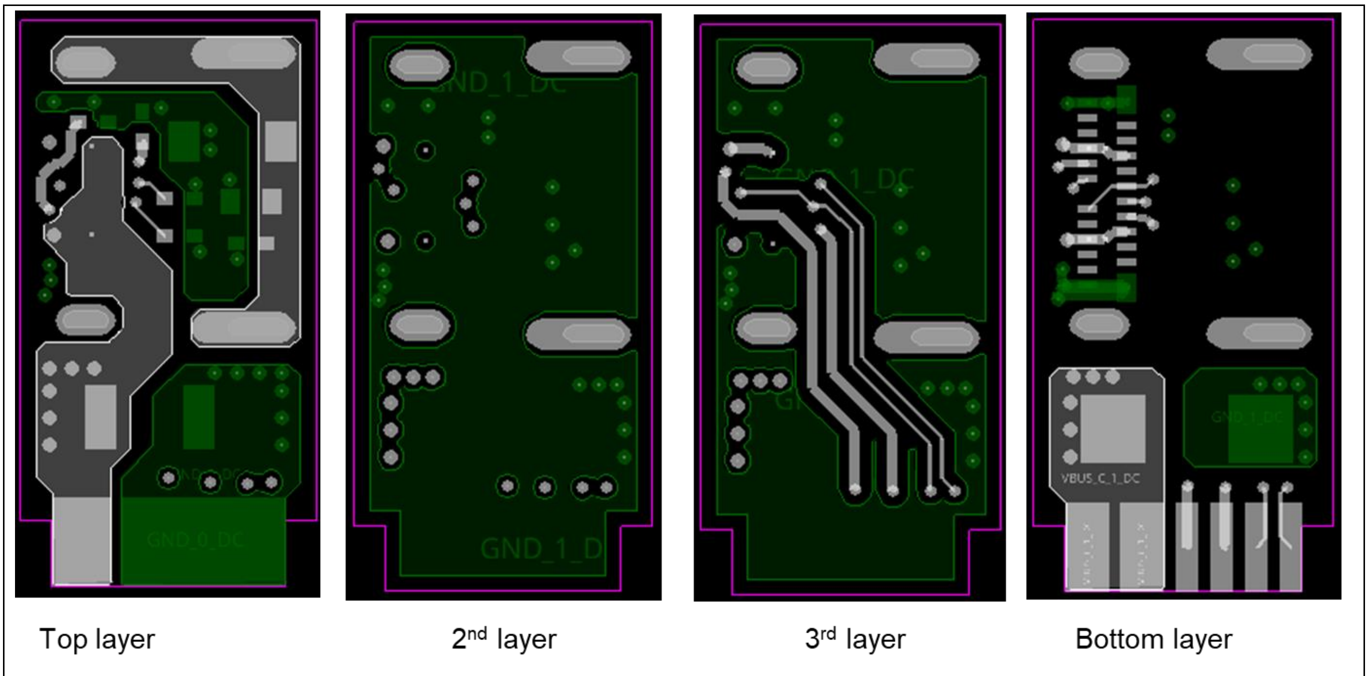


Figure 63 CLA solution demo (SD2230-3-R3) board – Port #1 Mushroom board PCB layout

10 Appendix – A: Efficiency measurement test setup

Efficiency measurements are captured with the following conditions.

- CLA board input connector to output connector; measurement points are shown in section **10.1**.

10.1 Efficiency measurement "input connector to the Type-C connector on the board"

The measurement includes, fuse, input differential mode inductor, output ferrite beads. Measurement equipment connectivity is shown in **Figure 64**.

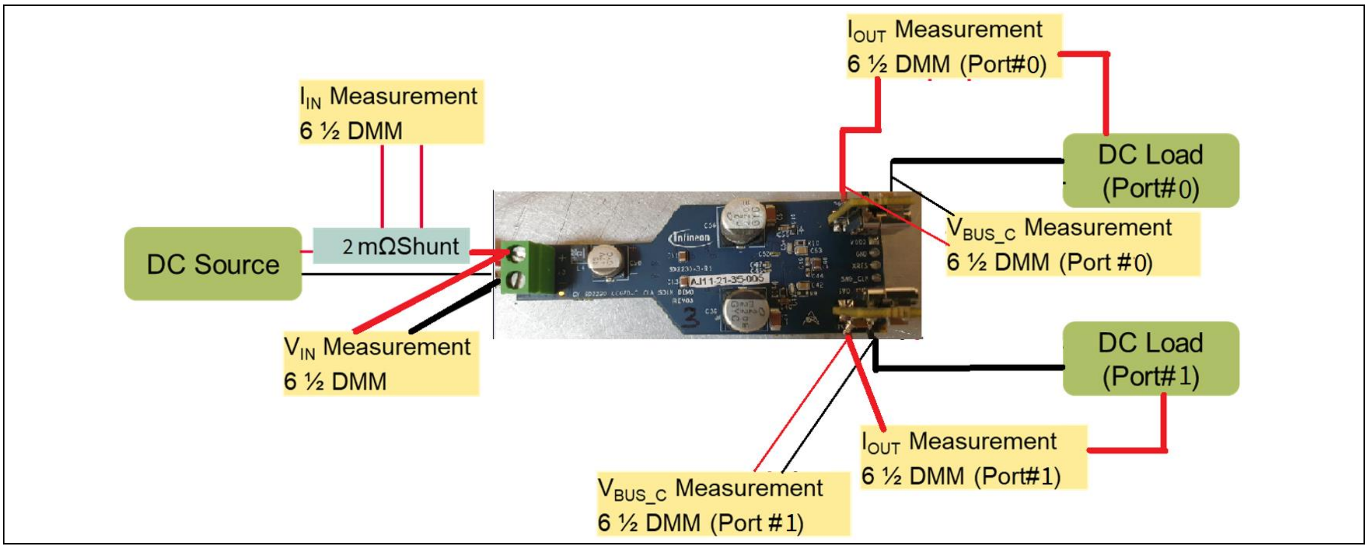


Figure 64 Efficiency measurement - "input connector to the Type-C connector on the board"

References

[1] 002-33978: Hardware design guidelines for EZ-PD™ CCG7D consumer - Cigarette lighter adapter (CLA)

[2] 002-33977: EZ-PD™ CCG7D consumer CLA power stage design calculator

[3] **EZ-PD™ Configuration Utility user manual**

[4] 002-32352: EZ-PD™ CCG7D consumer datasheet

Revision history

Date	Version	Description
2021-09-23	**	Initial release
2021-10-12	*A	Added the following sections: • **4.11.8 PWM mode transition in FCCM** • **4.13 Current consumption** • **5.3 Temperature measurement using thermocouple at elevated ambient temperature** Updated **Table 2** and **Table 3**
2022-02-07	*B	Updated **Figure 2** block diagram Updated efficiency values in **Table 7** and **Table 8** Updated efficiency graphs from **Figure 5** to **Figure 9** Updated temperature values in **Table 21** and **Table 22**
2022-03-24	*C	Updated **Table 2** and **Table 29**

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