Perspective of Loss Mechanisms for Silicon and Wide Band-Gap Power Devices

Gerald Deboy, Oliver Haeberlen, and Michael Treu

***Abstract*—With the commercial availability of GaN and SiC-based power semiconductor devices having significantly improved material characteristics, there is a need to discuss the perspective of the underlying physical loss mechanisms of these devices versus their silicon counterparts. This article will compare latest generation Superjunction power transistors versus e-mode GaN HEMTs and SiC MOSFETs in terms of semiconductor losses and their potential for further improvement. A short application section will give practical information on best matching circuits for each device concept.**

***Index Terms*—GaN HEMT, loss mechanisms, power semiconductor devices, Superjunction, wide bandgap devices.**

I. Introduction

THROUGH the introduction of the Superjunction principle [1]-[3], the characteristics of silicon based power MOSFETs could be greatly improved extending the life cycle of this technology up to now and potentially far into the future. Continuous improvement of the technology and major cost-down steps in the fabrication have made Superjunction transistors the first choice for high voltage power devices in the 500 V to 800 V domain. AC to DC power converters in a wide variety of applications such as lighting, adapter, server and telecom power supplies, and EV charging are based on Superjunction transistors as the prevailing technology utilizing a number of well-established power circuits and control methods.

With the arrival of GaN High Electron Mobility Transistors (HEMT) as a potentially game-changing technology [4] new topologies and control methods are challenging classic power supply architectures.

As it is rarely meaningful to put entirely new devices into existing sockets, it is worthwhile to analyze the underlying physical loss mechanisms both for wide band-gap devices and Superjunction transistors. Based on this loss analysis best matches in terms of circuits and control methods are identified. Starting from today's achievements we will give an outlook into further improvement potential with respect to semiconductor losses.

Section II will introduce the limit line of silicon and ways to overcome it with various device concepts. Perspectives are given to further lower the on-state resistance.

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In Section III, switching losses are derived from a physical understanding of the mechanisms inside the device. The influence of control and application circuit is discussed. Experimentally measured values are given both for e-mode GaN HEMTs and latest generation of Superjunction devices.

Based on the loss analysis Section IV suggests best matching circuits and control methods for each power device concept.

A short summary will conclude the article.

II. Device Concepts and Their Potential Towards Lowering the On-State Resistance

A. The Limit Line of Silicon

The optimization of the specific on-state resistance has always been a strong driving factor for the semiconductor industry as it allows differentiation from competition through lower $R_{DS(on)}$ in a given package as well as to lower costs through fabricating more dies on the same wafer.

In the simplest case, the dependency of the on-state resistance can be derived from the Poisson equation in a one-dimensional way as:

$$R_{on} = \frac{4BV^2}{\mu\varepsilon E_C^3}. \tag{1}$$

Modeling silicon's dependency of the critical electric field on doping concentration in an empirical way leads to the well-known formula:

$$R_{on} \approx 8.3\times10^{-9} BV^{2.5}\Omega\cdot cm^2. \tag{2}$$

This relation is known as the "silicon limit". It describes the best specific on-state resistance, which can theoretically be achieved for a given breakdown voltage in case of a one-dimensional p-n junction. It is noteworthy that the optimum doping profile is not constant as function of depth, but shows an increase towards the drain electrode [5] following a hyperbolic sine function. Practically, margins need to be considered both for voltage and $R_{DS(on)}$. Commercial products are therefore typically 20% or more above the limit line [6].

Improvements beyond this barrier have been the subject for research for many decades. In principle there are three fundamental concepts:

1) Changing the material system towards wide band-gap. SiC MOSFETs and JFETs follow this path.

2) Breaking away from the limitations of the one-dimensional Poisson equation by introducing two- or three-dimensional structures. Superjunction devices and field plate (or shielded gate) concepts are classic representatives.
3) Overcoming the relationship between doping and conductivity as expressed in the Poisson equation through doping-independent conduction. The two-dimensional electron gas of GaN lateral high electron mobility transistors proves this concept.

B. Wide Band-Gap Devices

(1) highlights, with its strong dependency on the critical electric field, the motivation to move into wide band-gap materials. The energy required for band-to-band electron-hole generation through impact ionization is much higher; the breakdown field e.g. in SiC with triple the band-gap (3.26 eV vs. 1.12 eV) is hence nearly a factor of 10 higher compared to silicon (2 MV/cm vs. 0.25 MV/cm). Taking further into account mobility and dielectric constant as expressed in the Baliga Figure-of-Merit (FoM), the limit line for SiC is 231 times below the silicon limit. The same rational applies for one-dimensional vertical GaN devices with a FoM advantage of 2097 [7]. Practically, the channel contribution, contact and substrate resistances, the re-distribution of current (especially in planar gate concepts), and last-but-not-least the ruggedness requirements such as short circuit operation [8] are barriers on the way towards the theoretical limits.

C. Two-dimensional Devices (2D)

Two-dimensional devices introduce an electric field component perpendicular to the direction of current flow. Conductivity in the on-state and blocking characteristic are hence no longer coupled through the Poisson equation.

As shown in Fig. 1, Superjunction transistors lower the specific on-state resistance through a compensation structure formed by p-doped pillars placed adjacent to the n-type current conducting regions, thus allowing much higher doping levels in the n-regions.

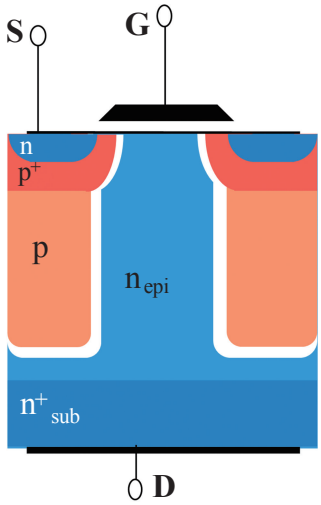

Fig. 1. Vertical Superjunction transistor with planar gate structure.

The p-pillars do not contribute to current conduction in the on-state, but help to maintain the blocking voltage during the off-state by compensating the donor charges in the n-columns. The blocking characteristic depends on the effective doping level, that is, donor charges minus acceptor charges, while the on-state resistance depends on the n-doping level alone. The concept allows therefore an optimization of the area-specific on-state resistance far below the silicon limit. As the adjacent p- and n-columns create a horizontal component of the electric field, an increase of doping level needs to be accompanied by reduction of the cell pitch to stay within the limits of the critical electrical field. The overall electric field is given by a superposition of horizontal and vertical field vectors. The relationship between blocking voltage and $R_{DS(on)}$ [3] can now be expressed as:

$$R_{on} \cdot A_V = 4 \cdot w \cdot \frac{V_B}{\mu \cdot \varepsilon \cdot E_C^{\,2}}. \tag{3}$$

This formula shows a significantly more favorable dependency between on-state resistance and breakdown voltage. Modelling the doping dependence of the critical electrical field in a similar way as described above gives $R_{on} \cdot A_V \approx V_B^{1.3}$ instead of $R_{on} \cdot A_V \approx V_B^{2.5}$ as expressed in (2). The direct proportionality to the cell pitch w, enables a continuous path towards ever lower on-state resistance. Fig. 2 shows this race towards lower R_{on} and the hitherto achieved results.

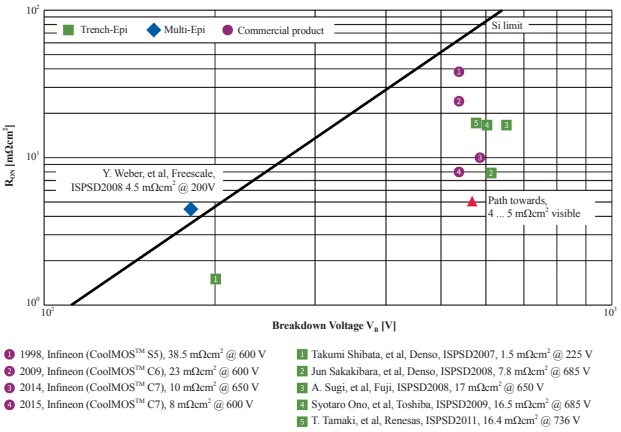

Fig. 2. Specific on-state resistance for different Superjunction devices using Trench Epi and Multi-Epi processes against the limit of silicon.

As the blocking capability of the device depends crucially on the local difference of charges, an elaborate scheme is required to control doping levels both in the p- and n-column precisely during mass production. In order to reduce the on-state resistance below the silicon limit, doping levels in the n-column in the upper 10^{15} cm^{-3} to lower 10^{16} cm^{-3} range are necessary, whereas a high blocking capability such as 600 V, mandates an effective doping level below 1 to $2 \cdot 10^{14}$ cm^{-3}. The relative difference of charges must be balanced within few percent of their absolute doping levels. A surplus of donor charges turns

the drift layer into a lightly n-doped area, a surplus of acceptor charges into a lightly p-doped area. Consequently, with constant doping profiles, the gradient of the vertical electric field changes its sign, moving the point of highest electric field from the top side to the bottom side of the device. Such a characteristic may create instabilities and must be avoided. Hence, constant doping profiles for p-and n-columns are not favorable [9].

In terms of manufacturing technology the subsequent deposition of epitaxial layers with intermediate implantation steps has proven to be compliant both with these needs and has paved a way towards an area specific on-state resistance below 10 $m\Omega \cdot cm^2$. Alternative concepts comprise trench etching and epitaxial re-fill of trenches. In this case grading of doping profiles need to be controlled through the taper angle of the trench.

From our view point refining production technology and device concept will allow further improvements down to an area specific on-state resistance in the range of 4 to 5 $m\Omega \cdot cm^2$. Besides production tolerances, early depletion of the current-conducting n-columns may pose a final limit to the Superjunction principle as pointed out by Disney and Dolny [10]. For more background on the history and further use cases of the Superjunction principle, we refer the reader to a recently published article by Udrea *et al.* [11].

The field plate concept is another representative of two-dimensional device concepts. The horizontal field component is created between a metal or quasi-metallic electrode being isolated from the drift region through a thick oxide. Being typically connected to the source electrode, the field plate helps to deplete the n-doped mesa region. Similar to Superjunction transistors, the n-doped region can be significantly higher doped than possible under the limitations of the one-dimensional Poisson equation. Another advantage of the concept is that the field plate shields the gate electrode, which is typically being fabricated within the same trench. The overlap between gate and drain electrode is therefore minimized. The concept is therefore not only beneficial for the on-state resistance, but also for the gate-to-drain capacitance. This makes this structure the preferred technology for power MOSFETs with low to medium breakdown voltages such as 25 V to few hundred volts. Since its introduction the area-specific on-state resistance has been lowered a factor of 50 versus planar silicon power MOSFETs and roughly one order of magnitude versus early implementations of the concept.

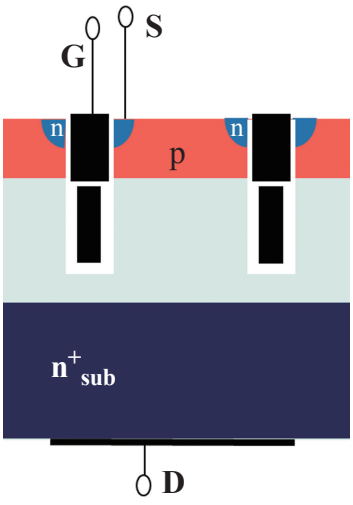

Fig. 3. Vertical power MOSFET with field plate.

Towards higher breakdown voltages the structure is limited by the thickness of the oxide around the field plate, which poses a barrier towards reduction of the pitch and technological challenges. Recent technology analysis has shown that the cross-over point in terms of on-state resistance between field plate and Superjunction concept is located between 300 V and 400 V. Fig. 3 shows the basic structure.

D. GaN High Electron Mobility Transistor

The third way to break the limit line of silicon is one of the most challenging but also the most rewarding. Stacking AlGaN on GaN forms a spontaneous charge layer at the interface due to the differences in polarization between the two materials. The charge is confined in the third dimension on the one hand by the bandgap difference at the hetero junction and on the other hand by the band curvature. Hence a two-dimensional charge sheet is created at the interface without any doping in which electrons can move freely. This so-called two dimensional electron gas (2DEG) is the basis for GaN High Electron Mobility Transistors (GaN HEMT). The concentration of the electrons is defined by the mismatch in polarization and can be adjusted through concentration and thickness of the AlGaN barrier.

Contacting this electron gas and controlling the current flow through a gate electrode forms high performance lateral transistors with very high electron mobility and the potential towards unrivalled low area-specific on-state resistance. As the electron gas conducts at zero gate bias, GaN HEMTs yield naturally normally-on transistors. Consequently, effort is required to turn transistors into normally-off or enhancement mode (e-mode) devices as the majority of power electronic applications are voltage source converters. Two major concepts have been commercially introduced to the market: MISFETs, where the AlGaN barrier is locally thinned and the gate electrode is insulated from the 2DEG through a very thin dielectric layer and p-GaN gate transistors having a p-n junction between gate and the 2DEG. The latter concept exists in two variants: the p-GaN gate injection transistor used by Panasonic and Infineon operates with an ohmic contact to the p-GaN gate. It requires a low bipolar current to clamp the gate to a positive forward bias during the on-state of the transistor, but has the unique advantage, that it can tolerate several amperes of forward current thus limiting effectively any voltage spikes on the gate [12]. The second variant of the p-GaN gate concept operates with a Schottky contact to the gate, which yields a low gate current but has issues with a high susceptibility to gate rupture through voltage spikes.

Besides devices showing a normally-off characteristic on

die, also normally-on or depletion mode transistors are commercially available. In this case the transistors are turned into normally-off through a cascode circuit, where a series low voltage MOSFET switches the source of the HEMT with the gate electrode of the HEMT being connected to the source of the LV FET. Even though driving the cascode is easy, we believe that the bigger potential is with e-mode devices. First, the series low voltage MOSFET adds capacitance and complexity deteriorating especially FoMs for charge of the output capacitance; second, power devices require essentially slew rate control. Hence, direct gate access as provided by the e-mode concept is preferred to the indirect switching of the cascode.

Fig. 4 shows an e-mode GaN HEMT and its electric symbol, Fig. 5 shows the cascode circuit.

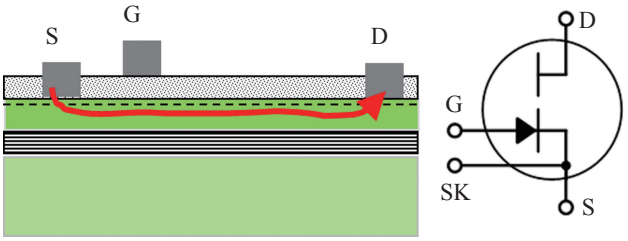

Fig. 4. Structure of lateral GaN HEMT and electrical symbol of the e-mode GaN HEMT.

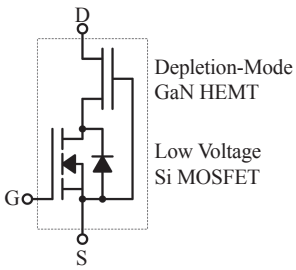

Fig. 5. Electric circuit for depletion mode GaN HEMT (cascode).

The relationship between on-state resistance and breakdown voltage does not follow the theory for vertical power devices but is much closer to the theory for silicon-on-insulator devices as formulated by Zingg [13]. In case of constant density of the 2DEG, the field distribution along the drift zone can be compared to one-dimensional RESURF devices. Characteristic are two distinct peaks of the electric field at the gate electrode and the drain contact. Further device optimization can therefore follow the ideas developed for lateral RESURF devices [14]. Fitting a curve to published experimental values of R_{DS}(on) and breakdown voltage suggests a dependency $R_{ON} \cdot A_V \approx V_B^{1.3}$ similar to the relationship derived for Superjunction transistors. Fig. 6 shows the corresponding graph in comparison to the vertical limit lines of silicon, SiC and GaN, where data points are taken from [7].

Obviously, there is large improvement potential from today's state-of-the-art towards fundamental limit lines making GaN HEMTs a very interesting candidate for significant

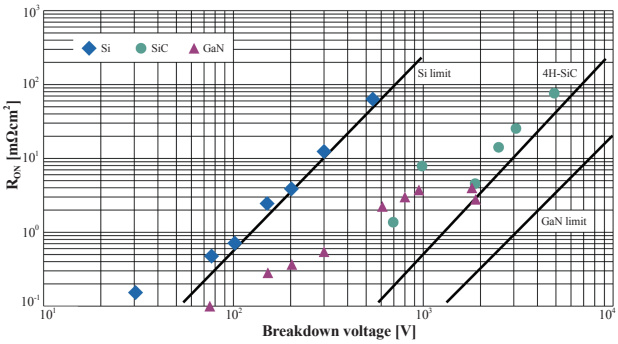

Fig. 6. Reported values for area specific on-state resistance for GaN HEMTs and SiC in comparison to material specific limit lines for vertical devices [7].

reduction in terms of $R_{on} \cdot A$ and cost.

III. Switching Losses With Special Emphasis on Wide Bandgap and Superjunction Power Devices

We will group switching losses into three distinct categories: turn-off losses, turn-on losses, and soft switching losses. We will not consider gate drive losses, as these losses are comparatively small for high voltage devices, being the main scope for this article.

A. Turn-off Losses

Fast switching power devices, such as Superjunction, GaN HEMT, or SiC devices, are able to come at least close to the theoretical limit of switching losses during turn-off. The minimum turn-off loss being recorded at the terminals as overlap of current and voltage is the energy stored in the output capacitance [15]. In this case, the channel - be it a MOS channel or a bipolar Gate-injection structure such as in e-mode GaN HEMTs - is turned off before the voltage across drain to source rises. The load current commutates into the output capacitance charging it from zero Volts up to the DC link voltage. If this mechanism is lossless - we will see later that this is not entirely true - the energy, observed on the oscilloscope as overlap between voltage and current, equals the energy E_{oss}, a value which is typically given in the datasheet. It is noteworthy that the energy stored in the output capacitance should be derived from large signal analysis not from small signal due to hysteresis effects especially in Superjunction devices [16], [17].

If we turn-off in this way, physically speaking, no energy is yet dissipated. The current inside the device flows as a capacitive displacement current not as a drift current. That means that the space charge layer inside the device structure builds up by carriers moving away from the boundary of the space charge layer towards the contacts. In case of a Superjunction transistor, electrons will move within the n-columns to the drain, holes will move within the p-columns to the source contact leaving a depleted zone behind. The key point is that these carriers are not crossing any space charge layer. They should always flow as majority carriers within unde-

pleted areas. The turn-off mechanism is hence in the ideal case entirely lossless. The energy stored in the output capacitance is dissipated when the device is turned on under voltage unless an external circuit provides zero voltage switching conditions. The energy stored in the output capacitance is therefore a good indicator on the strength of a power device to achieve low overall switching losses. Especially for hard switching circuits such as Continuous Current Modulation (CCM) for e.g. Power Factor Correction (PFC) applications, improvements in the energy stored in the output capacitance lead directly to corresponding lower overall losses and better efficiency.

Even though fast turn-off is desirable from an efficiency perspective, there are several drawbacks to this concept. There is basically no slew rate control as the voltage rise dv/dt (4) is defined by the load current and the shape of the output capacitance.

$$dv/dt = \frac{I_l}{C_{oss}} \tag{4}$$

Reducing the output capacitance especially on the high voltage end helps to reduce the energy stored in the output capacitance, but makes the device inevitably faster switching. This is especially true for Superjunction devices and GaN HEMTs. Both devices have the capability to switch at a speed of far greater than 100 V/ns.

In abnormal conditions such as an AC cycle drop in a PFC stage or a secondary side short circuit on a LLC converter, very high currents may occur, leading to excessive high dv/dt. These high slew rates may create issues with EMI or induce parasitic oscillations, which may potentially destroy the power device.

In many cases, the switching speed must be limited. The most effective and most common way is to use a gate resistor, which limits the current for charging and discharging the gate capacitance of the device. Turning off the MOS channel takes a little bit longer. The control is now implemented through the reverse capacitance C_{gd}. The slew rate is expressed as (5) with gate current I_g, gate resistor R_g, and Miller plateau voltage V_{MP}. By varying R_g the slew rate can be controlled accordingly. During the Miller plateau phase, the voltage across drain to source V_{DS} rises; the entire gate current flows through the reverse capacitance C_{gd}, the gate voltage V_{GS} does not change. After this plateau, the voltage has reached the DC link voltage and the current starts to fall. The device is controlled in this period by the discharging of the input capacitance below the Miller plateau voltage and the corresponding transconductance of the power device.

$$dv/dt = \frac{I_g}{C_{gd}} = \frac{V_{MP}}{R_g \cdot C_{gd}} \tag{5}$$

Fig. 7 shows these behaviors in an ideal manner without any parasitics.

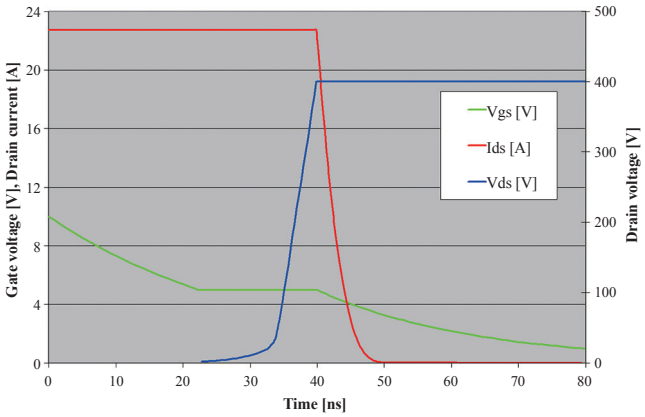

Fig. 7. Ideal turn-off of a power device by controlling the turn-off speed by the gate current flowing through the reverse capacitance C_{gd}.

Ideally, the gate resistor is chosen in such a way, that in normal operation conditions, optimum lossless turn-off is maintained, but at high peak currents both dv/dt and di/dt is controlled. In this way, both safe operation and best efficiency is achieved.

Fig. 8 shows resulting di/dt and dv/dt slew rates as a function of load current and gate resistor for a 190 mΩ Superjunction device (CoolMOS™ CP). Limiting, for example, di/dt below 2000 A/µs and dv/dt below 60 V/ns requires a gate resistor of around 20 Ω. For load currents below 5 A di/dt and dv/dt is still linearly increasing with load current. Control follows hence the lossless charging of the output capacitance. At higher currents, however, the control is shifted into C_{gd} control with corresponding limitations on dv/dt and di/dt.

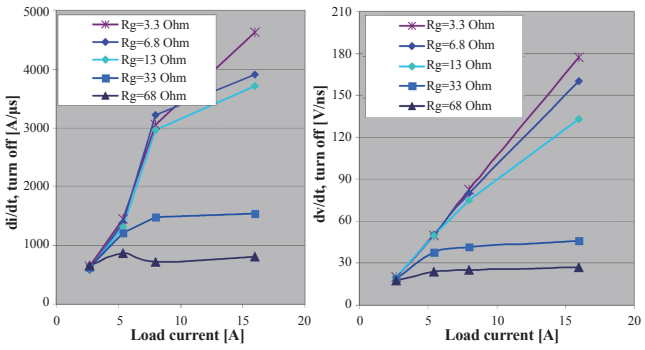

Fig. 8. Slew rated di/dt (left) and dv/dt (right) as function of load current and gate resistor during turn-off, Superjunction device 600 V / 190 mΩ.

Recent Superjunction generations have been optimized to allow this combined control seamlessly with minimum effect on efficiency. Fig. 9 shows the turn-off losses as function of load current for the latest generation of Superjunction devices (CoolMOS™ C7).

As shown in Fig. 9 using, for example, a gate resistor in the range of 10 Ω allows minimum turn-off losses close to the theoretical limit for a current range up to 15 A.

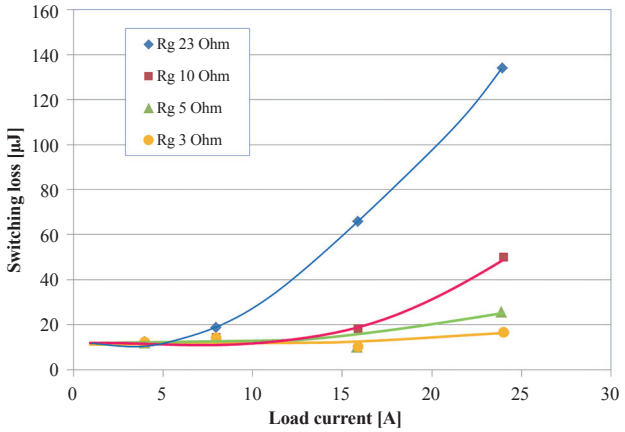

Fig. 9. Turn-off loss of a 60 mΩ / 600 V rated Superjunction device as function of current and gate resistor switching against a 6 A SiC Schottky barrier diode.

B. Turn-on Losses

Turn-on losses can be divided into two major contributions: one loss source arises from parasitic capacitances of the switching cell circuit, and a second loss source comes from shortening the output capacitance of the power device itself. A switching cell consists fundamentally of the switch, a freewheeling element, and at least an input capacitor. In case of a boost converter the freewheeling element is a diode, preferably a SiC Schottky barrier diode, or in case of a synchronous boost, a power MOSFET such as Superjunction or GaN HEMT. In case of a flyback, the freewheeling element is a synchronous MOSFET or a diode on the secondary side of the transformer.

In hard switching conditions the charge of the freewheeling element is added to the load current causing a characteristic current peak. Fig. 10 shows an example of a 70 mΩ GaN HEMT half bridge device arranged in a symmetric half bridge. Both turn-on and turn-off show very linear di/dt and dv/dt slopes. The turn-off waveform demonstrates perfect shut-off of the channel before the voltage rises, thus bringing

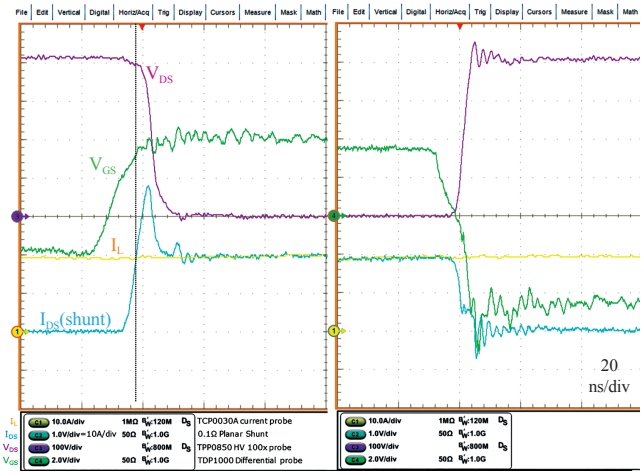

Fig. 10. Turn-on and turn-off waveform of a 70 mΩ / 600 V rated e-mode GaN HEMT arranged in a symmetric half bridge.

the turn-off loss very close to its theoretical minimum. It is noteworthy, that GaN offers such loss-less turn-off at a time scale of just a few ns.

The losses from the freewheeling element amount in total to $Q_{oss} \cdot V_{DC}$ as a minimum with Q_{oss} being the charge stored in the output capacitance of the freewheeling element. The distribution of this loss into the device turning on and the freewheeling element respectively is given by the voltage dependency of Q_{oss}. Whereas Superjunction devices basically deliver the entire Q_{oss} at very low voltage, GaN HEMTs show a more favorable dependency with losses roughly evenly split between both devices in the half bridge. Fig. 11 shows the Q_{oss} curves of advanced Superjunction versus an e-mode GaN HEMT.

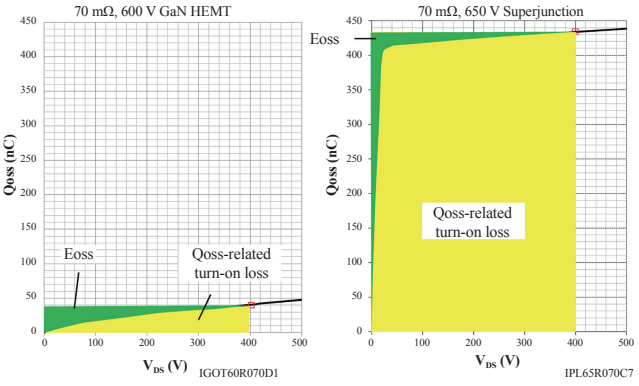

Fig. 11. Comparison of Q_{oss} versus voltage for an e-mode GaN HEMT (left) to an advanced Superjunction device (right).

The Q_{oss} curve represents the losses associated from the freewheeling element as yellow shaded area. These losses can be expressed as:

$$E_{Qoss} = \int_0^{V_{DC}} Q_{oss}(V) \cdot dV \,. \tag{6}$$

Similarly, the losses associated with short-circuiting the output capacitance E_{oss} can be seen as green shaded area in the same graph [18]. Despite GaN HEMTs having nearly a factor 10 lower Q_{oss} in comparison to Superjunction, the energy E_{oss} is in the same order of magnitude. The losses originating from E_{oss} can be expressed as:

$$E_{Eoss} = \int_0^{V_{DC}} C_{oss}(V) \cdot V \cdot dV \,. \tag{7}$$

The output capacitance should be derived from large signal analysis. The strong non-linear shape of the output capacitance of Superjunction devices leads to a very good optimization of E_{oss}-associated losses, which is a prerequisite for hard-switching circuits with SiC Schottky barrier diodes or silicon-based ultra-fast diodes as freewheeling elements. GaN HEMTs will in addition also perform perfectly well in symmetrical half bridges, where Superjunction devices can only be used with external circuitry providing zero voltage conditions.

A third contribution of turn-on losses comes from the inevitable overlap of load current with voltage. Assuming constant dv/dt and di/dt slopes these losses can be modeled as:

$$E_{I-V} = \frac{1}{2} \cdot \left(V_{DC} \cdot \frac{I_L^2}{dI/dt} + I_L \cdot \frac{V_{DC}^{\ 2}}{dV/dt} \right). \qquad (8)$$

This formula gives an interesting insight into the necessity for fast switching to optimize losses. As long as both di/dt and dv/dt increase linearly with load current, turn-on losses from the overlap of current and voltage will increase only linearly with load current. The efficiency of a power converter with losses only linearly increasing with load is constant. If, however, di/dt or dv/dt needs to be limited, losses will increase parabolically; the converter efficiency will correspondingly decrease as function of load.

It is hence of utmost importance to optimize layout and parasitic inductances of the switching cell to take the maximum benefit of modern power devices with their intrinsic capabilities to reduce switching losses. SMD packages such as TO-leadless or at least packages with separate source bond wire (Kelvin contact) such as 4-pin TO 247 will be mandatory to tap into the performance advantages of modern power devices.

Fig. 12 shows turn-on, turn-off, and sum of switching losses for an e-mode GaN HEMT arranged in a symmetric half bridge.

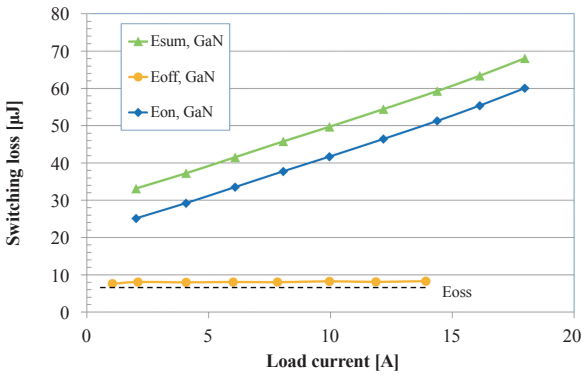

Fig. 12. Turn-on, turn-off, and sum of switching losses of a 70 mΩ / 600 V rated e-mode GaN HEMT arranged in a symmetric half bridge.

In the considerations above we assumed unipolar current transport in the freewheeling element. This is both true for GaN HEMTs and for SiC Schottky barrier diodes, however false for Superjunction devices. In reverse direction the intrinsic body diode of the device (see Fig. 1) will conduct and will flood the voltage supporting zone with electron hole plasma. In hard switching symmetric half bridges, there will be hard commutation of this conducting body diode. Due to the device structure of Superjunction devices with its deep p-columns, the electron-hole plasma needs to be entirely removed before the device blocks voltage. This effect leads to a very high reverse recovery peak and a snappy discontinuation of the reverse recovery current with very high di/dt values. Fig. 13 shows a comparison of the hard commutation behavior of a Superjunction device in comparison to an e-mode GaN switch.

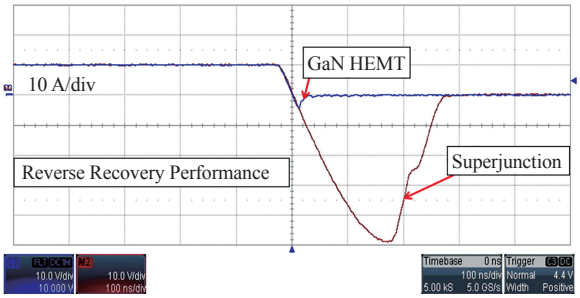

Fig. 13. Comparison of the reverse recovery behavior of an e-mode GaN HEMT in comparison to a Superjunction device.

The amount of reverse recovery charge can be reduced through reduction of the ambipolar carrier life time leading to overall lower losses. The device can be made rugged to ensure survival during hard commutation events (e.g. CoolMOS™ P7); the snappiness of the body diode however will always remain.

Taking these additional Q_{rr} losses into account, Superjunction devices are ruled out for symmetric half bridge circuits unless external circuitry is provided for zero voltage switching. We will discuss examples of these circuits in Section IV.

C. Perspective of Switching Losses

All power devices discussed in this article, be it based on silicon using field plate, on the Superjunction concept, or on wide bandgap materials, have the possibility to switch at several thousand amperes per microsecond and at dv/dts beyond 100V/ns. Losses arising from the overlap of current and voltage can hence be minimized to limits given by EMI and layout parasitics.

With GaN HEMTs, and to some extent with SiC MOSFETs, (near) Q_{rr}-free devices exist.

The energy stored in the output capacitance, E_{oss}, can be reduced further with every technology step. Fig. 14 shows a comparison of the output capacitance of three consecutive technology nodes of Superjunction devices versus an e-mode GaN HEMT.

The continuous race for lower area specific on-state resistance shifts the output capacitance into more pronounced non-linearity with every generation. This trend helps to reduce the energy stored in the output capacitance, yielding lower switching losses and better efficiency in hard switching applications. However, the devices inherently switch faster at the same load current. Furthermore the turn-off delay time, an important feature for resonant applications, increases.

GaN HEMTs show, in comparison, a near linear shape of the output capacitance which is reflected in and extremely linear switching waveform with near constant dv/dt as

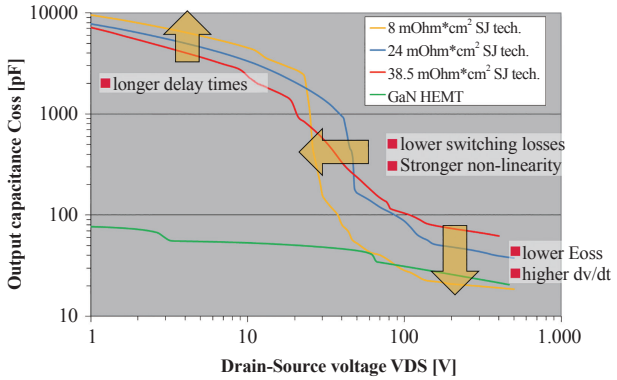

Fig. 14. Development of the characteristic output capacitance of three consecutive technology nodes of Superjunction device in comparison to an e-mode GaN HEMT.

shown in Fig. 10. The comparison of the energy stored in the output capacitance is given in Fig. 15.

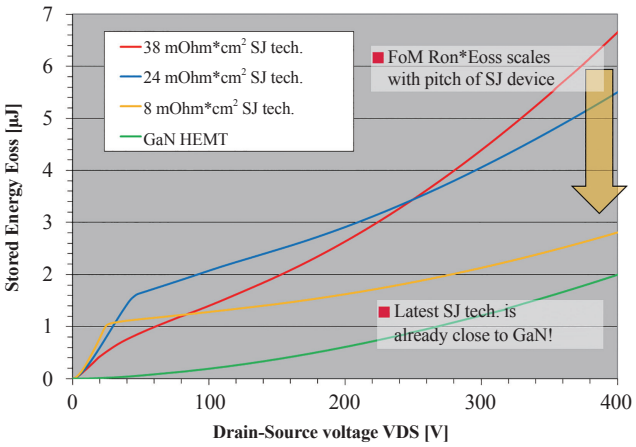

Fig. 15. Trend for the energy stored in the output capacitance across three consecutive generations of Superjunction devices in comparison to GaN HEMTs.

The latest generations of Superjunction devices are already reaching the E_{oss} levels of GaN HEMT devices. With every generation E_{oss} will further decrease. The path down towards 4 to 5 mΩ·cm^2 will hence coincide with a reduction of the E_{oss} of another factor of 2. Obviously, improvements in GaN device concept and technology will also result in a lowering of the energy stored in the output capacitance.

The outlook into the primary intrinsic loss mechanism for power device is hence bright both for Superjunction and wide bandgap devices.

All device concepts allow, in hard switching applications, superior performance. Superjunction devices are best when switched against SiC Schottky barrier diodes. Wide bandgap devices, GaN HEMTs and SiC MOSFETs, can be switched in a symmetric half bridge configuration.

In soft switching applications, where an external circuit ensures zero voltage transition, the sum of turn-on and turn-off losses can be significantly below the E_{oss} limit. As the turn-off mechanism is, physically speaking, lossless and the voltage is reduced to zero volts prior to turn on of the device, the only remaining losses are arising from secondary effects such as charging and discharging of internal capacitances and from lumped resistances e.g. in the device contact areas. Fig. 16 shows the sum of hard switching losses versus soft switching losses and the theoretical limit line of E_{oss} for the latest generation of Superjunction devices.

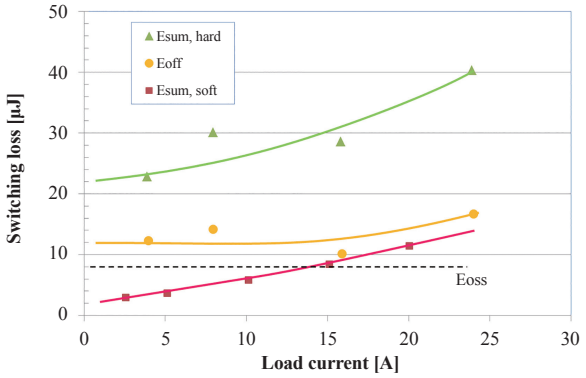

Fig. 16. Comparison of the sum of soft switching losses versus hard switching losses and the energy stored in the output capacitance, E_{oss}. 600 V rated device, 60 mΩ, switching against 6 A SiC Schottky barrier diode.

As long as turn-off losses are constant (up to around 15 A for the 60 mΩ / 600 V rated device) the sum of soft switching turn-on and turn-off losses stays clearly below the E_{oss} limit line. The linear increase of losses in this range can be attributed to charging and discharging the output capacitance and reflects increasing losses due to an increasing dv/dt slew rate. Beyond 15 A additional losses from turn-off are added as the channel is now not completely turned off before the voltage across the device rises.

Fig. 17 shows a comparison of round-cycle soft switching losses of Superjunction, GaN HEMT and SiC MOSFET measured with a novel calorimetric approach [19]. The level of loss energies of all device concepts is with a few µJ quite similar. The GaN HEMT not only shows the lowest losses but will offer the greatest improvement potential for the future with respect to soft switching losses.

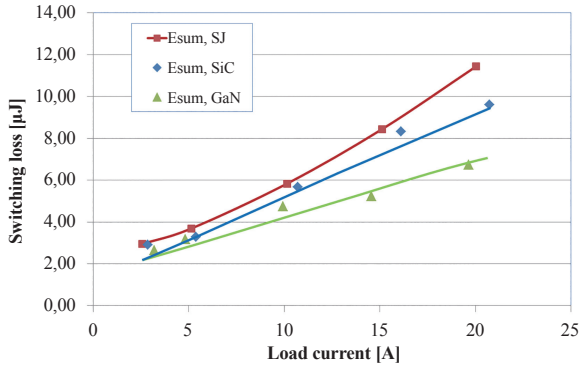

Fig. 17. Comparison of soft switching losses for Superjunction, GaN HEMT and SiC MOSFET, taken from [19].

IV. Device Concepts and Their Best Matching Application Circuit

The key for a true comparison of devices in the application is to choose appropriate circuits and control methods, which bring out the best performance of the individual device concept. As we discussed in the previous sections, Superjunction performs best when switching versus a SiC Schottky barrier diode as freewheeling element. Alternatively, good results are found in zero voltage switching applications at low to medium high switching frequency (30 to 300 kHz). GaN HEMTs can be used in hard switching applications due to their true zero reverse recovery charge. SiC MOSFETs still show some reverse recovery charge even though the ambipolar carrier life time is extremely short. Nevertheless, even for a GaN HEMT the Q_{oss} related charge is roughly a factor 5 higher than the corresponding charge of a SiC Schottky barrier diode. Switching frequencies for hard switching half bridges need hence to be chosen appropriate to keep Q_{oss} related switching losses comparatively low.

Fig. 18 shows the classic Continuous Current-Mode (CCM) boost stage, which is the prevailing topology for many switch mode power supply applications. As a result, as shown in Fig. 19, a peak efficiency of 98.5% and full load efficiency above 98% is achieved when this circuit is used with the latest generation of Superjunction devices and SiC Schottky barrier diodes.

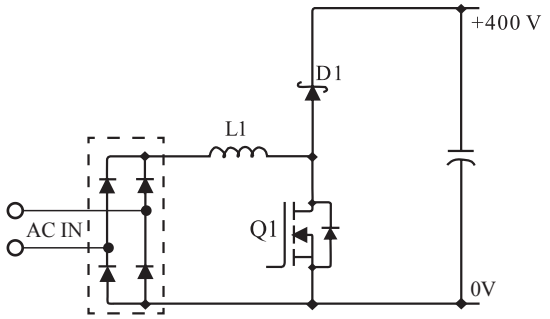

Fig. 18. Classic continuous current-mode boost stage.

This type of power factor correction stage achieves Platinum or Platinum + level if combined with a well-designed LLC stage including synchronous rectification. If Titanium level needs to be reached, the losses of the bridge rectifier become a major hurdle. Two conducting diodes create at high line (230 V AC) an efficiency drop of around 0.7%. This issue can be overcome with bridgeless topologies, having only one or even no conducting diode in the power flow path.

Fig. 20 shows two alternative circuits for bridgeless topologies with only one remaining conducting diode.

Both topologies have only one inductor and two switches. The totem pole has, in the minimum configuration, two slow diodes (D1, D2), but should use another two slow diodes for surge protection. The H4 topology uses two fast diodes (SiC

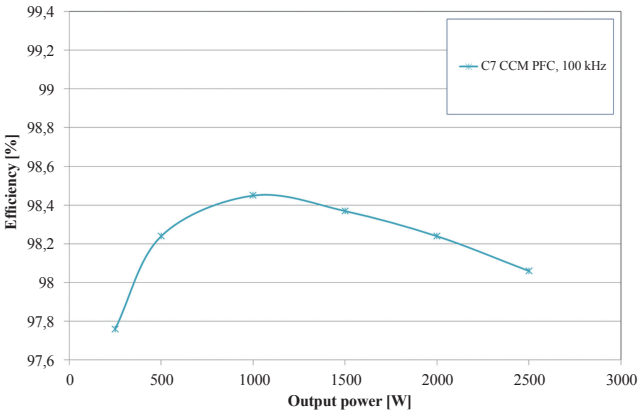

Fig. 19. Measured efficiency of a CCM PFC stage using a 65 mΩ Superjunction device in a 4-pin Kelvin contact TO package switching at 100 kHz versus a 16 A rated SiC Schottky barrier diode.

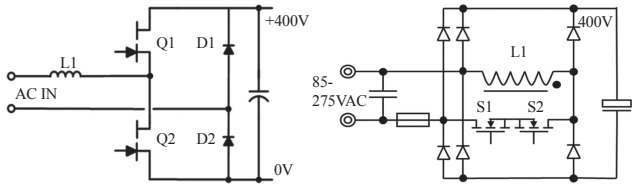

Fig. 20. Bridgeless topologies with only one conducting diode in the power flow path: totem pole (left) and H4 topology (right).

Schottky barrier diodes or ultrafast silicon diodes) and four slow diodes [20]. In the totem pole there is only one diode conducting in the power path. The H4 topology has, during the on-phase of switches S1 and S2, no conducting diode in the power path; during the off-phase of the anti-serial switches, one fast diode and one slow diode conducts. This topology is therefore versatile for low line conditions where the modulation index of switches S1/S2 is high.

When operating in continuous current mode, the totem pole requires switches with very low Q_{oss} and ideally zero reverse recovery charge. The totem pole therefore works best with GaN HEMTs. The H4 topology can be equipped with Superjunction and SiC Schottky barrier diodes for equally good performance. Forward looking, a bidirectionally blocking and conducting GaN HEMT is an interesting alternative for this topology.

Fig. 21 shows an analysis of the loss contribution from bridge rectifier, freewheeling element, and switches for both topologies.

The loss contribution from the freewheeling element is

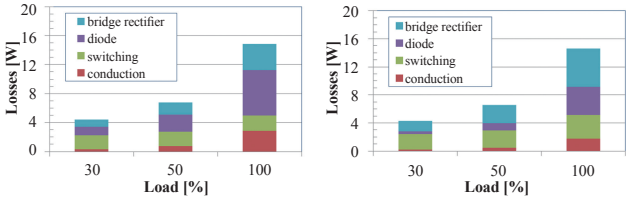

Fig. 21. Loss analysis of totem pole (left) and H4 topology (right), 1600 W, 230 V AC in, 65 kHz.

higher in the H4 topology due to higher forward voltage V_f of the SiC Schottky barrier diode in comparison to the losses of the GaN HEMT conducting in reverse direction in synchronous rectification mode. However, as the slow diode only conducts when switches S1/S2 are off, the contribution from the bridge rectifier is lower in comparison to the totem pole topology. Furthermore, the switching losses in the H4 circuit are lower as the switching losses of a Superjunction device switching against a SiC Schottky barrier diode is lower than of a GaN half bridge circuit operating at the same switching frequency. In total, the efficiency of both topologies is very similar across the entire load range with peak efficiency around 98.8% when operating at 65 kHz.

The totem pole topology can be further improved by replacing slow diodes D1 and D2 with power MOSFETs. This circuit is often referred to as full bridge totem pole. In this case no diode is left in the power flow path. GaN HEMTs are the best choice when operating in continuous current mode. Due to hard switching transients, the losses from both Q_{oss} and reverse recovery charge do not allow the use of Superjunction devices in this circuit. Therefore, we need to change the control strategy if Superjunction devices should be used in this circuit.

We need to ensure full removal of the reverse recovery charge and ideally discharge the output capacitance before turning on the device to eliminate all associated switching losses. This can be achieved by changing from Continuous Current Mode (CCM) into Triangular Current Mode (TCM) [21] as shown in Fig. 22.

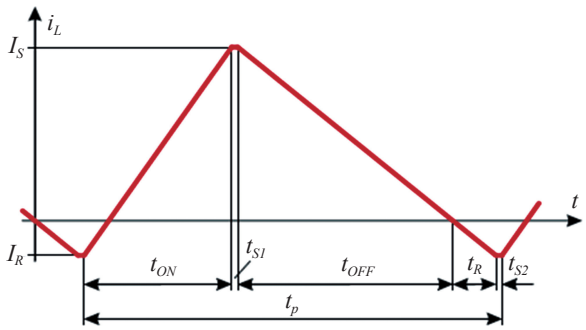

Fig. 22. Triangular current modulation scheme allowing zero voltage switching in half-bridge circuits.

Due to higher peak current from this modulation scheme it is advised to interleave two or more high frequency legs. The resulting circuits for continuous current and triangular current mode are shown in Fig. 23.

In, for example, positive line voltage, a positive current in inductor L1 is built up by turning on switch Q4 (vice versa in inductor L2 by turning on switch Q6). At the desired peak current Q4 is turned off with the current now freewheeling through the body diode of switch Q3, charging the DC link capacitor and returning through Q2. Switch Q3 can now be turned on at any time in a zero voltage condition parallel to the conducting body diode to allow synchronous rectification. After time interval t_{off}, the current reaches zero. Keeping Q3 further in the on-state will result in a change of the direction of current flow. Now the current in switch Q3 is positive. Keeping the device on for an interval t_R with:

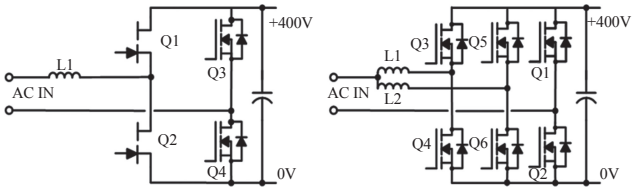

Fig. 23. Full bridge totem pole circuits using one high frequency leg with GaN HEMT devices in continuous current modulation (left) or two interleaved high frequency legs with Superjunction devices in triangular current modulation (right).

$$\tfrac{1}{2} \cdot I_R \cdot t_R > Q_{rr}(I) \tag{9}$$

ensures complete removal of the reverse recovery charge Qrr from switch Q3. The negative current I_R furthermore stores energy in inductor L1, which can be used to discharge the half bridge switching node between switches Q3 and Q4 prior to turning on Q4. Zero voltage switching can be achieved, if

$$\tfrac{1}{2} \cdot L \cdot I_R{}^2 > Q_{oss}(V) \cdot V_{DC} \cdot \tag{10}$$

It is noteworthy, that for zero voltage switching conditions in half bridge circuits the term $Q_{oss}*V_{DC}$ needs to be considered and not the energy term E_{oss} [22]. Referring to Fig. 11 the sum of the yellow and green coloured area needs to be taken into account.

Thus, when both equations are fulfilled, all switching losses related to Q_{rr} and Q_{oss} are removed. The devices are now achieving the extremely low soft switching losses as shown in Fig. 16 and Fig. 17 respectively. A peak efficiency above 99.2% has been demonstrated with this type of modulation scheme [23].

Due to the nature of the control scheme, the switching frequency varies strongly with load and across the AC sine wave; between full load / peak AC voltage and light load / zero voltage crossing, the frequency may change up to one order of magnitude. This strong frequency variation may create issues for the control. Furthermore, residual switching losses as shown in Fig. 17, are posing upper limits to the switching frequency.

The frequency swing can be limited by increasing the reverse current time, t_R, thus trading off switching losses versus additional conduction losses. A combination of partially hard switching and soft switching, thus combining the best aspects of both control schemes, has been proposed to overcome the limits of continuous and triangular current modulation, respectively [24].

The full bridge totem pole achieves in contrast same or better peak efficiency with great simplicity of control. Fig. 24 shows the measured efficiencies of half bridge and full

bridge totem pole configurations.

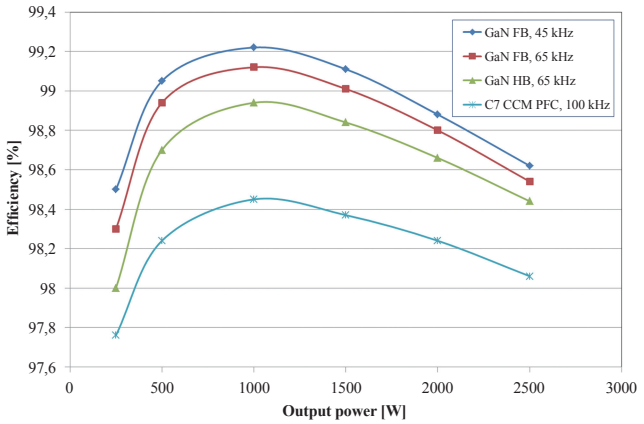

Fig. 24. Measured efficiencies for various totem pole configurations (half bridge, full bridge) using e-mode GaN HEMTs in comparison to the "classic" CCM PFC stage based on Superjunction and SiC Schottky barrier diode.

With just two 70 mΩ GaN HEMTs, a peak efficiency above 99% can be achieved in the full bridge totem pole circuit using two additional 35 mΩ Superjunction devices as low frequency switches. Lowering the switching frequency to 45 kHz allows greater than 99% efficiency from a load range of 20 to 70% of the full load.

Even though we discussed only power factor correction in this section, the underlying concept can be transferred to many applications in power electronics.

V. Conclusion

The comparison of different power device concepts is only meaningful in combination with their best matching circuits. We showed that both the latest generation of Superjunction devices as well as wide bandgap devices can achieve peak efficiencies above 99% in, for example, non-isolating power factor correction applications. While the control concept for silicon based power devices is more challenging, circuit and control for wide bandgap power devices is relatively simple and straight forward.

Both silicon and wide bandgap power devices have significant potential to further lower on-state resistance and correspondingly the cost of the fabricated die. We showed that Superjunction devices achieve best performance with SiC Schottky diodes as freewheeling element, while wide bandgap devices are very efficient in hard switching half bridge circuits, too.

In soft switching applications, GaN HEMTs with their unique device properties, have the potential towards very high switching frequencies, while silicon-based counterparts are limited to low and moderate switching frequencies.

VI. Acknowledgment

I would like to express my gratitude to many colleagues who contributed to aspects of this article. Without their knowhow and support this article would not exist. Special thanks go to Eric Persson and Matteo Kutschak for discussions on the e-mode GaN HEMT and application circuits and to Dr. Oliver Blank for discussions on the field plate concept.

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He is a Sr. member of IEEE and member of the IEEE EDS Power Devices and ICs Technical Committee. He has served as a member of the Technical Program Committee for Power Devices of the IEEE IEDM and ISPSD conferences and was Technical Program Chair for the ISPSD'16 conference. He is author and co-author of over 100 international patents and patent applications in the field of power semiconductors.

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