Solving Critical Ground-Shift Problems

Low-side gate-driver ICs are frequently used components in Switched Mode Power Supplies (SMPS). They serve to properly drive power MOSFETS into ON and OFF conditions. In Boost-PFCs they drive the low-side high-voltage power MOSFET. In high-voltage DC/DC-stages, such as LLC, ZVS, and TTF, they turn on and off the high-voltage power MOSFETs via a gate-driver transformer. In center-tapped synchronous rectification stages they are directly attached to the low-voltage MOSFETs. Gate drivers such as the 1EDN7550B and the 1EDN8550B provide sufficient robustness against GND shifts commonly present in large single-layer PCB designs as well as applications where the mechanical design requirements translate into large distances between the PWM controller IC and the gate-driver IC. **Hubert Baierl, Senior Marketing Manager, Infineon Technologies AG, Germany**

The input signal levels of conventional low-side gate-driver ICs in a typical SMPS (Figure 1) are referenced to the ground potential of the gate driver IC. False triggering of the gate-driver IC can occur if its ground potential shifts too far away from the ground potential of the controller IC. This can compromise the performance of the SMPS up to the level that half-bridge shoot-through occurs and the connected power MOSFETs are subject to functional disintegration due to electrical overstress.

Hard switching challenges

In hard-switching topologies such Boost-PFC and TTF stages, the parasitic inductances in the source contact of the power MOSFETs and in the ground-path of the PCB require special attention. Hard-switching goes hand in hand with high di/dt, which in turn leads to switching noise on the ground potential. This switching noise is a high voltage oscillation ranging between 50 MHz and 120 MHz, with amplitudes as high as up to ± 70 V. It is a prominent root-cause for transient shifts of the ground potential between the controller IC and the gate-driver IC. The higher the power rating of the SMPS the more pronounced tends this effect to be. Furthermore, if printed circuit board designs are not optimal due to cost constraints and industrial design requirements the situation can become

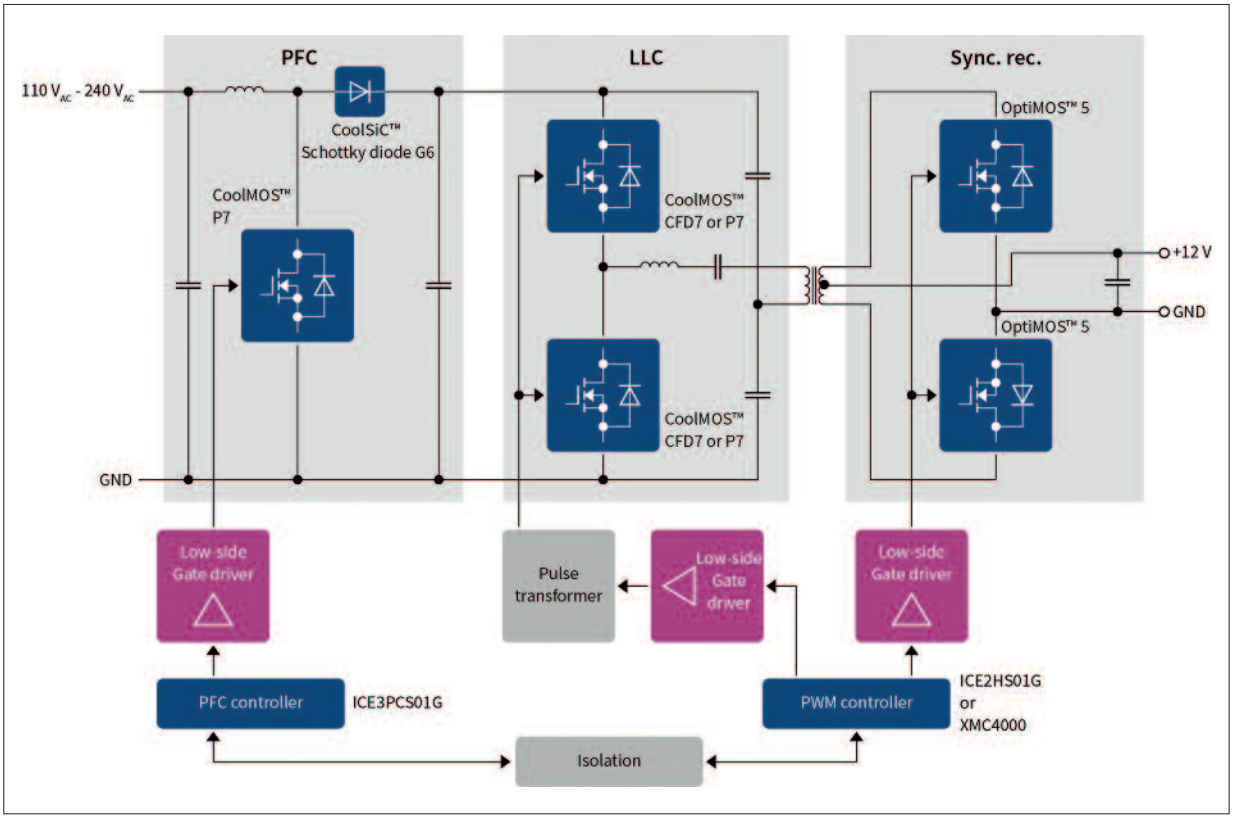

Figure 1: **Block diagram of a typical 800 W SMPS**

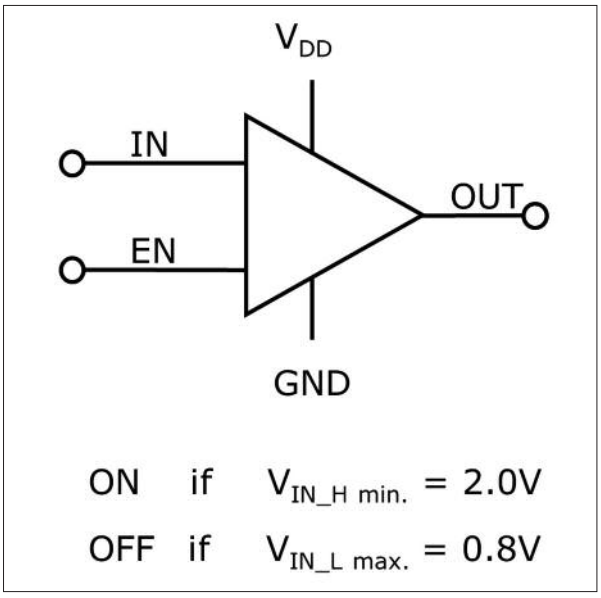

Figure 2: **Conventional low-side gate driver IC, inputs are referenced to the gate driver GND**

even more aggravated.

Solving this challenge is complex. Ultimately, the lower the parasitic ground inductances in the power loop the lower will be the induced ground oscillations and the lower the risk of false triggers. To keep the undesired ground shift as low as possible, designers have a few options. They can keep the dynamic gate-loop within a minimum physical PCB area and use in the PCB separate GND traces to provide a current path with the least possible inductance. Other solutions include designing gate driver output traces that are as wide as possible, using lead-less power MOSFETs or using power MOSFETs with a separate Kelvin Source connection to reduce the effects of the hard-switching impact on the gate-driving circuitry. All of these design solutions work, but may add complexity and significantly increase the design cost.

Conventional low-side gate-driver ICs are prone to false triggering

In a conventional low-side gate-driver IC, the interpretation of the control- and enable-input signals is always done through a comparison which is referenced to the ground potential of that gate-driver IC. In the example shown in Figure 2, the input is understood to be logically OFF as long as the input signal is not higher than 0.8 V relative to the ground. Conversely, if the input signal-level is at least 2.0 V higher than the ground potential then that input is logically ON.

To better understand the problem that arises if the gate-driver IC's GND-potential shifts, consider that the gate-driver inputs are typically connected to a controller IC. From an electrical design perspective, the controller IC is on a more stable ground potential then the gate-driver IC's ground. In some designs the situation is worsen if the ground contact of the gate-driver IC is far away from the ground contact of the controller IC. This can happen, for example, when the controller IC resides on a daughter board which is inserted onto the main power-PCB.

Figure 3a shows a Boost-PFC using a power-MOSFET with a Kelvin Source contact. A galvanically isolated gate-driver IC is used to decouple the two ground potentials, i. e. that of the controller IC and the gate-driver IC input side (GND1) from that at the gate-driver IC output side (GND2). This is called "cutting the ground loop".

In circuitries as shown in Figure 3a, the

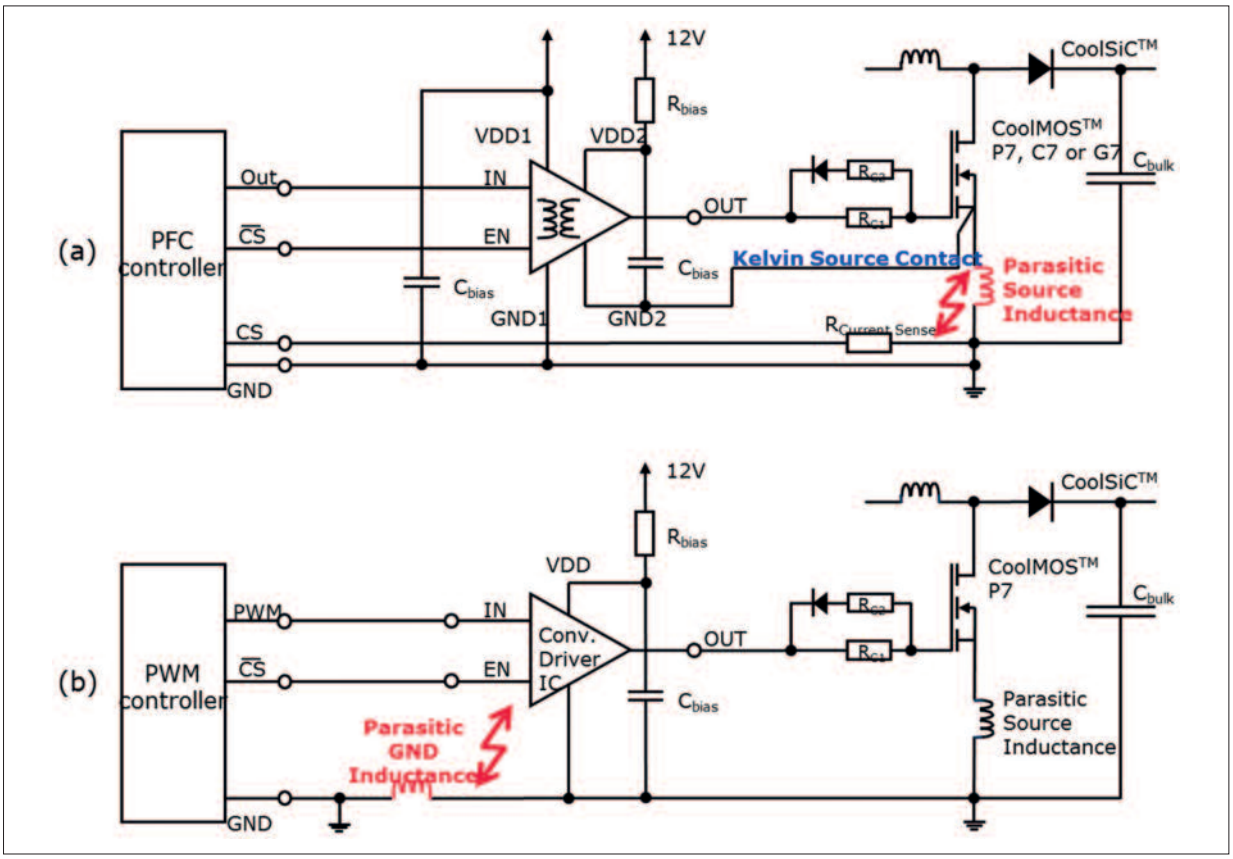

Figure 3: **Kelvin Source power MOSFET driven by galvanically isolated gate-driver IC to cut the ground loop (a) and parasitic ground inductance example (b)**

Kelvin Source contact is used to reduce the impact of the parasitic source inductance of the power MOSFET onto the gate-driver IC ground potential. Measurements of such topologies show that the oscillations between the PWM controller IC ground and the gate-driver IC GND2 can still amount to as much as ± 60 V.

In low-power SMPS, highest performance is not always the prime objective. In many cases, mechanical design requirements as well as component and PCB cost tend to be the overriding considerations. Such constraints can lead to SMPS designs with longer than desired distances between the gate-driver IC and the controller IC. This may force the designer to use single layer PCBs and preclude the use of isolated gate-driver ICs. Under such circumstances, high parasitic ground inductances are a frequent result (Figure 3b). In such applications, switching the power MOSFET can easily lead to a dynamic ground shift between the PWM controller IC and the gate-driver IC of up to ± 20 V.

Low-side gate-driver IC with truly differential inputs resolves GND shift problems

If a gate-driver IC has truly differential inputs, its control signals are largely independent from the ground potential of that IC. Only the voltage difference between its input contacts is of relevance to turn its output ON or OFF. For example, if the potential of V_{in+} is higher than the potential of V_{in-} by 1.8 V this is interpreted as a logical ON. If the difference is less than 1.5 V this is interpreted as a logical OFF.

The 1EDN7550B and 1EDN8550B EiceDRIVER™ from Infineon are single-channel low-side gate driver ICs that can resolve static GND shift problems of up to ± 70 V. If the ground shift is transient, which is typical for MOSFET switching induced ground noise, these gate-driver ICs are robust against shifts of as much as ± 150 V_{peak}. This can be referred to as static and dynamic common mode immunity of the gate-driver IC's control inputs.

As these gate-driver ICs operation is based on the voltage difference between its two inputs, the most important design rule is to place two common mode resistors physically close to the two input contacts of the gate driver ICs. That layout has to be done geometrically and parasitically symmetrical. The output pinout arrangement and the VDD pin are in line with commonly used single-channel low-side gate driver ICs. Therefore, when up-grading existing designs with the 1EDN7550 or the 1EDN8550 only the input side of the PCB design must be modified.

The 1EDN7550B and 1EDN8550B EiceDRIVER have a small 6-pin SOT-23 package. This helps improving power density, relative to using galvanically isolated gate-driver ICs. A second advantage that comes along with this package type is that designers can place these gate-driver ICs in the most optimal location relative to the power MOSFET gate connection.

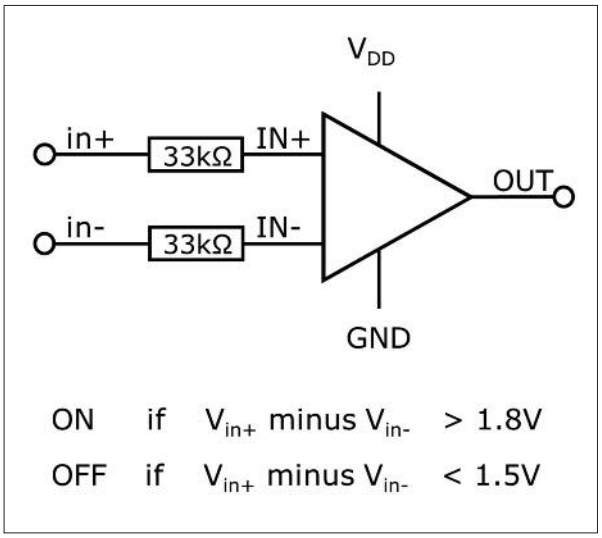

Figure 4: Low-side gate driver IC with truly differential inputs; inputs are independent from the gate driver GND

Conclusion

Low-side gate-driver ICs with truly differential control inputs, such as the 1EDN7550B or 1EDN8550B from Infineon, can withstand common mode ground shifts of up to ± 70 V statically and ± 150 V_{peak} dynamically (both are operational range values, applicable if PCB layout recommendations are followed). With the 1EDN7550B and the 1EDN8550B, it is possible to use a single-channel low-side gate-driver IC to drive Kelvin Source power MOSFETs such as CoolMOS P7, C7, or G7 in applications like 2.5 kW Boost-PFCs. There is no need to cut the ground loop with a galvanically isolated gate-driver IC. As has been shown, the 1EDN7550B and the 1EDN8550B provide sufficient robustness against GND shifts commonly present in large single-layer PCB designs as well as applications where the mechanical design requirements translate into large distances between the PWM controller IC and the gate-driver IC.

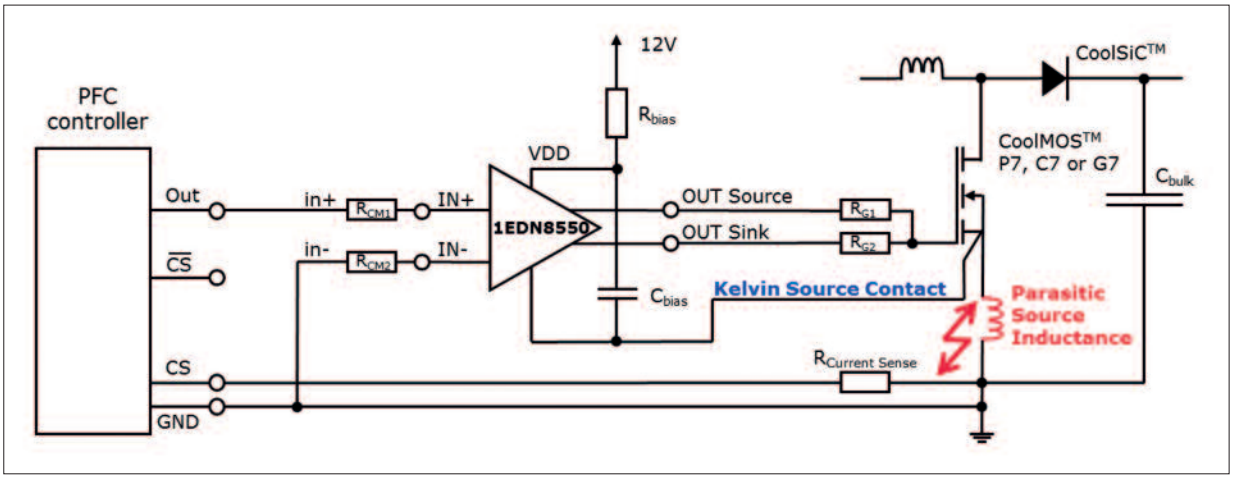

Figure 5: Kelvin Source power MOSFET driven by a gate-driver IC with truly differential control inputs