No more ground-shift challenges to your SMPS designs

Infineon's low-side gate driver ICs with truly differential inputs

Hubert Baierl, Senior Marketing Manager, Infineon Technologies AG

The best-in-class operation and performance of modern switch-mode power supplies (SMPS) have one thing in common: they are rooted in semiconductor devices that are fundamental to their designs. Reliable and high-performance semiconductor components always have been the domain of high-end systems.
In this article, Infineon will delve into the topic of low-side gate driver ICs for SMPS applications and look at how they can contribute to achieve the performance required for today's designs.

There are multiple ways how a gate driver can be used in SMPS applications. Low-side gate drivers are often used in SMPS and play a significant role in ensuring that power MOSFETs are properly driven into 'on' and 'off' conditions. In boost power factor correction (PFC) circuits they drive the low-side high-voltage power MOSFET. In high-voltage DC/DC-stages with LLC resonant converters, in zero voltage switching (ZVS) circuits or in two transistor forward (TTF) topologies they turn on and off the high-voltage power MOSFETs via a gate-driver transformer.
In center-tapped synchronous rectification stages they are directly attached to the low-voltage MOSFETs.

Electrical overstress of power MOSFETs can lead to functional disintegration of the SMPS. False triggering of the gate-drive IC is a prominent reason for such electrical overstress. Shift of the low-side gate-driver IC's ground potential too far away from the ground potential of the controller IC can be the reason for such false triggering (note: the input signal levels of conventional low-side gate-driver ICs are referenced to the ground potential of the gate driver). Infineon's 1EDN7550 and 1EDN8550 1-channel low-side gate drivers are designed to prevent false triggering of power MOSFETs in industrial, server and telecom SMPS, in wireless charging applications, telecom DC-DC converters, power tools and solar micro inverters.

DESIGN CHALLENGES OF HARD SWITCHING TOPOLOGIES

In hard-switching topologies, such as boost-PFC and TTF stages, the parasitic inductances in the source contact of the power MOSFETs and in the ground-path of the PCB require special attention. Hard-switching goes hand in hand with high dI/dt, which when paired with parasitic inductances leads to switching noise on the ground potential. This noise is a high voltage oscillation ranging between 50 MHz and 120 MHz, with amplitudes as high as up to ± 70 V. It is the dominant root-cause for transient shifts of the ground

potential between the controller IC and the gate-driver IC. The higher the power rating of the SMPS is, the more pronounced this effect tends to be. Furthermore, if printed circuit board designs are not optimal due to cost constraints and industrial design requirements the situation can become even more aggravated.

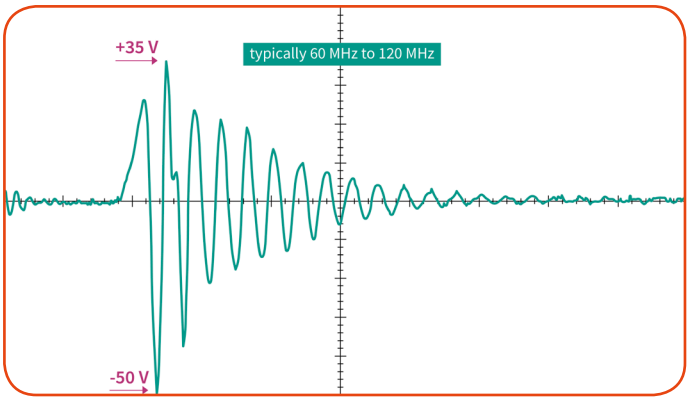


Figure 1: Example of switching noise on ground potential

The challenge is complex and the solution frequently a delicate trade-off. Basically, the lower the parasitic ground inductances in the power loop, the lower the induced ground oscillations will be and the lower the risk of false triggering. To keep the undesired ground shift as low as possible designers have only a few options.
Either they can keep the dynamic gate-loop within a minimum physical PCB area and use separate ground traces in the PCB to provide a current path with the lowest possible inductance, or they design gate driver output traces that are as wide as possible.
Using lead-less power MOSFETs or power MOSFETs with a separate Kelvin Source connection further helps reducing the effects of the hard-switching impact on the gate-driving circuitry.

FALSE TRIGGERING IS A COMMON PHENOMENON

Conventional low-side gate-driver ICs are prone to false triggering. In these gate-driver ICs the interpretation of the control and enable input signal is always done through a comparison which is referenced to the ground potential of that gate-driver IC.
An example is depicted in Figure 2 where the input is understood to be logically 'off' as long as the input signal is not higher than 0.8 V relative to the ground. Conversely, if the input signal-level is at least 2.0 V higher than the ground potential then that input is logically 'on'.

To better understand the problem that arises if the gate-driver IC's GND-potential shifts, consider that the gate-driver inputs are typically connected to a controller IC. From an electrical design perspective, the controller IC is on a more stable ground potential then the gate-driver IC's ground.
In some designs the ground contact of the gate-driver IC is far away from the ground contact of the controller IC, resulting in worse outcomes. For instance this may happen when the controller IC resides on a daughter board which is inserted onto the main power-PCB.

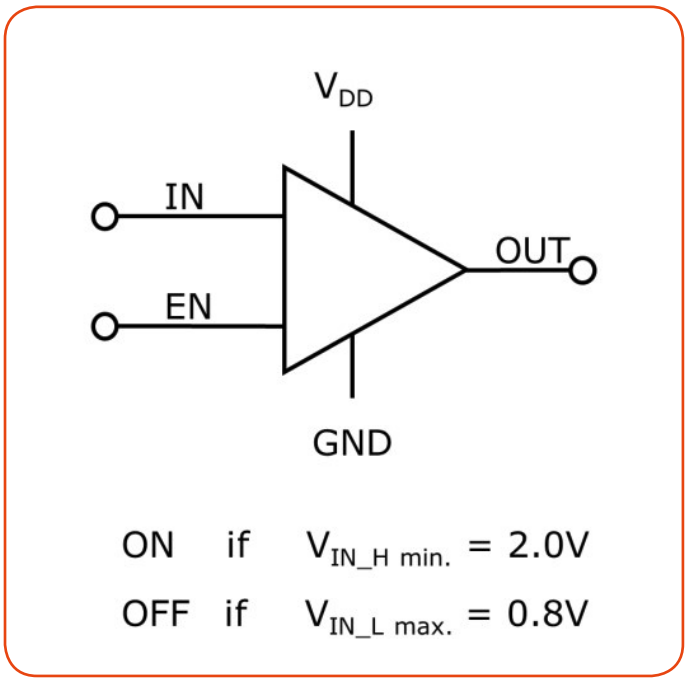


Figure 2: Conventional low-side gate driver IC, inputs are referenced to the gate driver GND

The frequently found recommendation to drive Kelvin Source power MOSFETs is to use galvanically isolated gate-driver IC to cut the ground loop and the parasitic ground inductance. Measurements of such topologies show that the oscillations between the PWM controller IC ground and the gate-driver IC GND2 can still amount to as much as ± 50 V (see Fig. 1).

SMPS designs with longer than desired distances between the gate-driver IC and the controller IC are quite common. Frequently, mechanical design requirements as well as component and PCB costs are in the focal point for design decisions, and in low-power SMPS highest performance is not always the main objective. This may force the designer to use single or dual layer PCBs and preclude the use of isolated gate-driver ICs. This often results in higher parasitic ground inductances than desired. In such applications switching the power MOSFET can easily lead to a dynamic ground shift between the PWM controller IC and the gate-driver IC of up to ± 20 V.

HOW TO RESOLVE GND SHIFT PROBLEMS

With a low-side gate-driver IC that has truly differential inputs only the voltage difference between its input contacts is relevant to turn its output 'on' or 'off'. Its inputs are largely independent from the gate driver GND potential. For example, if the potential of Vin+ is higher than the potential of Vin- by 1.8 V this is interpreted as a logical 'on'. If the difference is less than 1.5 V, this is interpreted as a logical 'off'.

Infineon's EiceDRIVER™ family members, 1EDN7550B and 1EDN8550B, single-channel low-side gate driver ICs can resolve static GND shift problems of up to ± 70 V. If the ground shift is transient, which is typical for MOSFET switching induced ground noise, these gate-driver ICs are robust against

Figure 3: 1EDN7550 driving CoolMOS™ SuperJunction MOSFET on 1-layer PCB

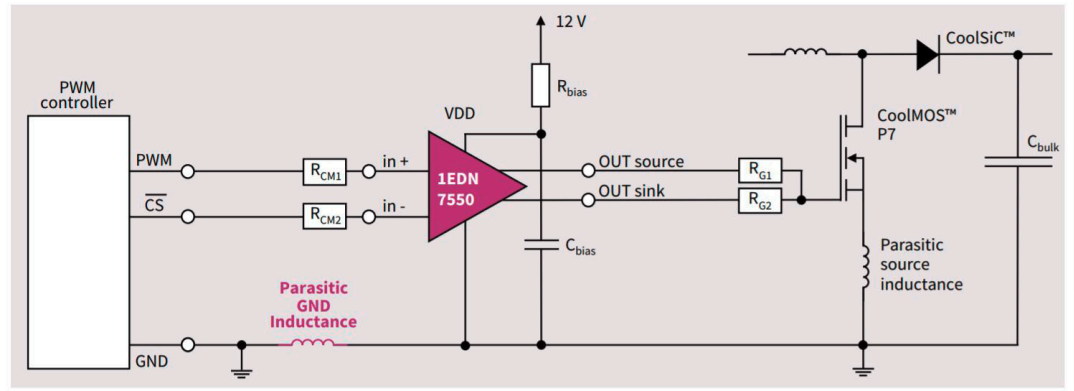


Figure 4: 1EDN8550 driving Kelvin Source CoolMOS™ MOSFET in boost-PFC

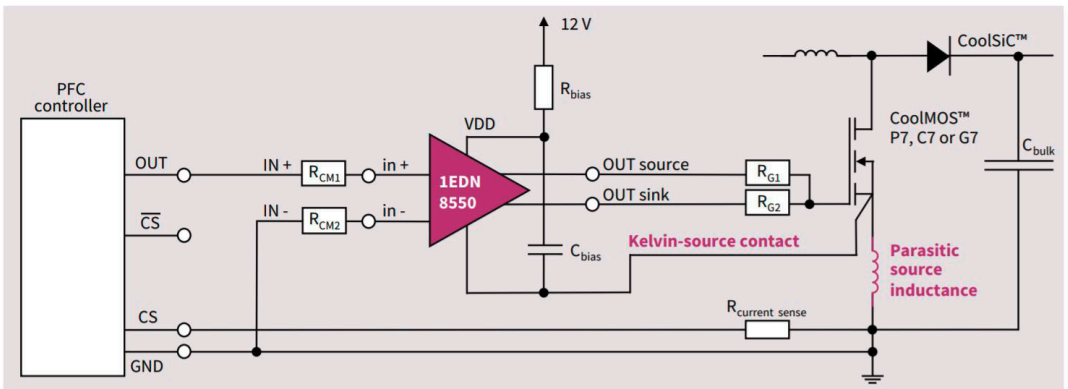
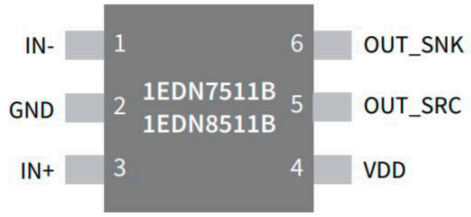


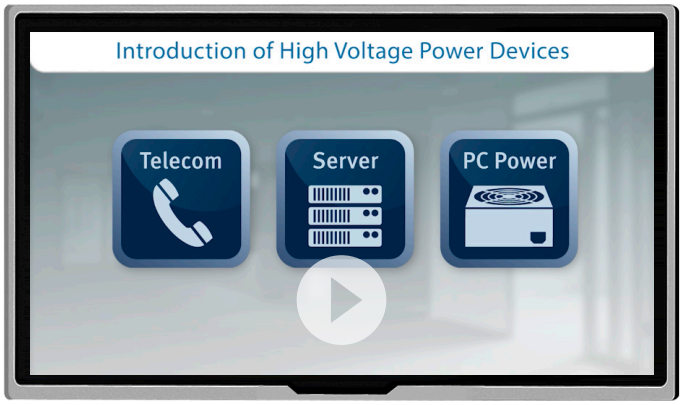
Figure 5: EiceDRIVER™ 1EDN7550B and 1EDN8550B product portfolio and pinout

Type	Ground shift robustness		UVLO	Package
	dynamic	static		
1EDN7550B	+/- 150 V	+/- 70 V	4 V	6pin SOT-23
1EDN8550B	+/- 150 V	+/- 70 V	8 V	6pin SOT-23



shifts of as much as ± 150 Vpeak. With the EiceDRIVER™ 1EDN7550B and 1EDN8550B components it is possible to use a single-channel low-side gate-driver IC to drive Kelvin Source power MOSFETs such as CoolMOS™ P7, C7 or G7 in applications like 2.5 kW boost-PFCs. There is no need to cut the ground loop with a galvanically isolated gate-driver IC.

As these gate-driver ICs' operation is based on the voltage difference between its two inputs, the most important design rule is to place two common mode resistors (RCM1 and RCM2 depicted in Fig. 3 and Fig. 4) physically close to the two input contacts of the gate driver ICs. That layout has to be done geometrically and parasitically symmetrical. The output pinout arrangement and the VDD pin are in line with commonly used single-channel low-side gate driver ICs.
Therefore, when upgrading existing designs with the 1EDN7550 or the 1EDN8550 only the input side of the PCB design must be modified. The small 6-pin SOT 23 package of EiceDRIVER™ 1EDN7550B and 1EDN8550B helps to improve power density, relative to using galvanically isolated gate-driver ICs. Also, this package design enables designers to place these gate-driver ICs in the most optimal location relative to the power MOSFET gate connection.
No matter the technical or design challenges of SMPS applications, combining Infineon's proven quality and reliable low-side gate-driver ICs with truly differential control inputs translates into faster go-to-market, higher power density, more robust and more efficient designs at a lower cost than traditional solutions. For more detailed information, please visit www.infineon.com/TDI. ■



More info

- Product Brief – EiceDRIVER™ 1EDN TDI

Kelvin Source CoolMOS™ SJ MOSFETs:

- Double DPAK (DDPAK)
- TO-Leadless (TOLL)
- TO-247 4pin
- ThinPAK 8x8

PCIM 2018
June 5th - 7th
Hall 9-412

- Whitepaper: Wireless charging