EiceDRIVER™ Safe

High voltage gate driver IC with reinforced isolation

1EDS-SRC

Technical description
1EDS20I12SV
1EDU20I12SV
1EDI20I12SV

EiceDRIVER™

Application note

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1 Scope

This application note includes a detailed description of the behavior regarding the gate current control IC 1EDS020I12SV (1EDS-SRC). Typical applications of this component are servo drives, industrial drives, uninterruptible power supplies and three level inverters in many kinds of applications. It provides reinforced isolation according to VDE 0884-10 by means of Infineon´s coreless transformer technology. This document gives helpful advice for the application of the device in terms of diagrams, text and calculation rules.

The document refers to the application together with power modules containing IGBT, but it is not restricted to it. The IC is also applicable to other kind of power transistors, such as modules with MOSFET or discrete power transistors even with low current ratings.

Practical information is given for the selection of external components as far as they are required for proper operation of the IC and its functions. This includes also the calculation of the power dissipation of the IC and external key elements.

This revision of the document is related to the current availability of test parameter values. Therefore, some values are to be defined until the full release of the final revision of the document.

2 Technical description

2.1 Supply and voltage domains of the driver IC's input side

The input side comprises the terminals VCC1, GND1, SIGI, SIGO, SPEED, /FLT, RDY1, RDY2, PADP, INP, INN, EN, and PADN. These pins belong to two different voltage domains according to Figure 1. The base domain must be supplied with 5 V including its tolerances in respect to the undervoltage lockout function (UVLO). The terminals VCC1, GND1, SIGI and SIGO belong to this domain and the voltage must stay within the maximum rating of 6.5 V. RDY1, RDY2 and /FLT belong to the same domain, but can accept up to 15V.

The second domain is supplied using the terminals PADP and PADN. The terminals SPEED, PADP, INP, INN, EN, and PADN belong to this domain. Terminals in this domain are referenced to terminal PADN. INP, INN and EN can accept voltages up to V_{PADP}, SPEED can accept voltages to an absolute maximum of V_{VCC1}.

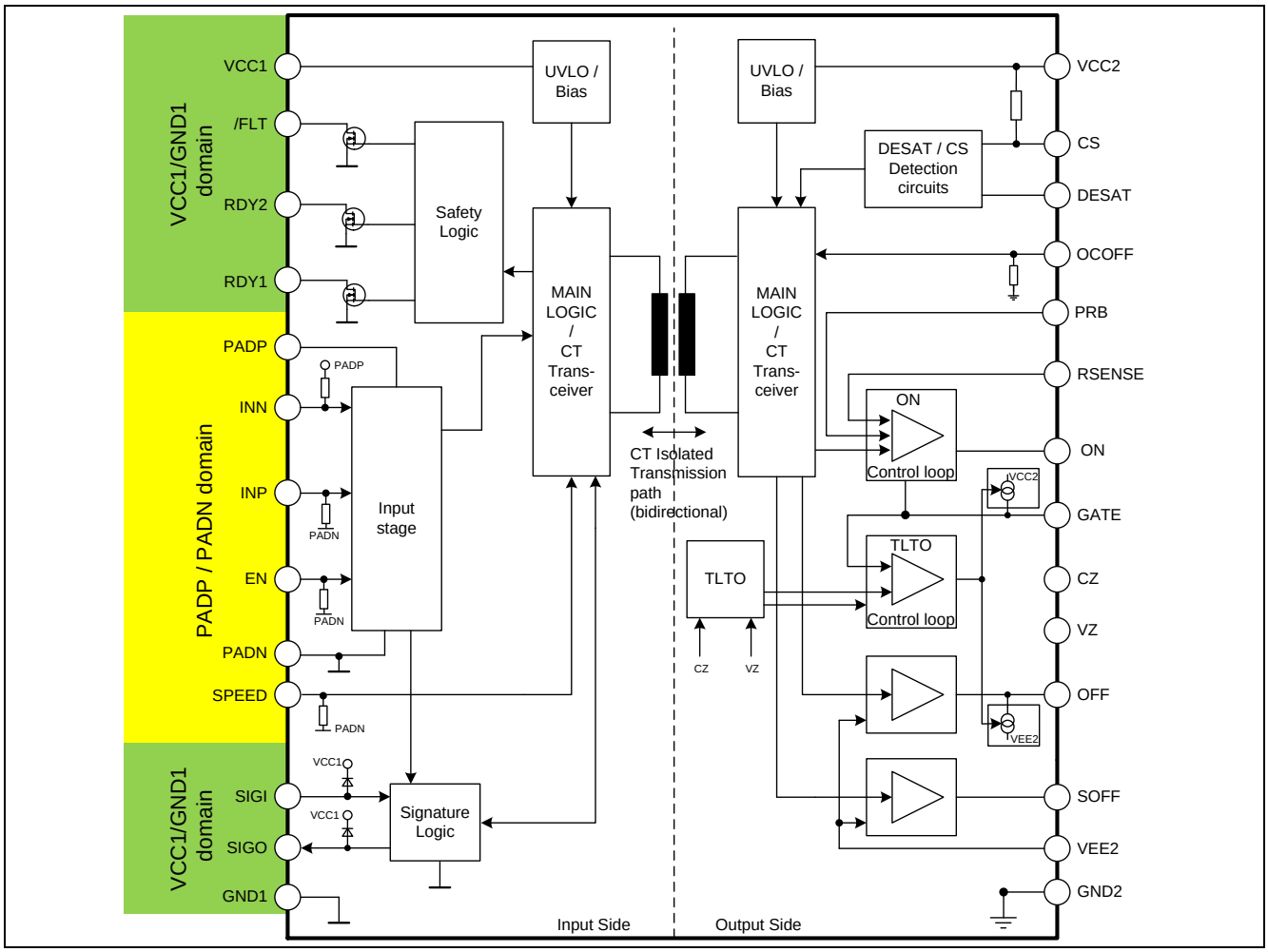

Figure 1 Block diagram and voltage domains of the input side

The PADP domain has its own UVLO levels which are correlated to the supply voltage range. Table 1 contains the limits of the UVLO of both domains. The initialization time of the input side during power up is approximately 22 µs and is over, when the RDY1 signal is pulled high.

Table 1 Undervoltage lockout limits of input side

Parameter	max. UVLO+	min. UVLO–
V_{VCC1}	4.85 V	3.5 V
V_{PADP}	2.95	1.6

The terminal RDY1 is pulled low as long as any of the input side's voltage domains are in UVLO state. It is necessary to buffer the supply voltage for both domains by means of ceramic capacitors located closely to the IC to avoid parasitic UVLO because of inductive voltage drops.

2.2 Supply of the output side

The output side is designed to support bipolar gate driving with a minimum of V_{VEE2} = -12 V and a maximum of V_{VCC2} = 20.3 V. However, the maximum difference between V_{VEE2} and V_{VCC2} must always be lower than 28 V. The positive and the negative supply must be sufficiently stabilized by capacitors, which are placed in close proximity to the IC. The capacitors must be able to provide sufficient current without disturbing the IC operation. This means that the gate charge value of the IGBT must be much smaller than the capacitor´s charge and the capacitor is located very close to the IC.

The power supply of the output side in systems which are qualified for reinforced isolation is often designed as a switch mode power supply (SMPS). These operate at considerably high switching frequency in a range often exceeding 50 kHz.

Thus, in a worst case scenario, the blocking capacitors have to provide the quiescent current, the gate charge as well as the charge for a damping element of the gate current control.

In a given circuit, the gate charge $Q_g(V_{ge})$, the quiescent current of the driver IC, and the damping capacitor are known. The blocking capacitor C2 according to Figure 12 is

$$C2 = \frac{Q_g + CD \cdot (V_{VCC2} - V_{VEE2}) + I_{q2} \cdot T_P}{\Delta V_{VCC2}} \quad (1)$$

Where Q_g represents the gate charge of an IGBT, *CD* is the value of the damping capacitor CD acc. to Figure 14, V_{VCC2} is the positive gate voltage, V_{VEE2} is the negative gate voltage, I_{q2} is the output side's quiescent current and T_P is the pulse period of the IC's power supply if a SMPS is used. ΔV_{VCC2} is the allowed peak-to-peak voltage ripple during a pulse period T_P.

The blocking capacitor of the negative gate voltage supply has to provide a capacitance in analogy to eqn. (1).

$$C3 = \frac{Q_g + CD \cdot (V_{VCC2} - V_{VEE2}) + I_{q3} \cdot T_P}{\Delta V_{VEE2}} \quad (2)$$

ΔV_{VEE2} is the allowed peak-to-peak voltage ripple during a pulse period T_P.

It is advised to keep an additional margin of approximately 20% due to production related tolerances of capacitors and IGBT. The UVLO levels of the output side are given in Table 2.

Table 2 Undervoltage lockout limits of output side

Parameter	max. UVLO+	typ. UVLO+	typ. UVLO–	min. UVLO–
V_{VCC2}	12.6 V	11.9 V	11.0 V	10.4 V

2.3 Input terminals INP and INN

The input terminal INN incorporates a pull-up resistor to PADP and terminal INP a pull-down resistor to PADN. This ensures a safe output state during insufficient supply voltage, unperfected solder joints or other cases of not connected pins according to the block diagram in Figure 1.

The PWM signal is usually applied to either INN or to INP. Figure 2 hints out several possible connections of the terminals INN and INP for various purposes.

Option A depicts a quasi-differential way of controlling the IC. Both input signals are related to PADN and terminal INP is controlled by an active high signal while INN is controlled by an active low signal. The output side is turned on if INP = /INN = High. The output side is turned off in any other case.

Option B gives the connection scheme for active low logic signals. The output follows the inverted input PWM-signal at terminal INN. The output side is turned on if INP = High & INN=Low. The terminal INP can act as an additional enabling terminal.

Option C is an example for an active high control. The output follows in phase with the input PWM at terminal INP. The output side is turned on if INN = Low & INP=High. The output is shut down in case that INN = High. INN can also act as an additional shut down path.

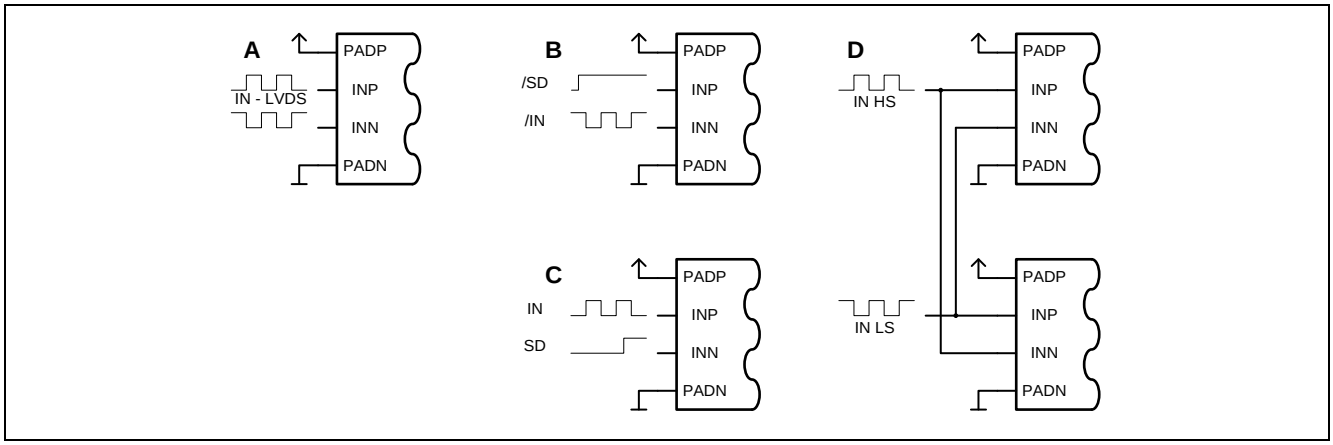

Figure 2 Connection options of 1EDS-SRC: quasi-differential (A), active low with enable (B), active high with shut down (C) and interlock (D)

The wiring of the 1EDS-SRC for a half bridge as shown in option D results in a very basic interlock function. The turn-on signal to the INP input of one 1EDS-SRC inhibits the turn-on of the opposite side´s 1EDS-SRC and vice versa.This concept can avoid cross conduction by means of corrupted or miscalculated PWM signals. Please note here, that the properties of power semiconductors and control IC such as propagation delays and delay deviations can still lead to temporary half bridge short circuits.

2.4 Enable terminal EN

The terminal EN controls the activation and the shutdown of the driver IC. The input structure also provides a pull-down resistor to PADN.

The driver IC immediately reacts on the instantaneous input signals at terminals INN and INP, if EN is controlled high. The preboost section according to section 2.8.1 is skipped, which can result in a rather slow turn-on. It is recommended to set the conditions for a low output before activating terminal EN in order to achieve a normal turn-on. Supplying a low signal at terminal EN will result in a soft turn-off on the output side. Please note that further redundant options of shutting down the IC are possible according to b) and c) of Figure 2 in section 2.3.

2.5 Status signals RDY1, RDY2, /FLT

These ready signals and the fault signal indicate the status of the input side as well as the output side. The ready signal RDY1 =High for the control side covers the conditions:

- UVLO status of the control side supply voltage domains at terminals VCC1 and PADP
- Correct signal transmission from input side to output side across the insulation barrier is established

The ready signal RDY2 = high for the output side indicates after a short delay:

- UVLO status of the output side supply voltage VCC2
- Bidirectional signal transmission across the insulation barrier established

Both signals are monitoring signals only and need not to be reset actively. Terminal /FLT is the indicator for a triggered Short Circuit (DESAT) or overcurrent (CS) event. It is pulled low by an internal FET. The /FLT function is reset by means of a low signal at terminal EN for more than $T_{EN,RST}$ = 870 ns.

Table 3 illustrates the reaction of the output and the status signals in respect of the supply condition of VCC1, PADP and VCC2. “UVLO ↑” means a transition of the corresponding supply during its power up, an “UVLO ↓” means a transition for power down. A static UVLO is given without arrow.

Table 3 1EDS020I12SV status UVLO at VCC1, VCC2 and PADP (EN = high)

VCC1	VCC2	PADP	RDY1	RDY2	Result
UVLO ↓	good	good	low	low	SOFF and 5 µs watchdog
UVLO ↑	good	good	high	high	acc. INP / INN (turn-on with preboost)
UVLO ↑	good	UVLO	low	high	OFF
X	UVLO ↓	X	X	low	activate OFF and SOFF simultaneously
good	UVLO ↑	good	high	high	acc. INP / INN (turn-on with preboost)
UVLO	UVLO ↑	good	low	low	OFF
X	X	UVLO ↓	low	low	SOFF and 5 µs watchdog
good	good	UVLO ↑	high	high	acc. INP / INN (turn-on with preboost)

RDY1, RDY2 and /FLT are open drain outputs. It is therefore possible to connect all three to a joint pull-up resistor. However, this comes along with a loss of specific information regarding the IC's status.

2.6 Adjusting the gate current amplitude on the output side

The voltage level at terminal SPEED controls the gate current amplitude for the turn-on phase according to section 2.8.2. The input voltage range between 0 and 3.3 V at terminal SPEED is divided into 11 sections. Each section corresponds to a separate reference value for the gate current control loop. Therefore, 11 levels of gate current are available during the turn-on phase. The levels can be changed during operation pulse-by-pulse with a delay of 120 µs.

Table 4 Switching speed levels on input and output side

	Voltage at terminal SPEED	Typ. reference V_{RSENSE}	% of turn-on gate current amplitude
Level 1	3.3 V	V_{VCC2}-0.197	20%
Level 2	2.91 V	V_{VCC2}-0.287	28.90%
Level 3	2.63 V	V_{VCC2}-0.376	37.80%
Level 4	2.35 V	V_{VCC2}-0.466	46.70%
Level 5	2.08 V	V_{VCC2}-0.556	55.60%
Level 6	1.80 V	V_{VCC2}-0.645	64.40%
Level 7	1.52 V	V_{VCC2}-0.735	73.30%
Level 8	1.25 V	V_{VCC2}-0.825	82.20%
Level 9	0.97 V	V_{VCC2}-0.912	91.10%
Level 10	0.69 V	V_{VCC2}-1.003	100%
Level 11	0	V_{VCC2}-1.543	157%

The default setting during or after a power up is level 4. It is mandatory to design a bias voltage to input terminal SPEED. Otherwise the terminal may float to level 11, because of the integrated pull-down resistor. A hysteresis of $V_{SPEED,hys}$ = 60mV helps to avoid a jitter of the switching speed.

The internal reference for the switching speed adjustment is V_{PADP}. It is therefore highly recommended to use voltage V_{PADP} as well as reference for a potential use of a digital-analog-converter (DAC). Only in this case it is guaranteed that variations of the voltage V_{PADP} do not change the selected SPEED level. The reference voltage of terminal SPEED is PADN. Please see further information in section 2.1.

2.7 Signature check

The I/O signature check is a feature that allows the confirmation of switching commands sent by the microcontroller to the driver IC. The SIGO output terminal is an exclusive-or (XOR) combination of the terminals INN, INP and EN according to Figure 3. The desaturation status on terminal DESAT and the correct voltage at terminal PADP are also monitored.

To save PCB space, the SIGI and SIGO terminals of a series of drivers can be interconnected via a daisy chain. In this case, terminal SIGI of the first driver in the daisy chain should be connected to VCC1 or GND1. Terminal SIGI of the next driver should be connected to terminal SIGO of the previous driver. Terminal SIGO of the last driver in the daisy chain should be connected to the microcontroller.

The I/O signature check does not monitor the status of the IGBT. It is recommended to connect terminal SIGI either to VCC1 or to GND1, if the signature check is not used. Also leave terminal SIGO not connected.

Monitored status

- INN / INP and EN
- DESAT
- PADP undervoltage

The reference terminals are VCC1 and GND1.

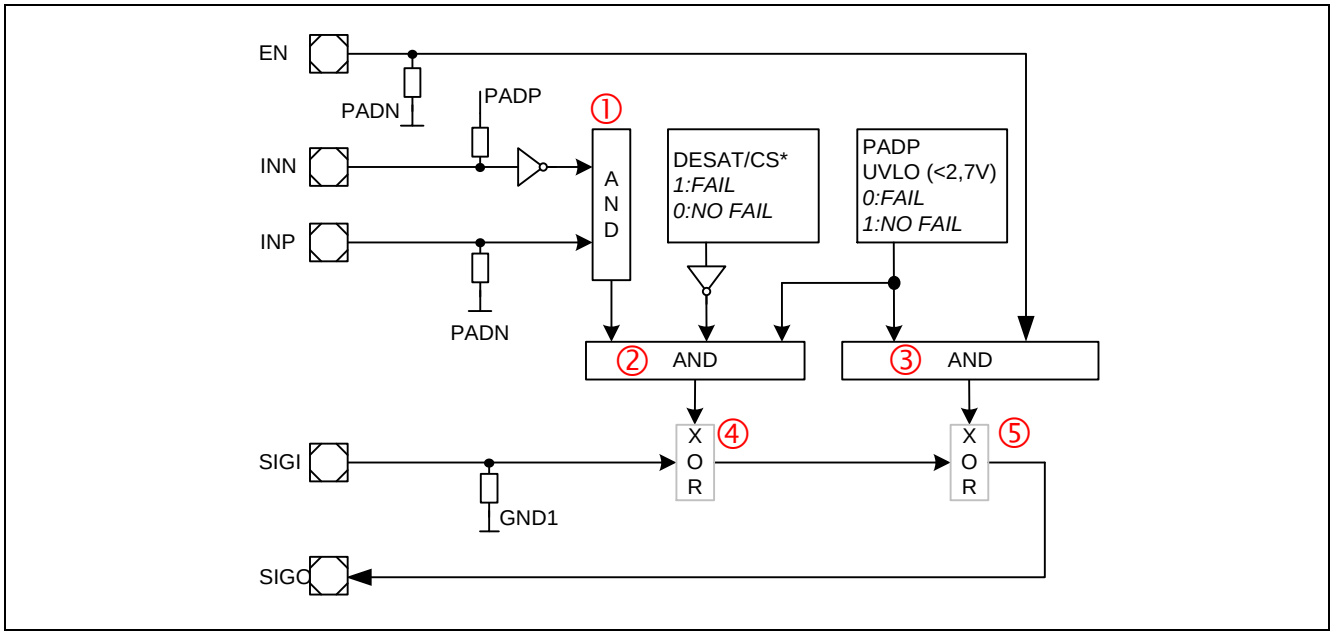

Figure 3 I/O signature check

The control input signals are evaluated in the AND gate "①". The output of this gate is logic "1", if INN = 0 and INP = 1. This state is related to a turn-on signal.

The 3-input AND gate ② combines this current turn-on control signal with the status of the output side in terms of desaturation or current sense trigger. A third signal is the input side supply state, i.e. UVLO of PADP. The output of gate ② indicates a working input side and no failure on the output during a turn-on status of the IGBT. The AND gate ③ monitors the EN status and again the UVLO status of PADP.

The two XOR gates ④ and ⑤ connect all signals. The output at terminal SIGO of the signature circuit is then identical to the input signal at terminal SIGI in case that the output is set for turn-on AND no fail occurs AND no UVLO is there on the input side AND the IC is enabled. In any other case, the signal SIGO is different from SIGI.

2.8 Gate turn-on process

The output stage consists of the internal regulation circuit inside the driver, an external sense resistor RS, and a number of external P-channel transistors placed in parallel. The number of paralleled transistors is limited by their gate charge, because the IC can deliver an minimum peak current of $I_{ON,pk}$ = ± 50mA. The IC is able to drive e.g. 3 BSD314SPE, OptiMOS™-P 3, 30 V, 140 mΩ, in parallel, which may be sufficient for IGBT up to 900 A.

The IGBT is switched on by means of a regulated current source after a short propagation delay. The short delay is caused by the gate charge needed for the p-channel MOSFET. The entire turn-on procedure is separated into three phases according to Figure 4: the preboost, the turn-on, and the V_{VCC2} clamping phase.

2.8.1 Preboost phase

The preboost phase controls a high current to drive the gate of the IGBT. This brings the gate voltage from its negative level to a voltage slightly lower than the gate-emitter threshold voltage $V_{GE(th)}$ of the IGBT, $v_{GE} < V_{GE(th)}$ acc. to Figure 4, within a period of typically 135 ns. The value of the preboost current I_{PRB} is proportional to the voltage V_{PRB} at terminal PRB with reference to V_{VEE2}. The maximum voltage V_{PRB} with reference to V_{VEE2} is 5 V. The preboost current I_{PRB} is defined as:

$$I_{PRB} = \left|\frac{2 \cdot (V_{PRB} - V_{VEE2})}{3 \cdot RS}\right| \quad (3)$$

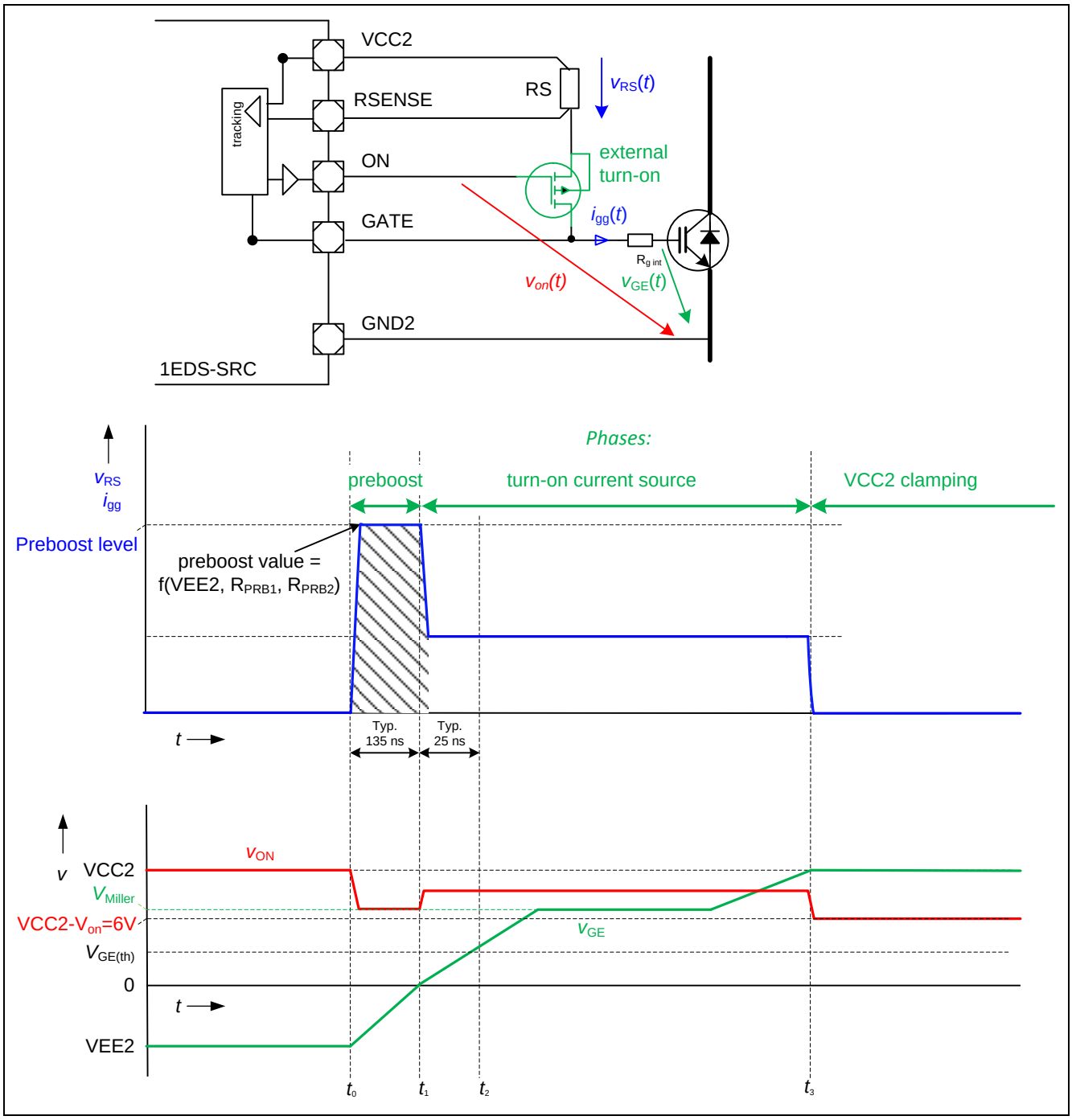

Figure 4 Timing diagram of the turn-on process

It is best practice in board layout engineering to keep tight proximity of the control loop to avoid oscillations. The control loop consists of driver IC, sense resistor, and p-channel MOSFET.

The preboost timer is always active, both in bipolar or unipolar power supply configuration. The only exception is, if the IGBT is turned on via EN according to section 2.4.

The preboost current I_{PRB} is set by a simple voltage divider for bipolar gate supply as well as for unipolar supply. In case of bipolar power supply, the voltage divider is connected between GND2, PRB, and VEE2. In case of a unipolar power supply, use VCC2, PRB, and VEE2 according to Figure 5.

The selected preboost current amplitude should charge the IGBT gate from the voltage V_{VEE2} to a value between 0 and the gate-emitter threshold voltage $V_{GE(th)}$ of the IGBT within 135 ns. The corresponding IGBT gate charge curves must be considered for the various collector-emitter voltages V_{CE} for best accuracy.

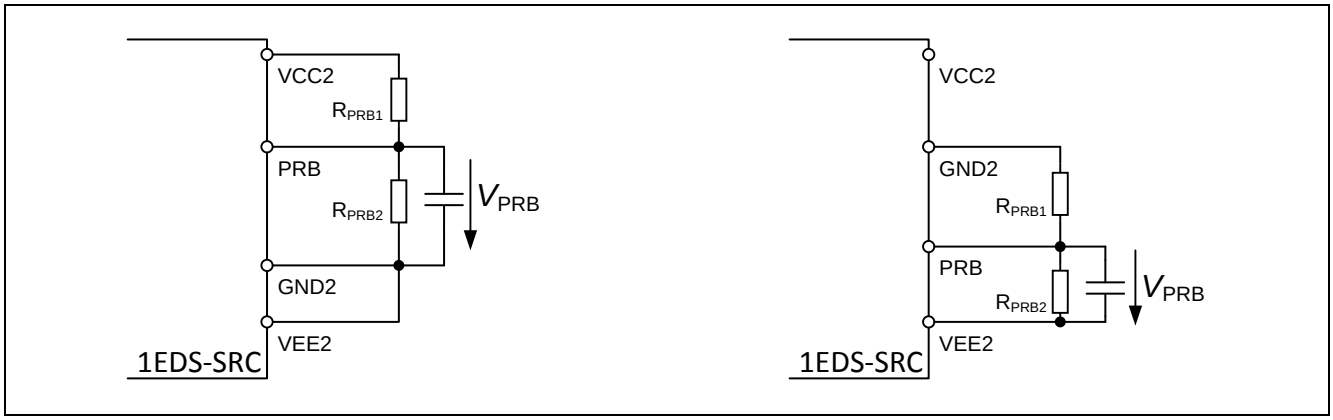

Figure 5 External circuit for setting of preboost current, unipolar supply to the left, bipolar supply to the right

2.8.2 Turn-on phase

The change from the preboost phase into the turn-on phase needs typically 25 ns. This time should be considered for the setting of the preboost current amplitude in order not to overcharge the gate until the turn-on phase starts.

The gate current during the turn-on phase can be selected pulse-by-pulse out of 11 levels for the proper adjustment of the turn-on transition. The partitioning into 11 different levels allows a highly accurate control. The driver IC controls the voltage drop across the sense resistor RS. The corresponding gate current I_{gg} is

$$I_{gg} = \frac{V_{RS}}{RS} \tag{4}$$

The real-time adjustment of the gate current for the turn-on phase is accomplished with terminal SPEED on the input side. Terminal SPEED is an input terminal that accepts voltage levels between 0 V and 3.3 V. The lowest voltage at terminal SPEED corresponds to the highest gate current level. The highest level would also be achieved by connecting SPEED to PADN.

2.8.3 Clamping phase

Finally, the IGBT gate voltage saturates at V_{VCC2} in the VCC2 clamping phase. The driver clamps the gate voltage of the external P-channel transistor 6 V below V_{VCC2} according to Figure 4. This provides a low-impedance connection between the gate of the IGBT and the supply of V_{VCC2}.

2.9 Overcurrent protection mechanisms

The IC features short circuit detection by desaturation (DESAT) monitoring as well as a sense input (CS) to externally trigger overcurrent events. The IC is latched in protection mode with the output switched off, when the function OCOFF according to section 2.9.3 is disabeld.

2.9.1 Short Circuit detection by DESAT function

Desaturation shut down protection ensures the protection of the IGBT in case of short circuit. This protection function is activated only during turn-on state of the IGBT. The collector-emitter voltage of the IGBT is below 3 V at rated operation for modern IGBT types. The DESAT current source injects 500 µA into the external circuit according to Figure 6 and charges the DESAT capacitor C_{DESAT}. The voltage at this capacitor reaches the voltage of

$$V_{DESAT} = v_T + V_{DDESAT} + V_{RDESAT} = v_T + 0.7\,V + 500\mu A \cdot R_{DESAT} \quad (5)$$

The output is driven low by soft turn-off, when the desaturation voltage on terminal DESAT reaches 9 V and the /FLT output terminal is activated. The blanking time is determined by the combination of the highly precise internal current source (± 10%) and an external capacitor. The blanking time $T_{DESATBLANK}$ is given with

$$T_{DESATBLANK} = \frac{V_{DESAT} \cdot C_{DESAT}}{I_{DESAT}} = \frac{9\,V \cdot C_{DESAT}}{500\,\mu A} \quad (6)$$

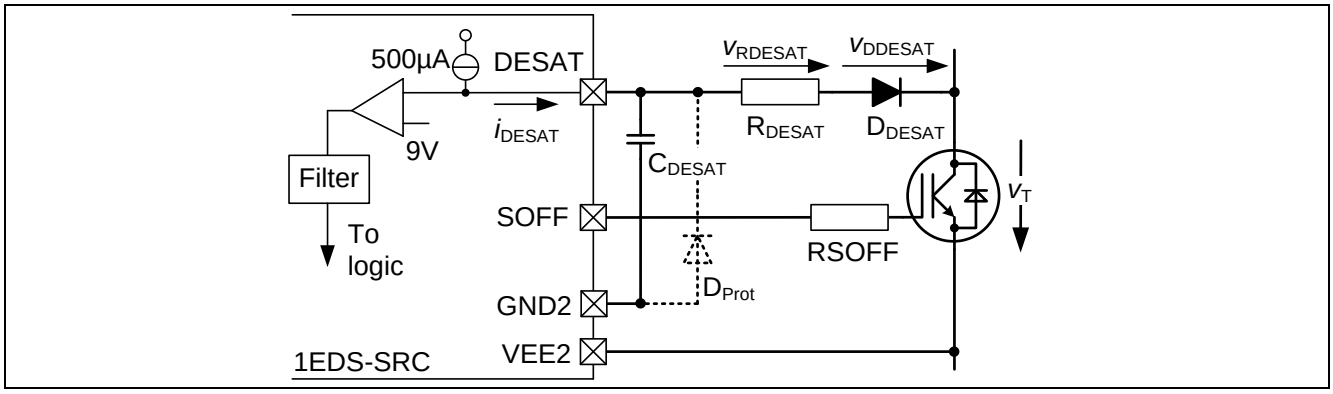

Figure 6 Desaturation detection circuit of the 1EDS-SRC

The diode D_{Prot} is optional. The IC's functionality is not corrupted, if the diode is not placed. However, turn-on d*v*/dt effects may pull down terminal DESAT slightly negative, so that the blanking time $T_{DESATBLANK}$ is different.

Desaturation protection is set active at $T_{DESATleb}$ = 400ns after the preboost phase. The shutdown process is initiated when the desaturation filter time $T_{DESATFIL}$ is elapsed. The full desaturation shut down timing including the fault report to the input side and reset is shown in Figure 7.

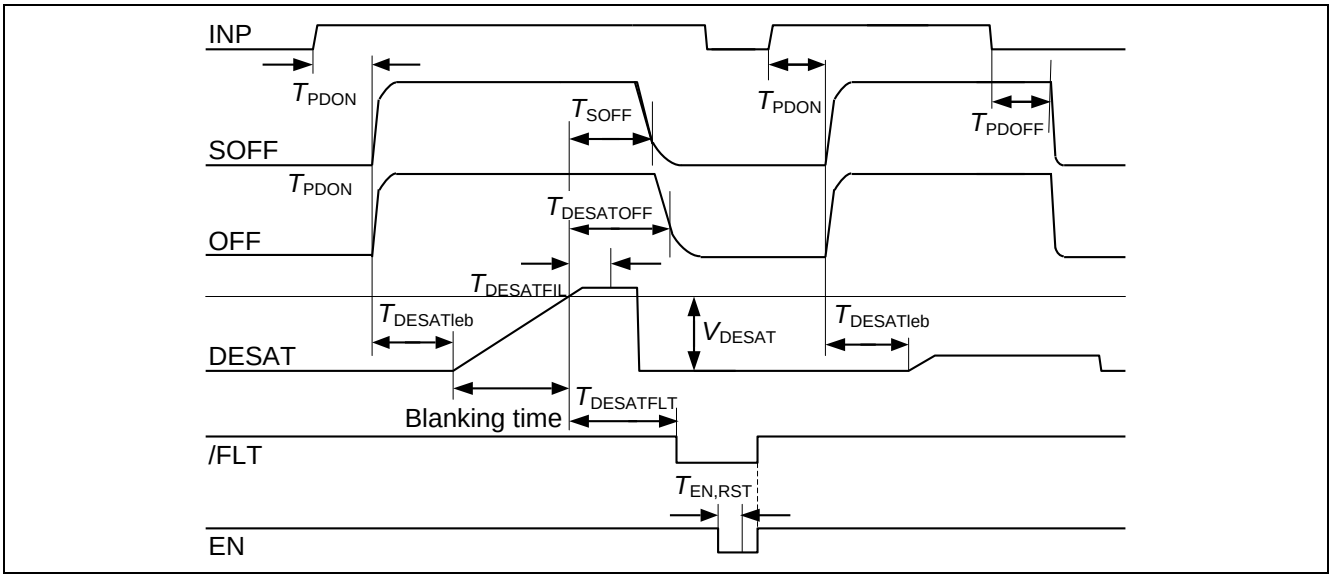

Figure 7 Timing for DESAT events incl. signals at the terminals SOFF, /FLT and EN

All incoming turn-off signals are automatically executed as a soft turn-off, when a DESAT event is detected. This means, that the filter- and blanking times $T_{DESATleb}$, $T_{DESATBLANK}$ and $T_{DESATFIL}$ are elapsed. Please note that a turn-off command, which arrives during a short circuit event but before $T_{DESATFIL}$ is passed, is still executed as hard turn-off and a considerably high voltage overshoot can occur. This can be actively avoided when using the two-level turn-off function according to section 2.10.

The output is latched to off-state after a DESAT event took place. A logical low pulse longer than 870 ns to the EN-pin is interpreted as a reset signal, putting the IC back to normal function again. The output reacts according to the input signals INP and INN with the exception that there is no preboost phase in case of a potential turn-on.

2.9.2 Overcurrent protection utilizing the current sense input (CS)

The IGBT overcurrent detection is a protection feature that makes use of the information gained by sensing the emitter current. This can be combined with current-sense IGBTs or standard IGBTs by using an emitter shunt resistor or a current transducer. The voltage at pin CS is forwarded to a comparator that triggers at 0.35 V according to Figure 8. The current sense signal at terminal CS is ignored while the IGBT is in off state. An external blanking circuit may be necessary to prevent false tripping during turn-on. With non-sensing IGBT types, a low resistive shunt is used to sense the emitter current. When a short circuit is detected, the IGBT is switched off by a soft turn-off. The fault status is signaled on terminal /FLT. The fault status has to be reset via terminal EN. IGBT overcurrent detection is set active 420ns after the preboost phase.

Both the desaturation and the current sense feature can be used at the same time. In this case, the terminal CS may be used as a free, pre-biased comparator in order to cover monitor functions, e.g. for temperatures, while the DESAT function protects against short circuit.

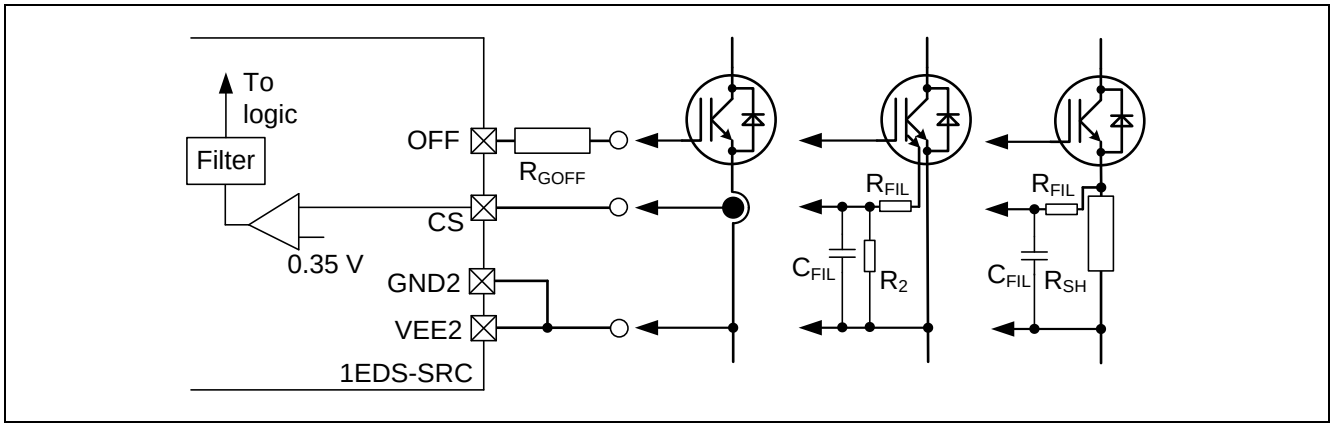

Figure 8 Current sense circuit of 1EDS-SRC with various options of current sense techniques

The full current sense shut down timing including the fault report to the input side and reset is shown in Figure 9.

All incoming turn-off signals are automatically executed as a soft turn-off, when a CS event is detected correctly. This means that the blanking time $T_{CS,blank}$ is passed. Please note here that a turn-off command, which arrives during a short circuit event but before $T_{CS,blank}$ is passed, is still executed as hard turn-off and a considerably high voltage overshoot can occur. This can be actively avoided, when using the two-level turn-off function acc. to section 2.10.

The output is latched to off-state after a DESAT or CS event took place. A logical low pulse longer than 870 ns to pin EN is interpreted as a reset signal, putting the IC back to normal function. The output reacts according to the input signals INP and INN with the exception that there is no preboost phase in case of a potential turn-on.

The terminal CS should be connected to GND2 to deactivate the CS function.

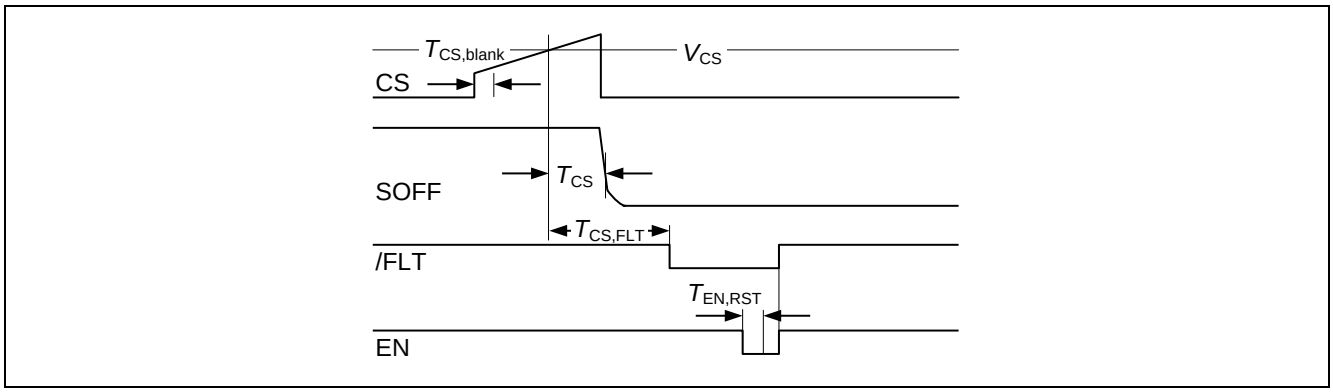

Figure 9 Timing for CS events including signals at terminals CS, SOFF, /FLT and EN

2.9.3 Overcurrent protection ON/OFF

It is well known that overvoltage events can occur in three-level inverters of NPC1 topology, when the inner two IGBT are turned off prior to the outer two IGBT. Such a situation can be handled properly by the 1EDS-SRC. If the terminal OCOFF is connected to GND2 or left unconnected, the IGBT is switched off via a soft turn-off in case of a CS or DESAT event. If the terminal OCOFF is connected to VCC2, the IGBT is not switched off in such cases. However, the signaling of CS or DESAT events to the output /FLT is done in any case.The IGBT can be turned off externally instead via control input EN. The reset procedure is the same in this case as seen in sections 2.9.1 and 2.9.2

2.10 Two-level turn-off (TLTO)

The TLTO function is activated, if a capacitor is applied between terminal CZ and terminal VEE2. It affects any turn-on and turn-off process, which is either initiated by the input signals INP, INN or EN or by any protection function on the output side. Connecting terminal CZ to terminal VEE2 will deactivate the two-level turn-off function.

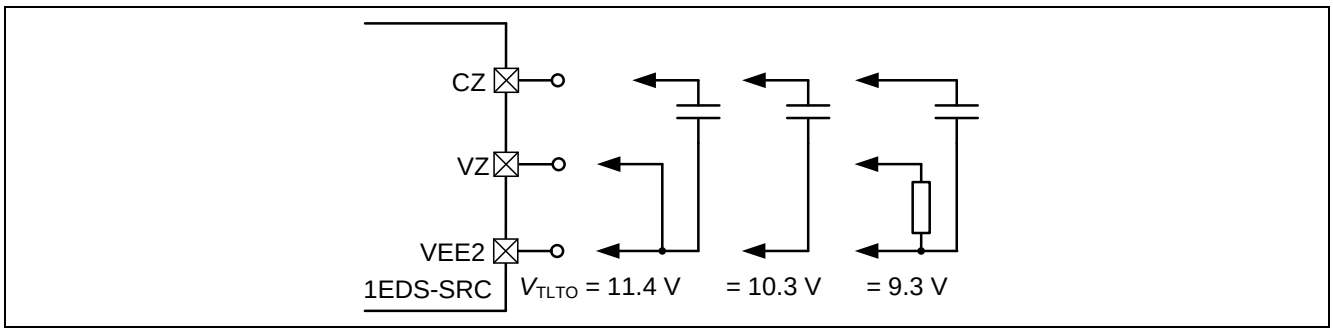

Figure 10 Two-level turn-off options

The two-level turn-off introduces a second, lower gate voltage level during the turn-off process according to Figure 11. The second gate voltage level reduces the channel conductivity of the IGBT when reaching this level. The obtained di_C/dt is therefore smaller and generates less induced overvoltage. The TLTO function is the only way to avoid excessive overvoltage during turn-off at any time. The required timing, which can be adjusted by the capacitance at terminal CZ, depends on stray inductance and overcurrent at the beginning of the two-level turn-off period.

Three voltage levels are available:

- The voltage level is set to V_{TLTO1} = 11.4 V if terminal VZ is connected to VEE2,
- the voltage level is set to V_{TLTO2} = 10.3 V if terminal VZ is floating,
- the voltage level is set to V_{TLTO3} = 9.3 V if terminal VZ is connected to VEE2 via a 27 kΩ resistor

The second voltage level is set in a way that turn-off losses are the same as during normal turn-off for nominal current values. The turn-on signal is delayed by the duration of the two-level turn-off in order to achieve identical pulse lengths. The duration T_{TLSET} of the plateau is set by the capacitor connected between terminals CZ and VEE2.

The IC starts charging the capacitance on CZ for obtaining the two-level set time T_{TLSET}, when a turn-on signal is given. The IC starts the turn-on sequence and resets the capacitor at terminal CZ as soon as the voltage at terminal CZ exceeds 2.5 V.

The IC additionally activates a soft turn-off sequence if a turn-off is initiated due to a desaturation condition on terminal DESAT.

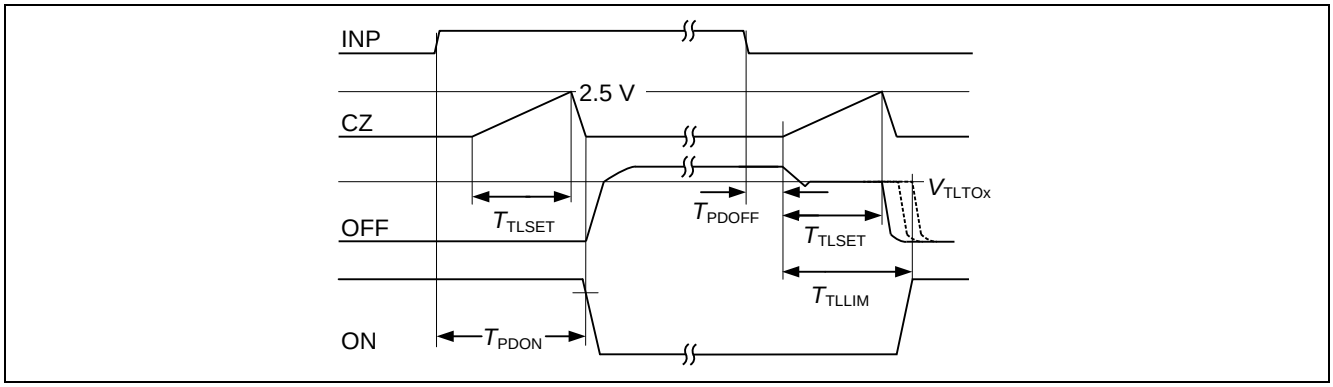

Figure 11 Timing for two-level turn-off

3 Typical application schematic

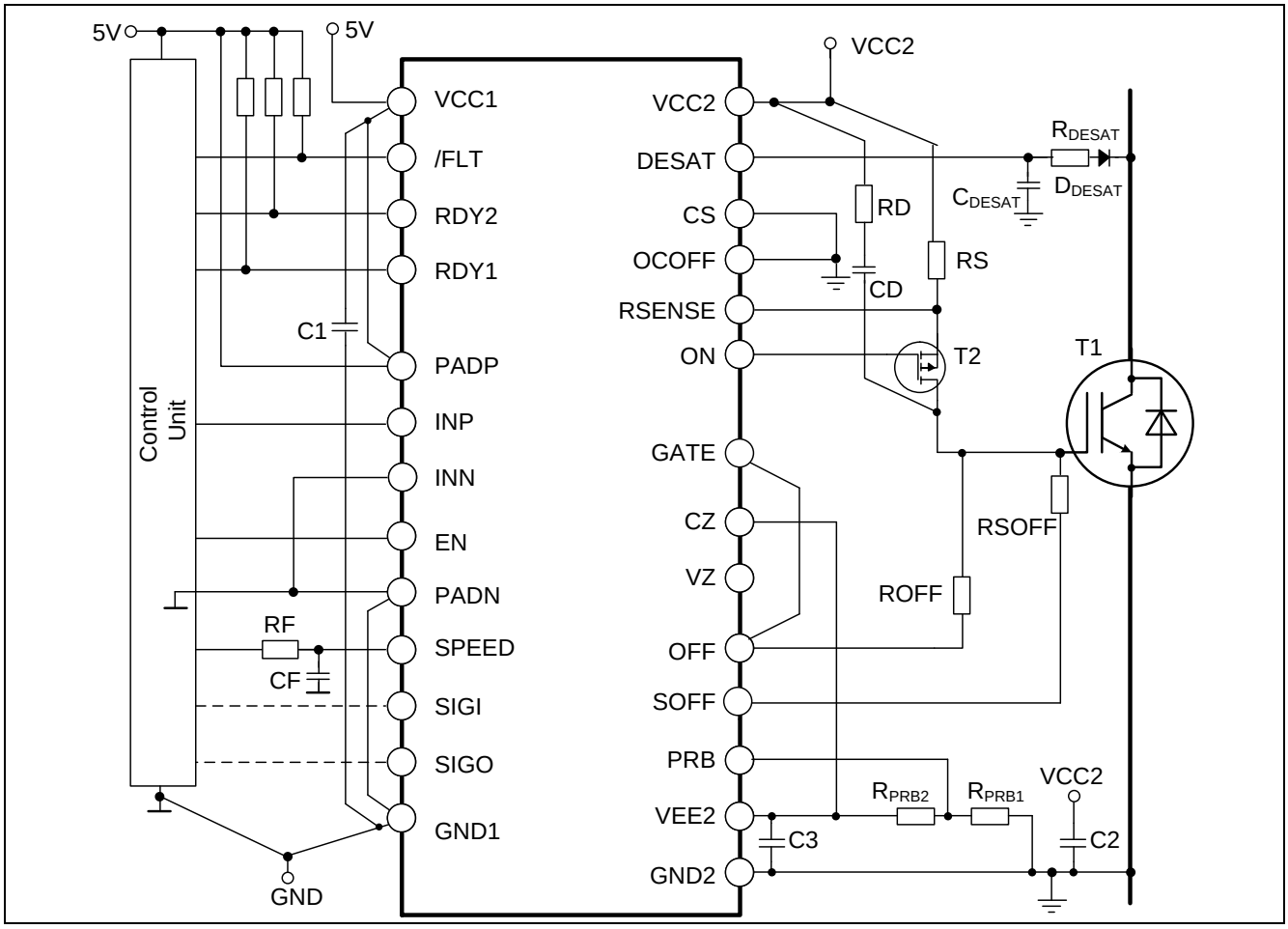

Figure 12 Typical application schematic for bipolar gate supply, soft turn-off and desaturation detection; terminal SPEED is controlled by the microcontroller

4 Design considerations

This section derives and executes the equations for external components and proper operation.

4.1 Turn-on gate current control loop

The gate current control loop for turn-on is the heart of the 1EDS-SRC. The design idea for this section is only slightly different compared to common voltage source IC. The number of components is similar and the aspects of the key components remain identical in terms of power dissipation and layout. The application of the 1EDS-SRC is therefore neither more complex nor more complicated compared to other gate drive ICs which need an external booster circuit.

The gate current control loop function can be described by two equations; hence there are two degrees of freedom for tuning the control loop. This allows achieving

- a strong preboost current and a considerably lower range of gate currents during turn-on phase. In this case a fine resolution of levels 1 to 11 is given. Or
- a large range of turn-on currents including the preboost value or even more than this. In this case the resolution of the 11 steps is rougher and therefore more visible.

The following sections describe the second approach, where the turn-on gate current I_{gg} covers a large range including the preboost value

The gate current control loop is very sensitive to stray inducatnces of the layout. It is important to have extremely short distances between the blocking caps of V_{VCC2}, the shunt resistor RS and the p-channel transistors. Distances of longer than 1 cm can already have negative effects on the gate current waveforms.

4.1.1 Calculation of the preboost current amplitude

The preboost current amplitude is set by means of the voltage divider at terminal PRB. The equation for the preboost current I_{PB} is given with the amount of gate charge to be injected into the gate and the preboost time period of T_{PRB} = 135 ns typ. It is important to note, that the gate-emitter voltage at the end of the preboost phase must be lower than the gate-emitter threshold voltage $V_{ge(th)}$ including its variations over temperature. The amplitude of I_{PB} is

$$I_{PB} = \frac{\Delta Q_{G,PRB}}{T_{PRB}} = \frac{\Delta Q_{G,PRB}}{135\ \text{ns}} \tag{7}$$

The charge needed is to be obtained out of the gate charge curve for the dedicated IGBT in use, covering the range of the gate voltage. This may even include negative gate-emitter voltages, when applicable.

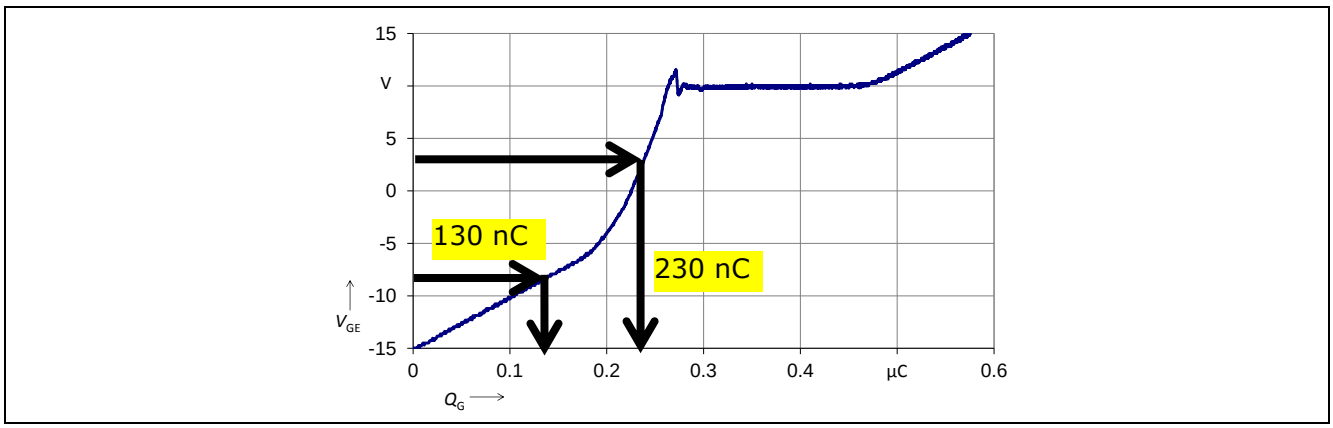

Figure 13 Example of gate charge curve from -15 V ≤ V_{GE} ≤ +15 V for FP75R12KT4

The preboost amplitude is calculated for an IGBT-module FP75R12KT4 acc. to Figure 13, when starting at a gate voltage of V_{VEE2} = - 8 V and ending at a gate voltage of $V_{GE(th)}/2 \approx 3$ V:

$$I_{PB} = \frac{\Delta Q_{G,PRB}}{135\ \text{ns}} = \frac{230\ \text{nC} - 130\ \text{nC}}{135\ \text{ns}} = \frac{100\ \text{nC}}{135\ \text{ns}} \approx 0.75\ \text{A}$$

Please note that the preboost amplitude can also be adjusted with the voltage divider at terminal PRB according to equation (3) as well as with the gate current sense resistor RS. This is explained in the following two sections.

4.1.2 Calculation of the gate current sense resistor

The gate current measurement resistor RS is a key element of the gate current control loop. The voltage drop across RS is the feedback signal for the control loop. Therefore, the value should be large enough in order to provide a stable feedback signal, so that the control loop can work precisely. It is a rule of thumb to correlate the preboost current value to I_{gg} gate current level 10 of the SPEED matrix of Table 4. The highest current during turn-on phase, thus the fastest turn-on of the IGBT, occurs with the same current amplitude as the preboost. The controllable range of turn-on gate current is then down to 20% of I_{PB}. This range is usually sufficient to achieve a d*v*/dt value of the IGBT collector-emitter voltage of 5 kV/µs or lower.

When using the example of section 4.1.1, the current sense resistor value *RS* is given by equation (8):

$$RS = \frac{V_{\mathrm{RS,10}}}{I_{\mathrm{gg,max}}} = \frac{1\,\mathrm{V}}{0.75\,\mathrm{A}} \approx 1.3\,\Omega \tag{8}$$

4.1.3 Voltage divider at terminal PRB

The preboost current I_{PB} = 2/3·(V_{PRB} - V_{VEE2}) / *RS* as given in section 2.8.1, where *RS* is the resistance of the current sense resistor RS. The previous section 4.1.2 explained the calculation of RS, which now allows calculating the bias voltage at terminal PRB. The pin PRB is referenced to VEE2. There are two ways of biasing the terminal PRB depending of the supply configuration of the output side according to Figure 5 in section 2.8.1.

The simplest way to bias is using a voltage divider. The divider is connected between VCC2 and VEE2 = GND2 for unipolar gate supply, e.g. 0 ≤ v_{ge} ≤ 15 V. It is sufficient for bipolar supply, e.g. -8 V ≤ v_{ge} ≤ 15 V, to have the divider only between the terminals GND2 and VEE2 as given in the right part of Figure 5. The voltage of terminal PRB is

$$V_{\mathrm{PRB}} = V_{\mathrm{VCC2}} \cdot \frac{R_{\mathrm{PRB2}}}{R_{\mathrm{PRB1}} + R_{\mathrm{PRB2}}} \qquad \text{for unipolar gate voltage} \tag{9}$$

$$V_{\mathrm{PRB}} = V_{\mathrm{VEE2}} \cdot \frac{R_{\mathrm{PRB2}}}{R_{\mathrm{PRB1}} + R_{\mathrm{PRB2}}} \qquad \text{for bipolar gate voltage} \tag{10}$$

A small capacitor in parallel to R_{PRB2} can filter noise and reduce coupling effects of parasitic elements. The values of R_{PRB1} and R_{PRB2} should be selected rather high for low current consumption concerning the VEE2 supply. The example in section 4.1.1 is further evaluated by means of equations (3) and (10) with V_{VEE2} = - 8 V, I_{PB} = 0.75 A, RS = 1.3 Ω and R_{PRB2} = 10 kΩ.

$$R_{\mathrm{PRB1}} = \frac{\frac{2}{3} \cdot \left|V_{\mathrm{VEE2}}\right| - I_{\mathrm{gg}} \cdot RS}{I_{\mathrm{gg}} \cdot RS} \cdot R_{\mathrm{PRB2}} = \frac{\frac{2}{3} \cdot 8\,\mathrm{V} - 0.75\,\mathrm{A} \cdot 1.3\,\Omega}{0.75\,\mathrm{A} \cdot 1.3\,\Omega} \cdot 10\,\mathrm{k\Omega} = 44.7\,\mathrm{k\Omega} \tag{11}$$

Now the complete slew rate control circuit is determined. The consumption of the divider circuit is 160 µA,

4.1.4 RC damping element

The parasitic gate-collector capacitance injects a displacement current into the turn-on loop, especially at fast turn-on according to Figure 14. This acts as a positive feedback for the control and may lead to oscillations with layout inductances. The selection of the values for CD and RD also depends on the individual PCB layout in respect to parasitic inductances and capacitances. Therefore, an experimental confirmation for the absence of oscillations is mandatory, by starting with with *CD* ≈ C_{res} and *RD* ≈ 10·*RS*.

The optimization of RD and CD values may first go for higher CD values. The target is to achieve a piecewise constant gate current and gate voltage waveforms according to Figure 4 The gate current control loop is very sensitive to stray inducatnces of the layout. It is important to have extremely short distances between the blocking caps of V_{VCC2}, the shunt resistor RS and the p-channel transistors. Distances of longer than 1 cm can already have negative effects on the gate current waveforms.

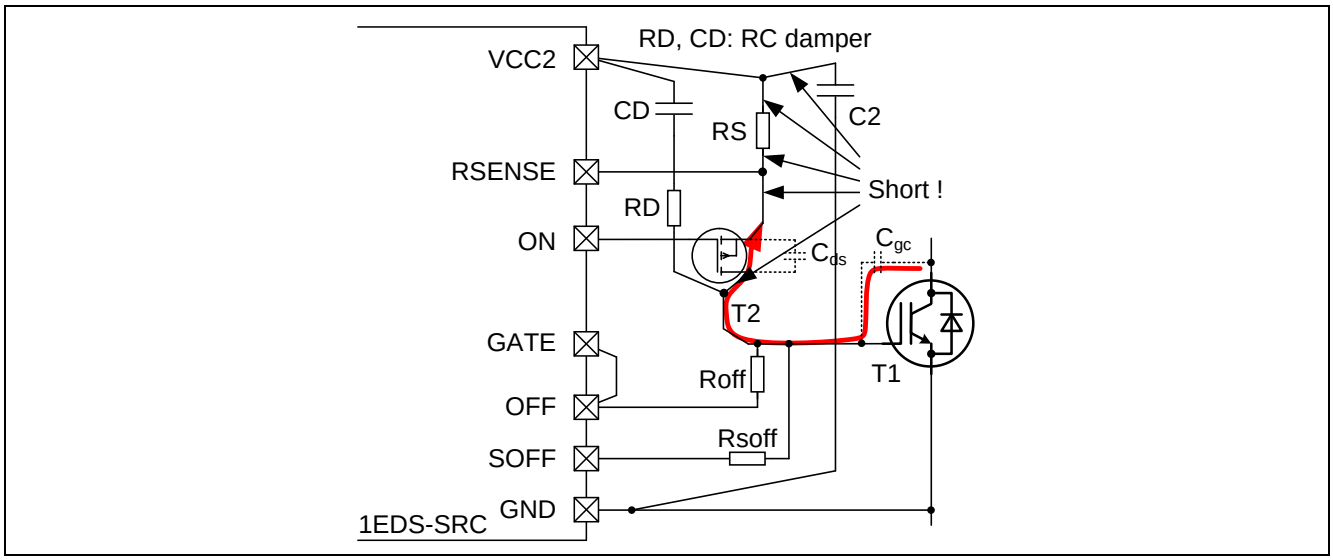

Figure 14 Injection path of capacitive current during fast turn-on (red) and damping circuit comprising of CD and RD

4.2 Calculation of power dissipation of the IC and its external key components

This section derives the equations for the power dissipation of the IC and its external key components. The major portion is dissipated during the preboost and the the turn-on phase. The power dissipation of the clamping phase is added therefore to the turn-on phase.

4.2.1 Power dissipation of the p-channel MOSFET

The instantaneous power dissipation of the p-channel MOSFET T2 according to Figure 14 and the current sense resistor RS is divided into the three phases preboost, turn-on and clamp. Each of the portions contributes to heat generation with dedicated average power dissipation.

The drain-source voltage of the p-channel MOSFET is not constant over the complete turn-on process, because it is controlled in current source mode. The MOSFET can be considered to represent a variable resistor. The gate current to be injected during the preboost phase can be handled like the charging current from a constant capacitance. The equivalent input capacitance during the preboost is assumed to be

$$C_{\text{ies,PRB}} = \frac{\Delta Q_{\text{G,PRB}}}{V_{\text{GE,PRB}} - V_{\text{VEE2}}} = \text{constant} \tag{12}$$

where $V_{\text{GE,PRB}}$ is the gate-emitter voltage at the end of the preboost phase.

The drain-source voltage of the p-channel FET during the preboost phase is characterized by

$$v_{\text{DS}}(t) = V_{\text{VCC2}} - V_{\text{VEE2}} - I_{\text{PB}} \left(RS + \frac{t}{C_{\text{ies,PRB}}} \right) \tag{13}$$

The calculated average power dissipation of the transistor in current source mode is

$$\begin{aligned} P_{\text{d,PMOS,avg1}} &= f_{\text{P}} \cdot \int_0^{T_{\text{PRB}}} I_{\text{PB}} \left(V_{\text{VCC2}} - V_{\text{VEE2}} - I_{\text{PB}} \left(RS + \frac{t}{C_{\text{ies,PRB}}} \right) \right) dt \\ &= f_{\text{P}} \cdot I_{\text{PB}} \cdot T_{\text{PRB}} \cdot \left(V_{\text{VCC2}} - V_{\text{VEE2}} - I_{\text{PB}} \cdot RS - I_{\text{PB}} \frac{T_{\text{PRB}}}{2 \cdot C_{\text{ies,PRB}}} \right) \end{aligned} \tag{14}$$

The average power dissipation during the turn-on phase T_{on} with constant current I_{gg} is

$$P_{\mathrm{d,PMOS,avg2}} = f_{\mathrm{P}} \cdot \int_0^{T_{\mathrm{on}}} I_{\mathrm{gg}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{GE,PRB}} - I_{\mathrm{gg}} RS\right) dt$$
$$= f_{\mathrm{P}} \cdot I_{\mathrm{gg}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{GE,PRB}} - I_{\mathrm{gg}} RS\right) \cdot T_{\mathrm{on}} \quad (15)$$

The interval T_{on} is a function of the setting at terminal SPEED.

$$T_{\mathrm{on}} = \frac{Q_{\mathrm{G,rest}}}{I_{\mathrm{gg}}} \quad (16)$$

The power dissipation in the turn-on phase which is given in equation (15) simplifies to

$$P_{\mathrm{d,PMOS,avg2}} = f_{\mathrm{P}} \cdot Q_{\mathrm{G,rest}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{GE,PRB}} - I_{\mathrm{gg}} RS\right) \quad (17)$$

Equation (17) shows that the power dissipation depends on the current level during the turn-on phase: The power dissipation is highest with the smallest instantaneous turn-on current level.

The total loss is the sum of the portions given in equation (14) and (17) :

$$P_{\mathrm{d,PMOS,tot}} = P_{\mathrm{d,PMOS,avg1}} + P_{\mathrm{d,PMOS,avg2}} \quad (18)$$

4.2.2 Power dissipation of the gate current sense resistor

The calculation of the average power losses of the current sense resistor is not as complex as for the FET. It is a good approximation to assume a rectangular current shape during the preboost section and with different amplitude also during the turn-on section. The total rms value of the current which flows through the current sense resistor is

$$I_{\mathrm{RS,rms}} = \sqrt{I_{PB}^2 \cdot 135\mathrm{ns} \cdot f_{\mathrm{P}} + I_{\mathrm{gg}}^2 \cdot T_{\mathrm{on}} \cdot f_{\mathrm{P}}} \quad (19)$$

where T_{on} is the duration of the turn-on phase and can be calculated according to (16). This includes already the portion of the clamp phase. The total power dissipation $P_{d,RSrms}$ of the shunt therefore is

$$P_{\mathrm{d,RSrms}} = I_{\mathrm{RS,rms}}^2 \cdot RS \quad (20)$$

4.2.3 Power dissipation of the gate current control IC

The power dissipation of the gate current control IC contains:

- Input supply current I_{VCC1} at terminal VCC1

$$P_{\mathrm{d,VCC1}} = I_{\mathrm{VCC1}} \cdot V_{\mathrm{VCC1}} \quad (21)$$

- Input supply current I_{PADP} at terminal PADP

$$P_{\mathrm{d,PADP}} = I_{\mathrm{PADP}} \cdot V_{\mathrm{PADP}} \quad (22)$$

- The sum of input bias currents of logic terminals which is usually neglectable

$$P_{\mathrm{d,IN}} = \sum_i I_{\mathrm{IN,i}} \cdot V_{\mathrm{IN,i}} \quad (23)$$

- Input supply current I_{VCC2} and I_{VEE2} at terminals VCC2 and VEE2, respectively

$$P_{\mathrm{d,VCC2}} = I_{\mathrm{VCC2}} \cdot V_{\mathrm{VCC2}} \qquad P_{\mathrm{d,VEE2}} = I_{\mathrm{VEE2}} \cdot V_{\mathrm{VEE2}} \quad (24)$$

- Sink current I_{OUT} at terminal OUT, if no external boost circuit is used

$$P_{\mathrm{d,OUT}} = \frac{1}{2} Q_{\mathrm{G,tot}} (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) f_{\mathrm{P}} \frac{2.3\ \Omega}{2.3\ \Omega + (ROFF + R_{\mathrm{Gint}})} \quad (25)$$

  where $Q_{G,tot}$ is the gate charge to be handled, when discharging the gate from V_{VCC2} to V_{VEE2}, *ROFF* is the turn-off gate resistor and R_{Gint} is the IGBT's integrated gate resistor. The IC's power dissipation may

be neglected in case of an external boost circuit, because the driving power for a typical pnp-transistors is very small.

The total power dissipation of the IC is the sum of results gathered from equations (21) to (25).

4.3 Calculation of the desaturation detection circuit

The timing of the DESAT function and the CS function is essential in order to avoid potential damage of the affected IGBT. Two portions contribute to the shutdown delay:

- IC related filter- blanking times and propagation delays
- IGBT related turn-off characteristics

This application note mainly focuses on the IC related timings and does not consider IGBT related items in detail. It is therefore important to evaluate the (soft) turn-off behavior in conjunction with the IGBT, which can vary over operating conditions, such as junction temperature, collector current, gate supply or (soft) turn-off gate resistor.

The short circuit withstand time of a 1200 V IGBT usually is T_{SC} = 10 µs. For 600 V IGBT less than 10 µs is common, the according numbers can be taken from the datasheets. The condition for safe turn-off timing is

$$\begin{aligned} T_{\max} &= T_{\mathrm{DESATleb}} + T_{\mathrm{DESATBLANK}} + T_{\mathrm{SOFF}} + T_{\mathrm{IGBT,off}} < T_{\mathrm{SC}} \quad \text{for DESAT} \\ T_{\max} &= 3\tau_{\mathrm{FIL}} + T_{\mathrm{CS,blank}} + T_{\mathrm{CS}} + T_{\mathrm{IGBT,off}} < T_{\mathrm{SC}} \quad \text{for CS} \end{aligned} \tag{26}$$

The parameters $T_{DESATleb}$ and T_{SOFF} for DESAT and the parameters $T_{CS,blank}$ and T_{CS} for the CS case are given in the 1EDS-SRC datasheet. The value τ_{FIL} is the time constant of the external filter at terminal CS, which consists of the components R_{FIL} and C_{FIL} according to Figure 8. The DESAT blanking time $T_{DESATBLANK}$ is given with the charging characteristic of a capacitor from a current source:

$$T_{\mathrm{DESATBLANK}} = \frac{C_{\mathrm{DESAT}}\, V_{\mathrm{DESAT}}}{I_{\mathrm{DESAT}}} \tag{27}$$

It can be seen in this equation, that the DESAT capacitor basically defines the blanking time

A good selection for the DESAT resistor is R_{DESAT} = 1 kΩ.

Maybe some designs do not use the DESAT function. It is recommended in this case to pull down the terminal DESAT to GND with a resistor of 1 kΩ.

4.4 Calculation of the two-level set time

The TLTO set time can be selected with the external capacitor at terminal CZ. The IC contains an integrated current source of typ. I_{CZ} = 950 µA which charges the external capacitance linearly. Therefore the external capacitance is defined by

$$C_{\mathrm{CZ}} = \frac{T_{\mathrm{TLSET}} \cdot I_{\mathrm{CZ}}}{V_{\mathrm{TLTO,th}}} = \frac{T_{\mathrm{TLSET}} \cdot 950\ \mu\mathrm{A}}{2.5\ \mathrm{V}} \tag{28}$$

It is not necessary to calculate a longer two-level set time T_{TLSET} than 5 µs, because the watch dog timer will turn-off the gate anyway after 5 µs. This is shown in Figure 15.

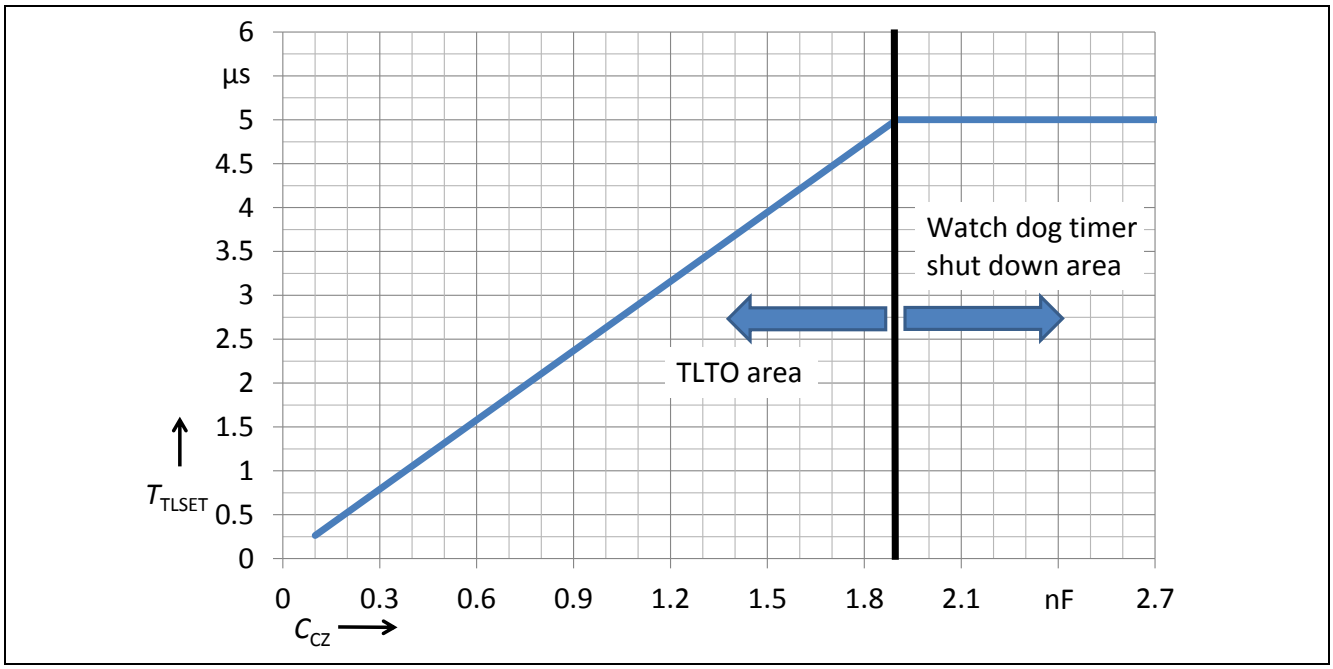

Figure 15 Two-level set time as a function of the capacitance at terminal CZ

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