IPD Protect: features description and design tips

About this document

Scope and purpose

The scope of the document is to describe the features of the Integrated Power Device (IPD) Protect and to provide tips for a proper design. This is a device specifically designed for induction cooking applications, which are based on a single-ended parallel resonant converter (SEPR). The part number of this device is IEWS20R5135IPB.

The IEWS20R5135IPB consists of a 20 A, 1350 V TRENCHSTOP™ reverse-conducting RC-H5 IGBT, co-packed with a smart IC, which acts as a gate driver for the IGBT, and implements unique protection features.

Intended audience

The application note is intended for designers who would like to design the IEWS20R5135IPB in an SEPR converter.

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1 Introduction

1.1 Description of the target application

Induction heating (IH) cookers are very popular today because of the many benefits they offer such as high energy efficiency and accurate heating power control. Typically, IH cookers use resonant converter topologies due to their soft switching operation, which reduces converter switching losses and EMI [1]. The SEPR topology has been used for many years in table-top cooker appliances with a power range up to 2.2 kW. However, the use of SEPR solutions is now also expanding to include multi-hob stove applications, mainly due to lower system costs. As shown in Figure 1.1, the SEPR converter is a single-switch-based topology, in which a >1200V IGBT is usually used. Due to the required bi-directionality of the switch, reverse-conducting IGBTs (RC IGBTs) are mainly used in this application [2]. Regulation of the cooking power is achieved by means of IGBT on-time control.

The main limitation of SEPR induction heating cookers is the uncontrolled high resonant voltage which requires high-voltage devices to be used. Since the voltage of the grid is amplified by the resonance, the collector node of the IGBT experiences very high voltage during the main switching cycle, according to the collector current peak (Figure 1.2, condition 3). Depending on the resonant network design, and the characteristic impedance of the load, a typical peak collector-emitter voltage of 1100 V can be reached.

Even though the system is well-designed to make the IGBT operate under safe conditions, there are still situations in which the IGBT limits could be exceeded (Figure 1.2, conditions 1, 2, 4 and 5). Figure 1.2 summarizes the different operating conditions to which the IGBT can be exposed in the application:

1) Very high collector current spikes during the initial turn-on due to the charging of the resonant capacitor. For well-designed layouts, the peak current is mainly limited by the IGBT transconductance.

2) High turn-on collector current spikes due to the loss of zero-voltage switching conditions (IGBT turns on when the resonant capacitance is not completely charged).

3) Normal operation, with zero-voltage switching at the IGBT turn-on, and soft switching at IGBT turn-off.

4) Peak turn-off collector current higher than the maximum IC allowable by the safe operating area (SOA) of the IGBT.

5) Peak collector-emitter voltage higher than the maximum breakdown voltage of the IGBT.

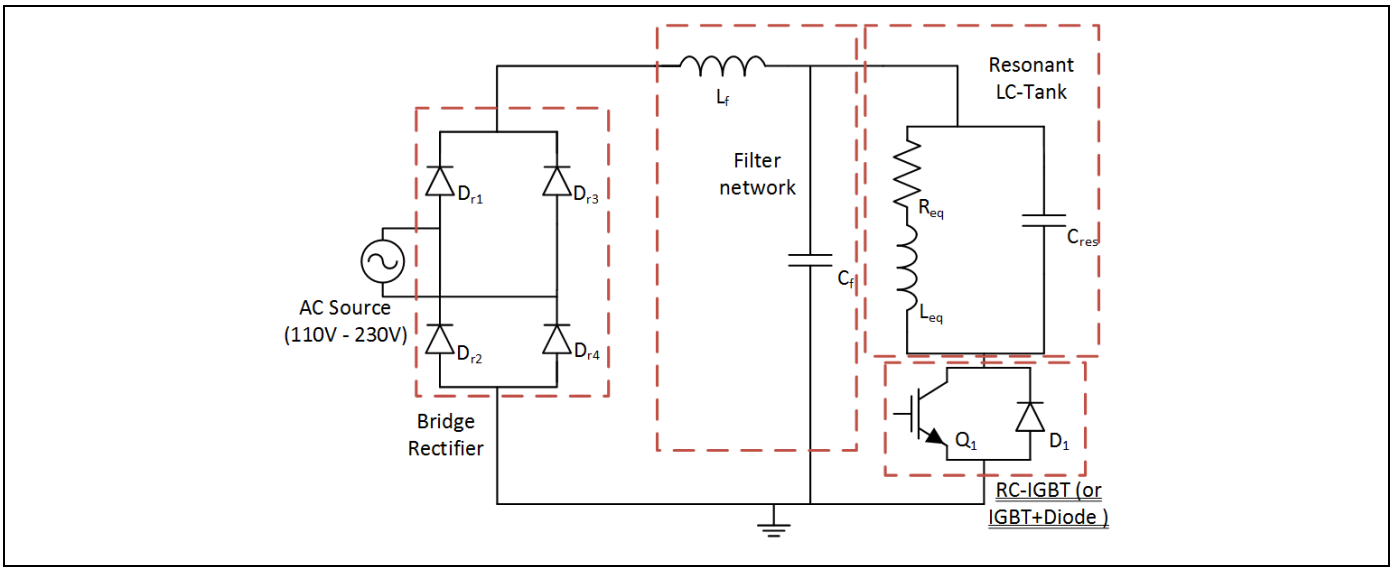


Figure 1.1: Typical SEPR cooker schematic

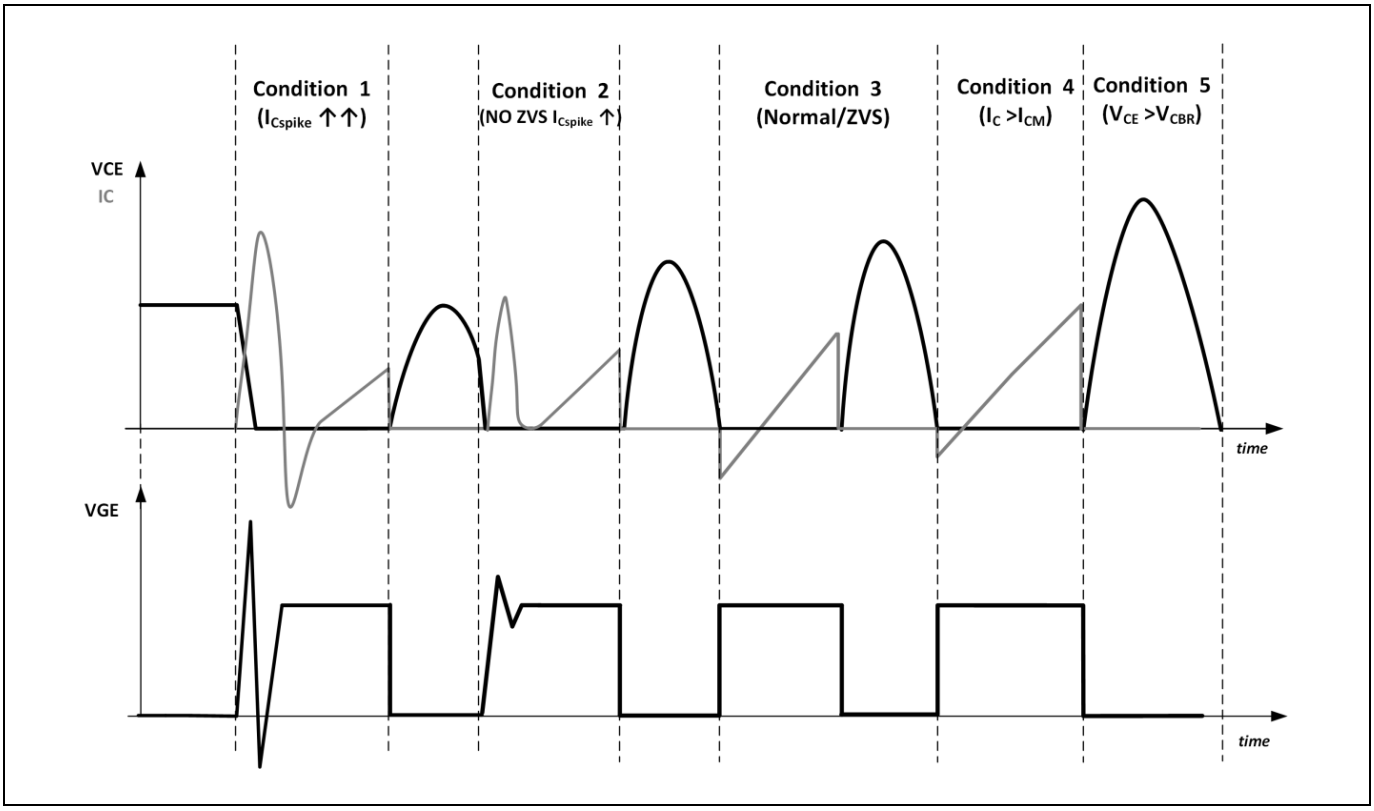


Figure 1.2: Normal and main critical operations of an SEPR topology: collector high-current spike at start-up (Condition 1), non-zero-voltage switching turn-on (Condition 2), normal operation (Condition 3), turn-off current exceeding the maximum IGBT pulse-collector current (Condition 4), collector-emitter voltage exceeding the maximum voltage of the IGBT (Condition 5)

Conditions 1-3 take place during the normal operation of the system, depending on the type of load and on the output power. Condition 4 may also occur during normal operation, if for example, the pan is suddenly removed from the cooking plane. The overcurrent may trigger an overvoltage in the subsequent IGBT turn-off phase (Condition 5) due to the excess energy stored in the resonant inductor. Both conditions 4 and 5 can also take place during surges, or due to grid voltage instability (mains interruptions, voltage dips, etc.). For this reason, a complete SEPR induction cooking system also includes additional circuitry, which should be capable of recognizing abnormal operation, and deactivate the system properly in order not to exceed the IGBT maximum ratings. However, despite the additional protection, severe conditions may still occur where the system does not react in time, leading to IGBT failure.

In order to guarantee adequate protection against the unsafe conditions depicted in Figure 1.2, Infineon has developed the IPD Protect, which represents an integration approach of an IGBT and a gate driver IC targeting an induction cooking application.

1.2 IPD Protect

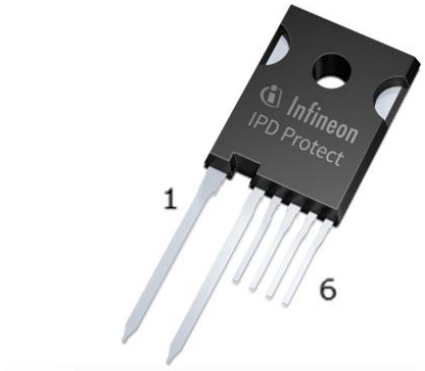
The IPD Protect is a new device developed by Infineon consisting of an integrated solution with co-packed reverse-conducting IGBT and gate driver IC in a TO-247 6-pin package (Figure 1.3a).

The TO-247 6-pin package has the same dimensions and single screw hole as standard TO-247 3- and 4-pin packages. This package allows for easier handling during manufacturing, and takes up less board space. Despite the same dimensions compared to a standard TO-247 3-pin, the 6-pin version features increased creepage distance between the high-voltage collector pin and the five low-voltage pins, as shown in Figure 1.4.

Introduction

The combination of the well-established and appreciated Infineon RC-IGBT technology with a full-featured IC guarantees best performance in the application, together with unique protection against overvoltage, overcurrent and over-temperature conditions:

- TRENCHSTOP™ RC-H5 IGBT: 20A 1350V reverse-conducting IGBT with monolithic body diode designed for soft commutation
- Integrated driver with:
    - Overvoltage protection with programmable overvoltage threshold and active clamp functionality
    - Overcurrent protection with programmable cycle-by-cycle overcurrent threshold
    - Integrated gate drive with 2 level turn-on current
    - Temperature warning and over-temperature protection
    - Feedback of the device status (Normal/Over-temperature/Shutdown)
    - VCC UVLO
    - Integrated ESD protection and latch immunity on all pins
- TO-247 6-pin package



1	C	Collector
2	E/COM	Emitter/Ground
3	VCC	Supply
4	CS	Current Sense
5	INN	PWM Input
6	VDET	Voltage Sense

Figure 1.3: Package and pinout of the IPD Protect

In the following sections, each of the functions of the IPD Protect are explained in detail, showing how they can guarantee higher reliability of the device in the abnormal conditions indicated in Figure 1.2.

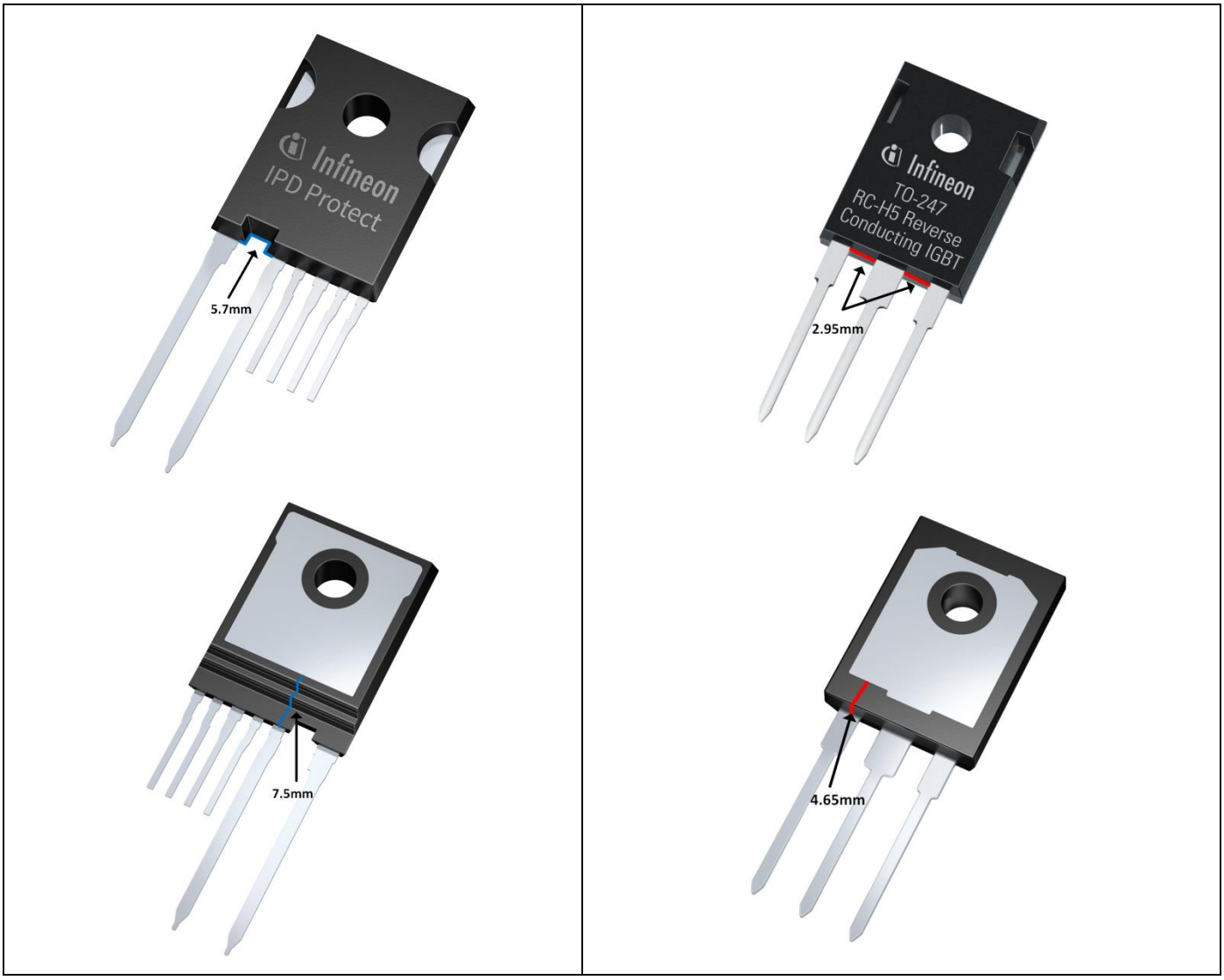


Figure 1.4: Increased creepage of the TO-247 6-pin (left) compared to the standard TO-247 (right)

2 Features of the IPD Protect

2.1 Collector current limitation

The IPD Protect implements a cycle-by-cycle current limitation, as shown in Figure 2.1, which limits the maximum current of the IGBT, independent of the control signal of the microcontroller. By means of proper maximum current settings, operation such as condition 4 depicted in Figure 1.2 can be avoided.

The current limitation is also a major safety feature, as it limits the maximum energy of the resonating load, and hence the maximum voltage across the IGBT during the turn-off phase (Figure 2.1).

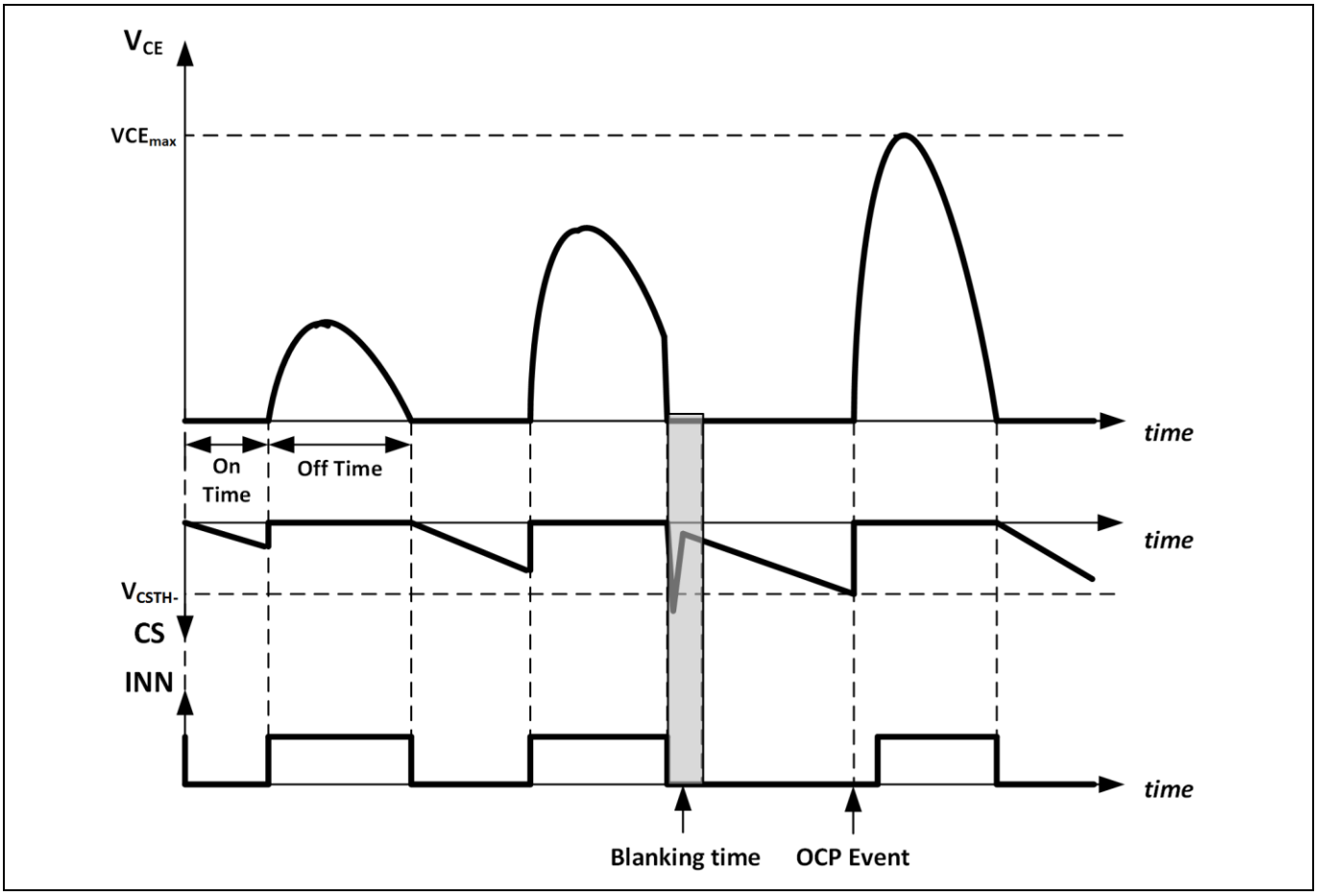


Figure 2.1: Cycle-by-cycle current limitation

Table 1 shows the datasheet parameters which are related to the current limitation function of the IPD Protect. The two main parameters are:

- Overcurrent threshold (V_{CSth-}), which has a typical value of -200 mV and a maximum variation of ±5%.
- Overcurrent detection internal blanking time (t_{CSBLK}): in order to avoid unwanted noise-induced triggering of the current limitation, an internal blanking time of typically 4 µs has been implemented.

The current-sense blanking time is particulary useful at IGBT turn-on. As shown in Figure 2.1, a current spike that triggers off the current sense (CS) limitation, and that occurs after the IGBT turn-on, is ignored if its duration is shorter than t_{CSBLK}. As a consequence, if the IGBT is turned on in hard-switching conditions (i.e. during the phase when the presence of a cooking vessel is detected, or when the system operates at low input power levels), the subsequent high-current spike does not generate a false overcurrent trigger. On the other hand, if the IGBT current exceeds the threshold value after t_{CSBLK}, the IGBT is turned-off immediately.

Table 1: CS limitation datasheet parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Overcurrent threshold voltage	V_{CSTH-}	-5%	-0.2	+5%	V
Overcurrent detection internal blank time	t_{CSBLK}	3.5	---	4.5	µs
Overcurrent detection propagation delay	t_{CS}	---	50	---	ns

In typical SEPR applications, current sensing is commonly used for controlling the power delivered by the inverter. As most of the time the IGBT current is sensed, the same signal can be used as a source for the current limitation. Since V_{CSth-} is negative, a typical arrangement such as in Figure 2.2a should be used. Such a configuration has also the advantage of removing the sense resistor from the gate driving loop. In addition, a resistor of typically 1 kOhm should be placed in series to the CS input to limit currents through the internal ESD-diodes due to transients (R1 in Figure 2.2a).

In case the current-sensing signal for the power control has to be positive (i.e., because it is directly sensed by the microcontroller), a simple bypass capacitor can be used in an arrangment such as the one depicted in Figure 2.2b.

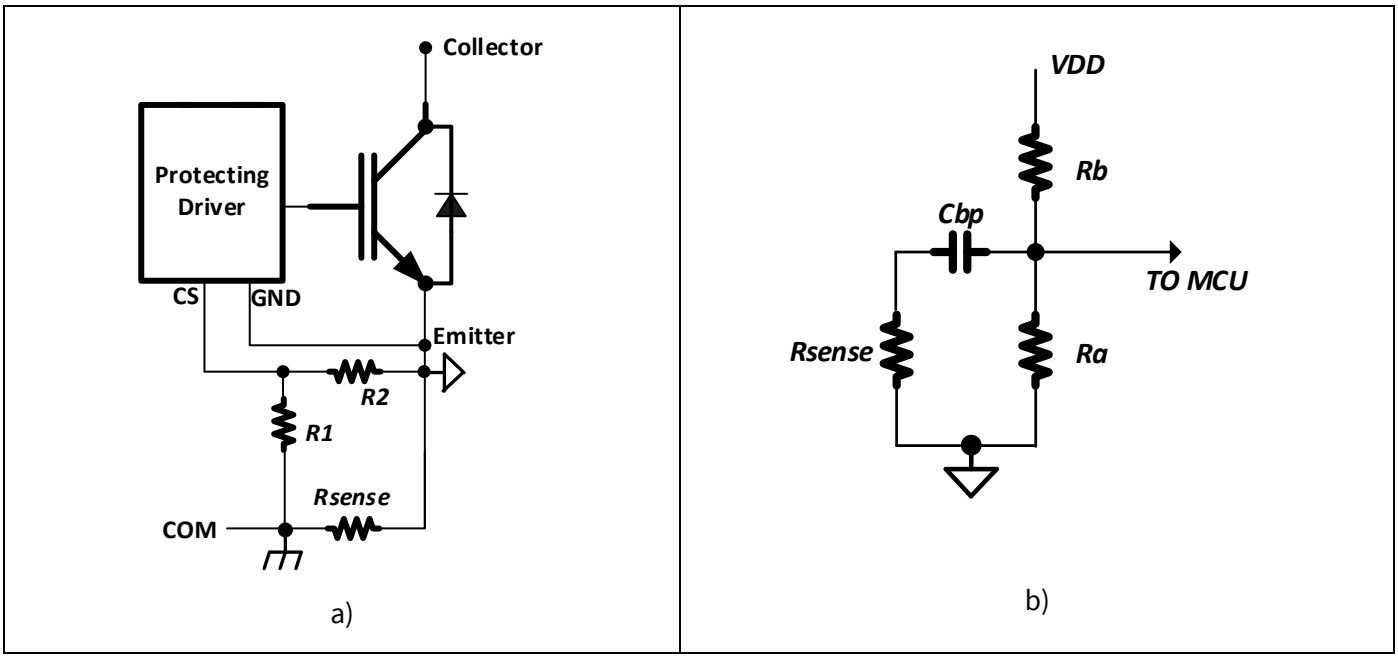


Figure 2.2: a) typical current-sensing configuration; b) simple level-shift circuit for current-sense signal

2.2 Collector voltage active clamp

A second important feature of the IPD Protect is the active clamp control (ACC), which offers a programmable clamping level to keep the voltage across the IGBT below its breakdown voltage. The active clamp functions even in case a surge transient occurs, which is not sufficiently limited by means of the CS limitation protection. The two protection mechanisms operate together in order to guarantee the safe operation of the IGBT under the typical surge conditions which occur in the application.

The active clamp control dynamically turns on the IGBT using a closed loop feedback to keep the voltage across the IGBT constant until the surge energy is dissipated.

More specifically, the active clamp works in two phases, as shown in Figure 2.3.

- When the voltage on the VDET pin crosses the first threshold (V_{DET+1}), the ACC takes over, and the IGBT is turned on for 5 µs (t_{clamp1}) in order to maintain the voltage at the VDET pin to that of V_{DET+1}. The IGBT consequently regulates the collector voltage to the desired clamping voltage. After this, the IGBT is switched off.

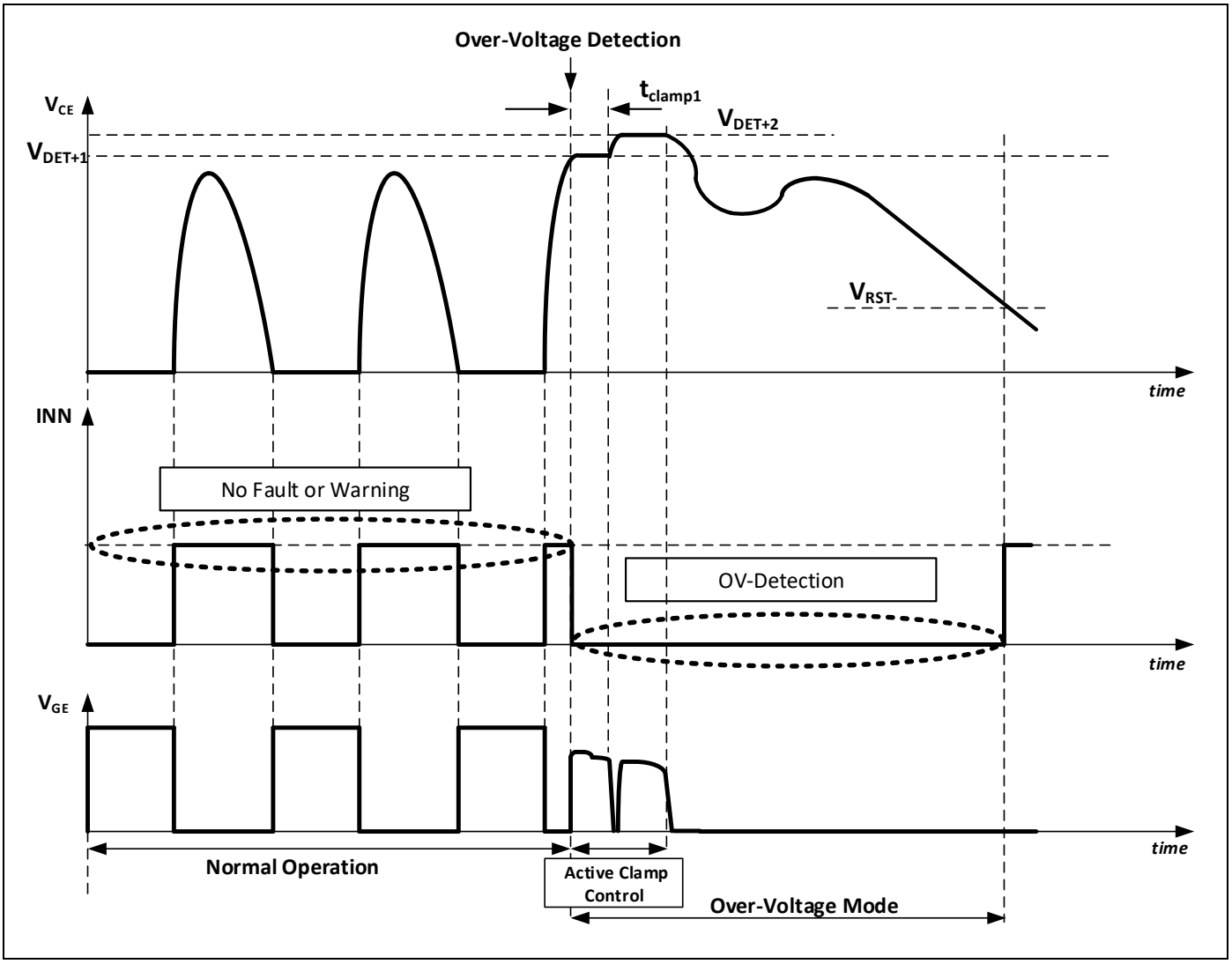


Figure 2.3: Behavior of the ACC control block

- If the energy of the inductor is not dissipated completely during the first 5 µs, VDET voltage starts to rise again after the IGBT is turned off, and eventually will cross the second VDET threshold (V_{DET+2}), which is 11% higher than V_{DET+1}. When this happens, the IGBT is turned on again and stays on in order to regulate VDET and consequently the collector voltage.

During the phase in which the ACC controls the IGBT, the device feeds back to the microcontroller (MCU) the status of overvoltage condition by means of the INN pin, as described in Section 2.4.

The active clamp control remains active until the voltage at VDET drops below V_{DET1+} during the first clamping phase or below V_{DET2+} during the second phase. By means of the aforementioned two-step clamping, the total energy which the IGBT has to dissipate is reduced significantly compared to a continuous clamping phase.

A third internal VDET threshold (V_{RST-}) blocks the IGBT's reactivation until the collector-emitter voltage drops below a programmable restart voltage. An additional blanking time (t_{OVT}) prevents the IGBT from being turned on immediately after the deactivation of the ACC. The minimum waiting time before the reactivation of the IGBT is 3 ms (see t_{OVT} value in Table 2).

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The threshold V_{RST-} is also used in normal operation, in order to prevent the IGBT from being turned on while the collector voltage is above the restart voltage (i.e. due to unwanted noise-induced turn-on from the MCU). Table 2 shows the values of the datasheet parameters which are related to the active clamp control function of the IPD Protect.

Table 2: Datasheet parameters of the active clamp control

Parameter	Symbol	Min.	Typ.	Max.	Unit
Overvoltage rising threshold voltage 1	V_{DET+1}	-3%	3.91	+3%	V
Overvoltage rising threshold voltage 2	V_{DET+2}	-3%	4.36	+3%	V
Restart falling threshold voltage	V_{RST-}	-3%	1.37	+3%	V
Overvoltage clamping time 1	t_{clamp1}	4.25	5.0	5.75	µs
Overvoltage blank timer	t_{OVT}	3	---	---	ms
Overvoltage blanking time @ turn-off IGBT	$t_{VDETBLK}$	---	1200	---	ns

The three threshold voltages of the overvoltage mode can be programmed by means of a resistor divider network between the collector and the VDET pin of the device, as shown in Figure 2.4. Since a similar network is generally used for the collector-emitter voltage zero crossing detection, the additional required components are limited.

The values of the resistors can be calculated starting from any of the three threshold voltages. If, as an example, the first threshold is used, the calculation of R2 is derived from the following formula, after R1 value has been chosen:

$$\mathbf{R_2} = \frac{\mathbf{R_1}}{\frac{\mathbf{V_{clamp1}}}{\mathbf{V_{DET+1}}} - \mathbf{1}}, \quad [1]$$

being V_{clamp1} the chosen value of the first clamping voltage.

After the appropriate resistor divider network has been chosen, the second clamping voltage (V_{clamp2}) and the restart voltage (V_{RST}) can be easily calculated by:

$$\mathbf{V_{clamp2}} = \mathbf{V_{clamp1}} * \frac{\mathbf{V_{DET+2}}}{\mathbf{V_{DET+1}}}, \quad [2]$$

$$V_{RST} = V_{clamp1} * \frac{V_{RST-}}{V_{DET+1}}. \quad [3]$$

R1 can be, in principle, arbitrarily chosen in order to minimize the static current consumption of the system.

In case of severe noise conditions, a simple resistor divider network may not be sufficient to guarantee a stable voltage value on the pin VDET. For this reason, an additional filter capacitance can be added in parallel to R2 (capacitance C1 in Figure 2.4). With this configuration, the value of R1 cannot be chosen arbitrarily but needs to be determined, together with the value of C1, in order to filter adequately the noise on VDET voltage.

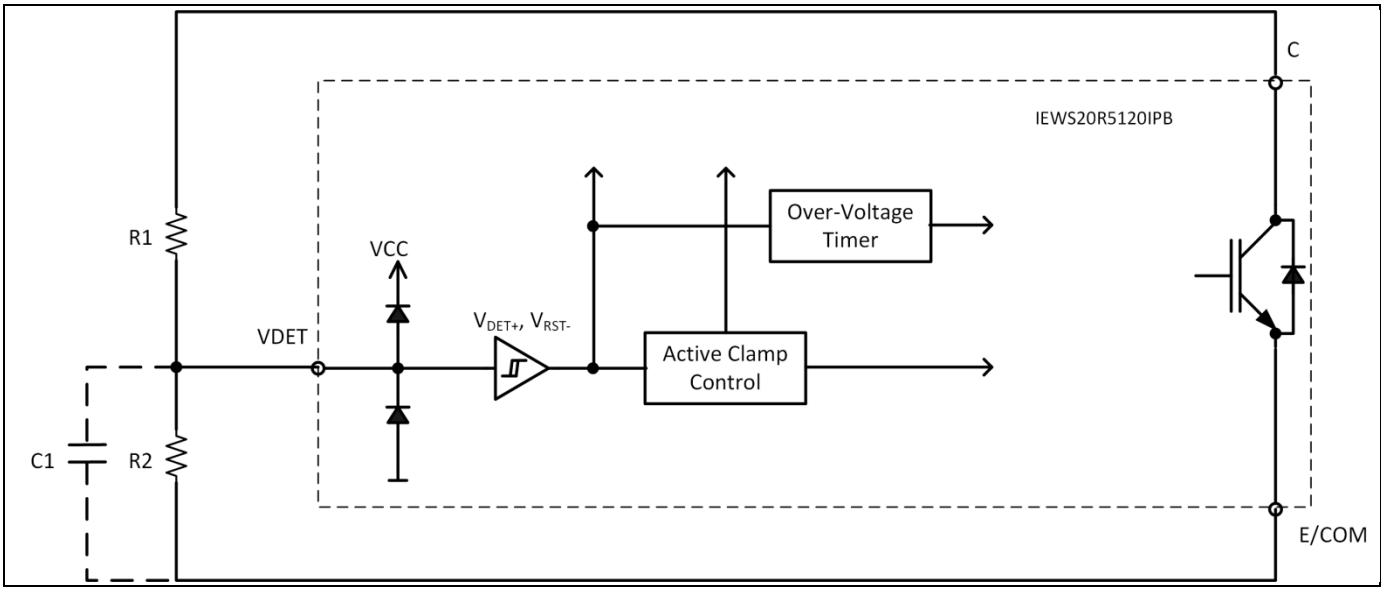

Figure 2.4: Description of the active clamp control block and external voltage divider

2.3 Two-level turn-on

During the operations of an SEPR converter, there are conditions where the IGBT does not turn on with zero voltage (Figure 1.2, conditions 1 and 2). If the VGE is driven fast to the nominal value, the IGBT exhibits a high current spike, which increases the stress on the IGBT itself and on the resonant capacitance. This may reduce the system reliability in the long term. In addition, turn-on current spikes also significantly worsen the EMI behavior of the system. The turn-on current spike is particularly high during the first IGBT turn-on (condition 1), when the device has to charge the resonant capacitance up to the bus voltage. Such a condition is usually repeated several times during the detection phase of a vessel onto the cooktop. Usually, induction cooking manufacturers test the system with a high number of repetitive turn-on pulses, and with the highest admissible bus voltage, in order to check the maximum capability of the components under high current stress. The hard-switching turn-on can also occur at low output power (condition 2), when the system cannot achieve the zero-voltage switching turn-on due to insufficient energy stored in the inductor at the turn-off phase.

Reducing the current spike in hard-switching turn-on is therefore very important in order to improve the system's reliability. To this aim, the IPD Protect is featured with a two-current level gate-drive control. The control strategy is depicted in Figure 2.5, and consists of driving the IGBT gate with two different currents, the first (I_{O1+}) being low enough to limit the charging of the gate capacitance during the initial phase of the turn-on. The second current level (I_{O2+}), being larger, guarantees that the gate voltage reaches the desired steady state value in order not to increase the conduction losses of the IGBT.

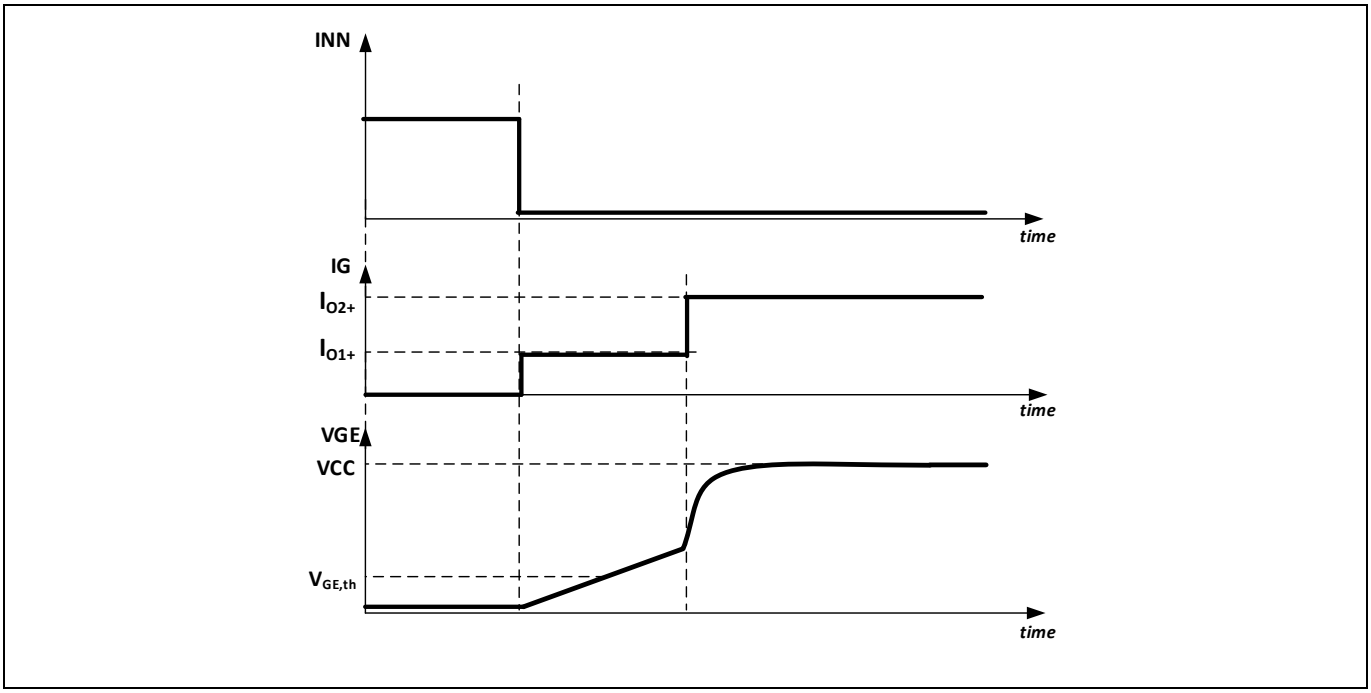

Figure 2.5: Behavior of the two-level turn-on control

2.4 PWM input / Diagnostic output (INN) functionalities

The INN pin of the IPD Protect is used for controlling the IGBT and to provide feedback on the status of the device during the operation. It acts as an input to control the ON-time of the IGBT in an inverted logic mode. During the turn-off time of the IGBT, the INN pin is controlled by a diagnostic block in order to pull up the voltage level according to the status of the device (see Table 3). The input block of the IPD Protect is shown in Figure 2.6.

In order to avoid unwanted current flow in/from the INN pin, the MCU pin that drives the device has to be put in high impedance mode when the IGBT has to be switched off. This can be implemented by using the open-drain configuration of the MCU pin (as shown in Figure 2.6).

Table 3: INN feedback voltages for over-temperature warning/shutdown

Status	INN Pull-up level			Corresponding datasheet parameter
	Min	Typ	Max	
No Fault	2.10 V	2.50 V	2.90 V	V_{IPUnf}
OT Warning	4.00 V	4.50 V	5.00 V	V_{IPUtw}
OV Detection	---	---	0.5 V	V_{IPUov}
OT Warning + OV Detection	---	---	0.5 V (OV dominates)	
OT Shut-Down	---	---	0.5 V	
UVLO	---	---	0.5 V	

The Schmitt trigger input of the INN is to guarantee compatibility down to 3.3 V controller. The Schmitt trigger input and noise filter provide beneficial noise rejection to short input pulses according to Figure 2.7.

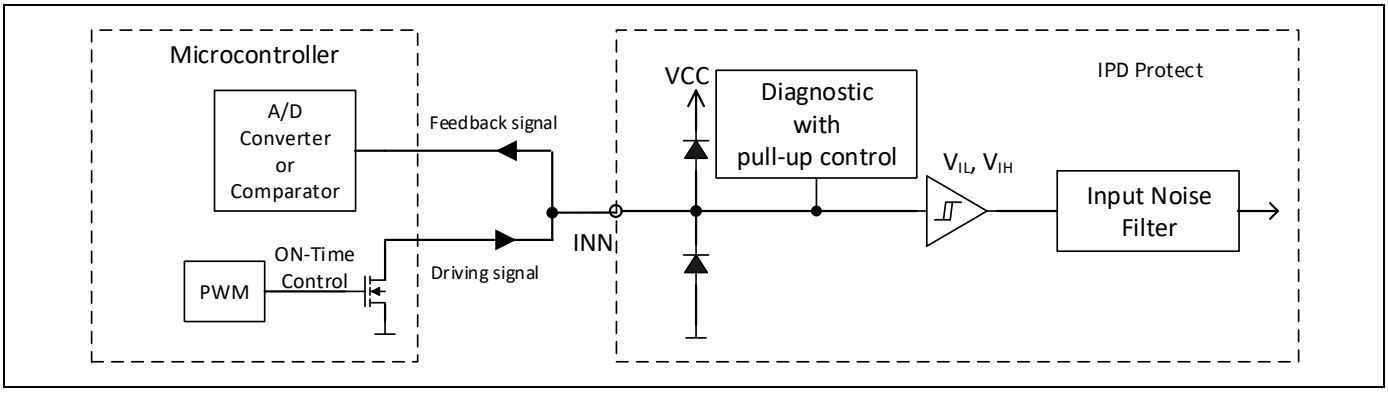

Figure 2.6: Block diagram of the INN internal structure

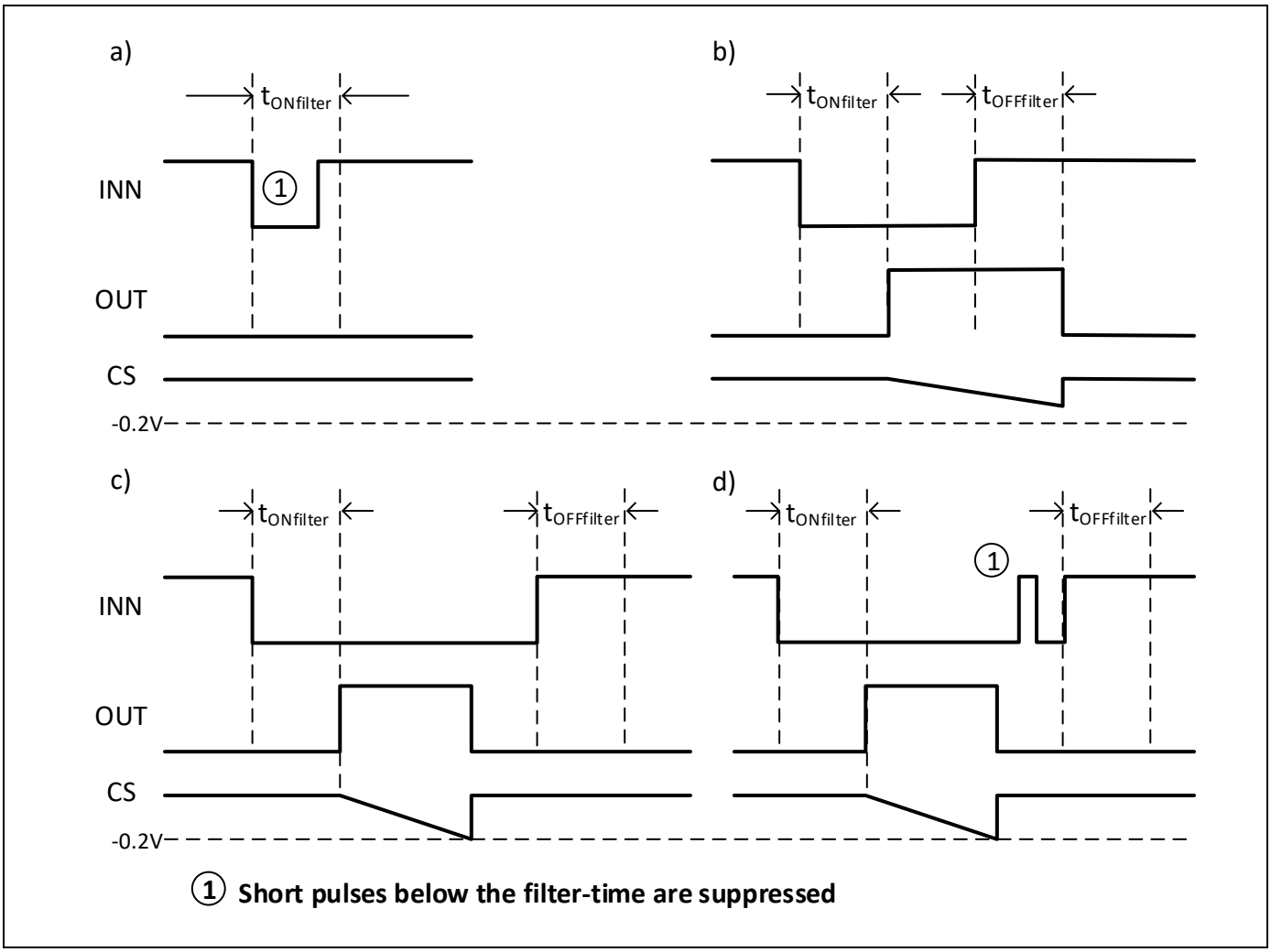

Figure 2.7: Behavior of the input filter times of the IPD Protect

2.5 Over-temperature protection

The IPD Protect also features an internal over-temperature protection implemented into the driver IC. The protection is based on two thresholds, which together determine three different operating states of the device depending on the temperature.

The behavior of the over-temperature protection is depicted in Figure 2.8 and explained in the following:

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- If the temperature of the device stays below the first threshold (T_{vjTW}), the device operates in the normal state. During this state, the INN feedback voltage is typically 2.5 V (as indicated by the V_{IPUnf} paramter).
- When the temperature passes the first threshold, the device generates a warning feedback by means of the INN pin to the system MCU so that it can react and, as an example, increase the speed of the system fan. The value of the INN feedback voltage in over-temperature condition is provided in the datasheet as the parameter V_{IPUtw}.
- If the temperature increases even further (i.e., due to fan malfunction) and exceeds the second threshold (T_{vjSD}), the IGBT is shut down immediately, and the device ignores all the controls coming from the MCU. This condition is held until the temperature falls below the temperature reset threshold (T_{vjRST}).

The values of the three thresholds that regulate the behavior of the over-temperature protection are shown in Table 4.

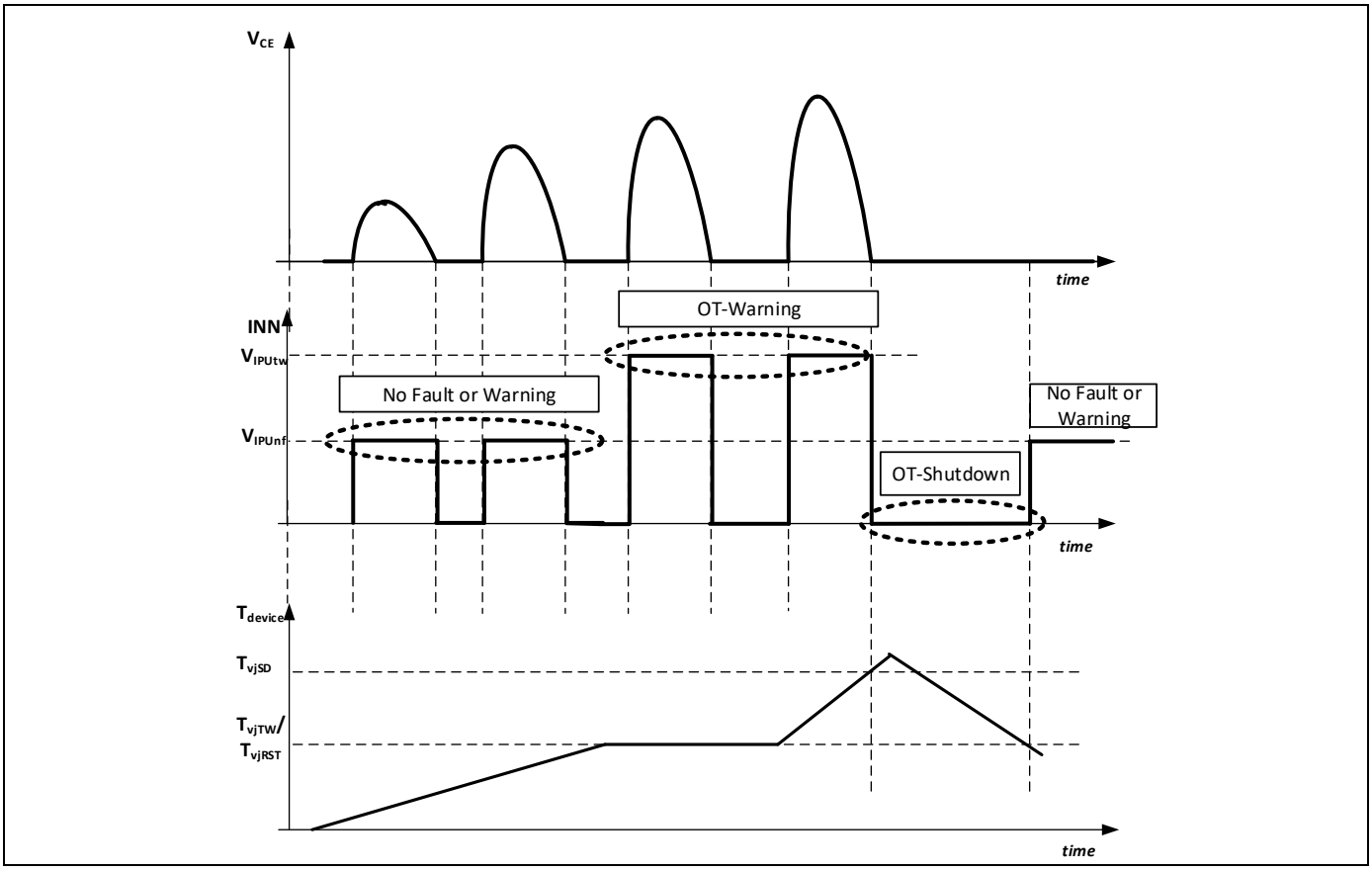

Figure 2.8: Behavior of the over-temperature protection and relative INN feedback

Table 4: Over-temperature warning / shutdown datasheet parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction temperature warning	T_{vjTW}	---	75	---	°C
Junction temperature thermal shutdown	T_{vjSD}	---	150	---	°C
Junction temperature thermal reset	T_{vjRST}	---	75	---	°C

3 Typical application

The IPD Protect features unique protection features which improve significantly the reliability of the device in the application. Nevertheless, care has to be taken in the system design to guarantee a proper and reproducible function in all the application conditions. The most important aspect that has to be considered is that the co-packed IC shares the same GND connection of the IGBT. This means that this node is in the main IGBT current path, and can be therefore exposed to significant fluctuations due to the parasitic inductances of the package (bond wires, leads, etc.). In order to effectively shield the IC, additional bypass capacitances should be used, especially close to the most sensitive pins. A typical application schematic of the IPD Protect is shown in Figure 3.1.

3.1 Power supply

The power supply of the IC has to be kept as stable as possible. In order to do so, a bypass capacitor (C3 in Figure 3.1) should be placed as close as possible to the device pins (a minimum value of 1 µF is recommended).

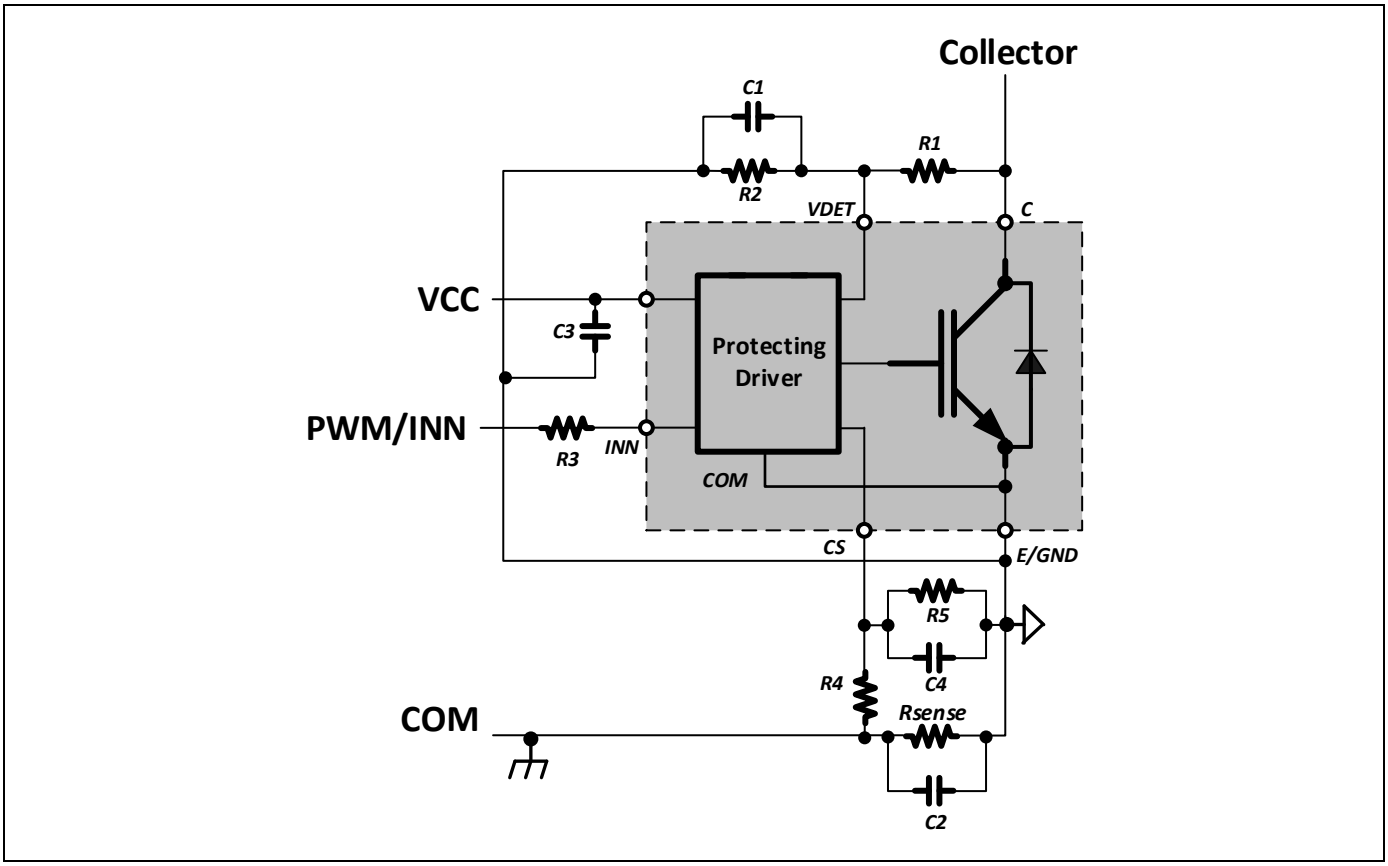

Figure 3.1: Typical application of the IPD Protect

3.2 Current-sensing stage (CS pin)

The current sense is the most sensitive block in all the IPD Protect, since it relies on a voltage level which falls in the range of millivolts. As a consequence, the signal which goes into the CS pin has to be as clean as possible. In this regard, a first measure to adopt consists in placing a filter capacitor in parallel to the current-sense resistor (capacitor C2 in Figure 3.1). This capacitor aims to filter the spikes produced by the parasitic inductance of the sense resistor. In order to strongly reduce the generation of such spikes, a sense resistor with low parasitic inductance is recommended.

In addition, a second bypass capacitance should be placed between the CS and GND pins (capacitor C4). This capacitor has the main purpose of reducing the spikes produced by the parastic inductance in the ground path. In order to reduce this inductance, the emitter lead of the IPD Protect has to be cut as close as possible to the body of the device. Alternatively, the bypass capacitor C4 has to be placed also very close to the package body. Whilst C4 filters the ground bounces on the CS pin, it also acts as a low-pass filter together with the resistors R4 and R5. Therefore, the values of C4, R4 and R5 have to be properly selected in order to guarantee a proper replica of the IGBT so that the proper functionality of the overcurrent limitation is not affected.

The R4 resistor should have a minimum value of 1 kOhm in order to limit currents through the internal ESD diodes due to transients.

3.3 Collector-voltage monitoring stage (VDET pin)

As described in Section 2.2, the IPD Protect implements an active clamp control block, which prevents the collector-to-emitter voltage from rising above the maximum withstand voltage of the IGBT. As for current sensing, the ACC block uses a scaled replica of the collector-to-emitter voltage, which has to be externally provided at the VDET pin. Since a stable voltage is also important for this block, it is recommended that a bypass capacitor is placed between the VDET and GND pins (C1 in Figure 3.1). The same considerations about the design of the low-pass filter in Section 3.2 are also valid here.

3.4 INN input stage

A resistor of 100 Ohm should be placed in series to the INN input to limit currents through the internal ESD diodes due to transients.

4 Layout

4.1 Layout guidelines

Due to the high sensitivity of the co-pack IC, it is recommended that the bypass capacitances are located as close as possible to the device body. In addition the leads should be shortened as much as possible to reduce the additional stray inductances.

A layout example is shown in Figure 4.1. The layout refers to the schematic shown in Figure 3.1. All the components except for the sense resistor are SMD 1206. R2 and C1 are SMD 0805.

Resistor R1 in Figure 3.1 has been implemented by means of five resistors in series (R1_1…R1_5) due to the limited voltage rating of the 1206 SMD resistors.

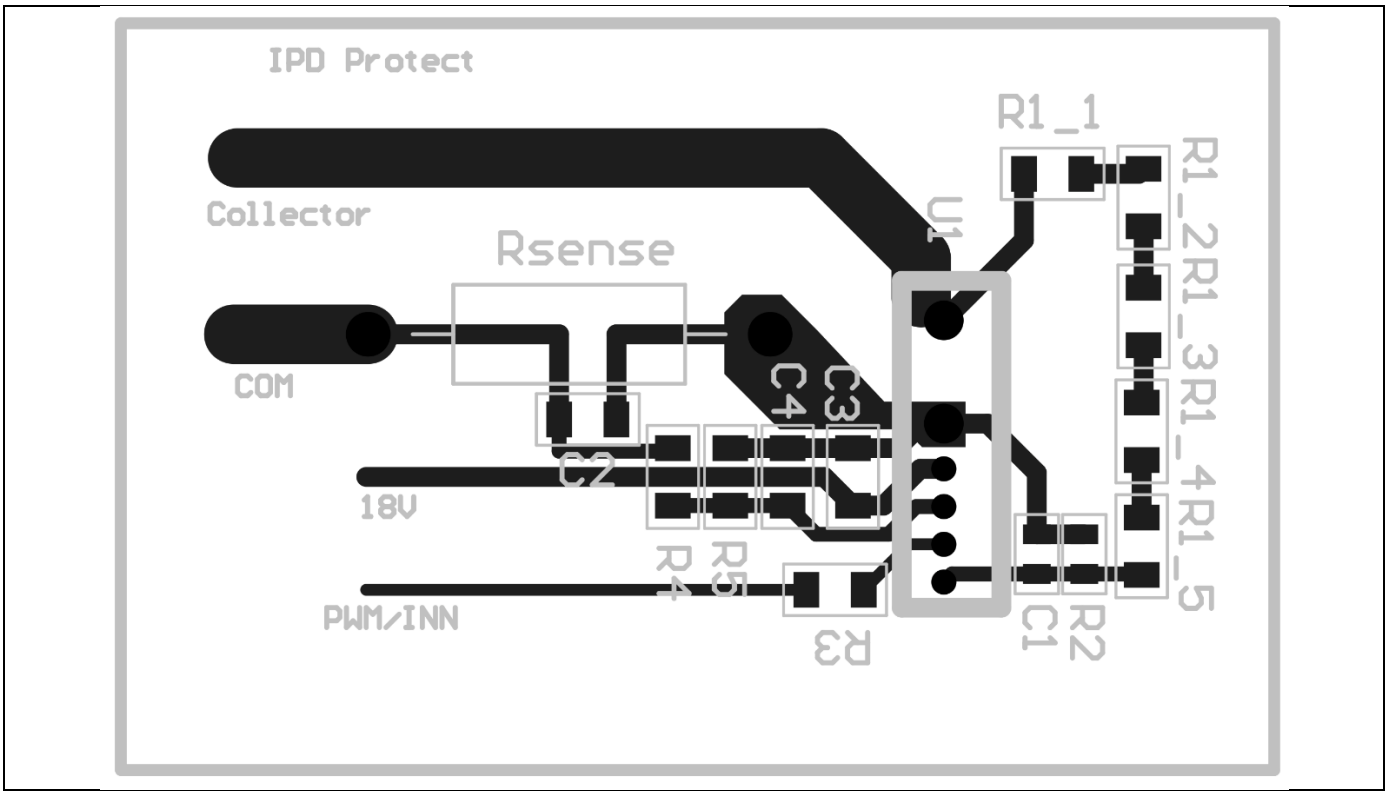

Figure 4.1: Recommended layout for the IPD Protect

5 Additional information

The reader can find all the available information about the IPD Protect at the following link: http://www.infineon.com/IPD-Protect.

6 Reference

[1] E.J. Davies, Induction Heating Handbook, McGraw-Hill, 1979

[2] O. Hellmund, et al.: 1200V Reverse Conducting IGBTs for Soft-Switching Applications; Conference on Power Electronics and Intelligent Motion (PCIM China); Shanghai, China, 2004

Reference

Revision history

Document version	Date of release	Description of changes
	21.09.2018	First version
1.1	30.10.2018	Errata corrige: page 9, Equation 1
1.2	12.11.2018	Page 20: disclaimer changed to exclude AEC qualification
1.3	21.01.2020	Product name changed to IPD. Updates of Figure 1.4 and Figure 4.1.

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