TRAVEO™ T2G 32-bit Automotive MCU

Based on Arm® Cortex®-M4F single

General description

CYT2CL is a family of TRAVEO™ T2G microcontrollers targeted at automotive systems such as cluster entry units. CYT2CL has an Arm® Cortex®-M4F CPU for primary processing, and an Arm® Cortex®-M0+ CPU for peripheral and security processing. These devices contain embedded peripherals supporting controller area network with flexible data rate (CAN FD), local interconnect network (LIN), clock extension peripheral interface (CXPI), LCD controller. TRAVEO™ T2G devices are manufactured on an advanced 40-nm process. CYT2CL incorporates Infineon's low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

Features

- **Dual CPU subsystem**
  - 160-MHz (max) 32-bit Arm® Cortex®-M4F CPU with
    - Single-cycle multiply
    - Single-precision floating point unit (FPU)
    - Memory protection unit (MPU)
  - 100-MHz (max) 32-bit Arm® Cortex®-M0+ CPU with
    - Single-cycle multiply
    - Memory protection unit
  - Inter-processor communication in hardware
  - Three DMA controllers
    - Peripheral DMA controller #0 (P-DMA0) with 76 channels
    - Peripheral DMA controller #1 (P-DMA1) with 84 channels
    - Memory DMA controller #0 (M-DMA0) with 4 channels
- **Integrated memories**
  - Up to 4160 KB of code-flash with an additional 128 KB of work-flash
    - Read-While-Write (RWW) allows updating the code-flash/work-flash while executing code from it
    - Single- and dual-bank modes (specifically for Firmware update Over The Air [FOTA])
    - Flash programming through SWD/JTAG interface
  - Up to 512 KB of SRAM with selectable retention granularity
- **Crypto engine**[1]
  - Supports Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM)
  - Secure boot and authentication
    - Using digital signature verification
    - Using fast secure boot
  - AES: 128-bit blocks, 128-/192-/256-bit keys
  - 3DES: 64-bit blocks, 64-bit key
  - Vector unit supporting asymmetric key cryptography such as Rivest-Shamir-Adleman (RSA) and Elliptic Curve (ECC)
  - SHA-1/2/3: SHA-512, SHA-256, SHA-160 with variable length input data
  - CRC: supports CCITT CRC16 and IEEE-802.3 CRC32
  - True random number generator (TRNG) and pseudo random number generator (PRNG)
  - Galois/Counter Mode (GCM)

Note
1. Crypto engine features are available on select MPNs.

Features

- **Functional safety for ASIL-B**
  - Memory protection unit (MPU)
  - Shared memory protection unit (SMPU)
  - Peripheral protection unit (PPU)
  - Watchdog timer (WDT)
  - Multi-counter watchdog timer (MCWDT)
  - Low-voltage detector (LVD)
  - Brown-out detector (BOD)
  - Overvoltage detection (OVD)
  - Clock supervisor (CSV)
    - Supported in all power modes
  - Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash)
- **Low-power 2.7-V to 5.5-V operation**
  - Low-power Active, Sleep, Low-power Sleep, DeepSleep, and Hibernate modes for fine-grained power management
  - Configurable options for robust BOD
    - Two threshold levels (2.7 V and 3.0 V) for BOD on V_{DDD} and V_{DDA_ADC}
    - One threshold level (1.1 V) for BOD on V_{CCD}
- **Wakeup support**
  - Up to four pins to wakeup from Hibernate mode
  - Wakeup recognition bit for each wakeup source
  - Up to 128 GPIO pins to wakeup from Sleep modes
  - Event Generator, SCB, Watchdog Timer, RTC alarms to wake from DeepSleep modes
- **Clock sources**
  - Internal main oscillator (IMO)
  - Internal low-speed oscillator (ILO)
  - External crystal oscillator (ECO)
  - Watch crystal oscillator (WCO)
  - Phase-locked loop (PLL)
  - Frequency-locked loop (FLL)
  - Low-power external crystal oscillator (LPECO)
- **LCD controller**
  - Up to four LCD controllers, with 32 segments (SEG) and four commons (COM)
  - Supports both Type A (standard) and Type B (low-power) drive waveforms
  - Three drive modes
    - PWM drive at 1/2 bias
    - PWM drive at 1/3 bias
    - Digital correlation
  - Operates in ACTIVE, SLEEP, and DeepSleep power modes
  - Digital contrast control
- **Sound subsystem**
  - Two time-division multiplexing (TDM) interfaces
  - Two pulse-code modulation-pulse width modulation (PCM-PWM) interfaces
  - Up to five sound generator (SG) interfaces
  - One PCM Audio stream mixer with five input streams

Features

- **Communication interfaces**
  - Up to four CAN FD channels
    - Increased data rate (up to 8 Mbps) compared to classic CAN, limited by physical layer topology and transceivers
    - Compliant to ISO 11898-1:2015
    - Supports all the requirements of Bosch CAN FD Specification V1.0 for non-ISO CAN FD
    - ISO 16845:2015 certificate available
  - Up to 12 runtime-reconfigurable SCB (serial communication block) channels, each configurable as I^2C, SPI, or UART
  - Up to two independent LIN channels
    - LIN protocol compliant with ISO 17987
  - Up to two CXPI channels with data rate up to 20 kbps
- **Serial memory interface (SMIF)**
  - One SPI (single, dual, quad, or octal), xSPI interface
  - On-the-fly encryption and decryption
  - Execute-In-Place (XIP) from external memory
- **Timers**
  - Up to 46 16-bit and 16 32-bit timer/counter pulse-width modulator (TCPWM) blocks for regular operations
    - Up to 12 16-bit counters optimized for motor-control operations (Equivalent to 6 stepper motor-control [SMC] channels with ZPD and slew rate control capability)
    - Supports timer, capture, quadrature decoding, pulse-width modulation (PWM), PWM with dead time (PWM_DT), pseudo-random PWM (PWM_PR), and shift-register (SR) modes
  - Up to 16 Event Generation (EVTGEN) timers supporting cyclic wakeup from DeepSleep
    - Events trigger a specific device operation (such as execution of an interrupt handler, a SAR ADC conversion, and so on)
- **Real time clock (RTC)**
  - Year/Month/Date, Day-of-week, Hour:Minute:Second fields
  - Supports both 12- and 24-hour formats
  - Automatic leap-year correction
- **I/O**
  - Up to 140 Programmable I/Os
  - Two I/O types
    - GPIO Standard (GPIO_STD)
    - GPIO Enhanced (GPIO_ENH)
    - GPIO Stepper Motor Control (GPIO_SMC)
    - High-Speed I/O Standard with Low Noise (HSIO_STDLN)
- **Regulators**
  - Generates 1.1-V nominal core supply from a 2.7-V to 5.5-V input supply
  - Two types of regulators
    - DeepSleep
    - Core internal
- **Programmable analog**
  - One SAR A/D converter
    - Each ADC supports 32 logical channels, with 48 external channels. Any external channel can be connected to any logical channel in the SAR.
    - 12-bit resolution and sampling rates up to 1 Msps
  - The ADC also supports six internal analog inputs like:
    - Bandgap reference to establish absolute voltage levels
    - Calibrated diode for junction temperature calculations
    - Two AMUXBUS inputs and two direct connections to monitor supply levels
  - ADC supports addressing of external multiplexers
  - ADC has a sequencer supporting autonomous scanning of configured channels

Features

- **Smart I/O**
  - One smart I/O block, which can perform Boolean operations on signals going to and from I/Os
  - Up to eight I/Os (GPIO_STD) supported
- **Debug interface**
  - JTAG controller and interface compliant to IEEE-1149.1-2001
  - Arm® SWD (serial wire debug) port
  - Supports Arm® Embedded Trace Macrocell (ETM) Trace
    - Data trace using SWD
    - Instruction and data trace using JTAG
- **Compatible with industry-standard tools**
  - GHS/MULTI or IAR EWARM for code development and debugging
- **Packages**
  - 144-LQFP, 16 × 16 × 1.7 mm (max), 0.4-mm lead pitch
  - 144-LQFP, 20 × 20 × 1.7 mm (max), 0.5-mm lead pitch
  - 176-LQFP, 24 × 24 × 1.7 mm (max), 0.5-mm lead pitch

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1 Features list

Table 1-1 CYT2CL feature list for all packages

Features	Package	
	144-LQFP	176-LQFP
CPU		
Core	32-bit Arm® Cortex®-M4F CPU and 32-bit Arm® Cortex®-M0+ CPU	
Functional safety	ASIL-B	
Operation voltage for GPIO_STD	2.7 V to 5.5 V	
Operation voltage for GPIO_ENH	2.7 V to 5.5 V	
Operation voltage for GPIO_SMC	2.7 V to 5.5 V	
Operation voltage for HSIO_STDLN	3.0 V to 3.6 V	
Core voltage	1.05 V to 1.15 V	
Operating frequency	Arm® Cortex®-M4F 160 MHz (max) and Arm® Cortex®-M0+ 100 MHz (max), related by integer frequency ratio (that is, 1:1, 1:2, 1:3, and so on)	
MPU, PPU	Supported	
FPU	Single precision (32-bit)	
DSP-MUL/DIV/MAC	Supported by Arm® Cortex®-M4F CPU	
Memory		
Code-flash	4160 KB (4032 KB/Large Sectors + 128 KB/Small Sectors)	
Work-flash	128 KB (96 KB/Large Sectors + 32 KB/Small Sectors)	
SRAM (configurable for retention)	512 KB (SRAM0/256 KB + SRAM1/256 KB)	
ROM	32 KB	
Communication interfaces		
CAN0 (CAN-FD: Up to 8 Mbps)	2 ch	
CAN1 (CAN-FD: Up to 8 Mbps)	2 ch	
CAN RAM	16 KB per instance (2 ch), 32 KB in total	
Serial communication block (SCB)	12 ch	
LIN/UART master support	2 ch	
CXPI controller	2 ch	
Memory interfaces		
SMIF (Single SPI / Dual SPI / Quad SPI /Octal SPI / xSPI)	1 ch (HSIO_STDLN at 100 MHz)	
Timers		
RTC	1 ch	
TCPWM (16-bit)	34 ch	
TCPWM (16-bit) SMC	12 ch	
TCPWM (32-bit)	16 ch	
External interrupts	108	140
Analog		
12-bit, 1 Msps SAR ADC	1 Unit (SAR0, 32 logical channels)	
	48 external channels	
	6 ch for Internal sampling	

Table 1-1 CYT2CL feature list for all packages *(continued)*

Features	Package	
	144-LQFP	176-LQFP
Security		
Flash security (program/work read protection)	Supported	
Flash chip erase enable	Configurable	
eSHE/HSM	By separate firmware[2]	
Sound		
Mixer	1 ch (5 mixer sources)	
PCM-PWM	2 ch	
TDM	2 TDM structures (TDM0/1 with up to 16 ch)	
Sound generator (SG)	5 ch	
LCD controller		
Common	4	
Segments	Up to 32 segments	
Type	Type A and Type B	
System		
DMA controller	P-DMA0 with 76 channels (32 general purpose), P-DMA1 with 84 channels (16 general purpose), and M-DMA0 with 4 channels	
Internal main oscillator	8 MHz	
Internal low-speed oscillator	32.768 kHz (nominal)	
PLL	Input frequency: 3.988 to 33.34 MHz, PLL output frequency: up to 160 MHz	
FLL	Input frequency: 0.25 to 80 MHz, FLL output frequency: up to 100 MHz	
Watchdog timer and multi-counter Watchdog timer	Supported (WDT + 2× MCWDT) MCWDT#0 tied to CM0+, MCWDT#1 to CM4	
Clock supervisor	Supported	
Cyclic wakeup	Supported	
GPIO standard (GPIO_STD)	66	96
GPIO enhanced (GPIO_ENH)	6	8
GPIO SMC (GPIO_SMC)	24	
HSIO standard low noise (HSIO_ST-DLN)	12	
Smart I/O (Blocks)	1 block, mapped through 8 I/Os	
Low-voltage detect	Two, 26 selectable levels	
Maximum ambient temperature	105°C for S-grade	
Debug interface	SWD/JTAG	
Debug trace	Arm® Cortex®-M4F ETB size of 8 KB, Arm® Cortex®-M0+ MTB size of 4 KB	

Note
2. Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM) support are enabled by third-party firmware.

1.1 Peripheral instance list

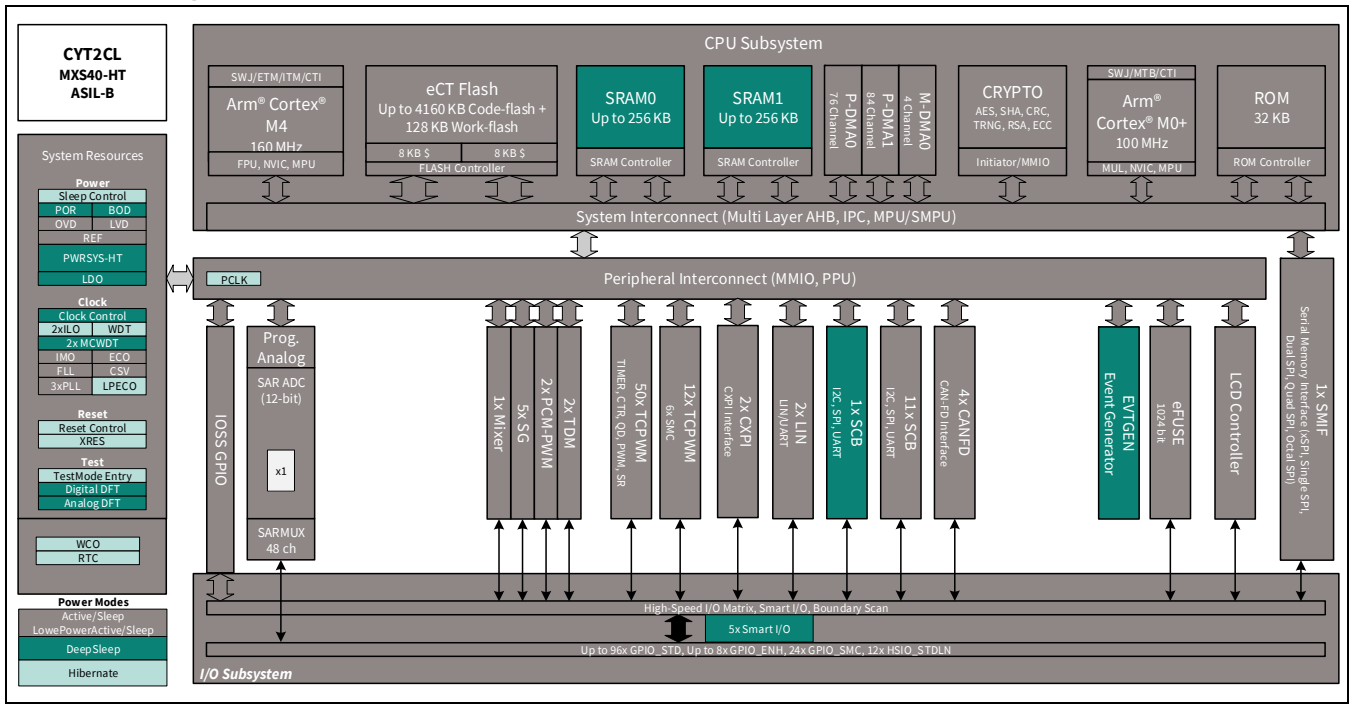
The following table lists the instances supported under each package for communication peripherals, based on the minimum pins needed for the functionality.

Table 1-2 Peripheral instance list

Module	144-LQFP	176-LQFP	Minimum pin function set
CXPI	0/1	0/1	TX, RX
CAN0	0/1	0/1	TX, RX
CAN1	0/1	0/1	TX, RX
LIN0	0/1	0/1	TX, RX
SCB/UART	0 to 11	0 to 11	TX, RX
SCB/I2C	0 to 11	0 to 11	SCL, SDA
SCB/SPI	0 to 11	0 to 11	MISO, MOSI, CLK, SELECT0
TDM/RX	0/1	0/1	MCK, FSYNC, SCK, SD
TDM/TX	0/1	0/1	MCK, FSYNC, SCK, SD
SG	0 to 4	0 to 4	TONE, AMPL
PWM	0/1	0/1	LINE1/2_P/N

2 Blocks and functionality

Block diagram



The **Block diagram** gives a simplified view of the interconnection between subsystems and blocks. CYT2CL has four major subsystems: CPU, system resources, peripherals, and I/O[3,4]. The color-coding shows the lowest power mode where the particular block is still functional.

CYT2CL provides extensive support for programming, testing, debugging, and tracing of both hardware and firmware.

Debug-on-chip functionality enables in-system debugging using the production device. It does not require special interfaces, debugging pods, simulators, or emulators.

The JTAG interface is fully compatible with industry-standard third-party probes such as I-jet, J-Link, and GHS.

The debug circuits are enabled by default.

CYT2CL provides a high level of security with robust flash protection and the ability to disable features such as debug.

Additionally, each device interface can be permanently disabled for applications concerned with phishing attacks from a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled.

Notes
3. GPIO_STD supporting 2.7 V to 5.5 V V_{DDIO} range.
4. GPIO_ENH supporting 2.7 V to 5.5 V V_{DDIO} range with higher currents at lower voltages.
5. GPIO_SMC supporting 2.7 V to 5.5 V V_{DDIO} range with currents higher than GPIO_ENH.
6. HSIO_STDLN supporting 3.0 V to 3.6 V V_{DDIO} range with high-speed signaling and programmable drive strength.

3 Functional description

3.1 CPU subsystem

3.1.1 CPU

The CYT2CL CPU subsystem contains a 32-bit Arm® Cortex®-M0+ CPU with MPU, and a 32-bit Arm® Cortex®-M4F CPU with MPU, and single-precision FPU. This subsystem also includes P-/M-DMA controllers, a cryptographic accelerator, code-flash of up to 4160 KB, 128 KB of work-flash, SRAM of up to 512 KB, and 32 KB of ROM.

The Cortex®-M0+ CPU provides a secure, un-interruptible boot function. This guarantees that, following completion of the boot function, system integrity is valid and privileges are enforced. Shared resources (flash, SRAM, peripherals, and so on) can be accessed through bus arbitration, and exclusive accesses are supported by an inter-processor communication (IPC) mechanism using hardware semaphores.

3.1.2 DMA controllers

CYT2CL has three DMA controllers: P-DMA0 with 32 general-purpose and 44 dedicated channels, P-DMA1 with 16 general-purpose and 68 dedicated channels, and M-DMA0 with four channels. P-DMA is used for peripheral-to-memory and memory-to-peripheral data transfers and provides low latency for a large number of channels. Each P-DMA controller uses a single data-transfer engine that is shared by the associated channels. General purpose channels have a rich interconnect matrix including P-DMA cross triggering which enables demanding data-transfer scenarios. Dedicated channels have a single triggering input (such as an ADC channel) to handle common transfer needs. M-DMA is used for memory-to-memory data transfers and provides high memory bandwidth for a small number of channels. M-DMA uses a dedicated data-transfer engine for each channel. They support independent accesses to peripherals using the AHB multi-layer bus.

3.1.3 Flash

CYT2CL has up to 4160 KB (4032 KB with a 32-KB sector size, and 128 KB with an 8-KB sector size) of code-flash with an additional work-flash of up to 128 KB (96 KB with 2-KB sector size, and 32 KB with 128-B sectors size). Work-flash is optimized for reprogramming many more times than code-flash. Code-flash supports Read-While-Write (RWW) operation allowing flash to be updated while the CPU is active. Both the code-flash and work-flash areas support dual-bank operation for over-the-air (OTA) programming.

3.1.4 SRAM

CYT2CL has up to 512 KB of SRAM (512 KB) with two independent controllers. The first controller SRAM0 provides DeepSleep retention in 32-KB increments while SRAM1 is selectable between fully retained and not retained.

3.1.5 ROM

CYT2CL has 32-KB ROM that contains boot and configuration routines. This ROM enables secure boot and authentication of user flash to guarantee a secure system.

3.1.6 Cryptography accelerator for security

The cryptography accelerator implements (3)DES block cipher, AES block cipher, SHA hash, cyclic redundancy check, pseudo random number generation, true random number generation, galois/counter mode, and a vector unit to support asymmetric key cryptography such as RSA and ECC.

Depending on the part number, this block is either completely or partially available or not available at all. See **Ordering information** for more details.

3.2 System resources

3.2.1 Power system

The power system ensures that the supply voltage levels meet the requirements of each power mode, and provides a full-system reset when these levels are not valid. Internal power-on reset (POR) guarantees full-chip reset during the initial power ramp.

Three Brown-Out Detection (BOD) circuits monitor the external supply voltages (V_{DDD}, V_{DDA_ADC}, V_{CCD}). The BOD on V_{DDD} and V_{CCD} are initially enabled and cannot be disabled. The BOD on V_{DDA_ADC} is initially disabled and can be enabled by the user. For the external supplies V_{DDD} and V_{DDA_ADC}, BOD circuits are software configurable with two settings; a 2.7-V minimum voltage that is robust for all internal signaling, and a 3.0-V minimum voltage, which is also robust for all I/O specifications (which are guaranteed at 2.7 V). The BOD on V_{CCD} is provided as a safety measure and is not a robust detector.

Three overvoltage detection (OVD) circuits are provided for monitoring external supplies (V_{DDD}, V_{DDA_ADC}, V_{CCD}), and overcurrent detection circuits (OCD) for monitoring internal and external regulators. OVD thresholds on V_{DDD} and V_{DDA_ADC} are configurable with two settings; a 5.0-V and 5.5-V maximum voltage.

Two voltage detection circuits are provided to monitor the external supply voltage (V_{DDD}) for falling and rising levels, each configurable for one of the 26 selectable levels.

All BOD, OVD, and OCD circuits on V_{DDD} and V_{CCD} generate a reset, because these protect the CPUs and fault logic. The BOD and OVD circuits on V_{DDA_ADC} can be configured to generate either a reset, or a fault.

3.2.2 Regulators

CYT2CL contains two regulators that provide power to the low-voltage core transistors: DeepSleep and core internal. These regulators accept a 2.7–5.5-V V_{DDD} supply and provide a low-noise 1.1-V supply to various parts of the device. These regulators are automatically enabled and disabled by hardware and firmware when switching between power modes. The core internal regulators operate in Active mode, and provide power to the CPU subsystem and associated peripherals.

3.2.2.1 DeepSleep

The DeepSleep regulator is used to maintain power to a small number of blocks when in DeepSleep mode. These blocks include the ILO and WDT timers, BOD detector, SCB0, SRAM memories, Smart I/O, and other configuration memories. The DeepSleep regulator is enabled when in DeepSleep mode, and the core internal regulator is disabled. It is disabled when XRES_L is asserted (LOW) and when the core internal regulator is disabled.

3.2.2.2 Core internal

The core internal regulator supports load currents up to 150 mA, and is operational during device startup (boot process), and in Active/Sleep modes.

3.2.3 Clock system

The CYT2CL clock system provides clocks to all subsystems that require them, and glitch-free switching between different clock sources. In addition, the clock system ensures that no metastable conditions occur.

The clock system for CYT2CL consists of the 8-MHz IMO, two ILOs, three watchdog timers, three PLLs, an FLL, five clock supervisors (CSV), a 7.2- to 33.34-MHz ECO, a 4- to 8-MHz LPECO, and a 32.768-kHz WCO.

The clock system supports two main clock domains: CLK_HF and CLK_LF.

- CLK_HFx are the active domain clocks. Each can use any of the high-frequency clock sources including IMO, EXT_CLK, ECO, LPECO, FLL, or PLL.
- CLK_LF is a DeepSleep domain clock and provides source for MCWDT or RTC modules. The reference clock for the CLK_LF domain is selectable from ILO0, ILO1, WCO, or disabled.

Table 3-1 CLK_HF destinations

Name	Description
CLK_HF0	CPUSS clocks, PERI, and AHB infrastructure
CLK_HF1	Event Generator, also available in HSIOM as an output
CLK_HF2	Sound Subsystem #0
CLK_HF3	Sound Subsystem #1
CLK_HF4	Sound Subsystem #2
CLK_HF5	SMIF #0

3.2.3.1 IMO clock source

The IMO is the frequency reference in CYT2CL when no external reference is available or enabled. The IMO operates at a frequency of around 8 MHz.

3.2.3.2 ILO clock source

An ILO is a low-power oscillator, nominally 32.768 kHz, which generates clocks for a watchdog timer when in DeepSleep mode. There are two ILOs to ensure CSV (clock supervisor) capability in DeepSleep mode. ILO-driven counters can be calibrated to the IMO, WCO, or ECO to improve their accuracy. ILO1 is also used for clock supervision.

3.2.3.3 PLL and FLL

A PLL (two 200 MHz and one 400 MHz) or FLL may be used to generate high-speed clocks from the IMO, ECO, or an EXT_CLK. The FLL provides a much faster lock than the PLL (5 µs instead of 35 µs) in exchange for a small amount (±2%) of frequency error[7] and a lower max output frequency (100 MHz instead of up to 400 MHz). 400-MHz PLLs supports spread spectrum clock generation (SSCG) with down spreading.

3.2.3.4 Clock supervisor

Each clock supervisor (CSV) allows one clock (reference) to supervise the behavior of another clock (monitored). Each CSV has counters for both the monitored and reference clocks. Parameters for each counter determine the frequency of the reference clock as well as the upper and lower frequency limits of the monitored clock. If the frequency range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled and either a reset or an interrupt is generated.

3.2.3.5 EXT_CLK

One of two I/Os can be used to provide an external clock input of up to 100 MHz. This clock can be used as the source clock for either the PLL or FLL, or can be used directly by the CLK_HF domain.

3.2.3.6 ECO

The ECO provides high-frequency clocking using an external crystal connected to the ECO_IN and ECO_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 7.2 to 33.34 MHz. When used in conjunction with the PLL, it generates CPU and peripheral clocks up to device's maximum frequency. ECO accuracy depends on the selected crystal. If the ECO is disabled, the associated pins can be used for any of the available I/O functions.

Note
7. Operation of reference-timed peripherals (such as a UART) with an FLL-based reference is not recommended due to the allowed frequency error.

3.2.3.7 LPECO

The LPECO provides high-frequency clocking using an external crystal connected to the LPECO_IN and LPECO_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 3.99 to 8.01 MHz. LPECO can operate during DeepSleep, and Hibernate modes with significant lower current consumptions. It can also be used for real-time-clock applications. When used in conjunction with the PLL, it generates CPU and peripheral clocks up to device's maximum frequency.

3.2.3.8 WCO

The WCO is a low-power, watch-crystal oscillator intended for real-time-clock applications. It requires an external 32.768-kHz crystal connected to the WCO_IN and WCO_OUT pins. The WCO can also be configured as a clock reference for CLK_LF, which is the clock source for the MCWDT and RTC.

3.2.4 Reset

CYT2CL can be reset from a variety of sources, including software. Reset events are asynchronous and guarantee reversion to a known state. The reset cause (POR, BOD, OVD, overcurrent, XRES_L, WDT, MCWDT, software reset, fault, CSV, Hibernate wakeup, debug) is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES_L pin is available for external reset.

3.2.5 Watchdog timers

CYT2CL has one watchdog timer (WDT) and two multi-counter watchdog timers (MCWDT).

The WDT is a free-running counter clocked only by ILO0, which allows it to be used as a wakeup source from Hibernate. This allows watchdog operation during all power modes and needs to be serviced during a configured window, otherwise generates a watchdog reset, if not serviced before the timeout occurs. A watchdog reset is recorded in the Reset Cause register.

An MCWDT is available for each of the CPU cores. These timers provide more capabilities than the WDT, and are only available in the Active, Sleep, and DeepSleep modes. These timers have multiple counters that can be used separately or cascaded to trigger interrupts and/or resets. They are clocked from ILO0 or the WCO.

3.2.6 Power modes

CYT2CL has six different power modes:

- Active – All peripherals are available
- Low-Power Active (LPACTIVE) – Low-power profile of Active mode where all peripherals and the CPUs are available, but with limited capability
- Sleep – All peripherals except the CPUs are available
- Low-Power Sleep (LPSLEEP) – Low-power profile of Sleep mode where all peripherals except the CPUs are available, but with limited capability
- DeepSleep – Only peripherals which work with CLK_LF are available
- Hibernate – The device and I/O states are frozen; the device resets on wakeup

3.3 Peripherals

3.3.1 Peripheral clock dividers

Integer and fractional clock dividers are provided for peripheral and timing purposes.

Table 3-2 Clock dividers

Divider	Count	Description
div_8	11	Integer divider, 8 bits
div_16	16	Integer divider, 16 bits
div_16_5	4	Fractional divider, 16.5 bits (16 integer bits, 5 fractional bits)
div_24_5	11	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

3.3.2 Peripheral protection unit

The Peripheral protection unit (PPU) controls and monitors unauthorized access from all masters (CPU, P-/M-DMA, Crypto, and any enabled debug interface) to the peripherals. It allows or restricts data transfers on the bus infrastructure. The access rules are enforced based on specific properties of a transfer, such as an address range for the transfer and access attributes (such as read/write, user/privilege, and secure/non-secure).

3.3.3 12-bit SAR ADC

CYT2CL contains one 1-Msps SAR ADCs. This ADC can be clocked at up to 26.67 MHz and provide a 12-bit result in 26 clock cycles.

The references for the SAR ADC comes from a dedicated pair of inputs: VREFH and VREFL[8].

CYT2CL supports 32 logical ADC channels which can select one of 54 input sources. Sources include 48 external inputs from I/Os, and six internal connections for diagnostic and monitoring purposes.

The number of ADC channels (per ADC and package type) are listed in **Table 1-1**.

SAR ADC has a sequencer, which autonomously cycles through the configured channels (sequencer scan) with zero-switching overhead (that is, the aggregate sampling bandwidth, when clocked at 26.67 MHz, is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is controlled through a state machine or firmware. The sequencer prioritizes trigger requests, enables the appropriate analog channel, controls ADC sampling, initiates ADC data conversion, manages results, and initiates subsequent conversions for repetitive or group conversions without CPU intervention.

SAR ADC has two analog multiplexers used to connect the signals to be measured to the ADC. One is SARMUX0 which has 24 GPIO_STD inputs (ADC[0]_0 to ADC[0]_23), and six additional inputs to measure internal signals such as a band-gap reference, a temperature sensor, V_{CCD}, V_{DDA_ADC} power supplies and AMUXBUSA/B signals. The other multiplexer is SARMUX1 which has 24 GPIO_SMC inputs (ADC[1]_0 to ADC[1]_23).

CYT2CL has a temperature sensor. Software post processing is required to convert the temperature sensor reading into kelvin or Celsius values.

To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmed for each channel. ADC also supports range comparison, which allows fast detection of out-of-range values without having to wait for a sequencer scan to complete and for the CPU firmware to evaluate the measurement for out-of-range values.

The ADC is not usable in DeepSleep and Hibernate modes as they require a high-speed clock. The ADC input reference voltage VREFH range is 2.7 V to V_{DDA_ADC} and VREFL is V_{SSA_ADC}.

Note
8. VREF_L prevents IR drops in the VSSIO and VSSA_ADC paths from impacting the measurements. VREF_L, when properly connected, reduces or removes the impact of IR drops in the VSSIO and VSSA_ADC paths from measurements.

3.3.4 Timer/counter/PWM block (TCPWM)

The TCPWM block consists of 16-bit (46 channels) and 32-bit (16 channels) counters with user-programmable period. Twelve of the 16-bit counters are optimized for DC and stepper motor-control operations. Each TCPWM counter contains a capture register to record the count at the time of an event, a period register (used to either stop or auto-reload the counter when its count is equal to the period register), and compare registers to generate signals that are used as PWM duty-cycle outputs.

Each counter within the TCPWM block supports several functional modes such as timer, capture, quadrature, PWM, PWM with dead-time insertion (PWM_DT, 8-bit), pseudo-random PWM (PWM_PR), and shift-register.

The TCPWM block also provides true and complement outputs, with programmable offset between them, to allow their use as deadband complementary PWM outputs. The TCPWM block also has a kill input (only for the PWM mode) to force outputs to a predetermined state; for example, this may be used in motor-drive systems when an overcurrent state is detected and the PWMs driving the FETs need to be shut off immediately (no time for software intervention).

Twelve of the 16-bit counters are optimized for DC and stepper motor-control operations, these also have ZPD (Zero Point detection) and slew rate control capabilities. Two of these TCPWM channels constitute one SMC channel.

3.3.5 Serial Communication Blocks (SCB)

CYT2CL contains 12 serial communication blocks, each configurable to support I^2C, UART, or SPI.

3.3.5.1 I^2C interface

An SCB can be configured to implement a full I^2C master (capable of multi-master arbitration) or slave interface. Each SCB configured for I^2C can operate at speeds of up to 1 Mbps (Fast-mode Plus[9]) and has flexible buffering options to reduce the interrupt overhead and latency of the CPU. In addition, each SCB supports FIFO buffering for receive and transmit data, which, by increasing the time for the CPU to read the data, reduces the need for clock stretching. The I^2C interface is compatible with Standard, Fast-mode, and Fast-mode Plus devices as specified in the NXP I^2C-bus specification and user manual (UM10204). The I^2C-bus I/O is implemented with GPIO in open-drain modes[10, 11].

3.3.5.2 UART interface

When configured as a UART, each SCB provides a full-featured UART with maximum signaling rate determined by the configured peripheral-clock frequency and over-sampling rate. It supports infrared interface (IrDA) and SmartCard (ISO 7816) protocols, which are minor variants of the UART protocol. It also supports the 9-bit multi-processor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity, number of stop bits, break detect, and frame error are supported. FIFO buffering of transmit and receive data allows greater CPU service latencies to be tolerated.

The LIN protocol is supported by the UART. LIN is based on a single-master multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports only LIN slave functionality. Compared to the dedicated LIN blocks, an SCB/UART used for LIN requires a higher level of software interaction and increased CPU load.

Notes
9. I/Os drive level does not support the full bus capacitance in Fast-mode Plus speeds.
10. This is not 100 percent compliant with the I^2C-bus specification; I/Os are not high-voltage compliant, do not support the 20-mA sink requirement of Fast-mode Plus, and violate the leakage specification when no power is applied.
11. See **Table 27-10** 'Serial Communication Block (SCB) specifications' for supported IO-cells and I^2C modes.

3.3.5.3 SPI interface

The SPI configuration supports full Motorola SPI, TI Synchronous Serial Protocol (SSP, essentially adds a start pulse that is used to synchronize SPI-based codecs), and National Microwire (a half-duplex form of SPI). The SPI interface can use the FIFO and operates with up to a 12.5-MHz SPI Clock. SCB also supports EZSPI[12] mode.

SCB0 supports the following additional features:

- Operable as a slave in DeepSleep mode
- I^2C slave EZ (EZI2C[13]) mode with up to 256-B data buffer for multi-byte communication without CPU intervention
- I^2C slave externally-clocked operations
- Command/response mode with a 512-B data buffer for multi-byte communication without CPU intervention

3.3.6 CAN FD

CYT2CL supports two CAN FD controller blocks, each supporting two CAN FD channel. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware. All functions concerning the handling of messages are implemented by the Rx and Tx handlers. The Rx handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The Tx handler is responsible for the transfer of transmit messages from the message RAM, to the CAN core, and provides transmit-message status.

3.3.7 Local interconnect network (LIN)

CYT2CL contains up to two LIN channels. Each channel supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN channel connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each channel also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

3.3.8 Clock extension peripheral interface (CXPI)

CYT2CL contains up to two CXPI channels compliant with JASO D015 and ISO standard 20794 including the controller specification.

Each channel supports:

- Master and slave functionality
- Polling and event trigger method for both normal and long frames
- Non-return to zero (NRZ) and PWM signaling modes
- Collision resolution and carries sense multiple access
- Wakeup pulse generation and detection
- CRC8 and CRC16 for both normal and long frames
- Error detection
- Dedicated FIFO (16 B) for transmit and receive

Notes

12. The Easy SPI (EZSPI) protocol is based on the Motorola SPI operating in any mode (0, 1, 2, or 3). It allows communication between master and slave, and reduces the need for CPU intervention.
13. The Easy I^2C (EZI2C) protocol is a unique communication scheme built on top of the I^2C protocol by Infineon. It uses a meta protocol around the standard I^2C protocol to communicate to an I^2C slave using indexed memory transfers. This reduces the need for CPU intervention.

3.3.9 Serial memory interface

In addition to the internal flash memory, CYT2CL supports direct connection to 128 MB of external flash or RAM memory. This connection is made through either a xSPI or serial peripheral interface (SPI). xSPI allows connection to HYPERFLASH™ and HYPERRAM™ devices, while SPI (single, dual, quad, or octal SPI) can connect with serial flash memory. Code stored in memory connected through this interface allows execute-in-place (XIP) operation, which does not require the instructions to be first copied to internal memory, and on-the-fly encryption and decryption for environments requiring secure external data and code.

3.3.10 Sound subsystem

CYT2CL supports the following,

- Up to two time-division multiplexing (TDM) interfaces
  - Full-duplex transmitter and receiver operation
  - Independent transmitter or receiver operation, each in master or slave mode
  - Up to 16 channels, each channel can be individually enabled or disabled
- Up to two pulse code modulation-pulse width modulation (PCM-PWM) interface
  - Conversion of PCM audio streaming to PWM signals
  - Up to 32-bit output sample resolution
  - Supports E- and H-bridge formats
  - Dead time insertion
- Up to five sound generator (SG) interfaces
  - PWM modulated (amplitude, tone) sound generation
  - Separate volume and frequency control (two signals) and combined volume-frequency control (one signal) formats
- One mixer supporting five input sources
  - Combines multiple PCM source streams into a single PCM destination stream
  - PCM source stream can be gain/volume controlled
  - Fixed PCM sample formatting (16-bit pairs)
  - LPF support by FIR filter
  - Fade-in and Fade-out control for both source and destination PCM streams

3.3.11 One-time-programmable (OTP) eFuse

CYT2CL devices contain a 1024-bit OTP eFuse memory that can be used to store and access a unique and unalterable identifier or serial number for each device. eFuses are also used to control the device life-cycle (manufacturing, programming, normal operation, end-of-life, and so on) and the security state. Of the 1024 bits, 192 are available for user purposes.

3.3.12 Event generator

The event generator supports generation of interrupts and triggers in the Active mode and interrupts in the DeepSleep mode. The event generators are used to trigger a specific device function (execution of an interrupt handler, a SAR ADC conversion, and so on) and to provide a cyclic wakeup mechanism from the DeepSleep mode. They provide CPU-free triggers for device functions, and reduce CPU involvement in triggering device functions, thus reducing overall power consumption and processing overhead.

3.3.13 Trigger multiplexer

CYT2CL supports connecting various peripherals using trigger signals. Triggers are used to inform a peripheral of the occurrence of an event or change of state. These triggers are used to affect or initiate some action in other peripherals. The trigger multiplexer is used to route triggers from a source peripheral to a destination. Triggers provide active logic functionality and are typically supported in the Active mode.

3.3.14 LCD controller

CYT2CL supports the following:

- Up to 32 segments (SEG) and four commons (COM)
- Type A (standard) and Type B (low-power) drive waveforms
- Configuration of any GPIO pin as a common or segment
- Three drive methods:
  - Digital correlation
  - PWM at 1/2 bias
  - PWM at 1/3 bias
- Active, Sleep, and Deep Sleep mode operations
- Digital contrast control

3.4 I/Os

CYT2CL has up to 140 programmable I/Os.

The I/Os are organized as logical entities called ports, which are a maximum of 8 bits wide. During power-on and reset, the I/Os are forced to the High-Z state. During the Hibernate mode, the I/Os are frozen.

Every I/O can generate an interrupt (if enabled) and each port has an interrupt request (IRQ) and interrupt service routine (ISR) associated with it.

The I/O port power source mapping is listed in **Table 3-3**. The associated supply determines the V_{OH}, V_{OL}, V_{IH}, and V_{IL} levels when configured for CMOS and Automotive thresholds.

Table 3-3 I/O port power source

Supply	Ports
VDDD	P0, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19
VDDIO_GPIO	P1, P2, P3, P4
VDDIO_HSIO	P8, P9
VDDIO_SMC	P5, P6, P7

Each I/O implements the following:

- Programmable drive mode
  - High impedance
  - Resistive pull-up
  - Resistive pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up or pull-down
  - Weak pull-up or pull-down

CYT2CL has four types of programmable GPIOs: GPIO Standard, GPIO Enhanced, GPIO SMC, HSIO Standard with Low noise. Only GPIO_STD, GPIO_ENH, and GPIO_SMC have the capability to wakeup the device from DeepSleep mode.

3.4.1 GPIO

Three types of GPIOs are supported:

- GPIO_STD, GPIO_ENH, and GPIO_SMC

These implement the following:

- Configurable input threshold (CMOS, TTL, or Automotive)
- Hold mode for latching previous state (used for retaining the I/O state in DeepSleep mode)
- Analog input mode (input and output buffers disabled)
- Edge-triggered interrupts on rising edge, falling edge, or on both the edges, on pin basis

3.4.1.1 GPIO standard (GPIO_STD)

Supports standard automotive signaling across the 2.7-V to 5.5-V V_{DDIO} range. GPIO Standard I/Os have multiple configurable drive levels, drive modes, and selectable input levels.

3.4.1.2 GPIO enhanced (GPIO_ENH)

Supports extended functionality automotive signaling across the 2.7-V to 5.5-V V_{DDIO} range with higher currents at lower voltages (full I^2C timing support, slew-rate control).

3.4.1.3 GPIO SMC (GPIO_SMC)

Provides significant drive strength than GPIO_STD and GPIO_ENH (Supports 30-mA drive).

3.4.2 HSIO

These I/Os are optimized exclusively for high-speed signaling and do not support slew-rate control, DeepSleep operation, POR mode control, analog connections, or non-CMOS signaling levels. HSIOs support programmable drive strength. They are available only in Active mode.

3.4.2.1 HSIO standard low noise (HSIO_STDLN)

Supports clocking and signaling up to 100 MHz. Also supports holding state during DeepSleep mode. Low noise version optimizes the noise generated by having specific modes for each interface support.

3.4.3 Port nomenclature

Px.y describes a particular bit “y” available within an I/O port “x.”

- For example, P4.2 reads “port 4, bit 2”.

3.4.4 Smart I/O

Smart I/O allows Boolean operations on signals going to the I/O from the subsystems of the chip or on signals coming into the chip. CYT2CL has one Smart I/O block. Operation can be synchronous or asynchronous and the blocks operate in all device power modes except for the Hibernate mode.

4 CYT2CL address map

The CYT2CL microcontroller supports the memory spaces shown in **Figure 4-1**:

- Code-flash
  - 4160 KB (4032 KB + 128 KB) of code-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
    - Single-bank mode - 4160 KB
    - Dual-bank mode - 2080 KB per bank
- Work-flash
  - 128 KB (96 KB + 32 KB) of work-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
    - Single-bank mode - 128 KB
    - Dual-bank mode - 64 KB per bank
- 32 KB of secure ROM
- 512 KB of SRAM (First 2 KB is reserved for internal usage)
- 128 MB SMIF XIP

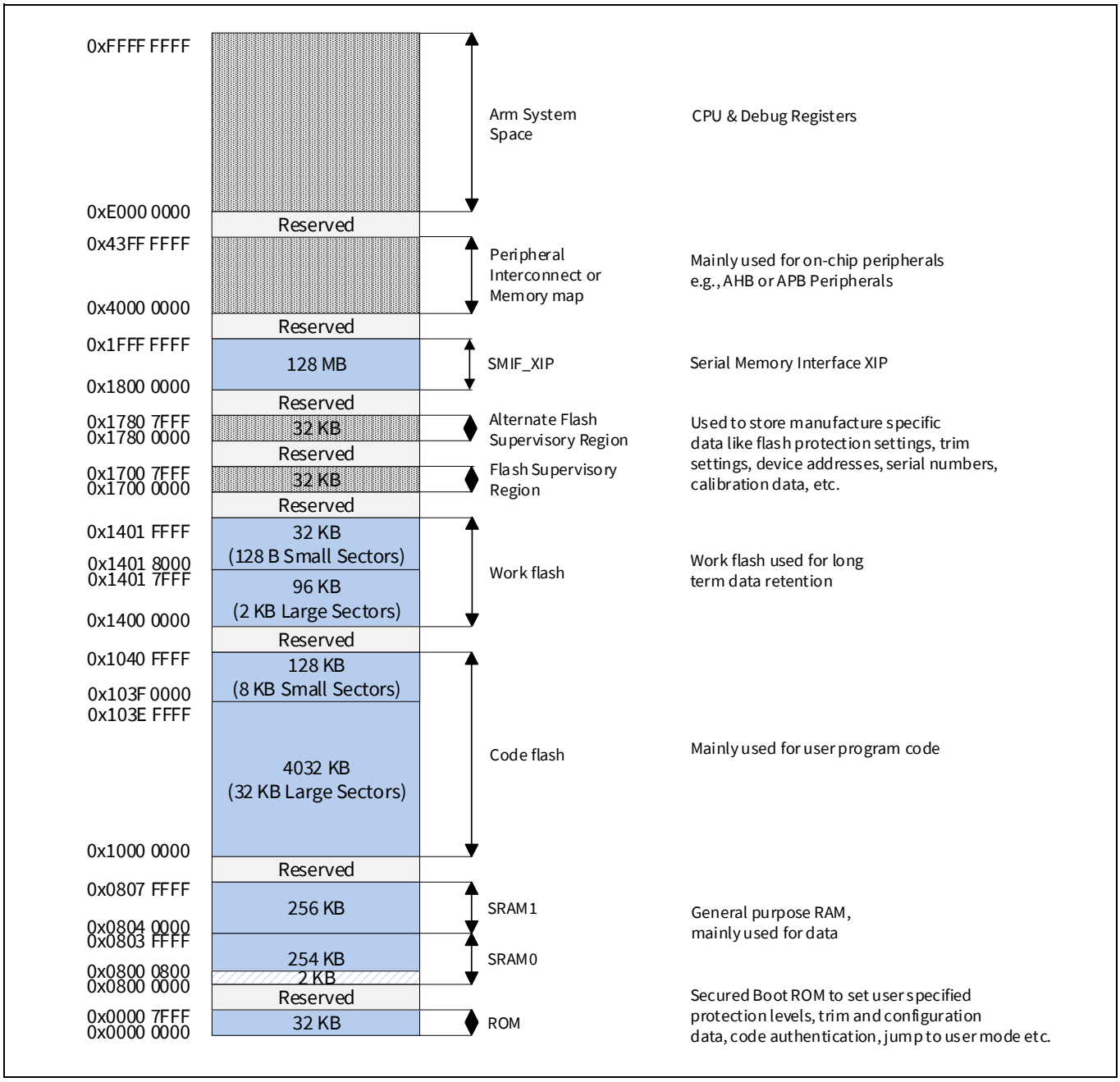


Figure 4-1 CYT2CL address map[14, 15]

Notes
14. The size representation is not up to scale.
15. First 2KB of SRAM is reserved, not available for users. User must keep the power of first 32KB block of SRAM0 in enabled or retained in all Active, LP Active, Sleep, LP Sleep, DeepSleep modes.

5 Flash base address map

Table 5-1 through Table 5-6 give information about the sector mapping of the code- and work-flash regions along with their respective base addresses.

Table 5-1 Code-flash address mapping in single bank mode

Code-flash Size (KB)	Large Sectors (LS)	Small Sectors (SS)	Large Sector Base Address	Small Sector Base Address
4160	32 KB × 126	8 KB × 16	0x1000 0000	0x103F 0000

Table 5-2 Work-flash address mapping in single bank mode

Work-flash Size (KB)	Large Sectors	Small Sectors	Large Sector Base Address	Small Sector Base Address
128	2 KB × 48	128 B × 256	0x1400 0000	0x1401 8000

Table 5-3 Code-flash address mapping in dual bank mode (Mapping A)

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
4160	32 KB × 63	8KB × 8	32 KB × 63	8 KB × 8	0x1000 0000	0x101F 8000	0x1200 0000	0x121F 8000

Table 5-4 Code-flash address mapping in dual bank mode (Mapping B)

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
4160	32 KB × 63	8 KB × 8	32 KB × 63	8 KB × 8	0x1200 0000	0x121F 8000	0x1000 0000	0x101F 8000

Table 5-5 Work-flash address mapping in dual bank mode (Mapping A)

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1400 0000	0x1400 C000	0x1500 0000	0x1500 C000

Table 5-6 Work-flash address mapping in dual bank mode (Mapping B)

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1500 0000	0x1500 C000	0x1400 0000	0x1400 C000

6 Peripheral I/O map

Table 6-1 CYT2CL peripheral I/O map

Section	Description	Base address	Instances	Instance size	Group	Slave
PERI	Peripheral interconnect	0x4000 0000			0	0
	Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9)	0x4000 4000	9	0x20		
	Peripheral trigger group	0x4000 8000	13	0x400		
	Peripheral 1:1 trigger group	0x4000 C000	13	0x400		
PERI_MS	Peripheral interconnect, master interface	0x4001 0000			0	1
	PERI Programmable PPU	0x4001 0000	6[16]	0x40		
	PERI Fixed PPU	0x4001 0800	450	0x40		
Crypto	Cryptography component	0x4010 0000			1	0
CPUSS	CPU subsystem (CPUSS)	0x4020 0000			2	0
FAULT	Fault structure subsystem	0x4021 0000			2	1
	Fault structures	0x4021 0000	4	0x100		
IPC	Inter process communication	0x4022 0000			2	2
	IPC structures	0x4022 0000	8	0x20		
	IPC interrupt structures	0x4022 1000	8	0x20		
PROT	Protection	0x4023 0000			2	3
	Shared memory protection unit structures	0x4023 2000	16	0x40		
	Memory protection unit structures	0x4023 4000	16	0x400		
FLASHC	Flash controller	0x4024 0000			2	4
SRSS	System Resources Sub-System Core Registers	0x4026 0000			2	5
	Clock Supervision High Frequency	0x4026 1400	3	0x10		
	Clock Supervision Reference Frequency	0x4026 1710	1			
	Clock Supervision Low Frequency	0x4026 1720	1			
	Clock Supervision Internal Low Frequency	0x4026 1730	1			
	Multi Counter WDT	0x4026 8000	2	0x100		
	Free Running WDT	0x4026 C000	1			
BACKUP	SRSS Backup Domain/RTC	0x4027 0000			2	6
	Backup Register	0x4027 1000	4	0x04		
P-DMA	P-DMA0 Controller	0x4028 0000			2	7
	P-DMA0 channel structures	0x4028 8000	76	0x40		
	P-DMA1 Controller	0x4029 0000			2	8
	P-DMA1 channel structures	0x4029 8000	84	0x40		
M-DMA	M-DMA0 Controller	0x402A 0000			2	9
	M-DMA0 channels	0x402A 1000	4	0x100		
eFUSE	eFUSE Customer Data (192 bits)	0x402C 0868	6	0x04	2	10
HSIOM	High-Speed I/O Matrix (HSIOM)	0x4030 0000	20	0x10	3	0
GPIO	GPIO port control/configuration	0x4031 0000	20	0x80	3	1

Note
16. These six Programmable PPUs are configured by the Boot ROM and are available for the user based on the access rights. Refer to the device specific TRM to know more about the configuration of these programmable PPUs.

Table 6-1 CYT2CL peripheral I/O map *(continued)*

Section	Description	Base address	Instances	Instance size	Group	Slave
SMARTIO	Programmable I/O configuration	0x4032 0000			3	2
	SMART I/O port configuration	0x4032 0C00	1	0x100		
TCPWM	Timer/Counter/PWM 0 (TCPWM0)	0x4038 0000			3	3
	TCPWM0 Group #0 (16-bit)	0x4038 0000	34	0x80		
	TCPWM0 Group #1 (16-bit, Motor control)	0x4038 8000	12	0x80		
	TCPWM0 Group #2 (32-bit)	0x4039 0000	16	0x80		
LCD	LCD Controller	0x403B 0000			3	4
	LCD Data	0x403B 0100	4	0x100		
EVTGEN	Event generator 0 (EVTGEN0)	0x403F 0000			3	5
	Event generator 0 comparator structures	0x403F 0800	16	0x20		
SMIF	Serial Memory Interface 0 (SMIF0)	0x4042 0000			4	0
	SMIF0 Devices	0x4042 0800	2	0x80		
LIN	Local Interconnect Network 0 (LIN0)	0x4050 0000			5	0
	LIN0 Channels	0x4050 8000	2	0x100		
CXPI	Clock Extension Peripheral Interface 0 (CXPI0)	0x4051 0000			5	1
	CXPI0 Channels	0x4051 8000	2	0x100		
TTCANFD	CAN0 controller	0x4052 0000	2	0x200	5	2
	Message RAM CAN0	0x4053 0000		0x2000		
	CAN1 controller	0x4054 0000	2	0x200	5	3
	Message RAM CAN1	0x4055 0000		0x2000		
SCB	Serial Communications Block (SPI/UART/I^2C)	0x4060 0000	12	0x10000	6	0-11
Sound	Time Division Multiplexer 0 (TDM0)	0x4081 0000			8	0
	TDM0 Structures	0x4081 8000	2	0x200		
	Sound Generator 0 (SG0)	0x4082 0000			8	1
	SG0 Structures	0x4082 8000	5	0x100		
	Pulse Width Modulation 0 (PWM0)	0x4083 0000			8	2
	PWM0 Structures	0x4083 8000	2	0x100		
	Mixer0	0x4088 0000			8	4
	Mixer0 Source Structures	0x4088 8000	5	0x100		
	Mixer0 Destination Structures	0x4088 C000	1			
SAR PASS	Programmable Analog Subsystem (PASS0)	0x4090 0000			9	0
	SAR0 channel controller	0x4090 0000				
	SAR0 channel structures	0x4090 0800	24	0x40		
	SAR1 channel structures	0x4090 1800	24	0x40		

7 CYT2CL clock diagram

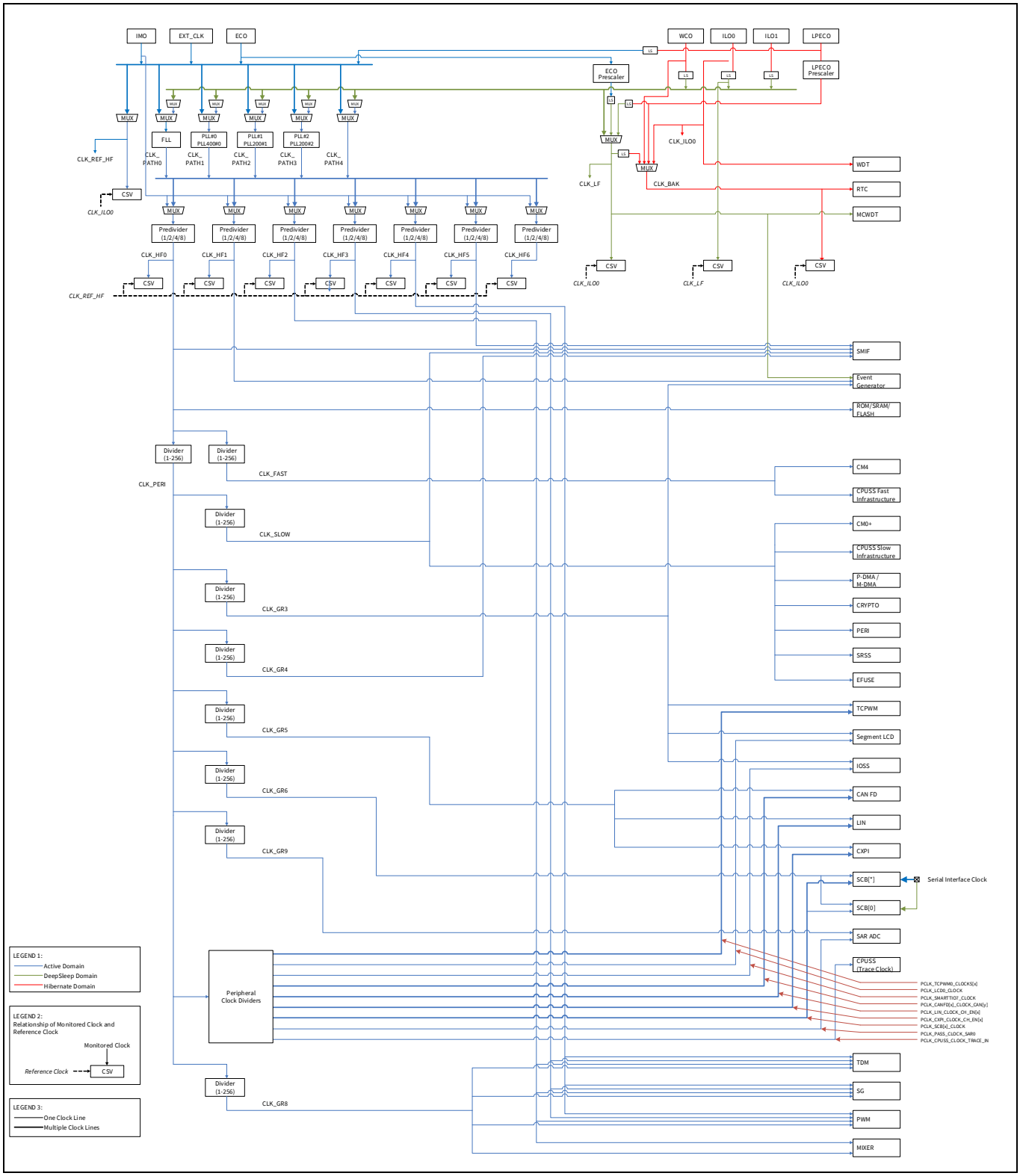


Figure 7-1 CYT2CL clock diagram

8 CYT2CL CPU start-up sequence

The following steps describe the start-up sequence:

1. System Reset (@0x0000 0000)
2. CM0+ executes ROM boot (@0x0000 0004)
   i. Applies trims
   ii. Applies Debug Access port (DAP) access restrictions and system protection from eFuse and supervisory flash
   iii. Authenticates flash boot (only in SECURE life-cycle stage) and transfers control to it
3. CM0+ executes flash boot (from Supervisory flash @0x1700 2000)
   i. Debug pins are configured as per the SWD/JTAG spec[17]
   ii. Sets CM0+ vector offset register (CM0_VTOR part of the Arm® system space) to the beginning of flash (@0x1000 0000)
   iii. CM0+ branches to its Reset handler
4. CM0+ starts execution
   i. Moves CM0+ vector table to SRAM (updates CM0+ vector table base)
   ii. Sets CM4_VECTOR_TABLE_BASE (@0x0000 0200) to the location of CM4 vector table mentioned in flash (specified in CM4 linker definition file)
   iii. Releases CM4 from reset
   iv. Continues execution of CM0+ user application
5. CM4 executes directly from either code-flash or SRAM
   i. CM4 branches to its Reset handler
   ii. Continues execution of CM4 user application

Note
17. Port configuration of SWD/JTAG pins will be changed from the default GPIO mode to support debugging after the boot process, see **Table 11-1** for pin assignments.

9 Pin assignment

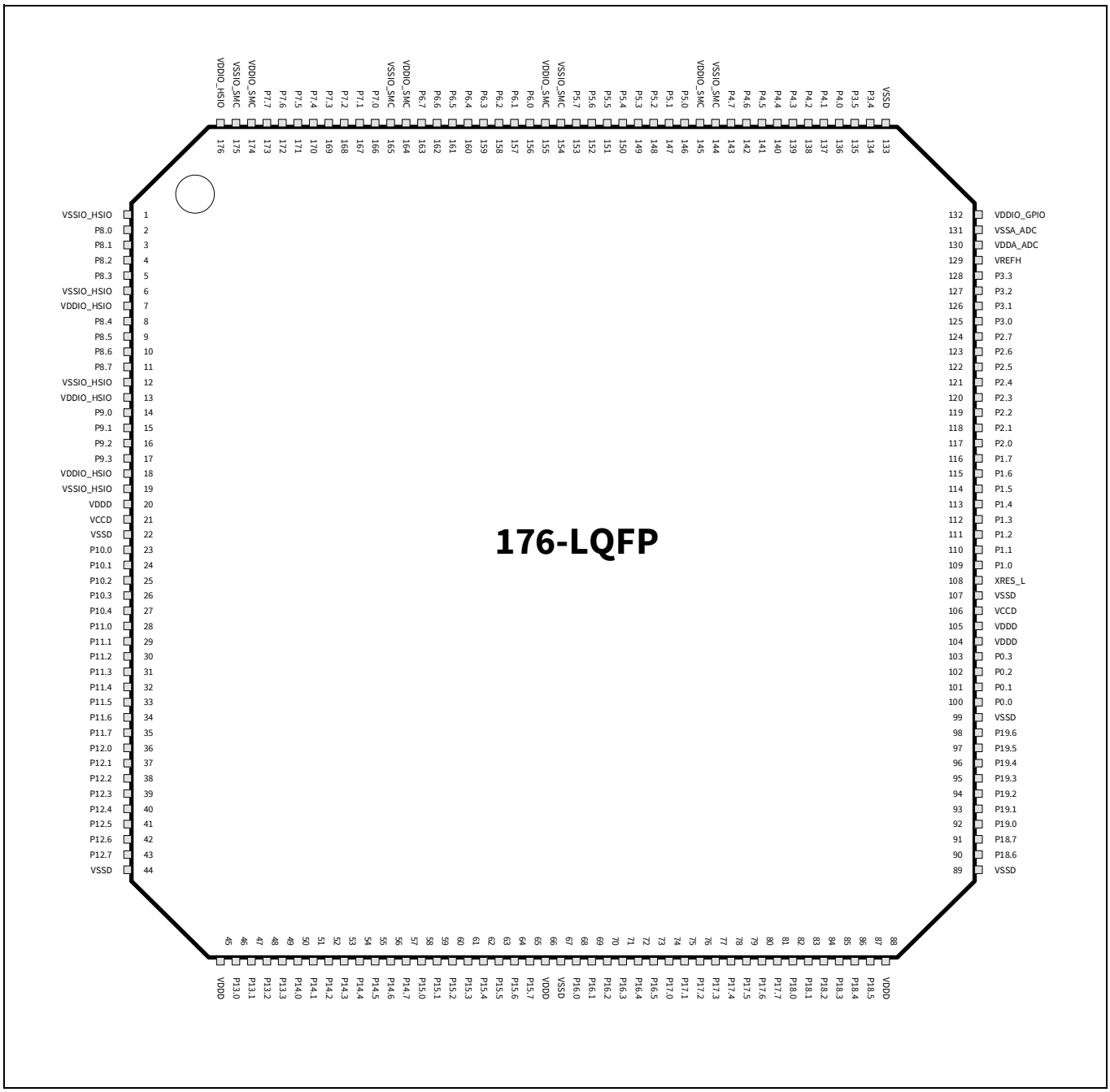


Figure 9-1 176-LQFP pin assignment

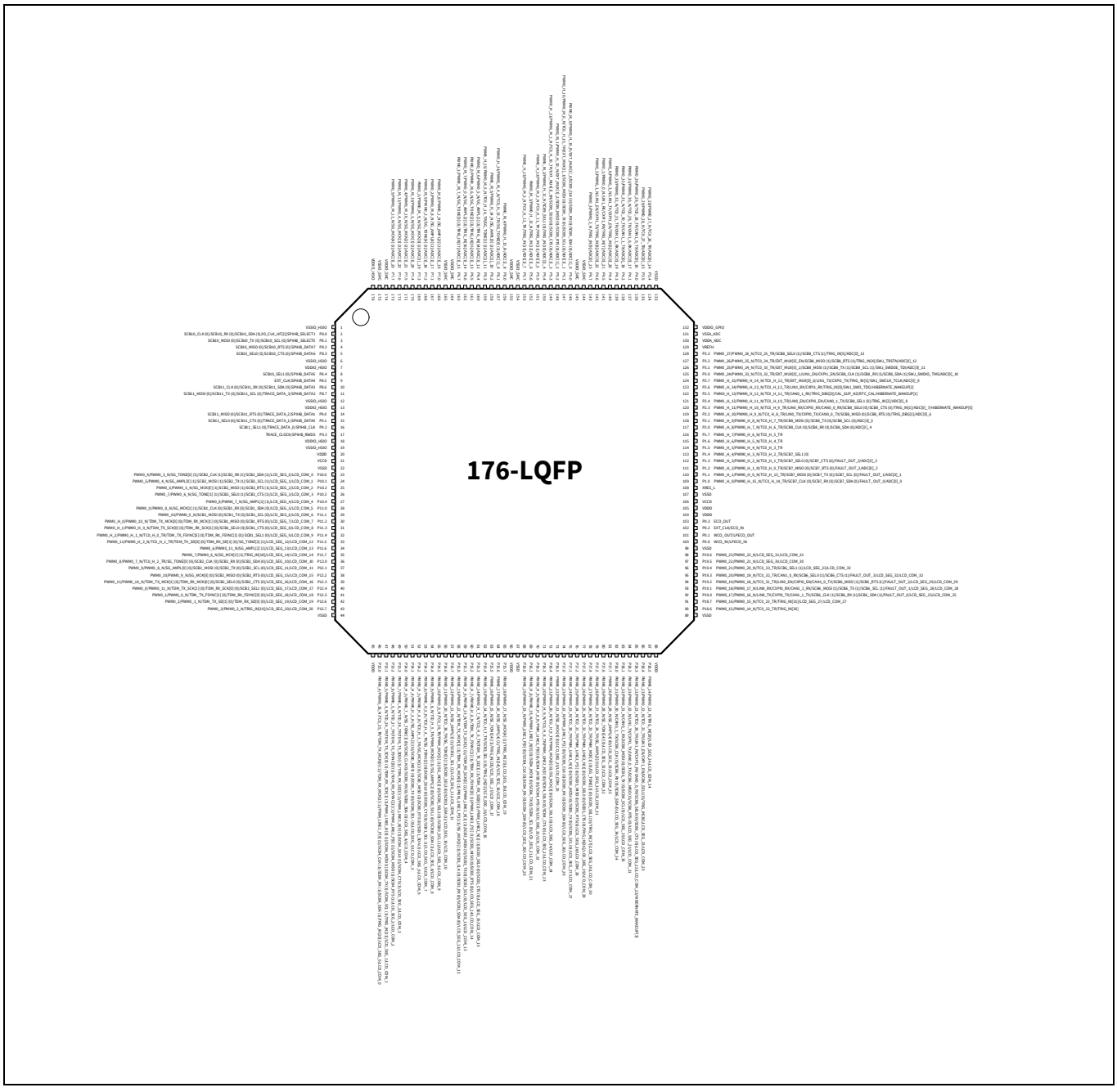


Figure 9-2 176-LQFP pin assignment with alternate functions

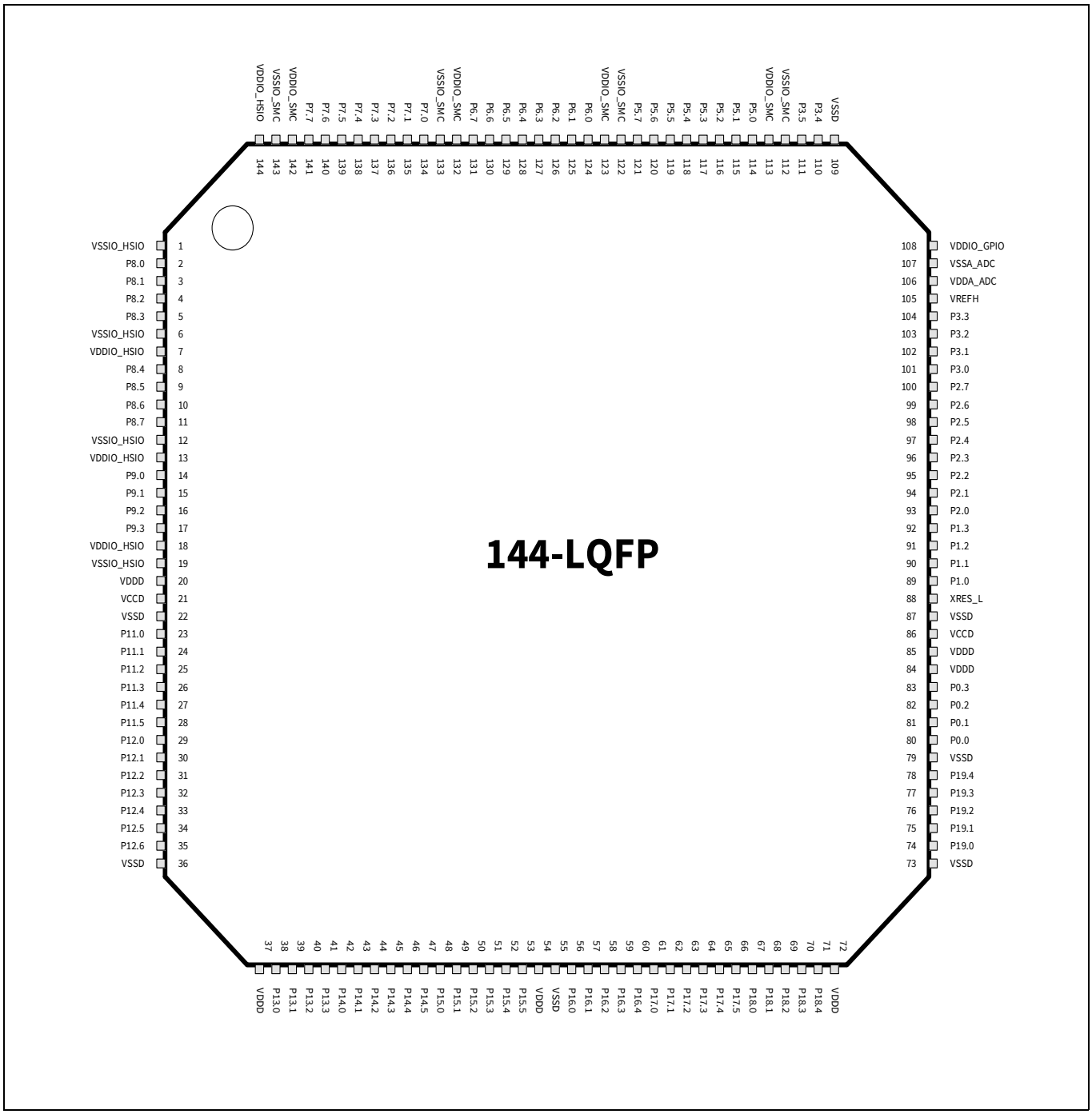


Figure 9-3 144-LQFP pin assignment

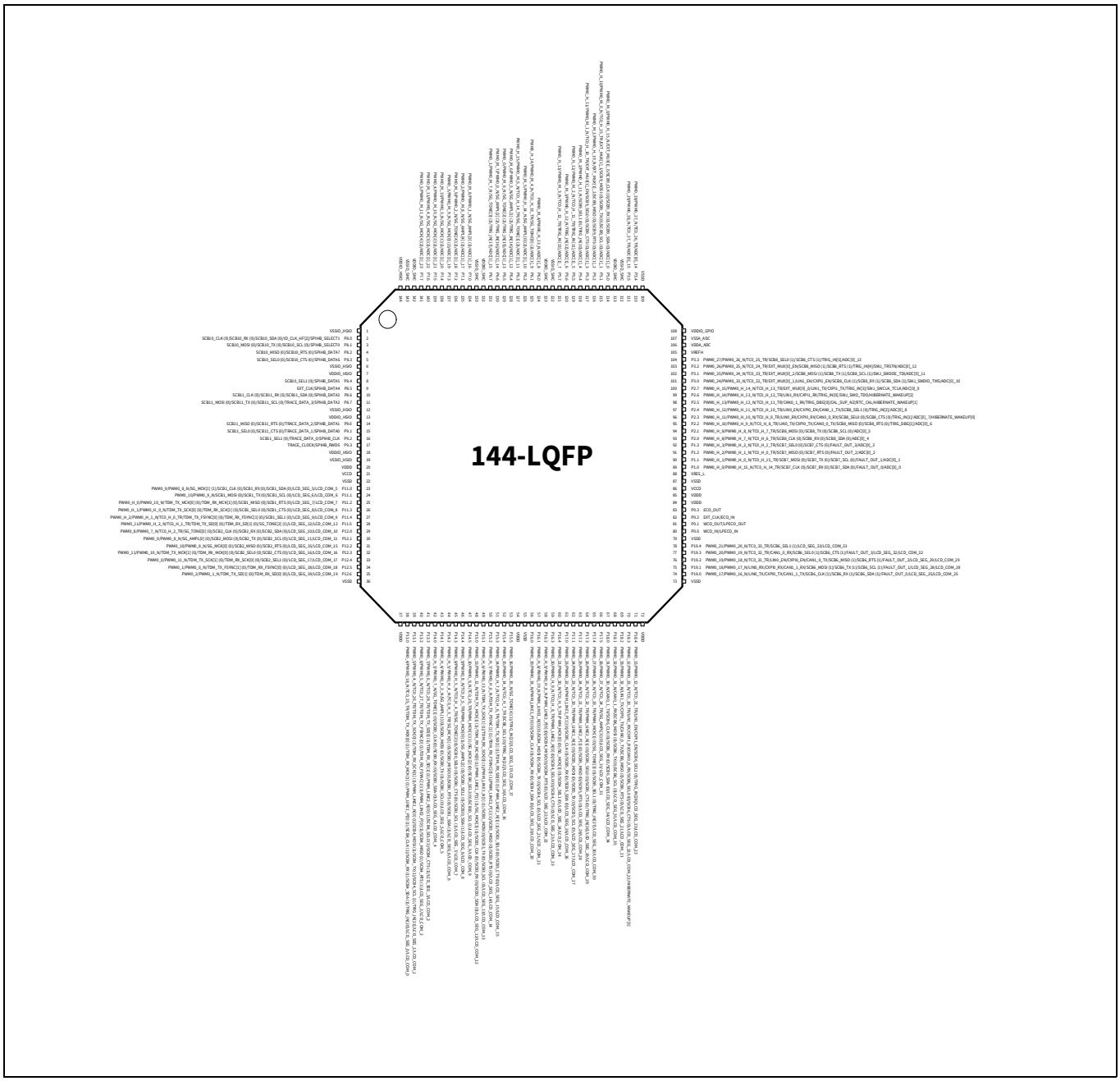


Figure 9-4 144-LQFP pin assignment with alternate functions

10 High-speed I/O matrix connections

Table 10-1 HSIOM connections reference

Name	Number	Description
HSIOM_SEL_GPIO	0	GPIO controls 'out'
HSIOM_SEL_GPIO_DSI	1	Reserved
HSIOM_SEL_DSI_DSI	2	
HSIOM_SEL_DSI_GPIO	3	
HSIOM_SEL_AMUXA	4	
HSIOM_SEL_AMUXB	5	
HSIOM_SEL_AMUXA_DSI	6	
HSIOM_SEL_AMUXB_DSI	7	
HSIOM_SEL_ACT_0	8	Active functionality 0
HSIOM_SEL_ACT_1	9	Active functionality 1
HSIOM_SEL_ACT_2	10	Active functionality 2
HSIOM_SEL_ACT_3	11	Active functionality 3
HSIOM_SEL_DS_0	12	DeepSleep functionality 0
HSIOM_SEL_DS_1	13	DeepSleep functionality 1
HSIOM_SEL_DS_2	14	DeepSleep functionality 2
HSIOM_SEL_DS_3	15	DeepSleep functionality 3
HSIOM_SEL_ACT_4	16	Active functionality 4
HSIOM_SEL_ACT_5	17	Active functionality 5
HSIOM_SEL_ACT_6	18	Active functionality 6
HSIOM_SEL_ACT_7	19	Active functionality 7
HSIOM_SEL_ACT_8	20	Active functionality 8
HSIOM_SEL_ACT_9	21	Active functionality 9
HSIOM_SEL_ACT_10	22	Active functionality 10
HSIOM_SEL_ACT_11	23	Active functionality 11
HSIOM_SEL_ACT_12	24	Active functionality 12
HSIOM_SEL_ACT_13	25	Active functionality 13
HSIOM_SEL_ACT_14	26	Active functionality 14
HSIOM_SEL_ACT_15	27	Active functionality 15
HSIOM_SEL_DS_4	28	DeepSleep functionality 4
HSIOM_SEL_DS_5	29	DeepSleep functionality 5
HSIOM_SEL_DS_6	30	DeepSleep functionality 6
HSIOM_SEL_DS_7	31	DeepSleep functionality 7

11 Package pin list and alternate functions

Most pins have alternate functionality, as specified in **Table 11-1**.

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O [23]

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O
	176-LQFP	144-LQFP	HCon#0	HCon#12[18]	HCon#13	HCon#14	HCon#15	HCon#29		
	Pin	Pin		DS#0[19, 20]	DS#1	DS#2	DS#3	DS#5		
P0.0	100	80	GPIO_STD						WCO_IN, LPECO_IN[21]	
P0.1	101	81	GPIO_STD						WCO_OUT,LPECO_OUT[21]	
P0.2	102	82	GPIO_STD						ECO_IN[21]	
P0.3	103	83	GPIO_STD						ECO_OUT[21]	
P1.0	109	89	GPIO_STD						ADC[0]_0	
P1.1	110	90	GPIO_STD						ADC[0]_1	
P1.2	111	91	GPIO_STD						ADC[0]_2	
P1.3	112	92	GPIO_STD						ADC[0]_3	
P1.4	113	NA	GPIO_STD							
P1.5	114	NA	GPIO_STD							
P1.6	115	NA	GPIO_STD							
P1.7	116	NA	GPIO_STD							
P2.0	117	93	GPIO_STD						ADC[0]_4	
P2.1	118	94	GPIO_STD						ADC[0]_5	
P2.2	119	95	GPIO_STD						ADC[0]_6	
P2.3	120	96	GPIO_STD						ADC[0]_7 HIBERNATE_WAKEUP[0]	
P2.4	121	97	GPIO_STD						ADC[0]_8	
P2.5	122	98	GPIO_STD					RTC_CAL	HIBERNATE_WAKEUP[1]	
P2.6	123	99	GPIO_STD					SWJ_SWO_TDO	HIBERNATE_WAKEUP[2]	
P2.7	124	100	GPIO_STD					SWJ_SWCLK_TCLK	ADC[0]_9	
P3.0	125	101	GPIO_STD					SWJ_SWDIO_TMS	ADC[0]_10	
P3.1	126	102	GPIO_STD					SWJ_SWDOE_TDI	ADC[0]_11	
P3.2	127	103	GPIO_STD					SWJ_TRSTN	ADC[0]_12	

Notes
18. High Speed I/O matrix connection (HCon) reference as per **Table 10-1**.
19. DeepSleep ordering (DS#0, DS#1, DS#2) does not have any impact on choosing any alternate functions; the HSIOM module handles the individual alternate function assignment.
20. All port pin functions available in DeepSleep mode are also available in Active mode.
21. I/O pins that support an oscillator function (WCO or ECO) must be configured for high-impedance if the oscillator is enabled.
22. This I/O will have increased leakage to ground when VDDD is below the POR threshold.
23. For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group “n”.

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O *(continued)*[23]

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O
	176-LQFP	144-LQFP	HCon#0	HCon#12[18]	HCon#13	HCon#14	HCon#15	HCon#29		
	Pin	Pin		DS#0[19, 20]	DS#1	DS#2	DS#3	DS#5		
P3.3	128	104	GPIO_STD						ADC[0]_13	
P3.4	134	110	GPIO_STD						ADC[0]_14	
P3.5	135	111	GPIO_STD						ADC[0]_15	
P4.0	136	NA	GPIO_STD						ADC[0]_16	
P4.1	137	NA	GPIO_STD						ADC[0]_17	
P4.2	138	NA	GPIO_STD						ADC[0]_18	
P4.3	139	NA	GPIO_STD						ADC[0]_19	
P4.4	140	NA	GPIO_STD						ADC[0]_20	
P4.5	141	NA	GPIO_STD						ADC[0]_21	
P4.6	142	NA	GPIO_STD						ADC[0]_22	
P4.7	143	NA	GPIO_STD						ADC[0]_23	
P5.0	146	114	GPIO_SMC						ADC[1]_0	
P5.1	147	115	GPIO_SMC						ADC[1]_1	
P5.2	148	116	GPIO_SMC						ADC[1]_2	
P5.3	149	117	GPIO_SMC						ADC[1]_3	
P5.4	150	118	GPIO_SMC						ADC[1]_4	
P5.5	151	119	GPIO_SMC						ADC[1]_5	
P5.6	152	120	GPIO_SMC						ADC[1]_6	
P5.7	153	121	GPIO_SMC						ADC[1]_7	
P6.0	156	124	GPIO_SMC						ADC[1]_8	
P6.1	157	125	GPIO_SMC						ADC[1]_9	
P6.2	158	126	GPIO_SMC						ADC[1]_10	
P6.3	159	127	GPIO_SMC						ADC[1]_11	
P6.4	160	128	GPIO_SMC						ADC[1]_12	
P6.5	161	129	GPIO_SMC						ADC[1]_13	
P6.6	162	130	GPIO_SMC						ADC[1]_14	
P6.7	163	131	GPIO_SMC						ADC[1]_15	
P7.0	166	134	GPIO_SMC						ADC[1]_16	SMARTIO7_0
P7.1	167	135	GPIO_SMC						ADC[1]_17	SMARTIO7_1
P7.2	168	136	GPIO_SMC						ADC[1]_18	SMARTIO7_2
P7.3	169	137	GPIO_SMC						ADC[1]_19	SMARTIO7_3

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O *(continued)*[23]

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O
	176-LQFP	144-LQFP	HCon#0	HCon#12[18]	HCon#13	HCon#14	HCon#15	HCon#29		
	Pin	Pin		DS#0[19, 20]	DS#1	DS#2	DS#3	DS#5		
P7.4	170	138	GPIO_SMC						ADC[1]_20	SMARTIO7_4
P7.5	171	139	GPIO_SMC						ADC[1]_21	SMARTIO7_5
P7.6	172	140	GPIO_SMC						ADC[1]_22	SMARTIO7_6
P7.7	173	141	GPIO_SMC						ADC[1]_23	SMARTIO7_7
P8.0	2	2	HSIO_STDLN							
P8.1	3	3	HSIO_STDLN							
P8.2	4	4	HSIO_STDLN							
P8.3	5	5	HSIO_STDLN							
P8.4	8	8	HSIO_STDLN							
P8.5	9	9	HSIO_STDLN							
P8.6	10	10	HSIO_STDLN							
P8.7	11	11	HSIO_STDLN							
P9.0	14	14	HSIO_STDLN							
P9.1	15	15	HSIO_STDLN							
P9.2	16	16	HSIO_STDLN							
P9.3	17	17	HSIO_STDLN							
P10.0	23	NA	GPIO_STD	LCD_SEG_0	LCD_COM_0					
P10.1	24	NA	GPIO_STD	LCD_SEG_1	LCD_COM_1					
P10.2	25	NA	GPIO_STD	LCD_SEG_2	LCD_COM_2					
P10.3	26	NA	GPIO_STD	LCD_SEG_3	LCD_COM_3					
P10.4	27	NA	GPIO_STD	LCD_SEG_4	LCD_COM_4					
P11.0	28	23	GPIO_STD	LCD_SEG_5	LCD_COM_5					
P11.1	29	24	GPIO_STD	LCD_SEG_6	LCD_COM_6					
P11.2	30	25	GPIO_STD	LCD_SEG_7	LCD_COM_7					
P11.3	31	26	GPIO_STD	LCD_SEG_8	LCD_COM_8					
P11.4	32	27	GPIO_STD	LCD_SEG_9	LCD_COM_9					
P11.5	33	28	GPIO_STD	LCD_SEG_12	LCD_COM_12					
P11.6	34	NA	GPIO_STD	LCD_SEG_13	LCD_COM_13					
P11.7	35	NA	GPIO_STD	LCD_SEG_14	LCD_COM_14					
P12.0	36	29	GPIO_STD	LCD_SEG_10	LCD_COM_10					
P12.1	37	30	GPIO_STD	LCD_SEG_11	LCD_COM_11					

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O *(continued)*[23]

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O
	176-LQFP	144-LQFP	HCon#0	HCon#12[18]	HCon#13	HCon#14	HCon#15	HCon#29		
	Pin	Pin		DS#0[19, 20]	DS#1	DS#2	DS#3	DS#5		
P12.2	38	31	GPIO_STD	LCD_SEG_15	LCD_COM_15					
P12.3	39	32	GPIO_STD	LCD_SEG_16	LCD_COM_16					
P12.4	40	33	GPIO_STD	LCD_SEG_17	LCD_COM_17					
P12.5	41	34	GPIO_STD	LCD_SEG_18	LCD_COM_18					
P12.6	42	35	GPIO_STD	LCD_SEG_19	LCD_COM_19					
P12.7	43	NA	GPIO_STD	LCD_SEG_20	LCD_COM_20					
P13.0	46	38	GPIO_STD	LCD_SEG_0	LCD_COM_0					
P13.1	47	39	GPIO_STD	LCD_SEG_1	LCD_COM_1					
P13.2	48	40	GPIO_STD	LCD_SEG_2	LCD_COM_2					
P13.3	49	41	GPIO_STD	LCD_SEG_3	LCD_COM_3					
P14.0	50	42	GPIO_ENH	LCD_SEG_4	LCD_COM_4	SCB0_CLK (0)	SCB0_SDA (0)			
P14.1	51	43	GPIO_ENH	LCD_SEG_5	LCD_COM_5	SCB0_MOSI (0)	SCB0_SCL (0)			
P14.2	52	44	GPIO_ENH	LCD_SEG_6	LCD_COM_6	SCB0_MISO (0)				
P14.3	53	45	GPIO_ENH	LCD_SEG_7	LCD_COM_7	SCB0_SEL0 (0)				
P14.4	54	46	GPIO_ENH	LCD_SEG_8	LCD_COM_8	SCB0_SEL1 (0)				
P14.5	55	47	GPIO_ENH	LCD_SEG_9	LCD_COM_9	SCB0_SEL2 (0)				
P14.6	56	NA	GPIO_ENH	LCD_SEG_10	LCD_COM_10	SCB0_SEL3 (0)				
P14.7	57	NA	GPIO_ENH	LCD_SEG_11	LCD_COM_11					
P15.0	58	48	GPIO_STD	LCD_SEG_12	LCD_COM_12					
P15.1	59	49	GPIO_STD	LCD_SEG_13	LCD_COM_13					
P15.2	60	50	GPIO_STD	LCD_SEG_14	LCD_COM_14					
P15.3	61	51	GPIO_STD	LCD_SEG_15	LCD_COM_15					
P15.4	62	52	GPIO_STD	LCD_SEG_16	LCD_COM_16					
P15.5	63	53	GPIO_STD	LCD_SEG_17	LCD_COM_17					
P15.6	64	NA	GPIO_STD	LCD_SEG_18	LCD_COM_18					
P15.7	65	NA	GPIO_STD	LCD_SEG_19	LCD_COM_19					
P16.0	68	56	GPIO_STD	LCD_SEG_20	LCD_COM_20					
P16.1	69	57	GPIO_STD	LCD_SEG_21	LCD_COM_21					
P16.2	70	58	GPIO_STD	LCD_SEG_22	LCD_COM_22					
P16.3	71	59	GPIO_STD	LCD_SEG_23	LCD_COM_23					

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O *(continued)*[23]

Name	Package		I/O Type	DeepSleep Mapping					Analog/HV	Smart I/O
	176-LQFP	144-LQFP	HCon#0	HCon#12[18]	HCon#13	HCon#14	HCon#15	HCon#29		
	Pin	Pin		DS#0[19, 20]	DS#1	DS#2	DS#3	DS#5		
P16.4	72	60	GPIO_STD	LCD_SEG_24	LCD_COM_24					
P16.5	73	NA	GPIO_STD	LCD_SEG_25	LCD_COM_25					
P17.0	74	61	GPIO_STD	LCD_SEG_26	LCD_COM_26					
P17.1	75	62	GPIO_STD	LCD_SEG_27	LCD_COM_27					
P17.2	76	63	GPIO_STD	LCD_SEG_28	LCD_COM_28					
P17.3	77	64	GPIO_STD	LCD_SEG_29	LCD_COM_29					
P17.4	78	65	GPIO_STD	LCD_SEG_30	LCD_COM_30					
P17.5	79	66	GPIO_STD	LCD_SEG_31	LCD_COM_31					
P17.6	80	NA	GPIO_STD	LCD_SEG_32	LCD_COM_32					
P17.7	81	NA	GPIO_STD	LCD_SEG_33	LCD_COM_33					
P18.0	82	67	GPIO_STD	LCD_SEG_34	LCD_COM_34					
P18.1	83	68	GPIO_STD	LCD_SEG_35	LCD_COM_35					
P18.2	84	69	GPIO_STD	LCD_SEG_21	LCD_COM_21					
P18.3	85	70	GPIO_STD	LCD_SEG_22	LCD_COM_22				HIBERNATE_WAKEUP[3]	
P18.4	86	71	GPIO_STD	LCD_SEG_23	LCD_COM_23					
P18.5	87	NA	GPIO_STD	LCD_SEG_24	LCD_COM_24					
P18.6[22]	90	NA	GPIO_STD							
P18.7	91	NA	GPIO_STD	LCD_SEG_27	LCD_COM_27					
P19.0	92	74	GPIO_STD	LCD_SEG_25	LCD_COM_25					
P19.1	93	75	GPIO_STD	LCD_SEG_28	LCD_COM_28					
P19.2	94	76	GPIO_STD	LCD_SEG_29	LCD_COM_29					
P19.3	95	77	GPIO_STD	LCD_SEG_32	LCD_COM_32					
P19.4	96	78	GPIO_STD	LCD_SEG_33	LCD_COM_33					
P19.5	97	NA	GPIO_STD	LCD_SEG_30	LCD_COM_30					
P19.6	98	NA	GPIO_STD	LCD_SEG_31	LCD_COM_31					
XRES_L	108	88								

12 Power pin assignments

Table 12-1 Power pin assignments

Name	Package		Remarks
	176-LQFP	144-LQFP	
VDDD	105, 104, 88, 66, 45, 20	85, 84, 72, 54, 37, 20	Main digital supply
VSS	133, 107, 99, 89, 67, 44, 22	109, 87, 79, 73, 55, 36, 22	Main digital ground
VDDIO_GPIO	132	108	Supply for GPIO_STD (2.7 - 5.5 V)
VDDIO_HSIO	176, 18, 13, 7	144, 18, 13, 7	Supply for HSIO_STDLN (3.0 - 3.6 V)
VSSIO_HSIO	19, 12, 6, 1	19, 12, 6, 1	HSIO_STDLN ground
VDDIO_SMC	174, 164, 155, 145	142, 132, 123, 113	Supply for GPIO_SMC (2.7 - 5.5 V)
VSSIO_SMC	175, 165, 154, 144	143, 133, 122, 112	GPIO_SMC ground
VCCD[24]	106, 21	86, 21	Main regulated supply. Driven by LDO regulator
VREFH	129	105	High reference voltage for SAR
VDDA_ADC	130	106	Main analog supply (for PASS/SAR)
VSSA_ADC	131	107	Main analog ground (VREFL is shared with VSSA_ADC)

Note
24.The V_{CCD} pins must be connected together to ensure a low-impedance connection. (see the requirement in **Figure 27-2**)

13 Alternate function pin assignments

Table 13-1 Alternate pin functions in active power mode [20, 27, 28]

Name	Active Mapping														
	HCon#8[25]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[26]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P0.0															
P0.1															
P0.2														EXT_CLK	
P0.3															
P1.0	PWM0_H_0	PWM0_H_15_N	TC0_H_14_TR							SCB7_CLK (0)	SCB7_RX (0)	SCB7_SDA (0)[29]			FAULT_OUT_0
P1.1	PWM0_H_1	PWM0_H_0_N	TC0_H_15_TR							SCB7_MOSI (0)	SCB7_TX (0)	SCB7_SCL (0)[29]			FAULT_OUT_1
P1.2	PWM0_H_2	PWM0_H_1_N	TC0_H_0_TR							SCB7_MISO (0)	SCB7_RTS (0)				FAULT_OUT_2
P1.3	PWM0_H_3	PWM0_H_2_N	TC0_H_1_TR							SCB7_SEL0 (0)	SCB7_CTS (0)				FAULT_OUT_3
P1.4	PWM0_H_4	PWM0_H_3_N	TC0_H_2_TR							SCB7_SEL1 (0)					
P1.5	PWM0_H_5	PWM0_H_4_N	TC0_H_3_TR												
P1.6	PWM0_H_6	PWM0_H_5_N	TC0_H_4_TR												
P1.7	PWM0_H_7	PWM0_H_6_N	TC0_H_5_TR												
P2.0	PWM0_H_8	PWM0_H_7_N	TC0_H_6_TR							SCB8_CLK (0)	SCB8_RX (0)	SCB8_SDA (0)[29]			
P2.1	PWM0_H_9	PWM0_H_8_N	TC0_H_7_TR							SCB8_MOSI (0)	SCB8_TX (0)	SCB8_SCL (0)[29]			
P2.2	PWM0_H_10	PWM0_H_9_N	TC0_H_8_TR		LIN0_TX	CXPI0_TX	CAN0_0_TX			SCB8_MISO (0)	SCB8_RTS (0)		TRIG_DBG[1]		
P2.3	PWM0_H_11	PWM0_H_10_N	TC0_H_9_TR		LIN0_RX	CXPI0_RX	CAN0_0_RX			SCB8_SEL0 (0)	SCB8_CTS (0)		TRIG_IN[1]		
P2.4	PWM0_H_12	PWM0_H_11_N	TC0_H_10_TR		LIN0_EN	CXPI0_EN	CAN0_1_TX			SCB8_SEL1 (0)			TRIG_IN[2]		
P2.5	PWM0_H_13	PWM0_H_12_N	TC0_H_11_TR				CAN0_1_RX						TRIG_DBG[0]		CAL_SUP_NZ
P2.6	PWM0_H_14	PWM0_H_13_N	TC0_H_12_TR		LIN1_RX	CXPI1_RX							TRIG_IN[0]		
P2.7	PWM0_H_15	PWM0_H_14_N	TC0_H_13_TR	EXT_MUX[0]_0	LIN1_TX	CXPI1_TX							TRIG_IN[3]		
P3.0	PWM0_24	PWM0_33_N	TC0_32_TR	EXT_MUX[0]_1	LIN1_EN	CXPI1_EN				SCB8_CLK (1)	SCB8_RX (1)	SCB8_SDA (1)[29]			
P3.1	PWM0_25	PWM0_24_N	TC0_33_TR	EXT_MUX[0]_2						SCB8_MOSI (1)	SCB8_TX (1)	SCB8_SCL (1)[29]			
P3.2	PWM0_26	PWM0_25_N	TC0_24_TR	EXT_MUX[0]_EN						SCB8_MISO (1)	SCB8_RTS (1)		TRIG_IN[4]		
P3.3	PWM0_27	PWM0_26_N	TC0_25_TR							SCB8_SEL0 (1)	SCB8_CTS (1)		TRIG_IN[5]		

Notes
25.High Speed I/O matrix connection (HCon) reference as per **Table 10-1**.
26.Active Mode ordering (ACT#0, ACT#1, and so on) does not have any impact on choosing any alternate functions; HSIOM module will handle the individual alternate function assignmen
27.Refer to **Table 14-1** for more information on pin multiplexer abbreviations used.
28.For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group “n”.
29.See **Table 27-10** 'Serial Communication Block (SCB) specifications' for supported IO-cells and I2C modes.

Table 13-1 Alternate pin functions in active power mode *(continued)* [20, 27, 28]

Name	Active Mapping															
	HCon#8[25]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[26]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P3.4	PWM0_28	PWM0_27_N	TC0_26_TR												
P3.5	PWM0_29	PWM0_28_N	TC0_27_TR												
P4.0	PWM0_30	PWM0_29_N	TC0_28_TR				CAN1_0_TX								
P4.1	PWM0_31	PWM0_30_N	TC0_29_TR				CAN1_0_RX								
P4.2	PWM0_32	PWM0_31_N	TC0_30_TR				CAN1_1_TX								
P4.3	PWM0_33	PWM0_32_N	TC0_31_TR				CAN1_1_RX								
P4.4	PWM0_0	PWM0_3_N			LIN1_TX	CXPI1_EN							TRIG_IN[6]		
P4.5	PWM0_1	PWM0_0_N			LIN1_RX	CXPI1_RX							TRIG_IN[7]		
P4.6	PWM0_2	PWM0_1_N			LIN1_EN	CXPI1_TX							TRIG_IN[8]		
P4.7	PWM0_3	PWM0_2_N											TRIG_IN[9]		
P5.0	PWM0_M_0	PWM0_H_15_N		EXT_MUX[1]_0						SCB9_CLK (0)	SCB9_RX (0)	SCB9_SDA (0)[29]			
P5.1	PWM0_H_10	PWM0_M_0_N	TC0_H_15_TR	EXT_MUX[1]_1						SCB9_MOSI (0)	SCB9_TX (0)	SCB9_SCL (0)[29]			
P5.2	PWM0_M_1	PWM0_H_10_N		EXT_MUX[1]_2						SCB9_MISO (0)	SCB9_RTS (0)				
P5.3	PWM0_H_11	PWM0_M_1_N	TC0_H_10_TR	EXT_MUX[1]_EN						SCB9_SEL0 (0)	SCB9_CTS (0)				
P5.4	PWM0_M_2	PWM0_H_11_N								SCB9_SEL1 (0)			TRIG_IN[10]		
P5.5	PWM0_H_12	PWM0_M_2_N	TC0_H_11_TR										TRIG_IN[11]		
P5.6	PWM0_M_3	PWM0_H_12_N											TRIG_IN[12]		
P5.7	PWM0_H_13	PWM0_M_3_N	TC0_H_12_TR										TRIG_IN[13]		
P6.0	PWM0_M_4	PWM0_H_13_N													
P6.1	PWM0_H_14	PWM0_M_4_N	TC0_H_13_TR						SG_TONE[0] (2)						
P6.2	PWM0_M_5	PWM0_H_14_N							SG_AMPL[0] (2)						
P6.3	PWM0_H_15	PWM0_M_5_N	TC0_H_14_TR						SG_TONE[1] (2)						
P6.4	PWM0_M_6	PWM0_5_N							SG_AMPL[1] (2)				TRIG_IN[14]		
P6.5	PWM0_0	PWM0_M_6_N							SG_TONE[2] (2)				TRIG_IN[15]		
P6.6	PWM0_M_7	PWM0_0_N							SG_AMPL[2] (2)				TRIG_IN[16]		
P6.7	PWM0_1	PWM0_M_7_N							SG_TONE[3] (2)				TRIG_IN[17]		
P7.0	PWM0_M_8	PWM0_1_N							SG_AMPL[3] (2)						
P7.1	PWM0_2	PWM0_M_8_N							SG_AMPL[4] (2)						
P7.2	PWM0_M_9	PWM0_2_N							SG_TONE[4] (2)						
P7.3	PWM0_3	PWM0_M_9_N							SG_MCK[0] (2)						
P7.4	PWM0_M_10	PWM0_3_N							SG_MCK[1] (2)						

Table 13-1 Alternate pin functions in active power mode *(continued)* [20, 27, 28]

Name	Active Mapping														
	HCon#8[25]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[26]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P7.5	PWM0_4	PWM0_M_10_N							SG_MCK[2] (2)						
P7.6	PWM0_M_11	PWM0_4_N							SG_MCK[3] (2)						
P7.7	PWM0_5	PWM0_M_11_N							SG_MCK[4] (2)						
P8.0										SCB10_CLK (0)	SCB10_RX (0)	SCB10_SDA (0)[29]		IO_CLK_HF[2]	SPIHB_SELECT1
P8.1										SCB10_MOSI (0)	SCB10_TX (0)	SCB10_SCL (0)[29]			SPIHB_SELECT0
P8.2										SCB10_MISO (0)	SCB10_RTS (0)				SPIHB_DATA7
P8.3										SCB10_SEL0 (0)	SCB10_CTS (0)				SPIHB_DATA6
P8.4										SCB10_SEL1 (0)					SPIHB_DATA5
P8.5														EXT_CLK	SPIHB_DATA4
P8.6										SCB11_CLK (0)	SCB11_RX (0)	SCB11_SDA (0)[29]			SPIHB_DATA3
P8.7										SCB11_MOSI (0)	SCB11_TX (0)	SCB11_SCL (0)[29]		TRACE_DATA_3	SPIHB_DATA2
P9.0										SCB11_MISO (0)	SCB11_RTS (0)			TRACE_DATA_2	SPIHB_DATA1
P9.1										SCB11_SEL0 (0)	SCB11_CTS (0)			TRACE_DATA_1	SPIHB_DATA0
P9.2										SCB11_SEL1 (0)				TRACE_DATA_0	SPIHB_CLK
P9.3														TRACE_CLOCK	SPIHB_RWDS
P10.0	PWM0_4	PWM0_3_N							SG_TONE[0] (1)	SCB2_CLK (1)	SCB2_RX (1)	SCB2_SDA (1)[29]			
P10.1	PWM0_5	PWM0_4_N							SG_AMPL[0] (1)	SCB2_MOSI (1)	SCB2_TX (1)	SCB2_SCL (1)[29]			
P10.2	PWM0_6	PWM0_5_N							SG_MCK[0] (1)	SCB2_MISO (1)	SCB2_RTS (1)				
P10.3	PWM0_7	PWM0_6_N							SG_TONE[1] (1)	SCB2_SEL0 (1)	SCB2_CTS (1)				
P10.4	PWM0_8	PWM0_7_N							SG_AMPL[1] (1)						
P11.0	PWM0_9	PWM0_8_N							SG_MCK[1] (1)	SCB1_CLK (0)	SCB1_RX (0)	SCB1_SDA (0)[29]			
P11.1	PWM0_10	PWM0_9_N								SCB1_MOSI (0)	SCB1_TX (0)	SCB1_SCL (0)[29]			
P11.2	PWM0_H_0	PWM0_10_N			TDM_TX_MCK[0] (0)	TDM_RX_MCK[1] (0)				SCB1_MISO (0)	SCB1_RTS (0)				
P11.3	PWM0_H_1	PWM0_H_0_N			TDM_TX_SCK[0] (0)	TDM_RX_SCK[1] (0)				SCB1_SEL0 (0)	SCB1_CTS (0)				
P11.4	PWM0_H_2	PWM0_H_1_N	TC0_H_0_TR		TDM_TX_FSYNC[0] (0)	TDM_RX_FSYNC[1] (0)				SCB1_SEL1 (0)					
P11.5	PWM0_11	PWM0_H_2_N	TC0_H_1_TR		TDM_TX_SD[0] (0)	TDM_RX_SD[1] (0)			SG_TONE[2] (1)						
P11.6	PWM0_6	PWM0_11_N							SG_AMPL[2] (1)						

Table 13-1 Alternate pin functions in active power mode *(continued)* [20, 27, 28]

Name	Active Mapping														
	HCon#8[25]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[26]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P11.7	PWM0_7	PWM0_6_N							SG_MCK[2] (1)				TRIG_IN[18]		
P12.0	PWM0_8	PWM0_7_N	TC0_H_2_TR						SG_TONE[0] (0)	SCB2_CLK (0)	SCB2_RX (0)	SCB2_SDA (0)[29]			
P12.1	PWM0_9	PWM0_8_N							SG_AMPL[0] (0)	SCB2_MOSI (0)	SCB2_TX (0)	SCB2_SCL (0)[29]			
P12.2	PWM0_10	PWM0_9_N							SG_MCK[0] (0)	SCB2_MISO (0)	SCB2_RTS (0)				
P12.3	PWM0_11	PWM0_10_N			TDM_TX_MCK[1] (0)	TDM_RX_MCK[0] (0)				SCB2_SEL0 (0)	SCB2_CTS (0)				
P12.4	PWM0_0	PWM0_11_N			TDM_TX_SCK[1] (0)	TDM_RX_SCK[0] (0)				SCB2_SEL1 (0)					
P12.5	PWM0_1	PWM0_0_N			TDM_TX_FSYNC[1] (0)	TDM_RX_FSYNC[0] (0)									
P12.6	PWM0_2	PWM0_1_N			TDM_TX_SD[1] (0)	TDM_RX_SD[0] (0)									
P12.7	PWM0_3	PWM0_2_N											TRIG_IN[19]		
P13.0	PWM0_4	PWM0_18_N	TC0_25_TR		TDM_TX_MCK[0] (1)	TDM_RX_MCK[1] (1)		PWM_LINE1_P[0] (1)		SCB4_CLK (1)	SCB4_RX (1)	SCB4_SDA (1)[29]	TRIG_IN[20]		
P13.1	PWM0_5	PWM0_4_N	TC0_26_TR		TDM_TX_SCK[0] (1)	TDM_RX_SCK[1] (1)		PWM_LINE1_N[0] (1)		SCB4_MOSI (1)	SCB4_TX (1)	SCB4_SCL (1)[29]	TRIG_IN[21]		
P13.2	PWM0_6	PWM0_5_N	TC0_27_TR		TDM_TX_FSYNC[0] (1)	TDM_RX_FSYNC[1] (1)		PWM_LINE2_P[0] (1)		SCB4_MISO (1)	SCB4_RTS (1)				
P13.3	PWM0_7	PWM0_6_N	TC0_28_TR		TDM_TX_SD[0] (1)	TDM_RX_SD[1] (1)		PWM_LINE2_N[0] (1)		SCB4_SEL0 (1)	SCB4_CTS (1)				
P14.0	PWM0_H_3	PWM0_7_N							SG_TONE[1] (0)		SCB0_RX (0)				
P14.1	PWM0_H_4	PWM0_H_3_N							SG_AMPL[1] (0)		SCB0_TX (0)				
P14.2	PWM0_H_5	PWM0_H_4_N	TC0_H_3_TR						SG_MCK[1] (0)		SCB0_RTS (0)	SCB1_SDA (1)			
P14.3	PWM0_8	PWM0_H_5_N	TC0_H_4_TR						SG_TONE[2] (0)		SCB0_CTS (0)	SCB1_SCL (1)			
P14.4	PWM0_9	PWM0_8_N	TC0_H_5_TR					PWM_MCK[0] (1)	SG_AMPL[2] (0)			SCB10_SDA (1)			
P14.5	PWM0_10	PWM0_9_N	TC0_29_TR					PWM_MCK[1] (1)	SG_MCK[2] (0)			SCB10_SCL (1)			
P14.6	PWM0_11	PWM0_10_N	TC0_30_TR						SG_TONE[3] (1)			SCB11_SDA (1)			
P14.7	PWM0_12	PWM0_11_N							SG_AMPL[3] (1)			SCB11_SCL (1)			
P15.0	PWM0_13	PWM0_12_N			TDM_TX_MCK[1] (1)	TDM_RX_MCK[0] (1)		PWM_LINE1_P[1] (1)	SG_MCK[3] (1)	SCB3_CLK (0)	SCB3_RX (0)	SCB3_SDA (0)[29]			
P15.1	PWM0_H_6	PWM0_13_N			TDM_TX_SCK[1] (1)	TDM_RX_SCK[0] (1)		PWM_LINE1_N[1] (1)		SCB3_MOSI (0)	SCB3_TX (0)	SCB3_SCL (0)[29]			
P15.2	PWM0_H_7	PWM0_H_6_N			TDM_TX_FSYNC[1] (1)	TDM_RX_FSYNC[0] (1)		PWM_LINE2_P[1] (1)		SCB3_MISO (0)	SCB3_RTS (0)				
P15.3	PWM0_14	PWM0_H_7_N	TC0_H_6_TR		TDM_TX_SD[1] (1)	TDM_RX_SD[0] (1)		PWM_LINE2_N[1] (1)		SCB3_SEL0 (0)	SCB3_CTS (0)				
P15.4	PWM0_15	PWM0_14_N	TC0_H_7_TR							SCB3_SEL1 (0)			TRIG_IN[22]		
P15.5	PWM0_16	PWM0_15_N							SG_TONE[4] (1)				TRIG_IN[23]		

Table 13-1 Alternate pin functions in active power mode *(continued)* [20, 27, 28]

Name	Active Mapping															
	HCon#8[25]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[26]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P15.6	PWM0_17	PWM0_16_N							SG_AMPL[4] (1)				TRIG_IN[24]		
P15.7	PWM0_18	PWM0_17_N							SG_MCK[4] (1)				TRIG_IN[25]		
P16.0	PWM0_19	PWM0_33_N						PWM_LINE1_P[0] (0)		SCB4_CLK (0)	SCB4_RX (0)	SCB4_SDA (0)[29]			
P16.1	PWM0_H_8	PWM0_19_N						PWM_LINE1_N[0] (0)		SCB4_MOSI (0)	SCB4_TX (0)	SCB4_SCL (0)[29]			
P16.2	PWM0_H_9	PWM0_H_8_N						PWM_LINE2_P[0] (0)		SCB4_MISO (0)	SCB4_RTS (0)				
P16.3	PWM0_20	PWM0_H_9_N	TC0_H_8_TR					PWM_LINE2_N[0] (0)		SCB4_SEL0 (0)	SCB4_CTS (0)				
P16.4	PWM0_21	PWM0_20_N	TC0_H_9_TR					PWM_MCK[0] (0)	SG_MCK[3] (0)	SCB4_SEL1 (0)					
P16.5	PWM0_22	PWM0_21_N							SG_MCK[4] (0)						
P17.0	PWM0_23	PWM0_22_N						PWM_LINE1_P[1] (0)		SCB5_CLK (0)	SCB5_RX (0)	SCB5_SDA (0)[29]			
P17.1	PWM0_24	PWM0_23_N	TC0_20_TR					PWM_LINE1_N[1] (0)		SCB5_MOSI (0)	SCB5_TX (0)	SCB5_SCL (0)[29]			
P17.2	PWM0_25	PWM0_24_N	TC0_21_TR					PWM_LINE2_P[1] (0)		SCB5_MISO (0)	SCB5_RTS (0)				
P17.3	PWM0_26	PWM0_25_N	TC0_22_TR					PWM_LINE2_N[1] (0)		SCB5_SEL0 (0)	SCB5_CTS (0)		TRIG_IN[26]		
P17.4	PWM0_27	PWM0_26_N	TC0_23_TR					PWM_MCK[1] (0)	SG_TONE[3] (0)	SCB5_SEL1 (0)			TRIG_IN[27]		
P17.5	PWM0_28	PWM0_27_N	TC0_24_TR						SG_AMPL[3] (0)						
P17.6	PWM0_29	PWM0_28_N							SG_TONE[4] (0)						
P17.7	PWM0_30	PWM0_29_N							SG_AMPL[4] (0)						
P18.0	PWM0_31	PWM0_30_N					CAN0_1_TX			SCB6_CLK (0)	SCB6_RX (0)	SCB6_SDA (0)[29]			
P18.1	PWM0_32	PWM0_31_N					CAN0_1_RX			SCB6_MOSI (0)	SCB6_TX (0)	SCB6_SCL (0)[29]			
P18.2	PWM0_33	PWM0_32_N			LIN1_TX	CXPI1_TX	CAN0_0_TX			SCB6_MISO (0)	SCB6_RTS (0)				
P18.3	PWM0_12	PWM0_23_N	TC0_20_TR		LIN1_RX	CXPI1_RX	CAN0_0_RX			SCB6_SEL0 (0)	SCB6_CTS (0)				
P18.4	PWM0_13	PWM0_12_N	TC0_21_TR		LIN1_EN	CXPI1_EN				SCB6_SEL1 (0)			TRIG_IN[28]		
P18.5	PWM0_14	PWM0_13_N											TRIG_IN[29]		
P18.6	PWM0_15	PWM0_14_N	TC0_22_TR										TRIG_IN[30]		
P18.7	PWM0_16	PWM0_15_N	TC0_23_TR										TRIG_IN[31]		
P19.0	PWM0_17	PWM0_16_N			LIN0_TX	CXPI0_TX	CAN1_1_TX			SCB6_CLK (1)	SCB6_RX (1)	SCB6_SDA (1)[29]			FAULT_OUT_0
P19.1	PWM0_18	PWM0_17_N			LIN0_RX	CXPI0_RX	CAN1_1_RX			SCB6_MOSI (1)	SCB6_TX (1)	SCB6_SCL (1)[29]			FAULT_OUT_1
P19.2	PWM0_19	PWM0_18_N	TC0_31_TR		LIN0_EN	CXPI0_EN	CAN1_0_TX			SCB6_MISO (1)	SCB6_RTS (1)				FAULT_OUT_2
P19.3	PWM0_20	PWM0_19_N	TC0_32_TR				CAN1_0_RX			SCB6_SEL0 (1)	SCB6_CTS (1)				FAULT_OUT_3

Table 13-1 Alternate pin functions in active power mode *(continued)* [20, 27, 28]

Name	Active Mapping														
	HCon#8[25]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[26]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P19.4	PWM0_21	PWM0_20_N	TC0_33_TR							SCB6_SEL1 (1)					
P19.5	PWM0_22	PWM0_21_N													
P19.6	PWM0_23	PWM0_22_N													

14 Pin function description

Table 14-1 Pin function description

Sl. No.	Pin	Module	Description
1	PWMx_y	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
2	PWMx_y_N	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
3	PWMx_M_y	TCPWM	TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number
4	PWMx_M_y_N	TCPWM	TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number
5	PWMx_H_y	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
6	PWMx_H_y_N	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
7	TCx_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
8	TCx_M_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number
9	TCx_H_y_TRz	TCPWM	TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
10	SCBx_RX	SCB	UART Receive, x-SCB block
11	SCBx_TX	SCB	UART Transmit, x-SCB block
12	SCBx_RTS	SCB	UART Request to Send (Handshake), x-SCB block
13	SCBx_CTS	SCB	UART Clear to Send (Handshake), x-SCB block
14	SCBx_SDA	SCB	I^2C Data line, x-SCB block
15	SCBx_SCL	SCB	I^2C Clock line, x-SCB block
16	SCBx_MISO	SCB	SPI Master Input Slave Output, x-SCB block
17	SCBx_MOSI	SCB	SPI Master Output Slave Input, x-SCB block
18	SCBx_CLK	SCB	SPI Serial Clock, x-SCB block
19	SCBx_SELy	SCB	SPI Slave Select, x-SCB block, y-select line
20	LINx_RX	LIN	LIN Receive line, x-LIN block
21	LINx_TX	LIN	LIN Transmit line, x-LIN block
22	LINx_EN	LIN	LIN Enable line, x-LIN block
23	CXPIx_RX	CXPI	CXPI Receive line, x-CXPI block
24	CXPIx_TX	CXPI	CXPI Transmit line, x-CXPI block
25	CXPIx_EN	CXPI	CXPI Enable line, x-CXPI block
26	CANx_y_TX	CAN FD	CAN Transmit line, x-CAN block, y-channel number
27	CANx_y_RX	CAN FD	CAN Receive line, x-CAN block, y-channel number
28	CAL_SUP_NZ	CPUSS	ETAS Calibration support line
29	FAULT_OUT_x	SRSS	Fault output line x-0 to 3
30	TRACE_DATA_x	SRSS	Trace dataout line x-0 to 3
31	TRACE_CLOCK	SRSS	Trace clock line
32	RTC_CAL	SRSS RTC	RTC calibration clock input

Table 14-1 Pin function description *(continued)*

Sl. No.	Pin	Module	Description
33	SWJ_TRSTN	SRSS	JTAG Test reset line (Active low)
34	SWJ_SWO_TDO	SRSS	JTAG Test data output/SWO (Serial Wire Output)
35	SWJ_SWCLK_TCLK	SRSS	JTAG Test clock/SWD clock (Serial Wire Clock)
36	SWJ_SWDIO_TMS	SRSS	JTAG Test mode select/SWD data (Serial Wire Data Input/Output)
37	SWJ_SWDOE_TDI	SRSS	JTAG Test data input
38	HIBERNATE_WAKEUP[x]	SRSS	Hibernate wakeup line x-0 to N (Check **Table 11-1**)
39	ADC[x]_y	PASS SAR	SAR, channel, x-SAR number, y-channel number
40	ADC[x]_M	PASS SAR	SAR motor control input, x-SAR number
41	EXT_MUX[x]_y	PASS SAR	External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2
42	EXT_MUX[x]_EN	PASS SAR	External SAR MUX enable line
43	EXT_CLK	SRSS	External clock input or output
44	SG_AMPL[x]	SG	Sound generator (SG) amplitude output, x-SG module number
45	SG_MCK[x]	SG	Sound generator (SG) master clock input, x-SG module number
46	SG_TONE[x]	SG	Sound generator (SG) tone output, x-SG module number
47	PWM_LINEx_N[y]	PCM PWM	Audio PWM complementary output line, x-PWM module instance
48	PWM_LINEx_P[y]	PCM PWM	Audio PWM output line, x-PWM module instance
49	PWM_MCK[x]	PCM PWM	Audio PWM master clock input, x-PWM module instance
50	TDM_RX_FSYNC[x]	TDM	TDM receive frame sync, x-TDM module number
51	TDM_RX_MCK[x]	TDM	TDM receive master clock input, x-TDM module number
52	TDM_RX_SCK[x]	TDM	TDM receive bit clock, x-TDM module number
53	TDM_RX_SD[x]	TDM	TDM receive serial data, x-TDM module number
54	TDM_TX_FSYNC[x]	TDM	TDM transmit frame sync, x-TDM module number
55	TDM_TX_MCK[x]	TDM	TDM transmit master clock input, x-TDM module number
56	TDM_TX_SCK[x]	TDM	TDM transmit bit clock, x-TDM module number
57	TDM_TX_SD[x]	TDM	TDM transmit serial data, x-TDM module number
58	SPIHB_CLK	SMIF	SMIF interface clock
59	SPIHB_RWDS	SMIF	SMIF (SPI/xSPI) read-write-data-strobe line
60	SPIHB_SELx	SMIF	SMIF (SPI/xSPI) memory select line, x-select line number
61	SPIHB_DATAx	SMIF	SMIF (SPI/xSPI) memory data read and write line, x-0 to 7 data lines
62	LCD_SEG_x	LCD	LCD segment lines x-0 to 35
63	LCD_COM_x	LCD	LCD common lines x-0 to 35
64	IO_CLK_HF[2]	SRSS	CLK_HF2 clock output
65	TRIG_IN[x]	HSIOM	HSIOM_IO_INPUT[x] of trigger inputs, x-0 to 31
66	TRIG_DBG[x]	HSIOM	HSIOM_IO_OUTPUT[x] of trigger outputs, x-0 to 1
67	WCO_IN	SRSS	Watch crystal oscillator input
68	WCO_OUT	SRSS	Watch crystal oscillator output
69	ECO_IN	SRSS	External crystal oscillator input
70	ECO_OUT	SRSS	External crystal oscillator output

15 Interrupts and wake-up assignments

Table 15-1 Peripheral interrupt assignments and wake-up sources

Interrupt	Source	Power Mode	Description
0	cpuss_interrupts_ipc_0_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #0
1	cpuss_interrupts_ipc_1_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #1
2	cpuss_interrupts_ipc_2_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #2
3	cpuss_interrupts_ipc_3_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #3
4	cpuss_interrupts_ipc_4_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #4
5	cpuss_interrupts_ipc_5_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #5
6	cpuss_interrupts_ipc_6_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #6
7	cpuss_interrupts_ipc_7_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #7
8	cpuss_interrupts_fault_0_IRQn	DeepSleep	CPUSS Fault Structure #0 Interrupt
9	cpuss_interrupts_fault_1_IRQn	DeepSleep	CPUSS Fault Structure #1 Interrupt
10	cpuss_interrupts_fault_2_IRQn	DeepSleep	CPUSS Fault Structure #2 Interrupt
11	cpuss_interrupts_fault_3_IRQn	DeepSleep	CPUSS Fault Structure #3 Interrupt
12	srss_interrupt_backup_IRQn	DeepSleep	BACKUP domain Interrupt
13	srss_interrupt_mcwdt_0_IRQn	DeepSleep	Multi Counter Watchdog Timer #0 interrupt
14	srss_interrupt_mcwdt_1_IRQn	DeepSleep	Multi Counter Watchdog Timer #1 interrupt
17	srss_interrupt_wdt_IRQn	DeepSleep	Hardware Watchdog Timer interrupt
18	srss_interrupt_IRQn	DeepSleep	Other combined Interrupts for SRSS (LVD, CLK_CAL)
19	evtgen_0_interrupt_dpslp_IRQn	DeepSleep	Event generator timer DeepSleep domain interrupt
20	scb_0_interrupt_IRQn	DeepSleep	Serial Communication Block#0 (DeepSleep capable)
22	ioss_interrupt_vdd_IRQn	DeepSleep	I/O Supply (V_{DDIO}, V_{DDA_ADC}, V_{DDD}) state change Interrupt
23	ioss_interrupt_gpio_dpslp_IRQn	DeepSleep	Consolidated interrupt for DeepSleep ports
24	ioss_interrupts_gpio_0_IRQn	DeepSleep	GPIO_STD Port #0 Interrupt
25	ioss_interrupts_gpio_1_IRQn	DeepSleep	GPIO_STD Port #1 Interrupt
26	ioss_interrupts_gpio_2_IRQn	DeepSleep	GPIO_STD Port #2 Interrupt
27	ioss_interrupts_gpio_3_IRQn	DeepSleep	GPIO_STD Port #3 Interrupt
28	ioss_interrupts_gpio_4_IRQn	DeepSleep	GPIO_STD Port #4 Interrupt
29	ioss_interrupts_gpio_5_IRQn	DeepSleep	GPIO_SMC Port #5 Interrupt
30	ioss_interrupts_gpio_6_IRQn	DeepSleep	GPIO_SMC Port #6 Interrupt
31	ioss_interrupts_gpio_7_IRQn	DeepSleep	GPIO_SMC Port #7 Interrupt
34	ioss_interrupts_gpio_10_IRQn	DeepSleep	GPIO_STD Port #10 Interrupt
35	ioss_interrupts_gpio_11_IRQn	DeepSleep	GPIO_STD Port #11 Interrupt
36	ioss_interrupts_gpio_12_IRQn	DeepSleep	GPIO_STD Port #12 Interrupt
37	ioss_interrupts_gpio_13_IRQn	DeepSleep	GPIO_STD Port #13 Interrupt
38	ioss_interrupts_gpio_14_IRQn	DeepSleep	GPIO_ENH Port #14 Interrupt
39	ioss_interrupts_gpio_15_IRQn	DeepSleep	GPIO_STD Port #15 Interrupt
40	ioss_interrupts_gpio_16_IRQn	DeepSleep	GPIO_STD Port #16 Interrupt
41	ioss_interrupts_gpio_17_IRQn	DeepSleep	GPIO_STD Port #17 Interrupt
42	ioss_interrupts_gpio_18_IRQn	DeepSleep	GPIO_STD Port #18 Interrupt
43	ioss_interrupts_gpio_19_IRQn	DeepSleep	GPIO_STD Port #19 Interrupt
50	ioss_interrupt_gpio_act_IRQn	Active	Consolidated interrupt for active I/O ports
52	ioss_interrupts_gpio_8_IRQn	Active	HSIO_STDLN Port #8 Interrupt
53	ioss_interrupts_gpio_9_IRQn	Active	HSIO_STDLN Port #9 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
70	cpuss_interrupt_crypto_IRQn	Active	Crypto Accelerator Interrupt
71	cpuss_interrupt_fm_IRQn	Active	FLASH Macro Interrupt
72	cpuss_interrupts_cm4_fp_IRQn	Active	CM4 Floating Point operation fault
74	cpuss_interrupts_cm0_cti_0_IRQn	Active	CM0+ CTI (Cross Trigger Interface) #0
75	cpuss_interrupts_cm0_cti_1_IRQn	Active	CM0+ CTI#1
76	cpuss_interrupts_cm4_cti_0_IRQn	Active	CM4 CTI#0
77	cpuss_interrupts_cm4_cti_1_IRQn	Active	CM4 CTI#1
80	evtgen_0_interrupt_IRQn	Active	Event Generator Active domain interrupt
81	smif_0_interrupt_IRQn	Active	SMIF#0 Interrupt
86	canfd_0_interrupt0_IRQn	Active	CAN#0, Consolidated Interrupt #0 for all three channels
87	canfd_0_interrupt1_IRQn	Active	CAN#0, Consolidated Interrupt #1 for all three channels
88	canfd_1_interrupt0_IRQn	Active	CAN#1, Consolidated Interrupt #0 for all three channels
89	canfd_1_interrupt1_IRQn	Active	CAN#1, Consolidated Interrupt #1 for all three channels
90	canfd_0_interrupts0_0_IRQn	Active	CAN#0, Interrupt #0, Channel #0
91	canfd_0_interrupts0_1_IRQn	Active	CAN#0, Interrupt #0, Channel #1
96	canfd_0_interrupts1_0_IRQn	Active	CAN#0, Interrupt #1, Channel #0
97	canfd_0_interrupts1_1_IRQn	Active	CAN#0, Interrupt #1, Channel #1
102	canfd_1_interrupts0_0_IRQn	Active	CAN#1, Interrupt #0, Channel #0
103	canfd_1_interrupts0_1_IRQn	Active	CAN#1, Interrupt #0, Channel #1
108	canfd_1_interrupts1_0_IRQn	Active	CAN#1, Interrupt #1, Channel #0
109	canfd_1_interrupts1_1_IRQn	Active	CAN#1, Interrupt #1, Channel #1
114	lin_0_interrupts_0_IRQn	Active	LIN#0, Channel #0 Interrupt
115	lin_0_interrupts_1_IRQn	Active	LIN#0, Channel #1 Interrupt
130	cxpi_0_interrupts_0_IRQn	Active	CXPI#0 Channel #0 Interrupt
131	cxpi_0_interrupts_1_IRQn	Active	CXPI#0 Channel #1 Interrupt
135	scb_1_interrupt_IRQn	Active	SCB#1 Interrupt
136	scb_2_interrupt_IRQn	Active	SCB#2 Interrupt
137	scb_3_interrupt_IRQn	Active	SCB#3 Interrupt
138	scb_4_interrupt_IRQn	Active	SCB#4 Interrupt
139	scb_5_interrupt_IRQn	Active	SCB#5 Interrupt
140	scb_6_interrupt_IRQn	Active	SCB#6 Interrupt
141	scb_7_interrupt_IRQn	Active	SCB#7 Interrupt
142	scb_8_interrupt_IRQn	Active	SCB#8 Interrupt
143	scb_9_interrupt_IRQn	Active	SCB#9 Interrupt
144	scb_10_interrupt_IRQn	Active	SCB#10 Interrupt
145	scb_11_interrupt_IRQn	Active	SCB#11 Interrupt
160	pass_0_interrupts_sar_0_IRQn	Active	SAR#0, Logical Channel#0 Interrupt
161	pass_0_interrupts_sar_1_IRQn	Active	SAR#0, Logical Channel#1 Interrupt
162	pass_0_interrupts_sar_2_IRQn	Active	SAR#0, Logical Channel#2 Interrupt
163	pass_0_interrupts_sar_3_IRQn	Active	SAR#0, Logical Channel#3 Interrupt
164	pass_0_interrupts_sar_4_IRQn	Active	SAR#0, Logical Channel#4 Interrupt
165	pass_0_interrupts_sar_5_IRQn	Active	SAR#0, Logical Channel#5 Interrupt
166	pass_0_interrupts_sar_6_IRQn	Active	SAR#0, Logical Channel#6 Interrupt
167	pass_0_interrupts_sar_7_IRQn	Active	SAR#0, Logical Channel#7 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
168	pass_0_interrupts_sar_8_IRQn	Active	SAR#0, Logical Channel#8 Interrupt
169	pass_0_interrupts_sar_9_IRQn	Active	SAR#0, Logical Channel#9 Interrupt
170	pass_0_interrupts_sar_10_IRQn	Active	SAR#0, Logical Channel#10 Interrupt
171	pass_0_interrupts_sar_11_IRQn	Active	SAR#0, Logical Channel#11 Interrupt
172	pass_0_interrupts_sar_12_IRQn	Active	SAR#0, Logical Channel#12 Interrupt
173	pass_0_interrupts_sar_13_IRQn	Active	SAR#0, Logical Channel#13 Interrupt
174	pass_0_interrupts_sar_14_IRQn	Active	SAR#0, Logical Channel#14 Interrupt
175	pass_0_interrupts_sar_15_IRQn	Active	SAR#0, Logical Channel#15 Interrupt
176	pass_0_interrupts_sar_16_IRQn	Active	SAR#0, Logical Channel#16 Interrupt
177	pass_0_interrupts_sar_17_IRQn	Active	SAR#0, Logical Channel#17 Interrupt
178	pass_0_interrupts_sar_18_IRQn	Active	SAR#0, Logical Channel#18 Interrupt
179	pass_0_interrupts_sar_19_IRQn	Active	SAR#0, Logical Channel#19 Interrupt
180	pass_0_interrupts_sar_20_IRQn	Active	SAR#0, Logical Channel#20 Interrupt
181	pass_0_interrupts_sar_21_IRQn	Active	SAR#0, Logical Channel#21 Interrupt
182	pass_0_interrupts_sar_22_IRQn	Active	SAR#0, Logical Channel#22 Interrupt
183	pass_0_interrupts_sar_23_IRQn	Active	SAR#0, Logical Channel#23 Interrupt
184	pass_0_interrupts_sar_24_IRQn	Active	SAR#0, Logical Channel#24 Interrupt
185	pass_0_interrupts_sar_25_IRQn	Active	SAR#0, Logical Channel#25 Interrupt
186	pass_0_interrupts_sar_26_IRQn	Active	SAR#0, Logical Channel#26 Interrupt
187	pass_0_interrupts_sar_27_IRQn	Active	SAR#0, Logical Channel#27 Interrupt
188	pass_0_interrupts_sar_28_IRQn	Active	SAR#0, Logical Channel#28 Interrupt
189	pass_0_interrupts_sar_29_IRQn	Active	SAR#0, Logical Channel#29 Interrupt
190	pass_0_interrupts_sar_30_IRQn	Active	SAR#0, Logical Channel#30 Interrupt
191	pass_0_interrupts_sar_31_IRQn	Active	SAR#0, Logical Channel#31 Interrupt
288	cpuss_interrupts_dmac_0_IRQn	Active	CPUSS M-DMA#0, Channel#0 Interrupt
289	cpuss_interrupts_dmac_1_IRQn	Active	CPUSS M-DMA#0, Channel#1 Interrupt
290	cpuss_interrupts_dmac_2_IRQn	Active	CPUSS M-DMA#0, Channel#2 Interrupt
291	cpuss_interrupts_dmac_3_IRQn	Active	CPUSS M-DMA#0, Channel#3 Interrupt
296	cpuss_interrupts_dw0_0_IRQn	Active	CPUSS P-DMA#0, Channel#0 Interrupt
297	cpuss_interrupts_dw0_1_IRQn	Active	CPUSS P-DMA#0, Channel#1 Interrupt
298	cpuss_interrupts_dw0_2_IRQn	Active	CPUSS P-DMA#0, Channel#2 Interrupt
299	cpuss_interrupts_dw0_3_IRQn	Active	CPUSS P-DMA#0, Channel#3 Interrupt
300	cpuss_interrupts_dw0_4_IRQn	Active	CPUSS P-DMA#0, Channel#4 Interrupt
301	cpuss_interrupts_dw0_5_IRQn	Active	CPUSS P-DMA#0, Channel#5 Interrupt
302	cpuss_interrupts_dw0_6_IRQn	Active	CPUSS P-DMA#0, Channel#6 Interrupt
303	cpuss_interrupts_dw0_7_IRQn	Active	CPUSS P-DMA#0, Channel#7 Interrupt
304	cpuss_interrupts_dw0_8_IRQn	Active	CPUSS P-DMA#0, Channel#8 Interrupt
305	cpuss_interrupts_dw0_9_IRQn	Active	CPUSS P-DMA#0, Channel#9 Interrupt
306	cpuss_interrupts_dw0_10_IRQn	Active	CPUSS P-DMA#0, Channel#10 Interrupt
307	cpuss_interrupts_dw0_11_IRQn	Active	CPUSS P-DMA#0, Channel#11 Interrupt
308	cpuss_interrupts_dw0_12_IRQn	Active	CPUSS P-DMA#0, Channel#12 Interrupt
309	cpuss_interrupts_dw0_13_IRQn	Active	CPUSS P-DMA#0, Channel#13 Interrupt
310	cpuss_interrupts_dw0_14_IRQn	Active	CPUSS P-DMA#0, Channel#14 Interrupt
311	cpuss_interrupts_dw0_15_IRQn	Active	CPUSS P-DMA#0, Channel#15 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
312	cpuss_interrupts_dw0_16_IRQn	Active	CPUSS P-DMA#0, Channel#16 Interrupt
313	cpuss_interrupts_dw0_17_IRQn	Active	CPUSS P-DMA#0, Channel#17 Interrupt
314	cpuss_interrupts_dw0_18_IRQn	Active	CPUSS P-DMA#0, Channel#18 Interrupt
315	cpuss_interrupts_dw0_19_IRQn	Active	CPUSS P-DMA#0, Channel#19 Interrupt
316	cpuss_interrupts_dw0_20_IRQn	Active	CPUSS P-DMA#0, Channel#20 Interrupt
317	cpuss_interrupts_dw0_21_IRQn	Active	CPUSS P-DMA#0, Channel#21 Interrupt
318	cpuss_interrupts_dw0_22_IRQn	Active	CPUSS P-DMA#0, Channel#22 Interrupt
319	cpuss_interrupts_dw0_23_IRQn	Active	CPUSS P-DMA#0, Channel#23 Interrupt
320	cpuss_interrupts_dw0_24_IRQn	Active	CPUSS P-DMA#0, Channel#24 Interrupt
321	cpuss_interrupts_dw0_25_IRQn	Active	CPUSS P-DMA#0, Channel#25 Interrupt
322	cpuss_interrupts_dw0_26_IRQn	Active	CPUSS P-DMA#0, Channel#26 Interrupt
323	cpuss_interrupts_dw0_27_IRQn	Active	CPUSS P-DMA#0, Channel#27 Interrupt
324	cpuss_interrupts_dw0_28_IRQn	Active	CPUSS P-DMA#0, Channel#28 Interrupt
325	cpuss_interrupts_dw0_29_IRQn	Active	CPUSS P-DMA#0, Channel#29 Interrupt
326	cpuss_interrupts_dw0_30_IRQn	Active	CPUSS P-DMA#0, Channel#30 Interrupt
327	cpuss_interrupts_dw0_31_IRQn	Active	CPUSS P-DMA#0, Channel#31 Interrupt
328	cpuss_interrupts_dw0_32_IRQn	Active	CPUSS P-DMA#0, Channel#32 Interrupt
329	cpuss_interrupts_dw0_33_IRQn	Active	CPUSS P-DMA#0, Channel#33 Interrupt
330	cpuss_interrupts_dw0_34_IRQn	Active	CPUSS P-DMA#0, Channel#34 Interrupt
331	cpuss_interrupts_dw0_35_IRQn	Active	CPUSS P-DMA#0, Channel#35 Interrupt
332	cpuss_interrupts_dw0_36_IRQn	Active	CPUSS P-DMA#0, Channel#36 Interrupt
333	cpuss_interrupts_dw0_37_IRQn	Active	CPUSS P-DMA#0, Channel#37 Interrupt
334	cpuss_interrupts_dw0_38_IRQn	Active	CPUSS P-DMA#0, Channel#38 Interrupt
335	cpuss_interrupts_dw0_39_IRQn	Active	CPUSS P-DMA#0, Channel#39 Interrupt
336	cpuss_interrupts_dw0_40_IRQn	Active	CPUSS P-DMA#0, Channel#40 Interrupt
337	cpuss_interrupts_dw0_41_IRQn	Active	CPUSS P-DMA#0, Channel#41 Interrupt
338	cpuss_interrupts_dw0_42_IRQn	Active	CPUSS P-DMA#0, Channel#42 Interrupt
339	cpuss_interrupts_dw0_43_IRQn	Active	CPUSS P-DMA#0, Channel#43 Interrupt
340	cpuss_interrupts_dw0_44_IRQn	Active	CPUSS P-DMA#0, Channel#44 Interrupt
341	cpuss_interrupts_dw0_45_IRQn	Active	CPUSS P-DMA#0, Channel#45 Interrupt
342	cpuss_interrupts_dw0_46_IRQn	Active	CPUSS P-DMA#0, Channel#46 Interrupt
343	cpuss_interrupts_dw0_47_IRQn	Active	CPUSS P-DMA#0, Channel#47 Interrupt
344	cpuss_interrupts_dw0_48_IRQn	Active	CPUSS P-DMA#0, Channel#48 Interrupt
345	cpuss_interrupts_dw0_49_IRQn	Active	CPUSS P-DMA#0, Channel#49 Interrupt
346	cpuss_interrupts_dw0_50_IRQn	Active	CPUSS P-DMA#0, Channel#50 Interrupt
347	cpuss_interrupts_dw0_51_IRQn	Active	CPUSS P-DMA#0, Channel#51 Interrupt
348	cpuss_interrupts_dw0_52_IRQn	Active	CPUSS P-DMA#0, Channel#52 Interrupt
349	cpuss_interrupts_dw0_53_IRQn	Active	CPUSS P-DMA#0, Channel#53 Interrupt
350	cpuss_interrupts_dw0_54_IRQn	Active	CPUSS P-DMA#0, Channel#54 Interrupt
351	cpuss_interrupts_dw0_55_IRQn	Active	CPUSS P-DMA#0, Channel#55 Interrupt
352	cpuss_interrupts_dw0_56_IRQn	Active	CPUSS P-DMA#0, Channel#56 Interrupt
353	cpuss_interrupts_dw0_57_IRQn	Active	CPUSS P-DMA#0, Channel#57 Interrupt
354	cpuss_interrupts_dw0_58_IRQn	Active	CPUSS P-DMA#0, Channel#58 Interrupt
355	cpuss_interrupts_dw0_59_IRQn	Active	CPUSS P-DMA#0, Channel#59 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
356	cpuss_interrupts_dw0_60_IRQn	Active	CPUSS P-DMA#0, Channel#60 Interrupt
357	cpuss_interrupts_dw0_61_IRQn	Active	CPUSS P-DMA#0, Channel#61 Interrupt
358	cpuss_interrupts_dw0_62_IRQn	Active	CPUSS P-DMA#0, Channel#62 Interrupt
359	cpuss_interrupts_dw0_63_IRQn	Active	CPUSS P-DMA#0, Channel#63 Interrupt
360	cpuss_interrupts_dw0_64_IRQn	Active	CPUSS P-DMA#0, Channel#64 Interrupt
361	cpuss_interrupts_dw0_65_IRQn	Active	CPUSS P-DMA#0, Channel#65 Interrupt
362	cpuss_interrupts_dw0_66_IRQn	Active	CPUSS P-DMA#0, Channel#66 Interrupt
363	cpuss_interrupts_dw0_67_IRQn	Active	CPUSS P-DMA#0, Channel#67 Interrupt
364	cpuss_interrupts_dw0_68_IRQn	Active	CPUSS P-DMA#0, Channel#68 Interrupt
365	cpuss_interrupts_dw0_69_IRQn	Active	CPUSS P-DMA#0, Channel#69 Interrupt
366	cpuss_interrupts_dw0_70_IRQn	Active	CPUSS P-DMA#0, Channel#70 Interrupt
367	cpuss_interrupts_dw0_71_IRQn	Active	CPUSS P-DMA#0, Channel#71 Interrupt
368	cpuss_interrupts_dw0_72_IRQn	Active	CPUSS P-DMA#0, Channel#72 Interrupt
369	cpuss_interrupts_dw0_73_IRQn	Active	CPUSS P-DMA#0, Channel#73 Interrupt
370	cpuss_interrupts_dw0_74_IRQn	Active	CPUSS P-DMA#0, Channel#74 Interrupt
371	cpuss_interrupts_dw0_75_IRQn	Active	CPUSS P-DMA#0, Channel#75 Interrupt
424	cpuss_interrupts_dw1_0_IRQn	Active	CPUSS P-DMA#1, Channel#0 Interrupt
425	cpuss_interrupts_dw1_1_IRQn	Active	CPUSS P-DMA#1, Channel#1 Interrupt
426	cpuss_interrupts_dw1_2_IRQn	Active	CPUSS P-DMA#1, Channel#2 Interrupt
427	cpuss_interrupts_dw1_3_IRQn	Active	CPUSS P-DMA#1, Channel#3 Interrupt
428	cpuss_interrupts_dw1_4_IRQn	Active	CPUSS P-DMA#1, Channel#4 Interrupt
429	cpuss_interrupts_dw1_5_IRQn	Active	CPUSS P-DMA#1, Channel#5 Interrupt
430	cpuss_interrupts_dw1_6_IRQn	Active	CPUSS P-DMA#1, Channel#6 Interrupt
431	cpuss_interrupts_dw1_7_IRQn	Active	CPUSS P-DMA#1, Channel#7 Interrupt
432	cpuss_interrupts_dw1_8_IRQn	Active	CPUSS P-DMA#1, Channel#8 Interrupt
433	cpuss_interrupts_dw1_9_IRQn	Active	CPUSS P-DMA#1, Channel#9 Interrupt
434	cpuss_interrupts_dw1_10_IRQn	Active	CPUSS P-DMA#1, Channel#10 Interrupt
435	cpuss_interrupts_dw1_11_IRQn	Active	CPUSS P-DMA#1, Channel#11 Interrupt
436	cpuss_interrupts_dw1_12_IRQn	Active	CPUSS P-DMA#1, Channel#12 Interrupt
437	cpuss_interrupts_dw1_13_IRQn	Active	CPUSS P-DMA#1, Channel#13 Interrupt
438	cpuss_interrupts_dw1_14_IRQn	Active	CPUSS P-DMA#1, Channel#14 Interrupt
439	cpuss_interrupts_dw1_15_IRQn	Active	CPUSS P-DMA#1, Channel#15 Interrupt
440	cpuss_interrupts_dw1_16_IRQn	Active	CPUSS P-DMA#1, Channel#16 Interrupt
441	cpuss_interrupts_dw1_17_IRQn	Active	CPUSS P-DMA#1, Channel#17 Interrupt
442	cpuss_interrupts_dw1_18_IRQn	Active	CPUSS P-DMA#1, Channel#18 Interrupt
443	cpuss_interrupts_dw1_19_IRQn	Active	CPUSS P-DMA#1, Channel#19 Interrupt
444	cpuss_interrupts_dw1_20_IRQn	Active	CPUSS P-DMA#1, Channel#20 Interrupt
445	cpuss_interrupts_dw1_21_IRQn	Active	CPUSS P-DMA#1, Channel#21 Interrupt
446	cpuss_interrupts_dw1_22_IRQn	Active	CPUSS P-DMA#1, Channel#22 Interrupt
447	cpuss_interrupts_dw1_23_IRQn	Active	CPUSS P-DMA#1, Channel#23 Interrupt
448	cpuss_interrupts_dw1_24_IRQn	Active	CPUSS P-DMA#1, Channel#24 Interrupt
449	cpuss_interrupts_dw1_25_IRQn	Active	CPUSS P-DMA#1, Channel#25 Interrupt
450	cpuss_interrupts_dw1_26_IRQn	Active	CPUSS P-DMA#1, Channel#26 Interrupt
451	cpuss_interrupts_dw1_27_IRQn	Active	CPUSS P-DMA#1, Channel#27 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
452	cpuss_interrupts_dw1_28_IRQn	Active	CPUSS P-DMA#1, Channel#28 Interrupt
453	cpuss_interrupts_dw1_29_IRQn	Active	CPUSS P-DMA#1, Channel#29 Interrupt
454	cpuss_interrupts_dw1_30_IRQn	Active	CPUSS P-DMA#1, Channel#30 Interrupt
455	cpuss_interrupts_dw1_31_IRQn	Active	CPUSS P-DMA#1, Channel#31 Interrupt
456	cpuss_interrupts_dw1_32_IRQn	Active	CPUSS P-DMA#1, Channel#32 Interrupt
457	cpuss_interrupts_dw1_33_IRQn	Active	CPUSS P-DMA#1, Channel#33 Interrupt
458	cpuss_interrupts_dw1_34_IRQn	Active	CPUSS P-DMA#1, Channel#34 Interrupt
459	cpuss_interrupts_dw1_35_IRQn	Active	CPUSS P-DMA#1, Channel#35 Interrupt
460	cpuss_interrupts_dw1_36_IRQn	Active	CPUSS P-DMA#1, Channel#36 Interrupt
461	cpuss_interrupts_dw1_37_IRQn	Active	CPUSS P-DMA#1, Channel#37 Interrupt
462	cpuss_interrupts_dw1_38_IRQn	Active	CPUSS P-DMA#1, Channel#38 Interrupt
463	cpuss_interrupts_dw1_39_IRQn	Active	CPUSS P-DMA#1, Channel#39 Interrupt
464	cpuss_interrupts_dw1_40_IRQn	Active	CPUSS P-DMA#1, Channel#40 Interrupt
465	cpuss_interrupts_dw1_41_IRQn	Active	CPUSS P-DMA#1, Channel#41 Interrupt
466	cpuss_interrupts_dw1_42_IRQn	Active	CPUSS P-DMA#1, Channel#42 Interrupt
467	cpuss_interrupts_dw1_43_IRQn	Active	CPUSS P-DMA#1, Channel#43 Interrupt
468	cpuss_interrupts_dw1_44_IRQn	Active	CPUSS P-DMA#1, Channel#44 Interrupt
469	cpuss_interrupts_dw1_45_IRQn	Active	CPUSS P-DMA#1, Channel#45 Interrupt
470	cpuss_interrupts_dw1_46_IRQn	Active	CPUSS P-DMA#1, Channel#46 Interrupt
471	cpuss_interrupts_dw1_47_IRQn	Active	CPUSS P-DMA#1, Channel#47 Interrupt
472	cpuss_interrupts_dw1_48_IRQn	Active	CPUSS P-DMA#1, Channel#48 Interrupt
473	cpuss_interrupts_dw1_49_IRQn	Active	CPUSS P-DMA#1, Channel#49 Interrupt
474	cpuss_interrupts_dw1_50_IRQn	Active	CPUSS P-DMA#1, Channel#50 Interrupt
475	cpuss_interrupts_dw1_51_IRQn	Active	CPUSS P-DMA#1, Channel#51 Interrupt
476	cpuss_interrupts_dw1_52_IRQn	Active	CPUSS P-DMA#1, Channel#52 Interrupt
477	cpuss_interrupts_dw1_53_IRQn	Active	CPUSS P-DMA#1, Channel#53 Interrupt
478	cpuss_interrupts_dw1_54_IRQn	Active	CPUSS P-DMA#1, Channel#54 Interrupt
479	cpuss_interrupts_dw1_55_IRQn	Active	CPUSS P-DMA#1, Channel#55 Interrupt
480	cpuss_interrupts_dw1_56_IRQn	Active	CPUSS P-DMA#1, Channel#56 Interrupt
481	cpuss_interrupts_dw1_57_IRQn	Active	CPUSS P-DMA#1, Channel#57 Interrupt
482	cpuss_interrupts_dw1_58_IRQn	Active	CPUSS P-DMA#1, Channel#58 Interrupt
483	cpuss_interrupts_dw1_59_IRQn	Active	CPUSS P-DMA#1, Channel#59 Interrupt
484	cpuss_interrupts_dw1_60_IRQn	Active	CPUSS P-DMA#1, Channel#60 Interrupt
485	cpuss_interrupts_dw1_61_IRQn	Active	CPUSS P-DMA#1, Channel#61 Interrupt
486	cpuss_interrupts_dw1_62_IRQn	Active	CPUSS P-DMA#1, Channel#62 Interrupt
487	cpuss_interrupts_dw1_63_IRQn	Active	CPUSS P-DMA#1, Channel#63 Interrupt
488	cpuss_interrupts_dw1_64_IRQn	Active	CPUSS P-DMA#1, Channel#64 Interrupt
489	cpuss_interrupts_dw1_65_IRQn	Active	CPUSS P-DMA#1, Channel#65 Interrupt
490	cpuss_interrupts_dw1_66_IRQn	Active	CPUSS P-DMA#1, Channel#66 Interrupt
491	cpuss_interrupts_dw1_67_IRQn	Active	CPUSS P-DMA#1, Channel#67 Interrupt
492	cpuss_interrupts_dw1_68_IRQn	Active	CPUSS P-DMA#1, Channel#68 Interrupt
493	cpuss_interrupts_dw1_69_IRQn	Active	CPUSS P-DMA#1, Channel#69 Interrupt
494	cpuss_interrupts_dw1_70_IRQn	Active	CPUSS P-DMA#1, Channel#70 Interrupt
495	cpuss_interrupts_dw1_71_IRQn	Active	CPUSS P-DMA#1, Channel#71 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
496	cpuss_interrupts_dw1_72_IRQn	Active	CPUSS P-DMA#1, Channel#72 Interrupt
497	cpuss_interrupts_dw1_73_IRQn	Active	CPUSS P-DMA#1, Channel#73 Interrupt
498	cpuss_interrupts_dw1_74_IRQn	Active	CPUSS P-DMA#1, Channel#74 Interrupt
499	cpuss_interrupts_dw1_75_IRQn	Active	CPUSS P-DMA#1, Channel#75 Interrupt
500	cpuss_interrupts_dw1_76_IRQn	Active	CPUSS P-DMA#1, Channel#76 Interrupt
501	cpuss_interrupts_dw1_77_IRQn	Active	CPUSS P-DMA#1, Channel#77 Interrupt
502	cpuss_interrupts_dw1_78_IRQn	Active	CPUSS P-DMA#1, Channel#78 Interrupt
503	cpuss_interrupts_dw1_79_IRQn	Active	CPUSS P-DMA#1, Channel#79 Interrupt
504	cpuss_interrupts_dw1_80_IRQn	Active	CPUSS P-DMA#1, Channel#80 Interrupt
505	cpuss_interrupts_dw1_81_IRQn	Active	CPUSS P-DMA#1, Channel#81 Interrupt
506	cpuss_interrupts_dw1_82_IRQn	Active	CPUSS P-DMA#1, Channel#82 Interrupt
507	cpuss_interrupts_dw1_83_IRQn	Active	CPUSS P-DMA#1, Channel#83 Interrupt
552	tcpwm_0_interrupts_0_IRQn	Active	TCPWM0 Group#0, Counter#0 Interrupt
553	tcpwm_0_interrupts_1_IRQn	Active	TCPWM0 Group#0, Counter#1 Interrupt
554	tcpwm_0_interrupts_2_IRQn	Active	TCPWM0 Group#0, Counter#2 Interrupt
555	tcpwm_0_interrupts_3_IRQn	Active	TCPWM0 Group#0, Counter#3 Interrupt
556	tcpwm_0_interrupts_4_IRQn	Active	TCPWM0 Group#0, Counter#4 Interrupt
557	tcpwm_0_interrupts_5_IRQn	Active	TCPWM0 Group#0, Counter#5 Interrupt
558	tcpwm_0_interrupts_6_IRQn	Active	TCPWM0 Group#0, Counter#6 Interrupt
559	tcpwm_0_interrupts_7_IRQn	Active	TCPWM0 Group#0, Counter#7 Interrupt
560	tcpwm_0_interrupts_8_IRQn	Active	TCPWM0 Group#0, Counter#8 Interrupt
561	tcpwm_0_interrupts_9_IRQn	Active	TCPWM0 Group#0, Counter#9 Interrupt
562	tcpwm_0_interrupts_10_IRQn	Active	TCPWM0 Group#0, Counter#10 Interrupt
563	tcpwm_0_interrupts_11_IRQn	Active	TCPWM0 Group#0, Counter#11 Interrupt
564	tcpwm_0_interrupts_12_IRQn	Active	TCPWM0 Group#0, Counter#12 Interrupt
565	tcpwm_0_interrupts_13_IRQn	Active	TCPWM0 Group#0, Counter#13 Interrupt
566	tcpwm_0_interrupts_14_IRQn	Active	TCPWM0 Group#0, Counter#14 Interrupt
567	tcpwm_0_interrupts_15_IRQn	Active	TCPWM0 Group#0, Counter#15 Interrupt
568	tcpwm_0_interrupts_16_IRQn	Active	TCPWM0 Group#0, Counter#16 Interrupt
569	tcpwm_0_interrupts_17_IRQn	Active	TCPWM0 Group#0, Counter#17 Interrupt
570	tcpwm_0_interrupts_18_IRQn	Active	TCPWM0 Group#0, Counter#18 Interrupt
571	tcpwm_0_interrupts_19_IRQn	Active	TCPWM0 Group#0, Counter#19 Interrupt
572	tcpwm_0_interrupts_20_IRQn	Active	TCPWM0 Group#0, Counter#20 Interrupt
573	tcpwm_0_interrupts_21_IRQn	Active	TCPWM0 Group#0, Counter#21 Interrupt
574	tcpwm_0_interrupts_22_IRQn	Active	TCPWM0 Group#0, Counter#22 Interrupt
575	tcpwm_0_interrupts_23_IRQn	Active	TCPWM0 Group#0, Counter#23 Interrupt
576	tcpwm_0_interrupts_24_IRQn	Active	TCPWM0 Group#0, Counter#24 Interrupt
577	tcpwm_0_interrupts_25_IRQn	Active	TCPWM0 Group#0, Counter#25 Interrupt
578	tcpwm_0_interrupts_26_IRQn	Active	TCPWM0 Group#0, Counter#26 Interrupt
579	tcpwm_0_interrupts_27_IRQn	Active	TCPWM0 Group#0, Counter#27 Interrupt
580	tcpwm_0_interrupts_28_IRQn	Active	TCPWM0 Group#0, Counter#28 Interrupt
581	tcpwm_0_interrupts_29_IRQn	Active	TCPWM0 Group#0, Counter#29 Interrupt
582	tcpwm_0_interrupts_30_IRQn	Active	TCPWM0 Group#0, Counter#30 Interrupt
583	tcpwm_0_interrupts_31_IRQn	Active	TCPWM0 Group#0, Counter#31 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
584	tcpwm_0_interrupts_32_IRQn	Active	TCPWM0 Group#0, Counter#32 Interrupt
585	tcpwm_0_interrupts_33_IRQn	Active	TCPWM0 Group#0, Counter#33 Interrupt
616	tcpwm_0_interrupts_256_IRQn	Active	TCPWM0 Group#1, Counter#0 Interrupt
617	tcpwm_0_interrupts_257_IRQn	Active	TCPWM0 Group#1, Counter#1 Interrupt
618	tcpwm_0_interrupts_258_IRQn	Active	TCPWM0 Group#1, Counter#2 Interrupt
619	tcpwm_0_interrupts_259_IRQn	Active	TCPWM0 Group#1, Counter#3 Interrupt
620	tcpwm_0_interrupts_260_IRQn	Active	TCPWM0 Group#1, Counter#4 Interrupt
621	tcpwm_0_interrupts_261_IRQn	Active	TCPWM0 Group#1, Counter#5 Interrupt
622	tcpwm_0_interrupts_262_IRQn	Active	TCPWM0 Group#1, Counter#6 Interrupt
623	tcpwm_0_interrupts_263_IRQn	Active	TCPWM0 Group#1, Counter#7 Interrupt
624	tcpwm_0_interrupts_264_IRQn	Active	TCPWM0 Group#1, Counter#8 Interrupt
625	tcpwm_0_interrupts_265_IRQn	Active	TCPWM0 Group#1, Counter#9 Interrupt
626	tcpwm_0_interrupts_266_IRQn	Active	TCPWM0 Group#1, Counter#10 Interrupt
627	tcpwm_0_interrupts_267_IRQn	Active	TCPWM0 Group#1, Counter#11 Interrupt
680	tcpwm_0_interrupts_512_IRQn	Active	TCPWM0 Group#2, Counter#0 Interrupt
681	tcpwm_0_interrupts_513_IRQn	Active	TCPWM0 Group#2, Counter#1 Interrupt
682	tcpwm_0_interrupts_514_IRQn	Active	TCPWM0 Group#2, Counter#2 Interrupt
683	tcpwm_0_interrupts_515_IRQn	Active	TCPWM0 Group#2, Counter#3 Interrupt
684	tcpwm_0_interrupts_516_IRQn	Active	TCPWM0 Group#2, Counter#4 Interrupt
685	tcpwm_0_interrupts_517_IRQn	Active	TCPWM0 Group#2, Counter#5 Interrupt
686	tcpwm_0_interrupts_518_IRQn	Active	TCPWM0 Group#2, Counter#6 Interrupt
687	tcpwm_0_interrupts_519_IRQn	Active	TCPWM0 Group#2, Counter#7 Interrupt
688	tcpwm_0_interrupts_520_IRQn	Active	TCPWM0 Group#2, Counter#8 Interrupt
689	tcpwm_0_interrupts_521_IRQn	Active	TCPWM0 Group#2, Counter#9 Interrupt
690	tcpwm_0_interrupts_522_IRQn	Active	TCPWM0 Group#2, Counter#10 Interrupt
691	tcpwm_0_interrupts_523_IRQn	Active	TCPWM0 Group#2, Counter#11 Interrupt
692	tcpwm_0_interrupts_524_IRQn	Active	TCPWM0 Group#2, Counter#12 Interrupt
693	tcpwm_0_interrupts_525_IRQn	Active	TCPWM0 Group#2, Counter#13 Interrupt
694	tcpwm_0_interrupts_526_IRQn	Active	TCPWM0 Group#2, Counter#14 Interrupt
695	tcpwm_0_interrupts_527_IRQn	Active	TCPWM0 Group#2, Counter#15 Interrupt
752	tdm_0_interrupts_tx_0_IRQn	Active	TDM0 TX #0 Interrupt
753	tdm_0_interrupts_rx_0_IRQn	Active	TDM0 RX #0 Interrupt
754	tdm_0_interrupts_tx_1_IRQn	Active	TDM0 TX #1 Interrupt
755	tdm_0_interrupts_rx_1_IRQn	Active	TDM0 RX #1 Interrupt
760	sg_0_interrupts_0_IRQn	Active	SG0 #0 Interrupt
761	sg_0_interrupts_1_IRQn	Active	SG0 #1 Interrupt
762	sg_0_interrupts_2_IRQn	Active	SG0 #2 Interrupt
763	sg_0_interrupts_3_IRQn	Active	SG0 #3 Interrupt
764	sg_0_interrupts_4_IRQn	Active	SG0 #4 Interrupt
768	pwm_0_interrupts_0_IRQn	Active	PCM-PWM0 #0 Interrupt
769	pwm_0_interrupts_1_IRQn	Active	PCM-PWM0 #1 Interrupt
780	mixer_0_interrupt_dst_IRQn	Active	MIXER0 Destination interrupt
781	mixer_0_interrupts_src_0_IRQn	Active	MIXER0 Source #0 Interrupt
782	mixer_0_interrupts_src_1_IRQn	Active	MIXER0 Source #1 Interrupt

Table 15-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description
783	mixer_0_interrupts_src_2_IRQn	Active	MIXER0 Source #2 Interrupt
784	mixer_0_interrupts_src_3_IRQn	Active	MIXER0 Source #3 Interrupt
785	mixer_0_interrupts_src_4_IRQn	Active	MIXER0 Source #4 Interrupt

16 Core interrupt types

Table 16-1 Core interrupt types

Interrupt	Source	Power Mode	Description
0	CPUIntIdx0_IRQn[30]	DeepSleep	CPU User Interrupt #0
1	CPUIntIdx1_IRQn[30]	DeepSleep	CPU User Interrupt #1
2	CPUIntIdx2_IRQn	DeepSleep	CPU User Interrupt #2
3	CPUIntIdx3_IRQn	DeepSleep	CPU User Interrupt #3
4	CPUIntIdx4_IRQn	DeepSleep	CPU User Interrupt #4
5	CPUIntIdx5_IRQn	DeepSleep	CPU User Interrupt #5
6	CPUIntIdx6_IRQn	DeepSleep	CPU User Interrupt #6
7	CPUIntIdx7_IRQn	DeepSleep	CPU User Interrupt #7
8	Internal0_IRQn	Active	Internal Software Interrupt #0
9	Internal1_IRQn	Active	Internal Software Interrupt #1
10	Internal2_IRQn	Active	Internal Software Interrupt #2
11	Internal3_IRQn	Active	Internal Software Interrupt #3
12	Internal4_IRQn	Active	Internal Software Interrupt #4
13	Internal5_IRQn	Active	Internal Software Interrupt #5
14	Internal6_IRQn	Active	Internal Software Interrupt #6
15	Internal7_IRQn	Active	Internal Software Interrupt #7

Note
30.User interrupt cannot be used for CM0+ application, as it is used internally by system calls. Note, this does not impact CM4 application.

17 Trigger multiplexer

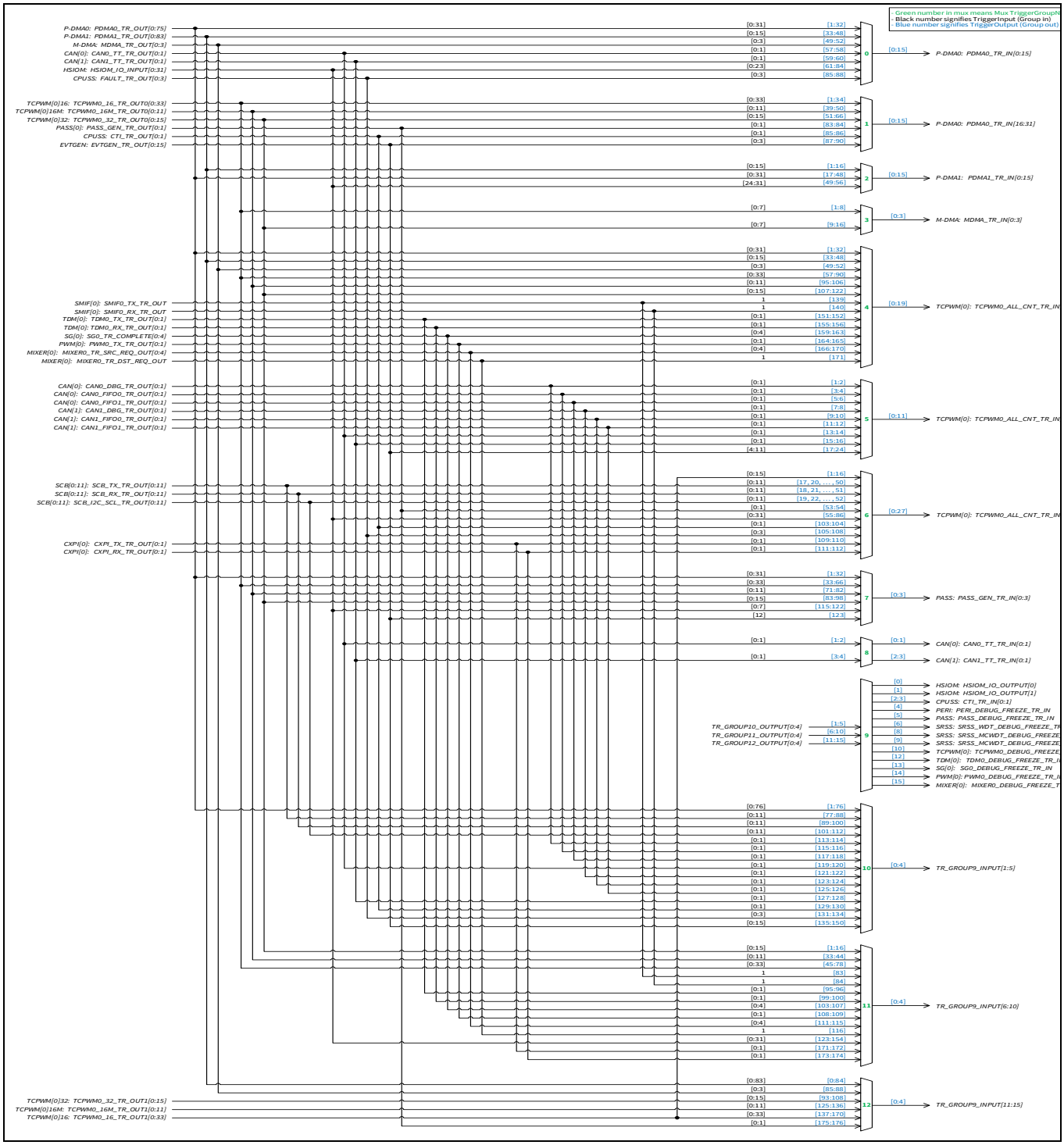


Figure 17-1 Trigger multiplexer[31]

Note
31. The diagram shows only the TRIG_LABEL, final trigger formation based on the formula TRIG_{PREFIX(IN/OUT)}_{MUX_x}_{TRIG_LABE / TRIG_{PREFIX(IN_1TO1/OUT_1TO1)}_{x}_{TRIG_LABEL} (see **Table 18-1**, **Table 19-1**, and **Table 20-1**.)

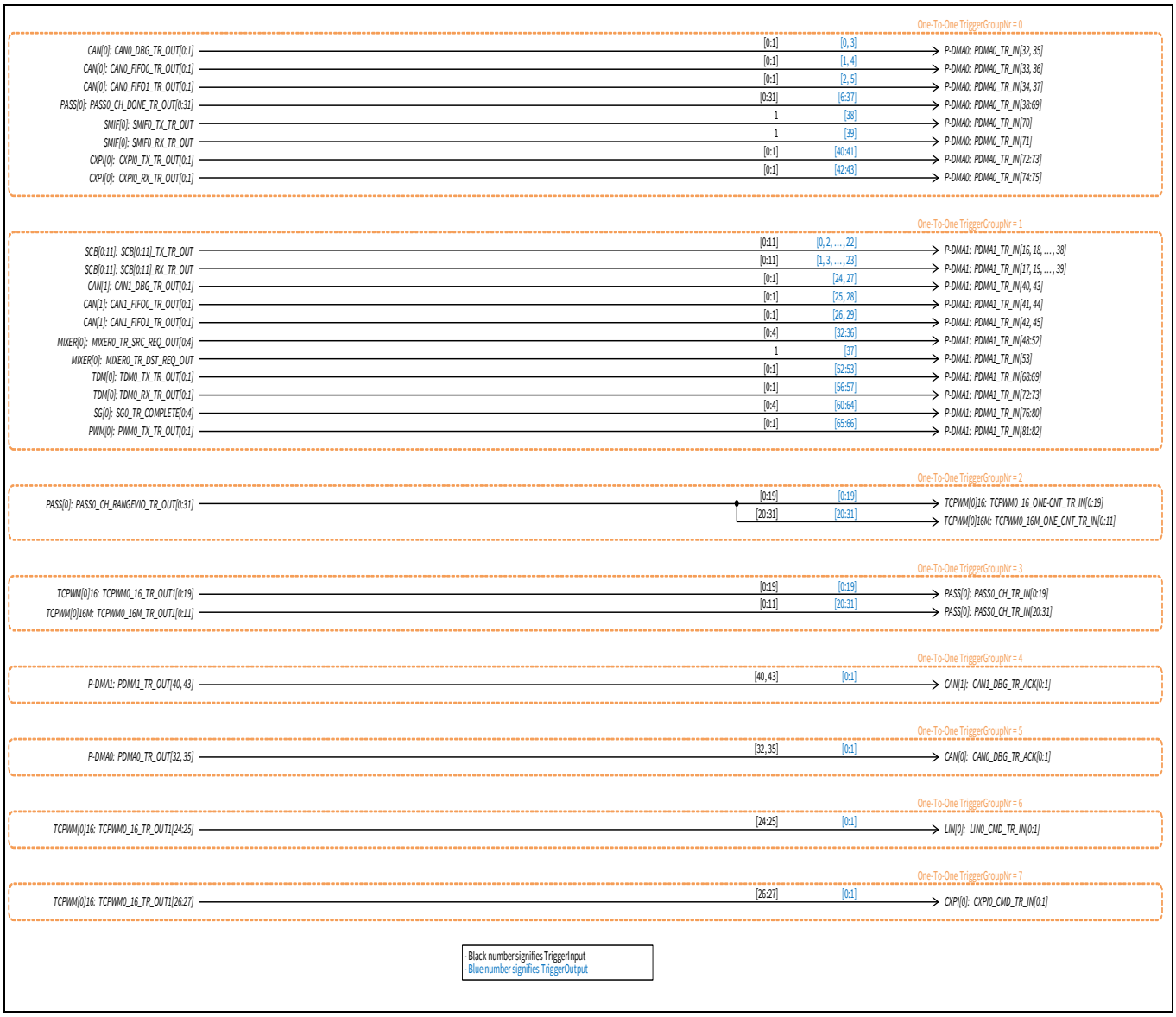


Figure 17-2 Triggers one-to-one[31]

18 Triggers group inputs

Table 18-1 Trigger inputs

Input	Trigger	Description
MUX Group 0: P-DMA0_0_15 trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	Allow P-DMA#0 to chain to itself. Channels 0 - 32 are general purpose channels available for chaining[32]
33:48	PDMA1_TR_OUT[0:15]	Cross connections from P-DMA#1 to P-DMA#0, Channels 0-15 are used
49:52	MDMA_TR_OUT[0:3]	Cross connections from M-DMA#0 to P-DMA#0
57:58	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
59:60	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
61:84	HSIOM_IO_INPUT[0:23]	I/O Inputs
85:88	FAULT_TR_OUT[0:3]	Fault events
MUX Group 1: P-DMA0_16_31 trigger multiplexer		
1:34	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
39:50	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
51:66	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
83:84	PASS_GEN_TR_OUT[0:1]	PASS#0 SAR events
85:86	CTI_TR_OUT[0:1]	Trace events
87:90	EVTGEN_TR_OUT[0:3]	Event generator triggers
MUX Group 2: P-DMA1_0_15 trigger multiplexer		
1:16	PDMA1_TR_OUT[0:15]	Allow P-DMA#1 to chain to itself. Channels 0–15 are dedicated for chaining
17:48	PDMA0_TR_OUT[0:31]	Cross connections from P-DMA#0 to P-DMA#1, channels 0-31 are used.
49:56	HSIOM_IO_INPUT[24:31]	I/O Inputs
MUX Group 3: M-DMA0 trigger multiplexer		
1:8	TCPWM0_16_TR_OUT0[0:7]	16-bit TCPWM#0 counters
9:16	TCPWM0_32_TR_OUT0[0:7]	32-bit TCPWM#0 counters
MUX Group 4: TCPWM0 Trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA#0 triggers
33:48	PDMA1_TR_OUT[0:15]	General purpose P-DMA#1 triggers
49:52	MDMA_TR_OUT[0:3]	AHB M-DMA#0 triggers
57:90	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
95:106	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
107:122	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
139	SMIF0_TX_TR_OUT	SMIF#0 TX trigger
140	SMIF0_RX_TR_OUT	SMIF#0 RX trigger
151:152	TDM0_TX_TR_OUT[0:1]	TDM#0 TX trigger
155:156	TDM0_RX_TR_OUT[0:1]	TDM#0 RX trigger
159:163	SG0_TX_TR_OUT[0:4]	SG#0 TX trigger
164:165	PWM0_TX_TR_OUT[0:1]	PWM#0 TX trigger
166:170	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER#0 SRC trigger
171	MIXER0_TR_DST_REQ_OUT	MIXER#0 DST trigger
MUX Group 5: TCPWM0_20_31 Trigger multiplexer		
1:2	CAN0_DBG_TR_OUT[0:1]	CAN#0 DMA events
3:4	CAN0_FIFO0_TR_OUT[0:1]	CAN#0 FIFO0 events

Note
32. "x:y" depicts a range starting from 'x' through 'y'.

Table 18-1 Trigger inputs *(continued)*

Input	Trigger	Description
5:6	CAN0_FIFO1_TR_OUT[0:1]	CAN#0 FIFO1 events
7:8	CAN1_DBG_TR_OUT[0:1]	CAN#1 DMA events
9:10	CAN1_FIFO0_TR_OUT[0:1]	CAN#1 FIFO0 events
11:12	CAN1_FIFO1_TR_OUT[0:1]	CAN#1 FIFO1 events
13:14	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
15:16	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
17:24	EVTGEN_TR_OUT[4:11]	Event generator triggers
MUX Group 6: TCPWM0_32_59 Trigger Multiplexer		
1:16	TCPWM0_16_TR_OUT1[0:15]	16-bit TCPWM#0 counters
17	SCB_TX_TR_OUT[0]	SCB#0 TX trigger
18	SCB_RX_TR_OUT[0]	SCB#0 RX trigger
19	SCB_I2C_SCL_TR_OUT[0]	SCB#0 I^2C trigger
20	SCB_TX_TR_OUT[1]	SCB#1 TX trigger
21	SCB_RX_TR_OUT[1]	SCB#1 RX trigger
22	SCB_I2C_SCL_TR_OUT[1]	SCB#1 I^2C trigger
23	SCB_TX_TR_OUT[2]	SCB#2 TX trigger
24	SCB_RX_TR_OUT[2]	SCB#2 RX trigger
25	SCB_I2C_SCL_TR_OUT[2]	SCB#2 I^2C trigger
26	SCB_TX_TR_OUT[3]	SCB#3 TX trigger
27	SCB_RX_TR_OUT[3]	SCB#3 RX trigger
28	SCB_I2C_SCL_TR_OUT[3]	SCB#3 I^2C trigger
29	SCB_TX_TR_OUT[4]	SCB#4 TX trigger
30	SCB_RX_TR_OUT[4]	SCB#4 RX trigger
31	SCB_I2C_SCL_TR_OUT[4]	SCB#4 I^2C trigger
32	SCB_TX_TR_OUT[5]	SCB#5 TX trigger
33	SCB_RX_TR_OUT[5]	SCB#5 RX trigger
34	SCB_I2C_SCL_TR_OUT[5]	SCB#5 I^2C trigger
35	SCB_TX_TR_OUT[6]	SCB#6 TX trigger
36	SCB_RX_TR_OUT[6]	SCB#6 RX trigger
37	SCB_I2C_SCL_TR_OUT[6]	SCB#6 I^2C trigger
38	SCB_TX_TR_OUT[7]	SCB#7 TX trigger
39	SCB_RX_TR_OUT[7]	SCB#7 RX trigger
40	SCB_I2C_SCL_TR_OUT[7]	SCB#7 I^2C trigger
41	SCB_TX_TR_OUT[8]	SCB#8 TX trigger
42	SCB_RX_TR_OUT[8]	SCB#8 RX trigger
43	SCB_I2C_SCL_TR_OUT[8]	SCB#8 I^2C trigger
44	SCB_TX_TR_OUT[9]	SCB#9 TX trigger
45	CB_RX_TR_OUT[9]	SCB#9 RX trigger
46	SCB_I2C_SCL_TR_OUT[9]	SCB#9 I^2C trigger
47	SCB_TX_TR_OUT[10]	SCB#10 TX trigger
48	SCB_RX_TR_OUT[10]	SCB#10 RX trigger
49	SCB_I2C_SCL_TR_OUT[10]	SCB#10 I^2C trigger
50	SCB_TX_TR_OUT[11]	SCB#11 TX trigger
51	SCB_RX_TR_OUT[11]	SCB#11 RX trigger
52	SCB_I2C_SCL_TR_OUT[11]	SCB#11 I^2C trigger

Table 18-1 Trigger inputs *(continued)*

Input	Trigger	Description
53:54	PASS_GEN_TR_OUT[0:1]	PASS#0 SAR events
55:86	HSIOM_IO_INPUT[0:31]	I/O inputs
103:104	CTI_TR_IN[0:1]	Trace events
105:108	FAULT_TR_OUT[0:3]	Fault events
109:110	CXPI_TX_TR_OUT[0:1]	CXPI#0 transmit events
111:112	CXPI_RX_TR_OUT[0:1]	CXPI#0 receive events
MUX Group 7: PASS0 SAR trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA#0 triggers
33:66	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
71:82	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
83:98	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
115:122	HSIOM_IO_INPUT[0:7]	I/O Inputs
123	EVTGEN_TR_OUT[12]	Event generator triggers
MUX Group 8: CAN TT Sync		
1:2	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
3:4	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
MUX Group 9: Debug MUX		
1:5	TR_GROUP10_OUTPUT[0:4]	Output from debug reduction multiplexer #1
6:10	TR_GROUP11_OUTPUT[0:4]	Output from debug reduction multiplexer #2
11:15	TR_GROUP12_OUTPUT[0:4]	Output from debug reduction multiplexer #3
MUX Group 10: Debug Reduction #1		
1:76	PDMA0_TR_OUT[0:75]	General purpose P-DMA#0 triggers
77:88	SCB_TX_TR_OUT[0:11]	SCB TX triggers
89:100	SCB_RX_TR_OUT[0:11]	SCB RX triggers
101:112	SCB_I2C_SCL_TR_OUT[0:11]	SCB I^2C triggers
113:114	CAN0_DBG_TR_OUT[0:1]	CAN#0 DMA
115:116	CAN0_FIFO0_TR_OUT[0:1]	CAN#0 FIFO0
117:118	CAN0_FIFO1_TR_OUT[0:1]	CAN#0 FIFO1
119:120	CAN0_TT_TR_OUT[0:1]	CAN#0 TT Sync Outputs
121:122	CAN1_DBG_TR_OUT[0:1]	CAN#1 DMA
123:124	CAN1_FIFO0_TR_OUT[0:1]	CAN#1 FIFO0
125:126	CAN1_FIFO1_TR_OUT[0:1]	CAN#1 FIFO1
127:128	CAN1_TT_TR_OUT[0:1]	CAN#1 TT Sync Outputs
129:130	CTI_TR_OUT[0:1]	Trace events
131:134	FAULT_TR_OU[0:3]	Fault events
135:150	EVTGEN_TR_OUT[0:15]	EVTGEN Triggers
MUX Group 11: Debug Reduction #2		
1:16	TCPWM0_32_TR_OUT0[0:15]	32-bit TCPWM#0 counters
33:44	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM#0 counters
45:78	TCPWM0_16_TR_OUT0[0:33]	16-bit TCPWM#0 counters
83	SMIF0_TX_TR_OUT	SMIF#0 TX trigger
84	SMIF0_RX_TR_OUT	SMIF#0 RX trigger
95:96	TDM0_TX_TR_OUT[0:1]	TDM#0 TX trigger
99:100	TDM0_RX_TR_OUT[0:1]	TDM#0 RX trigger
103:107	SG0_TX_TR_OUT[0:4]	SG#0 TX trigger

Table 18-1 Trigger inputs *(continued)*

Input	Trigger	Description
108:109	PWM0_TX_TR_OUT[0:1]	PWM#0 TX trigger
111:115	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER#0 SRC trigger
116	MIXER0_TR_DST_REQ_OUT	MIXER#0 DST trigger
123:154	HSIOM_IO_INPUT[0:31]	I/O inputs
171:172	CXPI_TX_TR_OUT[0:1]	CXPI#0 TX trigger
173:174	CXPI_RX_TR_OUT[0:1]	CXPI#0 RX trigger
MUX Group 12: Debug Reduction #3		
1:84	PDMA1_TR_OUT[0:83]	General purpose P-DMA#1 triggers
85:88	MDMA_TR_OUT[0:3]	M-DMA#0 triggers
93:108	TCPWM0_32_TR_OUT1[0:15]	32-bit TCPWM#0 counters
125:136	TCPWM0_16M_TR_OUT1[0:11]	16-bit Motor enhanced TCPWM#0 counters
137:170	TCPWM0_16_TR_OUT1[0:33]	16-bit TCPWM#0 counters
175:176	PASS_GEN_TR_OUT[0:1]	PASS#0 SAR events

19 Triggers group outputs

Table 19-1 Trigger outputs

Output	Trigger	Description
MUX Group 0: P-DMA0_0_15 trigger multiplexer		
0:15	PDMA0_TR_IN[0:15]	Triggers to P-DMA#0[0:15]
MUX Group 1: P-DMA0_16_31 trigger multiplexer		
0:15	PDMA0_TR_IN[16:31]	Triggers to P-DMA#0[16:31]
MUX Group 2: P-DMA1_0_15 trigger multiplexer		
0:15	PDMA1_TR_IN[0:15]	Triggers to P-DMA#1
MUX Group 3: M-DMA0 trigger multiplexer		
0:3	MDMA_TR_IN[0:3]	Triggers to M-DMA#0
MUX Group 4: TCPWM0 Trigger multiplexer		
0:19	TCPWM0_ALL_CNT_TR_IN[0:19]	Triggers to TCPWM#0
MUX Group 5: TCPWM0_20_31 Trigger multiplexer		
0:11	TCPWM0_ALL_CNT_TR_IN[20:31]	Triggers to TCPWM#0
MUX Group 6: TCPWM0_32_59 Trigger multiplexer		
0:27	TCPWM0_ALL_CNT_TR_IN[32:59]	Triggers to TCPWM#0
MUX Group 7: PASS0 SAR trigger multiplexer		
0:3	PASS_GEN_TR_IN[0:3]	Triggers to PASS#0 SAR
MUX Group 8: CAN TT Sync		
0:1	CAN0_TT_TR_IN[0:1]	CAN#0 TT Sync Inputs
2:3	CAN1_TT_TR_IN[0:1]	CAN#1 TT Sync Inputs
MUX Group 9: Debug MUX		
0	HSIOM_IO_OUTPUT[0]	To HSIOM as an output
1	HSIOM_IO_OUTPUT[1]	To HSIOM as an output
2:3	CTI_TR_IN[0:1]	To the Cross Trigger system
4	PERI_DEBUG_FREEZE_TR_IN	Signal to Freeze PERI operation
5	PASS_DEBUG_FREEZE_TR_IN	Signal to Freeze PASS#0 SAR operation
6	SRSS_WDT_DEBUG_FREEZE_TR_IN	Signal to Freeze WDT operation
8	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1]	Signal to Freeze MCWDT#1 operation
9	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0]	Signal to Freeze MCWDT#0 operation
10	TCPWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TCPWM#0 operation
12	TDM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TDM#0 operation
13	SG0_DEBUG_FREEZE_TR_IN	Signal to Freeze SG0# operation
14	PWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze PWM#0 operation
15	MIXER0_DEBUG_FREEZE_TR_IN	Signal to Freeze MIXER#0 operation
MUX Group 10: Debug Reduction #1		
0:4	TR_GROUP9_INPUT[1:5]	To main debug multiplexer
MUX Group 11: Debug Reduction #2		
0:4	TR_GROUP9_INPUT[6:10]	To main debug multiplexer
MUX Group 12: Debug Reduction #3		
0:4	TR_GROUP9_INPUT[11:15]	To main debug multiplexer

20 Triggers one-to-one

Table 20-1 Triggers 1:1

Input	Trigger In	Trigger Out	Description
MUX Group 0: CAN0 to P-DMA0 Triggers			
0	CAN0_DBG_TR_OUT[0]	PDMA0_TR_IN[32]	CAN0, Channel #0 P-DMA0 trigger
1	CAN0_FIFO0_TR_OUT[0]	PDMA0_TR_IN[33]	CAN0, Channel #0 FIFO0 trigger
2	CAN0_FIFO1_TR_OUT[0]	PDMA0_TR_IN[34]	CAN0, Channel #0 FIFO1 trigger
3	CAN0_DBG_TR_OUT[1]	PDMA0_TR_IN[35]	CAN0, Channel #1 P-DMA0 trigger
4	CAN0_FIFO0_TR_OUT[1]	PDMA0_TR_IN[36]	CAN0, Channel #1 FIFO0 trigger
5	CAN0_FIFO1_TR_OUT[1]	PDMA0_TR_IN[37]	CAN0, Channel #1 FIFO1 trigger
6:37	PASS0_CH_DONE_TR_OUT[0:31]	PDMA0_TR_IN[38:69]	PASS0 SAR0 to P-DMA0 direct connect
38	SMIF0_TX_TR_OUT	PDMA0_TR_IN[70]	SMIF TX to P-DMA0 Trigger
39	SMIF0_RX_TR_OUT	PDMA0_TR_IN[71]	SMIF RX to P-DMA0 Trigger
40:41	CXPI0_TX_TR_OUT[0:1]	PDMA0_TR_IN[72:73]	CXPI 0 TX P-DMA0 Triggers
42:43	CXPI0_RX_TR_OUT[0:1]	PDMA0_TR_IN[74:75]	CXPI 0 RX P-DMA0 Triggers
MUX Group 1: SCBx to P-DMA1 Triggers			
0	SCB0_TX_TR_OUT	PDMA1_TR_IN[16]	SCB0 to P-DMA1 Trigger
1	SCB0_RX_TR_OUT	PDMA1_TR_IN[17]	SCB0 to P-DMA1 Trigger
2	SCB1_TX_TR_OUT	PDMA1_TR_IN[18]	SCB1 to P-DMA1 Trigger
3	SCB1_RX_TR_OUT	PDMA1_TR_IN[19]	SCB1 to P-DMA1 Trigger
4	SCB2_TX_TR_OUT	PDMA1_TR_IN[20]	SCB2 to P-DMA1 Trigger
5	SCB2_RX_TR_OUT	PDMA1_TR_IN[21]	SCB2 to P-DMA1 Trigger
6	SCB3_TX_TR_OUT	PDMA1_TR_IN[22]	SCB3 to P-DMA1 Trigger
7	SCB3_RX_TR_OUT	PDMA1_TR_IN[23]	SCB3 to P-DMA1 Trigger
8	SCB4_TX_TR_OUT	PDMA1_TR_IN[24]	SCB4 to P-DMA1 Trigger
9	SCB4_RX_TR_OUT	PDMA1_TR_IN[25]	SCB4 to P-DMA1 Trigger
10	SCB5_TX_TR_OUT	PDMA1_TR_IN[26]	SCB5 to P-DMA1 Trigger
11	SCB5_RX_TR_OUT	PDMA1_TR_IN[27]	SCB5 to P-DMA1 Trigger
12	SCB6_TX_TR_OUT	PDMA1_TR_IN[28]	SCB6 to P-DMA1 Trigger
13	SCB6_RX_TR_OUT	PDMA1_TR_IN[29]	SCB6 to P-DMA1 Trigger
14	SCB7_TX_TR_OUT	PDMA1_TR_IN[30]	SCB7 to P-DMA1 Trigger
15	SCB7_RX_TR_OUT	PDMA1_TR_IN[31]	SCB7 to P-DMA1 Trigger
16	SCB8_TX_TR_OUT	PDMA1_TR_IN[32]	SCB8 to P-DMA1 Trigger
17	SCB8_RX_TR_OUT	PDMA1_TR_IN[33]	SCB8 to P-DMA1 Trigger
18	SCB9_TX_TR_OUT	PDMA1_TR_IN[34]	SCB9 to P-DMA1 Trigger
19	SCB9_RX_TR_OUT	PDMA1_TR_IN[35]	SCB9 to P-DMA1 Trigger
20	SCB10_TX_TR_OUT	PDMA1_TR_IN[36]	SCB10 to P-DMA1 Trigger
21	SCB10_RX_TR_OUT	PDMA1_TR_IN[37]	SCB10 to P-DMA1 Trigger
22	SCB11_TX_TR_OUT	PDMA1_TR_IN[38]	SCB11 to P-DMA1 Trigger
23	SCB11_RX_TR_OUT	PDMA1_TR_IN[39]	SCB11 to P-DMA1 Trigger
24	CAN1_DBG_TR_OUT[0]	PDMA1_TR_IN[40]	CAN1 Channel #0 P-DMA1 trigger
25	CAN1_FIFO0_TR_OUT[0]	PDMA1_TR_IN[41]	CAN1 Channel #0 FIFO0 trigger
26	CAN1_FIFO1_TR_OUT[0]	PDMA1_TR_IN[42]	CAN1 Channel #0 FIFO1 trigger
27	CAN1_DBG_TR_OUT[1]	PDMA1_TR_IN[43]	CAN1 Channel #1 P-DMA1 trigger
28	CAN1_FIFO0_TR_OUT[1]	PDMA1_TR_IN[44]	CAN1 Channel #1 FIFO0 trigger
29	CAN1_FIFO1_TR_OUT[1]	PDMA1_TR_IN[45]	CAN1 Channel #1 FIFO1 trigger

Table 20-1 Triggers 1:1 *(continued)*

Input	Trigger In	Trigger Out	Description
32:36	MIXER0_TR_SRC_REQ_OUT[0:4]	PDMA1_TR_IN[48:52]	MIXER0 to P-DMA1 trigger
37	MIXER0_TR_DST_REQ_OUT	PDMA1_TR_IN[53]	MIXER0 to P-DMA1 trigger
52:53	TDM0_TX_TR_OUT[0:1]	PDMA1_TR_IN[68:69]	TDM0 TX to P-DMA1 trigger
56:57	TDM0_RX_TR_OUT[0:1]	PDMA1_TR_IN[72:73]	TDM0 RX to P-DMA1 trigger
60:64	SG0_TX_TR_OUT[0:4]	PDMA1_TR_IN[76:80]	SG0 TX to P-DMA1 trigger
65:66	PWM0_TX_TR_OUT[0:1]	PDMA1_TR_IN[81:82]	PWM0 TX to P-DMA1 trigger
MUX Group 2: PASS SARx to TCPWM1 direct connect			
0	PASS0_CH_RANGEVIO_TR_OUT[0]	TCPWM0_16_ONE_CNT_TR_IN[0]	SAR0 ch#0[33], range violation to TCPWM0 Group#0 Counter#00 trig=2
1	PASS0_CH_RANGEVIO_TR_OUT[1]	TCPWM0_16_ONE_CNT_TR_IN[1]	SAR0 ch#1, range violation to TCPWM0 Group#0 Counter#01 trig=2
2	PASS0_CH_RANGEVIO_TR_OUT[2]	TCPWM0_16_ONE_CNT_TR_IN[2]	SAR0 ch#2, range violation to TCPWM0 Group#0 Counter#02 trig=2
3	PASS0_CH_RANGEVIO_TR_OUT[3]	TCPWM0_16_ONE_CNT_TR_IN[3]	SAR0 ch#3, range violation to TCPWM0 Group#0 Counter#03 trig=2
4	PASS0_CH_RANGEVIO_TR_OUT[4]	TCPWM0_16_ONE_CNT_TR_IN[4]	SAR0 ch#4, range violation to TCPWM0 Group#0 Counter#04 trig=2
5	PASS0_CH_RANGEVIO_TR_OUT[5]	TCPWM0_16_ONE_CNT_TR_IN[5]	SAR0 ch#5, range violation to TCPWM0 Group#0 Counter#05 trig=2
6	PASS0_CH_RANGEVIO_TR_OUT[6]	TCPWM0_16_ONE_CNT_TR_IN[6]	SAR0 ch#6, range violation to TCPWM0 Group#0 Counter#06 trig=2
7	PASS0_CH_RANGEVIO_TR_OUT[7]	TCPWM0_16_ONE_CNT_TR_IN[7]	SAR0 ch#7, range violation to TCPWM0 Group#0 Counter#07 trig=2
8	PASS0_CH_RANGEVIO_TR_OUT[8]	TCPWM0_16_ONE_CNT_TR_IN[8]	SAR0 ch#8, range violation to TCPWM0 Group#0 Counter#08 trig=2
9	PASS0_CH_RANGEVIO_TR_OUT[9]	TCPWM0_16_ONE_CNT_TR_IN[9]	SAR0 ch#9, range violation to TCPWM0 Group#0 Counter#09 trig=2
10	PASS0_CH_RANGEVIO_TR_OUT[10]	TCPWM0_16_ONE_CNT_TR_IN[10]	SAR0 ch#10, range violation to TCPWM0 Group#0 Counter#10 trig=2
11	PASS0_CH_RANGEVIO_TR_OUT[11]	TCPWM0_16_ONE_CNT_TR_IN[11]	SAR0 ch#11, range violation to TCPWM0 Group#0 Counter#11 trig=2
12	PASS0_CH_RANGEVIO_TR_OUT[12]	TCPWM0_16_ONE_CNT_TR_IN[12]	SAR0 ch#12, range violation to TCPWM0 Group#0 Counter#12 trig=2
13	PASS0_CH_RANGEVIO_TR_OUT[13]	TCPWM0_16_ONE_CNT_TR_IN[13]	SAR0 ch#13, range violation to TCPWM0 Group#0 Counter#13 trig=2
14	PASS0_CH_RANGEVIO_TR_OUT[14]	TCPWM0_16_ONE_CNT_TR_IN[14]	SAR0 ch#14, range violation to TCPWM0 Group#0 Counter#14 trig=2
15	PASS0_CH_RANGEVIO_TR_OUT[15]	TCPWM0_16_ONE_CNT_TR_IN[15]	SAR0 ch#15, range violation to TCPWM0 Group#0 Counter#15 trig=2
16	PASS0_CH_RANGEVIO_TR_OUT[16]	TCPWM0_16_ONE_CNT_TR_IN[16]	SAR0 ch#16, range violation to TCPWM0 Group#0 Counter#16 trig=2
17	PASS0_CH_RANGEVIO_TR_OUT[17]	TCPWM0_16_ONE_CNT_TR_IN[17]	SAR0 ch#17, range violation to TCPWM0 Group#0 Counter#17 trig=2
18	PASS0_CH_RANGEVIO_TR_OUT[18]	TCPWM0_16_ONE_CNT_TR_IN[18]	SAR0 ch#18, range violation to TCPWM0 Group#0 Counter#18 trig=2
19	PASS0_CH_RANGEVIO_TR_OUT[19]	TCPWM0_16_ONE_CNT_TR_IN[19]	SAR0 ch#19, range violation to TCPWM0 Group#0 Counter#19 trig=2
20	PASS0_CH_RANGEVIO_TR_OUT[20]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#20, range violation to TCPWM0 Group#1 Counter#00 trig=2
21	PASS0_CH_RANGEVIO_TR_OUT[21]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR0 ch#21, range violation to TCPWM0 Group#1 Counter#01 trig=2
22	PASS0_CH_RANGEVIO_TR_OUT[22]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR0 ch#22, range violation to TCPWM0 Group#1 Counter#02 trig=2
23	PASS0_CH_RANGEVIO_TR_OUT[23]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#23, range violation to TCPWM0 Group#1 Counter#03 trig=2
24	PASS0_CH_RANGEVIO_TR_OUT[24]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR0 ch#24, range violation to TCPWM0 Group#1 Counter#04 trig=2
25	PASS0_CH_RANGEVIO_TR_OUT[25]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR0 ch#25, range violation to TCPWM0 Group#1 Counter#05 trig=2
26	PASS0_CH_RANGEVIO_TR_OUT[26]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#26, range violation to TCPWM0 Group#1 Counter#06 trig=2
27	PASS0_CH_RANGEVIO_TR_OUT[27]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR0 ch#27, range violation to TCPWM0 Group#1 Counter#07 trig=2
28	PASS0_CH_RANGEVIO_TR_OUT[28]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR0 ch#28, range violation to TCPWM0 Group#1 Counter#08 trig=2
29	PASS0_CH_RANGEVIO_TR_OUT[29]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#29, range violation to TCPWM0 Group#1 Counter#09 trig=2
30	PASS0_CH_RANGEVIO_TR_OUT[30]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR0 ch#30, range violation to TCPWM0 Group#1 Counter#10 trig=2
31	PASS0_CH_RANGEVIO_TR_OUT[31]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR0 ch#31, range violation to TCPWM0 Group#1 Counter#11 trig=2
MUX Group 3: TCPWM0 to PASS SARx			
0:19	TCPWM0_16_TR_OUT1[0:19]	PASS0_CH_TR_IN[0:19]	TCPWM0 Group #0 Counter #00 through 19 (PWM0_0 to PWM0_19) to SAR0 ch#0 through SAR0 ch#19

Note
33.Each logical channel of SAR ADC[x] can be connected to any of the SAR ADC[x]_y external pin. (x = 0, or 1, or, 2 and y=0 to max 31)

Table 20-1 Triggers 1:1 *(continued)*

Input	Trigger In	Trigger Out	Description
20:31	TCPWM0_16M_TR_OUT1[0:11]	PASS0_CH_TR_IN[20:31]	TCPWM0 Group #1 Counter #00 through 11 (PWM0_M_0 to PWM0_M_11) to SAR0 ch#20 through SAR0 ch#31
MUX Group 4: Acknowledge triggers from P-DMA1 to CAN1			
0	PDMA1_TR_OUT[40]	CAN1_DBG_TR_ACK[0]	CAN1 Channel#0 P-DMA1 acknowledge
1	PDMA1_TR_OUT[43]	CAN1_DBG_TR_ACK[1]	CAN1 Channel#1 P-DMA1 acknowledge
MUX Group 5: Acknowledge triggers from P-DMA0 to CAN0			
0	PDMA0_TR_OUT[32]	CAN0_DBG_TR_ACK[0]	CAN0 Channel#0 P-DMA0 acknowledge
1	PDMA0_TR_OUT[35]	CAN0_DBG_TR_ACK[1]	CAN0 Channel#1 P-DMA0 acknowledge
MUX Group 6: TCPWM0 to LIN0 triggers			
0:1	TCPWM0_16_TR_OUT1[24:25]	LIN0_CMD_TR_IN[0:1]	TCPWM0 (Group #0 Counter #24 to #25) to LIN0
MUX Group 7: TCPWM0_TO_CXPI (TCPWM0 to CXPI)			
0:1	TCPWM0_16_TR_OUT1[26:27]	CXPI0_CMD_TR_IN[0:1]	TCPWM0 (Group #0 Counter #24 to #25) to CXPI0

21 Peripheral clocks

Table 21-1 Peripheral clock assignments

Output	Destination	Description
0	PCLK_CPUSS_CLOCK_TRACE_IN	Trace clock
1	PCLK_SMARTIO7_CLOCK	SMART I/O#7
2	PCLK_CANFD0_CLOCK_CAN0	CAN#0, Channel#0
3	PCLK_CANFD0_CLOCK_CAN1	CAN#0, Channel#1
4	PCLK_CANFD1_CLOCK_CAN0	CAN#1, Channel#0
5	PCLK_CANFD1_CLOCK_CAN1	CAN#1, Channel#1
6	PCLK_LIN0_CLOCK_CH_EN0	LIN#0, Channel#0
7	PCLK_LIN0_CLOCK_CH_EN1	LIN#0, Channel#1
8	PCLK_CXPI0_CLOCK_CH_EN0	CXPI#0 Channel#0
9	PCLK_CXPI0_CLOCK_CH_EN1	CXPI#0 Channel#1
10	PCLK_SCB0_CLOCK	SCB#0
11	PCLK_SCB1_CLOCK	SCB#1
12	PCLK_SCB2_CLOCK	SCB#2
13	PCLK_SCB3_CLOCK	SCB#3
14	PCLK_SCB4_CLOCK	SCB#4
15	PCLK_SCB5_CLOCK	SCB#5
16	PCLK_SCB6_CLOCK	SCB#6
17	PCLK_SCB7_CLOCK	SCB#7
18	PCLK_SCB8_CLOCK	SCB#8
19	PCLK_SCB9_CLOCK	SCB#9
20	PCLK_SCB10_CLOCK	SCB#10
21	PCLK_SCB11_CLOCK	SCB#11
22	PCLK_PASS0_CLOCK_SAR0	SAR#0
23	PCLK_LCD0_CLOCK	LCD Controller
24	PCLK_TCPWM0_CLOCKS0	TCPWM#0 Group #0, Counter #0
25	PCLK_TCPWM0_CLOCKS1	TCPWM#0 Group #0, Counter #1
26	PCLK_TCPWM0_CLOCKS2	TCPWM#0 Group #0, Counter #2
27	PCLK_TCPWM0_CLOCKS3	TCPWM#0 Group #0, Counter #3
28	PCLK_TCPWM0_CLOCKS4	TCPWM#0 Group #0, Counter #4
29	PCLK_TCPWM0_CLOCKS5	TCPWM#0 Group #0, Counter #5
30	PCLK_TCPWM0_CLOCKS6	TCPWM#0 Group #0, Counter #6
31	PCLK_TCPWM0_CLOCKS7	TCPWM#0 Group #0, Counter #7
32	PCLK_TCPWM0_CLOCKS8	TCPWM#0 Group #0, Counter #8
33	PCLK_TCPWM0_CLOCKS9	TCPWM#0 Group #0, Counter #9
34	PCLK_TCPWM0_CLOCKS10	TCPWM#0 Group #0, Counter #10
35	PCLK_TCPWM0_CLOCKS11	TCPWM#0 Group #0, Counter #11
36	PCLK_TCPWM0_CLOCKS12	TCPWM#0 Group #0, Counter #12
37	PCLK_TCPWM0_CLOCKS13	TCPWM#0 Group #0, Counter #13
38	PCLK_TCPWM0_CLOCKS14	TCPWM#0 Group #0, Counter #14
39	PCLK_TCPWM0_CLOCKS15	TCPWM#0 Group #0, Counter #15
40	PCLK_TCPWM0_CLOCKS16	TCPWM#0 Group #0, Counter #16
41	PCLK_TCPWM0_CLOCKS17	TCPWM#0 Group #0, Counter #17
42	PCLK_TCPWM0_CLOCKS18	TCPWM#0 Group #0, Counter #18
43	PCLK_TCPWM0_CLOCKS19	TCPWM#0 Group #0, Counter #19
44	PCLK_TCPWM0_CLOCKS20	TCPWM#0 Group #0, Counter #20
45	PCLK_TCPWM0_CLOCKS21	TCPWM#0 Group #0, Counter #21
46	PCLK_TCPWM0_CLOCKS22	TCPWM#0 Group #0, Counter #22
47	PCLK_TCPWM0_CLOCKS23	TCPWM#0 Group #0, Counter #23
48	PCLK_TCPWM0_CLOCKS24	TCPWM#0 Group #0, Counter #24
49	PCLK_TCPWM0_CLOCKS25	TCPWM#0 Group #0, Counter #25
50	PCLK_TCPWM0_CLOCKS26	TCPWM#0 Group #0, Counter #26
51	PCLK_TCPWM0_CLOCKS27	TCPWM#0 Group #0, Counter #27

Table 21-1 Peripheral clock assignments *(continued)*

Output	Destination	Description
52	PCLK_TCPWM0_CLOCKS28	TCPWM#0 Group #0, Counter #28
53	PCLK_TCPWM0_CLOCKS29	TCPWM#0 Group #0, Counter #29
54	PCLK_TCPWM0_CLOCKS30	TCPWM#0 Group #0, Counter #30
55	PCLK_TCPWM0_CLOCKS31	TCPWM#0 Group #0, Counter #31
56	PCLK_TCPWM0_CLOCKS32	TCPWM#0 Group #0, Counter #32
57	PCLK_TCPWM0_CLOCKS33	TCPWM#0 Group #0, Counter #33
58	PCLK_TCPWM0_CLOCKS256	TCPWM#0 Group #1, Counter #0
59	PCLK_TCPWM0_CLOCKS257	TCPWM#0 Group #1, Counter #1
60	PCLK_TCPWM0_CLOCKS258	TCPWM#0 Group #1, Counter #2
61	PCLK_TCPWM0_CLOCKS259	TCPWM#0 Group #1, Counter #3
62	PCLK_TCPWM0_CLOCKS260	TCPWM#0 Group #1, Counter #4
63	PCLK_TCPWM0_CLOCKS261	TCPWM#0 Group #1, Counter #5
64	PCLK_TCPWM0_CLOCKS262	TCPWM#0 Group #1, Counter #6
65	PCLK_TCPWM0_CLOCKS263	TCPWM#0 Group #1, Counter #7
66	PCLK_TCPWM0_CLOCKS264	TCPWM#0 Group #1, Counter #8
67	PCLK_TCPWM0_CLOCKS265	TCPWM#0 Group #1, Counter #9
68	PCLK_TCPWM0_CLOCKS266	TCPWM#0 Group #1, Counter #10
69	PCLK_TCPWM0_CLOCKS267	TCPWM#0 Group #1, Counter #11
70	PCLK_TCPWM0_CLOCKS512	TCPWM#0 Group #2, Counter #0
71	PCLK_TCPWM0_CLOCKS513	TCPWM#0 Group #2, Counter #1
72	PCLK_TCPWM0_CLOCKS514	TCPWM#0 Group #2, Counter #2
73	PCLK_TCPWM0_CLOCKS515	TCPWM#0 Group #2, Counter #3
74	PCLK_TCPWM0_CLOCKS516	TCPWM#0 Group #2, Counter #4
75	PCLK_TCPWM0_CLOCKS517	TCPWM#0 Group #2, Counter #5
76	PCLK_TCPWM0_CLOCKS518	TCPWM#0 Group #2, Counter #6
77	PCLK_TCPWM0_CLOCKS519	TCPWM#0 Group #2, Counter #7
78	PCLK_TCPWM0_CLOCKS520	TCPWM#0 Group #2, Counter #8
79	PCLK_TCPWM0_CLOCKS521	TCPWM#0 Group #2, Counter #9
80	PCLK_TCPWM0_CLOCKS522	TCPWM#0 Group #2, Counter #10
81	PCLK_TCPWM0_CLOCKS523	TCPWM#0 Group #2, Counter #11
82	PCLK_TCPWM0_CLOCKS524	TCPWM#0 Group #2, Counter #12
83	PCLK_TCPWM0_CLOCKS525	TCPWM#0 Group #2, Counter #13
84	PCLK_TCPWM0_CLOCKS526	TCPWM#0 Group #2, Counter #14
85	PCLK_TCPWM0_CLOCKS527	TCPWM#0 Group #2, Counter #15

22 Faults

Table 22-1 Fault assignments

Fault	Source	Description
0	CPUSS_MPU_VIO_0	CM0+ MPU/SMPU violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation.
1	CPUSS_MPU_VIO_1	CRYPTO SMPU violation. See CPUSS_MPU_VIO_0 description.
2	CPUSS_MPU_VIO_2	P-DMA#0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
3	CPUSS_MPU_VIO_3	P-DMA#1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
4	CPUSS_MPU_VIO_4	M-DMA#0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
15	CPUSS_MPU_VIO_15	Test Controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
16	CPUSS_MPU_VIO_16	CM4 system bus AHB-Lite interface MPU violation. See CPUSS_MPU_VIO_0 description.
17	CPUSS_MPU_VIO_17	CM4 code bus AHB-Lite interface MPU violation for non flash controller accesses. See CPUSS_MPU_VIO_0 description.
18	CPUSS_MPU_VIO_18	CM4 code bus AHB-Lite interface MPU violation for flash controller accesses. See CPUSS_MPU_VIO_0 description.
26	PERI_PERI_C_ECC	Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word.
27	PERI_PERI_NC_ECC	Peripheral protection SRAM non-correctable ECC violation
28	PERI_MS_VIO_0	CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: master interface, PPU violation, “1': timeout detected, “2”: bus error, other: undefined.
29	PERI_MS_VIO_1	CM4 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
30	PERI_MS_VIO_2	P-DMA0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
31	PERI_MS_VIO_3	P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
32	PERI_GROUP_VIO_0	Peripheral group #0 violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: decoder or peripheral bus error, other: undefined.
33	PERI_GROUP_VIO_1	Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description.
34	PERI_GROUP_VIO_2	Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description.
35	PERI_GROUP_VIO_3	Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description.
36	PERI_GROUP_VIO_4	Peripheral Group #4 violation. See PERI_GROUP_VIO_0 description.
37	PERI_GROUP_VIO_5	Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description.
38	PERI_GROUP_VIO_6	Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description.

Table 22-1 Fault assignments *(continued)*

Fault	Source	Description
40	PERI_GROUP_VIO_8	Peripheral Group #8 violation. See PERI_GROUP_VIO_0 description.
41	PERI_GROUP_VIO_9	Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description.
48	CPUSS_FLASHC_MAIN_BUS_ERROR	Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
49	CPUSS_FLASHC_MAIN_C_ECC	Flash controller main flash correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).
50	CPUSS_FLASHC_MAIN_NC_ECC	Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description.
51	CPUSS_FLASHC_WORK_BUS_ERROR	Flash controller work flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
52	CPUSS_FLASHC_WORK_C_ECC	Flash controller work flash correctable ECC violation DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word.
53	CPUSS_FLASHC_WORK_NC_ECC	Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description.
54	CPUSS_FLASHC_CM0_CA_C_ECC	Flash controller CM0+ cache correctable ECC violation DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xC).
55	CPUSS_FLASHC_CM0_CA_NC_ECC	Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
56	CPUSS_FLASHC_CM4_CA_C_ECC	Flash controller CM4 cache correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
57	CPUSS_FLASHC_CM4_CA_NC_ECC	Flash controller CM4 cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
58	CPUSS_RAMC0_C_ECC	System memory controller 0 correctable ECC violation DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word.
59	CPUSS_RAMC0_NC_ECC	System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
60	CPUSS_RAMC1_C_ECC	System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
61	CPUSS_RAMC1_NC_ECC	System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
64	CPUSS_CRYPTO_C_ECC	Crypto memory correctable ECC violation DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.
65	CPUSS_CRYPTO_NC_ECC	CRYPTO memory non-correctable ECC violation. See CPUSS_CRYPTO_C_ECC description.
70	CPUSS_DW0_C_ECC	Datawire0 memory correctable ECC violation DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word.
71	CPUSS_DW0_NC_ECC	P-DMA#0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
72	CPUSS_DW1_C_ECC	P-DMA#1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description.
73	CPUSS_DW1_NC_ECC	P-DMA#1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
74	CPUSS_FM_SRAM_C_ECC	Flash code storage SRAM memory correctable ECC violation DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word.
75	CPUSS_FM_SRAM_NC_ECC	Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description.

Table 22-1 Fault assignments *(continued)*

Fault	Source	Description
80	CANFD_0_CAN_C_ECC	CAN#0 message buffer correctable ECC violation DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.
81	CANFD_0_CAN_NC_ECC	CAN#0 message buffer non-correctable ECC violation DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).
82	CANFD_1_CAN_C_ECC	CAN#1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description.
83	CANFD_1_CAN_NC_ECC	CAN#1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description.
90	SRSS_FAULT_CSV	Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CSV violation occurred on corresponding CLK_HF* root clock DATA0[24]: CSV violation occurred on reference clock for CLK_HF CSVs DATA0[25]: CSV violation occurred on CLK_LF DATA0[26]: CSV violation occurred on CLK_ILO0 DATA0[27]: CSV violation occurred on CLK_BAK
91	SRSS_FAULT_SSV	Consolidated fault output for supply supervisors. Multiple counters can detect a violation at the same time. DATA0[0]: BOD detected on VDDA_ADC DATA0[1]: OVD detected on VDDA_ADC DATA0[16]: violation detected on LVD/HVD #1 DATA0[17]: violation detected on LVD/HVD #2
92	SRSS_FAULT_MCWDT0	Fault output for MCWDT#0 (all sub-counters). Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT
93	SRSS_FAULT_MCWDT1	Fault output for MCWDT#1 (all sub-counters). See SRSS_FAULT_MCWDT#0 description.

23 Peripheral protection unit fixed structure pairs

Protection pair is a pair PPU structures, a master and a slave structure. The master structure protects the slave structure, and the slave structure protects resources such as peripheral registers, or the peripheral itself.

Table 23-1 PPU fixed structure pairs

Pair No.	PPU fixed structure pair	Address	Size	Description
0	PERI_MAIN	0x40000000	0x00002000	Peripheral Interconnect main
1	PERI_SECURE	0x40002000	0x00000004	Peripheral interconnect secure
2	PERI_GR0_GROUP	0x40004010	0x00000004	Peripheral Group #0 main
3	PERI_GR1_GROUP	0x40004030	0x00000004	Peripheral Group #1 main
4	PERI_GR2_GROUP	0x40004050	0x00000004	Peripheral Group #2 main
5	PERI_GR3_GROUP	0x40004060	0x00000020	Peripheral Group #3 main
6	PERI_GR4_GROUP	0x40004080	0x00000020	Peripheral Group #4 main
7	PERI_GR5_GROUP	0x400040A0	0x00000020	Peripheral Group #5 main
8	PERI_GR6_GROUP	0x400040C0	0x00000020	Peripheral Group #6 main
9	PERI_GR8_GROUP	0x40004100	0x00000020	Peripheral Group #8 main
10	PERI_GR9_GROUP	0x40004120	0x00000020	Peripheral Group #9 main
11	PERI_TR	0x40008000	0x00008000	Peripheral trigger multiplexer
12	CRYPTO_MAIN	0x40100000	0x00000400	Crypto main
13	CRYPTO_CRYPTO	0x40101000	0x00000800	Crypto MMIO (Memory Mapped I/O)
14	CRYPTO_BOOT	0x40102000	0x00000100	Crypto boot
15	CRYPTO_KEY0	0x40102100	0x00000004	Crypto Key #0
16	CRYPTO_KEY1	0x40102120	0x00000004	Crypto Key #1
17	CRYPTO_BUF	0x40108000	0x00002000	Crypto buffer
18	CPUSS_CM4	0x40200000	0x00000400	CM4 CPU core
19	CPUSS_CM0	0x40201000	0x00001000	CM0+ CPU core
20	CPUSS_BOOT[34]	0x40202000	0x00000200	CPUSS boot
21	CPUSS_CM0_INT	0x40208000	0x00001000	CPUSS CM0+ interrupts
22	CPUSS_CM4_INT	0x4020A000	0x00001000	CPUSS CM4 interrupts
23	FAULT_STRUCT0_MAIN	0x40210000	0x00000100	CPUSS Fault Structure #0 main
24	FAULT_STRUCT1_MAIN	0x40210100	0x00000100	CPUSS Fault Structure #1 main
25	FAULT_STRUCT2_MAIN	0x40210200	0x00000100	CPUSS Fault Structure #2 main
26	FAULT_STRUCT3_MAIN	0x40210300	0x00000100	CPUSS Fault Structure #3 main
27	IPC_STRUCT0_IPC	0x40220000	0x00000020	CPUSS IPC Structure #0
28	IPC_STRUCT1_IPC	0x40220020	0x00000020	CPUSS IPC Structure #1
29	IPC_STRUCT2_IPC	0x40220040	0x00000020	CPUSS IPC Structure #2
30	IPC_STRUCT3_IPC	0x40220060	0x00000020	CPUSS IPC Structure #3
31	IPC_STRUCT4_IPC	0x40220080	0x00000020	CPUSS IPC Structure #4
32	IPC_STRUCT5_IPC	0x402200A0	0x00000020	CPUSS IPC Structure #5
33	IPC_STRUCT6_IPC	0x402200C0	0x00000020	CPUSS IPC Structure #6
34	IPC_STRUCT7_IPC	0x402200E0	0x00000020	CPUSS IPC Structure #7
35	IPC_INTR_STRUCT0_INTR	0x40221000	0x00000010	CPUSS IPC Interrupt Structure #0
36	IPC_INTR_STRUCT1_INTR	0x40221020	0x00000010	CPUSS IPC Interrupt Structure #1
37	IPC_INTR_STRUCT2_INTR	0x40221040	0x00000010	CPUSS IPC Interrupt Structure #2
38	IPC_INTR_STRUCT3_INTR	0x40221060	0x00000010	CPUSS IPC Interrupt Structure #3

Note
34.Fixed PPU is configured inside the Boot and user is not allowed to change the attributes of this PPU.

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
39	IPC_INTR_STRUCT4_INTR	0x40221080	0x00000010	CPUSS IPC Interrupt Structure #4
40	IPC_INTR_STRUCT5_INTR	0x402210A0	0x00000010	CPUSS IPC Interrupt Structure #5
41	IPC_INTR_STRUCT6_INTR	0x402210C0	0x00000010	CPUSS IPC Interrupt Structure #6
42	IPC_INTR_STRUCT7_INTR	0x402210E0	0x00000010	CPUSS IPC Interrupt Structure #7
43	PROT_SMPU_MAIN	0x40230000	0x00000040	Peripheral protection SMPU main
44	PROT_MPU0_MAIN	0x40234000	0x00000004	Peripheral protection MPU #0 main
45	PROT_MPU14_MAIN	0x40237800	0x00000004	Peripheral protection MPU #14 main
46	PROT_MPU15_MAIN	0x40237C00	0x00000400	Peripheral protection MPU #15 main
47	FLASHC_MAIN	0x40240000	0x00000008	Flash controller main
48	FLASHC_CMD	0x40240008	0x00000004	Flash controller command
49	FLASHC_DFT	0x40240200	0x00000100	Flash controller tests
50	FLASHC_CM0	0x40240400	0x00000080	Flash controller CM0+
51	FLASHC_CM4	0x40240480	0x00000080	Flash controller CM4
52	FLASHC_CRYPTO	0x40240500	0x00000004	Flash controller Crypto
53	FLASHC_DW0	0x40240580	0x00000004	Flash controller P-DMA#0
54	FLASHC_DW1	0x40240600	0x00000004	Flash controller P-DMA#1
55	FLASHC_DMAC	0x40240680	0x00000004	Flash controller M-DMA#0
56	FLASHC_FlashMgmt[34]	0x4024F000	0x00000080	Flash management
57	FLASHC_MainSafety	0x4024F400	0x00000008	Flash controller main safety
58	FLASHC_WorkSafety	0x4024F500	0x00000004	Flash controller work safety
59	SRSS_GENERAL	0x40260000	0x00000400	SRSS General
60	SRSS_MAIN	0x40261000	0x00001000	SRSS main
61	SRSS_SECURE	0x40262000	0x00002000	SRSS secure
62	MCWDT0_CONFIG	0x40268000	0x00000080	MCWDT #0 configuration
63	MCWDT1_CONFIG	0x40268100	0x00000080	MCWDT #1 configuration
64	MCWDT0_MAIN	0x40268080	0x00000040	MCWDT #0 main
65	MCWDT1_MAIN	0x40268180	0x00000040	MCWDT #1 main
66	WDT_CONFIG	0x4026C000	0x00000020	System WDT configuration
67	WDT_MAIN	0x4026C040	0x00000020	System WDT main
68	BACKUP_BACKUP	0x40270000	0x00010000	SRSS backup
69	DW0_DW	0x40280000	0x00000100	P-DMA#0 main
70	DW1_DW	0x40290000	0x00000100	P-DMA#1 main
71	DW0_DW_CRC	0x40280100	0x00000080	P-DMA#0 CRC
72	DW1_DW_CRC	0x40290100	0x00000080	P-DMA#1 CRC
73	DW0_CH_STRUCT0_CH	0x40288000	0x00000040	P-DMA#0 Channel #0
74	DW0_CH_STRUCT1_CH	0x40288040	0x00000040	P-DMA#0 Channel #1
75	DW0_CH_STRUCT2_CH	0x40288080	0x00000040	P-DMA#0 Channel #2
76	DW0_CH_STRUCT3_CH	0x402880C0	0x00000040	P-DMA#0 Channel #3
77	DW0_CH_STRUCT4_CH	0x40288100	0x00000040	P-DMA#0 Channel #4
78	DW0_CH_STRUCT5_CH	0x40288140	0x00000040	P-DMA#0 Channel #5
79	DW0_CH_STRUCT6_CH	0x40288180	0x00000040	P-DMA#0 Channel #6
80	DW0_CH_STRUCT7_CH	0x402881C0	0x00000040	P-DMA#0 Channel #7
81	DW0_CH_STRUCT8_CH	0x40288200	0x00000040	P-DMA#0 Channel #8
82	DW0_CH_STRUCT9_CH	0x40288240	0x00000040	P-DMA#0 Channel #9
83	DW0_CH_STRUCT10_CH	0x40288280	0x00000040	P-DMA#0 Channel #10

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
84	DW0_CH_STRUCT11_CH	0x402882C0	0x00000040	P-DMA#0 Channel #11
85	DW0_CH_STRUCT12_CH	0x40288300	0x00000040	P-DMA#0 Channel #12
86	DW0_CH_STRUCT13_CH	0x40288340	0x00000040	P-DMA#0 Channel #13
87	DW0_CH_STRUCT14_CH	0x40288380	0x00000040	P-DMA#0 Channel #14
88	DW0_CH_STRUCT15_CH	0x402883C0	0x00000040	P-DMA#0 Channel #15
89	DW0_CH_STRUCT16_CH	0x40288400	0x00000040	P-DMA#0 Channel #16
90	DW0_CH_STRUCT17_CH	0x40288440	0x00000040	P-DMA#0 Channel #17
91	DW0_CH_STRUCT18_CH	0x40288480	0x00000040	P-DMA#0 Channel #18
92	DW0_CH_STRUCT19_CH	0x402884C0	0x00000040	P-DMA#0 Channel #19
93	DW0_CH_STRUCT20_CH	0x40288500	0x00000040	P-DMA#0 Channel #20
94	DW0_CH_STRUCT21_CH	0x40288540	0x00000040	P-DMA#0 Channel #21
95	DW0_CH_STRUCT22_CH	0x40288580	0x00000040	P-DMA#0 Channel #22
96	DW0_CH_STRUCT23_CH	0x402885C0	0x00000040	P-DMA#0 Channel #23
97	DW0_CH_STRUCT24_CH	0x40288600	0x00000040	P-DMA#0 Channel #24
98	DW0_CH_STRUCT25_CH	0x40288640	0x00000040	P-DMA#0 Channel #25
99	DW0_CH_STRUCT26_CH	0x40288680	0x00000040	P-DMA#0 Channel #26
100	DW0_CH_STRUCT27_CH	0x402886C0	0x00000040	P-DMA#0 Channel #27
101	DW0_CH_STRUCT28_CH	0x40288700	0x00000040	P-DMA#0 Channel #28
102	DW0_CH_STRUCT29_CH	0x40288740	0x00000040	P-DMA#0 Channel #29
103	DW0_CH_STRUCT30_CH	0x40288780	0x00000040	P-DMA#0 Channel #30
104	DW0_CH_STRUCT31_CH	0x402887C0	0x00000040	P-DMA#0 Channel #31
105	DW0_CH_STRUCT32_CH	0x40288800	0x00000040	P-DMA#0 Channel #32
106	DW0_CH_STRUCT33_CH	0x40288840	0x00000040	P-DMA#0 Channel #33
107	DW0_CH_STRUCT34_CH	0x40288880	0x00000040	P-DMA#0 Channel #34
108	DW0_CH_STRUCT35_CH	0x402888C0	0x00000040	P-DMA#0 Channel #35
109	DW0_CH_STRUCT36_CH	0x40288900	0x00000040	P-DMA#0 Channel #36
110	DW0_CH_STRUCT37_CH	0x40288940	0x00000040	P-DMA#0 Channel #37
111	DW0_CH_STRUCT38_CH	0x40288980	0x00000040	P-DMA#0 Channel #38
112	DW0_CH_STRUCT39_CH	0x402889C0	0x00000040	P-DMA#0 Channel #39
113	DW0_CH_STRUCT40_CH	0x40288A00	0x00000040	P-DMA#0 Channel #40
114	DW0_CH_STRUCT41_CH	0x40288A40	0x00000040	P-DMA#0 Channel #41
115	DW0_CH_STRUCT42_CH	0x40288A80	0x00000040	P-DMA#0 Channel #42
116	DW0_CH_STRUCT43_CH	0x40288AC0	0x00000040	P-DMA#0 Channel #43
117	DW0_CH_STRUCT44_CH	0x40288B00	0x00000040	P-DMA#0 Channel #44
118	DW0_CH_STRUCT45_CH	0x40288B40	0x00000040	P-DMA#0 Channel #45
119	DW0_CH_STRUCT46_CH	0x40288B80	0x00000040	P-DMA#0 Channel #46
120	DW0_CH_STRUCT47_CH	0x40288BC0	0x00000040	P-DMA#0 Channel #47
121	DW0_CH_STRUCT48_CH	0x40288C00	0x00000040	P-DMA#0 Channel #48
122	DW0_CH_STRUCT49_CH	0x40288C40	0x00000040	P-DMA#0 Channel #49
123	DW0_CH_STRUCT50_CH	0x40288C80	0x00000040	P-DMA#0 Channel #50
124	DW0_CH_STRUCT51_CH	0x40288CC0	0x00000040	P-DMA#0 Channel #51
125	DW0_CH_STRUCT52_CH	0x40288D00	0x00000040	P-DMA#0 Channel #52
126	DW0_CH_STRUCT53_CH	0x40288D40	0x00000040	P-DMA#0 Channel #53
127	DW0_CH_STRUCT54_CH	0x40288D80	0x00000040	P-DMA#0 Channel #54
128	DW0_CH_STRUCT55_CH	0x40288DC0	0x00000040	P-DMA#0 Channel #55

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
129	DW0_CH_STRUCT56_CH	0x40288E00	0x00000040	P-DMA#0 Channel #56
130	DW0_CH_STRUCT57_CH	0x40288E40	0x00000040	P-DMA#0 Channel #57
131	DW0_CH_STRUCT58_CH	0x40288E80	0x00000040	P-DMA#0 Channel #58
132	DW0_CH_STRUCT59_CH	0x40288EC0	0x00000040	P-DMA#0 Channel #59
133	DW0_CH_STRUCT60_CH	0x40288F00	0x00000040	P-DMA#0 Channel #60
134	DW0_CH_STRUCT61_CH	0x40288F40	0x00000040	P-DMA#0 Channel #61
135	DW0_CH_STRUCT62_CH	0x40288F80	0x00000040	P-DMA#0 Channel #62
136	DW0_CH_STRUCT63_CH	0x40288FC0	0x00000040	P-DMA#0 Channel #63
137	DW0_CH_STRUCT64_CH	0x40289000	0x00000040	P-DMA#0 Channel #64
138	DW0_CH_STRUCT65_CH	0x40289040	0x00000040	P-DMA#0 Channel #65
139	DW0_CH_STRUCT66_CH	0x40289080	0x00000040	P-DMA#0 Channel #66
140	DW0_CH_STRUCT67_CH	0x402890C0	0x00000040	P-DMA#0 Channel #67
141	DW0_CH_STRUCT68_CH	0x40289100	0x00000040	P-DMA#0 Channel #68
142	DW0_CH_STRUCT69_CH	0x40289140	0x00000040	P-DMA#0 Channel #69
143	DW0_CH_STRUCT70_CH	0x40289180	0x00000040	P-DMA#0 Channel #70
144	DW0_CH_STRUCT71_CH	0x402891C0	0x00000040	P-DMA#0 Channel #71
145	DW0_CH_STRUCT72_CH	0x40289200	0x00000040	P-DMA#0 Channel #72
146	DW0_CH_STRUCT73_CH	0x40289240	0x00000040	P-DMA#0 Channel #73
147	DW0_CH_STRUCT74_CH	0x40289280	0x00000040	P-DMA#0 Channel #74
148	DW0_CH_STRUCT75_CH	0x402892C0	0x00000040	P-DMA#0 Channel #75
149	DW1_CH_STRUCT0_CH	0x40298000	0x00000040	P-DMA#1 Channel #0
150	DW1_CH_STRUCT1_CH	0x40298040	0x00000040	P-DMA#1 Channel #1
151	DW1_CH_STRUCT2_CH	0x40298080	0x00000040	P-DMA#1 Channel #2
152	DW1_CH_STRUCT3_CH	0x402980C0	0x00000040	P-DMA#1 Channel #3
153	DW1_CH_STRUCT4_CH	0x40298100	0x00000040	P-DMA#1 Channel #4
154	DW1_CH_STRUCT5_CH	0x40298140	0x00000040	P-DMA#1 Channel #5
155	DW1_CH_STRUCT6_CH	0x40298180	0x00000040	P-DMA#1 Channel #6
156	DW1_CH_STRUCT7_CH	0x402981C0	0x00000040	P-DMA#1 Channel #7
157	DW1_CH_STRUCT8_CH	0x40298200	0x00000040	P-DMA#1 Channel #8
158	DW1_CH_STRUCT9_CH	0x40298240	0x00000040	P-DMA#1 Channel #9
159	DW1_CH_STRUCT10_CH	0x40298280	0x00000040	P-DMA#1 Channel #10
160	DW1_CH_STRUCT11_CH	0x402982C0	0x00000040	P-DMA#1 Channel #11
161	DW1_CH_STRUCT12_CH	0x40298300	0x00000040	P-DMA#1 Channel #12
162	DW1_CH_STRUCT13_CH	0x40298340	0x00000040	P-DMA#1 Channel #13
163	DW1_CH_STRUCT14_CH	0x40298380	0x00000040	P-DMA#1 Channel #14
164	DW1_CH_STRUCT15_CH	0x402983C0	0x00000040	P-DMA#1 Channel #15
165	DW1_CH_STRUCT16_CH	0x40298400	0x00000040	P-DMA#1 Channel #16
166	DW1_CH_STRUCT17_CH	0x40298440	0x00000040	P-DMA#1 Channel #17
167	DW1_CH_STRUCT18_CH	0x40298480	0x00000040	P-DMA#1 Channel #18
168	DW1_CH_STRUCT19_CH	0x402984C0	0x00000040	P-DMA#1 Channel #19
169	DW1_CH_STRUCT20_CH	0x40298500	0x00000040	P-DMA#1 Channel #20
170	DW1_CH_STRUCT21_CH	0x40298540	0x00000040	P-DMA#1 Channel #21
171	DW1_CH_STRUCT22_CH	0x40298580	0x00000040	P-DMA#1 Channel #22
172	DW1_CH_STRUCT23_CH	0x402985C0	0x00000040	P-DMA#1 Channel #23
173	DW1_CH_STRUCT24_CH	0x40298600	0x00000040	P-DMA#1 Channel #24

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
174	DW1_CH_STRUCT25_CH	0x40298640	0x00000040	P-DMA#1 Channel #25
175	DW1_CH_STRUCT26_CH	0x40298680	0x00000040	P-DMA#1 Channel #26
176	DW1_CH_STRUCT27_CH	0x402986C0	0x00000040	P-DMA#1 Channel #27
177	DW1_CH_STRUCT28_CH	0x40298700	0x00000040	P-DMA#1 Channel #28
178	DW1_CH_STRUCT29_CH	0x40298740	0x00000040	P-DMA#1 Channel #29
179	DW1_CH_STRUCT30_CH	0x40298780	0x00000040	P-DMA#1 Channel #30
180	DW1_CH_STRUCT31_CH	0x402987C0	0x00000040	P-DMA#1 Channel #31
181	DW1_CH_STRUCT32_CH	0x40298800	0x00000040	P-DMA#1 Channel #32
182	DW1_CH_STRUCT33_CH	0x40298840	0x00000040	P-DMA#1 Channel #33
183	DW1_CH_STRUCT34_CH	0x40298880	0x00000040	P-DMA#1 Channel #34
184	DW1_CH_STRUCT35_CH	0x402988C0	0x00000040	P-DMA#1 Channel #35
185	DW1_CH_STRUCT36_CH	0x40298900	0x00000040	P-DMA#1 Channel #36
186	DW1_CH_STRUCT37_CH	0x40298940	0x00000040	P-DMA#1 Channel #37
187	DW1_CH_STRUCT38_CH	0x40298980	0x00000040	P-DMA#1 Channel #38
188	DW1_CH_STRUCT39_CH	0x402989C0	0x00000040	P-DMA#1 Channel #39
189	DW1_CH_STRUCT40_CH	0x40298A00	0x00000040	P-DMA#1 Channel #40
190	DW1_CH_STRUCT41_CH	0x40298A40	0x00000040	P-DMA#1 Channel #41
191	DW1_CH_STRUCT42_CH	0x40298A80	0x00000040	P-DMA#1 Channel #42
192	DW1_CH_STRUCT43_CH	0x40298AC0	0x00000040	P-DMA#1 Channel #43
193	DW1_CH_STRUCT44_CH	0x40298B00	0x00000040	P-DMA#1 Channel #44
194	DW1_CH_STRUCT45_CH	0x40298B40	0x00000040	P-DMA#1 Channel #45
195	DW1_CH_STRUCT46_CH	0x40298B80	0x00000040	P-DMA#1 Channel #46
196	DW1_CH_STRUCT47_CH	0x40298BC0	0x00000040	P-DMA#1 Channel #47
197	DW1_CH_STRUCT48_CH	0x40298C00	0x00000040	P-DMA#1 Channel #48
198	DW1_CH_STRUCT49_CH	0x40298C40	0x00000040	P-DMA#1 Channel #49
199	DW1_CH_STRUCT50_CH	0x40298C80	0x00000040	P-DMA#1 Channel #50
200	DW1_CH_STRUCT51_CH	0x40298CC0	0x00000040	P-DMA#1 Channel #51
201	DW1_CH_STRUCT52_CH	0x40298D00	0x00000040	P-DMA#1 Channel #52
202	DW1_CH_STRUCT53_CH	0x40298D40	0x00000040	P-DMA#1 Channel #53
203	DW1_CH_STRUCT54_CH	0x40298D80	0x00000040	P-DMA#1 Channel #54
204	DW1_CH_STRUCT55_CH	0x40298DC0	0x00000040	P-DMA#1 Channel #55
205	DW1_CH_STRUCT56_CH	0x40298E00	0x00000040	P-DMA#1 Channel #56
206	DW1_CH_STRUCT57_CH	0x40298E40	0x00000040	P-DMA#1 Channel #57
207	DW1_CH_STRUCT58_CH	0x40298E80	0x00000040	P-DMA#1 Channel #58
208	DW1_CH_STRUCT59_CH	0x40298EC0	0x00000040	P-DMA#1 Channel #59
209	DW1_CH_STRUCT60_CH	0x40298F00	0x00000040	P-DMA#1 Channel #60
210	DW1_CH_STRUCT61_CH	0x40298F40	0x00000040	P-DMA#1 Channel #61
211	DW1_CH_STRUCT62_CH	0x40298F80	0x00000040	P-DMA#1 Channel #62
212	DW1_CH_STRUCT63_CH	0x40298FC0	0x00000040	P-DMA#1 Channel #63
213	DW1_CH_STRUCT64_CH	0x40299000	0x00000040	P-DMA#1 Channel #64
214	DW1_CH_STRUCT65_CH	0x40299040	0x00000040	P-DMA#1 Channel #65
215	DW1_CH_STRUCT66_CH	0x40299080	0x00000040	P-DMA#1 Channel #66
216	DW1_CH_STRUCT67_CH	0x402990C0	0x00000040	P-DMA#1 Channel #67
217	DW1_CH_STRUCT68_CH	0x40299100	0x00000040	P-DMA#1 Channel #68
218	DW1_CH_STRUCT69_CH	0x40299140	0x00000040	P-DMA#1 Channel #69

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
219	DW1_CH_STRUCT70_CH	0x40299180	0x00000040	P-DMA#1 Channel #70
220	DW1_CH_STRUCT71_CH	0x402991C0	0x00000040	P-DMA#1 Channel #71
221	DW1_CH_STRUCT72_CH	0x40299200	0x00000040	P-DMA#1 Channel #72
222	DW1_CH_STRUCT73_CH	0x40299240	0x00000040	P-DMA#1 Channel #73
223	DW1_CH_STRUCT74_CH	0x40299280	0x00000040	P-DMA#1 Channel #74
224	DW1_CH_STRUCT75_CH	0x402992C0	0x00000040	P-DMA#1 Channel #75
225	DW1_CH_STRUCT76_CH	0x40299300	0x00000040	P-DMA#1 Channel #76
226	DW1_CH_STRUCT77_CH	0x40299340	0x00000040	P-DMA#1 Channel #77
227	DW1_CH_STRUCT78_CH	0x40299380	0x00000040	P-DMA#1 Channel #78
228	DW1_CH_STRUCT79_CH	0x402993C0	0x00000040	P-DMA#1 Channel #79
229	DW1_CH_STRUCT80_CH	0x40299400	0x00000040	P-DMA#1 Channel #80
230	DW1_CH_STRUCT81_CH	0x40299440	0x00000040	P-DMA#1 Channel #81
231	DW1_CH_STRUCT82_CH	0x40299480	0x00000040	P-DMA#1 Channel #82
232	DW1_CH_STRUCT83_CH	0x402994C0	0x00000040	P-DMA#1 Channel #83
233	DMAC_TOP	0x402A0000	0x00000010	M-DMA#0 main
234	DMAC_CH0_CH	0x402A1000	0x00000100	M-DMA#0 Channel #0
235	DMAC_CH1_CH	0x402A1100	0x00000100	M-DMA#0 Channel #1
236	DMAC_CH2_CH	0x402A1200	0x00000100	M-DMA#0 Channel #2
237	DMAC_CH3_CH	0x402A1300	0x00000100	M-DMA#0 Channel #3
238	EFUSE_CTL	0x402C0000	0x00000200	EFUSE control
239	EFUSE_DATA	0x402C0800	0x00000200	EFUSE data
240	BIST	0x402F0000	0x00001000	Built-in self test
241	HSIOM_PRT0_PRT	0x40300000	0x00000008	HSIOm Port #0
242	HSIOM_PRT1_PRT	0x40300010	0x00000008	HSIOm Port #1
243	HSIOM_PRT2_PRT	0x40300020	0x00000008	HSIOm Port #2
244	HSIOM_PRT3_PRT	0x40300030	0x00000008	HSIOm Port #3
245	HSIOM_PRT4_PRT	0x40300040	0x00000008	HSIOm Port #4
246	HSIOM_PRT5_PRT	0x40300050	0x00000008	HSIOm Port #5
247	HSIOM_PRT6_PRT	0x40300060	0x00000008	HSIOm Port #6
248	HSIOM_PRT7_PRT	0x40300070	0x00000008	HSIOm Port #7
249	HSIOM_PRT8_PRT	0x40300080	0x00000008	HSIOm Port #8
250	HSIOM_PRT9_PRT	0x40300090	0x00000008	HSIOm Port #9
251	HSIOM_PRT10_PRT	0x403000A0	0x00000008	HSIOm Port #10
252	HSIOM_PRT11_PRT	0x403000B0	0x00000008	HSIOm Port #11
253	HSIOM_PRT12_PRT	0x403000C0	0x00000008	HSIOm Port #12
254	HSIOM_PRT13_PRT	0x403000D0	0x00000008	HSIOm Port #13
255	HSIOM_PRT14_PRT	0x403000E0	0x00000008	HSIOm Port #14
256	HSIOM_PRT15_PRT	0x403000F0	0x00000008	HSIOm Port #15
257	HSIOM_PRT16_PRT	0x40300100	0x00000008	HSIOm Port #16
258	HSIOM_PRT17_PRT	0x40300110	0x00000008	HSIOm Port #17
259	HSIOM_PRT18_PRT	0x40300120	0x00000008	HSIOm Port #18
260	HSIOM_PRT19_PRT	0x40300130	0x00000008	HSIOm Port #19
261	HSIOM_AMUX	0x40302000	0x00000010	HSIOm Analog multiplexer
262	HSIOM_MON	0x40302200	0x00000010	HSIOm monitor
263	GPIO_PRT0_PRT	0x40310000	0x00000040	GPIO_STD Port #0

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
264	GPIO_PRT1_PRT	0x40310080	0x00000040	GPIO_STD Port #1
265	GPIO_PRT2_PRT	0x40310100	0x00000040	GPIO_STD Port #2
266	GPIO_PRT3_PRT	0x40310180	0x00000040	GPIO_STD Port #3
267	GPIO_PRT4_PRT	0x40310200	0x00000040	GPIO_STD Port #4
268	GPIO_PRT5_PRT	0x40310280	0x00000040	GPIO_SMC Port #5
269	GPIO_PRT6_PRT	0x40310300	0x00000040	GPIO_SMC Port #6
270	GPIO_PRT7_PRT	0x40310380	0x00000040	GPIO_SMC Port #7
271	GPIO_PRT8_PRT	0x40310400	0x00000040	HSIO_STDLN Port #8
272	GPIO_PRT9_PRT	0x40310480	0x00000040	HSIO_STDLN Port #9
273	GPIO_PRT10_PRT	0x40310500	0x00000040	GPIO_STD Port #10
274	GPIO_PRT11_PRT	0x40310580	0x00000040	GPIO_STD Port #11
275	GPIO_PRT12_PRT	0x40310600	0x00000040	GPIO_STD Port #12
276	GPIO_PRT13_PRT	0x40310680	0x00000040	GPIO_STD Port #13
277	GPIO_PRT14_PRT	0x40310700	0x00000040	GPIO_ENH Port #14
278	GPIO_PRT15_PRT	0x40310780	0x00000040	GPIO_STD Port #15
279	GPIO_PRT16_PRT	0x40310800	0x00000040	GPIO_STD Port #16
280	GPIO_PRT17_PRT	0x40310880	0x00000040	GPIO_STD Port #17
281	GPIO_PRT18_PRT	0x40310900	0x00000040	GPIO_STD Port #18
282	GPIO_PRT19_PRT	0x40310980	0x00000040	GPIO_STD Port #19
283	GPIO_PRT0_CFG	0x40310040	0x00000020	GPIO_STD Port #0 configuration
284	GPIO_PRT1_CFG	0x403100C0	0x00000020	GPIO_STD Port #1 configuration
285	GPIO_PRT2_CFG	0x40310140	0x00000020	GPIO_STD Port #2 configuration
286	GPIO_PRT3_CFG	0x403101C0	0x00000020	GPIO_STD Port #3 configuration
287	GPIO_PRT4_CFG	0x40310240	0x00000020	GPIO_STD Port #4 configuration
288	GPIO_PRT5_CFG	0x403102C0	0x00000020	GPIO_SMC Port #5 configuration
289	GPIO_PRT6_CFG	0x40310340	0x00000020	GPIO_SMC Port #6 configuration
290	GPIO_PRT7_CFG	0x403103C0	0x00000020	GPIO_SMC Port #7 configuration
291	GPIO_PRT8_CFG	0x40310440	0x00000040	HSIO_STDLN Port #8 configuration
292	GPIO_PRT9_CFG	0x403104C0	0x00000040	HSIO_STDLN Port #9 configuration
293	GPIO_PRT10_CFG	0x40310540	0x00000020	GPIO_STD Port #10 configuration
294	GPIO_PRT11_CFG	0x403105C0	0x00000020	GPIO_STD Port #11 configuration
295	GPIO_PRT12_CFG	0x40310640	0x00000020	GPIO_STD Port #12 configuration
296	GPIO_PRT13_CFG	0x403106C0	0x00000020	GPIO_STD Port #13 configuration
297	GPIO_PRT14_CFG	0x40310740	0x00000020	GPIO_ENH Port #14 configuration
298	GPIO_PRT15_CFG	0x403107C0	0x00000020	GPIO_STD Port #15 configuration
299	GPIO_PRT16_CFG	0x40310840	0x00000020	GPIO_STD Port #16 configuration
300	GPIO_PRT17_CFG	0x403108C0	0x00000020	GPIO_STD Port #17 configuration
301	GPIO_PRT18_CFG	0x40310940	0x00000020	GPIO_STD Port #18 configuration
302	GPIO_PRT19_CFG	0x403109C0	0x00000020	GPIO_STD Port #19 configuration
303	GPIO_GPIO	0x40314000	0x00000040	GPIO main
304	GPIO_TEST	0x40315000	0x00000008	GPIO test
305	SMARTIO_PRT7_PRT	0x40320700	0x00000100	SMART I/O #7
306	TCPWM0_GRP0_CNT0_CNT	0x40380000	0x00000080	TCPWM#0 Group #0, Counter #0
307	TCPWM0_GRP0_CNT1_CNT	0x40380080	0x00000080	TCPWM#0 Group #0, Counter #1
308	TCPWM0_GRP0_CNT2_CNT	0x40380100	0x00000080	TCPWM#0 Group #0, Counter #2

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
309	TCPWM0_GRP0_CNT3_CNT	0x40380180	0x00000080	TCPWM#0 Group #0, Counter #3
310	TCPWM0_GRP0_CNT4_CNT	0x40380200	0x00000080	TCPWM#0 Group #0, Counter #4
311	TCPWM0_GRP0_CNT5_CNT	0x40380280	0x00000080	TCPWM#0 Group #0, Counter #5
312	TCPWM0_GRP0_CNT6_CNT	0x40380300	0x00000080	TCPWM#0 Group #0, Counter #6
313	TCPWM0_GRP0_CNT7_CNT	0x40380380	0x00000080	TCPWM#0 Group #0, Counter #7
314	TCPWM0_GRP0_CNT8_CNT	0x40380400	0x00000080	TCPWM#0 Group #0, Counter #8
315	TCPWM0_GRP0_CNT9_CNT	0x40380480	0x00000080	TCPWM#0 Group #0, Counter #9
316	TCPWM0_GRP0_CNT10_CNT	0x40380500	0x00000080	TCPWM#0 Group #0, Counter #10
317	TCPWM0_GRP0_CNT11_CNT	0x40380580	0x00000080	TCPWM#0 Group #0, Counter #11
318	TCPWM0_GRP0_CNT12_CNT	0x40380600	0x00000080	TCPWM#0 Group #0, Counter #12
319	TCPWM0_GRP0_CNT13_CNT	0x40380680	0x00000080	TCPWM#0 Group #0, Counter #13
320	TCPWM0_GRP0_CNT14_CNT	0x40380700	0x00000080	TCPWM#0 Group #0, Counter #14
321	TCPWM0_GRP0_CNT15_CNT	0x40380780	0x00000080	TCPWM#0 Group #0, Counter #15
322	TCPWM0_GRP0_CNT16_CNT	0x40380800	0x00000080	TCPWM#0 Group #0, Counter #16
323	TCPWM0_GRP0_CNT17_CNT	0x40380880	0x00000080	TCPWM#0 Group #0, Counter #17
324	TCPWM0_GRP0_CNT18_CNT	0x40380900	0x00000080	TCPWM#0 Group #0, Counter #18
325	TCPWM0_GRP0_CNT19_CNT	0x40380980	0x00000080	TCPWM#0 Group #0, Counter #19
326	TCPWM0_GRP0_CNT20_CNT	0x40380A00	0x00000080	TCPWM#0 Group #0, Counter #20
327	TCPWM0_GRP0_CNT21_CNT	0x40380A80	0x00000080	TCPWM#0 Group #0, Counter #21
328	TCPWM0_GRP0_CNT22_CNT	0x40380B00	0x00000080	TCPWM#0 Group #0, Counter #22
329	TCPWM0_GRP0_CNT23_CNT	0x40380B80	0x00000080	TCPWM#0 Group #0, Counter #23
330	TCPWM0_GRP0_CNT24_CNT	0x40380C00	0x00000080	TCPWM#0 Group #0, Counter #24
331	TCPWM0_GRP0_CNT25_CNT	0x40380C80	0x00000080	TCPWM#0 Group #0, Counter #25
332	TCPWM0_GRP0_CNT26_CNT	0x40380D00	0x00000080	TCPWM#0 Group #0, Counter #26
333	TCPWM0_GRP0_CNT27_CNT	0x40380D80	0x00000080	TCPWM#0 Group #0, Counter #27
334	TCPWM0_GRP0_CNT28_CNT	0x40380E00	0x00000080	TCPWM#0 Group #0, Counter #28
335	TCPWM0_GRP0_CNT29_CNT	0x40380E80	0x00000080	TCPWM#0 Group #0, Counter #29
336	TCPWM0_GRP0_CNT30_CNT	0x40380F00	0x00000080	TCPWM#0 Group #0, Counter #30
337	TCPWM0_GRP0_CNT31_CNT	0x40380F80	0x00000080	TCPWM#0 Group #0, Counter #31
338	TCPWM0_GRP0_CNT32_CNT	0x40381000	0x00000080	TCPWM#0 Group #0, Counter #32
339	TCPWM0_GRP0_CNT33_CNT	0x40381080	0x00000080	TCPWM#0 Group #0, Counter #33
340	TCPWM0_GRP1_CNT0_CNT	0x40388000	0x00000080	TCPWM#0 Group #1, Counter #0
341	TCPWM0_GRP1_CNT1_CNT	0x40388080	0x00000080	TCPWM#0 Group #1, Counter #1
342	TCPWM0_GRP1_CNT2_CNT	0x40388100	0x00000080	TCPWM#0 Group #1, Counter #2
343	TCPWM0_GRP1_CNT3_CNT	0x40388180	0x00000080	TCPWM#0 Group #1, Counter #3
344	TCPWM0_GRP1_CNT4_CNT	0x40388200	0x00000080	TCPWM#0 Group #1, Counter #4
345	TCPWM0_GRP1_CNT5_CNT	0x40388280	0x00000080	TCPWM#0 Group #1, Counter #5
346	TCPWM0_GRP1_CNT6_CNT	0x40388300	0x00000080	TCPWM#0 Group #1, Counter #6
347	TCPWM0_GRP1_CNT7_CNT	0x40388380	0x00000080	TCPWM#0 Group #1, Counter #7
348	TCPWM0_GRP1_CNT8_CNT	0x40388400	0x00000080	TCPWM#0 Group #1, Counter #8
349	TCPWM0_GRP1_CNT9_CNT	0x40388480	0x00000080	TCPWM#0 Group #1, Counter #9
350	TCPWM0_GRP1_CNT10_CNT	0x40388500	0x00000080	TCPWM#0 Group #1, Counter #10
351	TCPWM0_GRP1_CNT11_CNT	0x40388580	0x00000080	TCPWM#0 Group #1, Counter #11
352	TCPWM0_GRP2_CNT0_CNT	0x40390000	0x00000080	TCPWM#0 Group #2, Counter #0
353	TCPWM0_GRP2_CNT1_CNT	0x40390080	0x00000080	TCPWM#0 Group #2, Counter #1

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
354	TCPWM0_GRP2_CNT2_CNT	0x40390100	0x00000080	TCPWM#0 Group #2, Counter #2
355	TCPWM0_GRP2_CNT3_CNT	0x40390180	0x00000080	TCPWM#0 Group #2, Counter #3
356	TCPWM0_GRP2_CNT4_CNT	0x40390200	0x00000080	TCPWM#0 Group #2, Counter #4
357	TCPWM0_GRP2_CNT5_CNT	0x40390280	0x00000080	TCPWM#0 Group #2, Counter #5
358	TCPWM0_GRP2_CNT6_CNT	0x40390300	0x00000080	TCPWM#0 Group #2, Counter #6
359	TCPWM0_GRP2_CNT7_CNT	0x40390380	0x00000080	TCPWM#0 Group #2, Counter #7
360	TCPWM0_GRP2_CNT8_CNT	0x40390400	0x00000080	TCPWM#0 Group #2, Counter #8
361	TCPWM0_GRP2_CNT9_CNT	0x40390480	0x00000080	TCPWM#0 Group #2, Counter #9
362	TCPWM0_GRP2_CNT10_CNT	0x40390500	0x00000080	TCPWM#0 Group #2, Counter #10
363	TCPWM0_GRP2_CNT11_CNT	0x40390580	0x00000080	TCPWM#0 Group #2, Counter #11
364	TCPWM0_GRP2_CNT12_CNT	0x40390600	0x00000080	TCPWM#0 Group #2, Counter #12
365	TCPWM0_GRP2_CNT13_CNT	0x40390680	0x00000080	TCPWM#0 Group #2, Counter #13
366	TCPWM0_GRP2_CNT14_CNT	0x40390700	0x00000080	TCPWM#0 Group #2, Counter #14
367	TCPWM0_GRP2_CNT15_CNT	0x40390780	0x00000080	TCPWM#0 Group #2, Counter #15
368	LCD0	0x403B0000	0x00010000	Segment LCD Controller#0
369	EVTGEN0	0x403F0000	0x00001000	Event generator #0
370	SMIF0_MAIN	0x40420000	0x00001000	Serial Memory Interface #0
371	LIN0_MAIN	0x40500000	0x00000008	LIN#0, main
372	LIN0_CH0_CH	0x40508000	0x00000100	LIN#0, Channel #0
373	LIN0_CH1_CH	0x40508100	0x00000100	LIN#0, Channel #1
374	CXPI0_MAIN	0x40510000	0x00000008	CXPI#0, main
375	CXPI0_CH0_CH	0x40518000	0x00000100	CXPI#0, Channel #0
376	CXPI0_CH1_CH	0x40518100	0x00000100	CXPI#0, Channel #1
377	CANFD0_CH0_CH	0x40520000	0x00000200	CAN#0, Channel #0
378	CANFD0_CH1_CH	0x40520200	0x00000200	CAN#0, Channel #1
379	CANFD1_CH0_CH	0x40540000	0x00000200	CAN#1, Channel #0
380	CANFD1_CH1_CH	0x40540200	0x00000200	CAN#1, Channel #1
381	CANFD0_MAIN	0x40521000	0x00000100	CAN#0 main
382	CANFD1_MAIN	0x40541000	0x00000100	CAN#1 main
383	CANFD0_BUF	0x40530000	0x00010000	CAN#0 buffer
384	CANFD1_BUF	0x40550000	0x00010000	CAN#1 buffer
385	SCB0	0x40600000	0x00010000	Serial Communication Block#0
386	SCB1	0x40610000	0x00010000	Serial Communication Block#1
387	SCB2	0x40620000	0x00010000	Serial Communication Block#2
388	SCB3	0x40630000	0x00010000	Serial Communication Block#3
389	SCB4	0x40640000	0x00010000	Serial Communication Block#4
390	SCB5	0x40650000	0x00010000	Serial Communication Block#5
391	SCB6	0x40660000	0x00010000	Serial Communication Block#6
392	SCB7	0x40670000	0x00010000	Serial Communication Block#7
393	SCB8	0x40680000	0x00010000	Serial Communication Block#8
394	SCB9	0x40690000	0x00010000	Serial Communication Block#9
395	SCB10	0x406A0000	0x00010000	Serial Communication Block#10
396	SCB11	0x406B0000	0x00010000	Serial Communication Block#11
397	TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX	0x40818000	0x00000100	TDM#0 TX Structure #0
398	TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX	0x40818200	0x00000100	TDM#0 TX Structure #1

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
399	TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX	0x40818100	0x00000100	TDM#0 RX Structure #0
400	TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX	0x40818300	0x00000100	TDM#0 RX Structure #1
401	SG0_SG_STRUCT0_TX	0x40828000	0x00000100	SG#0 TX Structure #0
402	SG0_SG_STRUCT1_TX	0x40828100	0x00000100	SG#0 TX Structure #1
403	SG0_SG_STRUCT2_TX	0x40828200	0x00000100	SG#0 TX Structure #2
404	SG0_SG_STRUCT3_TX	0x40828300	0x00000100	SG#0 TX Structure #3
405	SG0_SG_STRUCT4_TX	0x40828400	0x00000100	SG#0 TX Structure #4
406	PWM0_MAIN	0x40830000	0x00000010	PWM#0 Main
407	PWM0_TX0_TX	0x40838000	0x00000100	PWM#0 TX0
408	PWM0_TX1_TX	0x40838100	0x00000100	PWM#0 TX1
409	MIXER0_MIXER_SRC_STRUCT0_SRC	0x40888000	0x00000100	MIXER#0 Source Structure #0
410	MIXER0_MIXER_SRC_STRUCT1_SRC	0x40888100	0x00000100	MIXER#0 Source Structure #1
411	MIXER0_MIXER_SRC_STRUCT2_SRC	0x40888200	0x00000100	MIXER#0 Source Structure #2
412	MIXER0_MIXER_SRC_STRUCT3_SRC	0x40888300	0x00000100	MIXER#0 Source Structure #3
413	MIXER0_MIXER_SRC_STRUCT4_SRC	0x40888400	0x00000100	MIXER#0 Source Structure #4
414	MIXER0_MIXER_DST_STRUCT_DST	0x4088C000	0x00000100	MIXER#0 Destination Structure
415	PASS0_SAR0_SAR	0x40900000	0x00000400	PASS SAR#0
416	PASS0_SAR1_SAR	0x40901000	0x00000008	PASS SAR#1
417	PASS0_SAR0_CH0_CH	0x40900800	0x00000040	SAR#0, Channel #0
418	PASS0_SAR0_CH1_CH	0x40900840	0x00000040	SAR#0, Channel #1
419	PASS0_SAR0_CH2_CH	0x40900880	0x00000040	SAR#0, Channel #2
420	PASS0_SAR0_CH3_CH	0x409008C0	0x00000040	SAR#0, Channel #3
421	PASS0_SAR0_CH4_CH	0x40900900	0x00000040	SAR#0, Channel #4
422	PASS0_SAR0_CH5_CH	0x40900940	0x00000040	SAR#0, Channel #5
423	PASS0_SAR0_CH6_CH	0x40900980	0x00000040	SAR#0, Channel #6
424	PASS0_SAR0_CH7_CH	0x409009C0	0x00000040	SAR#0, Channel #7
425	PASS0_SAR0_CH8_CH	0x40900A00	0x00000040	SAR#0, Channel #8
426	PASS0_SAR0_CH9_CH	0x40900A40	0x00000040	SAR#0, Channel #9
427	PASS0_SAR0_CH10_CH	0x40900A80	0x00000040	SAR#0, Channel #10
428	PASS0_SAR0_CH11_CH	0x40900AC0	0x00000040	SAR#0, Channel #11
429	PASS0_SAR0_CH12_CH	0x40900B00	0x00000040	SAR#0, Channel #12
430	PASS0_SAR0_CH13_CH	0x40900B40	0x00000040	SAR#0, Channel #13
431	PASS0_SAR0_CH14_CH	0x40900B80	0x00000040	SAR#0, Channel #14
432	PASS0_SAR0_CH15_CH	0x40900BC0	0x00000040	SAR#0, Channel #15
433	PASS0_SAR0_CH16_CH	0x40900C00	0x00000040	SAR#0, Channel #16
434	PASS0_SAR0_CH17_CH	0x40900C40	0x00000040	SAR#0, Channel #17
435	PASS0_SAR0_CH18_CH	0x40900C80	0x00000040	SAR#0, Channel #18
436	PASS0_SAR0_CH19_CH	0x40900CC0	0x00000040	SAR#0, Channel #19
437	PASS0_SAR0_CH20_CH	0x40900D00	0x00000040	SAR#0, Channel #20
438	PASS0_SAR0_CH21_CH	0x40900D40	0x00000040	SAR#0, Channel #21
439	PASS0_SAR0_CH22_CH	0x40900D80	0x00000040	SAR#0, Channel #22
440	PASS0_SAR0_CH23_CH	0x40900DC0	0x00000040	SAR#0, Channel #23
441	PASS0_SAR0_CH24_CH	0x40900E00	0x00000040	SAR#0, Channel #24
442	PASS0_SAR0_CH25_CH	0x40900E40	0x00000040	SAR#0, Channel #25
443	PASS0_SAR0_CH26_CH	0x40900E80	0x00000040	SAR#0, Channel #26

Table 23-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU fixed structure pair	Address	Size	Description
444	PASS0_SAR0_CH27_CH	0x40900EC0	0x00000040	SAR#0, Channel #27
445	PASS0_SAR0_CH28_CH	0x40900F00	0x00000040	SAR#0, Channel #28
446	PASS0_SAR0_CH29_CH	0x40900F40	0x00000040	SAR#0, Channel #29
447	PASS0_SAR0_CH30_CH	0x40900F80	0x00000040	SAR#0, Channel #30
448	PASS0_SAR0_CH31_CH	0x40900FC0	0x00000040	SAR#0, Channel #31
449	PASS0_TOP	0x409F0000	0x00001000	PASS0 SAR main

24 Bus masters

The Arbiter (part of flash controller) performs priority-based arbitration based on the master identifier. Each bus master has a dedicated 4-bit master identifier. This master identifier is used for bus arbitration and IPC functionality.

Table 24-1 Bus masters for access and protection control

ID No.	Master ID	Description
0	CPUSS_MS_ID_CM0	Master ID for Cortex®-M0+ CPU
1	CPUSS_MS_ID_CRYPTO	Master ID for Crypto
2	CPUSS_MS_ID_DW0	Master ID for P-DMA#0
3	CPUSS_MS_ID_DW1	Master ID for P-DMA#1
4	CPUSS_MS_ID_DMAC	Master ID for M-DMA#0
14	CPUSS_MS_ID_CM4	Master ID for Cortex®-M4F CPU
15	CPUSS_MS_ID_TC	Master ID for DAP Tap Controller

25 Miscellaneous configuration

Table 25-1 Miscellaneous configuration for CYT2CL devices

Sl. No.	Configuration	Number/ instances	Description
0	SRSS_NUM_CLKPATH	6	Number of clock paths. One for each of FLL, PLL, Direct and CSV
1	SRSS_NUM_HFROOT	6	Number of CLK_HFs roots present
2	PERI_PC_NR	8	Number of protection contexts
3	PERI_CLOCK_NR	85	Number of programmable clocks (outputs)
4	PERI_DIV_8_NR	11	Number of divide-by-8 clock dividers
5	PERI_DIV_16_NR	16	Number of divide-by-16 clock dividers
	PERI_DIV_16_5_NR	4	Number of divide-by-16.5 clock dividers
6	PERI_DIV_24_5_NR	11	Number of divide-by-24.5 clock dividers
7	CPUSS_CM0P_MPU_NR	8	Number of MPU regions in CM0+
8	CPUSS_CM4_MPU_NR	8	Number of MPU regions in CM4
9	CPUSS_CRYPTO_BUFF_SIZE	2048	Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)
10	CPUSS_FAULT_FAULT_NR	4	Number of fault structures
11	CPUSS_IPC_IPC_NR	8	Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM4 access 2 - Reserved for DAP access Remaining for user purposes
12	SCB0_EZ_DATA_NR	256	Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports EZ mode
13	CPUSS_PROT_SMPU_STRUCT_NR	16	Number of SMPU protection structures
14	TCPWM_TR_ONE_CNT_NR	1	Number of input triggers per counter, routed to one counter
15	TCPWM_TR_ALL_CNT_NR	60	Number of input triggers routed to all counters, based on the pin package
16	TCPWM_GRP_NR	3	Number of TCPWM#0 counter groups
17	TCPWM_GRP_NR0_GRP_GRP_CNT_NR	34	Number of counters per TCPWM#0 Group #0
18	TCPWM_GRP_NR0_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM#0 Group #0
19	TCPWM_GRP_NR1_GRP_GRP_CNT_NR	12	Number of counters per TCPWM#0 Group #1
20	TCPWM_GRP_NR1_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM#0 Group #1
21	TCPWM_GRP_NR2_GRP_GRP_CNT_NR	16	Number of counters per TCPWM#0 Group #2
22	TCPWM_GRP_NR2_CNT_GRP_CNT_WIDTH	32	Counter width in number of bits per TCPWM#0 Group #2
23	CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE	16	Message RAM size in kB shared by all the channels
24	EVTGEN_COMP_STRUCT_NR	16	Number of Event Generator comparator structures

26 Development support

CYT2CL has a rich set of documentation, programming tools, and online resources to assist during the development process. Visit **www.infineon.com** to find out more.

26.1 Documentation

A suite of documentation supports CYT2CL to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

26.1.1 Software user guide

A step-by-step guide for using the sample driver library along with third-party IDEs such as IAR EWARM and GHS Multi.

26.1.2 Technical reference manual

The technical reference manual (TRM) contains all the technical detail needed to use a CYT2CL device, including a complete description of all registers. The TRM is available in the documentation section at **www.infineon.com**.

26.2 Tools

CYT2CL is supported on third-party development tool ecosystems such as IAR and GHS. CYT2CL is also supported by Infineon programming utilities for programming, erasing, or reading using Infineon's MiniProg4 or Segger J-link. More details are available in the documentation section at **www.infineon.com**.

27 Electrical specifications

27.1 Absolute maximum ratings

Use of this device under conditions outside the Min and Max limits listed in **Table 27-1** may cause permanent damage to the device. Exposure to conditions within the limits of **Table 27-1** but beyond those of normal operation for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When operated under conditions within the limits of **Table 27-1** but beyond those of normal operation, the device may not operate to specification.

Power considerations

The average chip-junction temperature, T_J, in °C, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Equation. 1

Where:

T_A is the ambient temperature in °C.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{IO} ($P_D = P_{INT} + P_{IO}$).

P_{INT} is the chip internal power. ($P_{INT} = V_{DDD} \times I_{DD} + V_{DDA\_ADC} \times I_{VDDA}$)

P_{IO} represents the power dissipation on input and output pins; user determined.

For most applications, $P_{IO} < P_{INT}$ and may be neglected.

On the other hand, P_{IO} may be significant if the device is configured to continuously drive external modules and/or memories.

Table 27-1 Absolute maximum ratings

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID10	V_{DDD_ABS}	Power supply voltage (V_{DDD})[35]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-3** for assignment of ports to supply domains
SID10A	$V_{DDIO\_GPIO\_ABS}$	Power supply voltage (V_{DDIO_GPIO})[35]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-3** for assignment of ports to supply domains
SID10B	$V_{DDIO\_SMC\_ABS}$	Power supply voltage (V_{DDIO_SMC})[35]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-3** for assignment of ports to supply domains
SID10C	$V_{DDIO\_HSIO\_ABS}$	Power supply voltage (V_{DDIO_HSIO})[35]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-3** for assignment of ports to supply domains
SID11	$V_{DDA\_ADC\_ABS}$	Analog power supply voltage (V_{DDA_ADC})[35] Supply for SAR ADC	V_{SSA_ADC} – 0.3	–	V_{SSA_ADC} + 6.0	V	
SID12	V_{REFH_ABS}	SAR Analog reference voltage, HIGH[35]	V_{SSA_ADC} – 0.3	–	V_{SSA_ADC} + 6.0	V	$V_{REFH} \le V_{DDA\_ADC}$ + 0.3 V
SID12A	V_{REFL_ABS}	SAR Analog reference voltage, LOW[35]	V_{SSA_ADC} – 0.3	–	V_{SSA_ADC} + 0.3	V	
SID13	V_{CCD_ABS}	Power supply voltage (V_{CCD})	V_{SS} – 0.3	–	V_{SS} + 1.21	V	
SID15A	$V_{I\_GPIO\_ABS}$	Input voltage[35]	V_{SS} – 0.5	–	V_{DDIO_GPIO} + 0.5	V	See **Table 3-3** for assignment of ports to supply domains
SID15B	$V_{I\_SMC\_ABS}$	Input voltage[35]	V_{SS} – 0.5	–	V_{DDIO_SMC} + 0.5	V	See **Table 3-3** for assignment of ports to supply domains
SID15C	$V_{I\_HSIO\_ABS}$	Input voltage[35]	V_{SS} – 0.5	–	V_{DDIO_HSIO} + 0.5	V	See **Table 3-3** for assignment of ports to supply domains
SID16	$V_{I\_ADC\_ABS}$	Analog input voltage[35]	V_{SSA_ADC} – 0.3	–	V_{DDA_ADC} + 0.3	V	See **Table 3-3** for assignment of ports to supply domains
SID17A	$V_{O\_GPIO\_ABS}$	Output voltage[35]	V_{SS} – 0.3	–	V_{DDIO_GPIO} + 0.3	V	See **Table 3-3** for assignment of ports to supply domains
SID17B	$V_{O\_SMC\_ABS}$	Output voltage[35]	V_{SS} – 0.3	–	V_{DDIO_SMC} + 0.3	V	See **Table 3-3** for assignment of ports to supply domains
SID17C	$V_{O\_HSIO\_ABS}$	Output voltage[35]	V_{SS} – 0.3	–	V_{DDIO_HSIO} + 0.3	V	See **Table 3-3** for assignment of ports to supply domains
SID18	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[36, 37, 38, 39]	–5	–	5	mA	Applicable to GPIO pins
SID18A	ΣI_{CLAMP_ABS}	Total maximum clamp current	–25	–	25	mA	Applicable to GPIO pins in total for V_{DDIO_GPIO}
SID18B	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[36, 37, 38, 39]	–52	–	52	mA	Applicable to SMC I/O pins
SID18C	ΣI_{CLAMP_ABS}	Total maximum clamp current	–624	–	624	mA	Applicable to SMC I/O pins clamping current occurred by sudden switching-off of inductive load (stepper motor coil) in total for V_{DDIO_SMC}
SID18D	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[36, 37, 38, 39]	–5	–	5	mA	Applicable to HSIO_STDLN
SID18E	ΣI_{CLAMP_ABS}	Total maximum clamp current	–25	–	25	mA	Applicable to I/O pins in total for V_{DDIO_HSIO}

Notes
35. These parameters are based on the condition that $V_{SS} = V_{SSA\_ADC} = 0.0$ V.
36. A current-limiting resistor must be provided such that the current at the I/O pin does not exceed rated values at any time, including during power transients. See **Figure 27-4** for more information on the recommended circuit.
37. VDDIO must be sufficiently loaded or protected to prevent the clamp current from pulling it above the normal operating range.
38. Clamp current can be applied only when the part is powered, and for ports between each pair of VDDIO/VSSIO pins (excluding ADC pins, ECO_IN/OUT, LPECO_IN/LPECO_OUT, WCO_IN/OUT and XRES_L).
39. When the conditions of [36], [37], [38] and SID18/A/B/C/D/E are met, $\lvert I_{CLAMP\_ABS}\rvert$ supersedes V_{I_ABS}.

Table 27-1 Absolute maximum ratings *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID20	$I_{OL1\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[40]	–	–	3.5	mA	Setting is 1 mA
SID21	$I_{OL2\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[40]	–	–	7	mA	Setting is 2 mA
SID22	$I_{OL3\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[40]	–	–	10	mA	Setting is 5 mA
SID22A	$I_{OL4\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[40]	–	–	10	mA	Setting is 6 mA
SID26	$\Sigma I_{OL\_GPIO\_ABS}$	LOW-level total output current for GPIO[41]	–	–	50	mA	
SID26A	$I_{OL\_SMC\_ABS}$	LOW-level maximum output current for SMC[42]	–	–	52	mA	Setting is 30 mA at –40°C
SID26B	$\Sigma I_{OL\_SMC\_ABS}$	LOW-level total output current for SMC[43]	–	–	300	mA	25°C < T_A ≤ 105°C
SID26I	$\Sigma I_{OL\_SMC\_ABS}$	LOW-level total output current for GPIO_SMC[43]	–	–	450	mA	–40°C ≤ T_A ≤ 25°C
SID26G	$I_{OL\_HSIO\_ABS}$	LOW-level maximum output current for HSIO[44]	–	–	15	mA	
SID26H	$\Sigma I_{OL\_HSIO\_ABS}$	LOW-level total output current for HSIO[45]	–	–	150	mA	
SID27	$I_{OH1\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[40]	–	–	–3.5	mA	Setting is 1 mA
SID28	$I_{OH2\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[40]	–	–	–7	mA	Setting is 2 mA
SID29	$I_{OH3\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[40]	–	–	–10	mA	Setting is 5 mA
SID29A	$I_{OH3\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[40]	–	–	–10	mA	Setting is 6 mA
SID33	$\Sigma I_{OH1\_GPIO\_ABS}$	HIGH-level total output current for GPIO[41]	–	–	–50	mA	
SID33A	$I_{OH\_SMC\_ABS}$	HIGH-level maximum output current for SMC[42]	–	–	–52	mA	Setting is 30 mA at –40 °C
SID33B	$\Sigma I_{OH\_SMC\_ABS}$	HIGH-level total output current for SMC[43]	–	–	–300	mA	
SID33G	$I_{OH\_HSIO\_ABS}$	HIGH-level maximum output current for HSIO[44]	–	–	–15	mA	
SID33H	$\Sigma I_{OH\_HSIO\_ABS}$	HIGH-level total output current for HSIO[45]	–	–	–150	mA	
SID34_3	P_D	Power dissipation	–	–	1800	mW	
SID36	T_A	Operating ambient temperature	–40	–	105	°C	For S-grade devices
SID38	T_{STG}	Storage temperature	–55	–	150	°C	
SID39	T_J	Operating junction temperature	–40	–	150	°C	
SID39A	V_{ESD_HBM}	Electrostatic discharge human body model	2000	–	–	V	
SID39B1	V_{ESD_CDM1}	Electrostatic discharge charged device model for corner pins	750	–	–	V	
SID39B2	V_{ESD_CDM2}	Electrostatic discharge charged device model for all other pins	500	–	–	V	
SID39C	I_{LU}	The maximum pin current the device can tolerate before triggering a latch-up	–100	–	100	mA	

Notes
40.The maximum output current is the peak current flowing through any one GPIO I/O.
41.The total output current is the maximum current flowing through all GPIO I/Os (GPIO_STD, and GPIO_ENH).
42.The maximum output current is the peak current flowing through any one SMC I/O.
43.The total output current is the maximum current flowing through all SMC I/Os (GPIO_SMC).
44.The maximum output current is the peak current flowing through any one HSIO I/O.
45.The total output current is the maximum current flowing through all HSIO I/Os (HSIO_STDLN)

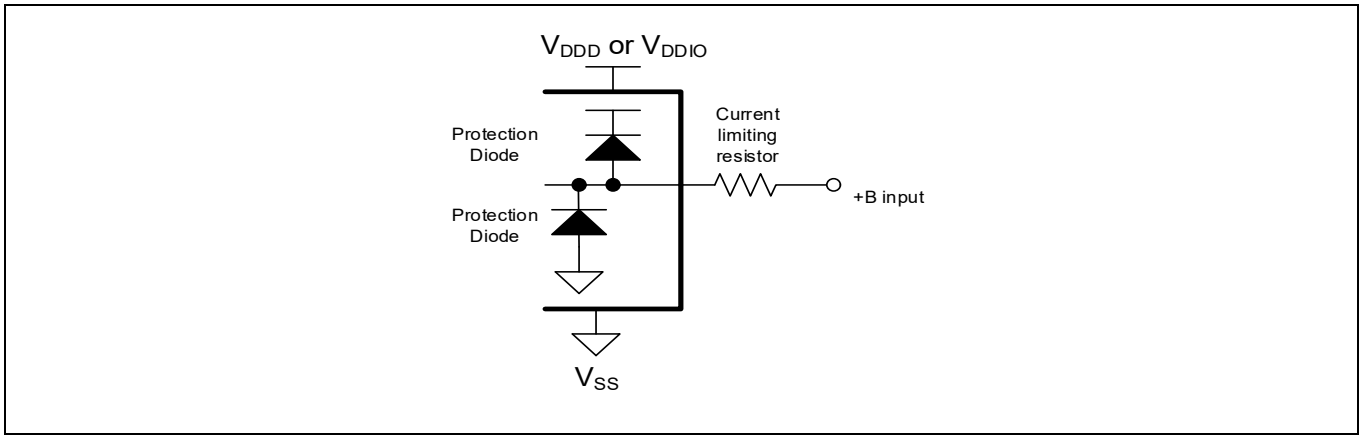


Figure 27-1 Example of a recommended circuit[46]

WARNING:
Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current, or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Note
46.+B is the positive battery voltage around 45 V.

27.2 Device-level specifications

Table 27-2 Recommended operating conditions

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended operating conditions							
SID40	V_{DDD}, V_{DDA_ADC}, V_{DDIO_GPIO}, V_{DDIO_SMC}	Power supply voltage[47]	2.7[48]	–	5.5[49]	V	
SID40M	V_{DDD}	Power supply voltage	2.7[48]	–	3.6	V	When using I^2S or TDM or (PCM)PWM
SID40A	V_{DDIO_EFP}	Power supply voltage for eFuse programming[50]	3	–	5.5	V	V_{DDD} for this product, when programming eFuses
SID40B	V_{DDIO_HSIO}	Power supply voltage	3.0	3.3	3.6	V	
SID41A	C_{S1}	Smoothing capacitor[51, 52]	3.76	10	11	µF	

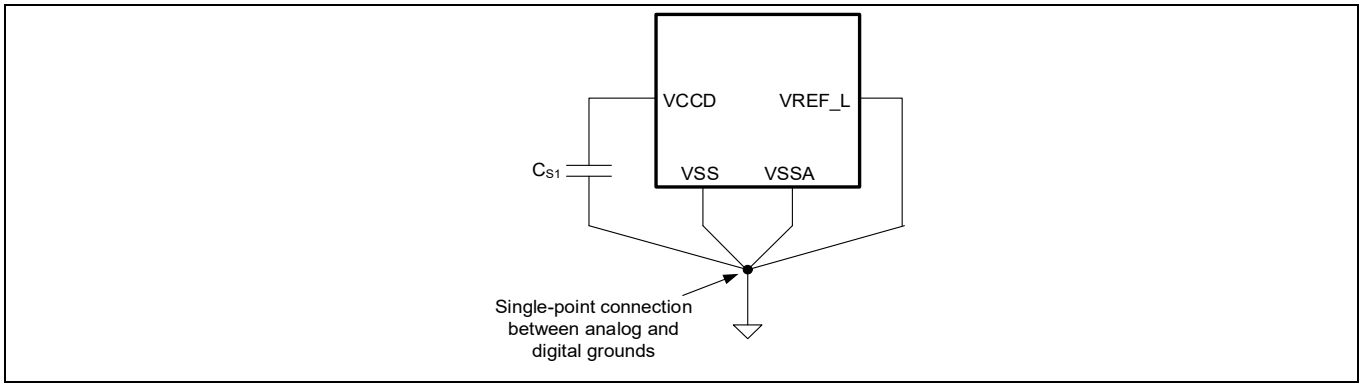


Figure 27-2 Smoothing capacitor

Notes

47. Ensure $V_{DDIO\_GPIO} \geq 0.8 \times V_{DDA\_ADC}$ when SARMUX0 is enabled.
48. 3.0 V ±10% is supported with a lower BOD setting option. This setting provides robust protection for internal timing but BOD reset occurs at a voltage below the specified operating conditions. A higher BOD setting option is available (consistent with down to 3.0 V) and guarantees that all operating conditions are met.
49. 5.0 V ±10% is supported with a higher OVD setting option. This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met. Voltage overshoot to a higher OVD setting range for V_{DDD} and V_{DDA_ADC} is permissible, provided the duration is less than 2 hours cumulated. Note that during overshoot voltage condition electrical parameters are not guaranteed.
50. eFuse programming must be executed with the part in a “quiet” state, with minimal activity (preferably only JTAG or a single LIN/CAN channel on V_{DDD} domain).
51. Smoothing capacitor, C_{S1} is required per chip (not per V_{CCD} pin). The V_{CCD} pins must be connected together to ensure a low-impedance connection (see the requirement in **Figure 27-2**).
52. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device, ensure that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature coefficient is normally found within a parts catalog (such as, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to operate to less than datasheet specifications.

27.3 DC specifications

Table 27-3 DC specifications, CPU current and transition time specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID56_2	I_{DD1}	Execute from flash; Cortex®-M4F CPU in Active mode, all peripherals enabled	–	52	140	mA	Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 105°C, T_J = 150°C, V_{DDD} = 5.5 V, process worst (FF) (Maximum expected V_{DDD} when T_J = 150°C is reached due to self-heating)
SID50A_2	I_{DD1}	Cortex®-M4F/M0+ CPUs in Sleep mode	–	7	26	mA	Clocks running at max frequency, All CPUs in Sleep mode. All peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 85°C, V_{DDD} = 5.5 V, process worst (FF)
SID50C_2	I_{DD1}	Cortex®-M4F/M0+ CPUs in Sleep mode (room temp)	–	–	12	mA	Clocks running at max frequency, All CPUs in Sleep mode. All peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No I/O toggling. Max: T_A = 25°C, V_{DDD} = 5.5 V, process worst (FF)
SID59_2	I_{DD_DS32A}	32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode	–	140	–	µA	Deep Sleep Mode (RTC at 32 kHz and EVTGEN operating, all other peripherals off, CAN MRAM disabled), Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT)
SID59A_2	I_{DD_DS32A}	32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode (room temp)	–	–	240	µA	Deep Sleep Mode (RTC at 32 kHz and EVTGEN operating, all other peripherals off, CAN MRAM disabled), Max: V_{DDD} = 5.5 V, T_A = 25°C, process worst (FF)
SID60_2	I_{DD_DS32B}	32 KB SRAM retention, LPECO(4 MHz) operation in DeepSleep mode	–	–	920	µA	DeepSleep Mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled), Max: V_{DDD} = 5.5 V, T_A = 85°C, process worst (FF)
SID64_2	I_{DD_DS32C}	32 KB SRAM retention, ILO operation in DeepSleep mode	–	40	750	µA	DeepSleep Mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled) Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 85°C, V_{DDD} = 5.5 V, process worst (FF)
SID64A_2	I_{DD_DS32D}	32 KB SRAM retention, ILO operation in DeepSleep mode (room temp)	–	–	140	µA	DeepSleep Mode (RTC at 32kHz and Event generator operating, all other peripherals off, CAN MRAM disabled) Max: T_A = 25°C, V_{DDD} = 5.5 V, process worst (FF)
Hibernate Mode							
SID66	I_{DD_HIB1}	V_{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	20	µA	T_A = 25°C using ILO, V_{DDD} = 5.0 V
SID66A	I_{DD_HIB2}	V_{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	40	µA	T_A = 25°C, using WCO, V_{DDD} = 5.0 V

Table 27-3 DC specifications, CPU current and transition time specifications *(continued)*

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID66B	I_{DD_HIB3}	V_{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	75	µA	T_A = 85°C, using WCO, V_{DDD} = 5.5 V
SID66C	I_{DD_HIB4}	V_{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	150	µA	T_A = 25°C using LPECO 4 MHz, 20-pF load of LPECO, V_{DDD} = 5.0 V
SID66D	I_{DD_HIB5}	V_{DDD} current, Hibernate Mode + RTC at 32.768 KHz	–	–	215	µA	T_A = 85°C, using LPECO 4 MHz, 20-pF load of LPECO, V_{DDD} = 5.5 V
Power Mode Transition Times							
SID69	t_{ACT_DS}	Power down time from ACTIVE to DEEPSLEEP (using the internal regulator)	–	–	2.5	µs	When IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.
SID67	t_{DS_ACT}	DeepSleep to Active transition time (IMO clock, flash execution)	–	–	26	µs	When using 8 MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T_A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs
SID67A	$t_{DS\_ACT\_FLL}$	DeepSleep to Active transition time (FLL clock, flash execution)	–	–	26	µs	When using FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T_A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs
SID67B	$t_{DS\_ACT\_PLL}$	DeepSleep to Active transition time (PLL clock)	–	–	60	µs	When using PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until PLL locks. T_A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs
SID68	t_{HIB_ACT}	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) until CM0+ begins executing ROM boot	–	–	265	µs	Without boot runtime. Guaranteed by design
SID68A	t_{LVR_ACT}	Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot	8	–	10	µs	Without boot runtime. Guaranteed by design
SID68B	t_{LVR_DS}	Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot	–	–	15	µs	Without boot runtime. Guaranteed by design

Table 27-3 DC specifications, CPU current and transition time specifications *(continued)*

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID79	$t_{HIBWAKE-UP\_PW}$	Pulse width for wakeup from Hibernate mode on HIBERANTE_WAKEUP pins	90	–	–	ns	Guaranteed by design
SID80A_2	t_{RB_N}	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	2600	µs	FAST_BOOT = 0, CM0+ clocked at 50 MHz
SID80B_2	t_{RB_S}	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	3800	µs	FAST_BOOT = 0, CM0+ clocked at 50 MHz
SID81A_2	t_{FB}	Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state	–	–	110	µs	FAST_BOOT = 0, TOC2_FLAGS=0x2CF, CM0+ clocked at 50 MHz, Listen window = 0 ms
SID81B_2	t_{FB_A}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	9800	µs	FAST_BOOT = 0, TOC2_FLAGS = 0x24F, CM0+ clocked at 50 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA-2048.
SID81C_2	t_{FB_B}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	17000	µs	FAST_BOOT = 0, TOC2_FLAGS = 0x24F, CM0+ clocked at 50 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 384 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA-3072.
Regulator Specifications							
SID600	V_{CCD}	Internal regulator core supply voltage (transient range)	1.05	1.1	1.15	V	
SID601_2	I_{DDD_ACT}	Regulator operating current in Active/Sleep mode	–	80	150	µA	Guaranteed by design
SID602	I_{DDD_DPSLP}	Regulator operating current in DeepSleep mode	–	1.5	20	µA	Guaranteed by design
SID603_2	I_{RUSH}	In-rush current	–	–	375	mA	Average V_{DDD} current until C_{S1} (connected to VCCD pin) is charged after Active regulator is turned on.
SID604_2	I_{OUT}	Internal regulator output current for operation	–	–	150	mA	Without triggering OVD

27.4 Reset specifications

Table 27-4 XRES_L Reset

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
XRES_L DC specifications							
SID73	I_{DD_XRES}	I_{DD} when XRES_L asserted	–	–	1.7	mA	Typ: T_A = 25°C, V_{DDD} = 5 V, process typ (TT) Max: T_A = 105°C, V_{DDD} = 5.5 V, process worst (FF)
SID74	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID75	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID76	R_{PULLUP}	Pull-up resistor	7	–	20	kΩ	
SID77	C_{IN}	Input capacitance	–	–	5	pF	
SID78	$V_{HYSXRES}$	Input voltage hysteresis	0.05 × V_{DDD}	–	–	V	
XRES_L AC specifications							
SID70	t_{XRES_ACT}	XRES_L release to Active transition time	–	–	265	µs	Without boot runtime. Guaranteed by design
SID71	t_{XRES_PW}	XRES_L pulse width	5	–	–	µs	
SID72	t_{XRES_FT}	Pulse suppression width	100	–	–	ns	

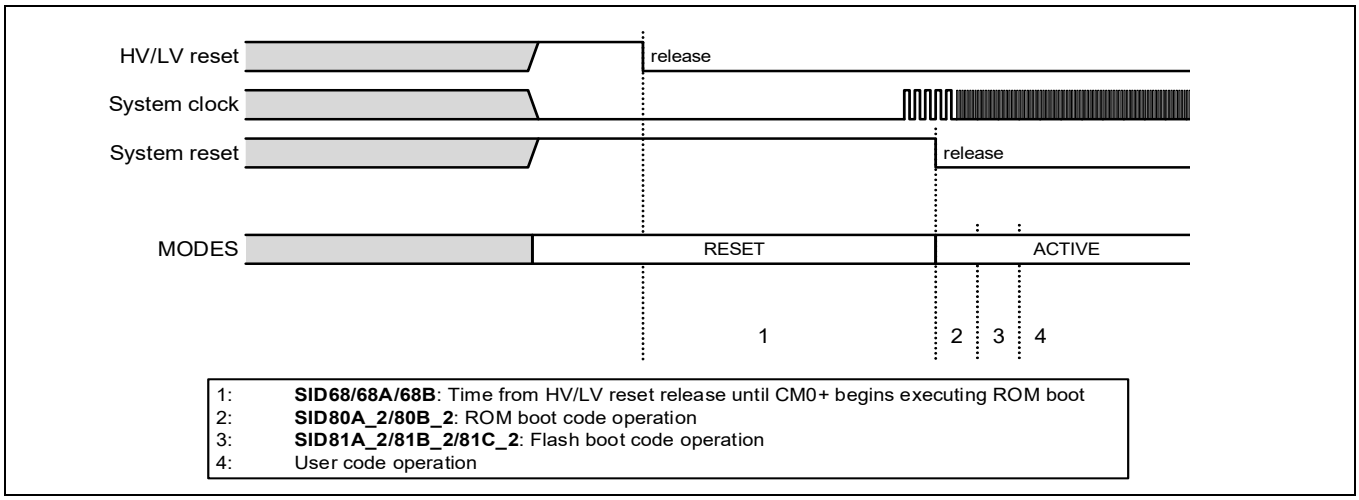


Figure 27-3 Reset sequence

27.5 I/O Specifications

Table 27-5 I/O specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
V_{DDIO_GPIO} (standard 5 V I/O) Specifications for GPIO_STD ports except GPIO_ENH							
SID650	V_{OL1}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, $V_{DDIO\_GPIO} \geq 4.5$ V
SID651	V_{OL2}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $V_{DDIO\_GPIO} \geq 4.5$ V
SID651D	V_{OL2}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID652	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $V_{DDIO\_GPIO} \geq 4.5$ V
SID652D	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID653	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $V_{DDIO\_GPIO} \geq 4.5$ V
SID653D	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID654	V_{OH1}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, $V_{DDIO\_GPIO} \geq 4.5$ V
SID654D	V_{OH1}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID655	V_{OH2}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, $V_{DDIO\_GPIO} \geq 4.5$ V
SID655D	V_{OH2}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID656	V_{OH3}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $V_{DDIO\_GPIO} \geq 4.5$ V
SID656D	V_{OH3}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID657	V_{OH4}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $V_{DDIO\_GPIO} \geq 4.5$ V
SID657D	V_{OH4}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID658	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID659	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID660	V_{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661	V_{IH_TTL}	Input voltage HIGH threshold in TTL mode	2	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662	V_{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 $4.5\ V \leq V_{DDIO\_GPIO} \leq 5.5$ V
SID663	V_{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID664	V_{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665	V_{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 $4.5\ V \leq V_{DDIO\_GPIO} \leq 5.5$ V
SID666	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0

Table 27-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID668	V_{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID669	C_{in}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID670	I_{IL}	Input leakage current	–1	–	1	µA	V_{DDIO_GPIO} = V_{DDD} = V_{DDA_ADC} = 5.5 V, V_{SS} < V_I < V_{DDIO_GPIO} -40°C ≤ TA ≤ 105°C This is valid for the pin which do not have ADC input functionality.
SID671	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	10	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b00, 20-pF load, entire V_{DDIO_GPIO} range
SID672	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b00, 50-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
SID673	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b01, 20-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
SID674	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b10, 10-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
SID675	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b11, 6-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
GPIO_SMC Specifications (Stepper Motor Control, 5 V I/Os)							
SID650A	V_{OL2}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V_{DDIO_SMC} ≥ 4.5 V
SID651A	V_{OL2}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V_{DDIO_SMC} ≥ 4.5 V
SID651E	V_{OL2}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, 2.7 V ≤ V_{DDIO_SMC} < 4.5 V
SID652A	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, V_{DDIO_SMC} ≥ 4.5 V
SID652E	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V_{DDIO_SMC} < 4.5 V
SID653A	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, V_{DDIO_SMC} ≥ 4.5 V
SID653E	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V_{DDIO_SMC} < 4.5 V
SID653B	V_{OL5}	Output voltage LOW level	–	–	0.5	V	I_{OL} = 30 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, 25°C < T_A ≤ 105°C, V_{DDIO_SMC} ≥ 4.5 V
SID653C	V_{OL5}	Output voltage LOW level	–	–	0.5	V	I_{OL} = 40 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –30°C < T_A ≤ 25°C, V_{DDIO_SMC} ≥ 4.5 V
SID653H	V_{OL5}	Output voltage LOW level	–	–	0.5	V	I_{OL} = 52 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –40°C ≤ T_A ≤ –30°C, V_{DDIO_SMC} ≥ 4.5 V
SID654A	V_{OH2}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, V_{DDIO_SMC} ≥ 4.5 V
SID654E	V_{OH2}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b01, 2.7 V ≤ V_{DDIO_SMC} < 4.5 V

Table 27-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID656A	V_{OH3}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $V_{DDIO\_SMC} \geq 4.5$ V
SID656E	V_{OH3}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, 2.7 V ≤ V_{DDIO_SMC} < 4.5 V
SID657A	V_{OH4}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $V_{DDIO\_SMC} \geq 4.5$ V
SID657E	V_{OH4}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, 2.7 V ≤ V_{DDIO_SMC} < 4.5 V
SID657B	V_{OH5}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OL} = –30 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, 25°C < T_A ≤ 105°C, $V_{DDIO\_SMC} \geq 4.5$ V
SID657C	V_{OH5}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OL} = –40 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –30°C < T_A ≤ 25°C, $V_{DDIO\_SMC} \geq 4.5$ V
SID657I	V_{OH5}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OL} = –52 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, –40°C < T_A ≤ –30°C, $V_{DDIO\_SMC} \geq 4.5$ V
SID658A	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID659A	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID659B	V_{OUT}	Mid range voltage level	2.45	–	2.55	V	CFG/DRIVE_MODE<2:0> = 0b001
SID660A	V_{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661A	V_{IH_TTL}	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662A	V_{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_SMC} ≤ 5.5 V
SID663A	V_{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDIO_SMC}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID664A	V_{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665A	V_{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDIO_SMC}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_SMC} ≤ 5.5 V
SID666A	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID668A	V_{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_SMC} ≤ 5.5 V
SID669A	C_{IN}	Input pin capacitance	–	–	7	pF	For 10 MHz and 100 MHz
SID670A	I_{IL}	Input leakage current	–2	–	2	µA	V_{DDIO_SMC} = V_{DDD} = 5.5 V, V_{SS} < V_I < V_{DDIO_SMC} –40°C ≤ T_A ≤ 105°C This is valid for the pin which do not have ADC input functionality.
SID673A	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	1	–	20	ns	5-mA drive strength 20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_OUT/SLOW<0:0> = 0b0, guaranteed by design
SID674A	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	1	–	20	ns	2-mA drive strength 10-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_OUT/SLOW<0:0> = 0b0, guaranteed by design

Table 27-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID675A	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	1	–	20	ns	1-mA drive strength 6-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b11, CFG_OUT/SLOW<0:0> = 0b0, guaranteed by design
SID676A	$t_{R\_F\_SMC\_SLOW}$	Fall time (10% to 90% of V_{DDIO_SMC})	15	–	80	ns	30-mA drive strength No load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676B	$t_{R\_F\_SMC\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	25	–	100	ns	30-mA drive strength 85-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676C	$t_{R\_F\_SMC\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	100	–	200	ns	30-mA drive strength 2.7-nF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
GPIO_ENH Specifications							
SID650C	V_{OL1}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $V_{DDIO\_GPIO} \geq 4.5$ V
SID650D	V_{OL1}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $V_{DDIO\_GPIO} \geq 4.5$ V
SID651C	V_{OL1}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID652C	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $V_{DDIO\_GPIO} \geq 4.5$ V
SID652F	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID653F	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $V_{DDIO\_GPIO} \geq 4.5$ V
SID653G	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID654C	V_{OH1}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $V_{DDIO\_GPIO} \geq 4.5$ V
SID654G	V_{OH1}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b0X, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID655C	V_{OH3}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $V_{DDIO\_GPIO} \geq 4.5$ V
SID656C	V_{OH3}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b10, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID657G	V_{OH4}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –1 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $V_{DDIO\_GPIO} \geq 4.5$ V
SID657H	V_{OH4}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –0.5 mA, CFG_OUT/DRIVE_SEL<1:0> = 0b11, $2.7\ V \leq V_{DDIO\_GPIO} < 4.5$ V
SID658C	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID659C	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID660C	V_{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661C	V_{IH_TTL}	Input voltage HIGH threshold in TTL mode	2	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662C	V_{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 $4.5\ V \leq V_{DDIO\_GPIO} \leq 5.5$ V
SID663C	V_{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0

Table 27-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID664C	V_{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665C	V_{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID666C	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID668C	V_{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID669C	C_{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID670C	I_{IL}	Input leakage current	–1	–	1	µA	$V_{DDIO\_GPIO} = V_{DDD}$ = 5.5 V, $V_{SS} < V_I < V_{DDIO\_GPIO}$ –40 °C ≤ T_A ≤ 105 °C
SID671C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	10	ns	20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range
SID672C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	50-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID673C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID674C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	10-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID675C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	6-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b11, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID676E	$t_{F\_I2C\_SLOW}$	Fall time (30% to 70% of V_{DDIO_GPIO})	20 × (V_{DDIO_GPIO} / 5.5)	–	250	ns	10-pF to 400-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, minimum external R_{PU} = 400 Ω
SID677C	$t_{R\_F\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	20 × (V_{DDIO_GPIO} / 5.5)	–	160	ns	20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, output frequency = 1 MHz
SID678C	$t_{R\_F\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	20 × (V_{DDIO_GPIO} / 5.5)	–	250	ns	400-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, output frequency = 400 kHz, Guaranteed by design
HSIO_STDLN Specifications (3 V I/Os)							
SID651F	V_{OL0}	Output LOW voltage level	–	–	0.2	V	I_{OL} = 0.1 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID654I	V_{OL1}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 10 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID655G	V_{OL2}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 2 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID656G	V_{OL3}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 1 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID656H	V_{OL4}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 0.5 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V

Table 27-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID658D	V_{OH0}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.2	–	–	V	I_{OH} = –0.1 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID661F	V_{OH1}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –10 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID662F	V_{OH2}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –2 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID663E	V_{OH3}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –1 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID663F	V_{OH4}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –0.5 mA, CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100, 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID664D	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID665F	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID667G	V_{IH0}	Input Voltage HIGH threshold	0.7 × V_{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID667I	V_{IH1}	Input Voltage HIGH threshold	2	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID671F	V_{IL0}	Input Voltage LOW threshold	–	–	0.3 × V_{DDIO_HSIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID671G	V_{IL1}	Input Voltage LOW threshold	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID674D	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID675D	C_{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID676H	I_{IL12}	Input leakage current	–1	–	1	µA	V_{DDIO_HSIO} = 3.6 V, V_{SS} < V_I < V_{DDIO_HSIO} –40°C ≤ T_A ≤ 105°C
GPIO Input Specifications							
SID98	t_{FT}	Analog glitch filter (pulse suppression width)	–	–	50[53]	ns	One filter per port group (required for some I^2C speeds)
SID99	t_{INT}	Minimum pulse width for GPIO interrupt	160	–	–	ns	

Note
53.If longer pulse suppression width is required, use Smart I/O.

27.6 Analog peripherals

27.6.1 SAR ADC

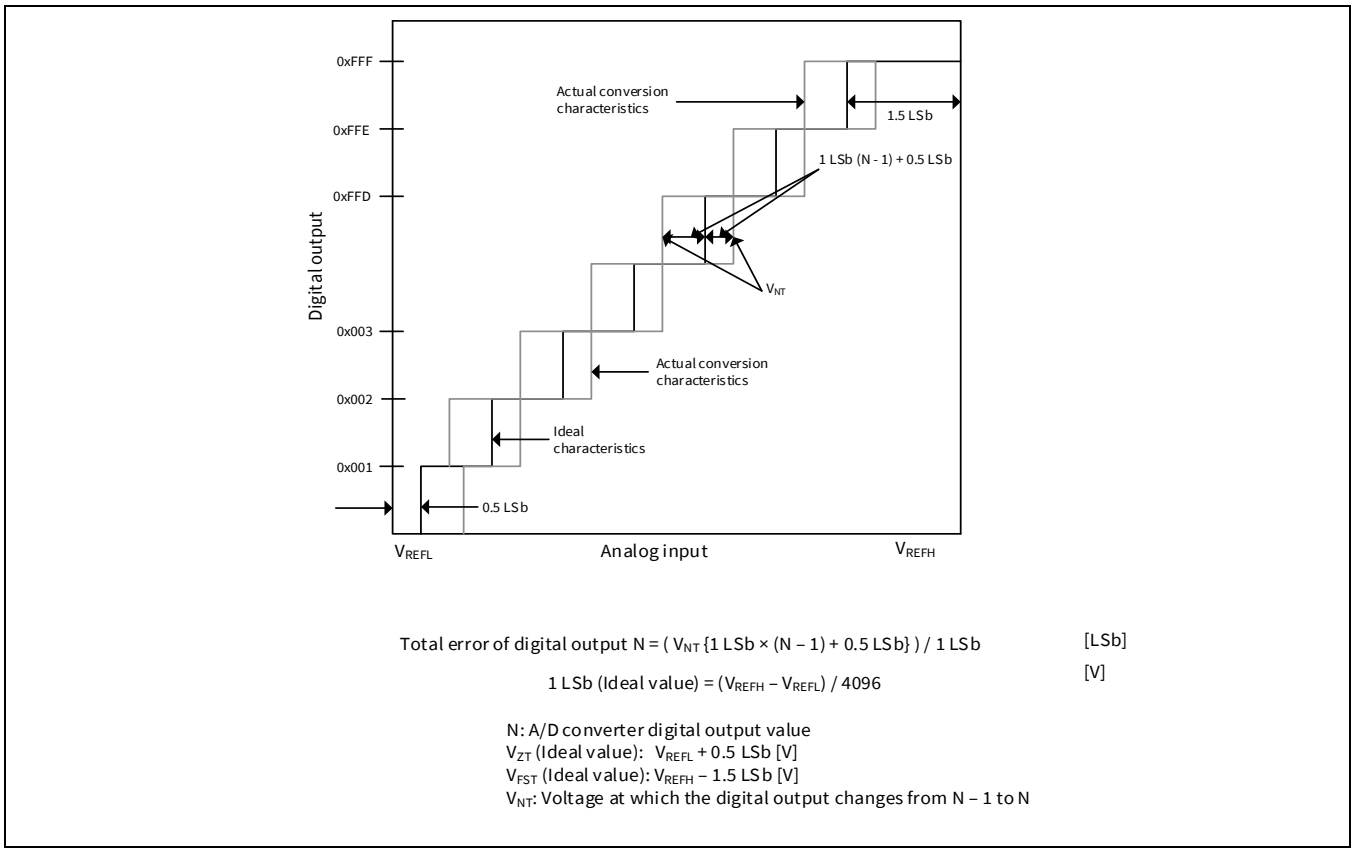
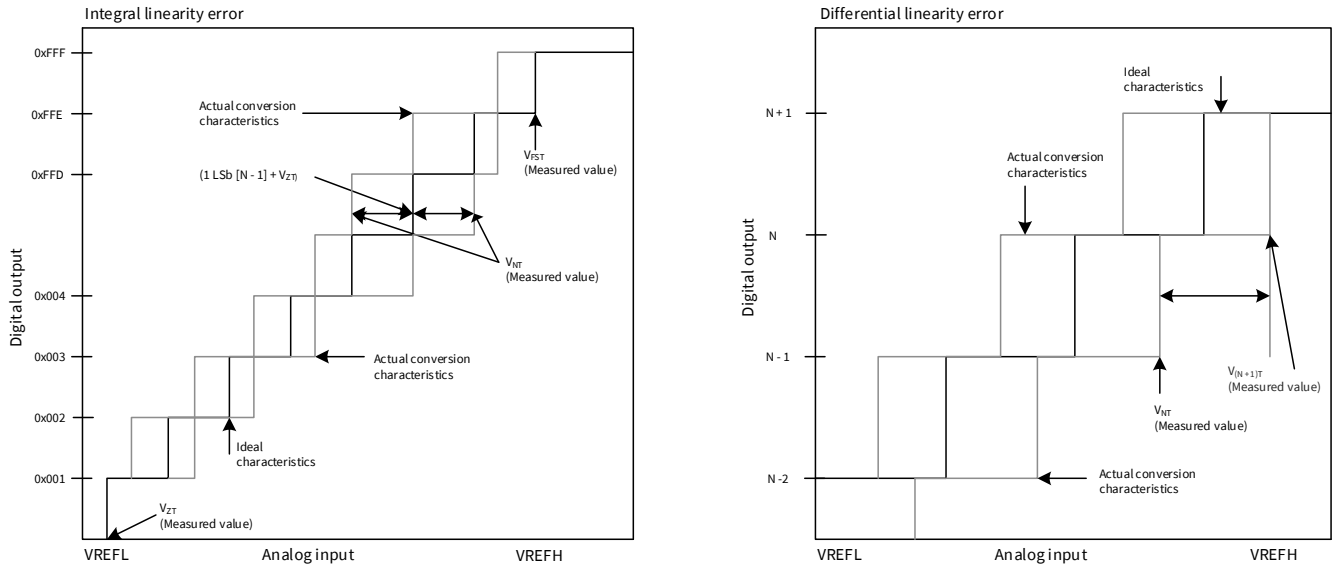


Figure 27-4 ADC characteristics and error definitions

Table 27-6 12-Bit SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID100	A_RES	SAR ADC resolution	–	–	12	bits	
SID101	V_{A_INV}	Input voltage range	V_{REFL}	–	V_{REFH}	V	
SID102	V_{REFH}	SAR ADC HIGH reference voltage range	2.7	–	V_{DDA_ADC}	V	ADC performance degrades when high reference is higher than supply
SID103	V_{REFL}	SAR ADC LOW reference voltage range	V_{SSA_ADC}	–	V_{SSA_ADC}	V	ADC performance degrades when low reference is lower than ground
SID103A	V_{BAND_GAP}	Internal band gap reference voltage	0.882	0.9	0.918	V	



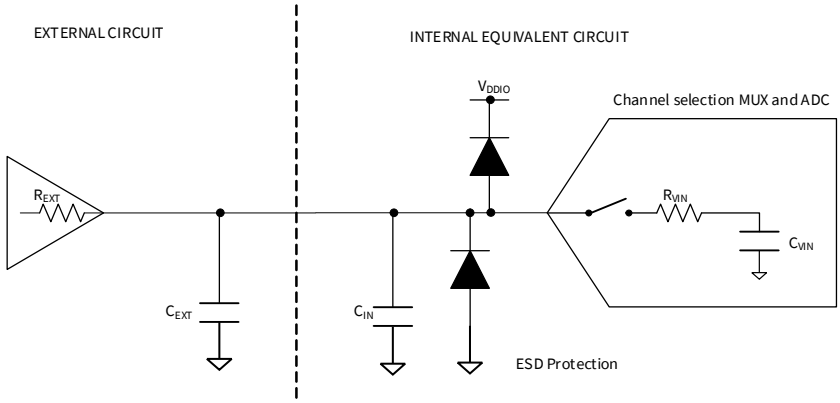
Integral linearity error of digital output N = (V_{NT} – {1 LSb × (N – 1) + V_{ZT}}) / 1 LSb [LSb]

Differential linearity error of digital output N = ($V_{(N+1)T}$ – V_{NT} – 1 LSb) / 1 LSb [LSb]

1 LSb = (V_{FST} – V_{ZT}) / 4094 [V]

V_{ZT}: Voltage for which digital output changes from 0x000 to 0x001
V_{FST}: Voltage for which digital output changes from 0xFFE to 0xFFF.

Figure 27-5 Integral and differential linearity errors



R_{EXT}: Source impedance
C_{EXT}: On-PCB capacitance
C_{IN}: I/O pad or Input capacitance
R_{VIN}: ADC equivalent input resistance
C_{VIN}: ADC equivalent input capacitance
K: Constant for sampling accuracy, K= ln(abs(4096/LSb_{SAMPLE}))

Sampling Time (t_{SAMPLE}) requirement is shown in the following equation
$t_{SAMPLE} > K \times \{ C_{VIN} \times (R_{VIN} + R_{EXT}) + (C_{IN} + C_{EXT}) \times (R_{EXT}) \}$ [seconds]

K = value of 9.0 is recommended to get ±0.5 LSb sampling accuracy at 12-bit (LSb_{SAMPLE} = ±0.5)

Figure 27-6 ADC equivalent circuit for analog input

Table 27-7 SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID104	V_{ZT}	Zero transition voltage	–20	–	20	mV	V_{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C before offset adjustment
SID105	V_{FST}	Full-scale transition voltage	–20	–	20	mV	V_{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C before offset adjustment
SID114	f_{ADC}	ADC operating frequency	2	–	26.67	MHz	
SID113	t_{S_4P5}	Analog input sample time (4.5 V ≤ V_{DDA_ADC}) for channels of SARMUX0	412	–	–	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113A	t_{S_2P7}	Analog input sample time (2.7 V ≤ V_{DDA_ADC}) for channels of SARMUX0	824	–	–	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113B	$t_{S\_DR\_4P5}$	Analog input sample time when input is from diagnostic reference (4.5 V ≤ V_{DDA_ADC})	2	–	–	µs	Guaranteed by design
SID113C	$t_{S\_DR\_2P7}$	Analog input sample time when input is from diagnostic reference (2.7 V ≤ V_{DDA_ADC})	2.5	–	–	µs	Guaranteed by design
SID113D	t_{S_TS}	Analog input sample time for temperature sensor	7	–	–	µs	Guaranteed by design
SID106	t_{ST1}	Max throughput (sample per second) for channels of SARMUX0	–	–	1	Msps	4.5 V ≤ V_{DDA_ADC} ≤ 5.5 V, 80 MHz / 3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles
SID106A	t_{ST2}	Max throughput (sample per second) for channels of SARMUX0	–	–	0.5	Msps	2.7 V ≤ V_{DDA_ADC} < 4.5 V, 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID107	C_{VIN}	ADC input sampling capacitance	–	–	4.8	pF	Guaranteed by design
SID108	R_{VIN1}	Input path ON resistance (4.5 V to 5.5 V)	–	–	9.4	kΩ	Guaranteed by design
SID108A	R_{VIN2}	Input path ON resistance (2.7 V to 4.5 V)	–	–	13.9	kΩ	Guaranteed by design
SID108B	R_{DREF1}	Diagnostic path ON resistance (4.5 V to 5.5 V)	–	–	40	kΩ	Guaranteed by design
SID108C	R_{DREF2}	Diagnostic path ON resistance (2.7 V to 4.5 V)	–	–	50	kΩ	Guaranteed by design
SID119	ACC_RLAD	Diagnostic reference resistor ladder accuracy	–4	–	4	%	

Table 27-7 SAR ADC AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID109	A_TE	Total error	–5	–	5	LSb	$V_{DDA\_ADC} = V_{REFH}$ = 2.7 V to 5.5 V, $V_{REFL} = V_{SSA\_ADC}$ –40°C ≤ T_A ≤ 105°C Total Error after offset and gain adjustment at 12-bit resolution mode
SID110	A_INL	Integral nonlinearity	–2.5	–	2.5	LSb	V_{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID111	A_DNL	Differential nonlinearity	–0.99	–	1.9	LSb	V_{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID112	A_GE	Measure the ADC output with input switching through all input channels of one ADC	–7	–	7	LSb	V_{DDA_ADC} = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID115	I_{AIC}	Analog input leakage current (GPIO_STD)	–350	–	350	nA	When input pad is selected for conversion, $V_{DDA\_ADC} = V_{REFH}$ = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID115D	I_{AIC}	Analog input leakage current (GPIO_SMC)	–1075	–	1075	nA	When input pad is selected for conversion, $V_{DDA\_ADC} = V_{REFH}$ = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID115A	I_{AIC2}	Analog input leakage current (GPIO_STD)	–	–	165	nA	When input pad is not selected for conversion, $V_{DDA\_ADC} = V_{REFH}$ = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID115E	I_{AIC2}	Analog input leakage current (GPIO_SMC)	–	–	1015	nA	When input pad is not selected for conversion, $V_{DDA\_ADC} = V_{REFH}$ = 2.7 V to 5.5 V, –40°C ≤ T_A ≤ 105°C
SID116	$I_{DIAGREF}$	Diagnostic reference current	–	–	70	µA	
SID117	I_{VDDA}	Analog power supply current while ADC is operating	–	360	550	µA	Per enabled ADC, without diagnosis
SID117A	I_{VDDA_DS}	Analog power supply current while ADC is not operating	–	1	21	µA	Per enabled ADC

Table 27-7 SAR ADC AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID118	I_{VREF}	Analog reference voltage current while ADC is operating	–	360	550	µA	Per enabled ADC, without diagnosis
SID118A	I_{VREF_LEAK}	Analog reference voltage current while ADC is not operating	–	1.8	5	µA	Per enabled ADC
SID118B	$t_{S\_4P5\_1}$	Analog input sample time (4.5 V ≤ V_{DDA_ADC}) for channels of SARMUX1	824	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design
SID118C	$t_{S\_2P7\_1}$	Analog input sample time (2.7 V ≤ V_{DDA_ADC}) for channels of SARMUX1	1648	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design
SID119A	t_{ST3}	Max throughput (sample per second) for channels of SARMUX1	–	–	0.5	Msps	4.5 V ≤ V_{DDA_ADC} ≤ 5.5 V, 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID119B	t_{ST4}	Max throughput (sample per second) for channels of SARMUX1	–	–	0.25	Msps	2.7 V ≤ V_{DDA_ADC} < 4.5 V, 80 MHz / 12 = 6.67 MHz, 11 sampling cycles, 15 conversion cycles

27.6.2 Temperature sensor

Table 27-8 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID201	$T_{SENSACC\_TR}$	Temperature sensor accuracy trimmed	–5	–	5	°C	This spec is valid for the following two conditions: 1. 3.0 V ≤ V_{DDA_ADC}=V_{REFH} ≤ 3.6 V and 3.0 V ≤ V_{DDD} ≤ 3.6 V 2. 4.5 V ≤ V_{DDA_ADC}=V_{REFH} ≤ 5.5 V and 4.5 V ≤ V_{DDD} ≤ 5.5 V (Calibrated accuracy by factory trimming)
SID202	$T_{SENSAC-C\_STD}$	Temperature sensor accuracy standard	–10	–	10	°C	This spec applies to all valid combinations for V_{DDA_ADC} = V_{REFH} and V_{DDD}, which are not covered by SID201 (Uncalibrated accuracy)

27.7 AC specifications

Unless otherwise noted, the timings are defined with the guidelines mentioned in the **Figure 27-7**

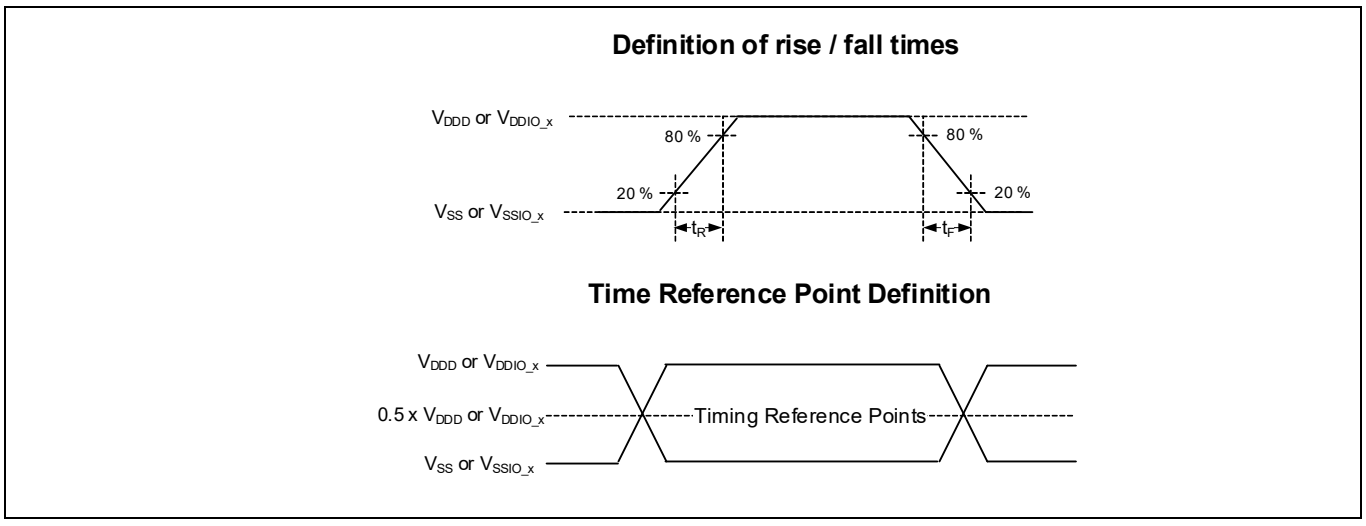


Figure 27-7 AC timings specifications

27.8 Digital peripherals

Table 27-9 Timer/Counter/PWM (TCPWM) specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID120	f_C	TCPWM operating frequency	–	–	100	MHz	f_C = peripheral clock
SID121	$t_{PWMENEXT}$	Input trigger pulse width for all trigger events	2 / f_C	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID122	t_{PWMEXT}	Output trigger pulse widths	2 / f_C	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID123	t_{CRES}	Resolution of counter	1 / f_C	–	–	ns	Minimum time between successive counts
SID124	t_{PWMRES}	PWM resolution	1 / f_C	–	–	ns	Minimum pulse width of PWM output
SID125	t_{QRES}	Quadrature inputs resolution	2 / f_C	–	–	ns	Minimum pulse width between Quadrature phase inputs.

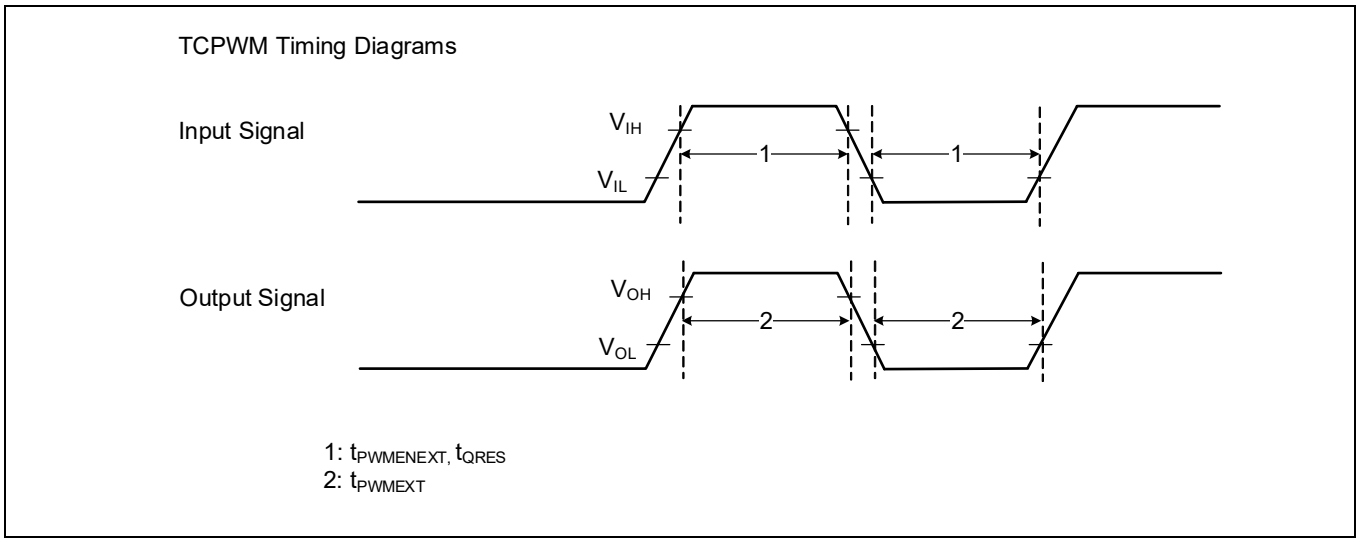


Figure 27-8 TCPWM timing diagrams

Table 27-10 Serial communication block (SCB) specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID129	f_{SCB}	SCB operating frequency	–	–	100	MHz	
SID129_2	t_{SPI_TRANS}	SCB transition in SPI mode	–	–	4	ns	
I²C Interface-Standard-mode							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0>=0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, , CFG_SLEW_EXT/SLEW<2:0> =0b000 (**Note**: SID138 is not valid for *HSIO_STDLN*)						
SID130	f_{SCL}	SCL clock frequency	–	–	100	kHz	
SID131	$t_{HD;STA}$	Hold time, START condition	4000	–	–	ns	
SID132	t_{LOW}	Low period of SCL	4700	–	–	ns	
SID133	t_{HIGH}	High period of SCL	4000	–	–	ns	
SID134	$t_{SU;STA}$	Setup time for a repeated START	4700	–	–	ns	
SID135	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	
SID136	$t_{SU;DAT}$	Data setup time	250	–	–	ns	
SID138	t_F	Fall time of SCL and SDA	–	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC, GPIO_STD
SID139	$t_{SU;STO}$	Setup time for STOP	4000	–	–	ns	
SID140	t_{BUF}	Bus-free time between START and STOP	4700	–	–	ns	
SID141	C_B	Capacitive load for each bus line	–	–	400	pF	
SID142	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	3450	ns	
SID143	$t_{VD;ACK}$	Data valid acknowledge time	–	–	3450	ns	
I²C Interface-Fast-mode							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 (**Note**: SID158 is not valid for *GPIO_STD*) **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0>=0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_SLEW_EXT/SLEW<2:0> =0b000 (**Note**: SID158 is not valid for *HSIO_STDLN*)						
SID150	f_{SCL_F}	SCL clock frequency	–	–	400[54]	kHz	
SID151	$t_{HD;STA\_F}$	Hold time, START condition	600	–	–	ns	
SID152	t_{LOW_F}	Low period of SCL	1300	–	–	ns	
SID153	t_{HIGH_F}	High period of SCL	600	–	–	ns	
SID154	$t_{SU;STA}$	Setup time for a repeated START	600	–	–	ns	
SID155	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	
SID156	$t_{SU;DAT}$	Data setup time	100	–	–	ns	
SID158	t_F	Fall time of SCL and SDA	$20 \times (V_{DDIO\_GPIO}/5.5)$	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC
SID159	$t_{SU;STO}$	Setup time for STOP	600	–	–	ns	
SID160	t_{BUF}	Bus free time between START and STOP	1300	–	–	ns	
SID161	C_B	Capacitive load for each bus line	–	–	400	pF	

Notes
54. To drive full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL}.
55. To drive full bus load at 1 MHz, 20 mA I_{OL} is required at 0.4 V V_{OL}. However, this device does not support it.

Table 27-10 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID162	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	900	ns	
SID163	$t_{VD;ACK}$	Data valid acknowledge time	–	–	900	ns	
SID164	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
I^2C Interface-Fast-Plus mode							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 (**Note**: SID178 is not valid for *GPIO_STD*) **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0 (**Note**: SID178 is not valid for *GPIO_SMC*) **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 CFG_SLEW_EXT/SLEW<2:0> = 0b000 (**Note:** SID178 is not valid for HSIO_STDLN)						
SID170	f_{SCL_FP}	SCL clock frequency	–	–	1[55]	MHz	
SID171	$t_{HD;STA\_FP}$	Hold time, START condition	260	–	–	ns	
SID172	t_{LOW_FP}	Low period of SCL	500	–	–	ns	
SID173	t_{HIGH_FP}	High period of SCL	260	–	–	ns	
SID174	$t_{SU;STA}$	Setup time for a repeated START	260	–	–	ns	
SID175	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	
SID176	$t_{SU;DAT}$	Data setup time	50	–	–	ns	
SID178	t_F	Fall time of SCL and SDA	20 × (V_{DDIO_GPIO} /5.5)	–	160	ns	Input and output, 20pF load Output: Only for GPIO_ENH
SID179	$t_{SU;STO}$	Setup time for STOP	260	–	–	ns	
SID180	t_{BUF}	Bus free time between START and STOP	500	–	–	ns	
SID181	C_B	Capacitive load for each bus line	–	–	20	pF	
SID182	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	450	ns	
SID183	$t_{VD;ACK}$	Data valid acknowledge time	–	–	450	ns	
SID184	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	

SPI Interface

Recommended I/O Configuration: (Applicable to all below SPI modes)
HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> =0b000

For SPI speeds ≤ 12.5 MHz
GPIO_STD: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0
GPIO_ENH: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0
GPIO_SMC: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0

SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, GPIO)							
SID190	f_{SPI}	SPI operating frequency	–	–	12.5	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID191	t_{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC

Table 27-10 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID192	t_{DSI}	SPI Master: MISO valid before SCLK capturing edge	40	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID193	t_{HMO}	SPI Master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID194	$t_{W\_SCLK\_H\_L}$	SPI SCLK pulse width HIGH or LOW	0.4 × (1 / f_{SPI})	0.5 × (1 / f_{SPI})	0.6 × (1 / f_{SPI})	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID195	t_{VSS}	SPI Master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID196	t_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID198	t_{EN_SETUP}	SSEL valid, before the first SCK capturing edge	0.5 × (1 / f_{SPI})	–	–	ns	Min is half clock period
SID199	t_{EN_SHOLD}	SSEL hold, after the last SCK capturing edge	0.5 × (1 / f_{SPI})	–	–	ns	Min is half clock period
SID197	C_{SPIM_MS}	SPI Capacitive Load	–	–	20	pF	
SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, HSIO)							
SID190A	f_{SPI}	SPI operating frequency	–	–	20	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz. for instances on HSIO_STDLN
SID191A	t_{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	9	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN

Table 27-10 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID192A	t_{DSI}	SPI Master: MISO valid before SCLK capturing edge	25	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID193A	t_{HMO}	SPI Master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID194A	$t_{W\_SCLK\_H\_L}$	SPI SCLK pulse width HIGH or LOW	0.4 × (1 / f_{SPI})	0.5 × (1 / f_{SPI})	0.6 × (1 /f_{SPI})	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID195A	t_{VSS}	SPI Master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID196A	t_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STDLN
SID197A	C_{SPIM_MS}	SPI Capacitive Load	–	–	20	pF	
SID198A	t_{EN_SETUP}	SSEL valid, before the first SCK capturing edge	0.5 × (1 / f_{SPI})	–	–	ns	Min is half clock period
SID199A	t_{EN_SHOLD}	SSEL hold, after the last SCK capturing edge	0.5 × (1 / f_{SPI})	–	–	ns	Min is half clock period
SPI Interface Slave (internally clocked, GPIO and HSIO)							
SID205	f_{SPI_INT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, internally clocked
SID206	t_{DMI_INT}	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI Slave, internally clocked
SID207	t_{DSO_INT}	SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode	–	–	60	ns	SPI Slave, internally clocked
SID208	t_{HSO_INT}	SPI Slave: Previous MISO data hold time	3	–	–	ns	SPI Slave, internally clocked
SID209	$t_{EN\_SETUP\_INT}$	SPI Slave: SSEL valid to first SCK valid edge	33	–	–	ns	SPI Slave, internally clocked
SID210	$t_{EN\_HOLD\_INT}$	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI Slave, internally clocked

Table 27-10 Serial communication block (SCB) specifications *(continued)*

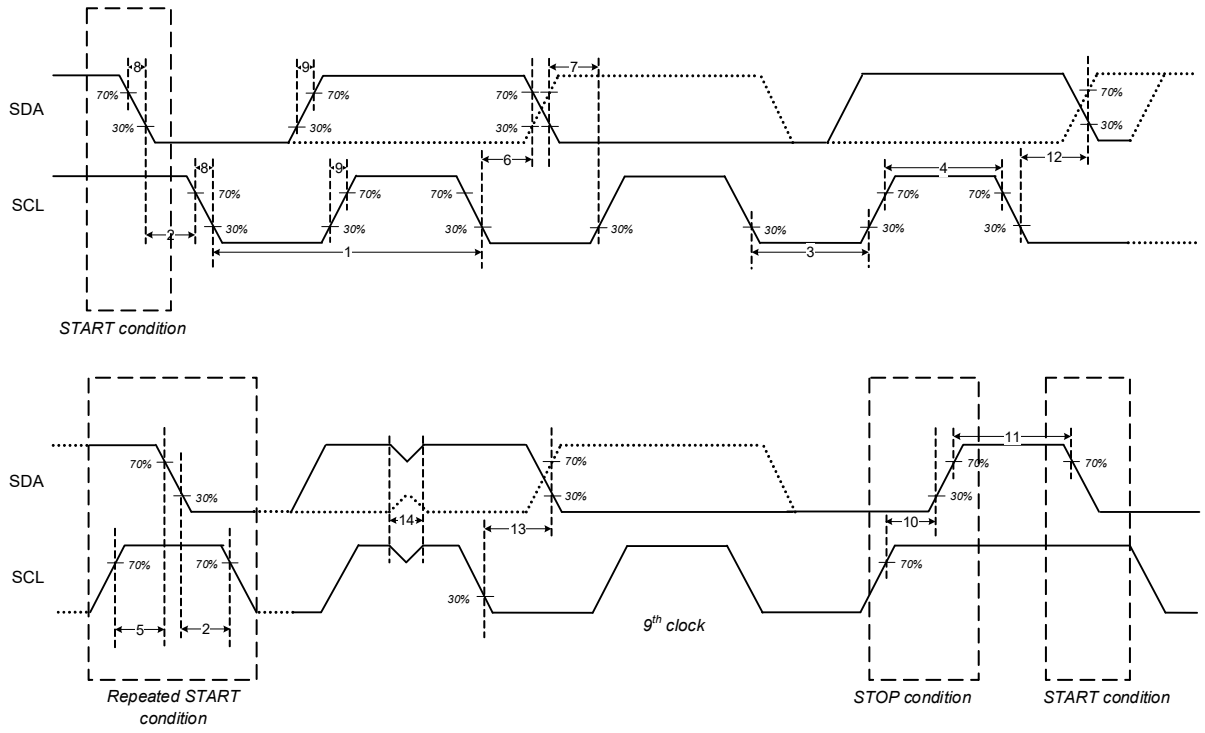
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID211	$t_{EN\_SETUP\_PRE}$	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID212	$t_{EN\_HOLD\_PRE}$	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID213	$t_{EN\_SETUP\_CO}$	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID214	$t_{EN\_HOLD\_CO}$	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID215	$t_{W\_DIS\_INT}$	SPI Slave Select inactive time	40	–	–	ns	SPI Slave, internally clocked
SID216	$t_{W\_SCLKH\_INT}$	SPI SCLK pulse width HIGH	32	–	–	ns	SPI Slave, internally clocked
SID217	$t_{W\_SCLKL\_INT}$	SPI SCLK pulse width LOW	32	–	–	ns	SPI Slave, internally clocked
SID218	t_{SIH_INT}	SPI MOSI hold from SCLK	20	–	–	ns	SPI Slave, internally clocked
SID219	C_{SPI_INT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, internally clocked
SPI Interface Slave (externally clocked, GPIO and HSIO)							
SID220	f_{SPI_EXT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, externally clocked: 12.5 Mbps
SID221	t_{DMI_EXT}	SPI Slave: MOSI Valid before Sclock capturing edge	8	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID222	t_{DSO_EXT}	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	30	ns	SPI Slave, externally clocked: 12.5 Mbps
SID223	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID224	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID225	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID226	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID227	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	32	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID228	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	32	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID229	t_{SIH_EXT}	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID230	C_{SPIS_EXT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 12.5 Mbps
SID231	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns	SPI Slave, externally clocked: 12.5 Mbps
SPI Interface Slave (internally clocked, SMC I/O)							
SID205_2	f_{SPI_INT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, internally clocked
SID206_2	t_{DMI_INT}	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI Slave, internally clocked
SID207_2	t_{DSO_INT}	SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode	–	–	64	ns	SPI Slave, internally clocked
SID208_2	t_{HSO_INT}	SPI Slave: Previous MISO data hold time	3	–	–	ns	SPI Slave, internally clocked
SID209_2	$t_{EN\_SETUP\_INT}$	SPI Slave: SSEL valid to first SCK valid edge	33	–	–	ns	SPI Slave, internally clocked
SID210_2	$t_{EN\_HOLD\_INT}$	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI Slave, internally clocked
SID211_2	$t_{EN\_SETUP\_PRE}$	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns	SPI Slave, internally clocked

Table 27-10 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID212_2	$t_{EN\_HOLD\_PRE}$	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID213_2	$t_{EN\_SETUP\_CO}$	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID214_2	$t_{EN\_HOLD\_CO}$	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID215_2	$t_{W\_DIS\_INT}$	SPI Slave Select inactive time	40	–	–	ns	SPI Slave, internally clocked
SID216_2	$t_{W\_SCLKH\_INT}$	SPI SCLK pulse width HIGH	36	–	–	ns	SPI Slave, internally clocked
SID217_2	$t_{W\_SCLKL\_INT}$	SPI SCLK pulse width LOW	36	–	–	ns	SPI Slave, internally clocked
SID218_2	t_{SIH_INT}	SPI MOSI hold from SCLK	20	–	–	ns	SPI Slave, internally clocked
SID219_2	C_{SPIS_INT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, internally clocked
SPI Interface Slave (externally clocked, SMC I/O)							
SID220_2	f_{SPI_EXT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, externally clocked: 12.5 Mbps
SID221_2	t_{DMI_EXT}	SPI Slave: MOSI Valid before Sclock capturing edge	8	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID222_2	t_{DSO_EXT}	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	34	ns	SPI Slave, externally clocked: 12.5 Mbps
SID223_2	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID224_2	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID225_2	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID226_2	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID227_2	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	36	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID228_2	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	36	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID229_2	t_{SIH_EXT}	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID230_2	C_{SPIS_EXT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 12.5 Mbps
SID231_2	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	37	ns	SPI Slave, externally clocked: 12.5 Mbps
SPI Interface Slave (externally clocked, 20 MHz)							
SID220A	f_{SPI_EXT}	SPI operating frequency	–	–	20	MHz	SPI Slave, externally clocked: 20 Mbps
SID221A	t_{DMI_EXT}	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID222A	t_{DSO_EXT}	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	18	ns	SPI Slave, externally clocked: 20 Mbps
SID223A	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID224A	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID225A	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID226A	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID227A	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps

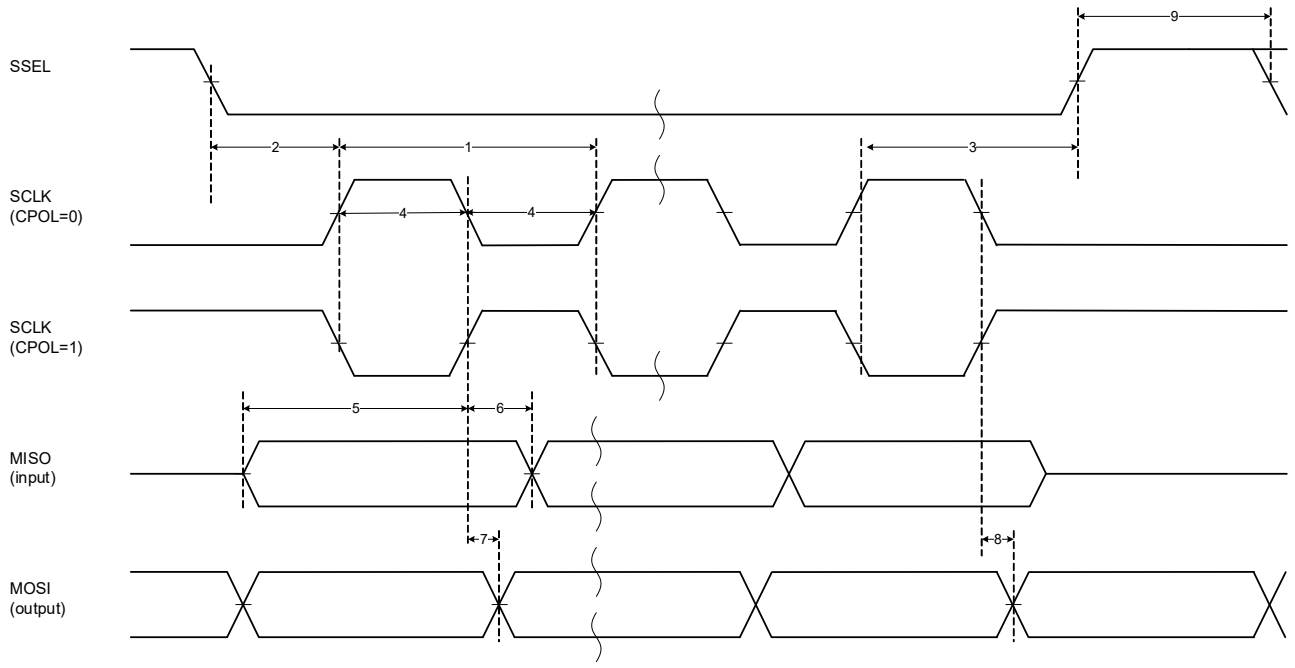
Table 27-10 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID228A	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID229A	t_{SIH_EXT}	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID230A	C_{SPIS_EXT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 20 Mbps
SID231A	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	23	ns	SPI Slave, externally clocked: 20 Mbps
UART Interface							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> =0b000							
SID240	f_{BPS}	Signaling rate	–	–	10	Mbps	



1: SCL clock period = $1/f_{SCL}$
2: Hold time, START condition = $t_{HD;STA}$
3: LOW period of SCL = t_{LOW}
4: HIGH period of SCL = t_{HIGH}
5: Setup time for a repeated START = $t_{SU;STA}$
6: Data hold time, for receiver = $t_{HD;DAT}$
7: Data setup time = $t_{SU;DAT}$
8: Fall time of SCL and SDA = t_F
9: Rise time of SCL and SDA = t_R
10: Setup time for STOP = $t_{SU;STO}$
11: Bus-free time between START and STOP = t_{BUF}
12: Time for data signal from SCL LOW to SDA output = $t_{VD;DAT}$
13: Data valid acknowledge time = $t_{VD;ACK}$
14: Pulse width of spikes that must be suppressed by the input filter = t_{SP}

Figure 27-9 I^2C timing diagrams



1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{DHI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data hold time = t_{HMO}
9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

Figure 27-10 SPI master timing diagrams with LOW clock phase

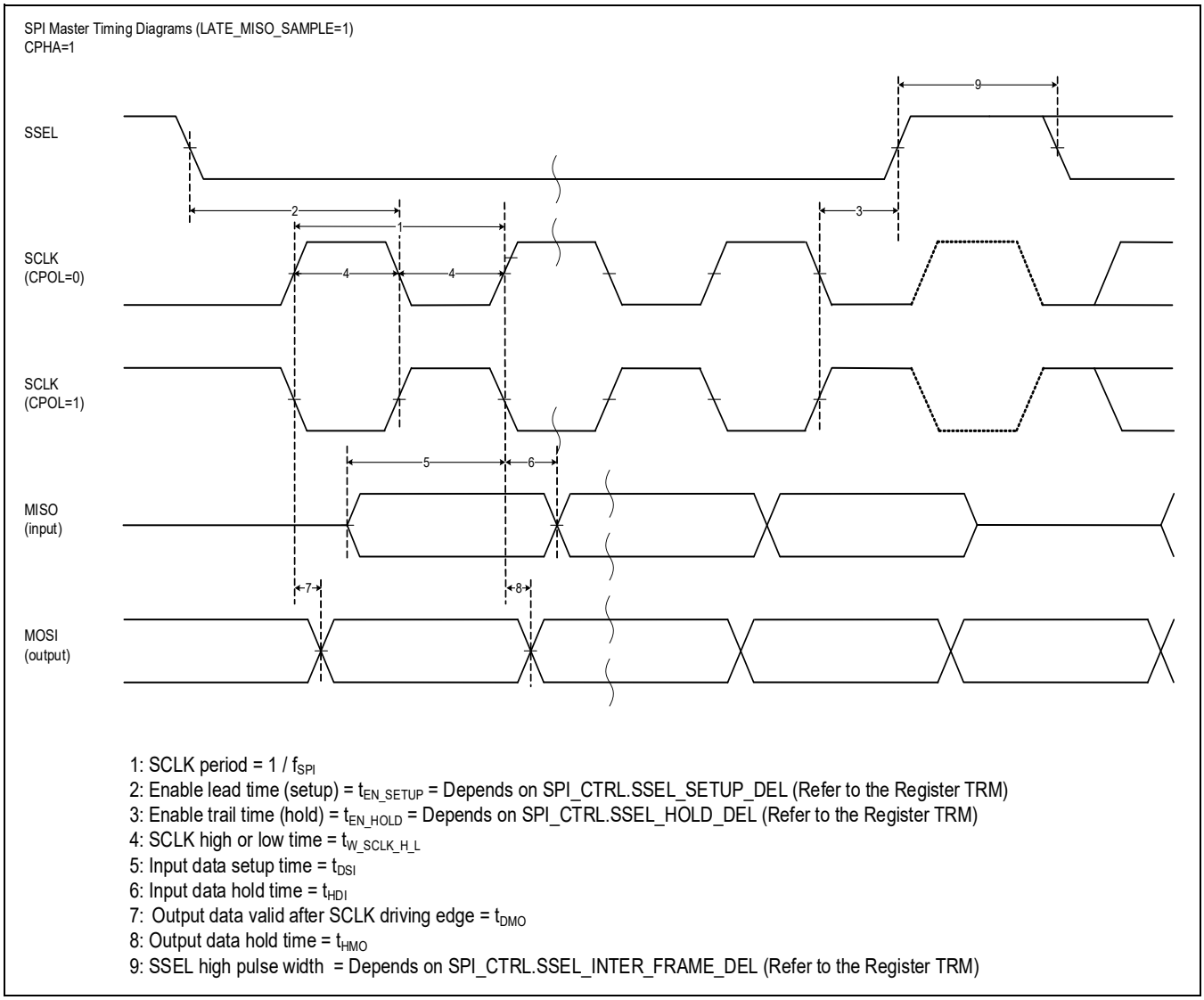


Figure 27-11 SPI master timing diagrams with HIGH clock phase

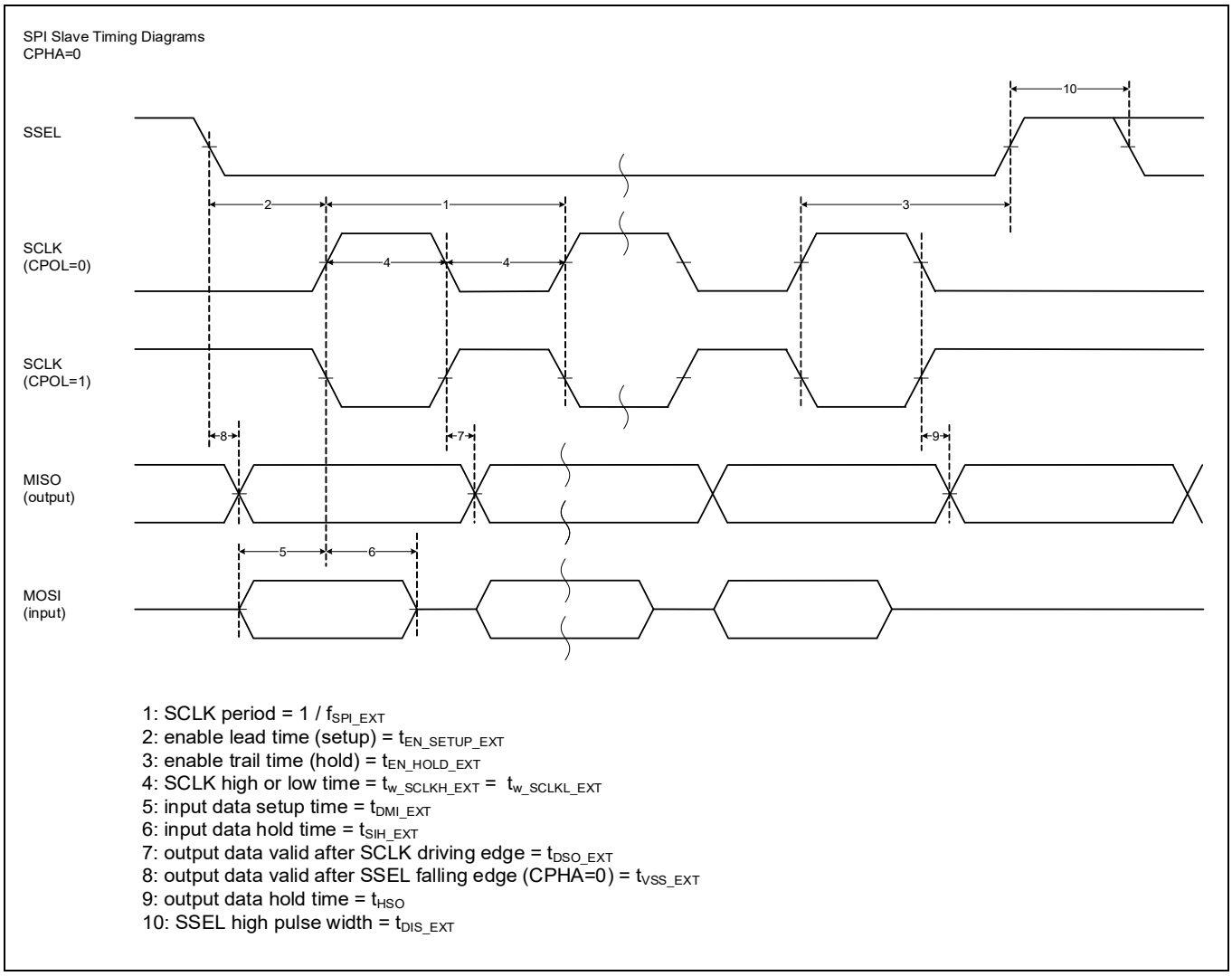


Figure 27-12 SPI slave timing diagrams with LOW clock phase

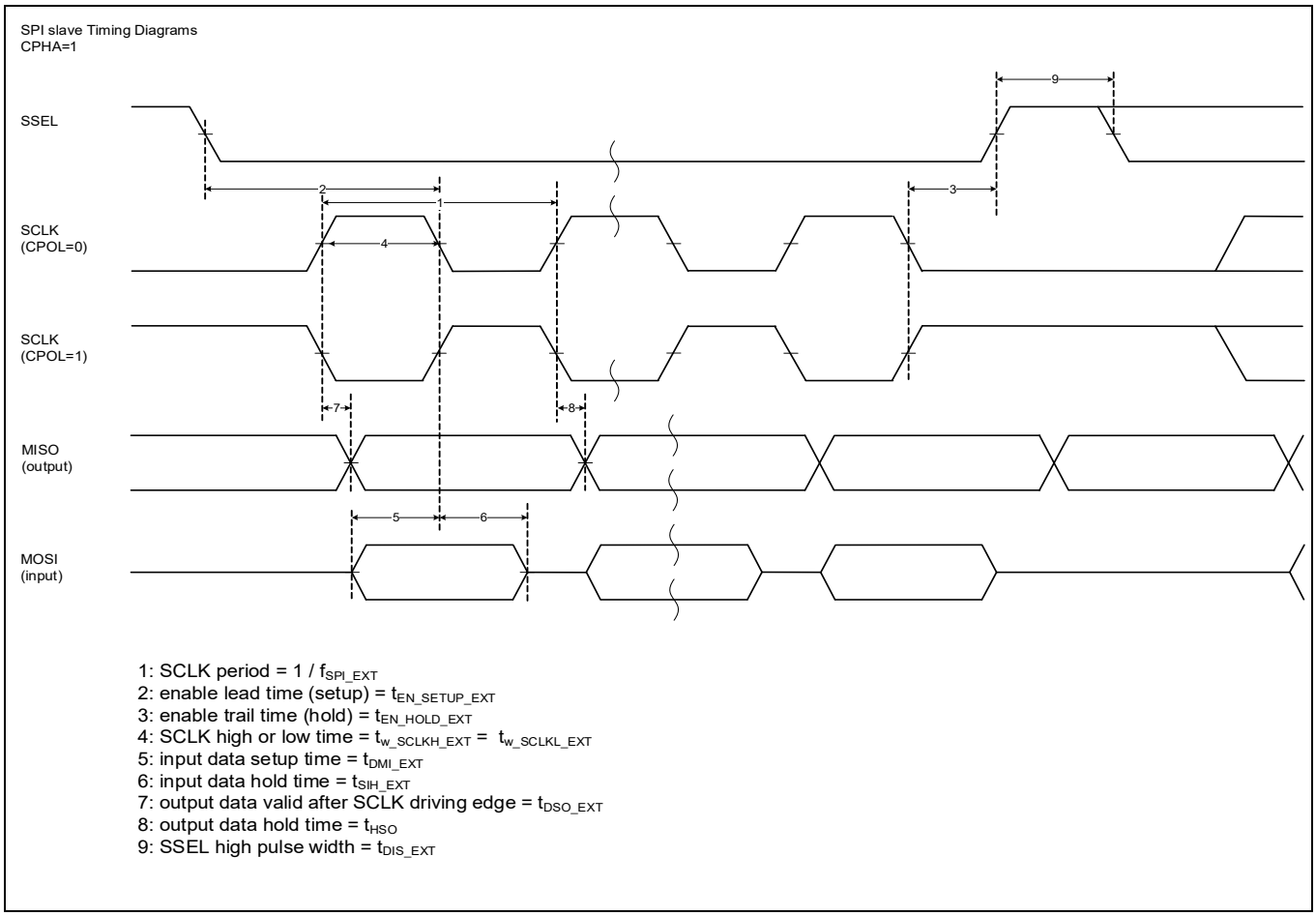


Figure 27-13 SPI slave timing diagrams with HIGH clock phase

27.8.1 LIN specifications

Table 27-11 LIN specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID249	f_{LIN}	Internal clock frequency to the LIN block	–	–	100	MHz	
SID250	BR_NOM	Bit rate on the LIN bus	1	–	20	kbps	Guaranteed by design
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	–	115.2	kbps	Guaranteed by design

27.8.2 CAN FD specifications

Table 27-12 CAN FD specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID630	f_{HCLK}	System clock (HCLK) frequency	–	–	100	MHz	$f_{CCLK} \le f_{HCLK}$, guaranteed by design
SID631	f_{CCLK}	CAN clock (CCLK) frequency	–	–	100	MHz	$f_{CCLK} \le f_{HCLK}$, guaranteed by design

27.9 Memory

Table 27-13 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257A	V_{PE}	Erase and program voltage	2.7	–	5.5	V	

Table 27-14 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257	f_{FO}	Maximum operation frequency	–	–	100	MHz	Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 320 MHz
SID254	t_{ERS_SUS}	Maximum time from erase suspend command till erase is indeed suspend	–	–	37.5	µs	
SID255	$t_{ERS\_RES\_SUS}$	Minimum time allowed from erase resume to erase suspend	250	–	–	µs	Guaranteed by design
SID258	t_{BC_WF}	Blank Check time for Work Flash N-byte	–	–	10 + 0.3 × N	µs	At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time
SID258A	$t_{AA\_BC\_ENTRY}$	Time to enter Blank Check mode	–	5	–	µs	
SID258B	$t_{AA\_BC\_EXIT}$	Time to exit Blank Check mode	–	5	–	µs	
SID259	$t_{SECTORE-RASE1}$	Sector erase time (code-flash: 32 KB)	–	45	90	ms	Includes internal preprogramming time
SID260	$t_{SECTORE-RASE2}$	Sector erase time (code-flash: 8 KB)	–	15	30	ms	Includes internal preprogramming time

Table 27-14 Flash AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID261	$t_{SECTORE-RASE3}$	Sector erase time (work-flash, 2 KB)	–	80	160	ms	Includes internal preprogramming time
SID262	$t_{SECTORE-RASE4}$	Sector erase time (work-flash, 128 B)	–	5	15	ms	Includes internal preprogramming time
SID263	t_{WRITE1}	64-bit write time (code-flash)	–	30	60	µs	Excludes system overhead time
SID264	t_{WRITE2}	256-bit write time (code-flash)	–	40	70	µs	Excludes system overhead time
SID265	t_{WRITE3}	4096-bit write time (code-flash)	–	320	1200	µs	Excludes system overhead time
SID266	t_{WRITE4}	32-bit write time (work-flash)	–	30	60	µs	Excludes system overhead time
SID267	t_{FRET1}	Code-flash retention. 1000 program/erase cycles	20	–	–	years	Temperature at write/erase time. $T_A \leq +85°C$ average
SID182T1	t_{FRET2}	Code-flash retention. 100 program/erase cycles	50	–	–	years	Temperature at write/erase time. $T_A \leq +30°C$ average
SID268	t_{FRET3}	Work-flash retention. 125,000 program/erase cycles	20	–	–	years	Temperature at write/erase time. $T_A \leq +85°C$ average
SID269	t_{FRET4}	Work-flash retention. 250,000 program/erase cycles	10	–	–	years	Temperature at write/erase time. $T_A \leq +85°C$ average
SID182T2	t_{FRET5}	Work-flash retention. 1000 program/erase cycles	50	–	–	years	Temperature at write/erase time. $T_A \leq +30°C$ average
SID612	I_{CC_ACT2}	Program operating current (code or work-flash)	–	15	62	mA	$V_{DDD} = 5$ V, $V_{CCD} = 1.1$ V Guaranteed by design
SID613	I_{CC_ACT3}	Erase operating current (code- or work-flash)	–	15	62	mA	$V_{DDD} = 5$ V, $V_{CCD} = 1.1$ V Guaranteed by design

27.10 System resources

Table 27-15 System resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
Power-on-reset specifications							
SID270	V_{POR_R}	POR rising trip voltage	1.5	–	2.35	V	Guaranteed by design
SID276	V_{POR_F}	POR falling trip voltage	1.45	–	2.1	V	
SID271	V_{POR_H}	Level detection hysteresis	20	–	300	mV	
SID272	t_{DLY_POR}	Delay between V_{DDD} rising through 2.3 V and POR reset output rising through V_{DDD} / 2	–	–	3	µs	Guaranteed by design
SID273	t_{POFF}	Power off time	350	–	–	µs	V_{DDD} < 1.45 V Does not apply to SID274A and SID274B
SID274A	POR_RR1	V_{DDD} power ramp rate with robust BOD - XRES_L asserted (BOD operation is guaranteed)	–	–	100	mV/µs	Applies to ramp up and ramp down
SID274B	POR_RR1	V_{DDD} power ramp rate with robust BOD - XRES_L de-asserted (BOD operation is guaranteed)	1	–	100	mV/µs	Applies to ramp up and ramp down
SID275	POR_RR2	V_{DDD} power ramp rate without robust BOD	100	–	1000	mV/µs	This ramp does not support robust BOD t_{POFF} must be satisfied. Applies to ramp up and ramp down
High-voltage BOD (HV BOD) specifications							
SID500	$V_{TR\_2P7\_R}$	HV BOD 2.7 V trimmed rising trip point for V_{DDD} and V_{DDA_ADC} (default)	2.474	2.55	2.627	V	
SID501	$V_{TR\_2P7\_F}$	HV BOD 2.7 V trimmed falling trip point for V_{DDD} and V_{DDA_ADC} (default)	2.449	2.525	2.601	V	
SID502	$V_{TR\_3P0\_R}$	HV BOD 3.0 V trimmed rising trip point for V_{DDD} and V_{DDA_ADC}	2.765	2.85	2.936	V	
SID503	$V_{TR\_3P0\_F}$	HV BOD 3.0 V trimmed falling trip point for V_{DDD} and V_{DDA_ADC}	2.74	2.825	2.91	V	
SID505	HVBOD_RR_A	Power ramp rate: V_{DDD} and V_{DDA_ADC} (Active)	–	–	100	mV/µs	
SID506	HVBOD_RR_DS	Power ramp rate: V_{DDD} and V_{DDA_ADC} (DeepSleep)	–	–	10	mV/µs	
SID507	$t_{DLY\_ACT\_HVBOD}$	Active mode delay between V_{DDD} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and an internal HV BOD output transitioning through V_{DDD} / 2	–	–	0.5	µs	Guaranteed by design

Table 27-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID507A	$t_{DLY\_ACT\_H-VBOD\_A}$	Active mode delay between V_{DDA_ADC} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and internal HV BOD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID507B	$t_{DLY\_DS\_HVBOD}$	DeepSleep mode delay between V_{DDD}/V_{DDA_ADC} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and an internal HV BOD output transitioning through V_{DDD} / 2	–	–	4	µs	Guaranteed by design
SID508	t_{RES_HVBOD}	Response time of HV BOD, V_{DDD}/V_{DDA_ADC} supply. HV BOD guaranteed to generate pulse for V_{DDD}/V_{DDA_ADC} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below $V_{TR\_2P7\_F}$ or $V_{TR\_3P0\_F}$)	100	–	–	ns	Guaranteed by design
Low-voltage BOD (LV BOD) specifications							
SID510	$V_{TR\_R\_LVBOD}$	LV BOD trimmed rising trip point for V_{CCD}	0.917	0.945	0.973	V	
SID511	$V_{TR\_F\_LVBOD}$	LV BOD trimmed falling trip point for V_{CCD}	0.892	0.92	0.948	V	
SID515	$t_{DLY\_ACT\_LVBOD}$	Active delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID515A	$t_{DLY\_DS\_LVBOD}$	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD output transitioning through V_{DDD} / 2	–	–	12	µs	Guaranteed by design
SID516	t_{RES_LVBOD}	Response time of LV BOD. LV BOD guaranteed to generate pulse for V_{CCD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below $V_{TR\_F\_LVBOD}$)	100	–	–	ns	Guaranteed by design
Low-voltage detector (LVD) DC specifications							
SID520	$V_{TR\_2P8\_F}$	LVD 2.8 V trimmed falling trip point for V_{DDD}	Typ – 4%	2800	Typ + 4%	mV	
SID521	$V_{TR\_2P9\_F}$	LVD 2.9 V trimmed falling trip point for V_{DDD}	Typ – 4%	2900	Typ + 4%	mV	
SID522	$V_{TR\_3P0\_F}$	LVD 3.0 V trimmed falling trip point for V_{DDD}	Typ – 4%	3000	Typ + 4%	mV	

Table 27-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID523	$V_{TR\_3P1\_F}$	LVD 3.1 V trimmed falling trip point for V_{DDD}	Typ – 4%	3100	Typ + 4%	mV	
SID524	$V_{TR\_3P2\_F}$	LVD 3.2 V trimmed falling trip point for V_{DDD}	Typ – 4%	3200	Typ + 4%	mV	
SID525	$V_{TR\_3P3\_F}$	LVD 3.3 V trimmed falling trip point for V_{DDD}	Typ – 4%	3300	Typ + 4%	mV	
SID526	$V_{TR\_3P4\_F}$	LVD 3.4 V trimmed falling trip point for V_{DDD}	Typ – 4%	3400	Typ + 4%	mV	
SID527	$V_{TR\_3P5\_F}$	LVD 3.5 V trimmed falling trip point for V_{DDD}	Typ – 4%	3500	Typ + 4%	mV	
SID528	$V_{TR\_3P6\_F}$	LVD 3.6 V trimmed falling trip point for V_{DDD}	Typ – 4%	3600	Typ + 4%	mV	
SID529	$V_{TR\_3P7\_F}$	LVD 3.7 V trimmed falling trip point for V_{DDD}	Typ – 4%	3700	Typ + 4%	mV	
SID530	$V_{TR\_3P8\_F}$	LVD 3.8 V trimmed falling trip point for V_{DDD}	Typ – 4%	3800	Typ + 4%	mV	
SID531	$V_{TR\_3P9\_F}$	LVD 3.9 V trimmed falling trip point for V_{DDD}	Typ – 4%	3900	Typ + 4%	mV	
SID532	$V_{TR\_4P0\_F}$	LVD 4.0 V trimmed falling trip point for V_{DDD}	Typ – 4%	4000	Typ + 4%	mV	
SID533	$V_{TR\_4P1\_F}$	LVD 4.1 V trimmed falling trip point for V_{DDD}	Typ – 4%	4100	Typ + 4%	mV	
SID534	$V_{TR\_4P2\_F}$	LVD 4.2 V trimmed falling trip point for V_{DDD}	Typ – 4%	4200	Typ + 4%	mV	
SID535	$V_{TR\_4P3\_F}$	LVD 4.3 V trimmed falling trip point for V_{DDD}	Typ – 4%	4300	Typ + 4%	mV	
SID536	$V_{TR\_4P4\_F}$	LVD 4.4 V trimmed falling trip point for V_{DDD}	Typ – 4%	4400	Typ + 4%	mV	
SID537	$V_{TR\_4P5\_F}$	LVD 4.5 V trimmed falling trip point for V_{DDD}	Typ – 4%	4500	Typ + 4%	mV	
SID538	$V_{TR\_4P6\_F}$	LVD 4.6 V trimmed falling trip point for V_{DDD}	Typ – 4%	4600	Typ + 4%	mV	
SID539	$V_{TR\_4P7\_F}$	LVD 4.7 V trimmed falling trip point for V_{DDD}	Typ – 4%	4700	Typ + 4%	mV	
SID540	$V_{TR\_4P8\_F}$	LVD 4.8 V trimmed falling trip point for V_{DDD}	Typ – 4%	4800	Typ + 4%	mV	
SID541	$V_{TR\_4P9\_F}$	LVD 4.9 V trimmed falling trip point for V_{DDD}	Typ – 4%	4900	Typ + 4%	mV	
SID542	$V_{TR\_5P0\_F}$	LVD 5.0 V trimmed falling trip point for V_{DDD}	Typ – 4%	5000	Typ + 4%	mV	
SID543	$V_{TR\_5P1\_F}$	LVD 5.1 V trimmed falling trip point for V_{DDD}	Typ – 4%	5100	Typ + 4%	mV	
SID544	$V_{TR\_5P2\_F}$	LVD 5.2 V trimmed falling trip point for V_{DDD}	Typ – 4%	5200	Typ + 4%	mV	
SID545	$V_{TR\_5P3\_F}$	LVD 5.3 V trimmed falling trip point for V_{DDD}	Typ – 4%	5300	Typ + 4%	mV	

Table 27-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID546	$V_{TR\_2P8\_R}$	LVD 2.8 V trimmed rising trip point for V_{DDD}	Typ – 4%	2825	Typ + 4%	mV	Same as $V_{TR\_2P8\_F}$ + 25 mV
SID547	$V_{TR\_2P9\_R}$	LVD 2.9 V trimmed rising trip point for V_{DDD}	Typ – 4%	2925	Typ + 4%	mV	Same as $V_{TR\_2P9\_F}$ + 25 mV
SID548	$V_{TR\_3P0\_R}$	LVD 3.0 V trimmed rising trip point for V_{DDD}	Typ – 4%	3025	Typ + 4%	mV	Same as $V_{TR\_3P0\_F}$ + 25 mV
SID549	$V_{TR\_3P1\_R}$	LVD 3.1 V trimmed rising trip point for V_{DDD}	Typ – 4%	3125	Typ + 4%	mV	Same as $V_{TR\_3P1\_F}$ + 25 mV
SID550	$V_{TR\_3P2\_R}$	LVD 3.2 V trimmed rising trip point for V_{DDD}	Typ – 4%	3225	Typ + 4%	mV	Same as $V_{TR\_3P2\_F}$ + 25 mV
SID551	$V_{TR\_3P3\_R}$	LVD 3.3 V trimmed rising trip point for V_{DDD}	Typ – 4%	3325	Typ + 4%	mV	Same as $V_{TR\_3P3\_F}$ + 25 mV
SID552	$V_{TR\_3P4\_R}$	LVD 3.4 V trimmed rising trip point for V_{DDD}	Typ – 4%	3425	Typ + 4%	mV	Same as $V_{TR\_3P4\_F}$ + 25 mV
SID553	$V_{TR\_3P5\_R}$	LVD 3.5 V trimmed rising trip point for V_{DDD}	Typ – 4%	3525	Typ + 4%	mV	Same as $V_{TR\_3P5\_F}$ + 25 mV
SID554	$V_{TR\_3P6\_R}$	LVD 3.6 V trimmed rising trip point for V_{DDD}	Typ – 4%	3625	Typ + 4%	mV	Same as $V_{TR\_3P6\_F}$ + 25 mV
SID555	$V_{TR\_3P7\_R}$	LVD 3.7 V trimmed rising trip point for V_{DDD}	Typ – 4%	3725	Typ + 4%	mV	Same as $V_{TR\_3P7\_F}$ + 25 mV
SID556	$V_{TR\_3P8\_R}$	LVD 3.8 V trimmed rising trip point for V_{DDD}	Typ – 4%	3825	Typ + 4%	mV	Same as $V_{TR\_3P8\_F}$ + 25 mV
SID557	$V_{TR\_3P9\_R}$	LVD 3.9 V trimmed rising trip point for V_{DDD}	Typ – 4%	3925	Typ + 4%	mV	Same as $V_{TR\_3P9\_F}$ + 25 mV
SID558	$V_{TR\_4P0\_R}$	LVD 4.0 V trimmed rising trip point for V_{DDD}	Typ – 4%	4025	Typ + 4%	mV	Same as $V_{TR\_4P0\_F}$ + 25 mV
SID559	$V_{TR\_4P1\_R}$	LVD 4.1 V trimmed rising trip point for V_{DDD}	Typ – 4%	4125	Typ + 4%	mV	Same as $V_{TR\_4P1\_F}$ + 25 mV
SID560	$V_{TR\_4P2\_R}$	LVD 4.2 V trimmed rising trip point for V_{DDD}	Typ – 4%	4225	Typ + 4%	mV	Same as $V_{TR\_4P2\_F}$ + 25 mV
SID561	$V_{TR\_4P3\_R}$	LVD 4.3 V trimmed rising trip point for V_{DDD}	Typ – 4%	4325	Typ + 4%	mV	Same as $V_{TR\_4P3\_F}$ + 25 mV
SID562	$V_{TR\_4P4\_R}$	LVD 4.4 V trimmed rising trip point for V_{DDD}	Typ – 4%	4425	Typ + 4%	mV	Same as $V_{TR\_4P4\_F}$ + 25 mV
SID563	$V_{TR\_4P5\_R}$	LVD 4.5 V trimmed rising trip point for V_{DDD}	Typ – 4%	4525	Typ + 4%	mV	Same as $V_{TR\_4P5\_F}$ + 25 mV
SID564	$V_{TR\_4P6\_R}$	LVD 4.6 V trimmed rising trip point for V_{DDD}	Typ – 4%	4625	Typ + 4%	mV	Same as $V_{TR\_4P6\_F}$ + 25 mV
SID565	$V_{TR\_4P7\_R}$	LVD 4.7 V trimmed rising trip point for V_{DDD}	Typ – 4%	4725	Typ + 4%	mV	Same as $V_{TR\_4P7\_F}$ + 25 mV
SID566	$V_{TR\_4P8\_R}$	LVD 4.8 V trimmed rising trip point for V_{DDD}	Typ – 4%	4825	Typ + 4%	mV	Same as $V_{TR\_4P8\_F}$ + 25 mV
SID567	$V_{TR\_4P9\_R}$	LVD 4.9 V trimmed rising trip point for V_{DDD}	Typ – 4%	4925	Typ + 4%	mV	Same as $V_{TR\_4P9\_F}$ + 25 mV
SID568	$V_{TR\_5P0\_R}$	LVD 5.0 V trimmed rising trip point for V_{DDD}	Typ – 4%	5025	Typ + 4%	mV	Same as $V_{TR\_5P0\_F}$ + 25 mV

Table 27-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID569	$V_{TR\_5P1\_R}$	LVD 5.1 V trimmed rising trip point for V_{DDD}	Typ – 4%	5125	Typ + 4%	mV	Same as $V_{TR\_5P1\_F}$ + 25 mV
SID570	$V_{TR\_5P2\_R}$	LVD 5.2 V trimmed rising trip point for V_{DDD}	Typ – 4%	5225	Typ + 4%	mV	Same as $V_{TR\_5P2\_F}$ + 25 mV
SID571	$V_{TR\_5P3\_R}$	LVD 5.3 V trimmed rising trip point for V_{DDD}	Typ – 4%	5325	Typ + 4%	mV	Same as $V_{TR\_5P3\_F}$ + 25 mV
SID573	LVD_RR_A	Power ramp rate: V_{DDD} (Active)	–	–	100	mV/µs	
SID574	LVD_RR_DS	Power ramp rate: V_{DDD} (DeepSleep)	–	–	10	mV/µs	
SID575	$t_{DLY\_ACT\_LVD}$	Active mode delay between V_{DDD} falling/rising through LVD rising/falling point and an internal LVD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID575A	$t_{DLY\_DS\_LVD}$	DeepSleep mode delay between V_{DDD} falling/rising through LVD rising/falling point and an internal LVD output transitioning through V_{DDD} / 2	–	–	4	µs	Guaranteed by design
SID576	t_{RES_LVD}	Response time of LVD, V_{DDD} supply. LVD guaranteed to generate pulse for V_{DDD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below LVD falling trip point.)	100	–	–	ns	Guaranteed by design
High-voltage OVD (HV OVD) specifications							
SID580	$V_{TR\_5P0\_R}$	HV OVD 5.0-V trimmed rising trip point for V_{DDD} and V_{DDA_ADC}	5.049	5.205	5.361	V	
SID581	$V_{TR\_5P0\_F}$	HV OVD 5.0-V trimmed falling trip point for V_{DDD} and V_{DDA_ADC}	5.025	5.18	5.335	V	
SID582	$V_{TR\_5P5\_R}$	HV OVD 5.5-V trimmed rising trip point for V_{DDD} and V_{DDA_ADC} (default)	5.548	5.72	5.892	V	
SID583	$V_{TR\_5P5\_F}$	HV OVD 5.5-V trimmed falling trip point for V_{DDD} and V_{DDA_ADC} (default)	5.524	5.695	5.866	V	
SID585	HVOVD_RR_A	Power ramp rate: V_{DDD} and V_{DDA_ADC} (Active)	–	–	100	mV/µs	
SID586	HVOVD_RR_DS	Power ramp rate: V_{DDD} and V_{DDA_ADC} (DeepSleep)	–	–	10	mV/µs	

Table 27-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID587	$t_{DLY\_ACT\_HVOVD}$	Active mode delay between V_{DDD} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID587A	$t_{DLY\_ACT\_H-VOVD\_A}$	Active mode delay between V_{DDA_ADC} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD output transitioning through V_{DDD} / 2	–	–	1.5	µs	Guaranteed by design
SID587B	$t_{DLY\_DS\_HVOVD}$	DeepSleep mode delay between V_{DDD}/V_{DDA_ADC} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD output transitioning through V_{DDD} / 2	–	–	4	µs	Guaranteed by design
SID588	t_{RES_HVOVD}	Response time of HV OVD HV OVD guaranteed to generate pulse for V_{DDD}/V_{DDA_ADC} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above $V_{TR\_5P0\_R}$ or $V_{TR\_5P5\_R}$)	100	–	–	ns	Guaranteed by design
Low-voltage OVD (LV OVD) specifications							
SID590	$V_{TR\_R\_LVOVD}$	LV OVD trimmed rising trip point for V_{CCD}	Typ – 3%	1300	Typ + 3%	mV	
SID591	$V_{TR\_F\_LVOVD}$	LV OVD trimmed falling trip point for V_{CCD}	Typ – 3%	1275	Typ + 3%	mV	Same as $V_{TR\_R\_LVOVD}$ – 25 mV
SID595	$t_{DLY\_ACT\_LVOVD}$	Active mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID595A	$t_{DLY\_DS\_LVOVD}$	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD output transitioning through V_{DDD} / 2	–	–	12	µs	Guaranteed by design
SID596	t_{RES_LVOVD}	Response time of LV OVD. LV OVD guaranteed to generate pulse for V_{CCD} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above $V_{TR\_R\_LVOVD}$)	100	–	–	ns	Guaranteed by design
Over current detection (OCD) specifications							

Table 27-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID598_A	I_{OCD}	Over current detection range for internal Active regulator	156	–	315	mA	
SID599	I_{OCD_DPSLP}	Over current detection range for internal DeepSleep regulator	18	–	72	mA	

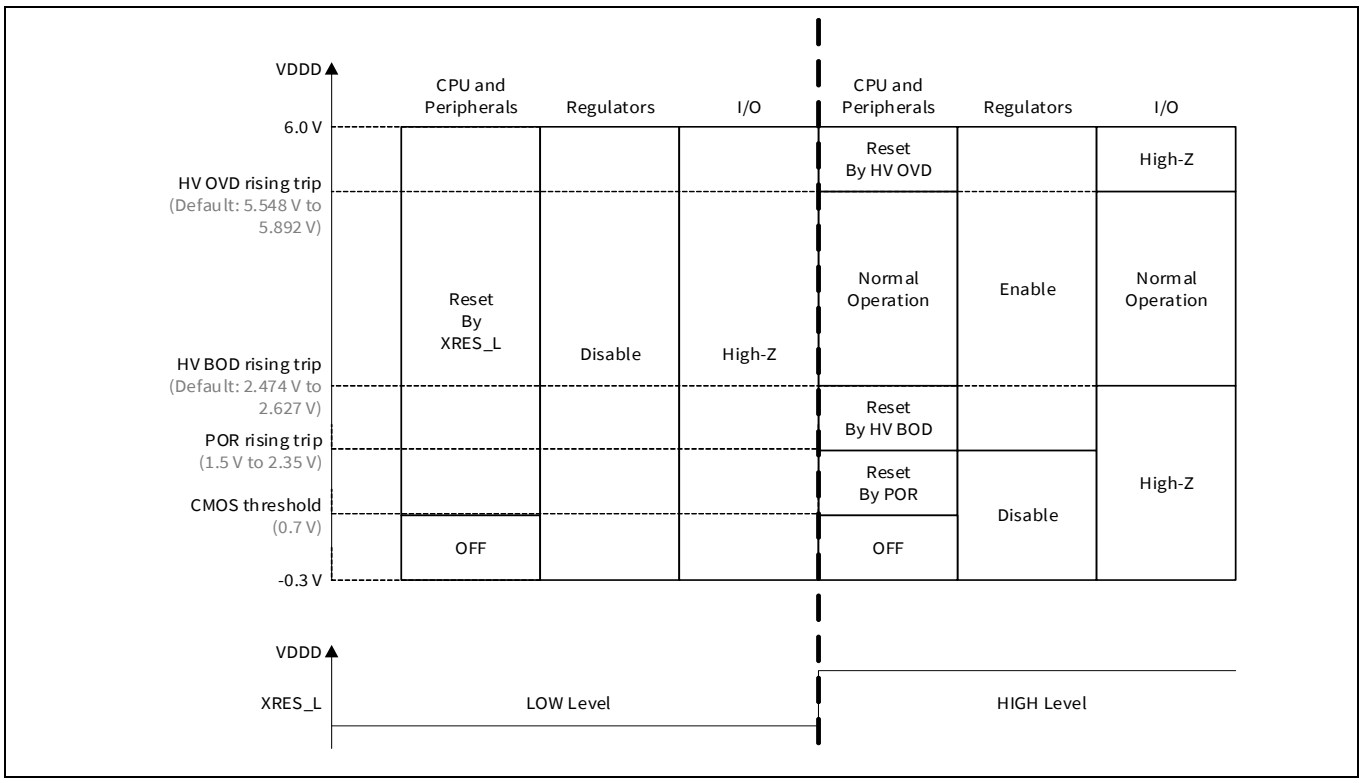


Figure 27-14 Device operations supply range

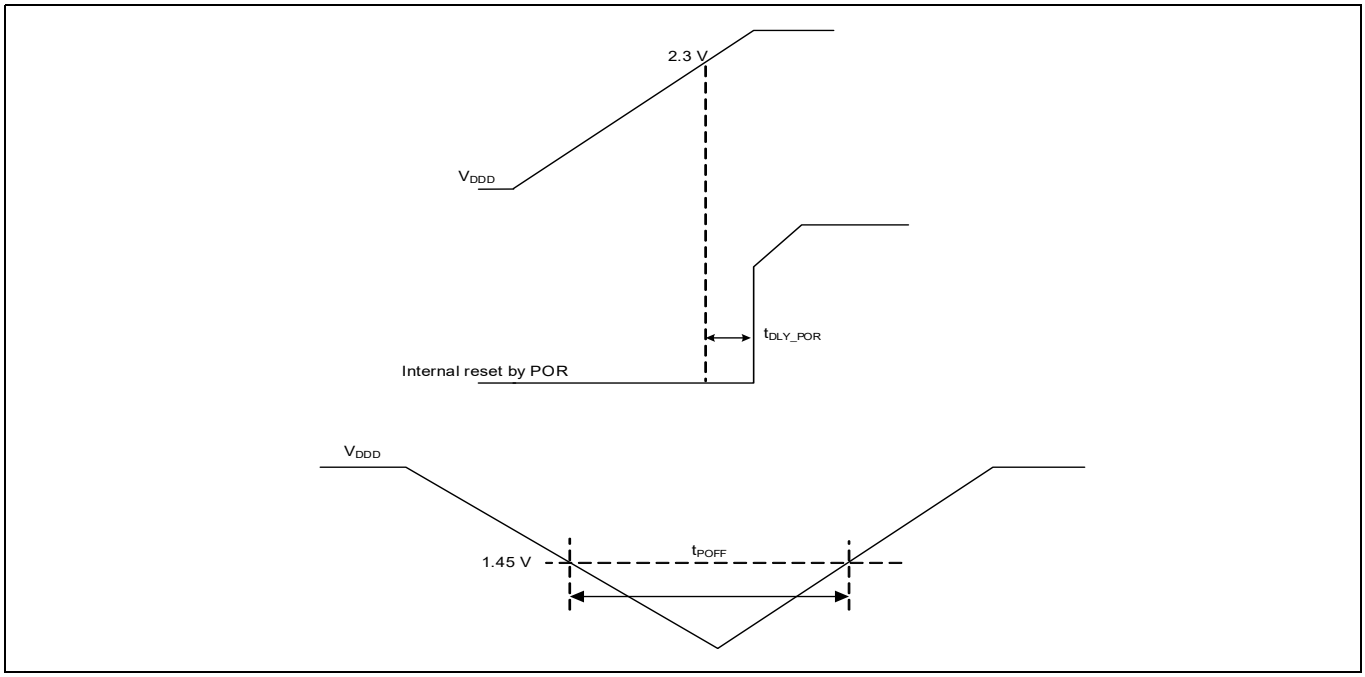


Figure 27-15 POR specifications

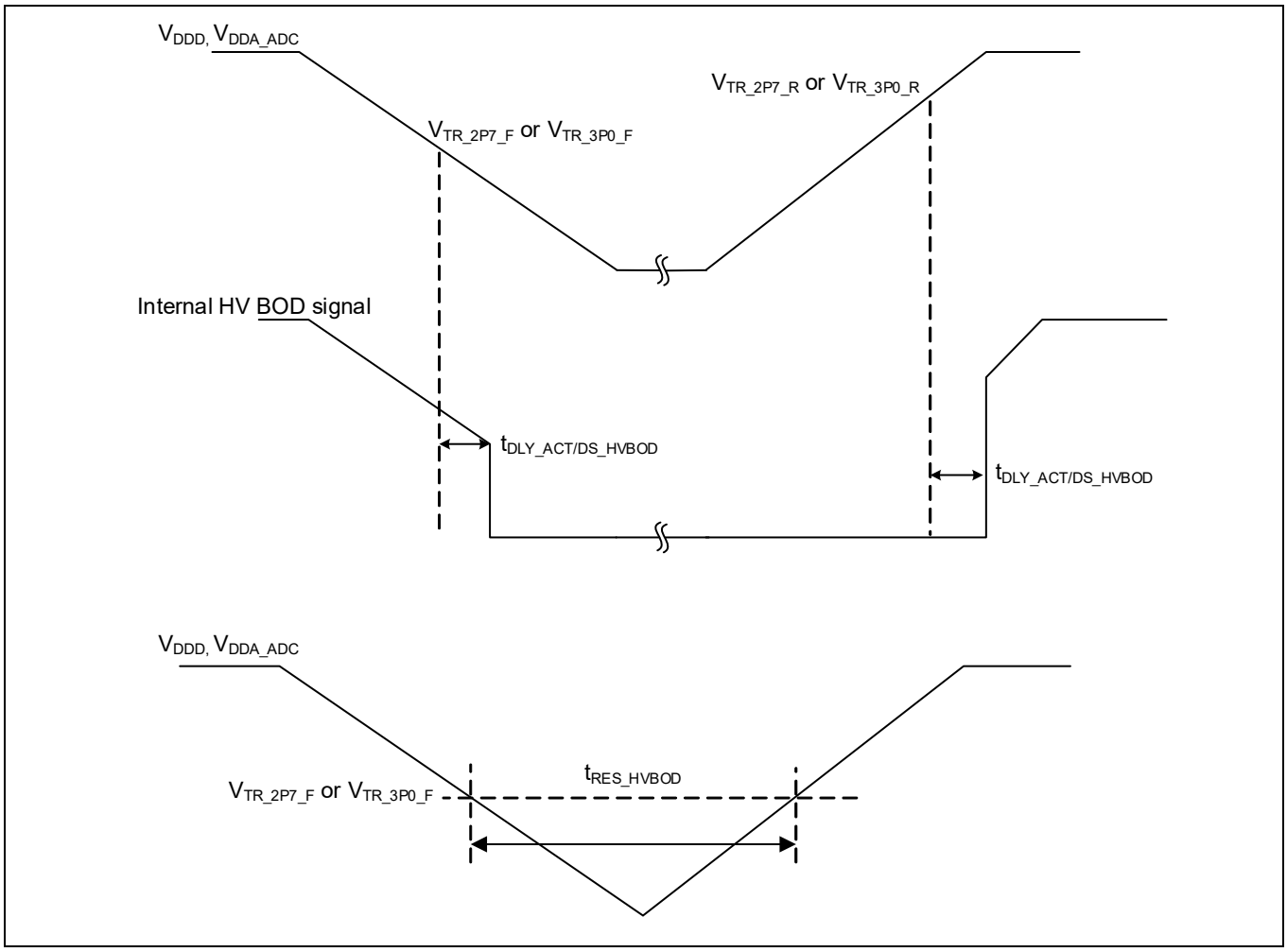


Figure 27-16 High-voltage BOD specifications

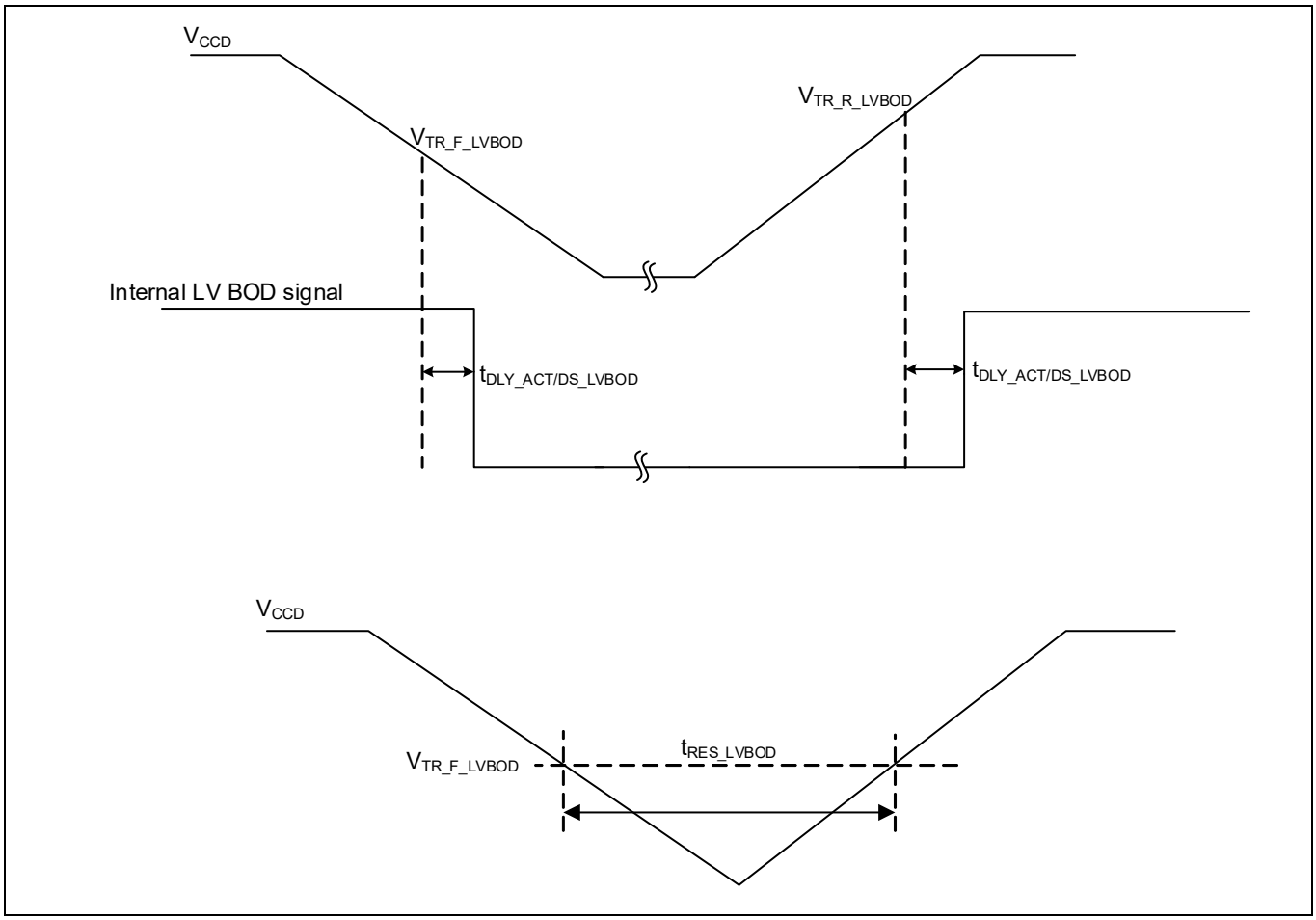


Figure 27-17 Low-voltage BOD specifications

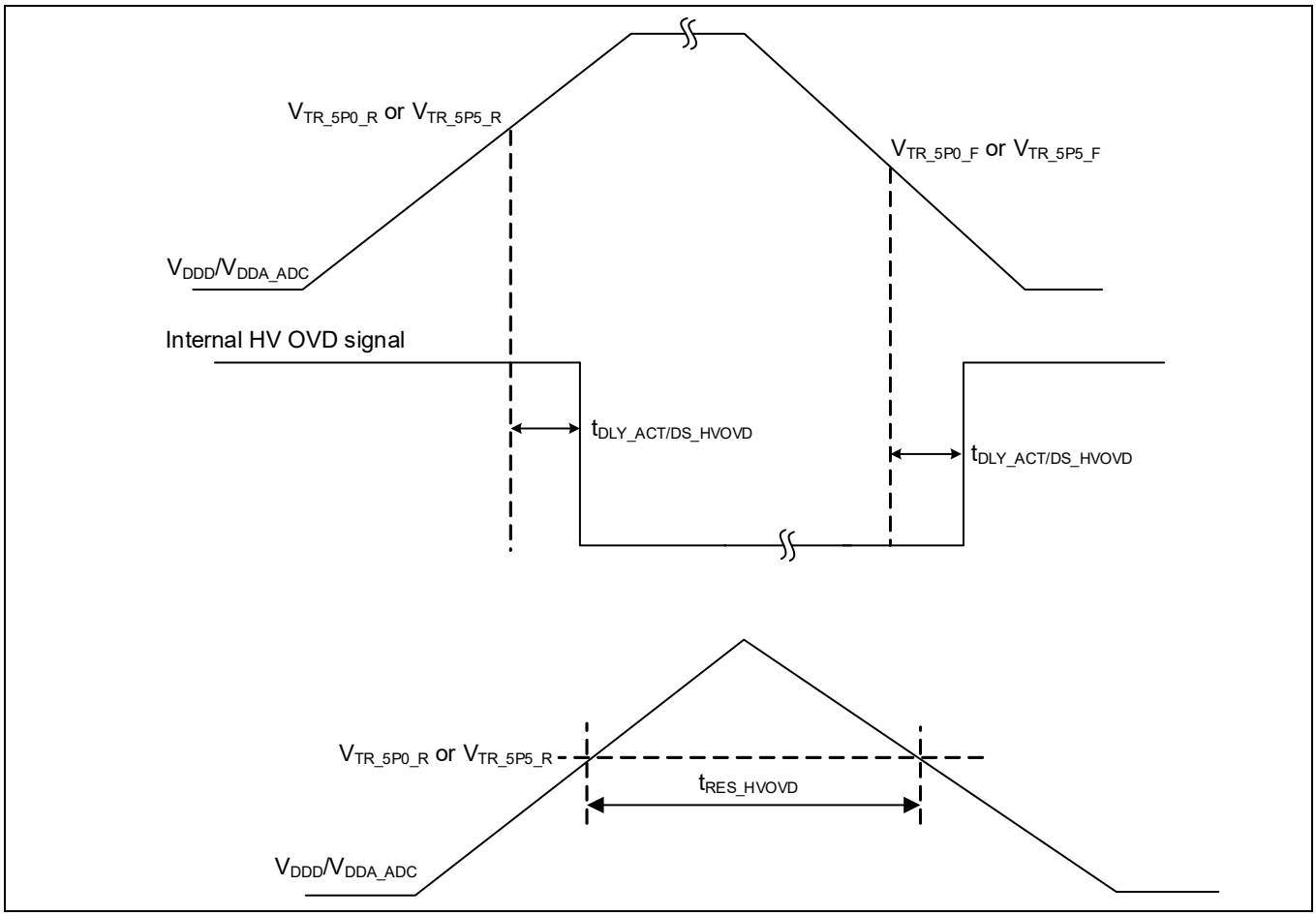


Figure 27-18 High-voltage OVD specifications

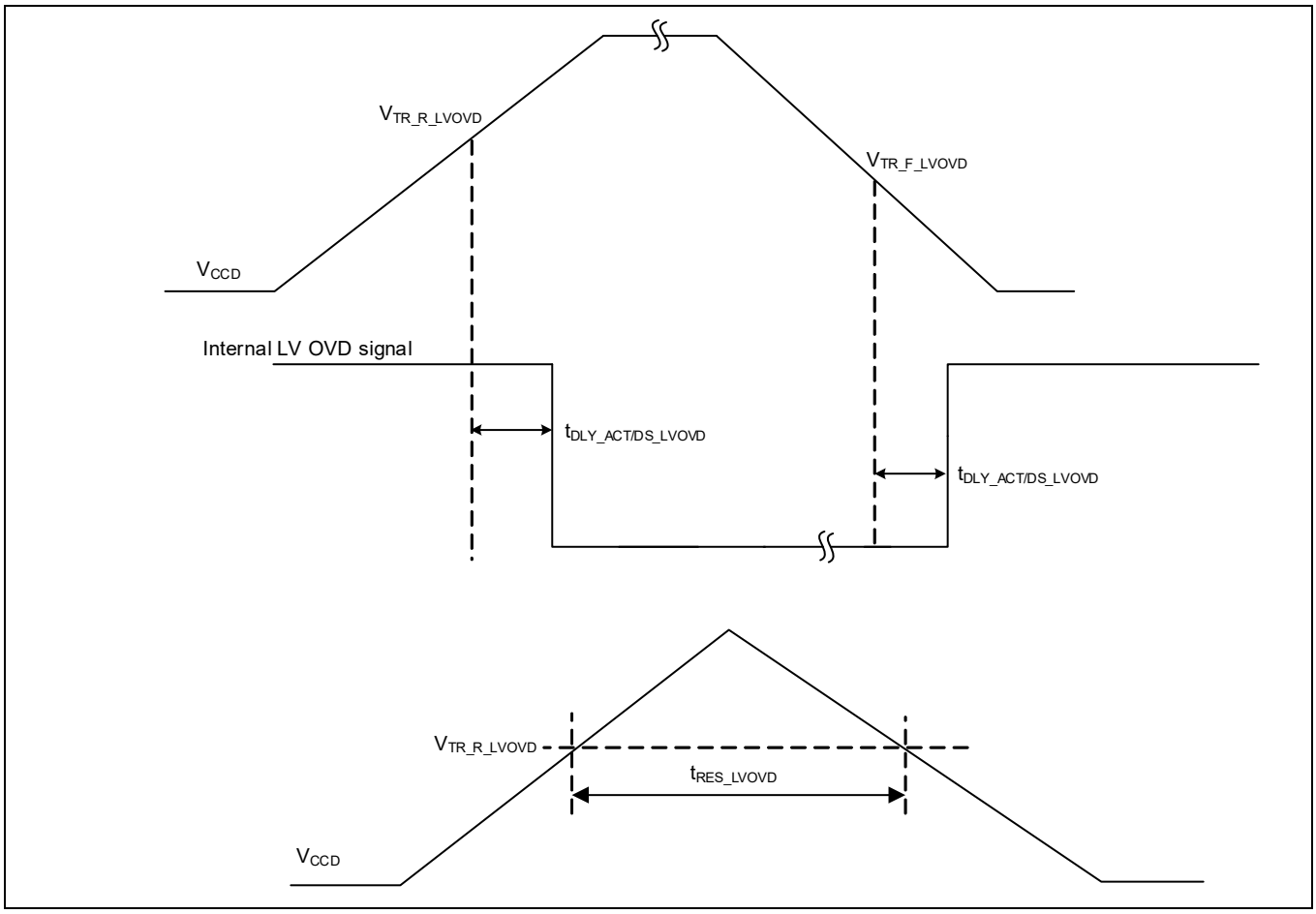


Figure 27-19 Low-voltage OVD specifications

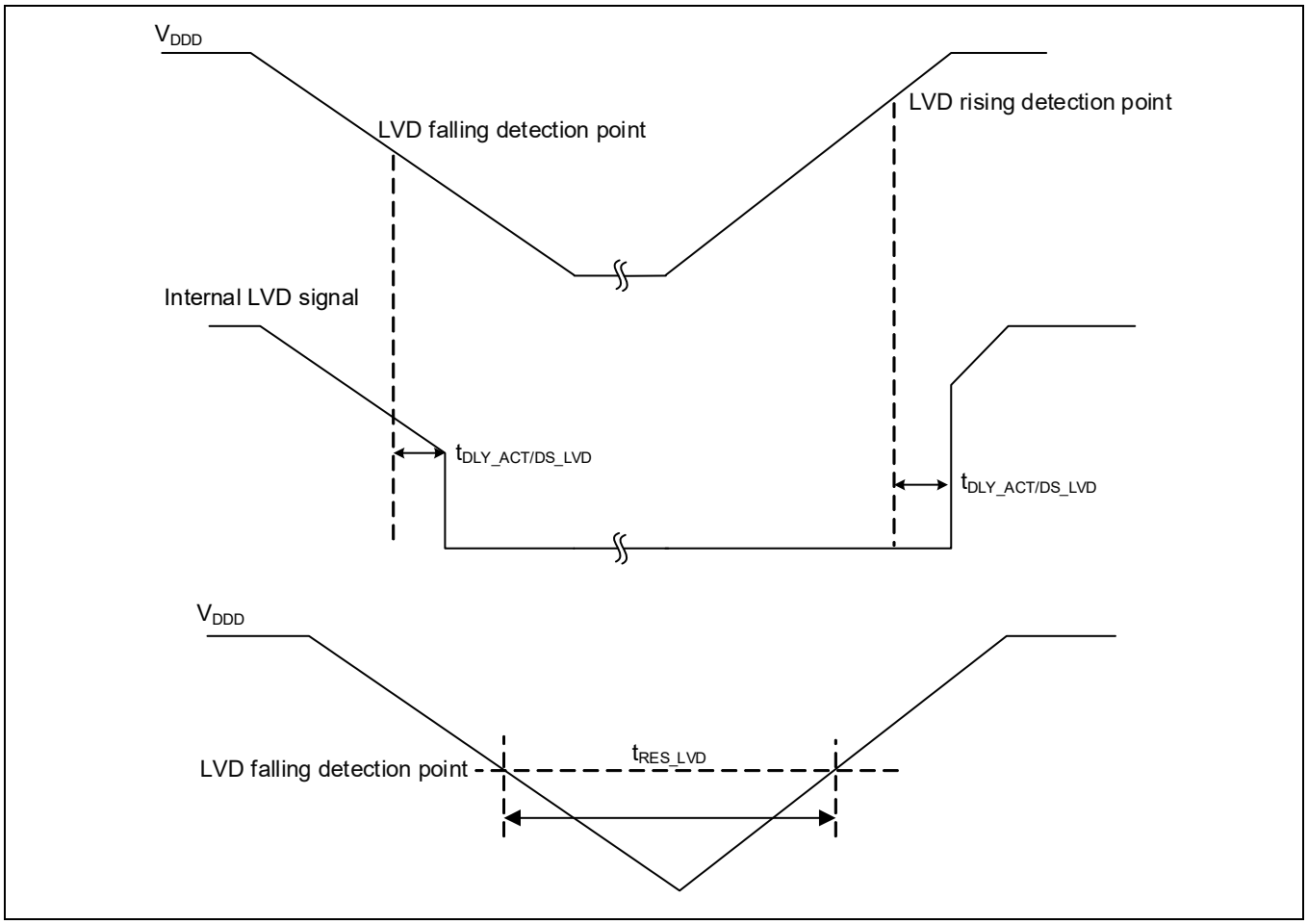


Figure 27-20 LVD specifications

Table 27-16 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> =0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID300	f_{SWDCLK}	SWD clock input frequency	–	–	10	MHz	2.7 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID301	t_{SWDI_SETUP}	SWDI setup time	0.25 × T	–	–	ns	T = 1 / f_{SWDCLK}
SID302	t_{SWDI_HOLD}	SWDI hold time	0.25 × T	–	–	ns	T = 1 / f_{SWDCLK}
SID303	t_{SWDO_VALID}	SWDO valid time	–	–	0.5 × T	ns	T = 1 / f_{SWDCLK}
SID304	t_{SWDO_HOLD}	SWDO hold time	1	–	–	ns	T = 1 / f_{SWDCLK}

Table 27-17 JTAG AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID620	t_{JCKH}	TCK HIGH time	25	–	–	ns	30-pF load on TDO
SID621	t_{JCKL}	TCK LOW time	25	–	–	ns	30-pF load on TDO
SID622	t_{JCP}	TCK clock period	62.5	–	–	ns	30-pF load on TDO
SID623	t_{JSU}	TDI/TMS setup time	6.25	–	–	ns	30-pF load on TDO
SID624	t_{JH}	TDI/TMS hold time	6.25	–	–	ns	30-pF load on TDO
SID625	t_{JZX}	TDO High-Z to active	–	–	25	ns	30-pF load on TDO
SID626	t_{JXZ}	TDO active to High-Z	–	–	25	ns	30-pF load on TDO
SID627	t_{JCO}	TDO clock to output	–	–	25	ns	30-pF load on TDO

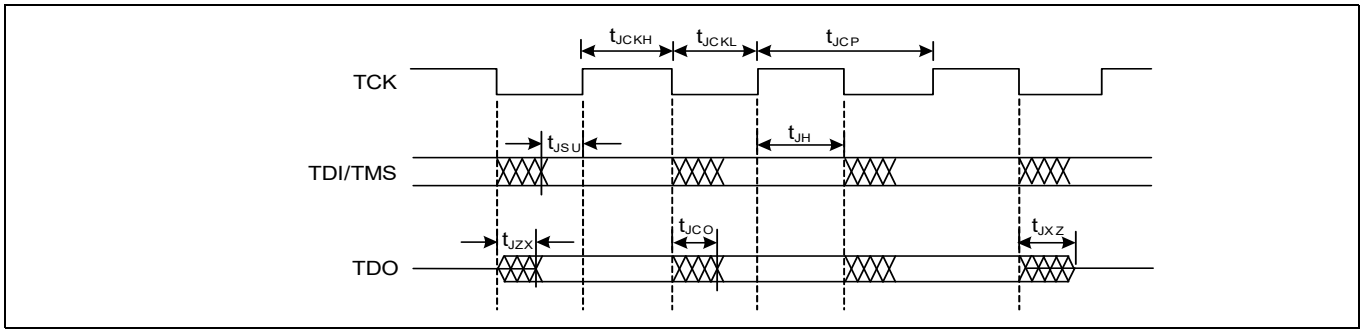


Figure 27-21 JTAG specifications

Table 27-18 Trace specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended I/O Configuration: **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b000, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID1412A	C_{TRACE}	Trace Capacitive Load	–	–	30	pF	
SID1412	t_{TRACE_CYC}	Trace clock period	20	–	–	ns	Trace clock cycle time for 50 MHz
SID1413	t_{TRACE_CLKL}	Trace clock LOW pulse width	2	–	–	ns	Clock low pulse width
SID1414	t_{TRACE_CLKH}	Trace clock HIGH pulse width	2	–	–	ns	Clock high pulse width

Table 27-18 Trace specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1415	t_{TRACE_SETUP}	Trace data setup time	2	–	–	ns	Trace data setup time, CLK_PERI ≥ 75 MHz
SID1416	t_{TRACE_HOLD}	Trace data hold time	1	–	–	ns	Trace data hold time, CLK_PERI ≥ 75 MHz
SID1415A	t_{TRACE_SETUP}	Trace data setup time	3	–	–	ns	Trace data setup time, CLK_PERI < 75 MHz
SID1416A	t_{TRACE_HOLD}	Trace data hold time	2	–	–	ns	Trace data hold time, CLK_PERI < 75 MHz

27.11 Clock specifications

The basic requirement on the clock frequency dependency of the cores is that the Cortex®-M0+ core should run at an integer divider from the Cortex®-M4F core clock. Example combinations are listed in the **Table 27-19**.

Table 27-19 Clock requirements

Core Cortex®-M4F Clock (MHz)	Core Cortex®-CM0+ Clock (MHz)
160	80
100	100
80	80

Table 27-20 Root and intermediate clocks[56, 57]

Root Clock	Maximum permitted clock frequency (MHz)[58]	Source	Maximum permitted clock frequency (MHz)[58]						Description
			PLL/FLL Clock source: ECO/LPECO[59]			PLL/FLL Clock source: IMO[60, 61]			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF0	160	PLL200#1	160	NA	NA	153	NA	NA	Root clock for CPUSS (CM0+, CM4), PERI (CLK_SLOW, CLK_PERI)
		FLL	100	NA	NA	100	NA	NA	
	100	PLL200#1	100	NA	NA	95	NA	NA	
		FLL	100	NA	NA	97	NA	NA	
CLK_HF1	100	PLL200#1	100	NA	NA	95	NA	NA	Event generator (CLK_REF), clock output on EXT_CLK pins (when used as output)
		FLL	100	NA	NA	97	NA	NA	
CLK_HF2	200	PLL400#0 / PLL200#2 / EXT_CLK	200	196	198	191	189	191	Sound Subsystem #0 root clock, (CLK_IF_SRSS0)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF3	200	PLL400#0 / PLL200#2 / EXT_CLK	200	196	198	191	189	191	Sound Subsystem #1 root clock (CLK_IF_SRSS1)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF4	200	PLL400#0 / PLL200#2 / EXT_CLK	200	196	198	191	189	191	Sound Subsystem #2 root clock (CLK_IF_SRSS2)
		FLL	100	NA	NA	100	NA	NA	

Notes
56. Intermediate clocks that are not listed have the same limitations as that of their parent clock.
57. Table indicates guaranteed mapping between a root clock (CLK_HFx) and the PLL.
58. Maximum clock frequency after the corresponding clock source (PLL/FLL + dividers). All internal tolerances and affects are covered by these frequencies.
59. For ECO, LPECO: up to ±150 ppm uncertainty of the external clock source are tolerated by design.
60. The IMO operation frequency tolerance is included.
61. ROM and flash boot execution with IMO/FLL at 100 MHz is guaranteed by design.

Table 27-20 Root and intermediate clocks[56, 57] *(continued)*

Root Clock	Maximum permitted clock frequency (MHz)[58]	Source	Maximum permitted clock frequency (MHz)[58]						Description
			PLL/FLL Clock source: ECO/LPECO[59]			PLL/FLL Clock source: IMO[60, 61]			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF5	200	PLL200#2	200	NA	NA	191	NA	NA	SMIF#0 root clock
		FLL	100	NA	NA	100	NA	NA	
CLK_HF6	ILO		NA						CSV Dedicated (< 1MHz)
CLK_FAST	160	CLK_HF0	160	NA	NA	153	NA	NA	Generated by dividing CLK_HF0, intermediate clock for CM4
		FLL	100	NA	NA	100	NA	NA	
CLK_SLOW	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_PERI, intermediate clock for CM0+, Crypto, P-DMA, M-DMA
		FLL	100	NA	NA	97	NA	NA	
CLK_PERI	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_HF0, intermediate clock for LIN, SCB, PASS, CAN, TCPWM,CXPI, IOSS, CPU trace
		FLL	100	NA	NA	97	NA	NA	

Table 27-21 PLL400 operation modes

PLL400 operation mode	Spread spectrum clock generation (SSCG)	Fractional
Integer	OFF	OFF
SSCG	ON	OFF
Fractional	OFF	ON

Table 27-22 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID310	f_{IMO}	IMO operating frequency	7.632	8	8.368	MHz	Accuracy after factory trimming
SID311	$t_{STARTIMO}$	IMO startup time	–	–	7.5	µs	Startup time to 90% of final frequency
SID312	I_{IMO_ACT}	IMO current	–	13.5	22	µA	Guaranteed by design

Table 27-23 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID320	$f_{ILOTRIM}$	ILO operating frequency	30.965	32.768	34.57	kHz	5.5% accuracy after factory trimming
SID321	$t_{STARTILO}$	ILO startup time	–	8	12	µs	Startup time to 90% of final frequency
SID323	I_{ILO}	ILO current	–	500	2800	nA	Guaranteed by design

Table 27-24 LPECO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID325	f_{LPECO}	LPECO operating frequency	3.99	–	8.01	MHz	Drive level protection DL ≥ 100 µW, ESR ≤ 200 Ω Crystal load capacitance (C_L) 5 pF to 25 pF
SID329	I_{LPECO_4M}	LPECO current at 4 MHz	–	93	110	µA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID354	I_{LPECO_4M}	LPECO current at 4 MHz	–	97	125	µA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID326	I_{LPECO_4M}	LPECO current at 4 MHz	–	106	145	µA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID355	I_{LPECO_4M}	LPECO current at 4 MHz	–	115	155	µA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID356	I_{LPECO_8M}	LPECO current at 8 MHz	–	140	165	µA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID357	I_{LPECO_8M}	LPECO current at 8 MHz	–	149	175	µA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID327	I_{LPECO_8M}	LPECO current at 8 MHz	–	165	190	µA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID358	I_{LPECO_8M}	LPECO current at 8 MHz	–	183	220	µA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0

Table 27-24 LPECO specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID328	t_{START_LPECO}	LPECO startup time[62]	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (BACKUP_LPECO_CTL.LPECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_LPECO_STATUS.LPECO_READY<0:0>=0b1 and BACKUP_LPECO_STATUS.LPECO_AMPDET_OK<0:0>=0b1).

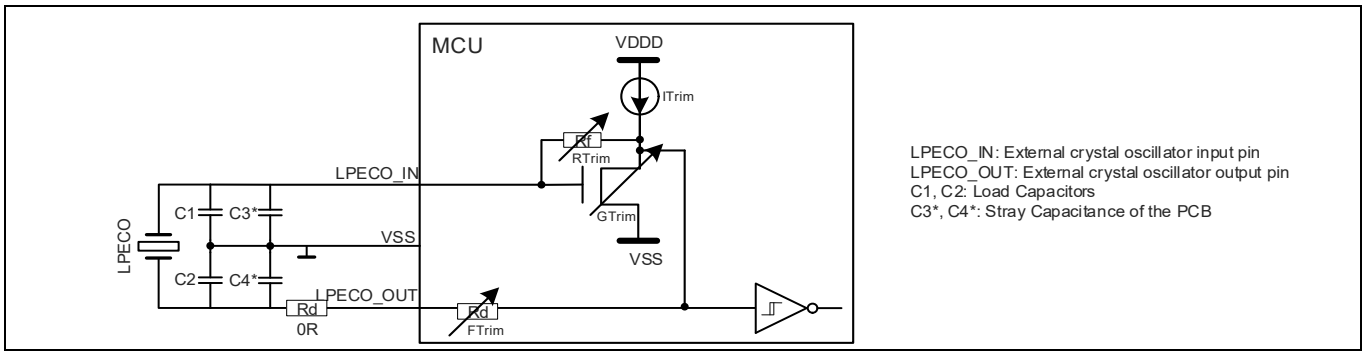


Figure 27-22 LPECO connection scheme[63]

Notes
62. Oscillator startup time is a performance parameter and mainly depending on the chosen external crystal and load capacitance.
63. See the family-specific Architecture TRM for more information on crystal requirements (002-19314, TRAVEO™ T2G Automotive Body Controller Entry Family Architecture Technical Reference Manual (TRM)).

Table 27-25 ECO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID330	f_{ECO}	Crystal frequency range	7.2	–	33.34	MHz	
SID332	R_{FDBK}	Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100 kΩ step size on RTRIM	100	–	400	kΩ	Guaranteed by design
SID333	I_{ECO3}	ECO current at T_J = 150 °C	–	1200	2000	µA	Maximum operation current at 33 MHz crystal, up to 18 pF load
SID334	t_{START_7M}	7.2 MHz ECO startup time[64]	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_-CONFIG.ECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.ECO_OK<0:0>=0b1 and CLK_ECO_STATUS.ECO_READY<0:0>=0b1).
SID335	t_{START_33M}	33 MHz ECO startup time[64]	–	–	1	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_-CONFIG.ECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.ECO_OK<0:0>=0b1 and CLK_ECO_STATUS.ECO_READY<0:0>=0b1).

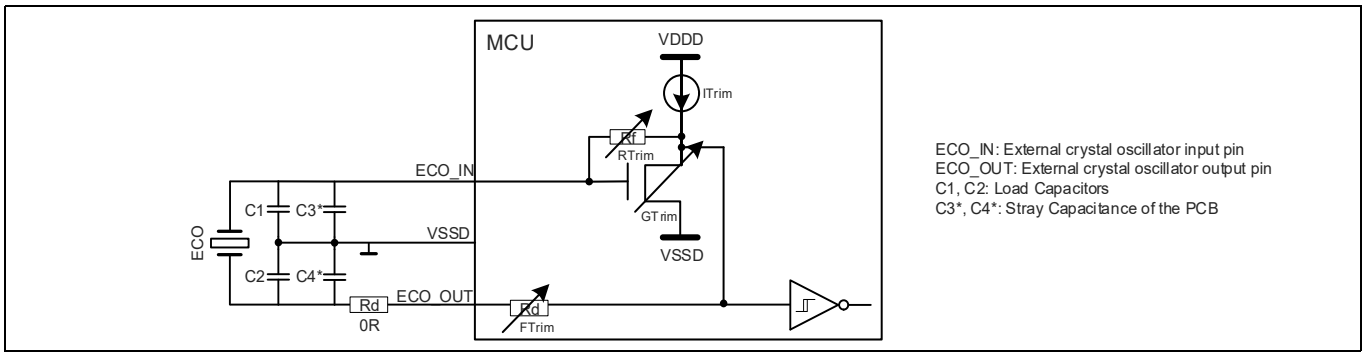


Figure 27-23 ECO connection scheme[65]

Notes
64. Oscillator startup time is a performance parameter and mainly depending on the chosen external crystal and load capacitance.
65. See the family-specific Architecture TRM for more information on crystal requirements (002-33175, TRAVEO™ T2G Automotive MCU cluster entry architecture technical reference manual).

Table 27-26 PLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
PLL Specifications for "PLL without SSCG and Fractional Operation" (PLL200)							
SID340	t_{PLL200_LOCK}	Time to achieve PLL lock	–	–	35	µs	Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set
SID341	f_{OUT}	Output frequency from PLL block (PLL_OUT)	10.998	–	200.03	MHz	
SID346	f_{IN}	PLL input frequency (Reference Clock f_{REF})	3.988	–	33.34	MHz	
SID347	I_{PLL_200M}	PLL operating current	–	0.87	1.85	mA	f_{OUT} = 200 MHz
SID348C	f_{PLL_VCO}	VCO frequency, clock output of 'Voltage Control Oscillator (VCO)'	169.9745	–	400.06	MHz	
SID349C	f_{PLL_PFD}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	8.0012	MHz	
SID342	PLL_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID343	PLL_LJIT2	Long term jitter	–0.5	–	0.5	ns	For 500 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID344	PLL_LJIT3	Long term jitter	–0.5	–	0.5	ns	For 1000 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID345A1	PLL_LJIT5	Long term jitter	–0.75	–	0.75	ns	For 10000 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
PLL Specifications for "PLL with SSCG and Fractional Operation" (PLL400)							
SID340A	t_{PLL400_LOCK}	Time to achieve PLL lock	–	–	50	µs	
SID341A	f_{OUT}	Output frequency from PLL block (PLL_OUT)	24.996	–	400.06	MHz	
SID343A	SPREAD_D	Spread spectrum modulation depth	0.5	–	3	%	Downspread only, triangle modulation
SID343B	f_{SPREAD_MR}	Spread spectrum modulation rate	–	–	32	kHz	Selected by modulation divider from f_{PFD}
SID346A	f_{IN}	PLL input frequency (Reference Clock f_{REF})	3.988	–	33.34	MHz	
SID347A	I_{PLL_400M}	PLL operating current	–	1.4	2.2	mA	f_{OUT} = 400 MHz

Table 27-26 PLL specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID348A	f_{PFD_S}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	20.003	MHz	Fractional operation OFF
SID349A	f_{PFD_F}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	7.9988	–	20.003	MHz	Fractional operation ON
SID345A	f_{VCO}	VCO frequency, Clock output of 'Voltage Control Oscillator (VCO)'	399.94	–	800.12	MHz	
SID342D1	PLL400_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz
SID343D1	PLL400_LJIT2	Long term jitter	–0.5	–	0.5	ns	For 500 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz
SID344D1	PLL400_LJIT3	Long term jitter	–1	–	1	ns	For 1000 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz
SID345E1	PLL400_LJIT5	Long term jitter	–1.5	–	1.5	ns	For 10000 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz

Table 27-27 FLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID350	t_{FLL_WAKE}	FLL wake up time	–	–	5	µs	Wakeup with < 10°C temperature change while in DeepSleep. f_{FLL_IN} = 8 MHz, f_{FLL_OUT} = 100 MHz, Time from stable reference clock until FLL frequency is within 5% of final value
SID351	f_{FLL_OUT}	Output frequency from FLL block	24	–	100	MHz	Output range of FLL divided-by-2 output
SID352	FLL_CJIT	FLL frequency accuracy	–1	–	1	%	This is added to the error of the source
SID353	f_{FLL_IN}	Input frequency	0.25	–	100	MHz	

Table 27-28 WCO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID360	f_{WCO}	Watch crystal frequency	–	32.768	–	kHz	Tuning Fork Crystal with following parameters: DL (drive level) ≥ 0.5 µW, ESR ≤ 130 kΩ
SID361	WCO_DC	WCO duty cycle	10	–	90	%	
SID362	t_{START_WCO}	WCO start up time[66]	–	–	1000	ms	Time from oscillator enable (BACKUP_CTL.WCO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_STATUS.WCO_OK<0:0>=0b1)
SID363	I_{WCO}	WCO current	–	1.4	–	µA	AGC = OFF

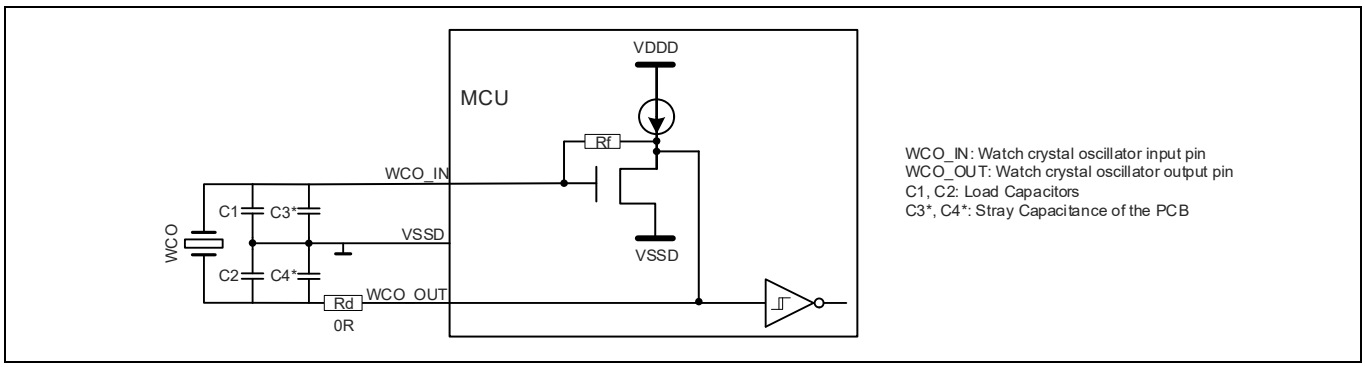


Figure 27-24 WCO connection scheme[67]

Table 27-29 External clock input specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID366	f_{EXT}	External clock input frequency	0.25	–	100	MHz	For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive)
SID367	EXT_DC	Duty cycle	45	–	55	%	

Notes
66. Oscillator startup time is a performance parameter and mainly depending on the chosen external crystal and load capacitance.
67. See the family-specific Architecture TRM for more information on crystal requirements (002-33175, TRAVEO™ T2G Automotive MCU cluster entry architecture technical reference manual).

27.12 Clock timing diagrams

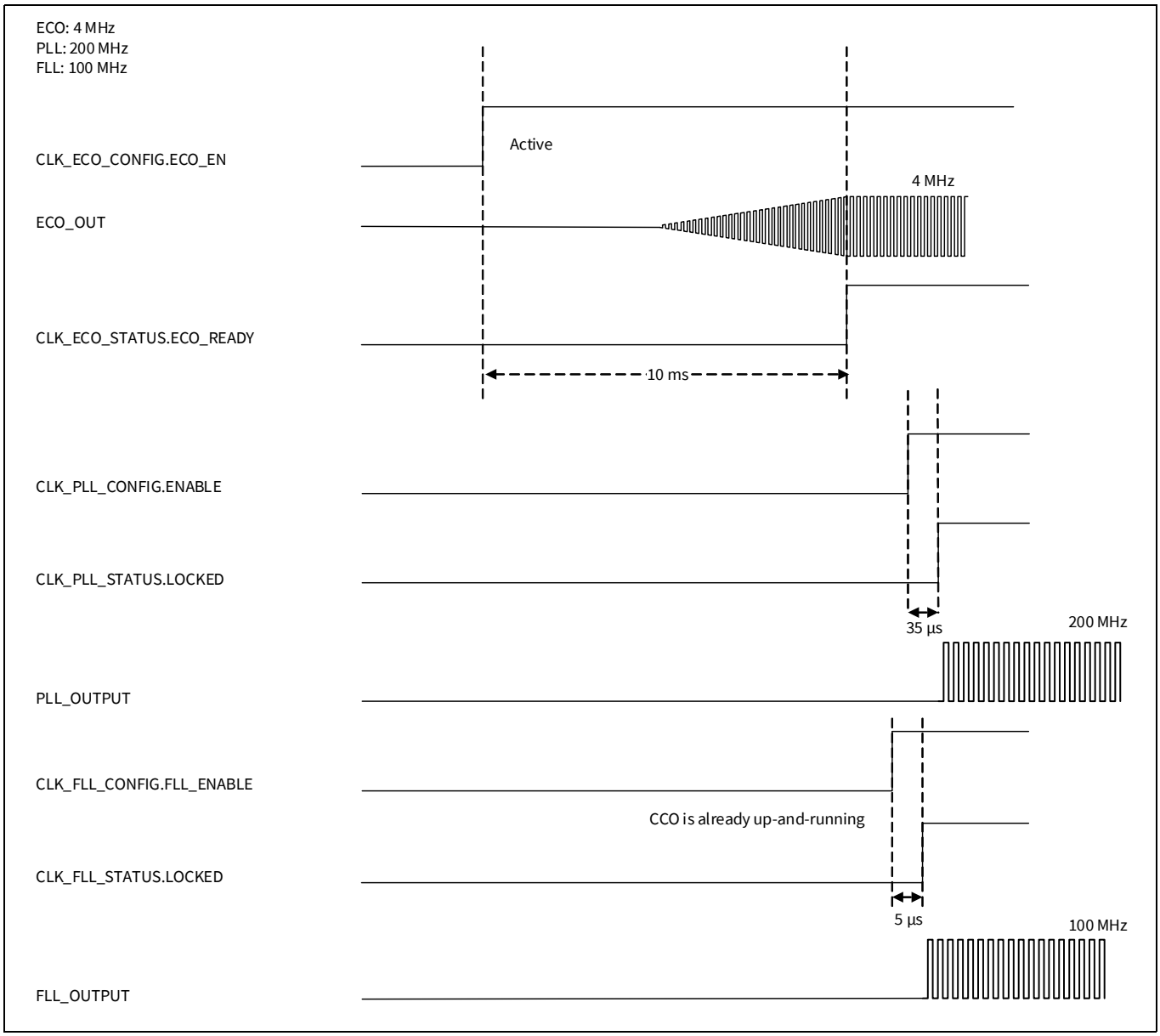


Figure 27-25 ECO to PLL or FLL diagram

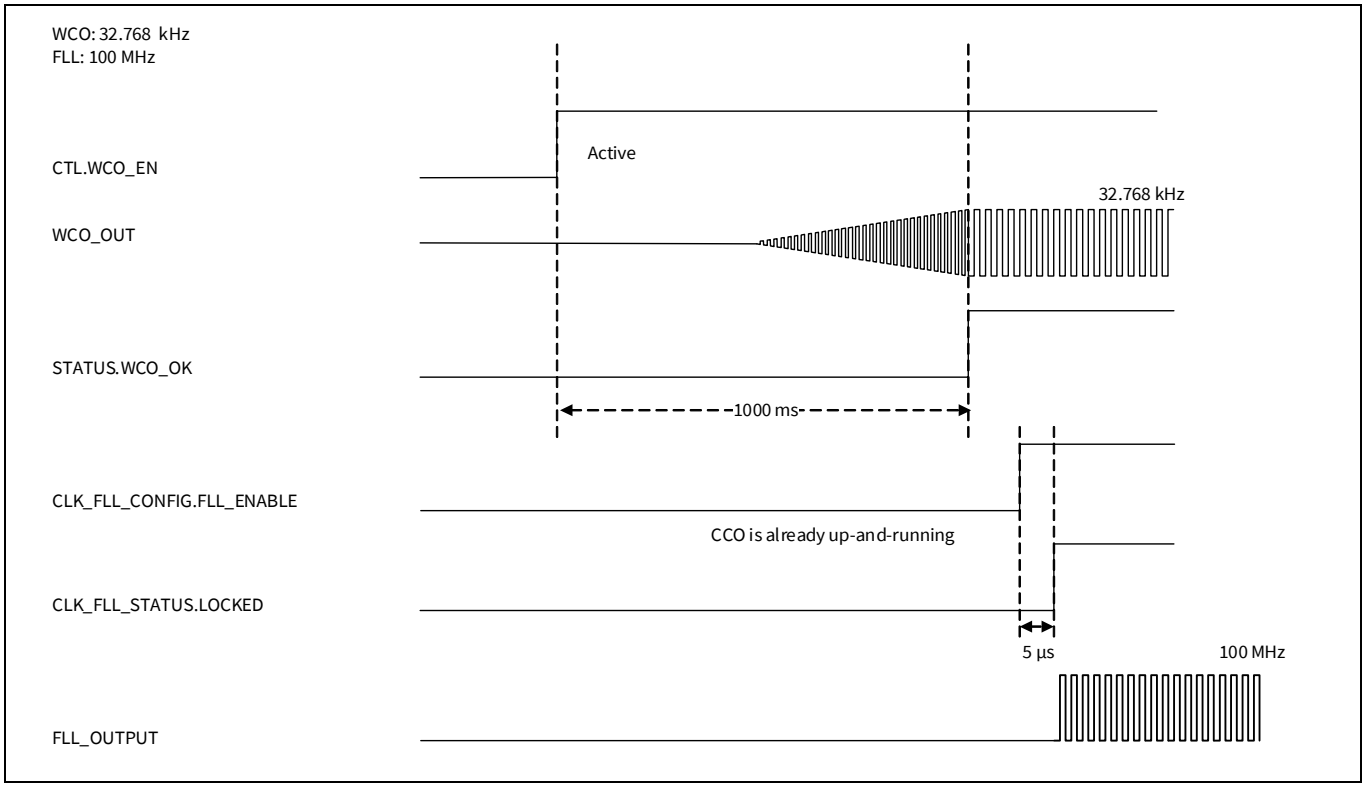


Figure 27-26 WCO to FLL diagram

Table 27-30 MCWDT timeout specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID410	t_{MCWDT1}	Minimum MCWDT timeout	57.85	–	–	µs	When using the ILO (32 kHz + 5.5%) and 16-bit MCWDT counter Guaranteed by design
SID411	t_{MCWDT2}	Maximum MCWDT timeout	–	–	2.12	s	When using the ILO (32 kHz – 5.5%) and 16-bit MCWDT counter Guaranteed by design

Table 27-31 WDT timeout specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID412	t_{WDT1}	Minimum WDT timeout	57.85	–	–	µs	When using the ILO (32 kHz + 5.5%) and 32-bit WDT counter Guaranteed by design
SID413	t_{WDT2}	Maximum WDT timeout	–	–	38.53	h	When using the ILO (32 kHz – 5.5%) and 32-bit WDT counter Guaranteed by design
SID414	t_{WDT3}	Default WDT timeout	–	1000	–	ms	When using the ILO and 32-bit WDT counter at 0x8000 (default value), guaranteed by design

27.13 Sound subsystem specifications

Table 27-32 Sound subsystem specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
I²S I/O Settings							
Recommended I/O configuration: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> =0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
I²S Serial Clock Frequency							
SID796	t_{SCLK}	Serial clock period	162	–	–	ns	Guaranteed by design No feature is used for low frequency I²S operation: DUT RX Master: * RX_IF_CTL.LATE_SAMPLE = 0 * RX_IF_CTL.LATE_CAPTURE = 0b00 DUT TX Slave: No special configuration DUT RX Slave: * RX_IF_CTL.LATE_SAMPLE = 0 I²S can only be used at 2.7 V ≤ V_{DDD} ≤ 3.6 V
SID797	t_{HC}	Serial clock high time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID798	t_{LC}	Serial clock low time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID799	t_{MCLK}	Master clock period	20	–	–	ns	Guaranteed by design I²S can only be used at 2.7 V ≤ V_{DDD} ≤ 3.6 V
I²S Transmitter Timing							
SID740	t_{DTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	–	–	0.8 × t_{SCLK}	ns	Guaranteed by design
SID741	t_{HTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID743	$t_{HR\_WS\_POL\_0}$	TX Slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	
I²S Receiver Timing							
SID751	t_{SR}	Setup on RX_SD/RX_FSYNC (WS) before the rising edge to RX_CLK	0.2 × t_{SCLK}	–	–	ns	Guaranteed by Design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE or SCK_POLARITY setting
SID752A	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the rising edge to RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 0
SID753	t_{SCLK_TRANS}	SCLK transition timing	1	–	8	ns	20% to 80%
SID754	t_{MCLK_TRANS}	MCLK transition timing	1	–	8	ns	20% to 80%
SID755	t_{DATA_TRANS}	DATA transition timing	1	–	8	ns	20% to 80%

Table 27-32 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
TDM I/O Settings							
Recommended I/O configuration: **For serial clock up to 25 MHz** **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
TDM Serial Clock							
SID1000B	t_{SCLK}	Serial clock period, TDM[x] (x=0 through 1)	40	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX Slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX Slave: RX_IF_CTL.SCK_POLARITY= 0 TDM can only be used at 2.7 V ≤ V_{DDD} ≤ 3.6 V
SID1000D	t_{SCLK}	Serial clock period, TDM[x] (x=0 through 1)	80	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX Slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX Slave: RX_IF_CTL.SCK_POLARITY = 0 TDM can only be used at 2.7 V ≤ V_{DDD} ≤ 3.6 V
SID1001	t_{HC}	Serial clock high time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID1002	t_{LC}	Serial clock low time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID1010A	t_{MCLK}	Master clock input period	20	–	–	ns	MCLK must be SCLK*2; The maximum output frequency of the TDM depends on the used I/O type.
SID1002B	t_{MCLK}	Master clock output period	40	–	–	ns	
SID1002D	t_{MCLK_IH}	Master clock input HIGH time	0.45 × t_{MCLK}	–	–	ns	
SID1002E	t_{MCLK_IL}	Master clock input LOW time	0.45 × t_{MCLK}	–	–	ns	
TDM Transmit Timing							
SID1003	t_{DTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	–	–	0.8 × t_{SCLK}	ns	Guaranteed by design
SID1004	t_{HTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID1011	$t_{HR\_WS\_POL\_0}$	TX Slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	

Table 27-32 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1012	$t_{HR\_WS\_POL\_1}$	TX Slave: Hold on TX_FSYNC (WS) after the 2nd edge following the driving edge of TX_CLK (SCK_POLARITY = 1, zero-cycle hold)	1.8	–	–	ns	
TDM Receive Timing							
SID1005	t_{SR}	Setup on RX_SD/RX_FSYNC (WS) before the 1st edge following the driving edge of RX_CLK	0.2 × t_{SCLK}	–	–	ns	Guaranteed by Design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE and SCK_POLARITY setting
SID1006C	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the 1st edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 0
SID1006D	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the 2nd edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 2nd edge (1 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 1, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 1
SID1006E	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the 3rd edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 3rd edge (1.5 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b01 RX Slave: Not Applicable
TDM Transition Timing							
SID1007B	t_{SCLK_TRANS}	SCLK transition timing	1	–	0.15 × t_{SCLK}	ns	Guaranteed by design
SID1008	t_{MCLK_TRANS}	MCLK transition timing	–	–	0.15 × t_{SCLK}	ns	Guaranteed by design
SID1009B	t_{DATA_TRANS}	DATA transition timing	1	–	0.15 × t_{SCLK}	ns	Guaranteed by design
(PCM) PWM							
Recommended I/O configuration: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_ENH:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_SMC:** CFG_OUT/DRIVE_SEL<1:0> = 0b01							
SID1100_2	t_{PW_2}	Pulse width on CH1_P, CH1_N, CH2_P, CH2_N for GPIO	20	–	–	ns	PWM clock ≤ 40 MHz, min pulse width nom. 25 ns – 20% max distortion (PCM) PWM can only be used at 2.7 V ≤ V_{DDD} ≤ 3.6 V Guaranteed by design
SID1101	f_{PWM}	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1110	t_{MCLK}	Master clock input period	10	–	–	ns	Guaranteed by design
SID1111	t_{MCLKI_DUTY}	Master clock input duty cycle	40	–	50	%	Guaranteed by design
Sound Generator							
Recommended I/O configuration: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_ENH:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_SMC:** CFG_OUT/DRIVE_SEL<1:0> = 0b01							
SID1102	f_{PWM}	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1103	t_{MCLK}	Master clock input period	10	–	–	ns	Guaranteed by design
SID1104	t_{MCLKI_DUTY}	Master clock input duty cycle	40	–	50	%	Guaranteed by design

27.14 CXPI specifications

Table 27-33 CXPI specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID1400	f_{CLK_AHB}	CLK_PERI clock frequency	–	–	100	MHz	Guaranteed by design, AHB Interface clock
SID1402	t_{BIT_CONT}	Width of clock disparity against the bit width t_{BIT_REF} of nominal signaling rate	–0.5	–	+0.5	%	Guaranteed by design
SID1403	$t_{RX\_0\_HI\_CONT}$	The time that should be detected the receiving node is HIGH level.	0.02	–	–	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design
SID1404	$t_{TX\_DIF\_CONT}$	Difference of width of LOW-level at the constant threshold that receiving node should discriminate logic ‘1’ and logic ‘0’	0.05	–	–	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design $t_{TX\_DIF\_CONT} = t_{TX\_0\_LO} - t_{TX\_1\_LO}$
SID1405	$t_{TX\_0\_P-D\_CONT}$[68]	At the time of logical value ‘0’ outputs, time from the LOW level detection of the communication bus unit falling the voltage “TH_dom”.	–	–	0.01	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, CTL0.FILTER_EN bit = '0', Guaranteed by design
SID1406	$t_{TX\_0\_P-D\_CONT}$[68]	At the time of logical value ‘0’ outputs, time from the LOW-level detection of the communication bus unit falling the voltage “TH_dom”.	–	–	0.0125	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, CTL0.FILTER_EN bit = '1', Guaranteed by design
SID1407	$t_{RX\_0\_FF\_-CONST}$	Delay from external serial data input pin to a flop. This is a standard to satisfy AC.11.	–	–	20	ns	Guaranteed by design
SID1408	$t_{TX\_0\_FF\_-CONST}$	Delay from a flop to external serial data output pin. This is a standard to satisfy AC.11.	–	–	80	ns	Guaranteed by design
SID1409	BR	Bit rate	–	–	20	kbps	
SID1411	OS	Oversampling factor	–	–	400		

Note
68. The AC spec, according to the CXPI controller specification, is maximum 0.01 t_{BIT}. The AC spec, according to the CXPI system specification, including transceiver or driver/receiver is maximum 0.1 t_{BIT}.

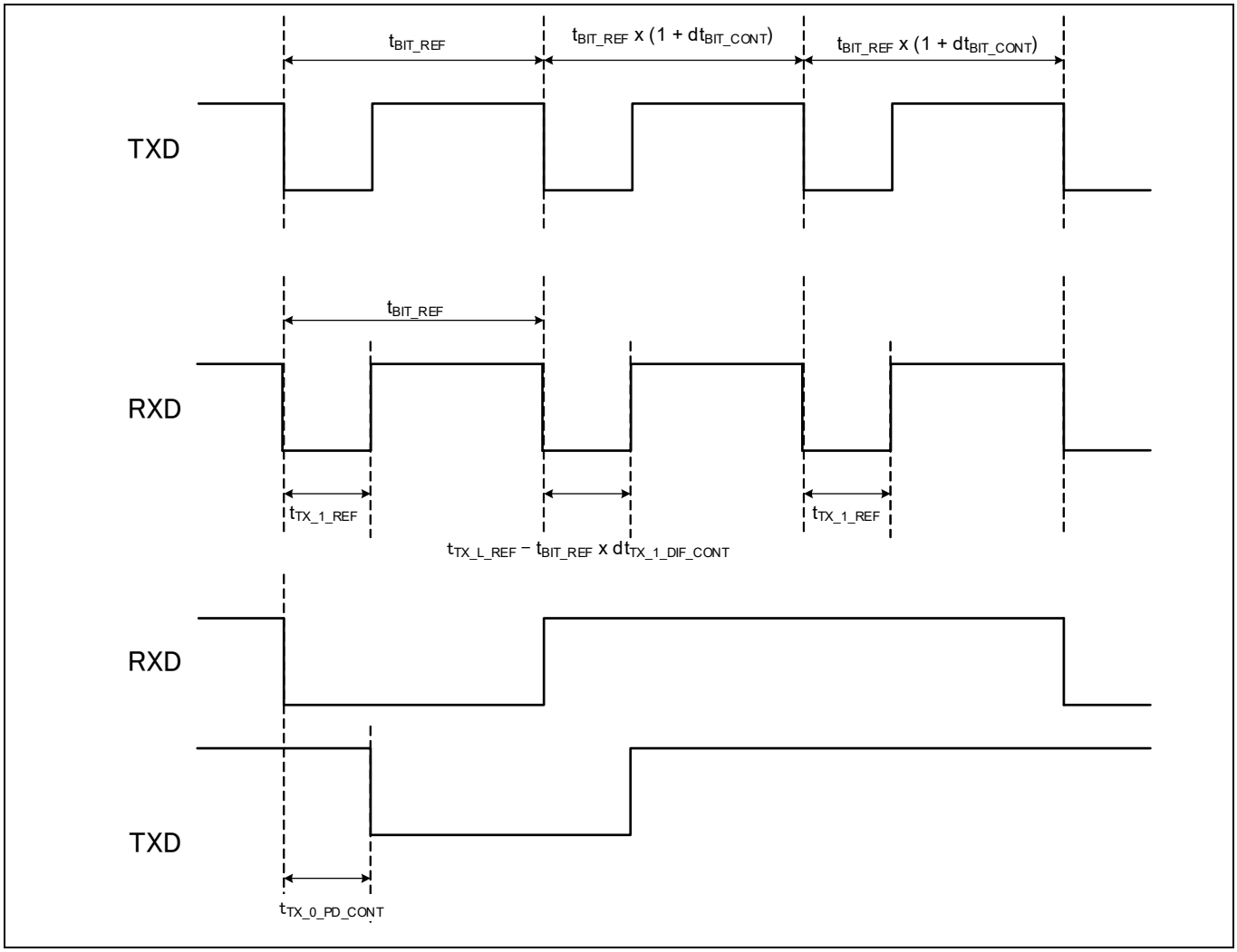


Figure 27-27 CXPI specifications

27.15 Serial memory interface specifications

Table 27-34 xSPI specifications

Spec ID	Parameter	Description	Min	Max	Units
xSPI (JEDEC JESD251 xSPI200)			**xSPI200**		
Recommended I/O configuration: **xSPI200: HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single and dual slave [load ≤ 15 pF])					
SID1500_3	t_{CK}	Interface clock period (JEDEC)	10	–	ns
SID1500_3CM	t_{CK}	Interface clock period (CMOS)	10	–	ns
SID1501_3	t_{CKDCD}	Allowable clock distortion[69]	–	0.05×t_{CK}	ns
SID1502_3	t_{CKMPW}	Minimum clock pulse width (JEDEC)	4.5	–	ns
SID1502_3CM	t_{CKMPW}	Minimum clock pulse width (CMOS)	4.5	–	ns
SID1503_3HV	OUT_SR	Output slew rate with respect to V_{OH}/V_{OL}	1.03	–	V/ns
SID1504_3	t_{OSU}	Output setup time of DS and I/O[7:0] to CK	1.1	–	ns
SID1505_3	t_{OH}	Output hold time of DS and I/O[7:0] to CK	1.1	–	ns
SID1506_3HV	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	1.03	–	V/ns
SID1507_3	t_{DSMPW}	Input min pulse width of DS (JEDEC)	4.1	–	ns
SID1507_3CM	t_{DSMPW}	Input min pulse width of DS (CMOS)	4.1	–	ns
SID1508_3	t_{RQ}	Input DS to I/O[7:0] valid time (JEDEC)	–	0.9	ns
SID1508_3CM	t_{RQ}	Input DS to I/O[7:0] valid time (CMOS)	–	0.9	ns
SID1509_3	t_{RQH}	Input I/O[7:0] invalid to DS time (JEDEC)	–	0.9	ns
SID1509_3CM	t_{RQH}	Input I/O[7:0] invalid to DS time (CMOS)	–	0.9	ns
SID1511_3	t_{CKLCSL}	CK LOW to CS LOW	8	–	ns
SID1512_3	t_{CSLCKH}	CS LOW to CK HIGH	8	–	ns
SID1513_3	t_{CKLCSH}	CK LOW to CS HIGH	8	–	ns
SID1514_3	t_{CSHCKH}	CS HIGH to CK HIGH	8	–	ns
SID1515_3	t_{DSLCSH}	DS LOW to CS HIGH	8	–	ns
SID1516_3	t_{CSHDST}	CS HIGH to DS High-Z	–	10	ns
SID1517_3	t_{CSLDSL}	CS LOW to DS LOW	0	–	ns
SID1518_3	t_{DSTCSL}	DS High-Z to CS LOW	0	–	ns

Table 27-35 xSPI (JEDEC JESD251) Delay tap recommended configuration

Feature	xSPI200
	Rx
Delay Tap Selection (*SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0>*)	6
Delay Line Selection (*SMIF_CTL/DELAY_LINE_SEL<2:0>*)	0

Note
69.PLL#400 with SSCG = 0, fractional divider = off.

Table 27-36 Input, output supported voltage reference levels

Signal	Supported modes for voltage reference levels	
	CMOS	JEDEC
Clock	$V_T = (50\% \times V_{DDIO\_HSIO})$	
RWDS (output)	$V_T = (50\% \times V_{DDIO\_HSIO})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO\_HSIO}$
DQ[7:0] (output)	$V_T = (50\% \times V_{DDIO\_HSIO})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO\_HSIO}$
RWDS (input)	$V_T = (50\% \times V_{DDIO\_HSIO})$	
DQ[7:0] (input)	$V_T = (50\% \times V_{DDIO\_HSIO})$	$V_{IH}/V_{IL} = 70\% / 30\% \times V_{DDIO\_HSIO}$

Notes

- One of the modes ("CMOS", "JEDEC") needs to be selected depending on the requirements of the actual memory.
- Some parameters may be available and listed separately for the individual modes. The corresponding mode will be mentioned in the parameter description.
- Parameters without explicit mode description (e.g. t_{OSU}) are applicable for all modes but the voltage reference level as per the table still applies.

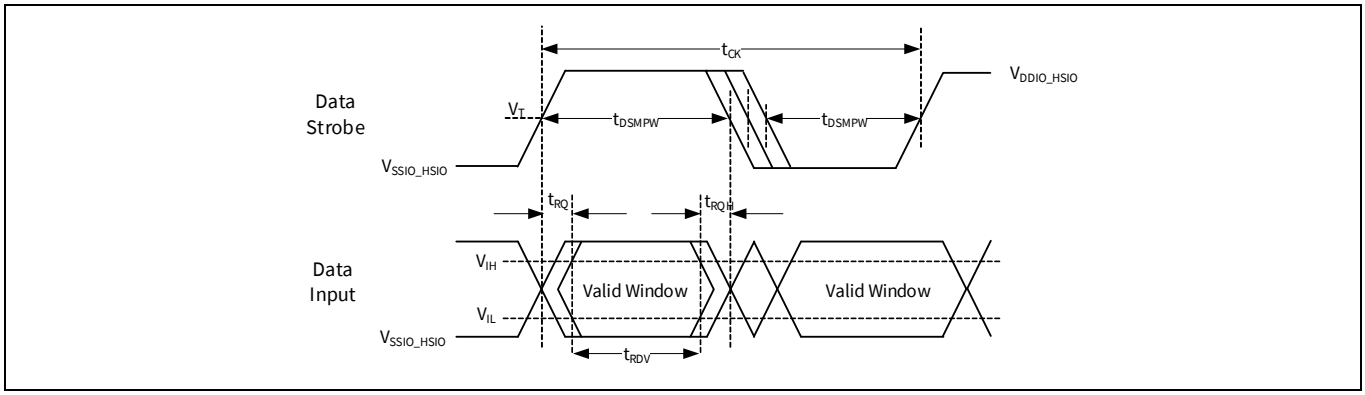


Figure 27-28 xSPI master data input timing reference level (JEDEC)

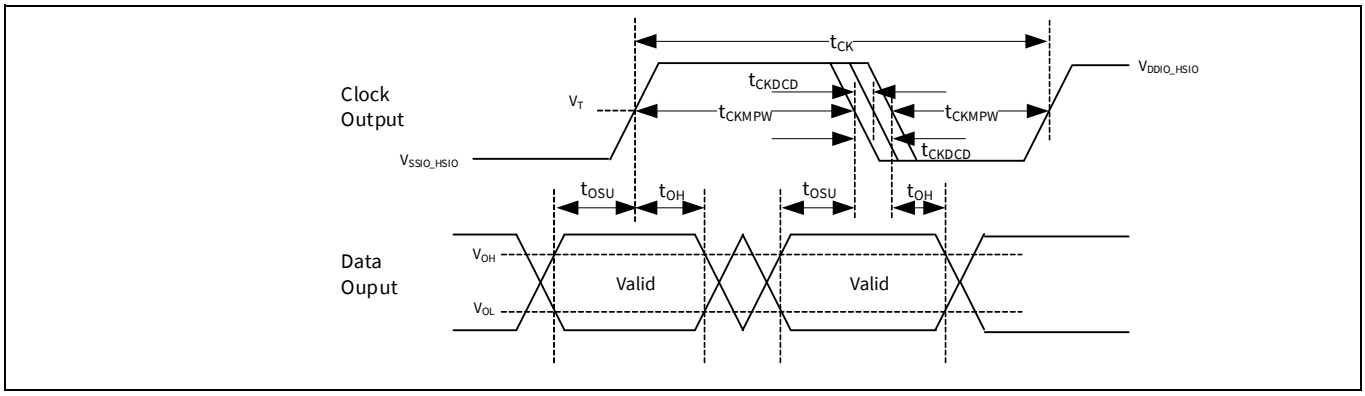


Figure 27-29 xSPI master data output timing reference level (JEDEC)

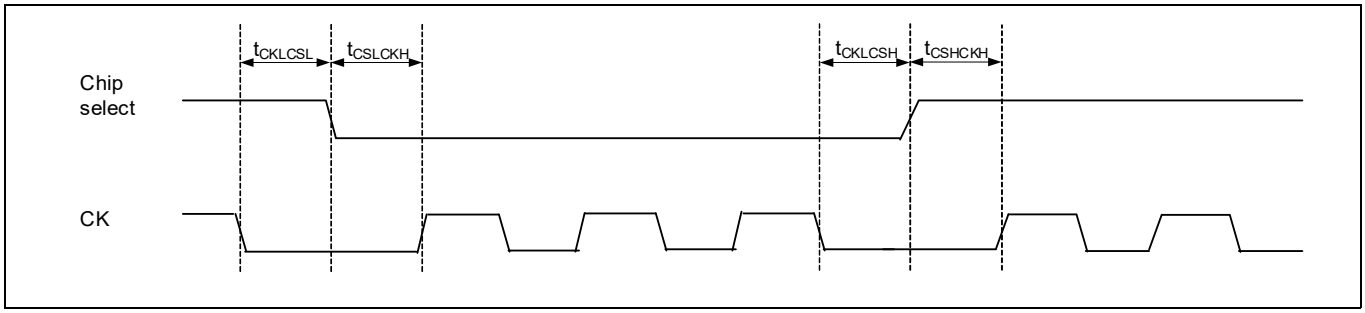


Figure 27-30 xSPI clock to chip select timing diagram

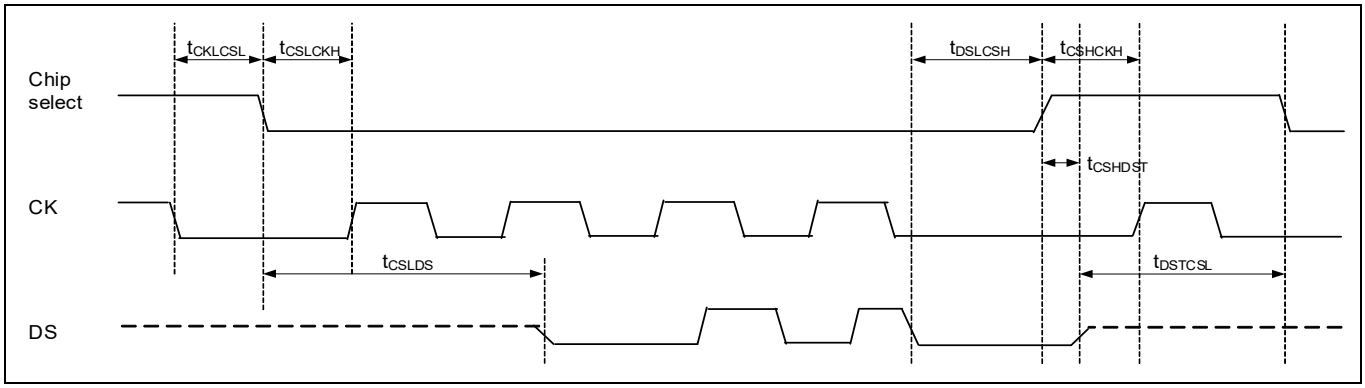


Figure 27-31 xSPI data strobe to chip select timing diagram

Table 27-37 Standard SPI specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Standard SPI SDR							
Recommended I/O configuration: **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> =0b000 **DLL Tap settings for RX**: SMIF_CTL/DELAY_LINE_SEL<2:0> = 0, SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0> = 2 All timings aligned with respect to V_T = (50% × V_{DDIO_HSIO}).							
SID1600_2[70]	t_{CK}	Interface clock period	10	–	–	ns	15-pF output loads, 3.3 V
SID1601	t_{CKPW}	Clock pulse width	0.45 × t_{CK}	–	0.55 × t_{CK}	ns	15-pF output loads
SID1602_HS	t_{CSS}	CS# active setup to CK (f_{CK} > 50 MHz)	4	–	–	ns	15-pF output loads, f_{CK} > 50 MHz Guaranteed by design
SID1602_LS	t_{CSS}	CS# active setup to CK (f_{CK} ≤ 50 MHz)	5	–	–	ns	15-pF output loads, f_{CK} ≤ 50 MHz Guaranteed by design
SID1603	t_{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1604	t_{CSH3}	CS# active hold to CK (mode 3)	6	–	–	ns	15-pF output loads Guaranteed by design
SID1605_2	t_{OSU}	Output setup time of DQ[7:0] to CK high (f_{CK} = 100 MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OSU} = t_{OSU\_min} + 0.45 \times (t_{CK} - t_{CK\_min})$ t_{OSU_min} = value at MIN of SID1605_2 t_{CK_min} = value at MIN of SID1600_2 t_{CK} = actual clock period
SID1606_2	t_{OH}	Output hold time of DQ[7:0] to CK high (f_{CK} = 100 MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OH} = t_{OH\_min} + 0.45 \times (t_{CK} - t_{CK\_min})$ t_{OH_min} = value at MIN of SID1606_2 t_{CK_min} = value at MIN of SID1600_2 t_{CK} = actual clock period
SID1607	t_{IN_V}	CK low to DQ[7:0] input valid time	1	–	6.7	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b0 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0>=0b01 3) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b1 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING

Note
70.Ensure to explicitly configure PLL#400 in Integer mode with "SSCG = OFF", "Fractional = OFF".

Table 27-37 Standard SPI specifications *(continued)*

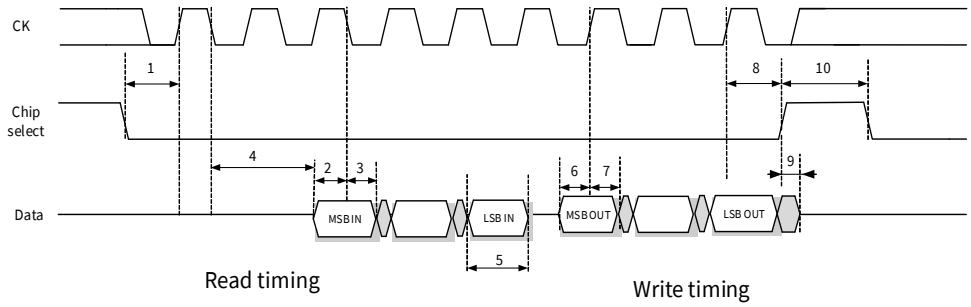
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1607A	t_{ISU}	DQ[7:0] input setup time	1.25	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011
SID1608	t_{IH}	DQ[7:0] input hold time	1.5	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011
SID1609	t_{RDV}	Input data valid time of DQ[7:0]	3.8	–	–	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b0 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0>=0b01 3) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b1 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING
SID1610	t_{CS}	CS# HIGH time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1610A	t_{CS}	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1610B	t_{CS}	CS# High time (Program / Erase)	50	–	–	ns	15-pF output loads Guaranteed by design
SID1611	t_{DIS}	CS# inactive to output disable time	–	–	8	ns	15-pF output loads Guaranteed by design
SID1614	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	1.03	–	–	V/ns	–
Standard SPI DDR							
Recommended I/O configuration: **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> =0b000 **DLL Tap settings for RX**: SMIF_CTL/DELAY_LINE_SEL<2:0> = 0, SMIF_DEVICE_DELAY_TAP_SEL/DELAY_TAPS_NR_LOG2<7:0> = 2 All timings aligned with respect to V_T = (50% × V_{DDIO_HSIO}).							
SID1700_2[70]	t_{CK}	Interface clock period	12.5	–	–	ns	15-pF output loads, 3.3 V
SID1701	t_{CKPW}	Clock pulse width	0.45 × t_{CK}	–	0.55 × t_{CK}	ns	15-pF output loads
SID1702_HS	t_{CSS}	CS# active setup to CK (f_{CK} > 50 MHz)	4	–	–	ns	15-pF output loads, f_{CK} > 50 MHz Guaranteed by design
SID1702_LS	t_{CSS}	CS# active setup to CK (f_{CK} ≤ 50 MHz)	5	–	–	ns	15-pF output loads, f_{CK} ≤ 50 MHz Guaranteed by design
SID1703	t_{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design

Table 27-37 Standard SPI specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1705_2	t_{OSU}	Output setup time of DQ[7:0] to CK edge (f_{CK} = 80MHz)	2.1	–	–	ns	15-pF output loads For other frequencies: $t_{OSU} = t_{OSU\_min} + 0.225 \times (t_{CK} - t_{CK\_min})$ t_{OSU_min} = value at MIN of SID1705_2 t_{CK_min} = value at MIN of SID1700_2 t_{CK} = actual clock period
SID1706_2	t_{OH}	Output hold time of DQ[7:0] to CK edge (f_{CK} = 80MHz)	1.6	–	–	ns	15-pF output loads For other frequencies: $t_{OH} = t_{OH\_min} + 0.225 \times (t_{CK} - t_{CK\_min})$ t_{OH_min} = value at MIN of SID1706_2 t_{CK_min} = value at MIN of SID1700_2 t_{CK} = actual clock period
SID1707	t_{IN_V}	CK edge to DQ[7:0] input valid time	1	–	6.7	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b0 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0>=0b01 3) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b1 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING
SID1707A	t_{ISU}	DQ[7:0] input setup time	1.25	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011
SID1708	t_{IH}	DQ[7:0] input hold time	1.5	–	–	ns	CTL/DELAY_TAP_ENABLE=0 (Delay line is disabled/bypassed) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011
SID1709_2	t_{RDV}	Input data valid time of DQ[7:0] ($f_{CK} \leq$ 80 MHz)	3.5	–	–	ns	CTL/DELAY_TAP_ENABLE=1 (Delay line is enabled) Three options 1) CTL/CLOCK_IF_RX_SEL<2:0> = 0b011 2) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b0 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0>=0b01 3) CTL/CLOCK_IF_RX_SEL<2:0> = 0b100 or 0b101 CTL/INT_CLOCK_DL_ENABLED<0:0> =0b1 CTL/INT_CLOCK_CAPTURE_CYCLE<1:0> needs to be adjusted based on INTR/DL_WARNING

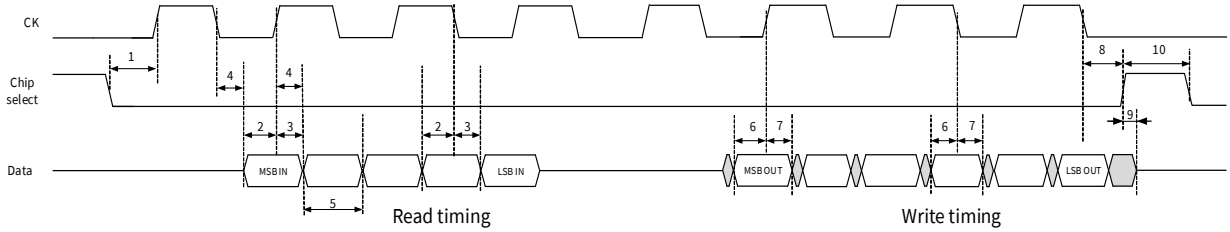
Table 27-37 Standard SPI specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1710	t_{CS}	CS# High time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1710A	t_{CS}	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1710B	t_{CS}	CS# High time (Program / Erase)	50	–	–	ns	15-pF output loads Guaranteed by design
SID1711	t_{DIS}	CS# inactive to output disable time	–	–	8	ns	15-pF output loads Guaranteed by design
SID1714	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	1.03	–	–	V/ns	–



1: CS# active setup to CK = t_{CSS}
2: Data setup time = t_{ISU}
3: Data hold time = t_{IH}
4: CK low to DQ[7:0] input valid time = t_{IN_V}
5: Read data valid time of DQ[7:0] = t_{RDV}
6: Output setup of DQ[7:0] to CK rise = t_{OSU}
7: Output hold time of DQ[7:0] from CK rise = t_{OH}
8: CS# active hold to CK = t_{CSH}
9: CS# inactive to output disable = t_{DIS}
10: Chip select HIGH time = t_{CS}

Figure 27-32 SDR write and read timing diagram



1: CS# active setup time to CK = t_{CSS}
2: Data setup time = t_{ISU}
3: Data hold time = t_{IH}
4: CK edge low to DQ[7:0] input valid time = t_{IN_V}
5: Read data valid time of DQ[7:0] = t_{RDV}
6: Output setup time of DQ[7:0] to CK edge = t_{OSU}
7: Output hold time of DQ[7:0] from CK edge = t_{OH}
8: CS# active hold time to CK = t_{CSH}
9: CS# inactive to output disable time = t_{DIS}
10: CS# HIGH time = t_{CS}

Figure 27-33 DDR write and read timing diagram

27.16 LCD controller specifications

Table 27-38 LCD controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID1243	f_{LCD_FR}	LCD frame rate	10	–	150	Hz	

28 Ordering information

The CYT2CL microcontroller part numbers and features are listed in **Table 28-1**. The Arm® TAP JTAG ID is 0x6BA0 0477.

Table 28-1 CYT2CL Ordering information[71]

Device Code	Ordering code	Package	Code-flash (KB)	Work-flash (KB)	SRAM (KB)	ADC Channels	SCB Channels	LIN Channels	CANFD Channels	CXPI Channels	LCD	SMIF	Mixer	PCM-PWM	TDM	Temperature Grade	JTAG ID CODE
CYT2CL7BAS	CYT2CL7BAAQ0AZSGS	144-LQFP[77]	4160[72]	128[73]	512	48	12	2	4	2	32 S x 4 C[74]	1x	1x	1x	2x	S[75]	0x1EC03069[76]
CYT2CLHBAS	CYT2CLHBAAQ0AZSGS	144-LQFP[78]	4160	128	512	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	S	0x1EC05069
CYT2CL8BAS	CYT2CL8BAAQ0AZSGS	176-LQFP	4160	128	512	48	12	2	4	2	32 S x 4 C	1x	1x	1x	2x	S	0x1EC01069

Notes
71. Supported shipment types are “Tray” (default) and “Tape and Reel”. Add the character ‘T’ at the end to get the ordering code for “Tape and Reel” shipment type.
72. Code-flash size 4160 KB = 32 KB × 126 (Large Sectors) + 8 KB × 16 (Small Sectors).
73. Work-flash size 128 KB = 2 KB × 48 (Large Sectors) + 128 B × 256 (Small Sectors).
74. 32 Segments and 4 Commons.
75. S-grade Temperature (–40°C to 105°C).
76. JTAG ID CODE bits 12 through 27, represents the Silicon ID of the device.
77. Package pin pitch is 0.5 mm.
78. Package pin pitch is 0.4 mm.

28.1 Part number nomenclature

Table 28-2 Device code nomenclature

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family	2	TRAVEO™ T2G (Core M4)
B	Application	C	Cluster Entry
D	Code-flash/Work-flash/SRAM quantity	L	4160 KB / 128 KB / 512 KB
P	Packages	8	176-LQFP
		7	144-LQFP (0.5 mm Pitch)
		H	144-LQFP (0.4 mm Pitch)
H	Hardware option	B	Security on (HSM), RSA-3072
I	Marketing option	A	No options
C	Temperature grade	S	S-grade (–40°C to 105°C)

Table 28-3 Ordering code nomenclature

Field	Description	Value	Meaning
CY	Cypress Prefix	CY	
T	Category	T	TRAVEO™
2	Family name	2	TRAVEO™ T2G (Core M4)
B	Application	C	Cluster Entry
D	Code-flash/Work-flash/SRAM quantity	L	4160 KB / 128 KB / 512 KB
P	Packages	8	176-LQFP
		7	144-LQFP (0.5 mm Pitch)
		H	144-LQFP (0.4 mm Pitch)
H	Hardware option	B	Security on (HSM), RSA-3072
I	Marketing option	A	No options
R	Revision	A	First revision
F	Fab location	Q	UMC (Fab 12i) Singapore
X	Reserved	0	Reserved
K	Package code	AZ	LQFP
C	Temperature grade	S	S-grade (–40°C to 105°C)
Q	Quality grade	ES	Engineering samples
		GS	Standard grade of automotive
S	Shipment type	Blank	Tray shipment
		T	Tape and reel shipment

29 Packaging

CYT2CL is offered in the packages listed in the **Table 29-1**.

Table 29-1 Package information

Package	Dimensions[79]	Contact/ Lead Pitch	Coefficient of Thermal Expansion[83]	I/O pins
176-LQFP	24 × 24 × 1.7 mm (max)	0.5 mm	a1[80] = 8.5 ppm/°C, a2[81] = 33.8 ppm/°C	140
144-LQFP	20 × 20 × 1.7 mm (max)	0.5 mm	a1[80] = 8.5 ppm/°C, a2[81] = 33.7 ppm/°C	108
144-LQFP	16 × 16 × 1.7 mm (max)	0.4 mm	a1[80] = 8.5 ppm/°C, a2[81] = 33.65 ppm/°C	108

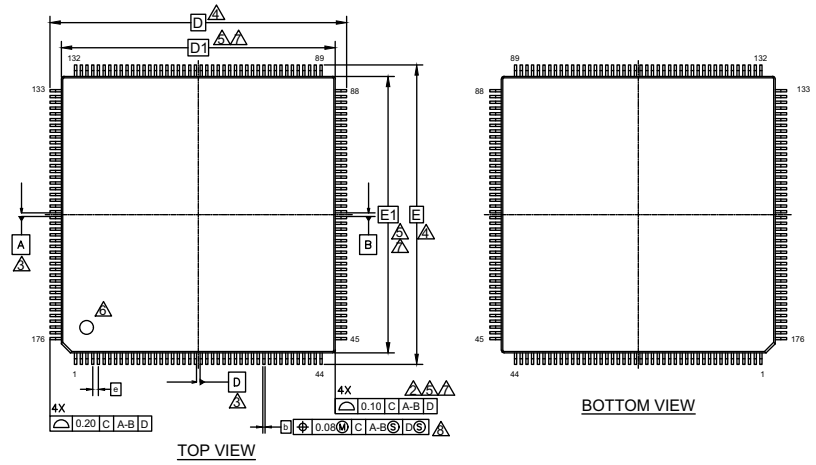
Table 29-2 Package characteristics[82]

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	S-grade	–40	–	105	°C
T_J	Operating junction temperature	–	–	–	150	°C
$R_{\theta JA}$	Package thermal resistance, junction to ambient θ_{JA}[79]	144 LQFP (0.4 mm)	–	–	23.0	°C/Watt
		144 LQFP (0.5 mm)	–	–	23.1	°C/Watt
		176 LQFP	–	–	21.8	°C/Watt
$R_{\theta JB}$	Package thermal resistance, junction to board θ_{JB}	144 LQFP (0.4 mm)	–	–	15.3	°C/Watt
		144 LQFP (0.5 mm)	–	–	15.0	°C/Watt
		176 LQFP	–	–	14.8	°C/Watt
$R_{\theta JC}$	Package thermal resistance, junction to case θ_{JC}	144 LQFP (0.4 mm)	–	–	5.2	°C/Watt
		144 LQFP (0.5 mm)	–	–	5.3	°C/Watt
		176 LQFP	–	–	4.5	°C/Watt

Table 29-3 Solder reflow peak temperature, package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	Maximum peak temperature (°C)	Maximum time at peak temperature (seconds)	MSL
144 LQFP (0.4 mm)	260	30	3
144 LQFP (0.5 mm)	260	30	3
176 LQFP	260	30	3

Notes
79.The dimensions (column 2) are valid for room temperature.
80.a1 = CTE (Coefficient of Thermal Expansion) value below T_g (ppm/°C) (T_g is glass transition temperature which is 131°C).
81.a2 = CTE value above T_g (ppm/°C).
82.Board condition complies to JESD51-7 (4 Layers).
83.The numbers are estimated values based simulation only and are based on a single bill of material combination per package type.



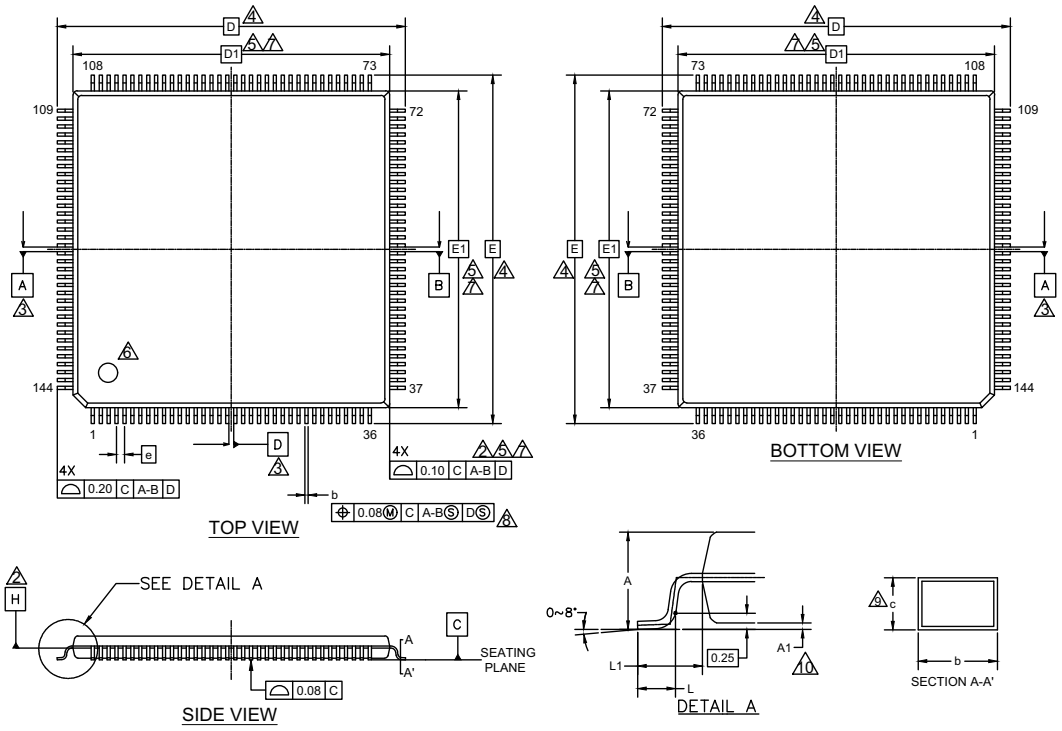
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D		26.00 BSC	
D1		24.00 BSC	
e		0.50 BSC	
E		26.00 BSC	
E1		24.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A–B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 *A

Figure 29-1 Package outline – 176-LQFP



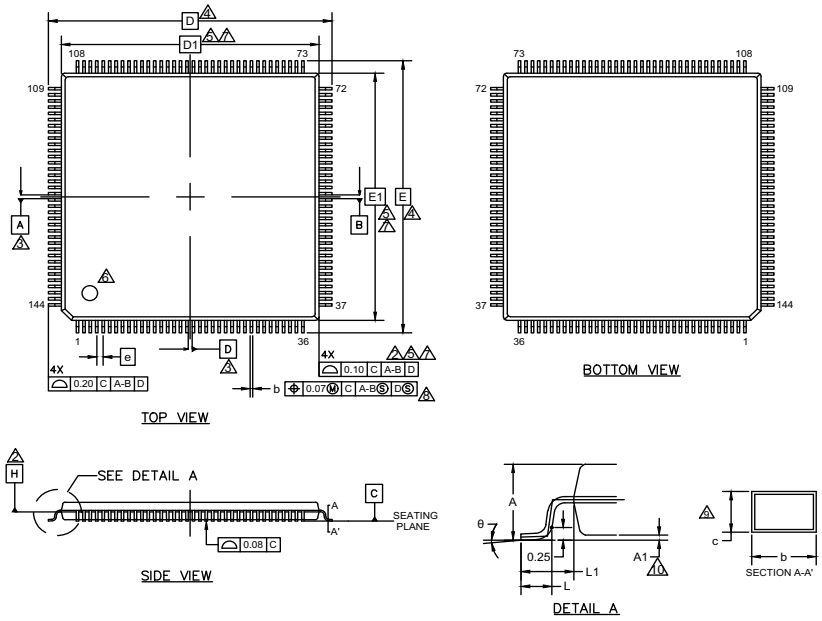
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A–B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *B

Figure 29-2 Package outline – 144-LQFP (0.5 mm)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.145	0.18	0.215
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.40 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	—	8°

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTI LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A–B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETE AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATE WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER B SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARG FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BU BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMB PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-14045 *A

Figure 29-3 Package outline – 144-LQFP (0.4 mm)

30 Appendix

30.1 Bootloading or End-of-line programming

- Triggered at device startup, if a trigger condition is applied
- Either CAN or LIN communication may be used
- Bootloader polls for the communication on CAN or LIN at separate time frames, until the overall 300-second timeout is reached
- If a boot loader command is received on either communication interface, the polling stops and boot loader starts using this interface

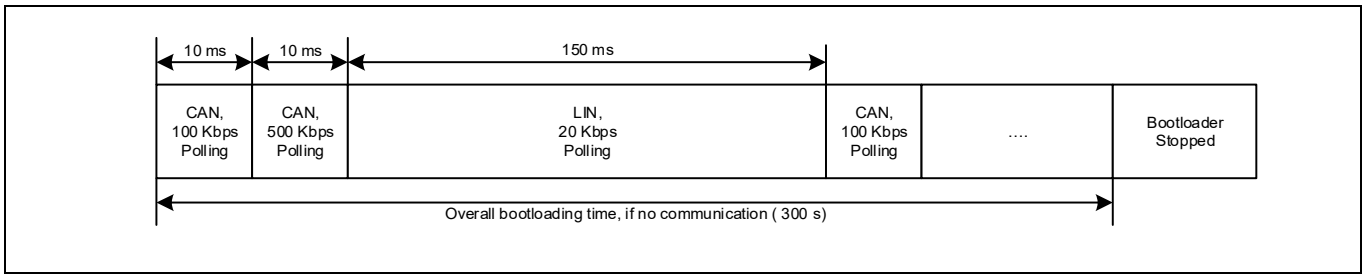


Figure 30-1 Bootloading sequence

Table 30-1 CAN interface details

Sl. No.	CAN interface	Configuration
1	CAN Mode	Classic CAN
2	CAN Instance	CAN0, Channel#0
3	CAN TX	P18.2 / CAN0_0_TX
4	CAN RX	P18.3 / CAN0_0_RX
5	CAN Transceiver EN (High)	P19.2
6	CAN Transceiver EN (Low)	P19.3
7	CAN RX Message ID	0x1A1
8	CAN TX Message ID	0x1B1
9	Baud	100 or 500 kbps alternating

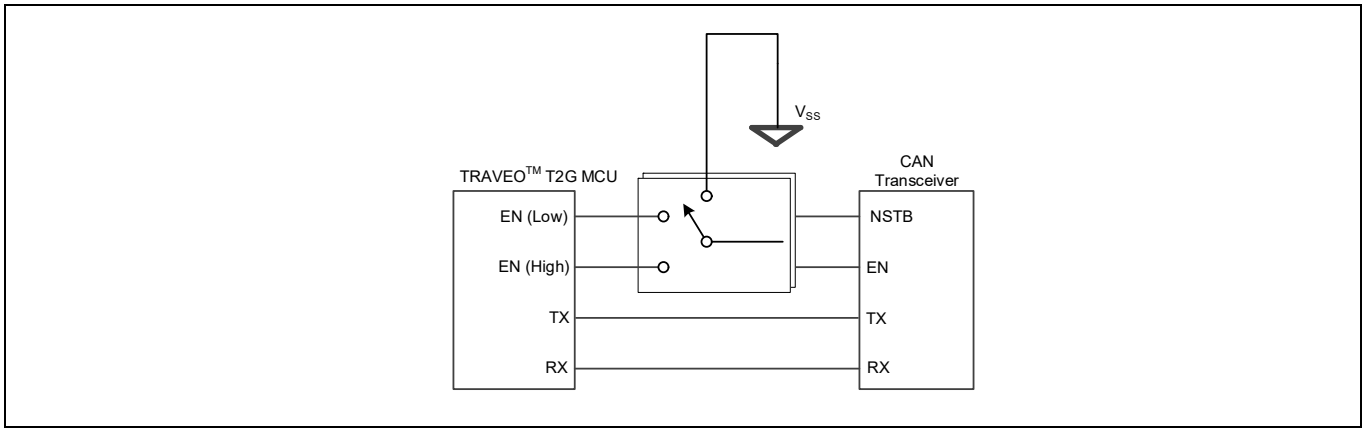


Figure 30-2 MCU to CAN transceiver connections

Table 30-2 LIN interface details

Sl. No.	LIN interface	Configuration
1	LIN type	LIN0, Channel#0
2	LIN mode	Slave
3	LIN checksum type	Classic
4	LIN TX	P19.0 / LIN0_0_TX
5	LIN RX	P19.1 / LIN0_0_RX
6	LIN EN / EN (High)	P19.2
7	LIN EN (Low)	P19.3
8	LIN TX PID	0x46
9	LIN RX PID	0x45
10	Baud	20 or 115.2 kbps
11	Break field length	11
12	Break delimiter length	1 bit

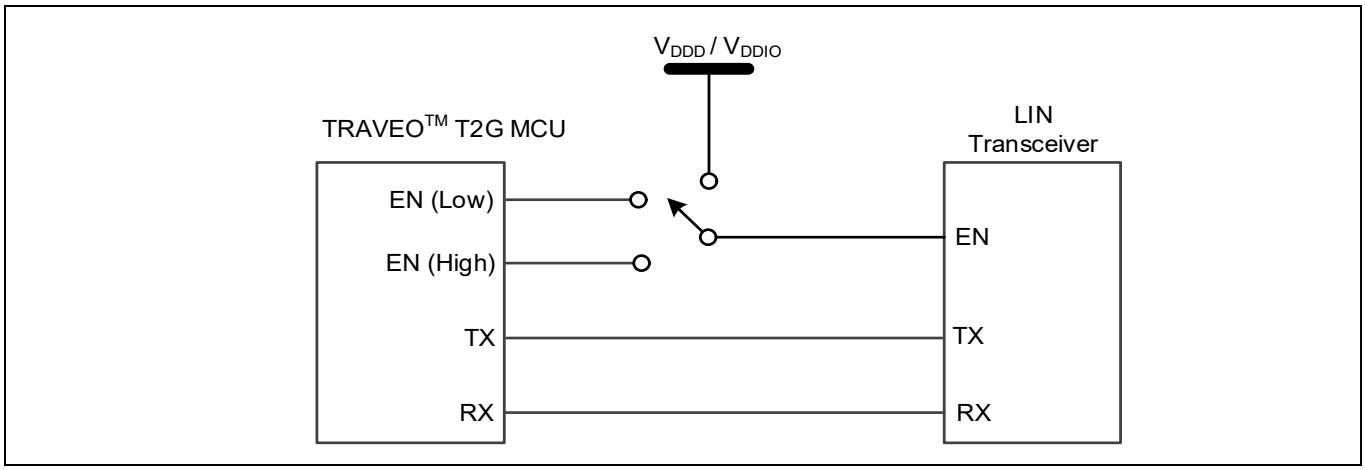


Figure 30-3 MCU to LIN transceiver connections

30.2 External IP revisions

Table 30-3 External IP revisions

Module	IP	Revision	Vendor
CAN FD	mxttcanfd	M_TTCAN IP revision: Rev.3.2.3	Bosch
Arm® Cortex®-M0+	armcm0p	Cortex®-M0+-r0p1	Arm®
Arm® Cortex®-M4F	armcm4	Cortex®-M4-r0p1	Arm®
Arm® Coresight	armcoresighttk	CoreSight-SoC-TM100-r3p2	Arm®

30.3 Internal IP revisions

Table 30-4 Internal IP revisions

Module	Revision
SMIF	SMIF version 3.0 (Variant v3.1)

31 Acronyms

Table 31-1 Acronyms used in the document

Acronym	Description	Acronym	Description
A/D	Analog to Digital	IRQ	Interrupt request
ABS	Absolute	JTAG	Joint test action group
ADC	Analog to Digital converter	LDO	Low drop out regulators
AES	Advanced encryption standard	LIN	Local Interconnect Network, a communications protocol
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus	LVD	Low voltage detection
Arm®	Advanced RISC machine, a CPU architecture	OTA	Over-the-air programming
ASIL	Automotive safety integrity level	OTP	One-time programmable
BOD	Brown-out detection	OVD	Overvoltage detection
CAN FD	Controller Area Network with Flexible Data rate	P-DMA	Peripheral-Direct Memory Access same as DW
CMOS	Complementary metal-oxide-semiconductor	PLL	Phase Locked Loop
CPU	Central Processing Unit	POR	Power-on reset
CRC	Cyclic redundancy check, an error-checking protocol	PPU	Peripheral protection unit
CSV	Clock supervisor	PRNG	Pseudorandom number generator
CTI	Cross trigger interface	PWM	Pulse-width modulation
CXPI	Clock Extension Peripheral Interface	MCU	Microcontroller Unit
DES	Data encryption standard	MCWDT	Multi-counter watchdog timer
DFT	Design-For-Test	M-DMA	Memory-Direct Memory Access
DW	Datawire same as P-DMA	MISO	SPI Master-in slave-out
ECC	Error correcting code/Elliptical curve cryptography	MMIO	Memory mapped I/O
ECO	External crystal oscillator	MOSI	SPI Master-out slave-in
ETM	Embedded Trace Macrocell	MPU	Memory protection unit
EVTGEN	Event Generator	MTB	Micro trace buffer
FLL	Frequency Locked Loop	MUL	Multiplier
FPU	Floating point unit	MUX	Multiplexer
GHS	Green Hills tool chain with Multi IDE	NVIC	Nested vectored interrupt controller
GPIO	General purpose input/output	RAM	Random access memory
HSM	Hardware security module	RISC	Reduced-instruction-set computing
I/O	Input/output	ROM	Read only memory
I^2C	Inter-Integrated Circuit, a communications protocol	RSA	Rivest-Shamir-Adleman Public Key Encryption Algorithm
ILO	Internal low-speed oscillator	RTC	Real-time clock
IMO	Internal main oscillator	SAR	Successive approximation register

Table 31-1 Acronyms used in the document *(continued)*

Acronym	Description	Acronym	Description
IOSS	Input/output sub-system	SCB	Serial communication block
IPC	Inter-processor communication	SCL	I^2C serial clock
IrDA	Infrared interface	SDA	I^2C serial data
SECDED	Single error correction, double error detection	TCPWM	Timer/Counter Pulse-width modulator
SHA	Secure hash algorithm	TTL	Transistor-transistor logic
SHE	Secure hardware extension	TRNG	True random number generator
SMPU	Shared memory protection unit	UART	Universal Asynchronous Transmitter Receiver
SPI	Serial peripheral interface, a communications protocol	WCO	Watch crystal oscillator
SRAM	Static random access memory	WDT	Watchdog timer reset
SWD	Serial wire debug	XRES_L	External reset I/O pin
SWJ	Serial wire JTAG		

32 Errata

This section describes the errata for the CYT2CL product family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Infineon Sales Representative if you have questions.

Part Numbers Affected

Part Number
All CYT2CL parts

CYT2CL Qualification Status

Production samples

CYT2CL Errata Summary

The following table defines the errata applicability to available CYT2CL family devices.

Items	Errata ID	CYT2CL	Silicon Rev.	Fix Status
[1.] **CAN FD RX FIFO top pointer feature does not function as expected**	96	CYT2CL7BAAQ0AZSGS CYT2CLHBAAQ0AZSGS CYT2CL8BAAQ0AZSGS	A	No silicon fix planned. Use workaround.
[2] **CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set**	97			No silicon fix planned. Use workaround.
[3] **TPIU peripheral ID mismatch**	98			No silicon fix planned.
[4] **CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID**	147			No silicon fix planned. Use workaround.
[5] **CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID**	167			No silicon fix planned. TRM was updated.
[6] **Misleading status is returned for Flash and eFuse system calls if there are pending NC ECC faults in SRAM controller #0**	175			No silicon fix planned. TRM was updated.
[7] **WDT reset causes loss of SRAM retention**	176			No silicon fix planned. TRM was updated.
[8] **Crypto ECC errors may be set after boot with application authentication**	185			No silicon fix planned. TRM was updated.
[9]**Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode**	198			Fixed to update the Flash settings from date code 312xxxxx.
[10]**Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep**	199			No silicon fix planned. TRM was updated.
[11] **A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM**	201			No silicon fix planned. Register TRM was updated.
[12] **Limitation of clock configuration before entering DeepSleep mode**	202			No silicon fix planned. TRM was updated.
[13] **Several data retention information in Register TRM are incorrect**	203			No silicon fix planned. Register TRM was updated.
[14] **SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally**	204			No silicon fix planned. Register TRM was updated.
[15] **Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode**	206			No silicon fix planned. TRM will be updated.
[16] **CM0+ operating frequency (CLK_SLOW) should be changed to 80 MHz or lower during eFuse reads**	207			Boot operating frequency will be changed from 100 MHz to 50 MHz in factory setting via Manufacturing Test Program. PCN will be released. Datasheet was updated.

Items	Errata ID	CYT2CL	Silicon Rev.	Fix Status
[17] **CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete**	209	CYT2CL7BAAQ0AZSGS CYT2CLHBAAQ0AZSGS CYT2CL8BAAQ0AZSGS	A	No silicon fix planned. Use workaround.
[18] **Added definition of minimum input slew rate for SPI-SDR and SPI-DDR of SMIF**	210			No silicon fix planned. Datasheet was updated.
[19] **Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM**	212			No silicon fix planned. Datasheet was updated. Architecture TRM will be updated.

1. CAN FD RX FIFO top pointer feature does not function as expected	
Problem Definition	RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should be re-start back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not re-start back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA to read messages from the wrong address in Message RAM.
Parameters Affected	N/A
Trigger Condition(s)	RX FIFO top pointer function is used when RX FIFO n size set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).
Scope of Impact	Received message cannot be correctly read by using RX FIFO top pointer function, when RX FIFO n size set to 1 element.
Workaround	Any of the following. 1) Set RX FIFO n size to 2 or more when using RX FIFO top pointer function. 2) Do not use RX FIFO top pointer function when RX FIFO n size set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.
Fix Status	No silicon fix planned. Use workaround.

2. CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set	
Problem Definition	If either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters Bus-off state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.
Parameters Affected	N/A
Trigger Condition(s)	Either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters Bus-off state.
Scope of Impact	The errata is limited to the use case when the Debug on CAN functionality is active. Normal operation of CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the bit CANFD_CH_RXF1S.DMS. In case CANFD_CH_RXF1S.DMS is set to 0b11, DMA request remains active. Bosch classifies this as non-critical error with low severity, there is no fix for the IP. Bosch recommends the workaround listed also here.
Workaround	In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.
Fix Status	No silicon fix planned. Use workaround.

3. TPIU peripheral ID mismatch	
Problem Definition	TPIU peripheral ID indicates that it is M3-TPIU instead of M4-TPIU.
Parameters Affected	N/A
Trigger Condition(s)	When debugger reads PID registers for component identification.
Scope of Impact	The debuggers read the TPIU as M3-TPIU and no other impact other than this.
Workaround	No specific workaround required. Debuggers can use trace features.
Fix Status	No silicon fix planned.

4. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID	
Problem Definition	Configuration: Several Tx Buffers are configured with same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests. Expected behavior: When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first. Observed behavior: It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).
Parameters Affected	N/A
Trigger Condition(s)	When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.
Scope of Impact	In the case described it may happen, that Tx Buffers configured with the same Message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).
Workaround	Any of the following: 1) First write the group of Tx message with the same Message ID to the Message RAM and then afterwards request transmission of all these messages concurrently by a single write access to CANFDx_CHy_TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request. 2) Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order. Applications not able to use workaround #1 or #2 can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.
Fix Status	No silicon fix planned. Use workaround.

5. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID	
Problem Definition	The following is the updated description in Section 3.5.2, Dedicated Tx Buffers and 3.5.4 Tx Queue, of the Architecture TRM related to transmission from multiple buffers configured with the same Message ID. **3.5.2 Dedicated Tx Buffers** - TRM Wording: If multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first. - Enhancement: These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR. **3.5.4 Tx Queue** - TRM Wording: If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first. - Replacement: In case multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT Index, a prediction of the transmission order is not possible. - Wording TRM: An Add Request cyclically increments the Put Index to the next free Tx Buffer. - Replacement: The PUT Index always points to that free buffer of the Tx Queue with the lowest number.
Parameters Affected	N/A
Trigger Condition(s)	Using multiple dedicated Tx Buffers or Tx Queue Buffers configured with the same Message ID.
Scope of Impact	In case the dedicated Tx Buffers with the same Message ID are not requested in ascending order or at the same time or in case there are multiple Tx Queue Buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.
Workaround	In case a defined order of transmission is required, the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx Buffers with the same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to CANFDx_CHy_TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.
Fix Status	No silicon fix planned. Use workaround. TRM was updated.

6. Misleading status is returned for Flash and eFuse system calls if there are pending NC ECC faults in SRAM controller #0	
Problem Definition	Flash and eFuse system calls will return misleading status of 0xf0000005 (“Page is write protected”) even for non-protected row or 0xf0000002 (“Invalid eFuse address”) for valid eFuse address in case of pending NC ECC faults in SRAM controller #0.
Parameters Affected	Return status of Flash and eFuse system calls
Trigger Condition(s)	NC ECC fault(s) pending in SRAM controller #0 and SWPUs are populated in the design.
Scope of Impact	Flash and eFuse system calls will not work until the NC ECC fault(s) pending in SRAM controller #0 is properly handled.
Workaround	If the NC ECC fault(s) are not due to HW malfunction (i.e., if the faults are due to usage of non-initialized SRAM or improper SRAM initialization), then clearing of these pending faults will resolve the issue.
Fix Status	No silicon fix planned. TRM was updated.

7. WDT reset causes loss of SRAM retention	
Problem Definition	Architecture TRM Table 19-1 shows WDT reset can retain SRAM if there is an orderly shutdown of the SRAM only during a warning interrupt. However, this is wrong. WDT reset causes loss of SRAM retention.
Parameters Affected	N/A
Trigger Condition(s)	WDT reset
Scope of Impact	WDT reset causes loss of SRAM retention.
Workaround	None
Fix Status	No silicon fix planned. TRM was updated.

8. Crypto ECC errors may be set after boot with application authentication	
Problem Definition	Due to the improper initialization of the Crypto memory buffer, Crypto ECC errors may be set after boot with application authentication.
Parameters Affected	N/A
Trigger Condition(s)	Boot device with application authentication.
Scope of Impact	Crypto ECC errors may be set after boot with application authentication.
Workaround	Clear or ignore Crypto ECC errors which generated during boot with application authentication.
Fix Status	No silicon fix planned. TRM was updated.

9. Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode	
Problem Definition	Code Flash memory can be erased in “Non-Blocking” mode; a Non-Blocking mode supported option allows users to suspend an ongoing erase sector operation. When an ongoing erase operation is interrupted using “Erase Suspend” and “Erase Resume”, Flash cells may not have been erased completely, even after the erase operation complete is indicated by FLASHC_STATUS register. Only Code Flash is impacted by this issue, Work Flash and Supervisory Flash (SFlash) are not impacted.
Parameters Affected	N/A
Trigger Condition(s)	Using EraseSector System Call in Non-Blocking mode for CM0+ to erase Code Flash and the ongoing erase operation is interrupted using EraseSuspend and EraseResume System calls.
Scope of Impact	When Code Flash sectors are erased in Non-Blocking mode and the ongoing erase operation is interrupted by Erase Suspend / Erase Resume, it cannot be guaranteed that the Code Flash cells are fully erased. Any read on the Code Flash area after the erase is complete or read on the programmed data after ProgramRow is complete can trigger ECC errors.
Workaround	Use any of the following: 1) Use Non-Blocking mode for EraseSector, but do not interrupt the erase operation using Erase Suspend / Erase Resume. 2) If a Code Flash sector erase operation is interrupted using Erase Suspend / Erase Resume, then erase the same sector again without Erase Suspend / Erase Resume before reading the sector or programming the sector.
Fix Status	Fixed to update the Flash settings from date code 312xxxxx.

10. Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep	
Problem Definition	The port state is not retained when the port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.
Parameters Affected	N/A
Trigger Condition(s)	The port selects peripherals (except for LIN or CAN-FD) and MCU wakes up from DeepSleep.
Scope of Impact	Unexpected port output change might affect user system.
Workaround	If the port selects peripherals (except for LIN or CAN FD), and the port output value needs to be maintained after wakeup from DeepSleep, set HSIOM_PRTx_PORT_SEL.IOy_SEL = 0 (GPIO) before DeepSleep and set the required output value in GPIO configuration registers. After wakeup, change HSIOM_PRTx-_PORT_SEL.IOy_SEL back to the peripheral module as needed.
Fix Status	No silicon fix planned. TRM was updated.

11. A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM	
Problem Definition	The following description is not present for PWR_CTL2.BGREF_LPMODE in the existing register TRM. “This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchro-nization.”
Parameters Affected	N/A
Trigger Condition(s)	Using the PWR_CTL2.BGREF_LPMODE.
Scope of Impact	PWR_CTL2.BGREF_LPMODE may not be set or cleared.
Workaround	Use the PWR_CTL2.BGREF_LPMODE according to the following description. “This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchro-nization.”
Fix Status	No silicon fix planned. Register TRM was updated.

12. Limitation of clock configuration before entering DeepSleep mode	
Problem Definition	DeepSleep should not be entered while any FLL/PLL is enabled and using ECO/LPECO as its reference clock. Since the unstable ECO/LPECO clock after wakeup is outside the allowed reference clock limits for FLL/PLL, there is possibility of failing the DeepSleep wakeup.
Parameters Affected	N/A
Trigger Condition(s)	DeepSleep transition while any FLL/PLL is enabled and using ECO/LPECO as its reference clock.
Scope of Impact	There is possibility of failing the DeepSleep wakeup.
Workaround	If any FLL/PLL is operating with the ECO/LPECO as its reference clock, change the clock to either ECO/LPECO direct or IMO direct or IMO with FLL/PLL before entering DeepSleep.
Fix Status	No silicon fix planned. TRM was updated.

13. Several data retention information in Register TRM are incorrect	
Problem Definition	The following registers are described as 'Retained' in the Register TRM while it is not guaranteed that the value before entering DeepSleep mode is still readable from the register. - SARADC: PASSx_SARy_CHz_RESULT - SRSS: PWR_LVD_STATUS - SRSS: PWR_LVD_STATUS2 - SRSS: CLK_CAL_CNT1 - SRSS: CLK_CAL_CNT2 - SRSS: CLK_FLL_STATUS - SRSS: WDT_INTR - SRSS: WDT_INTR_MASKED - SRSS: CLK_PLL400Mx_STATUS - MIXER: MIXER_DST_STRUCT_INTR_DST_MASKED
Parameters Affected	N/A
Trigger Condition(s)	Use of the related function and wakeup from DeepSleep mode.
Scope of Impact	The values before entering DeepSleep are not retained.
Workaround	For PASSx_SARy_CHz_RESULT, any of following: 1) Store the conversion values at another memory location before entering DeepSleep mode 2) Restart the conversion after wakeup from DeepSleep mode For the other registers: Rewrite the register value or read the status flags again after wakeup.
Fix Status	No silicon fix planned. Register TRM was updated.

14. SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally	
Problem Definition	There is possibility of setting the SCBx_INTR_TX.UNDERFLOW bit even if the FIFO is not empty.
Parameters Affected	N/A
Trigger Condition(s)	Using the TX FIFO for SCB when the AHB-Lite interface clock (CLK_GR6) frequency of the AHB bus is greater than 3x the SCB functionality clock (PCLK_SCBx_CLOCK).
Scope of Impact	SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally.
Workaround	Ignore the SCBx_INTR_TX.UNDERFLOW bit if the FIFO is not empty.
Fix Status	No silicon fix planned. Register TRM was updated.

15.Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode	
Problem Definition	The following SROM APIs read data in SFlash from bank#0 (or bank#1 if dual bank mode with mapping B is used). While doing that, they check if active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault based on the FLASHC_FLASH_CTL register settings. Affected SROM APIs: • ReadSWPU • WriteSWPU • GenerateHash • Checksum* • ComputeBasicHash* • CheckFactoryHash • ProgramWorkFlash** *: Do not call it to calculate on the bank where programming/erasing is in progress. **: Do not use it during non-blocking operation.

Parameters Affected	N/A
Trigger Condition(s)	Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).
Scope of Impact	The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).
Workaround	Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).
Fix Status	No silicon fix planned. TRM will be updated.
Impact on Infineon Software	S-LLD, HSM-Perf-Lib: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do any of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty

16.CM0+ operating frequency (CLK_SLOW) should be changed to 80 MHz or lower during eFuse reads

Problem Definition	With FAST_BOOT setting enabled, CLK_SLOW is configured to run at 100 MHz. This means CM0+ and eFuse are clocked at 100 MHz. This setting can cause CM0+ to read wrong data from eFuse during boot. This can affect the behavior of the device (e.g., the device can enter DEAD state from boot). Also, eFuse reads are possible from the user application using system calls. User application cannot configure CLK_SLOW > 80 MHz if system calls target eFuse reads.
Parameters Affected	SID80A: 1700 µs to SID80A_2: 2600 µs SID80B: 2300 µs to SID80B_2: 3800 µs SID81A: 190 µs to SID81A_2: 110 µs SID81B: 5000 µs to SID81B_2: 9800 µs SID81C: 8150 µs to SID81C_2: 17000 µs
Trigger Condition(s)	1) FAST_BOOT enabled (CLK_SLOW = 100 MHz) 2) Use of following system calls when CLK_SLOW > 80 MHz: TransitiontoSecure, TransitiontoRMA, CheckFactoryHash, SiliconID, ReadFuseByte, ReadFuseByteMargin
Scope of Impact	1) System startup time will be longer than existing devices. 2) User application cannot configure CLK_SLOW > 80 MHz when using any of the affected system calls.
Workaround	1) Infineon will change FAST_BOOT setting to support boot only at 50 MHz (i.e. CLK_SLOW = 50 MHz) 2) Change CM0+ operating frequency (CLK_SLOW) to 80 MHz or lower before accessing any of the affected system calls.
Fix Status	Boot operating frequency will be changed from 100 MHz to 50 MHz in factory setting via Manufacturing Test Program. PCN will be released and the datasheet was updated.
Impact on Infineon Software	Impact: No Related modules: MCU Comment: Software in scope does not use functions that trigger the failure. If the MCAL MCU module is used to configure the clocks, CLK_SLOW is displayed as McuSlowClockFrequency.

17.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Problem Definition

During frame reception the Rx Handler accesses the external Message RAM for acceptance filtering (read accesses) and for storing of the accepted messages (write accesses).
The time needed for acceptance filtering and for storing of a received message depends on

- The Host clock frequency
- The worst-case latency of the read and write accesses to the external Message RAM
- The number of configured filter elements
- The workload of the transmit message (Tx) handler in parallel to the receive message (Rx) handler

Received data bytes (DB0..DBm) from the CAN Core are buffered in the cache of the Rx Handler before they are written to the Message RAM (in words of 4 byte). Data words inside the Message RAM are numbered from R2 to Rn (n ≤ 17).

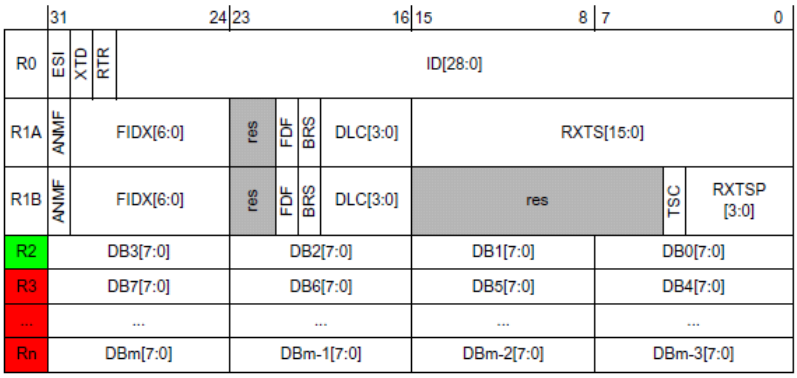


Figure 1 Rx Buffer and FIFO Element

Under the following conditions, a received message has corrupted data while the received message is signaled as valid to the host.
1) The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2) The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5).
3) While condition 1) and 2) apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens.

The data will be corrupted in a way, that in the Message RAM R(i+1) has the same content as Ri.

Despite the corrupted data, the M_TTCAN signals the storage of a valid frame in the Message RAM:
• Rx FIFO: FIFO put index RXFnS.FnPI is updated.
• Dedicated Rx Buffer: New Data flag NDATn.NDxx is set.
• Interrupt flag IR.MRAF is not set.

The issue may occur in the FD Frame Format as well as in the Classic Frame Format.

Figure 2 shows how the available time for acceptance filtering and storage is reduced.

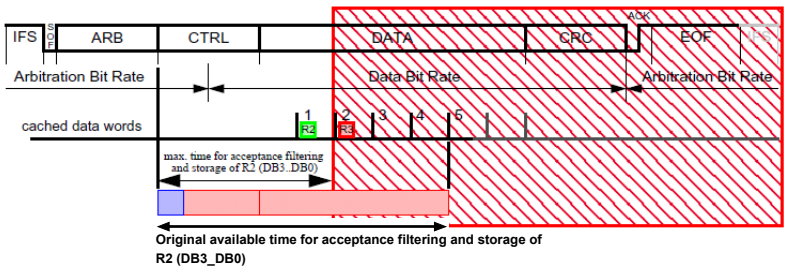


Figure 2 CAN Frame with DLC>4

17.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Table 1 TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5

Number of configured active filter element 11-bit IDs / 29-bit IDs	Number of active CAN channels in an instance	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
32 / 16	2	3.9 MHz	7.1 MHz	13.1 MHz	22.8 MHz	7.7 MHz	14.1 MHz	26.1 MHz	31.5 MHz
	3	5.4 MHz	9.9 MHz	18.3 MHz	31.8 MHz	10.7 MHz	19.7 MHz	36.5 MHz	44.0 MHz
64 / 32	2	7.4 MHz	13.5 MHz	24.9 MHz	43.4 MHz	14.7 MHz	26.9 MHz	49.8 MHz	60.0 MHz
	3	10.3 MHz	18.8 MHz	34.9 MHz	60.7 MHz	20.5 MHz	37.6 MHz	69.7 MHz	84.0 MHz
96 / 48	2	10. 8 MHz	19.9 MHz	36.8 MHz	64.0 MHz	21.6 MHz	39.7 MHz	73.5 MHz	88.6 MHz
	3	15.1 MHz	27.8 MHz	51.5 MHz	89.6 MHz	30.2 MHz	55.6 MHz	102.9 MHz[3]	124.0 MHz[3]
128 / 64	2	14.3 MHz	26.3 MHz	48.6 MHz	84.7 MHz	28.4 MHz	52.5 MHz	97.2 MHz	117.2 MHz[3]
	3	20.0 MHz	36.8 MHz	68.0 MHz	118.5 MHz[3]	40.0 MHz	73.5 MHz	136.0 MHz[3]	164.0 MHz[3]

1.M_TTCAN always starts at filter element #0 and proceeds through the filter list to find a matching element. Acceptance filtering stops at the first matching element and the following filter elements are not evaluated for this message. Therefore, the sequence of configured filter elements has a significant impact on the performance of the filtering process.
2.Acceptance filtering search for 11-bit IDs and 29-bit IDs filter element runs separately; only one configured filter setting should be considered. Searching for one 29-bit filter element requires approximately double cycles for one 11-bit filter element.
3. Frequency is not reachable since the maximum host clock frequency for M_TTCAN in TRAVEO™ T2G is 100 MHz.

Parameters Affected

N/A

Trigger Condition(s)

Under the following conditions a received message has corrupted data while the received message is signaled as valid to the host:
1) The data length code (DLC) of the received message is greater than 4 (DLC > 4)
2) The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where $2 \le i \le 5$).
3) While condition 1) and 2) apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens.

Scope of Impact

The erratum is limited to the case when the Host clock frequency used in the actual device is below the limit shown in **Table 1**.
Corrupted data is written to the Rx FIFO element from the respective dedicated Rx Buffer.
The received frame is nevertheless signaled as valid.

17.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete	
Workaround	Check whether the minimum Host clock frequency (shown in **Table 1**) is below the Host clock frequency used in the actual device. If yes, there is no problem with the selected configuration. If no, use one of the following two workarounds. **1)** Try a different configuration by changing the following parameters until the actual Host clock frequency (CLK_GR5) is above the minimum host frequency shown in **Table 1**: • Increase the CLK_GR5 frequency in the actual device • Reduce the CAN-FD data bit rate • Reduce the number of configured filter elements • Reduce the number of active CAN channels in an instance Also, use DLC ≥ 8 instead of DLCs 5, 6, and 7 in the CAN environment/system, as they place higher demands on the minimum Host clock frequency (the worst case is DLC = 5) or restrict your CAN environment/system to DLC 4. **Note:** While changing the actual host clock frequency, CLK_GR5 must always be equal to or higher than PCLK_-CANFD[x]_CLOCK_CAN[y] for all configurations. **2)** Due to condition 3) listed in **"Trigger Conditions"**, the issue occurs only sporadically. Use an end-to-end (E2E) protection (for example, checksum or CRC covering the data field) and add it to all messages in the CAN system, to detect data corruption in the received frames.
Fix Status	No silicon fix planned. Use workaround.
Impact on Infineon software	Impact: Limitation Related modules: CAN, MCU Comment: Evaluate the impact of the erratum for each CAN instance separately. A CAN instance is the entirety of CanControllers with the same CanControllerInstance value. 1) For the number of active CAN nodes: Use the maximum number of CanController configurations of a CAN instance that can be active (Autosar controller state STARTED or SLEEP) at a time. 2) For the host clock frequency: In McuPeriGroupSettings, locate the setting with McuPeriGroup = MCU_PERI_GROUP5_MMIO5 and take the value from McuPeriGroupClockFrequency. 4) For the number of configured active filter element 11-bit IDs / 29-bit IDs: Use the corresponding values from the "Message RAM (…) linking table" in the generated *Can_PBcfg.h* file. Note that each CanController has its separate table. Take the maximum values. 5) For the arbitration bit rate: Use the maximum CanControllerBaudRate value of all the CanControllers. 6) For the data bit rate: Use the maximum CanControllerFdBaudRate value of all the CanControllers if configured. Otherwise use CanControllerBaudRate.

18.Added definition of minimum input slew rate for SPI-SDR and SPI-DDR of SMIF	
Problem Definition	The minimum input slew rate of SPI-SDR and SPI-DDR mode of the serial memory interface were not defined, which can cause transaction malfunction.
Parameters Affected	Added the following parameters: - SPI-SDR: SID1614 = min 1.03 V/ns - SPI-DDR: SID1714 = min 1.03 V/ns
Trigger Condition(s)	Using SPI-SDR and SPI-DDR mode of the serial memory interface
Scope of Impact	If the minimum input slew rate is not fulfilled, SMIF can cause transaction malfunction.
Workaround	The minimum input slew must be fulfilled for reliable operation.
Fix Status	No silicon fix planned. Datasheet was updated.
Impact on Infineon Software	Impact: No Related modules: None Comment: Software in scope does not support SMIF.

19.Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM

Problem Definition

The existing datasheet shows 'trig=0' in the description for PASS SARx to TCPWMx direct connect triggers one-to-one, which is the incorrect TCPWM input trigger selection (TR_IN_SEL) value. The correct value is '2'. Therefore, the correct description and Table 25-2 in the architecture TRM (chapter 25) are as follows:

Table 25-2 shows how the multiplexer should be handled for the input trigger event generation. The TRAVEO™ T2G Cluster MCU supports the following input triggers:

- Number of specific one-to-one trigger inputs: 1
- Number of general-purpose trigger inputs: 60

Table 2 Handling input trigger multiplexers

Input trigger selection	Input trigger	Input trigger source
0	Constant ‘0’	Constant ‘0’
1	Constant ‘1’	Constant ‘1’
2	HSIOM column ACT#2 or PASS (programmable analog subsystem), through 1:1 trigger mux #2	Refer to the "Alternate function pin assignments" or "Triggers one-to-one" section in the device datasheet
3	tr_all_cnt_in[0]	Refer to the trigger mux block in the device datasheet
:	:	:
62	tr_all_cnt_in[59]	Refer to the trigger mux block in the device datasheet

Parameters Affected	N/A
Trigger Condition(s)	Using the triggers one-to-one for PASS SARx to TCPWMx direct connect
Scope of Impact	The triggers one-to-one for PASS SARx to TCPWMx direct connect cannot work if TCPWM's input trigger selection is not correct
Workaround	Use '2' as TCPWM's input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect
Fix Status	No silicon fix planned. Datasheet was updated. Architecture TRM will be updated.
Impact on Infineon Software	Impact: No Related modules: PWM Comment: The MCAL PWM module does not support one-to-one triggers.

Revision history

Document version	Date of release	Description of changes
**	2021-03-11	New datasheet
*A	2021-05-13	Correction in the package dimensions for 144-LQFP (0.4 mm) Updated **Features list**. Corrected **Power modes** description. Updated **Table 3-3**. Added Trigger MUX diagrams and subsequent tables in **Trigger multiplexer**. Added Peripheral Protection Unit Fixed Structure Pairs Table in **Peripheral protection unit fixed structure pairs**. Updated **Electrical specifications**. Updated SCB/SPI Diagrams. Added “AC Specifications”. Added **Table 27-20**. Updated **Table 29-1** and **Figure 29-3** Added **Table 30-4**.
*B	2021-09-17	Renamed Traveo™ II to TRAVEO™ T2G. Updated **Features list**. Added **Peripheral instance list**. Updated **Pin assignment** diagrams. Updated **Package pin list and alternate functions**. Updated **Alternate function pin assignments**. Updated **Pin function description**. Updated **Electrical specifications**. Updated **Packaging**. Updated **Package outline – 176-LQFP**, **Package outline – 144-LQFP (0.5 mm)**, and **Package outline – 144-LQFP (0.4 mm)** Updated **CAN interface details**, **LIN interface details**
*C	2022-07-15	Migrated to IFX template. Updated **Features**. Updated **CPU subsystem**, **System resources**, **Peripherals**, **I/Os**. Updated **CYT2CL address map**. Updated **Alternate function pin assignments**. Updated **Interrupts and wake-up assignments**. Updated **Faults**. Updated **Electrical specifications**. Updated **Ordering information**. Updated **Errata**.
*D	2022-09-15	Changed datasheet status to Final. Updated **Electrical specifications**.
*E	2022-10-07	Added note 84. Updated **Errata**.
*F	2022-10-20	Updated **Ordering information**.
*G	2023-02-14	Updated **Features list**. Updated **Peripheral I/O map**. Updated **Pin function description**. Updated **Electrical specifications**. Updated **Packaging**.

Document version	Date of release	Description of changes
*H	2023-05-19	Updated **CYT2CL clock diagram**. Updated **Pin function description**. Updated **Electrical specifications**. Updated **Errata**.
*I	2024-03-04	Updated **Blocks and functionality**. Updated **Peripherals**. Updated **Triggers one-to-one**. Updated **Electrical specifications**. Updated **Errata**.

Revision history change log

Rev. *I Section Updates

Section	Change Description	Current Spec	New Spec	Reason for change
2. Blocks and functionality	Block diagram	4x LCD Controller	LCD Controller	Correction
3.3 Peripherals	3.3.14 LCD controller	none	Added "3.3.14 LCD controller" section	Added
20. Triggers one-to-one	MUX Group 3: PASS SARx to TCPWM0 direct connect Input: 0 : Input 63	Description: SAR0 ch#0, range violation to TCPWM0 Group #0 Counter #00 trig=0 : SAR0 ch#31, range violation to TCPWM0 Group #1 Counter #11 trig=0	Description: SAR0 ch#0, range violation to TCPWM0 Group #0 Counter #00 trig=2 : SAR0 ch#31, range violation to TCPWM0 Group #1 Counter #11 trig=2	Correction
27.Electrical Specifications	Table 27-10 Serial communication block (SCB) specifications I2C Interface-Standard-mode	Recommended I/O Configuration: HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0>=0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, , CFG_SLEW_EXT/SLEW<2:0> =0b000, CFG_SLEW_EXT/SLEW<2:0> =0b000, CFG_SLEW_EXT/SLEW<2:0> =0b000 (Note: SID138 is not valid for HSIO_STDLN)	Recommended I/O Configuration:HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0>=0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, , CFG_SLEW_EXT/SLEW<2:0> =0b000 (Note: SID138 is not valid for HSIO_STDLN)	Correction
27.Electrical Specifications	Table 27-10 Serial communication block (SCB) specifications I2C Interface-Fast-Plus mode	Recommended I/O Configuration: : HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 (Note: SID178 is not valid for HSIO_STDLN)	Recommended I/O Configuration: : HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 CFG_SLEW_EXT/SLEW<2:0> = 0b000 (Note: SID178 is not valid for HSIO_STDLN)	Correction
27.Electrical Specifications	Table 27-34 xSPI specifications SPI (JEDEC JESD251 xSPI200)	Recommended I/O configuration: xSPI200: HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0	Recommended I/O configuration: xSPI200: HSIO_STDLN: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b001, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single and dual slave [load ≤ 15 pF])	Correction
32. Errata	CYT2CL Errata Summary [15] Items: Fix Status:	Items: Hardfault may occur when calling ReadSWPU or WriteSWPU while executing EraseSector or ProgramRow in non-blocking mode Fix Status: No silicon fix planned. TRM was updated.	Items: Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode Fix Status: No silicon fix planned. TRM will be updated.	Updated
32. Errata	CYT2CL Errata Summary [17] Items: Errata ID: Fix Status:	none	Items: CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete Errata ID: 209 Fix Status: No silicon fix planned. Use workaround.	Added errata

Rev. *I Section Updates *(continued)*

Section	Change Description	Current Spec	New Spec	Reason for change
32. Errata	CYT2CL Errata Summary [18] Items: Errata ID: Fix Status:	none	Items: Added definition of minimum input slew rate for SPI-SDR and SPI-DDR of SMIF Errata ID: 210 Fix Status: No silicon fix planned. Datasheet was updated.	Added errata
32. Errata	CYT2CL Errata Summary [19] Items: Errata ID: Fix Status:	none	Items: Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM Errata ID: 212 Fix Status: No silicon fix planned. Datasheet was updated. Architecture TRM will be updated.	Added errata
32. Errata	15.Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode Problem Definition: Trigger Condition(s): Scope of Impact: Workaround: Fix Status: Impact on Infineon Software:	Problem Definition: ReadSWPU or WriteSWPU read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation will trigger a bus error which can result in a hardfault occurrence based on FLASHC_FLASH_CTL register settings. Trigger Condition(s): Calling ReadSWPU or WriteSWPU while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Scope of Impact: ReadSWPU or WriteSWPU can't be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Workaround: Do not use ReadSWPU or WriteSWPU while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Fix Status: No silicon fix planned. TRM was updated. Impact on Infineon Software: HSM-Perf-Lib: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not not do any of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty	Problem Definition: The following SROM APIs read data in SFlash from bank#0 (or bank#1 if dual bank mode with mapping B is used). While doing that, they check if active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault based on the FLASHC_FLASH_CTL register settings. Affected SROM APIs: • ReadSWPU • WriteSWPU • GenerateHash • Checksum* • ComputeBasicHash* • CheckFactoryHash • ProgramWorkFlash** *: Do not call it to calculate on the bank where programming/erasing is in progress. **: Do not use it during non-blocking operation. Trigger Condition(s): Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Scope of Impact: The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Workaround: Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used). Fix Status: No silicon fix planned. TRM will be updated. Impact on Infineon Software: S-LLD, HSM-Perf-Lib: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do any of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty	Updated

Rev. *I Section Updates *(continued)*

Section	Change Description	Current Spec	New Spec	Reason for change
32. Errata	17.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete	none	Added "17.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete"	Added errata
32. Errata	18.Added definition of minimum input slew rate for SPI-SDR and SPI-DDR of SMIF	none	Added "18.Added definition of minimum input slew rate for SPI-SDR and SPI-DDR of SMIF"	Added errata
32. Errata	19. Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM	none	Added "19. Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM"	Added errata

Rev. *I Electrical spec updates

Section	Spec ID	Description	Changed Item	Current Spec	New Spec	Reason for Change
27. Electrical Specifications	SID1614	Input slew rate with respect to VIH/VIL	All	none	Spec ID: SID1614 Parameter: IN_SR Description: Input slew rate with respect to VIH/VIL Min: 1.03 V/ns Typ: - Max: - Details/conditions: -	Added Spec
27. Electrical Specifications	SID1714	Input slew rate with respect to VIH/VIL	All	none	Spec ID: SID1714 Parameter: IN_SR Description: Input slew rate with respect to VIH/VIL Min: 1.03 V/ns Typ: - Max: - Details/conditions: -	Added Spec

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