

TRAVEO™ T2G Automotive MCU: TVII-B-E-4M body controller entry registers

Technical reference manual

About this document

Scope and purpose

The TRAVEO™ T2G body controller entry registers TRM provides reference information for registers and contains respective programming details.

Intended audience

This manual is for system designer and programmers who are designing or programming using TVII-B-E-4M parts.

Definitions

Register Permission

The following table lists the register permission based on protection context and privileges.

| Permission | Description |
|-------------------|---|
| READ | User mode = Read access, privilege mode = Read access, Non-secure = yes |
| PRIVILEGE - WRITE | User mode = Read access, privilege mode = Read and Write access, Non-secure = yes |
| NO-ACCESS | User mode = No access, Privilege mode = No access, Non-secure = yes |
| SECURE - READ | User mode = Read access, Privilege mode = Read access, Non-secure = No |
| FULL | Read and Write access in all modes, Non-secure = yes |

Software Access

The following table lists the behavior of registers, on various Software Read/Write Accesses.

| SW Access | HW Access | Software Reads Register | Software Writes Register | Software Description |
|-----------|-----------|-------------------------|-------------------------------------|-------------------------------------|
| R | any | Register contents | Ignored | Software read-only |
| RW | any | Register contents | Register takes data written | Software read and write |
| RW1S | any | Register contents | Every bit is set upon writing 1 | Software read and write 1 to set |
| RW0S | any | Register contents | Every bit is set upon writing 0 | Software read and write 0 to set |
| RW1C | any | Register contents | Every bit is cleared upon writing 1 | Software read and write 1 to clear |
| RW0C | any | Register contents | Every bit is cleared upon writing 0 | Software read and write 0 to clear |
| RW1SC | any | NA | NA | Illegal |
| RW0SC | any | NA | NA | Illegal |
| W | any | Zero | Register takes data written | Software write only |
| W1S | any | Zero | Every bit is set upon writing 1 | Software write 1 to set (no read) |
| W0S | any | Zero | Every bit is set upon writing 0 | Software write 0 to set (no read) |
| W1C | any | Zero | Every bit is cleared upon writing 1 | Software write 1 to clear (no read) |
| W0C | any | Zero | Every bit is cleared upon writing 0 | Software write 0 to clear (no read) |
| W1SC | any | NA | NA | Illegal |
| W0SC | any | NA | NA | Illegal |
| A | any | NA | NA | Illegal |

Hardware Access

The following table lists the behavior of registers, on various Hardware Read/Write Accesses.

| HW Access | SW Access | Hardware Description |
|-----------|-----------|-----------------------------|
| any | R | Hardware read only |
| any | RW | Hardware read and write |
| any | RW1S | Hardware read and set |
| any | RW0S | Hardware read and set |
| any | RW1C | Hardware read and clear |
| any | RW0C | Hardware read and clear |
| any | RW1SC | Hardware read and set/clear |
| any | RW0SC | Hardware read and set/clear |
| any | W | Write access only |
| any | W1S | Hardware set |
| any | W0S | Hardware set |
| any | W1C | Hardware clear |
| any | W0C | Hardware clear |
| any | W1SC | Hardware set/clear |
| any | W0SC | Hardware set/clear |
| R | A | Not supported |
| RW | A | Hardware read and write |
| RW1S | A | Hardware read and set |
| RW0S | A | Hardware read and set |
| RW1C | A | Hardware read and clear |
| RW0C | A | Hardware read and clear |
| RW1SC | A | Not supported |
| RW0SC | A | Not supported |
| W | A | Not supported |
| W1S | A | Not supported |
| W0S | A | Not supported |
| W1C | A | Not supported |
| W0C | A | Not supported |
| W1SC | A | Not supported |
| W0SC | A | Not supported |

Core, Bus and Memory Access

The Cortex-M4 CPUSS uses AHB-Lite also for the system interconnect. Most of the IPs are compliant to the AHB-Lite protocol.

The AHB-Lite protocol is little endian; the least significant byte of a word is mapped onto the word's lowest byte address IPs use a bus data width of 32 bit.

This allows for byte (8-bit), halfword (16-bit) and word (32-bit) transfers. We distinguish two types of transfer types:

- MMIO registers: These registers are typically used for IP control and status information. Unless otherwise noted, transfers to these registers must be 32-bit transfers; any other transfer size generates an AHB-Lite bus error. An IP's MMIO registers do not necessarily fully occupy a consecutive memory region; i.e. holes may be present in the region

- Memory structures: This includes generic memory structures, such as system FLASH, system RAM and system ROM, but also IP specific memory structures. Transfer to these memory structures may be 8-bit, 16-bit or 32-bit transfers; any other transfer size generates an AHB-Lite bus error. A memory structure fully occupies a consecutive memory region; i.e. no holes are present in the memory structure region

A bus slave memory region may contain both MMIO registers and zero or more memory structures. Gaps might exist in the bus slave's memory region, either due to gaps in the MMIO memory region or gaps between the MMIO and memory structure region(s)

Gaps in the address space are reserved. Do not access these gaps, if accessed can result in Hard faults or BUS ERROR depending on which bus segment or a peripheral an address space is allocated to.

List of Partnumber

This TRM is valid for the following part numbers.

| MPN | Package | Code Flash(KB) | Work Flash(KB) | SRAM(KB) |
|------------|----------|----------------|----------------|----------|
| CYT2BL3BAS | 64-LQFP | 4160 | 128 | 512 |
| CYT2BL3BAE | 64-LQFP | 4160 | 128 | 512 |
| CYT2BL3CAS | 64-LQFP | 4160 | 128 | 512 |
| CYT2BL3CAE | 64-LQFP | 4160 | 128 | 512 |
| CYT2BL4BAS | 80-LQFP | 4160 | 128 | 512 |
| CYT2BL4BAE | 80-LQFP | 4160 | 128 | 512 |
| CYT2BL4CAS | 80-LQFP | 4160 | 128 | 512 |
| CYT2BL4CAE | 80-LQFP | 4160 | 128 | 512 |
| CYT2BL5BAS | 100-LQFP | 4160 | 128 | 512 |
| CYT2BL5BAE | 100-LQFP | 4160 | 128 | 512 |
| CYT2BL5CAS | 100-LQFP | 4160 | 128 | 512 |
| CYT2BL5CAE | 100-LQFP | 4160 | 128 | 512 |
| CYT2BL7BAS | 144-LQFP | 4160 | 128 | 512 |
| CYT2BL7BAE | 144-LQFP | 4160 | 128 | 512 |
| CYT2BL7CAS | 144-LQFP | 4160 | 128 | 512 |
| CYT2BL7CAE | 144-LQFP | 4160 | 128 | 512 |
| CYT2BL8BAS | 176-LQFP | 4160 | 128 | 512 |
| CYT2BL8BAE | 176-LQFP | 4160 | 128 | 512 |
| CYT2BL8CAS | 176-LQFP | 4160 | 128 | 512 |
| CYT2BL8CAE | 176-LQFP | 4160 | 128 | 512 |

Memory mapping

| MMIO | IP | Address | Description |
|--------|------------|------------|--|
| MMIO0 | PERI | 0x40000000 | Peripheral interconnect |
| | PERI_MS | 0x40010000 | Peripheral interconnect, master interface |
| MMIO1 | CRYPTO | 0x40100000 | Cryptography component |
| MMIO2 | CPUSS | 0x40200000 | CPU subsystem (CPUSS) |
| | FAULT | 0x40210000 | Fault structures |
| | IPC | 0x40220000 | IPC |
| | PROT | 0x40230000 | Protection |
| | FLASHC | 0x40240000 | Flash controller |
| | SRSS | 0x40260000 | SRSS Core Registers (ver3) |
| | BACKUP | 0x40270000 | SRSS Backup Domain (ver3) |
| | DW 0 | 0x40280000 | Datawire Controller |
| | DW 1 | 0x40290000 | Datawire Controller |
| | DMAC | 0x402a0000 | DMAC |
| | EFUSE | 0x402c0000 | EFUSE MXS40 registers |
| | EFUSE_DATA | 0x402c0800 | eFUSE memory |
| MMIO3 | HSIOM | 0x40300000 | High Speed IO Matrix (HSIOM) |
| | GPIO | 0x40310000 | GPIO port control/configuration |
| | SMARTIO | 0x40320000 | Programmable IO configuration |
| | TCPWM | 0x40380000 | Timer/Counter/PWM |
| | EVTGEN | 0x403f0000 | Event generator |
| MMIO5 | LIN | 0x40500000 | LIN |
| | CXPI | 0x40510000 | CXPI |
| | CANFD 0 | 0x40520000 | CAN Controller |
| | CANFD 1 | 0x40540000 | CAN Controller |
| MMIO6 | SCB 0 | 0x40600000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 1 | 0x40610000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 2 | 0x40620000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 3 | 0x40630000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 4 | 0x40640000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 5 | 0x40650000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 6 | 0x40660000 | Serial Communications Block (SPI/UART/I2C) |
| | SCB 7 | 0x40670000 | Serial Communications Block (SPI/UART/I2C) |
| MMIO9 | PASS | 0x40900000 | Programmable Analog Subsystem for S40E |
| SFLASH | SFLASH | 0x17000000 | FLASH Supervisory Region |
| SYSTEM | CM0P | 0xe0000000 | Cortex-M0+ specific registers |
| | CM4 | 0xe0000000 | Cortex-M4 specific registers |
| | SYSAP | 0xe0000000 | System debug Access Port (SYSAP) registers |

1 BACKUP

Description SRSS Backup Domain (ver3)
Base Address 0x40270000
Size 0x10000
Slave Num MMIO2 - 6

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|---|
| BACKUP_CTL | 0x40270000 | FULL | Control Note: VDDBAK_CTL VBACKUP_MEAS EN_CHARGE_KEY are not available for this register |
| BACKUP_RTC_RW | 0x40270008 | FULL | RTC Read Write register |
| BACKUP_CAL_CTL | 0x4027000C | FULL | Oscillator calibration for absolute frequency |
| BACKUP_STATUS | 0x40270010 | FULL | Status |
| BACKUP_RTC_TIME | 0x40270014 | FULL | Calendar Seconds, Minutes, Hours, Day of Week |
| BACKUP_RTC_DATE | 0x40270018 | FULL | Calendar Day of Month, Month, Year |
| BACKUP_ALM1_TIME | 0x4027001C | FULL | Alarm 1 Seconds, Minute, Hours, Day of Week |
| BACKUP_ALM1_DATE | 0x40270020 | FULL | Alarm 1 Day of Month, Month |
| BACKUP_ALM2_TIME | 0x40270024 | FULL | Alarm 2 Seconds, Minute, Hours, Day of Week |
| BACKUP_ALM2_DATE | 0x40270028 | FULL | Alarm 2 Day of Month, Month |
| BACKUP_INTR | 0x4027002C | FULL | Interrupt request register |
| BACKUP_INTR_SET | 0x40270030 | FULL | Interrupt set request register |
| BACKUP_INTR_MASK | 0x40270034 | FULL | Interrupt mask register |
| BACKUP_INTR_MASKED | 0x40270038 | FULL | Interrupt masked request register |
| BACKUP_RESET | 0x40270048 | FULL | Backup reset register |
| BACKUP_BREG0 | 0x40271000 | FULL | Backup register region |
| BACKUP_BREG1 | 0x40271004 | FULL | Backup register region |
| BACKUP_BREG2 | 0x40271008 | FULL | Backup register region |
| BACKUP_BREG3 | 0x4027100C | FULL | Backup register region |

1.1 Register Details

1.1.1 BACKUP_CTL

Description: Control
Address: 0x40270000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------|------------|---|---|
| Name | None [7:4] | | | | WCO_EN [3:3] | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|-------------------|----|--------------|----|---------------|---|
| Name | None [15:14] | | PRESCALER [13:12] | | None [11:10] | | CLK_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----------------------|--------------------|----|--------------------|
| Name | None [23:20] | | | | VBACKUP_MEAS [19:19] | VDDBAK_CTL [18:17] | | WCO_BYPASS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------------|----|----|----|----|----|----|----|
| Name | EN_CHARGE_KEY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|---|
| 3 | WCO_EN | RW | A | 0 | Watch-crystal oscillator (WCO) enable. If there is a write in progress when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_bak, like for example RTC or WDTs. Follow the procedure in BACKUP_RTC_RW to access this bit. |
| 8:9 | CLK_SEL | RW | A | 0 | Clock select for RTC clock |
| | WCO | | | 0 | Watch-crystal oscillator input, available in Active, DeepSleep, Hibernate, and XRES. |
| | ALTBK | | | 1 | This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is only available in Active and DeepSleep power modes. Note that LFCLK clock glitches can propagate into the backup logic when the clock is stopped. For this reason, if the WCO or ILO is intended as the clock source then choose it directly instead of routing through LFCLK. |
| | ILO | | | 2 | Internal Low frequency Oscillator, available in Active, DeepSleep, Hibernate, and XRES. For Hibernate operation CLK_ILO_CONFIG. ILO_BACKUP must be set. If there are multiple ILO, this is ILO0. |
| | LPECO_PRESCALER | | | 3 | Low-power external crystal oscillator prescaler output, available in Active, DeepSleep, Hibernate, and XRES. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|---|
| 12:13 | PRESCALER | RW | A | 0 | Prescaler for real time clock used when WCO_BYPASS=1 and CLK_SEL = WCO. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO output pin. Do not connect WCO input pin. 1: reserved 2: reserved 3: reserved |
| 16 | WCO_BYPASS | RW | A | 0 | Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins. 1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. |
| 17:18 | VDDBAK_CTL | RW | A | 0 | Controls the behavior of the switch that generates vddbak from vbackup or vddd. 0: automatically select vddd if its brownout detector says it is valid. If the brownout says its not valid, then use vmax which is the highest of vddd or vbackup. 1,2,3: force vddbak and vmax to select vbackup, regardless of its voltage. |
| 19 | VBACKUP_MEAS | RW | A | 0 | Connect vbackup supply to the vbackup_meas output for measurement by an ADC attached to amuxbusa_adft_vddd. The vbackup_meas signal is scaled to 10 percent of vbackup, so it is within the supply range of the ADC. |
| 24:31 | EN_CHARGE_KEY | RW | A | 0 | When set to 3C, the supercap charger circuit is enabled. Any other code disables the supercap charger. THIS CHARGING CIRCUIT IS FOR A SUPERCAP ONLY AND CANNOT SAFELY CHARGE A BATTERY. DO NOT WRITE THIS KEY WHEN VBACKUP IS CONNECTED TO A BATTERY. |

1.1.2 BACKUP_RTC_RW

Description: RTC Read Write register
Address: 0x40270008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain but reset in DEEPSLEEP.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-------------|------------|
| Name | None [7:2] | | | | | | WRITE [1:1] | READ [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | READ | RW | A | 0 | Read bit When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running. Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. |
| 1 | WRITE | RW | A | 0 | Write bit Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set. The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers. Only user RTC registers that were written to will get copied, others will not be affected. When the SECONDS field is updated then TICKS will also be reset (WDT is not affected). When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost. Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. |

1.1.3 BACKUP_CAL_CTL

Description: Oscillator calibration for absolute frequency
Address: 0x4027000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. Calibration only works when the PRESCALER is set to 32768. Writes are ignored unless Write bit is set
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|-------------------|-----------------|---|---|---|---|---|
| Name | None [7:7] | CALIB_SIG N [6:6] | CALIB_VAL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|-----------------|----|--------------|----|----|----|
| Name | CAL_OUT [31:31] | None [30:30] | CAL_SEL [29:28] | | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|--|
| 0:5 | CALIB_VAL | RW | A | 0 | Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/(60*60*32,768)). Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field) Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments. |
| 6 | CALIB_SIGN | RW | A | 0 | Calibration sign: 0= Negative sign: remove pulses (it takes more clock ticks to count one second) 1= Positive sign: add pulses (it takes less clock ticks to count one second) |
| 28:29 | CAL_SEL | RW | A | 0 | Select calibration wave output signal |
| | CAL512 | | | 0 | 512Hz wave, not affected by calibration setting (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) |
| | RESERVED | | | 1 | N/A |
| | CAL2 | | | 2 | 2Hz wave, includes the effect of the calibration setting, (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) |
| | CAL1 | | | 3 | 1Hz wave, includes the effect of the calibration setting (supported for all input clocks) |
| 31 | CAL_OUT | RW | A | 0 | Output enable for wave signal for calibration and allow CALIB_VAL to be written. |

1.1.4 BACKUP_STATUS

Description: Status
Address: 0x40270010
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--------------|------------|----------------|
| Name | None [7:3] | | | | | WCO_OK [2:2] | None [1:1] | RTC_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0 | RTC_BUSY | R | W | 0 | Pending RTC write |
| 2 | WCO_OK | R | W | 0 | Indicates that output has transitioned. |

1.1.5 BACKUP_RTC_TIME

Description: Calendar Seconds, Minutes, Hours, Day of Week

Address: 0x40270014

Offset: 0x14

Retention: Retained

IsDeepSleep: No

Comment: These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit is set and the values are copied from the RTC into these registers..

Default: 0x1000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---------------|---|---|---|---|---|
| Name | None [7:6] | | RTC_SEC [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----------------|----|----|----|---|---|
| Name | None [15:14] | | RTC_MIN [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------------|--------------|------------------|----|----|----|----|
| Name | None [23:23] | CTRL_12HR [22:22] | None [21:21] | RTC_HOUR [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|-----------------|----|----|
| Name | None [31:27] | | | | | RTC_DAY [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 0:5 | RTC_SEC | RW | A | 0 | Calendar seconds, 0-59 |
| 8:13 | RTC_MIN | RW | A | 0 | Calendar minutes, 0-59 |
| 16:20 | RTC_HOUR | RW | A | 0 | Calendar hours, value depending on 12/24HR mode 0=24HR: [20:16]=0-23 1=12HR: [20]:0=AM, 1=PM, [19:16]=1-12 |
| 22 | CTRL_12HR | RW | A | 0 | Select 12/24HR mode: 1=12HR, 0=24HR |
| 24:26 | RTC_DAY | RW | A | 1 | Calendar Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended |

1.1.6 BACKUP_RTC_DATE

Description: Calendar Day of Month, Month, Year
Address: 0x40270018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit is set and the values are copied from the RTC into these registers..
Default: 0x101

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|---|---|---|---|
| Name | None [7:5] | | | RTC_DATE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----------------|----|---|---|
| Name | None [15:12] | | | | RTC_MON [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|------------------|----|----|----|----|----|----|
| Name | None [23:23] | RTC_YEAR [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|---|
| 0:4 | RTC_DATE | RW | A | 1 | Calendar Day of the Month, 1-31 Automatic Leap Year Correction |
| 8:11 | RTC_MON | RW | A | 1 | Calendar Month, 1-12 |
| 16:22 | RTC_YEAR | RW | A | 0 | Calendar year, 0-99 |

1.1.7 BACKUP_ALM1_TIME

Description: Alarm 1 Seconds, Minute, Hours, Day of Week
Address: 0x4027001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. This register is only used when BACKUP_ALM1_DATE.ALM_EN=1. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit is set and the values are copied from the RTC into these registers..
Default: 0x1000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|------------|---------------|---|---|---|---|---|
| Name | ALM_SEC_EN [7:7] | None [6:6] | ALM_SEC [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|--------------|----------------|----|----|----|---|---|
| Name | ALM_MIN_EN [15:15] | None [14:14] | ALM_MIN [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|--------------|----|------------------|----|----|----|----|
| Name | ALM_HOUR_EN [23:23] | None [22:21] | | ALM_HOUR [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|--------------|----|----|----|-----------------|----|----|
| Name | ALM_DAY_EN [31:31] | None [30:27] | | | | ALM_DAY [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 0:5 | ALM_SEC | RW | A | 0 | Alarm seconds, 0-59 |
| 7 | ALM_SEC_EN | RW | A | 0 | Alarm second enable: 0=ignore, 1=match |
| 8:13 | ALM_MIN | RW | A | 0 | Alarm minutes, 0-59 |
| 15 | ALM_MIN_EN | RW | A | 0 | Alarm minutes enable: 0=ignore, 1=match |
| 16:20 | ALM_HOUR | RW | A | 0 | Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 |
| 23 | ALM_HOUR_EN | RW | A | 0 | Alarm hour enable: 0=ignore, 1=match |
| 24:26 | ALM_DAY | RW | A | 1 | Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended |
| 31 | ALM_DAY_EN | RW | A | 0 | Alarm Day of the Week enable: 0=ignore, 1=match |

1.1.8 BACKUP_ALM1_DATE

Description: Alarm 1 Day of Month, Month

Address: 0x40270020

Offset: 0x20

Retention: Retained

IsDeepSleep: No

Comment: These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit is set and the values are copied from the RTC into these registers..

Default: 0x101

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|------------|---|----------------|---|---|---|---|
| Name | ALM_DATE_EN [7:7] | None [6:5] | | ALM_DATE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|--------------|----|----|----------------|----|---|---|
| Name | ALM_MON_EN [15:15] | None [14:12] | | | ALM_MON [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ALM_EN [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:4 | ALM_DATE | RW | A | 1 | Alarm Day of the Month, 1-31 Leap Year corrected |
| 7 | ALM_DATE_EN | RW | A | 0 | Alarm Day of the Month enable: 0=ignore, 1=match |
| 8:11 | ALM_MON | RW | A | 1 | Alarm Month, 1-12 |
| 15 | ALM_MON_EN | RW | A | 0 | Alarm Month enable: 0=ignore, 1=match |
| 31 | ALM_EN | RW | A | 0 | Master enable for alarm 1. 0: Alarm 1 is disabled. Fields for date and time are ignored. 1: Alarm 1 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. |

1.1.9 BACKUP_ALM2_TIME

Description: Alarm 2 Seconds, Minute, Hours, Day of Week
Address: 0x40270024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. This register is only used when BACKUP_ALM2_DATE.ALM_EN=1. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit is set and the values are copied from the RTC into these registers..
Default: 0x1000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|------------|---------------|---|---|---|---|---|
| Name | ALM_SEC_EN [7:7] | None [6:6] | ALM_SEC [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|--------------|----------------|----|----|----|---|---|
| Name | ALM_MIN_EN [15:15] | None [14:14] | ALM_MIN [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|--------------|----|------------------|----|----|----|----|
| Name | ALM_HOUR_EN [23:23] | None [22:21] | | ALM_HOUR [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|--------------|----|----|----|-----------------|----|----|
| Name | ALM_DAY_EN [31:31] | None [30:27] | | | | ALM_DAY [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 0:5 | ALM_SEC | RW | A | 0 | Alarm seconds, 0-59 |
| 7 | ALM_SEC_EN | RW | A | 0 | Alarm second enable: 0=ignore, 1=match |
| 8:13 | ALM_MIN | RW | A | 0 | Alarm minutes, 0-59 |
| 15 | ALM_MIN_EN | RW | A | 0 | Alarm minutes enable: 0=ignore, 1=match |
| 16:20 | ALM_HOUR | RW | A | 0 | Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 |
| 23 | ALM_HOUR_EN | RW | A | 0 | Alarm hour enable: 0=ignore, 1=match |
| 24:26 | ALM_DAY | RW | A | 1 | Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended |
| 31 | ALM_DAY_EN | RW | A | 0 | Alarm Day of the Week enable: 0=ignore, 1=match |

1.1.10 BACKUP_ALM2_DATE

Description: Alarm 2 Day of Month, Month

Address: 0x40270028

Offset: 0x28

Retention: Retained

IsDeepSleep: No

Comment: These bits are in vddbak domain. Writes are ignored unless Write bit is set. After reset, these will read as zero until the read bit is set and the values are copied from the RTC into these registers..

Default: 0x101

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|------------|---|----------------|---|---|---|---|
| Name | ALM_DATE_EN [7:7] | None [6:5] | | ALM_DATE [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|--------------|----|----|----------------|----|---|---|
| Name | ALM_MON_EN [15:15] | None [14:12] | | | ALM_MON [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ALM_EN [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:4 | ALM_DATE | RW | A | 1 | Alarm Day of the Month, 1-31 Leap Year corrected |
| 7 | ALM_DATE_EN | RW | A | 0 | Alarm Day of the Month enable: 0=ignore, 1=match |
| 8:11 | ALM_MON | RW | A | 1 | Alarm Month, 1-12 |
| 15 | ALM_MON_EN | RW | A | 0 | Alarm Month enable: 0=ignore, 1=match |
| 31 | ALM_EN | RW | A | 0 | Master enable for alarm 2. 0: Alarm 2 is disabled. Fields for date and time are ignored. 1: Alarm 2 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. |

1.1.11 BACKUP_INTR

Description: Interrupt request register
Address: 0x4027002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. Interrupt signal from SRSS includes this register and also BACKUP_INTR, if present.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---------------|--------------|--------------|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|------|-----------------|----------------------------|
| 0 | ALARM1 | RW1C | RW1S | 0 | Alarm 1 Interrupt |
| 1 | ALARM2 | RW1C | RW1S | 0 | Alarm 2 Interrupt |
| 2 | CENTURY | RW1C | RW1S | 0 | Century overflow interrupt |

1.1.12 BACKUP_INTR_SET

Description: Interrupt set request register
Address: 0x40270030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. Allows setting interrupts for firmware testing.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---------------|--------------|--------------|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|----|-----------------|--|
| 0 | ALARM1 | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | ALARM2 | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | CENTURY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

1.1.13 BACKUP_INTR_MASK

Description: Interrupt mask register
Address: 0x40270034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. When Mask bit is set the interrupt is enabled.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---------------|--------------|--------------|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | ALARM1 | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | ALARM2 | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | CENTURY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

1.1.14 BACKUP_INTR_MASKED

Description: Interrupt masked request register

Address: 0x40270038

Offset: 0x38

Retention: Retained

IsDeepSleep: No

Comment: These bits are in vddbak domain. When read, this register reflects a bitwise and between the interrupt request and mask registers.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---------------|--------------|--------------|
| Name | None [7:3] | | | | | CENTURY [2:2] | ALARM2 [1:1] | ALARM1 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | ALARM1 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 1 | ALARM2 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 2 | CENTURY | R | RW | 0 | Logical and of corresponding request and mask bits. |

1.1.15 BACKUP_RESET

Description: Backup reset register
Address: 0x40270048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: This register is used to reset the backup domain from firmware.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|----|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | RESET [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|--|
| 31 | RESET | RW1S | A | 0 | Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. |

1.1.16 BACKUP_BREG

Description: Backup register region
Address: 0x40271000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment: These bits are in vddbak domain. Backup memory
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | BREG [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | BREG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | BREG [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | BREG [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | BREG | RW | A | 0 | Backup memory that contains application-specific data. Memory is retained on vbackup supply. |

2 CANFD

2.1 CANFD 0

| | |
|---------------------|----------------|
| Description | CAN Controller |
| Base Address | 0x40520000 |
| Size | 0x20000 |
| Slave Num | MMIO5 - 2 |

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|--|
| CANFD0_CTL | 0x40521000 | FULL | Global CAN control register |
| CANFD0_STATUS | 0x40521004 | FULL | Global CAN status register |
| CANFD0_INTR0_CAUSE | 0x40521010 | FULL | Consolidated interrupt0 cause register |
| CANFD0_INTR1_CAUSE | 0x40521014 | FULL | Consolidated interrupt1 cause register |
| CANFD0_TS_CTL | 0x40521020 | FULL | Time Stamp control register |
| CANFD0_TS_CNT | 0x40521024 | FULL | Time Stamp counter value |
| CANFD0_ECC_CTL | 0x40521080 | FULL | ECC control |
| CANFD0_ECC_ERR_INJ | 0x40521084 | FULL | ECC error injection |

2.1.1 CH 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD0_CH0_RXFTOP_CTL | 0x40520180 | FULL | Receive FIFO Top control |
| CANFD0_CH0_RXFTOP0_STAT | 0x405201A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH0_RXFTOP0_DATA | 0x405201A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH0_RXFTOP1_STAT | 0x405201B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH0_RXFTOP1_DATA | 0x405201B8 | FULL | Receive FIFO 1 Top Data |

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| Register Name | Address | Permission | Description |
|------------------|------------|------------|---|
| CANFD0_CH0_CREL | 0x40520000 | FULL | Core Release Register |
| CANFD0_CH0_ENDN | 0x40520004 | FULL | Endian Register |
| CANFD0_CH0_DBTP | 0x4052000C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH0_TEST | 0x40520010 | FULL | Test Register |
| CANFD0_CH0_RWD | 0x40520014 | FULL | RAM Watchdog |
| CANFD0_CH0_CCCR | 0x40520018 | FULL | CC Control Register |
| CANFD0_CH0_NBTP | 0x4052001C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH0_TSCC | 0x40520020 | FULL | Timestamp Counter Configuration |
| CANFD0_CH0_TSCV | 0x40520024 | FULL | Timestamp Counter Value |
| CANFD0_CH0_TOCC | 0x40520028 | FULL | Timeout Counter Configuration |
| CANFD0_CH0_TOCV | 0x4052002C | FULL | Timeout Counter Value |
| CANFD0_CH0_ECR | 0x40520040 | FULL | Error Counter Register |
| CANFD0_CH0_PSR | 0x40520044 | FULL | Protocol Status Register |
| CANFD0_CH0_TDCR | 0x40520048 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH0_IR | 0x40520050 | FULL | Interrupt Register |
| CANFD0_CH0_IE | 0x40520054 | FULL | Interrupt Enable |
| CANFD0_CH0_ILS | 0x40520058 | FULL | Interrupt Line Select |
| CANFD0_CH0_ILE | 0x4052005C | FULL | Interrupt Line Enable |
| CANFD0_CH0_GFC | 0x40520080 | FULL | Global Filter Configuration |
| CANFD0_CH0_SIDFC | 0x40520084 | FULL | Standard ID Filter Configuration |
| CANFD0_CH0_XIDFC | 0x40520088 | FULL | Extended ID Filter Configuration |
| CANFD0_CH0_XIDAM | 0x40520090 | FULL | Extended ID AND Mask |
| CANFD0_CH0_HPMS | 0x40520094 | FULL | High Priority Message Status |
| CANFD0_CH0_NDAT1 | 0x40520098 | FULL | New Data 1 |
| CANFD0_CH0_NDAT2 | 0x4052009C | FULL | New Data 2 |
| CANFD0_CH0_RXF0C | 0x405200A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH0_RXF0S | 0x405200A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH0_RXF0A | 0x405200A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH0_RXBC | 0x405200AC | FULL | Rx Buffer Configuration |
| CANFD0_CH0_RXF1C | 0x405200B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH0_RXF1S | 0x405200B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH0_RXF1A | 0x405200B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH0_RXESC | 0x405200BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH0_TXBC | 0x405200C0 | FULL | Tx Buffer Configuration |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD0_CH0_TXFQS | 0x405200C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH0_TXESC | 0x405200C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH0_TXBRP | 0x405200CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH0_TXBAR | 0x405200D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH0_TXBCR | 0x405200D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH0_TXBTO | 0x405200D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH0_TXBCF | 0x405200DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH0_TXBTIE | 0x405200E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH0_TXBCIE | 0x405200E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH0_TXEFC | 0x405200F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH0_TXEFS | 0x405200F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH0_TXEFA | 0x405200F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH0_TTMC | 0x40520100 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH0_TTRMC | 0x40520104 | FULL | TT Reference Message Configuration |
| CANFD0_CH0_TTOCF | 0x40520108 | FULL | TT Operation Configuration |
| CANFD0_CH0_TTMLM | 0x4052010C | FULL | TT Matrix Limits |
| CANFD0_CH0_TURCF | 0x40520110 | FULL | TUR Configuration |
| CANFD0_CH0_TTOCN | 0x40520114 | FULL | TT Operation Control |
| CANFD0_CH0_TTGP | 0x40520118 | FULL | TT Global Time Preset |
| CANFD0_CH0_TTTMK | 0x4052011C | FULL | TT Time Mark |
| CANFD0_CH0_TTIR | 0x40520120 | FULL | TT Interrupt Register |
| CANFD0_CH0_TTIE | 0x40520124 | FULL | TT Interrupt Enable |
| CANFD0_CH0_TTILS | 0x40520128 | FULL | TT Interrupt Line Select |
| CANFD0_CH0_TTOST | 0x4052012C | FULL | TT Operation Status |
| CANFD0_CH0_TURNA | 0x40520130 | FULL | TUR Numerator Actual |
| CANFD0_CH0_TTLGT | 0x40520134 | FULL | TT Local & Global Time |
| CANFD0_CH0_TTCTC | 0x40520138 | FULL | TT Cycle Time & Count |
| CANFD0_CH0_TTCPT | 0x4052013C | FULL | TT Capture Time |
| CANFD0_CH0_TTCSM | 0x40520140 | FULL | TT Cycle Sync Mark |

2.1.2 CH 1

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD0_CH1_RXFTOP_CTL | 0x40520380 | FULL | Receive FIFO Top control |
| CANFD0_CH1_RXFTOP0_STAT | 0x405203A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH1_RXFTOP0_DATA | 0x405203A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH1_RXFTOP1_STAT | 0x405203B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH1_RXFTOP1_DATA | 0x405203B8 | FULL | Receive FIFO 1 Top Data |

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| Register Name | Address | Permission | Description |
|------------------|------------|------------|---|
| CANFD0_CH1_CREL | 0x40520200 | FULL | Core Release Register |
| CANFD0_CH1_ENDN | 0x40520204 | FULL | Endian Register |
| CANFD0_CH1_DBTP | 0x4052020C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH1_TEST | 0x40520210 | FULL | Test Register |
| CANFD0_CH1_RWD | 0x40520214 | FULL | RAM Watchdog |
| CANFD0_CH1_CCCR | 0x40520218 | FULL | CC Control Register |
| CANFD0_CH1_NBTP | 0x4052021C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH1_TSCC | 0x40520220 | FULL | Timestamp Counter Configuration |
| CANFD0_CH1_TSCV | 0x40520224 | FULL | Timestamp Counter Value |
| CANFD0_CH1_TOCC | 0x40520228 | FULL | Timeout Counter Configuration |
| CANFD0_CH1_TOCV | 0x4052022C | FULL | Timeout Counter Value |
| CANFD0_CH1_ECR | 0x40520240 | FULL | Error Counter Register |
| CANFD0_CH1_PSR | 0x40520244 | FULL | Protocol Status Register |
| CANFD0_CH1_TDCR | 0x40520248 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH1_IR | 0x40520250 | FULL | Interrupt Register |
| CANFD0_CH1_IE | 0x40520254 | FULL | Interrupt Enable |
| CANFD0_CH1_ILS | 0x40520258 | FULL | Interrupt Line Select |
| CANFD0_CH1_ILE | 0x4052025C | FULL | Interrupt Line Enable |
| CANFD0_CH1_GFC | 0x40520280 | FULL | Global Filter Configuration |
| CANFD0_CH1_SIDFC | 0x40520284 | FULL | Standard ID Filter Configuration |
| CANFD0_CH1_XIDFC | 0x40520288 | FULL | Extended ID Filter Configuration |
| CANFD0_CH1_XIDAM | 0x40520290 | FULL | Extended ID AND Mask |
| CANFD0_CH1_HPMS | 0x40520294 | FULL | High Priority Message Status |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD0_CH1_NDAT1 | 0x40520298 | FULL | New Data 1 |
| CANFD0_CH1_NDAT2 | 0x4052029C | FULL | New Data 2 |
| CANFD0_CH1_RXF0C | 0x405202A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH1_RXF0S | 0x405202A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH1_RXF0A | 0x405202A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH1_RXBC | 0x405202AC | FULL | Rx Buffer Configuration |
| CANFD0_CH1_RXF1C | 0x405202B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH1_RXF1S | 0x405202B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH1_RXF1A | 0x405202B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH1_RXESC | 0x405202BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH1_TXBC | 0x405202C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH1_TXFQS | 0x405202C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH1_TXESC | 0x405202C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH1_TXBRP | 0x405202CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH1_TXBAR | 0x405202D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH1_TXBCR | 0x405202D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH1_TXBTO | 0x405202D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH1_TXBCF | 0x405202DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH1_TXBTIE | 0x405202E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH1_TXBCIE | 0x405202E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH1_TXEFC | 0x405202F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH1_TXEFS | 0x405202F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH1_TXEFA | 0x405202F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH1_TTTMC | 0x40520300 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH1_TTRMC | 0x40520304 | FULL | TT Reference Message Configuration |
| CANFD0_CH1_TTOCF | 0x40520308 | FULL | TT Operation Configuration |
| CANFD0_CH1_TTMLM | 0x4052030C | FULL | TT Matrix Limits |
| CANFD0_CH1_TURCF | 0x40520310 | FULL | TUR Configuration |
| CANFD0_CH1_TTOCN | 0x40520314 | FULL | TT Operation Control |
| CANFD0_CH1_TTGRP | 0x40520318 | FULL | TT Global Time Preset |
| CANFD0_CH1_TTTMK | 0x4052031C | FULL | TT Time Mark |
| CANFD0_CH1_TTIR | 0x40520320 | FULL | TT Interrupt Register |
| CANFD0_CH1_TTIE | 0x40520324 | FULL | TT Interrupt Enable |
| CANFD0_CH1_TTILS | 0x40520328 | FULL | TT Interrupt Line Select |
| CANFD0_CH1_TTOST | 0x4052032C | FULL | TT Operation Status |
| CANFD0_CH1_TURNA | 0x40520330 | FULL | TUR Numerator Actual |
| CANFD0_CH1_TLGT | 0x40520334 | FULL | TT Local & Global Time |
| CANFD0_CH1_TTCTC | 0x40520338 | FULL | TT Cycle Time & Count |
| CANFD0_CH1_TTCPT | 0x4052033C | FULL | TT Capture Time |
| CANFD0_CH1_TTCSM | 0x40520340 | FULL | TT Cycle Sync Mark |

2.1.3 CH 2

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD0_CH2_RXFTOP_CTL | 0x40520580 | FULL | Receive FIFO Top control |
| CANFD0_CH2_RXFTOP0_STAT | 0x405205A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH2_RXFTOP0_DATA | 0x405205A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH2_RXFTOP1_STAT | 0x405205B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH2_RXFTOP1_DATA | 0x405205B8 | FULL | Receive FIFO 1 Top Data |

2.1.3.1 M_TTCAN

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---|
| CANFD0_CH2_CREL | 0x40520400 | FULL | Core Release Register |
| CANFD0_CH2_ENDN | 0x40520404 | FULL | Endian Register |
| CANFD0_CH2_DBTP | 0x4052040C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH2_TEST | 0x40520410 | FULL | Test Register |
| CANFD0_CH2_RWD | 0x40520414 | FULL | RAM Watchdog |
| CANFD0_CH2_CCCR | 0x40520418 | FULL | CC Control Register |
| CANFD0_CH2_NBTP | 0x4052041C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH2_TSCC | 0x40520420 | FULL | Timestamp Counter Configuration |
| CANFD0_CH2_TSCV | 0x40520424 | FULL | Timestamp Counter Value |
| CANFD0_CH2_TOCC | 0x40520428 | FULL | Timeout Counter Configuration |
| CANFD0_CH2_TOCV | 0x4052042C | FULL | Timeout Counter Value |
| CANFD0_CH2_ECR | 0x40520440 | FULL | Error Counter Register |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD0_CH2_PSR | 0x40520444 | FULL | Protocol Status Register |
| CANFD0_CH2_TDCR | 0x40520448 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH2_IR | 0x40520450 | FULL | Interrupt Register |
| CANFD0_CH2_IE | 0x40520454 | FULL | Interrupt Enable |
| CANFD0_CH2_ILS | 0x40520458 | FULL | Interrupt Line Select |
| CANFD0_CH2_ILE | 0x4052045C | FULL | Interrupt Line Enable |
| CANFD0_CH2_GFC | 0x40520480 | FULL | Global Filter Configuration |
| CANFD0_CH2_SIDFC | 0x40520484 | FULL | Standard ID Filter Configuration |
| CANFD0_CH2_XIDFC | 0x40520488 | FULL | Extended ID Filter Configuration |
| CANFD0_CH2_XIDAM | 0x40520490 | FULL | Extended ID AND Mask |
| CANFD0_CH2_HPMS | 0x40520494 | FULL | High Priority Message Status |
| CANFD0_CH2_NDAT1 | 0x40520498 | FULL | New Data 1 |
| CANFD0_CH2_NDAT2 | 0x4052049C | FULL | New Data 2 |
| CANFD0_CH2_RXF0C | 0x405204A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH2_RXF0S | 0x405204A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH2_RXF0A | 0x405204A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH2_RXBC | 0x405204AC | FULL | Rx Buffer Configuration |
| CANFD0_CH2_RXF1C | 0x405204B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH2_RXF1S | 0x405204B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH2_RXF1A | 0x405204B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH2_RXESC | 0x405204BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH2_TXBC | 0x405204C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH2_TXFQS | 0x405204C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH2_TXESC | 0x405204C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH2_TXBRP | 0x405204CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH2_TXBAR | 0x405204D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH2_TXBCR | 0x405204D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH2_TXBTO | 0x405204D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH2_TXBCF | 0x405204DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH2_TXBTIE | 0x405204E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH2_TXBCIE | 0x405204E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH2_TXEFC | 0x405204F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH2_TXEFS | 0x405204F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH2_TXEFA | 0x405204F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH2_TTTMC | 0x40520500 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH2_TTRMC | 0x40520504 | FULL | TT Reference Message Configuration |
| CANFD0_CH2_TTOCF | 0x40520508 | FULL | TT Operation Configuration |
| CANFD0_CH2_TTMLM | 0x4052050C | FULL | TT Matrix Limits |
| CANFD0_CH2_TURCF | 0x40520510 | FULL | TUR Configuration |
| CANFD0_CH2_TTOCN | 0x40520514 | FULL | TT Operation Control |
| CANFD0_CH2_TTGPL | 0x40520518 | FULL | TT Global Time Preset |
| CANFD0_CH2_TTTMK | 0x4052051C | FULL | TT Time Mark |
| CANFD0_CH2_TTIR | 0x40520520 | FULL | TT Interrupt Register |
| CANFD0_CH2_TTIE | 0x40520524 | FULL | TT Interrupt Enable |
| CANFD0_CH2_TTILS | 0x40520528 | FULL | TT Interrupt Line Select |
| CANFD0_CH2_TTOST | 0x4052052C | FULL | TT Operation Status |
| CANFD0_CH2_TURNA | 0x40520530 | FULL | TUR Numerator Actual |
| CANFD0_CH2_TTLGT | 0x40520534 | FULL | TT Local & Global Time |
| CANFD0_CH2_TTCTC | 0x40520538 | FULL | TT Cycle Time & Count |
| CANFD0_CH2_TTCPT | 0x4052053C | FULL | TT Capture Time |
| CANFD0_CH2_TTCSM | 0x40520540 | FULL | TT Cycle Sync Mark |

2.1.4 CH 3

This instance is not available in the following part numbers:

CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE, CYT2BL4BAS, CYT2BL4BAE, CYT2BL4CAS, CYT2BL4CAE.

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD0_CH3_RXFTOP_CTL | 0x40520780 | FULL | Receive FIFO Top control |
| CANFD0_CH3_RXFTOP0_STAT | 0x405207A0 | FULL | Receive FIFO 0 Top Status |
| CANFD0_CH3_RXFTOP0_DATA | 0x405207A8 | FULL | Receive FIFO 0 Top Data |
| CANFD0_CH3_RXFTOP1_STAT | 0x405207B0 | FULL | Receive FIFO 1 Top Status |
| CANFD0_CH3_RXFTOP1_DATA | 0x405207B8 | FULL | Receive FIFO 1 Top Data |

2.1.4.1 M_TTCAN

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD0_CH3_CREL | 0x40520600 | FULL | Core Release Register |
| CANFD0_CH3_ENDN | 0x40520604 | FULL | Endian Register |
| CANFD0_CH3_DBTP | 0x4052060C | FULL | Data Bit Timing & Prescaler Register |
| CANFD0_CH3_TEST | 0x40520610 | FULL | Test Register |
| CANFD0_CH3_RWD | 0x40520614 | FULL | RAM Watchdog |
| CANFD0_CH3_CCCR | 0x40520618 | FULL | CC Control Register |
| CANFD0_CH3_NBTP | 0x4052061C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD0_CH3_TSCC | 0x40520620 | FULL | Timestamp Counter Configuration |
| CANFD0_CH3_TSCV | 0x40520624 | FULL | Timestamp Counter Value |
| CANFD0_CH3_TOCC | 0x40520628 | FULL | Timeout Counter Configuration |
| CANFD0_CH3_TOCV | 0x4052062C | FULL | Timeout Counter Value |
| CANFD0_CH3_ECR | 0x40520640 | FULL | Error Counter Register |
| CANFD0_CH3_PSR | 0x40520644 | FULL | Protocol Status Register |
| CANFD0_CH3_TDCR | 0x40520648 | FULL | Transmitter Delay Compensation Register |
| CANFD0_CH3_IR | 0x40520650 | FULL | Interrupt Register |
| CANFD0_CH3_IE | 0x40520654 | FULL | Interrupt Enable |
| CANFD0_CH3_ILS | 0x40520658 | FULL | Interrupt Line Select |
| CANFD0_CH3_ILE | 0x4052065C | FULL | Interrupt Line Enable |
| CANFD0_CH3_GFC | 0x40520680 | FULL | Global Filter Configuration |
| CANFD0_CH3_SIDFC | 0x40520684 | FULL | Standard ID Filter Configuration |
| CANFD0_CH3_XIDFC | 0x40520688 | FULL | Extended ID Filter Configuration |
| CANFD0_CH3_XIDAM | 0x40520690 | FULL | Extended ID AND Mask |
| CANFD0_CH3_HPMS | 0x40520694 | FULL | High Priority Message Status |
| CANFD0_CH3_NDAT1 | 0x40520698 | FULL | New Data 1 |
| CANFD0_CH3_NDAT2 | 0x4052069C | FULL | New Data 2 |
| CANFD0_CH3_RXF0C | 0x405206A0 | FULL | Rx FIFO 0 Configuration |
| CANFD0_CH3_RXF0S | 0x405206A4 | FULL | Rx FIFO 0 Status |
| CANFD0_CH3_RXF0A | 0x405206A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD0_CH3_RXBC | 0x405206AC | FULL | Rx Buffer Configuration |
| CANFD0_CH3_RXF1C | 0x405206B0 | FULL | Rx FIFO 1 Configuration |
| CANFD0_CH3_RXF1S | 0x405206B4 | FULL | Rx FIFO 1 Status |
| CANFD0_CH3_RXF1A | 0x405206B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD0_CH3_RXESC | 0x405206BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD0_CH3_TXBC | 0x405206C0 | FULL | Tx Buffer Configuration |
| CANFD0_CH3_TXFQS | 0x405206C4 | FULL | Tx FIFO/Queue Status |
| CANFD0_CH3_TXESC | 0x405206C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD0_CH3_TXBRP | 0x405206CC | FULL | Tx Buffer Request Pending |
| CANFD0_CH3_TXBAR | 0x405206D0 | FULL | Tx Buffer Add Request |
| CANFD0_CH3_TXBCR | 0x405206D4 | FULL | Tx Buffer Cancellation Request |
| CANFD0_CH3_TXBTO | 0x405206D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD0_CH3_TXBCF | 0x405206DC | FULL | Tx Buffer Cancellation Finished |
| CANFD0_CH3_TXBTIE | 0x405206E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD0_CH3_TXBCIE | 0x405206E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD0_CH3_TXEFC | 0x405206F0 | FULL | Tx Event FIFO Configuration |
| CANFD0_CH3_TXEFS | 0x405206F4 | FULL | Tx Event FIFO Status |
| CANFD0_CH3_TXEFA | 0x405206F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD0_CH3_TTTMC | 0x40520700 | FULL | TT Trigger Memory Configuration |
| CANFD0_CH3_TTRMC | 0x40520704 | FULL | TT Reference Message Configuration |
| CANFD0_CH3_TTOCF | 0x40520708 | FULL | TT Operation Configuration |
| CANFD0_CH3_TTMLM | 0x4052070C | FULL | TT Matrix Limits |
| CANFD0_CH3_TURCF | 0x40520710 | FULL | TUR Configuration |
| CANFD0_CH3_TTOCN | 0x40520714 | FULL | TT Operation Control |
| CANFD0_CH3_TTGTP | 0x40520718 | FULL | TT Global Time Preset |
| CANFD0_CH3_TTTMK | 0x4052071C | FULL | TT Time Mark |
| CANFD0_CH3_TTIR | 0x40520720 | FULL | TT Interrupt Register |
| CANFD0_CH3_TTIE | 0x40520724 | FULL | TT Interrupt Enable |
| CANFD0_CH3_TTILS | 0x40520728 | FULL | TT Interrupt Line Select |
| CANFD0_CH3_TTOST | 0x4052072C | FULL | TT Operation Status |
| CANFD0_CH3_TURNA | 0x40520730 | FULL | TUR Numerator Actual |
| CANFD0_CH3_TTLGT | 0x40520734 | FULL | TT Local & Global Time |
| CANFD0_CH3_TTCTC | 0x40520738 | FULL | TT Cycle Time & Count |
| CANFD0_CH3_TTCPT | 0x4052073C | FULL | TT Capture Time |
| CANFD0_CH3_TTCSM | 0x40520740 | FULL | TT Cycle Sync Mark |

2.2 CANFD 1

| | |
|---------------------|----------------|
| Description | CAN Controller |
| Base Address | 0x40540000 |
| Size | 0x20000 |
| Slave Num | MMIO5 - 3 |

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|--|
| CANFD1_CTL | 0x40541000 | FULL | Global CAN control register |
| CANFD1_STATUS | 0x40541004 | FULL | Global CAN status register |
| CANFD1_INTR0_CAUSE | 0x40541010 | FULL | Consolidated interrupt0 cause register |
| CANFD1_INTR1_CAUSE | 0x40541014 | FULL | Consolidated interrupt1 cause register |
| CANFD1_ECC_CTL | 0x40541080 | FULL | ECC control |
| CANFD1_ECC_ERR_INJ | 0x40541084 | FULL | ECC error injection |

2.2.1 CH 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD1_CH0_RXFTOP_CTL | 0x40540180 | FULL | Receive FIFO Top control |
| CANFD1_CH0_RXFTOP0_STAT | 0x405401A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH0_RXFTOP0_DATA | 0x405401A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH0_RXFTOP1_STAT | 0x405401B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH0_RXFTOP1_DATA | 0x405401B8 | FULL | Receive FIFO 1 Top Data |

2.2.1.1 M_TTCAN

| Register Name | Address | Permission | Description |
|------------------|------------|------------|---|
| CANFD1_CH0_CREL | 0x40540000 | FULL | Core Release Register |
| CANFD1_CH0_ENDN | 0x40540004 | FULL | Endian Register |
| CANFD1_CH0_DBTP | 0x4054000C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH0_TEST | 0x40540010 | FULL | Test Register |
| CANFD1_CH0_RWD | 0x40540014 | FULL | RAM Watchdog |
| CANFD1_CH0_CCCR | 0x40540018 | FULL | CC Control Register |
| CANFD1_CH0_NBTP | 0x4054001C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH0_TSCC | 0x40540020 | FULL | Timestamp Counter Configuration |
| CANFD1_CH0_TSCV | 0x40540024 | FULL | Timestamp Counter Value |
| CANFD1_CH0_TOCC | 0x40540028 | FULL | Timeout Counter Configuration |
| CANFD1_CH0_TOCV | 0x4054002C | FULL | Timeout Counter Value |
| CANFD1_CH0_ECR | 0x40540040 | FULL | Error Counter Register |
| CANFD1_CH0_PSR | 0x40540044 | FULL | Protocol Status Register |
| CANFD1_CH0_TDCR | 0x40540048 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH0_IR | 0x40540050 | FULL | Interrupt Register |
| CANFD1_CH0_IE | 0x40540054 | FULL | Interrupt Enable |
| CANFD1_CH0_ILS | 0x40540058 | FULL | Interrupt Line Select |
| CANFD1_CH0_ILE | 0x4054005C | FULL | Interrupt Line Enable |
| CANFD1_CH0_GFC | 0x40540080 | FULL | Global Filter Configuration |
| CANFD1_CH0_SIDFC | 0x40540084 | FULL | Standard ID Filter Configuration |
| CANFD1_CH0_XIDFC | 0x40540088 | FULL | Extended ID Filter Configuration |
| CANFD1_CH0_XIDAM | 0x40540090 | FULL | Extended ID AND Mask |
| CANFD1_CH0_HPMS | 0x40540094 | FULL | High Priority Message Status |
| CANFD1_CH0_NDAT1 | 0x40540098 | FULL | New Data 1 |
| CANFD1_CH0_NDAT2 | 0x4054009C | FULL | New Data 2 |
| CANFD1_CH0_RXF0C | 0x405400A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH0_RXF0S | 0x405400A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH0_RXF0A | 0x405400A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH0_RXBC | 0x405400AC | FULL | Rx Buffer Configuration |
| CANFD1_CH0_RXF1C | 0x405400B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH0_RXF1S | 0x405400B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH0_RXF1A | 0x405400B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH0_RXESC | 0x405400BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH0_TXBC | 0x405400C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH0_TXFQS | 0x405400C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH0_TXESC | 0x405400C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH0_TXBRP | 0x405400CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH0_TXBAR | 0x405400D0 | FULL | Tx Buffer Add Request |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD1_CH0_TXBCR | 0x405400D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH0_TXBTO | 0x405400D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH0_TXBCF | 0x405400DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH0_TXBTIE | 0x405400E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH0_TXBCIE | 0x405400E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH0_TXEFC | 0x405400F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH0_TXEFS | 0x405400F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH0_TXEFA | 0x405400F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH0_TTTMC | 0x40540100 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH0_TTRMC | 0x40540104 | FULL | TT Reference Message Configuration |
| CANFD1_CH0_TTOCF | 0x40540108 | FULL | TT Operation Configuration |
| CANFD1_CH0_TTMLM | 0x4054010C | FULL | TT Matrix Limits |
| CANFD1_CH0_TURCF | 0x40540110 | FULL | TUR Configuration |
| CANFD1_CH0_TTOCN | 0x40540114 | FULL | TT Operation Control |
| CANFD1_CH0_TTGTP | 0x40540118 | FULL | TT Global Time Preset |
| CANFD1_CH0_TTTMK | 0x4054011C | FULL | TT Time Mark |
| CANFD1_CH0_TTIR | 0x40540120 | FULL | TT Interrupt Register |
| CANFD1_CH0_TTIE | 0x40540124 | FULL | TT Interrupt Enable |
| CANFD1_CH0_TTILS | 0x40540128 | FULL | TT Interrupt Line Select |
| CANFD1_CH0_TTOST | 0x4054012C | FULL | TT Operation Status |
| CANFD1_CH0_TURNA | 0x40540130 | FULL | TUR Numerator Actual |
| CANFD1_CH0_TTLGT | 0x40540134 | FULL | TT Local & Global Time |
| CANFD1_CH0_TTCTC | 0x40540138 | FULL | TT Cycle Time & Count |
| CANFD1_CH0_TTCPT | 0x4054013C | FULL | TT Capture Time |
| CANFD1_CH0_TTCSM | 0x40540140 | FULL | TT Cycle Sync Mark |

2.2.2 CH 1

This instance is not available in the following part numbers:
CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE.

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD1_CH1_RXFTOP_CTL | 0x40540380 | FULL | Receive FIFO Top control |
| CANFD1_CH1_RXFTOP0_STAT | 0x405403A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH1_RXFTOP0_DATA | 0x405403A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH1_RXFTOP1_STAT | 0x405403B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH1_RXFTOP1_DATA | 0x405403B8 | FULL | Receive FIFO 1 Top Data |

2.2.2.1 M_TTCAN

| Register Name | Address | Permission | Description |
|------------------|------------|------------|---|
| CANFD1_CH1_CREL | 0x40540200 | FULL | Core Release Register |
| CANFD1_CH1_ENDN | 0x40540204 | FULL | Endian Register |
| CANFD1_CH1_DBTP | 0x4054020C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH1_TEST | 0x40540210 | FULL | Test Register |
| CANFD1_CH1_RWD | 0x40540214 | FULL | RAM Watchdog |
| CANFD1_CH1_CCCR | 0x40540218 | FULL | CC Control Register |
| CANFD1_CH1_NBTP | 0x4054021C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH1_TSCC | 0x40540220 | FULL | Timestamp Counter Configuration |
| CANFD1_CH1_TSCV | 0x40540224 | FULL | Timestamp Counter Value |
| CANFD1_CH1_TOCC | 0x40540228 | FULL | Timeout Counter Configuration |
| CANFD1_CH1_TOCV | 0x4054022C | FULL | Timeout Counter Value |
| CANFD1_CH1_ECR | 0x40540240 | FULL | Error Counter Register |
| CANFD1_CH1_PSR | 0x40540244 | FULL | Protocol Status Register |
| CANFD1_CH1_TDCR | 0x40540248 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH1_IR | 0x40540250 | FULL | Interrupt Register |
| CANFD1_CH1_IE | 0x40540254 | FULL | Interrupt Enable |
| CANFD1_CH1_ILS | 0x40540258 | FULL | Interrupt Line Select |
| CANFD1_CH1_ILE | 0x4054025C | FULL | Interrupt Line Enable |
| CANFD1_CH1_GFC | 0x40540280 | FULL | Global Filter Configuration |
| CANFD1_CH1_SIDFC | 0x40540284 | FULL | Standard ID Filter Configuration |
| CANFD1_CH1_XIDFC | 0x40540288 | FULL | Extended ID Filter Configuration |
| CANFD1_CH1_XIDAM | 0x40540290 | FULL | Extended ID AND Mask |
| CANFD1_CH1_HPMS | 0x40540294 | FULL | High Priority Message Status |
| CANFD1_CH1_NDAT1 | 0x40540298 | FULL | New Data 1 |
| CANFD1_CH1_NDAT2 | 0x4054029C | FULL | New Data 2 |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD1_CH1_RXF0C | 0x405402A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH1_RXF0S | 0x405402A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH1_RXF0A | 0x405402A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH1_RXBC | 0x405402AC | FULL | Rx Buffer Configuration |
| CANFD1_CH1_RXF1C | 0x405402B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH1_RXF1S | 0x405402B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH1_RXF1A | 0x405402B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH1_RXESC | 0x405402BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH1_TXBC | 0x405402C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH1_TXFQS | 0x405402C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH1_TXESC | 0x405402C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH1_TXBRP | 0x405402CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH1_TXBAR | 0x405402D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH1_TXBCR | 0x405402D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH1_TXBTO | 0x405402D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH1_TXBCF | 0x405402DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH1_TXBTIE | 0x405402E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH1_TXBCIE | 0x405402E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH1_TXEFC | 0x405402F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH1_TXEFS | 0x405402F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH1_TXEFA | 0x405402F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH1_TTMCM | 0x40540300 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH1_TTRMC | 0x40540304 | FULL | TT Reference Message Configuration |
| CANFD1_CH1_TTOCF | 0x40540308 | FULL | TT Operation Configuration |
| CANFD1_CH1_TTMMLM | 0x4054030C | FULL | TT Matrix Limits |
| CANFD1_CH1_TURCF | 0x40540310 | FULL | TUR Configuration |
| CANFD1_CH1_TTOCN | 0x40540314 | FULL | TT Operation Control |
| CANFD1_CH1_TTGRP | 0x40540318 | FULL | TT Global Time Preset |
| CANFD1_CH1_TTMMK | 0x4054031C | FULL | TT Time Mark |
| CANFD1_CH1_TTIR | 0x40540320 | FULL | TT Interrupt Register |
| CANFD1_CH1_TTIE | 0x40540324 | FULL | TT Interrupt Enable |
| CANFD1_CH1_TTILS | 0x40540328 | FULL | TT Interrupt Line Select |
| CANFD1_CH1_TTOST | 0x4054032C | FULL | TT Operation Status |
| CANFD1_CH1_TURNA | 0x40540330 | FULL | TUR Numerator Actual |
| CANFD1_CH1_TTLGT | 0x40540334 | FULL | TT Local & Global Time |
| CANFD1_CH1_TTCTC | 0x40540338 | FULL | TT Cycle Time & Count |
| CANFD1_CH1_TTCPT | 0x4054033C | FULL | TT Capture Time |
| CANFD1_CH1_TTCSM | 0x40540340 | FULL | TT Cycle Sync Mark |

2.2.3 CH 2

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD1_CH2_RXFTOP_CTL | 0x40540580 | FULL | Receive FIFO Top control |
| CANFD1_CH2_RXFTOP0_STAT | 0x405405A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH2_RXFTOP0_DATA | 0x405405A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH2_RXFTOP1_STAT | 0x405405B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH2_RXFTOP1_DATA | 0x405405B8 | FULL | Receive FIFO 1 Top Data |

2.2.3.1 M_TTCAN

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---|
| CANFD1_CH2_CREL | 0x40540400 | FULL | Core Release Register |
| CANFD1_CH2_ENDN | 0x40540404 | FULL | Endian Register |
| CANFD1_CH2_DBTP | 0x4054040C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH2_TEST | 0x40540410 | FULL | Test Register |
| CANFD1_CH2_RWD | 0x40540414 | FULL | RAM Watchdog |
| CANFD1_CH2_CCCR | 0x40540418 | FULL | CC Control Register |
| CANFD1_CH2_NBTP | 0x4054041C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH2_TSCC | 0x40540420 | FULL | Timestamp Counter Configuration |
| CANFD1_CH2_TSCV | 0x40540424 | FULL | Timestamp Counter Value |
| CANFD1_CH2_TOCC | 0x40540428 | FULL | Timeout Counter Configuration |
| CANFD1_CH2_TOCV | 0x4054042C | FULL | Timeout Counter Value |
| CANFD1_CH2_ECR | 0x40540440 | FULL | Error Counter Register |
| CANFD1_CH2_PSR | 0x40540444 | FULL | Protocol Status Register |
| CANFD1_CH2_TDCR | 0x40540448 | FULL | Transmitter Delay Compensation Register |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD1_CH2_IR | 0x40540450 | FULL | Interrupt Register |
| CANFD1_CH2_IE | 0x40540454 | FULL | Interrupt Enable |
| CANFD1_CH2_ILS | 0x40540458 | FULL | Interrupt Line Select |
| CANFD1_CH2_ILE | 0x4054045C | FULL | Interrupt Line Enable |
| CANFD1_CH2_GFC | 0x40540480 | FULL | Global Filter Configuration |
| CANFD1_CH2_SIDFC | 0x40540484 | FULL | Standard ID Filter Configuration |
| CANFD1_CH2_XIDFC | 0x40540488 | FULL | Extended ID Filter Configuration |
| CANFD1_CH2_XIDAM | 0x40540490 | FULL | Extended ID AND Mask |
| CANFD1_CH2_HPMS | 0x40540494 | FULL | High Priority Message Status |
| CANFD1_CH2_NDAT1 | 0x40540498 | FULL | New Data 1 |
| CANFD1_CH2_NDAT2 | 0x4054049C | FULL | New Data 2 |
| CANFD1_CH2_RXF0C | 0x405404A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH2_RXF0S | 0x405404A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH2_RXF0A | 0x405404A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH2_RXBC | 0x405404AC | FULL | Rx Buffer Configuration |
| CANFD1_CH2_RXF1C | 0x405404B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH2_RXF1S | 0x405404B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH2_RXF1A | 0x405404B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH2_RXESC | 0x405404BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH2_TXBC | 0x405404C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH2_TXFQS | 0x405404C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH2_TXESC | 0x405404C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH2_TXBRP | 0x405404CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH2_TXBAR | 0x405404D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH2_TXBCR | 0x405404D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH2_TXBTO | 0x405404D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH2_TXBCF | 0x405404DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH2_TXBTIE | 0x405404E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH2_TXBCIE | 0x405404E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH2_TXEFC | 0x405404F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH2_TXEFS | 0x405404F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH2_TXEFA | 0x405404F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH2_TTTMC | 0x40540500 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH2_TTRMC | 0x40540504 | FULL | TT Reference Message Configuration |
| CANFD1_CH2_TTOCF | 0x40540508 | FULL | TT Operation Configuration |
| CANFD1_CH2_TTMLM | 0x4054050C | FULL | TT Matrix Limits |
| CANFD1_CH2_TURCF | 0x40540510 | FULL | TUR Configuration |
| CANFD1_CH2_TTOCN | 0x40540514 | FULL | TT Operation Control |
| CANFD1_CH2_TTGTP | 0x40540518 | FULL | TT Global Time Preset |
| CANFD1_CH2_TTTMK | 0x4054051C | FULL | TT Time Mark |
| CANFD1_CH2_TTIR | 0x40540520 | FULL | TT Interrupt Register |
| CANFD1_CH2_TTIE | 0x40540524 | FULL | TT Interrupt Enable |
| CANFD1_CH2_TTILS | 0x40540528 | FULL | TT Interrupt Line Select |
| CANFD1_CH2_TTOST | 0x4054052C | FULL | TT Operation Status |
| CANFD1_CH2_TURNA | 0x40540530 | FULL | TUR Numerator Actual |
| CANFD1_CH2_TTLGT | 0x40540534 | FULL | TT Local & Global Time |
| CANFD1_CH2_TTCTC | 0x40540538 | FULL | TT Cycle Time & Count |
| CANFD1_CH2_TTCPT | 0x4054053C | FULL | TT Capture Time |
| CANFD1_CH2_TTCSM | 0x40540540 | FULL | TT Cycle Sync Mark |

2.2.4 CH 3

This instance is not available in the following part numbers:
CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE.

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---------------------------|
| CANFD1_CH3_RXFTOP_CTL | 0x40540780 | FULL | Receive FIFO Top control |
| CANFD1_CH3_RXFTOP0_STAT | 0x405407A0 | FULL | Receive FIFO 0 Top Status |
| CANFD1_CH3_RXFTOP0_DATA | 0x405407A8 | FULL | Receive FIFO 0 Top Data |
| CANFD1_CH3_RXFTOP1_STAT | 0x405407B0 | FULL | Receive FIFO 1 Top Status |
| CANFD1_CH3_RXFTOP1_DATA | 0x405407B8 | FULL | Receive FIFO 1 Top Data |

2.2.4.1 M_TTCAN

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|-----------------------|
| CANFD1_CH3_CREL | 0x40540600 | FULL | Core Release Register |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CANFD1_CH3_ENDN | 0x40540604 | FULL | Endian Register |
| CANFD1_CH3_DBTP | 0x4054060C | FULL | Data Bit Timing & Prescaler Register |
| CANFD1_CH3_TEST | 0x40540610 | FULL | Test Register |
| CANFD1_CH3_RWD | 0x40540614 | FULL | RAM Watchdog |
| CANFD1_CH3_CCCR | 0x40540618 | FULL | CC Control Register |
| CANFD1_CH3_NBTP | 0x4054061C | FULL | Nominal Bit Timing & Prescaler Register |
| CANFD1_CH3_TSCC | 0x40540620 | FULL | Timestamp Counter Configuration |
| CANFD1_CH3_TSCV | 0x40540624 | FULL | Timestamp Counter Value |
| CANFD1_CH3_TOCC | 0x40540628 | FULL | Timeout Counter Configuration |
| CANFD1_CH3_TOCV | 0x4054062C | FULL | Timeout Counter Value |
| CANFD1_CH3_ECR | 0x40540640 | FULL | Error Counter Register |
| CANFD1_CH3_PSR | 0x40540644 | FULL | Protocol Status Register |
| CANFD1_CH3_TDRC | 0x40540648 | FULL | Transmitter Delay Compensation Register |
| CANFD1_CH3_IR | 0x40540650 | FULL | Interrupt Register |
| CANFD1_CH3_IE | 0x40540654 | FULL | Interrupt Enable |
| CANFD1_CH3_ILS | 0x40540658 | FULL | Interrupt Line Select |
| CANFD1_CH3_ILE | 0x4054065C | FULL | Interrupt Line Enable |
| CANFD1_CH3_GFC | 0x40540680 | FULL | Global Filter Configuration |
| CANFD1_CH3_SIDFC | 0x40540684 | FULL | Standard ID Filter Configuration |
| CANFD1_CH3_XIDFC | 0x40540688 | FULL | Extended ID Filter Configuration |
| CANFD1_CH3_XIDAM | 0x40540690 | FULL | Extended ID AND Mask |
| CANFD1_CH3_HPMS | 0x40540694 | FULL | High Priority Message Status |
| CANFD1_CH3_NDAT1 | 0x40540698 | FULL | New Data 1 |
| CANFD1_CH3_NDAT2 | 0x4054069C | FULL | New Data 2 |
| CANFD1_CH3_RXF0C | 0x405406A0 | FULL | Rx FIFO 0 Configuration |
| CANFD1_CH3_RXF0S | 0x405406A4 | FULL | Rx FIFO 0 Status |
| CANFD1_CH3_RXF0A | 0x405406A8 | FULL | Rx FIFO 0 Acknowledge |
| CANFD1_CH3_RXBC | 0x405406AC | FULL | Rx Buffer Configuration |
| CANFD1_CH3_RXF1C | 0x405406B0 | FULL | Rx FIFO 1 Configuration |
| CANFD1_CH3_RXF1S | 0x405406B4 | FULL | Rx FIFO 1 Status |
| CANFD1_CH3_RXF1A | 0x405406B8 | FULL | Rx FIFO 1 Acknowledge |
| CANFD1_CH3_RXESC | 0x405406BC | FULL | Rx Buffer / FIFO Element Size Configuration |
| CANFD1_CH3_TXBC | 0x405406C0 | FULL | Tx Buffer Configuration |
| CANFD1_CH3_TXFQS | 0x405406C4 | FULL | Tx FIFO/Queue Status |
| CANFD1_CH3_TXESC | 0x405406C8 | FULL | Tx Buffer Element Size Configuration |
| CANFD1_CH3_TXBRP | 0x405406CC | FULL | Tx Buffer Request Pending |
| CANFD1_CH3_TXBAR | 0x405406D0 | FULL | Tx Buffer Add Request |
| CANFD1_CH3_TXBCR | 0x405406D4 | FULL | Tx Buffer Cancellation Request |
| CANFD1_CH3_TXBTO | 0x405406D8 | FULL | Tx Buffer Transmission Occurred |
| CANFD1_CH3_TXBCF | 0x405406DC | FULL | Tx Buffer Cancellation Finished |
| CANFD1_CH3_TXBTIE | 0x405406E0 | FULL | Tx Buffer Transmission Interrupt Enable |
| CANFD1_CH3_TXBCIE | 0x405406E4 | FULL | Tx Buffer Cancellation Finished Interrupt Enable |
| CANFD1_CH3_TXEFC | 0x405406F0 | FULL | Tx Event FIFO Configuration |
| CANFD1_CH3_TXEFS | 0x405406F4 | FULL | Tx Event FIFO Status |
| CANFD1_CH3_TXEFA | 0x405406F8 | FULL | Tx Event FIFO Acknowledge |
| CANFD1_CH3_TTTMC | 0x40540700 | FULL | TT Trigger Memory Configuration |
| CANFD1_CH3_TTRMC | 0x40540704 | FULL | TT Reference Message Configuration |
| CANFD1_CH3_TTOCF | 0x40540708 | FULL | TT Operation Configuration |
| CANFD1_CH3_TTMLM | 0x4054070C | FULL | TT Matrix Limits |
| CANFD1_CH3_TURCF | 0x40540710 | FULL | TUR Configuration |
| CANFD1_CH3_TTOCN | 0x40540714 | FULL | TT Operation Control |
| CANFD1_CH3_TTGTP | 0x40540718 | FULL | TT Global Time Preset |
| CANFD1_CH3_TTTMK | 0x4054071C | FULL | TT Time Mark |
| CANFD1_CH3_TTIR | 0x40540720 | FULL | TT Interrupt Register |
| CANFD1_CH3_TTIE | 0x40540724 | FULL | TT Interrupt Enable |
| CANFD1_CH3_TTILS | 0x40540728 | FULL | TT Interrupt Line Select |
| CANFD1_CH3_TTOST | 0x4054072C | FULL | TT Operation Status |
| CANFD1_CH3_TURNA | 0x40540730 | FULL | TUR Numerator Actual |
| CANFD1_CH3_TTLGT | 0x40540734 | FULL | TT Local & Global Time |
| CANFD1_CH3_TTCTC | 0x40540738 | FULL | TT Cycle Time & Count |
| CANFD1_CH3_TTCPT | 0x4054073C | FULL | TT Capture Time |
| CANFD1_CH3_TTCSM | 0x40540740 | FULL | TT Cycle Sync Mark |

2.3 Register Details

2.3.1 CANFD_CTL

Description: Global CAN control register
Address: 0x40521000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------|----|----|----|----|----|----|
| Name | STOP_REQ [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | MRAM_OFF [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:7 | STOP_REQ | RW | R | 0 | Clock Stop Request for each TTCAN IP . The m_ttcn_clkstop_req of each TTCAN IP is directly driven by these bits. |
| 31 | MRAM_OFF | RW | R | 0 | MRAM off 0= Default MRAM on (with MRAM retained in DeepSleep). 1= Switch MRAM off (not retained) to save power. Before setting this bit all the CAN channels have to be powered down using the STOP_REQ/ACK bits. When the MRAM is off any access attempt to it is considered an address error (as if MRAM_SIZE=0). After switching the MRAM on again software needs to allow for a certain power up time before MRAM can be used, i.e. before STOP_REQ can be de-asserted. The power up time is equivalent to the system SRAM power up time specified in the CPUSS.RAM_PWR_DELAY_CTL register. MRAM_OFF should be set to 0 prior to transitioning to Hibernate mode. |

2.3.2 CANFD_STATUS

Description: Global CAN status register
Address: 0x40521004
Offset: 0x1004
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | STOP_ACK [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:7 | STOP_ACK | R | RW | 0 | Clock Stop Acknowledge for each TTCAN IP. These bits are directly driven by m_tcan_clkstop_ack of each TTCAN IP. When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will be enabled for each AHB write |

2.3.3 CANFD_INTRO_CAUSE

Description: Consolidated interrupt0 cause register
Address: 0x40521010
Offset: 0x1010
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | INT0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:7 | INT0 | R | RW | 0 | Show pending m_ttcan_int0 of each channel |

2.3.4 CANFD_INTR1_CAUSE

Description: Consolidated interrupt1 cause register
Address: 0x40521014
Offset: 0x1014
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | INT1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:7 | INT1 | R | RW | 0 | Show pending m_ttcan_int1 of each channel |

2.3.5 CANFD_TS_CTL

Description: Time Stamp control register
Address: 0x40521020
Offset: 0x1020
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | PRESCALE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PRESCALE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:15 | PRESCALE | RW | R | 0 | Time Stamp counter prescale value. When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. |
| 31 | ENABLED | RW | R | 0 | Counter enable bit 0 = Count disabled. Stop counting up and keep the counter value 1 = Count enabled. Start counting up from the current value |

2.3.6 CANFD_TS_CNT

Description: Time Stamp counter value
Address: 0x40521024
Offset: 0x1024
Retention: Not Retained
IsDeepSleep: No
Comment: Not retained
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:15 | VALUE | RW | A | 0 | The counter value of the Time Stamp Counter. When enabled this counter will count Time Stamp clock ticks from the pre-scaler. When written this counter and the pre-scaler will reset to 0 (write data is ignored). |

2.3.7 CANFD_ECC_CTL

Description: ECC control
Address: 0x40521080
Offset: 0x1080
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----------------|
| Name | None [23:17] | | | | | | | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 16 | ECC_EN | RW | R | 0 | Enable ECC for CANFD SRAM When disabled also all error injection functionality is disabled. |

2.3.8 CANFD_ECC_ERR_INJ

Description: ECC error injection
Address: 0x40521084
Offset: 0x1084
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFC

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | ERR_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----------------|--------------|----|----|----|
| Name | None [23:21] | | | ERR_EN [20:20] | None [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|-----------------|----|----|----|----|----|----|
| Name | None [31:31] | ERR_PAR [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 2:15 | ERR_ADDR | RW | R | 16383 | Specifies the address of the word where an error will be injected on write or a non-correctable error will be suppressed. When the ERR_EN bit is set an error parity (ERR_PAR) is injected when any write, from bus or a CAN channel, is done to this address. When the ERR_EN bit is set and the access address matches ERR_ADDR then a non-correctable ECC error or an Address error will NOT result in a bus error or CAN channel shutdown. Note that error reporting to the fault structure cannot be suppressed. |
| 20 | ERR_EN | RW | R | 0 | Enable error injection (ECC_EN must be 1). When this bit is set the error parity (ERR_PAR) will be used when an AHB write is done to the ERR_ADDR address. When the error word is read a single or double error will be reported to the fault structure just like for a real ECC error (even if this bit is no longer set). When this bit is set (and ECC_EN=1) a non-correctable error (ECC or address error) for the ERR_ADDR will not be reported back to the CAN channel or AHB bus. |
| 24:30 | ERR_PAR | RW | R | 0 | ECC Parity bits to use for ECC error injection at address ERR_ADDR. |

2.3.9 CH

2.3.9.1 CANFD_CH_RXFTOP_CTL

Description: Receive FIFO Top control
Address: 0x40520180
Offset: 0x180
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-------------|-------------|
| Name | None [7:2] | | | | | | F1TPE [1:1] | F0TPE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | F0TPE | RW | R | 0 | FIFO 0 Top Pointer Enable. This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter. This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1). When this logic is disabled a Read from RXFTOP0_DATA is undefined. |
| 1 | F1TPE | RW | R | 0 | FIFO 1 Top Pointer Enable. |

2.3.9.2 CANFD_CH_RXFTOP0_STAT

Description: Receive FIFO 0 Top Status
Address: 0x405201A0
Offset: 0x1A0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | F0TA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | F0TA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:15 | F0TA | R | RW | 0 | Current FIFO 0 Top Address. This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC) $FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC$ |

2.3.9.3 CANFD_CH_RXFTOP0_DATA

Description: Receive FIFO 0 Top Data
Address: 0x405201A8
Offset: 0x1A8
Retention: Retained
IsDeepSleep: No
Comment: Read side effect, except if read from debug host
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | F0TD [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | F0TD [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | F0TD [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | F0TD [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | F0TD | R | W | Undefined | <p>When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met:</p> <ul style="list-style-type: none"> - M_TTCAN not being reconfigured (CCCR.CCE=0) - FIFO Top Pointer logic is enabled (FnTPE=1) - FIFO is not empty (FnFL!=0) <p>The read side effect is as follows:</p> <ul style="list-style-type: none"> - if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI - FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message) - the FIFO top address FnTA is incremented (with FIFO wrap around) <p>When this logic is disabled (F0TPE=0) a Read from this register returns undefined data.</p> |

2.3.9.4 CANFD_CH_RXFTOP1_STAT

Description: Receive FIFO 1 Top Status
Address: 0x405201B0
Offset: 0x1B0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | F1TA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | F1TA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|----------------------|
| 0:15 | F1TA | R | RW | 0 | See F0TA description |

2.3.9.5 CANFD_CH_RXFTOP1_DATA

Description: Receive FIFO 1 Top Data
Address: 0x405201B8
Offset: 0x1B8
Retention: Retained
IsDeepSleep: No
Comment: Read side effect, except if read from debug host
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | F1TD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | F1TD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | F1TD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | F1TD [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|----------------------|
| 0:31 | F1TD | R | W | Undefined | See F0TD description |

2.3.9.6 M_TTCAN

2.3.9.6.1 CANFD_CH_CREL

Description: Core Release Register
Address: 0x40520000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|--------------|----|----|----|
| Name | DAY [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | MON [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | SUBSTEP [23:20] | | | | YEAR [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | REL [31:28] | | | | STEP [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|---|
| 0:7 | DAY | R | R | 0 | Time Stamp Day Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. |
| 8:15 | MON | R | R | 0 | Time Stamp Month Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. |
| 16:19 | YEAR | R | R | 0 | Time Stamp Year One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. |
| 20:23 | SUBSTEP | R | R | 0 | Sub-step of Core Release One digit, BCD-coded. |
| 24:27 | STEP | R | R | 0 | Step of Core Release One digit, BCD-coded. |
| 28:31 | REL | R | R | 0 | Core Release One digit, BCD-coded. |

2.3.9.6.2 CANFD_CH_ENDN

Description: Endian Register
Address: 0x40520004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x87654321

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | ETV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | ETV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | ETV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | ETV [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | ETV | R | R | 227156048 1 | Endianness Test Value The endianness test value is 0x87654321. |

2.3.9.6.3 CANFD_CH_DBTP

Description: Data Bit Timing & Prescaler Register
Address: 0x4052000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Protected Write
Default: 0xA33

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|--------------|----|---------------|------------|----|----|----|
| Name | DTSEG2 [7:4] | | | | DSJW [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | DTSEG1 [12:8] | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TDC [23:23] | None [22:21] | | DBRP [20:16] | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|---|
| 0:3 | DSJW | RW | R | 3 | Data (Re)Synchronization Jump Width 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 4:7 | DTSEG2 | RW | R | 3 | Data time segment after sample point 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 8:12 | DTSEG1 | RW | R | 10 | Data time segment before sample point 0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 16:20 | DBRP | RW | R | 0 | Data Bit Rate Prescaler 0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 23 | TDC | RW | R | 0 | Transmitter Delay Compensation 0= Transmitter Delay Compensation disabled 1= Transmitter Delay Compensation enabled |

2.3.9.6.4 CANFD_CH_TEST

Description: Test Register
Address: 0x40520010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Protected Write
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----------|----|------------|-----------|-----------|-----------|-----------|
| Name | RX [7:7] | TX [6:5] | | LBCK [4:4] | CAT [3:3] | CAM [2:2] | TAT [1:1] | TAM [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | TAM | RW | R | 0 | ASC is not supported by M_TTCAN Test ASC Multiplexer Control Controls output pin m_ttcn_ascm in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcn_ascm controlled by FSE 1= Level at pin m_ttcn_ascm = '1' |
| 1 | TAT | RW | R | 0 | ASC is not supported by M_TTCAN Test ASC Transmit Control Controls output pin m_ttcn_asct in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcn_asct controlled by FSE 1= Level at pin m_ttcn_asct = '1' |
| 2 | CAM | RW | R | 0 | ASC is not supported by M_TTCAN Check ASC Multiplexer Control Monitors level at output pin m_ttcn_ascm. 0= Output pin m_ttcn_ascm = '0' 1= Output pin m_ttcn_ascm = '1' |
| 3 | CAT | RW | R | 0 | ASC is not supported by M_TTCAN Check ASC Transmit Control Monitors level at output pin m_ttcn_asct. 0= Output pin m_ttcn_asct = '0' |
| 4 | LBCK | RW | R | 0 | Loop Back Mode 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled (see Section 3.1.9, Test Modes) |
| 5:6 | TX | RW | R | 0 | Control of Transmit Pin 00 Reset value, m_ttcn_tx controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin m_ttcn_tx 10 Dominant ('0') level at pin m_ttcn_tx 11 Recessive ('1') at pin m_ttcn_tx |
| 7 | RX | R | R | Undefined | Receive Pin Monitors the actual value of pin m_ttcn_rx 0= The CAN bus is dominant (m_ttcn_rx = '0') 1= The CAN bus is recessive (m_ttcn_rx = '1') |

2.3.9.6.5 CANFD_CH_RWD

Description: RAM Watchdog
Address: 0x40520014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Protected Write
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | WDC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | WDV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:7 | WDC | RW | R | 0 | Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. |
| 8:15 | WDV | R | R | 0 | Watchdog Value Actual Message RAM Watchdog Counter Value. |

2.3.9.6.6 CANFD_CH_CCCR

Description: CC Control Register
Address: 0x40520018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Protected Write
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|-----------|------------|-----------|-----------|-----------|-----------|------------|
| Name | TEST [7:7] | DAR [6:6] | MON_ [5:5] | CSR [4:4] | CSA [3:3] | ASM [2:2] | CCE [1:1] | INIT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-------------|--------------|--------------|--------------|----|------------|------------|
| Name | NISO [15:15] | TXP [14:14] | EFBI [13:13] | PXHD [12:12] | None [11:10] | | BRSE [9:9] | FDOE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | INIT | RW | R | 1 | Initialization 0= Normal Operation 1= Initialization is started |
| 1 | CCE | RW | R | 0 | Configuration Change Enable 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') |
| 2 | ASM | RW | R | 0 | Restricted Operation Mode Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode see Section 3.1.5. 0= Normal CAN operation 1= Restricted Operation Mode active |
| 3 | CSA | RW | R | 0 | Clock Stop Acknowledge 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcn_hclk and m_ttcn_cclk |
| 4 | CSR | RW | R | 0 | Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead. 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. |
| 5 | MON_ | RW | R | 0 | Bus Monitoring Mode Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 6 | DAR | RW | R | 0 | Disable Automatic Retransmission 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled |
| 7 | TEST | RW | R | 0 | Test Mode Enable 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled |
| 8 | FDOE | RW | R | 0 | FD Operation Enable 0= FD operation disabled 1= FD operation enabled |
| 9 | BRSE | RW | R | 0 | Bit Rate Switch Enable 0= Bit rate switching for transmissions disabled 1= Bit rate switching for transmissions enabled |
| 12 | PXHD | RW | R | 0 | Protocol Exception Handling Disable 0= Protocol exception handling enabled 1= Protocol exception handling disabled |
| 13 | EFBI | RW | R | 0 | Edge Filtering during Bus Integration 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization |
| 14 | TXP | RW | R | 0 | Transmit Pause If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 3.5). 0= Transmit pause disabled 1= Transmit pause enabled |
| 15 | NISO | RW | R | 0 | Non ISO Operation If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO 11898-1:2015 1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD |

2.3.9.6.7 CANFD_CH_NBTP

Description: Nominal Bit Timing & Prescaler Register
Address: 0x4052001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: Protected Write. With a CAN clock (m_can_cclk) of 8 MHz, the reset value of 0x06000A03 configures the M_CAN for a bit rate of 500 Kbit/s.
Default: 0x6000A03

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|----|----|----|----|--------------|
| Name | None [7:7] | NTSEG2 [6:0] | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | NTSEG1 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | NBRP [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | NSJW [31:25] | | | | | | | NBRP [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|---|
| 0:6 | NTSEG2 | RW | R | 3 | Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 8:15 | NTSEG1 | RW | R | 10 | Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 16:24 | NBRP | RW | R | 0 | Nominal Bit Rate Prescaler 0x000-0x1FF The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 25:31 | NSJW | RW | R | 3 | Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |

2.3.9.6.8 CANFD_CH_TSCC

Description: Timestamp Counter Configuration
Address: 0x40520020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-----------|---|
| Name | None [7:2] | | | | | | TSS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|-------------|----|----|----|
| Name | None [23:20] | | | | TCP [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:1 | TSS | RW | R | 0 | Timestamp Select, should always be set to external timestamp counter 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as '00' |
| 16:19 | TCP | RW | R | 0 | Timestamp Counter Prescaler (still used for TOCC) 0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |

2.3.9.6.9 CANFD_CH_TSCV

Description: Timestamp Counter Value
Address: 0x40520024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | TSC [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TSC [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:15 | TSC | RW | R | 0 | Timestamp Counter, not used for M_TTCAN The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. |

2.3.9.6.10 CANFD_CH_TOCC

Description: Timeout Counter Configuration
Address: 0x40520028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0xFFFF0000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------|---|------------|
| Name | None [7:3] | | | | | TOS [2:1] | | ETOC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TOP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TOP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|---|
| 0 | ETOC | RW | R | 0 | Enable Timeout Counter 0= Timeout Counter disabled 1= Timeout Counter enabled |
| 1:2 | TOS | RW | R | 0 | Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1 |
| 16:31 | TOP | RW | R | 65535 | Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. |

2.3.9.6.11 CANFD_CH_TOCV

Description: Timeout Counter Value
Address: 0x4052002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | TOC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | TOC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:15 | TOC | RW | R | 65535 | Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. |

2.3.9.6.12 CANFD_CH_ECR

Description: Error Counter Register
Address: 0x40520040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Read side effect, except if read from debug host
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | TEC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|------------|----|----|----|----|---|---|
| Name | RP [15:15] | REC [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | CEL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|------|-----------------|--|
| 0:7 | TEC | R | RW | 0 | Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255 |
| 8:14 | REC | R | RW | 0 | Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127 |
| 15 | RP | R | RW | 0 | Receive Error Passive 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128 |
| 16:23 | CEL | R | RW1C | 0 | CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. |

2.3.9.6.13 CANFD_CH_PSR

Description: Protocol Status Register
Address: 0x40520044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Read side effect, except if read from debug host
Default: 0x707

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|----------|----------|-----------|---|-----------|---|---|
| Name | BO [7:7] | EW [6:6] | EP [5:5] | ACT [4:3] | | LEC [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-------------|--------------|--------------|--------------|-------------|---|---|
| Name | None [15:15] | PXE [14:14] | RFDF [13:13] | RBRS [12:12] | RESI [11:11] | DLEC [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|--------------|----|----|----|----|----|----|
| Name | None [23:23] | TDCV [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|------|-----------------|--|
| 0:2 | LEC | R | RW1S | 7 | <p>Last Error Code, Set on Read0</p> <p>The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error.</p> <p>0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCErrror: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register.</p> |
| 3:4 | ACT | R | RW | 0 | <p>Activity</p> <p>Monitors the module's CAN communication state.</p> <p>00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter</p> |
| 5 | EP | R | RW | 0 | <p>Error Passive</p> <p>0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_CAN is in the Error_Passive state</p> |
| 6 | EW | R | RW | 0 | <p>Warning Status</p> <p>0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96</p> |
| 7 | BO | R | RW | 0 | <p>Bus_Off Status</p> <p>0= The M_CAN is not Bus_Off 1= The M_CAN is in Bus_Off state</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|------|-----------------|---|
| 8:10 | DLEC | R | RW1S | 7 | Data Phase Last Error Code , Set on Read Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. |
| 11 | RESI | R | RW1C | 0 | ESI flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set |
| 12 | RBRS | R | RW1C | 0 | BRS flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set |
| 13 | RFDF | R | RW1C | 0 | Received a CAN FD Message , Reset on Read This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with FDF flag set has been received |
| 14 | PXE | R | RW1C | 0 | Protocol Exception Event , Reset on Read 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred |
| 16:22 | TDCV | R | RW | 0 | Transmitter Delay Compensation Value 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. |

2.3.9.6.14 CANFD_CH_TDCR

Description: Transmitter Delay Compensation Register
Address: 0x40520048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|---|---|---|---|---|---|
| Name | None [7:7] | TDCF [6:0] | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-------------|----|----|----|----|---|---|
| Name | None [15:15] | TDCO [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:6 | TDCF | RW | R | 0 | Transmitter Delay Compensation Filter Window Length 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcn_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq |
| 8:14 | TDCO | RW | R | 0 | Transmitter Delay Compensation Offset 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcn_tx to m_ttcn_rx and the secondary sample point. Valid values are 0 to 127 mtq. |

2.3.9.6.15 CANFD_CH_IR

Description: Interrupt Register
Address: 0x40520050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|------------|------------|------------|-------------|------------|------------|------------|
| Name | RF1L_ [7:7] | RF1F [6:6] | RF1W [5:5] | RF1N [4:4] | RF0L_ [3:3] | RF0F [2:2] | RF0W [1:1] | RF0N [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|--------------|--------------|--------------|-------------|-------------|----------|-----------|
| Name | TEFL_ [15:15] | TEFF [14:14] | TEFW [13:13] | TEFN [12:12] | TFE [11:11] | TCF [10:10] | TC [9:9] | HPM [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|-------------|-------------|-------------|-------------|-------------|--------------|-------------|
| Name | EP_ [23:23] | ELO [22:22] | BEU [21:21] | BEC [20:20] | DRX [19:19] | TOO [18:18] | MRAF [17:17] | TSW [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | None [31:30] | | ARA [29:29] | PED [28:28] | PEA [27:27] | WDI [26:26] | BO_ [25:25] | EW_ [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|---|
| 0 | RF0N | RW1C | RW | 0 | Rx FIFO 0 New Message 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0 |
| 1 | RF0W | RW1C | RW | 0 | Rx FIFO 0 Watermark Reached 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark |
| 2 | RF0F | RW1C | RW | 0 | Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full |
| 3 | RF0L_ | RW1C | RW | 0 | Rx FIFO 0 Message Lost 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero |
| 4 | RF1N | RW1C | RW | 0 | Rx FIFO 1 New Message 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1 |
| 5 | RF1W | RW1C | RW | 0 | Rx FIFO 1 Watermark Reached 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark |
| 6 | RF1F | RW1C | RW | 0 | Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full |
| 7 | RF1L_ | RW1C | RW | 0 | Rx FIFO 1 Message Lost 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero |
| 8 | HPM | RW1C | RW | 0 | High Priority Message 0= No high priority message received 1= High priority message received |
| 9 | TC | RW1C | RW | 0 | Transmission Completed 0= No transmission completed 1= Transmission completed |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|---|
| 10 | TCF | RW1C | RW | 0 | Transmission Cancellation Finished 0= No transmission cancellation finished 1= Transmission cancellation finished |
| 11 | TFE | RW1C | RW | 0 | Tx FIFO Empty 0= Tx FIFO non-empty 1= Tx FIFO empty |
| 12 | TEFN | RW1C | RW | 0 | Tx Event FIFO New Entry 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element |
| 13 | TEFW | RW1C | RW | 0 | Tx Event FIFO Watermark Reached 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark |
| 14 | TEFF | RW1C | RW | 0 | Tx Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full |
| 15 | TEFL_ | RW1C | RW | 0 | Tx Event FIFO Element Lost 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero |
| 16 | TSW | RW1C | RW | 0 | Timestamp Wraparound 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around |
| 17 | MRAF | RW1C | RW | 0 | Message RAM Access Failure The flag is set, when the Rx Handler - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode (see Section 3.1.5). To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred |
| 18 | TOO | RW1C | RW | 0 | Timeout Occurred 0= No timeout 1= Timeout reached |
| 19 | DRX | RW1C | RW | 0 | Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer |
| 20 | BEC | RW1C | RW | 0 | Bit Error Corrected This bit always reads as 0. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 21 | BEU | RW1C | RW | 0 | <p>Bit Error Uncorrected</p> <p>Message RAM bit error detected, uncorrected. The flag is set in the following cases.</p> <ul style="list-style-type: none"> - M_TTCAN detects uncorrectable ECC error from Message RAM when ECC is enabled and ECC error injection is disabled. - M_TTCAN reads from an out of range Message RAM address. <p>Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data.</p> <p>0= No bit error detected when reading from Message RAM</p> <p>1= Bit error detected, uncorrected</p> |
| 22 | ELO | RW1C | RW | 0 | <p>Error Logging Overflow</p> <p>0= CAN Error Logging Counter did not overflow</p> <p>1= Overflow of CAN Error Logging Counter occurred</p> |
| 23 | EP_ | RW1C | RW | 0 | <p>Error Passive</p> <p>0= Error_Passive status unchanged</p> <p>1= Error_Passive status changed</p> |
| 24 | EW_ | RW1C | RW | 0 | <p>Warning Status</p> <p>0= Error_Warning status unchanged</p> <p>1= Error_Warning status changed</p> |
| 25 | BO_ | RW1C | RW | 0 | <p>Bus_Off Status</p> <p>0= Bus_Off status unchanged</p> <p>1= Bus_Off status changed</p> |
| 26 | WDI | RW1C | RW | 0 | <p>Watchdog Interrupt</p> <p>0= No Message RAM Watchdog event occurred</p> <p>1= Message RAM Watchdog event due to missing READY</p> |
| 27 | PEA | RW1C | RW | 0 | <p>Protocol Error in Arbitration Phase (Nominal Bit Time is used)</p> <p>0= No protocol error in arbitration phase</p> <p>1= Protocol error in arbitration phase detected (PSR.LEC != 0,7)</p> |
| 28 | PED | RW1C | RW | 0 | <p>Protocol Error in Data Phase (Data Bit Time is used)</p> <p>0= No protocol error in data phase</p> <p>1= Protocol error in data phase detected (PSR.DLEC != 0,7)</p> |
| 29 | ARA | RW1C | RW | 0 | <p>Access to Reserved Address</p> <p>0= No access to reserved address occurred</p> <p>1= Access to reserved address occurred</p> |

2.3.9.6.16 CANFD_CH_IE

Description: Interrupt Enable
Address: 0x40520054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | RF1LE [7:7] | RF1FE [6:6] | RF1WE [5:5] | RF1NE [4:4] | RF0LE [3:3] | RF0FE [2:2] | RF0WE [1:1] | RF0NE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|---------------|---------------|---------------|--------------|--------------|-----------|------------|
| Name | TEFLE [15:15] | TEFFE [14:14] | TEFWE [13:13] | TEFNE [12:12] | TFEE [11:11] | TCFE [10:10] | TCE [9:9] | HPME [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|
| Name | EPE [23:23] | ELOE [22:22] | BEUE [21:21] | BECE [20:20] | DRXE [19:19] | TOOE [18:18] | MRAFE [17:17] | TSWE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|--------------|--------------|--------------|--------------|-------------|-------------|
| Name | None [31:30] | | ARAE [29:29] | PEDE [28:28] | PEAE [27:27] | WDIE [26:26] | BOE [25:25] | EWE [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | RF0NE | RW | R | 0 | Rx FIFO 0 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 1 | RF0WE | RW | R | 0 | Rx FIFO 0 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 2 | RF0FE | RW | R | 0 | Rx FIFO 0 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 3 | RF0LE | RW | R | 0 | Rx FIFO 0 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 4 | RF1NE | RW | R | 0 | Rx FIFO 1 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 5 | RF1WE | RW | R | 0 | Rx FIFO 1 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 6 | RF1FE | RW | R | 0 | Rx FIFO 1 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 7 | RF1LE | RW | R | 0 | Rx FIFO 1 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 8 | HPME | RW | R | 0 | High Priority Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 9 | TCE | RW | R | 0 | Transmission Completed Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 10 | TCFE | RW | R | 0 | Transmission Cancellation Finished Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 11 | TFEE | RW | R | 0 | Tx FIFO Empty Interrupt Enable 0= Interrupt Disabled 1= Interrupt EnabledTx FIFO Empty Interrupt Enable |
| 12 | TEFNE | RW | R | 0 | Tx Event FIDO New Entry Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 13 | TEFWE | RW | R | 0 | Tx Event FIFO Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 14 | TEFFE | RW | R | 0 | Tx Event FIFO Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 15 | TEFLE | RW | R | 0 | Tx Event FIFO Event Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 16 | TSWE | RW | R | 0 | Timestamp Wraparound Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 17 | MRAFE | RW | R | 0 | Message RAM Access Failure Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 18 | TOOE | RW | R | 0 | Timeout Occurred Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 19 | DRXE | RW | R | 0 | Message stored to Dedicated Rx Buffer Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 20 | BECE | RW | R | 0 | Bit Error Corrected Interrupt Enable (not used in M_TTCAN) 0= Interrupt Disabled 1= Interrupt Enabled |
| 21 | BEUE | RW | R | 0 | Bit Error Uncorrected Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 22 | ELOE | RW | R | 0 | Error Logging Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 23 | EPE | RW | R | 0 | Error Passive Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 24 | EWE | RW | R | 0 | Warning Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 25 | BOE | RW | R | 0 | Bus_Off Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 26 | WDIE | RW | R | 0 | Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 27 | PEAE | RW | R | 0 | Protocol Error in Arbitration Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 28 | PEDE | RW | R | 0 | Protocol Error in Data Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 29 | ARAE | RW | R | 0 | Access to Reserved Address Enable 0= Interrupt Disabled 1= Interrupt Enabled |

2.3.9.6.17 CANFD_CH_ILS

Description: Interrupt Line Select

Address: 0x40520058

Offset: 0x58

Retention: Retained

IsDeepSleep: No

Comment: The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | RF1LL [7:7] | RF1FL [6:6] | RF1WL [5:5] | RF1NL [4:4] | RF0LL [3:3] | RF0FL [2:2] | RF0WL [1:1] | RF0NL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|---------------|---------------|---------------|--------------|--------------|-----------|------------|
| Name | TEFLL [15:15] | TEFFL [14:14] | TEFWL [13:13] | TEFNL [12:12] | TFEL [11:11] | TCFL [10:10] | TCL [9:9] | HPML [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|
| Name | EPL [23:23] | ELOL [22:22] | BEUL [21:21] | BECL [20:20] | DRXL [19:19] | TOOL [18:18] | MRAFL [17:17] | TSWL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|--------------|--------------|--------------|--------------|-------------|-------------|
| Name | None [31:30] | | ARAL [29:29] | PEDL [28:28] | PEAL [27:27] | WDIL [26:26] | BOL [25:25] | EWL [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0 | RF0NL | RW | R | 0 | Rx FIFO 0 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 1 | RF0WL | RW | R | 0 | Rx FIFO 0 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 2 | RF0FL | RW | R | 0 | Rx FIFO 0 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 3 | RF0LL | RW | R | 0 | Rx FIFO 0 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 4 | RF1NL | RW | R | 0 | Rx FIFO 1 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 5 | RF1WL | RW | R | 0 | Rx FIFO 1 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 6 | RF1FL | RW | R | 0 | Rx FIFO 1 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 7 | RF1LL | RW | R | 0 | Rx FIFO 1 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 8 | HPML | RW | R | 0 | High Priority Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 9 | TCL | RW | R | 0 | Transmission Completed Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 10 | TCFL | RW | R | 0 | Transmission Cancellation Finished Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 11 | TFEL | RW | R | 0 | Tx FIFO Empty Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 12 | TEFNL | RW | R | 0 | Tx Event FIFO New Entry Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 13 | TEFWL | RW | R | 0 | Tx Event FIFO Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 14 | TEFFL | RW | R | 0 | Tx Event FIFO Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 15 | TEFLL | RW | R | 0 | Tx Event FIFO Event Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 16 | TSWL | RW | R | 0 | Timestamp Wraparound Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 17 | MRAFL | RW | R | 0 | Message RAM Access Failure Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 18 | TOOL | RW | R | 0 | Timeout Occurred Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 19 | DRXL | RW | R | 0 | Message stored to Dedicated Rx Buffer Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 20 | BECL | RW | R | 0 | Bit Error Corrected Interrupt Select (not used in M_TTCAN) 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 21 | BEUL | RW | R | 0 | Bit Error Uncorrected Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 22 | ELOL | RW | R | 0 | Error Logging Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 23 | EPL | RW | R | 0 | Error Passive Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 24 | EWL | RW | R | 0 | Warning Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 25 | BOL | RW | R | 0 | Bus_Off Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 26 | WDIL | RW | R | 0 | Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 27 | PEAL | RW | R | 0 | Protocol Error in Arbitration Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 28 | PEDL | RW | R | 0 | Protocol Error in Data Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 29 | ARAL | RW | R | 0 | Access to Reserved Address Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |

2.3.9.6.18 CANFD_CH_ILE

Description: Interrupt Line Enable
Address: 0x4052005C
Offset: 0x5C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-------------|-------------|
| Name | None [7:2] | | | | | | EINT1 [1:1] | EINT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0 | EINT0 | RW | R | 0 | Enable Interrupt Line 0 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled |
| 1 | EINT1 | RW | R | 0 | Enable Interrupt Line 1 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled |

2.3.9.6.19 CANFD_CH_GFC

Description: Global Filter Configuration
Address: 0x40520080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------|---|------------|---|------------|------------|
| Name | None [7:6] | | ANFS [5:4] | | ANFE [3:2] | | RRFS [1:1] | RRFE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | RRFE | RW | R | 0 | Reject Remote Frames Extended 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs |
| 1 | RRFS | RW | R | 0 | Reject Remote Frames Standard 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs |
| 2:3 | ANFE | RW | R | 0 | Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject |
| 4:5 | ANFS | RW | R | 0 | Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject |

2.3.9.6.20 CANFD_CH_SIDFC

Description: Standard ID Filter Configuration
Address: 0x40520084
Offset: 0x84
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | FLSSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | LSS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 2:15 | FLSSA | RW | R | 0 | Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Figure 2). |
| 16:23 | LSS | RW | R | 0 | List Size Standard 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements 128= Values greater than 128 are interpreted as 128 |

2.3.9.6.21 CANFD_CH_XIDFC

Description: Extended ID Filter Configuration
Address: 0x40520088
Offset: 0x88
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | FLESA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------|----|----|----|----|----|----|
| Name | None [23:23] | LSE [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 2:15 | FLESA | RW | R | 0 | Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Figure 2). |
| 16:22 | LSE | RW | R | 0 | List Size Extended 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements 64= Values greater than 64 are interpreted as 64 |

2.3.9.6.22 CANFD_CH_XIDAM

Description: Extended ID AND Mask
Address: 0x40520090
Offset: 0x90
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x1FFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|--------------|----|----|----|----|
| Name | EIDM [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | EIDM [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | EIDM [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:29] | | | EIDM [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:28 | EIDM | RW | R | 536870911 | Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. |

2.3.9.6.23 CANFD_CH_HPMS

Description: High Priority Message Status
Address: 0x40520094
Offset: 0x94
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|------------|---|---|---|---|---|
| Name | MSI [7:6] | | BIDX [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-------------|----|----|----|----|---|---|
| Name | FLST [15:15] | FIDX [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:5 | BIDX | R | RW | 0 | Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. |
| 6:7 | MSI | R | RW | 0 | Message Storage Indicator 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1 |
| 8:14 | FIDX | R | RW | 0 | Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. |
| 15 | FLST | R | RW | 0 | Filter List Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List |

2.3.9.6.24 CANFD_CH_NDAT1

Description: New Data 1
Address: 0x40520098
Offset: 0x98
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----|----|----|----|----|----|----|
| Name | ND [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | ND [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | ND [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ND [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:31 | ND | RW1C | RW | 0 | New Data The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message |

2.3.9.6.25 CANFD_CH_NDAT2

Description: New Data 2
Address: 0x4052009C
Offset: 0x9C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----|----|----|----|----|----|----|
| Name | ND [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | ND [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | ND [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ND [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:31 | ND | RW1C | RW | 0 | New Data The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message |

2.3.9.6.26 CANFD_CH_RXF0C

Description: Rx FIFO 0 Configuration
Address: 0x405200A0
Offset: 0xA0
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | F0SA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------|----|----|----|----|----|----|
| Name | None [23:23] | F0S [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------|----|----|----|----|----|----|
| Name | F0OM [31:31] | F0WM [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|---|
| 2:15 | F0SA | RW | R | 0 | Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Figure 2). |
| 16:22 | F0S | RW | R | 0 | Rx FIFO 0 Size 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1 |
| 24:30 | F0WM | RW | R | 0 | Rx FIFO 0 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) 64= Watermark interrupt disabled |
| 31 | F0OM | RW | R | 0 | FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode |

2.3.9.6.27 CANFD_CH_RXF0S

Description: Rx FIFO 0 Status
Address: 0x405200A4
Offset: 0xA4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|--------------|----|----|----|--------------|-------------|
| Name | None [7:7] | | F0FL [6:0] | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:14] | | F0GI [13:8] | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:22] | | F0PI [21:16] | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:26] | | | | | | RF0L [25:25] | F0F [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|---|
| 0:6 | F0FL | R | RW | 0 | Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. |
| 8:13 | F0GI | R | RW | 0 | Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI |
| 16:21 | F0PI | R | RW | 0 | Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. |
| 24 | F0F | R | RW | 0 | Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full |
| 25 | RF0L | R | RW | 0 | Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero |

2.3.9.6.28 CANFD_CH_RXF0A

Description: Rx FIFO 0 Acknowledge
Address: 0x405200A8
Offset: 0xA8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------|---|---|---|---|---|
| Name | None [7:6] | | F0AI [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:5 | F0AI | RW | A | 0 | Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. |

2.3.9.6.29 CANFD_CH_RXBC

Description: Rx Buffer Configuration
Address: 0x405200AC
Offset: 0xAC
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | RBSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 2:15 | RBSA | RW | R | 0 | Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C. |

2.3.9.6.30 CANFD_CH_RXF1C

Description: Rx FIFO 1 Configuration
Address: 0x405200B0
Offset: 0xB0
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | F1SA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------|----|----|----|----|----|----|
| Name | None [23:23] | F1S [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------|----|----|----|----|----|----|
| Name | F1OM [31:31] | F1WM [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|---|
| 2:15 | F1SA | RW | R | 0 | Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Figure 2). |
| 16:22 | F1S | RW | R | 0 | Rx FIFO 1 Size 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1 |
| 24:30 | F1WM | RW | R | 0 | Rx FIFO 1 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) 64= Watermark interrupt disabled |
| 31 | F1OM | RW | R | 0 | FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode |

2.3.9.6.31 CANFD_CH_RXF1S

Description: Rx FIFO 1 Status
Address: 0x405200B4
Offset: 0xB4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|------------|--------------|----|----|----|--------------|-------------|
| Name | None [7:7] | F1FL [6:0] | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:14] | | F1GI [13:8] | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:22] | | F1PI [21:16] | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DMS [31:30] | | None [29:26] | | | | RF1L [25:25] | F1F [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|---|
| 0:6 | F1FL | R | RW | 0 | Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. |
| 8:13 | F1GI | R | RW | 0 | Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI |
| 16:21 | F1PI | R | RW | 0 | Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. |
| 24 | F1F | R | RW | 0 | Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full |
| 25 | RF1L | R | RW | 0 | Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero |
| 30:31 | DMS | R | RW | 0 | Debug Message Status 00= Idle state, wait for reception of debug messages, DMA request is cleared 01= Debug message A received 10= Debug messages A, B received 11= Debug messages A, B, C received, DMA request is set |

2.3.9.6.32 CANFD_CH_RXF1A

Description: Rx FIFO 1 Acknowledge
Address: 0x405200B8
Offset: 0xB8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------|---|---|---|---|---|
| Name | None [7:6] | | F1AI [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:5 | F1AI | RW | A | 0 | Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. |

2.3.9.6.33 CANFD_CH_RXESC

Description: Rx Buffer / FIFO Element Size Configuration
Address: 0x405200BC
Offset: 0xBC
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|---|---|------------|------------|---|---|
| Name | None [7:7] | F1DS [6:4] | | | None [3:3] | F0DS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|-------------|---|---|
| Name | None [15:11] | | | | | RBDS [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:2 | F0DS | RW | R | 0 | Rx FIFO 0 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field |
| 4:6 | F1DS | RW | R | 0 | Rx FIFO 1 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field |
| 8:10 | RBDS | RW | R | 0 | Rx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field |

2.3.9.6.34 CANFD_CH_TXBC

Description: Tx Buffer Configuration
Address: 0x405200C0
Offset: 0xC0
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | TBSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|--------------|----|----|----|----|----|
| Name | None [23:22] | | NDTB [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------|--------------|----|----|----|----|----|
| Name | None [31:31] | TFQM [30:30] | TFQS [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 2:15 | TBSA | RW | R | 0 | Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 2). |
| 16:21 | NDTB | RW | R | 0 | Number of Dedicated Transmit Buffers 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers 32= Values greater than 32 are interpreted as 32 |
| 24:29 | TFQS | RW | R | 0 | Transmit FIFO/Queue Size 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue 32= Values greater than 32 are interpreted as 32 |
| 30 | TFQM | RW | R | 0 | Tx FIFO/Queue Mode 0= Tx FIFO operation 1= Tx Queue operation |

2.3.9.6.35 CANFD_CH_TXFQS

Description: Tx FIFO/Queue Status
Address: 0x405200C4
Offset: 0xC4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------|---|---|---|---|---|
| Name | None [7:6] | | TFFL [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------|----|----|---|---|
| Name | None [15:13] | | | TFGI [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|--------------|---------------|----|----|----|----|
| Name | None [23:22] | | TFQF [21:21] | TFQPI [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 0:5 | TFFL | R | RW | 0 | Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') |
| 8:12 | TFGI | R | RW | 0 | Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1'). |
| 16:20 | TFQPI | R | RW | 0 | Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. |
| 21 | TFQF | R | RW | 0 | Tx FIFO/Queue Full 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full |

2.3.9.6.36 CANFD_CH_TXESC

Description: Tx Buffer Element Size Configuration
Address: 0x405200C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|------------|---|---|
| Name | None [7:3] | | | | | TBDS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:2 | TBDS | RW | R | 0 | Tx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field |

2.3.9.6.37 CANFD_CH_TXBRP

Description: Tx Buffer Request Pending
Address: 0x405200CC
Offset: 0xCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TRP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TRP [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TRP [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TRP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | TRP | R | RW | 0 | <p>Transmission Request Pending</p> <p>Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR.</p> <p>TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (see Section 3.5, Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset.</p> <p>After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission</p> <p>In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions.</p> <p>0= No transmission request pending 1= Transmission request pending</p> |

2.3.9.6.38 CANFD_CH_TXBAR

Description: Tx Buffer Add Request
Address: 0x405200D0
Offset: 0xD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----|----|----|----|----|----|----|
| Name | AR [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | AR [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | AR [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | AR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | AR | RW | RW | 0 | Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added |

2.3.9.6.39 CANFD_CH_TXBCR

Description: Tx Buffer Cancellation Request
Address: 0x405200D4
Offset: 0xD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | CR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | CR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | CR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | CR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | CR | RW | R | 0 | Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending |

2.3.9.6.40 CANFD_CH_TXBTO

Description: Tx Buffer Transmission Occurred
Address: 0x405200D8
Offset: 0xD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | TO [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | TO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | TO [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | TO [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | TO | R | RW | 0 | Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred |

2.3.9.6.41 CANFD_CH_TXBCF

Description: Tx Buffer Cancellation Finished
Address: 0x405200DC
Offset: 0xDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | CF [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | CF [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | CF [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | CF [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CF | R | RW | 0 | Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished |

2.3.9.6.42 CANFD_CH_TXBTIE

Description: Tx Buffer Transmission Interrupt Enable
Address: 0x405200E0
Offset: 0xE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | TIE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | TIE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TIE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TIE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | TIE | RW | R | 0 | Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable |

2.3.9.6.43 CANFD_CH_TXBCIE

Description: Tx Buffer Cancellation Finished Interrupt Enable
Address: 0x405200E4
Offset: 0xE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | CFIE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CFIE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CFIE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CFIE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CFIE | RW | R | 0 | Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled |

2.3.9.6.44 CANFD_CH_TXEFC

Description: Tx Event FIFO Configuration
Address: 0x405200F0
Offset: 0xF0
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | EFSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|-------------|----|----|----|----|----|
| Name | None [23:22] | | EFS [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|--------------|----|----|----|----|----|
| Name | None [31:30] | | EFWM [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 2:15 | EFSA | RW | R | 0 | Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 2). |
| 16:21 | EFS | RW | R | 0 | Event FIFO Size 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements 32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1 |
| 24:29 | EFWM | RW | R | 0 | Event FIFO Watermark 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) 32= Watermark interrupt disabled |

2.3.9.6.45 CANFD_CH_TXEFS

Description: Tx Event FIFO Status
Address: 0x405200F4
Offset: 0xF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|------------|--------------|----|----|--------------|-------------|
| Name | None [7:6] | | EFFL [5:0] | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | EFGI [12:8] | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:21] | | | EFPI [20:16] | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:26] | | | | | | TEFL [25:25] | EFF [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:5 | EFFL | R | RW | 0 | Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. |
| 8:12 | EFGI | R | RW | 0 | Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. |
| 16:20 | EFPI | R | RW | 0 | Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. |
| 24 | EFF | R | RW | 0 | Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full |
| 25 | TEFL | R | RW | 0 | Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. |

2.3.9.6.46 CANFD_CH_TXEFA

Description: Tx Event FIFO Acknowledge
Address: 0x405200F8
Offset: 0xF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------|---|---|---|---|
| Name | None [7:5] | | | EFAI [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:4 | EFAI | RW | R | 0 | Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. |

2.3.9.6.47 CANFD_CH_TTTMC

Description: TT Trigger Memory Configuration
Address: 0x40520100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | TMSA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------|----|----|----|----|----|----|
| Name | None [23:23] | TME [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 2:15 | TMSA | RW | R | 0 | Trigger Memory Start Address Start address of Trigger Memory in Message RAM (32-bit word address, see Figure 2). |
| 16:22 | TME | RW | R | 0 | Trigger Memory Elements 0= No Trigger Memory 1-64= Number of Trigger Memory elements 64= Values greater than 64 are interpreted as 64 |

2.3.9.6.48 CANFD_CH_TTRMC

Description: TT Reference Message Configuration
Address: 0x40520104
Offset: 0x104
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|-------------|--------------|-------------|----|----|----|----|
| Name | RID [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | RID [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | RID [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | RMPS [31:31] | XTD [30:30] | None [29:29] | RID [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:28 | RID | RW | R | 0 | Reference Identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. |
| 30 | XTD | RW | R | 0 | Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier |
| 31 | RMPS | RW | R | 0 | Reference Message Payload Select Ignored in case of time slaves. 0= Reference message has no additional payload 1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB Level 1: bytes 2-8, Level 0,2: bytes 5-8) |

2.3.9.6.49 CANFD_CH_TTOCF

Description: TT Operation Configuration
Address: 0x40520108
Offset: 0x108
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x10000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|----------|-----------|------------|----------|---|
| Name | LDSDL [7:5] | | | TM [4:4] | GEN [3:3] | None [2:2] | OM [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-------------|----|----|----|----|---|---|
| Name | EECS [15:15] | IRTO [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | AWL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|--------------|-------------|--------------|
| Name | None [31:27] | | | | | EVTP [26:26] | ECC [25:25] | EGTF [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:1 | OM | RW | R | 0 | Operation Mode 00= Event-driven CAN communication, default 01= TTCAN level 1 10= TTCAN level 2 11= TTCAN level 0 |
| 3 | GEN | RW | R | 0 | Gap Enable 0= Strictly time-triggered operation 1= External event-synchronized time-triggered operation |
| 4 | TM | RW | R | 0 | Time Master 0= Time Master function disabled 1= Potential Time Master |
| 5:7 | LDSDL | RW | R | 0 | LD of Synchronization Deviation Limit The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with $SDL = 2(LDSDL + 5)$. It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7 LD of Synchronization Deviation Limit ($SDL \leq 32 \dots 4096$) |
| 8:14 | IRTO | RW | R | 0 | Initial Reference Trigger Offset 0x00-7F Positive offset, range from 0 to 127 |
| 15 | EECS | RW | R | 0 | Enable External Clock Synchronization If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. 0= External clock synchronization in TTCAN Level 0,2 disabled 1= External clock synchronization in TTCAN Level 0,2 enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 16:23 | AWL | RW | R | 1 | Application Watchdog Limit The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. |
| 24 | EGTF | RW | R | 0 | Enable Global Time Filtering 0= Global time filtering in TTCAN Level 0,2 is disabled 1= Global time filtering in TTCAN Level 0,2 is enabled |
| 25 | ECC | RW | R | 0 | Enable Clock Calibration 0= Automatic clock calibration in TTCAN Level 0,2 is disabled 1= Automatic clock calibration in TTCAN Level 0,2 is enabled |
| 26 | EVTP | RW | R | 0 | Event Trigger Polarity 0= Rising edge trigger 1= Falling edge trigger |

2.3.9.6.50 CANFD_CH_TTLM

Description: TT Matrix Limits
Address: 0x4052010C
Offset: 0x10C
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|-----------|----|--------------|----|----|----|
| Name | CSS [7:6] | | CCM [5:0] | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | TXEW [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | ENTT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:28] | | | | ENTT [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:5 | CCM | RW | R | 0 | Cycle Count Max 0x00 1 Basic Cycle per Matrix Cycle 0x01 2 Basic Cycles per Matrix Cycle 0x03 4 Basic Cycles per Matrix Cycle 0x07 8 Basic Cycles per Matrix Cycle 0x0F 16 Basic Cycles per Matrix Cycle 0x1F 32 Basic Cycles per Matrix Cycle 0x3F 64 Basic Cycles per Matrix Cycle others Reserved |
| 6:7 | CSS | RW | R | 0 | Cycle Start Synchronization Enables sync pulse output at pin m_ttcan_soc. 00= No sync pulse 01= Sync pulse at start of basic cycle 10= Sync pulse at start of matrix cycle 11= Reserved |
| 8:11 | TXEW | RW | R | 0 | Tx Enable Window 0x0-F Length of Tx enable window, 1-16 NTU cycles |
| 16:27 | ENTT | RW | R | 0 | Expected Number of Tx Triggers 0x000-FFF Expected number of Tx Triggers in one Matrix Cycle |

2.3.9.6.51 CANFD_CH_TURCF

Description: TUR Configuration
Address: 0x40520110
Offset: 0x110
Retention: Retained
IsDeepSleep: No
Comment: Protected Write.
Default: 0x10000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|--------------|------------|----|----|----|----|----|
| Name | NCL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | NCL [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DC [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ELT [31:31] | None [30:30] | DC [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:15 | NCL | RW | R | 0 | Numerator Configuration Low Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'. 0x0000-FFFF Numerator Configuration Low |
| 16:29 | DC | RW | R | 4096 | Denominator Configuration 0x0000 Illegal value 0x0001-3FFF Denominator Configuration |
| 31 | ELT | RW | R | 0 | Enable Local Time 0= Local time is stopped, default 1= Local time is enabled |

2.3.9.6.52 CANFD_CH_TTOCN

Description: TT Operation Control
Address: 0x40520114
Offset: 0x114
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|------------|-----------|---|-----------|-----------|-----------|
| Name | TMC [7:6] | | RTIE [5:5] | SWS [4:3] | | SWP [2:2] | ECS [1:1] | SGT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|--------------|--------------|-------------|-------------|-------------|-----------|------------|
| Name | LCKC [15:15] | None [14:14] | ESCN [13:13] | NIG [12:12] | TMG [11:11] | FGP [10:10] | GCS [9:9] | TTIE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | SGT | RW | R | 0 | Set Global time Writing a '1' to SGT sets TOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. |
| 1 | ECS | RW | R | 0 | External Clock Synchronization Writing a '1' to ECS sets TOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. |
| 2 | SWP | RW | R | 0 | Stop Watch Polarity 0= Rising edge trigger 1= Falling edge trigger |
| 3:4 | SWS | RW | R | 0 | Stop Watch Source 00= Stop Watch disabled 01= Actual value of cycle time is copied to TTCPT.SWV 10= Actual value of local time is copied to TTCPT.SWV 11= Actual value of global time is copied to TTCPT.SWV |
| 5 | RTIE | RW | R | 0 | Register Time Mark Interrupt Pulse Enable Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Register Time Mark Interrupt output m_tcan_rtp disabled 1= Register Time Mark Interrupt output m_tcan_rtp enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 6:7 | TMC | RW | R | 0 | Register Time Mark Compare 00= No Register Time Mark Interrupt generated 01= Register Time Mark Interrupt if Time Mark = cycle time 10= Register Time Mark Interrupt if Time Mark = local time 11= Register Time Mark Interrupt if Time Mark = global time |
| 8 | TTIE | RW | R | 0 | Trigger Time Mark Interrupt Pulse Enable External time mark events are configured by trigger memory element TMEX (see Section 2.4.7). A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. 0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled 1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled |
| 9 | GCS | RW | R | 0 | Gap Control Select 0= Gap control independent from m_ttcan_evt 1= Gap control by input pin m_ttcan_evt |
| 10 | FGP | RW | R | 0 | Finish Gap Set by the CPU, reset by each reference message 0= No reference message requested 1= Application requested start of reference message |
| 11 | TMG | RW | R | 0 | Time Mark Gap 0= Reset by each reference message 1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated |
| 12 | NIG | RW | R | 0 | Next is Gap This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1') 0= No action, reset by reception of any reference message 1= Transmit next reference message with Next_is_Gap = '1' |
| 13 | ESCN | RW | R | 0 | External Synchronization Control If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt (see Section 4.11). 0= External synchronization disabled 1= External synchronization enabled |
| 15 | LCKC | R | RW | 0 | TT Operation Control Register Locked Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0= Write access to TTOCN enabled 1= Write access to TTOCN locked |

2.3.9.6.53 CANFD_CH_TTGTP

Description: TT Global Time Preset
Address: 0x40520118
Offset: 0x118
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | TP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | TP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | CTP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | CTP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:15 | TP | RW | R | 0 | Time Preset TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP 0x8000 reserved 0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) |
| 16:31 | CTP | RW | R | 0 | Cycle Time Target Phase CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set (see Section 4.11). 0x0000-FFFF Defines target value of cycle time when a rising edge of m_tcan_evt is expected |

2.3.9.6.54 CANFD_CH_TTTMK

Description: TT Time Mark
Address: 0x4052011C
Offset: 0x11C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|--------------|----|----|----|----|----|----|
| Name | TM_ [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TM_ [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:23] | TICC [22:16] | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | LCKM [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:15 | TM_ | RW | R | 0 | Time Mark 0x0000-FFFF Time Mark |
| 16:22 | TICC | RW | R | 0 | Time Mark Cycle Code Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = ccccccc |
| 31 | LCKM | R | RW | 0 | TT Time Mark Register Locked Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain. 0= Write access to TTTMK enabled 1= Write access to TTTMK locked |

2.3.9.6.55 CANFD_CH_TTIR

Description: TT Interrupt Register
Address: 0x40520120
Offset: 0x120
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|-----------|------------|------------|-----------|------------|-----------|-----------|
| Name | GTW [7:7] | SWE [6:6] | TTMI [5:5] | RTMI [4:4] | SOG [3:3] | CSM_ [2:2] | SMC [1:1] | SBC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|-------------|-------------|-------------|-------------|-------------|-----------|-----------|
| Name | IWT [15:15] | ELC [14:14] | SE2 [13:13] | SE1 [12:12] | TXO [11:11] | TXU [10:10] | GTE [9:9] | GTD [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|-------------|------------|------------|
| Name | None [23:19] | | | | | CER [18:18] | AW [17:17] | WT [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0 | SBC | RW1C | RW | 0 | Start of Basic Cycle 0= No Basic Cycle started since bit has been reset 1= Basic Cycle started |
| 1 | SMC | RW1C | RW | 0 | Start of Matrix Cycle 0= No Matrix Cycle started since bit has been reset 1= Matrix Cycle started |
| 2 | CSM_ | RW1C | RW | 0 | Change of Synchronization Mode 0= No change in master to slave relation or schedule synchronization 1= Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset |
| 3 | SOG | RW1C | RW | 0 | Start of Gap 0= No reference message seen with Next_is_Gap bit set 1= Reference message with Next_is_Gap bit set becomes valid |
| 4 | RTMI | RW1C | RW | 0 | Register Time Mark Interrupt Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Time mark not reached 1= Time mark reached |
| 5 | TTMI | RW1C | RW | 0 | Trigger Time Mark Event Internal Internal time mark events are configured by trigger memory element TMIN (see Section 2.4.7). Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. 0= Time mark not reached 1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 6 | SWE | RW1C | RW | 0 | Stop Watch Event 0= No rising/falling edge at stop watch trigger pin m_ttcn_swt detected 1= Rising/falling edge at stop watch trigger pin m_ttcn_swt detected |
| 7 | GTW | RW1C | RW | 0 | Global Time Wrap 0= No global time wrap occurred 1= Global time wrap from 0xFFFF to 0x0000 occurred |
| 8 | GTD | RW1C | RW | 0 | Global Time Discontinuity 0= No discontinuity of global time 1= Discontinuity of global time |
| 9 | GTE | RW1C | RW | 0 | Global Time Error Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. 0= Synchronization deviation within limit 1= Synchronization deviation exceeded limit |
| 10 | TXU | RW1C | RW | 0 | Tx Count Underflow 0= Number of Tx Trigger as expected 1= Less Tx trigger than expected in one matrix cycle |
| 11 | TXO | RW1C | RW | 0 | Tx Count Overflow 0= Number of Tx Trigger as expected 1= More Tx trigger than expected in one matrix cycle |
| 12 | SE1 | RW1C | RW | 0 | Scheduling Error 1 0= No scheduling error 1 1= Scheduling error 1 occurred |
| 13 | SE2 | RW1C | RW | 0 | Scheduling Error 2 0= No scheduling error 2 1= Scheduling error 2 occurred |
| 14 | ELC | RW1C | RW | 0 | Error Level Changed Not set when error level changed during initialization. 0= No change in error level 1= Error level changed |
| 15 | IWT | RW1C | RW | 0 | Initialization Watch Trigger The initialization is restarted by resetting IWT. 0= No missing reference message during system startup 1= No system startup due to missing reference message |
| 16 | WT | RW1C | RW | 0 | Watch Trigger 0= No missing reference message 1= Missing reference message (Level 0: cycle time 0xFF00) |
| 17 | AW | RW1C | RW | 0 | Application Watchdog 0= Application watchdog served in time 1= Application watchdog not served in time |
| 18 | CER | RW1C | RW | 0 | Configuration Error Trigger out of order. 0= No error found in trigger list 1= Error found in trigger list |

2.3.9.6.56 CANFD_CH_TTIE

Description: TT Interrupt Enable
Address: 0x40520124
Offset: 0x124
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|-------------|-------------|-------------|------------|------------|------------|
| Name | GTWE [7:7] | SWEE [6:6] | TTMIE [5:5] | RTMIE [4:4] | SOGIE [3:3] | CSME [2:2] | SMCE [1:1] | SBCE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|--------------|--------------|--------------|--------------|--------------|------------|------------|
| Name | IWTE [15:15] | ELCE [14:14] | SE2E [13:13] | SE1E [12:12] | TXOE [11:11] | TXUE [10:10] | GTEE [9:9] | GTDE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|--------------|--------------|-------------|
| Name | None [23:19] | | | | | CERE [18:18] | AWE_ [17:17] | WTE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0 | SBCE | RW | R | 0 | Start of Basic Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 1 | SMCE | RW | R | 0 | Start of Matrix Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 2 | CSME | RW | R | 0 | Change of Synchronization Mode Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 3 | SOGIE | RW | R | 0 | Start of Gap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 4 | RTMIE | RW | R | 0 | Register Time Mark Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 5 | TTMIE | RW | R | 0 | Trigger Time Mark Event Internal Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 6 | SWEE | RW | R | 0 | Stop Watch Event Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 7 | GTWE | RW | R | 0 | Global Time Wrap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 8 | GTDE | RW | R | 0 | Global Time Discontinuity Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 9 | GTEE | RW | R | 0 | Global Time Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 10 | TXUE | RW | R | 0 | Tx Count Underflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 11 | TXOE | RW | R | 0 | Tx Count Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 12 | SE1E | RW | R | 0 | Scheduling Error 1 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 13 | SE2E | RW | R | 0 | Scheduling Error 2 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 14 | ELCE | RW | R | 0 | Change Error Level Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 15 | IWTE | RW | R | 0 | Initialization Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 16 | WTE | RW | R | 0 | Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 17 | AWE_ | RW | R | 0 | Application Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |
| 18 | CERE | RW | R | 0 | Configuration Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled |

2.3.9.6.57 CANFD_CH_TTILS

Description: TT Interrupt Line Select

Address: 0x40520128

Offset: 0x128

Retention: Retained

IsDeepSleep: No

Comment: The TT Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the TT Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1. 0= TT interrupt assigned to interrupt line m_ttcan_int0 1= TT interrupt assigned to interrupt line m_ttcan_int1

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| Name | GTWL [7:7] | SWEL [6:6] | TTMIL [5:5] | RTMIL [4:4] | SOGL [3:3] | CSML [2:2] | SMCL [1:1] | SBCL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|--------------|--------------|--------------|--------------|--------------|------------|------------|
| Name | IWTL [15:15] | ELCL [14:14] | SE2L [13:13] | SE1L [12:12] | TXOL [11:11] | TXUL [10:10] | GTEL [9:9] | GTDL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|--------------|--------------|-------------|
| Name | None [23:19] | | | | | CERL [18:18] | AWL_ [17:17] | WTL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | SBCL | RW | R | 0 | Start of Basic Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 1 | SMCL | RW | R | 0 | Start of Matrix Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 2 | CSML | RW | R | 0 | Change of Synchronization Mode Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 3 | SOGL | RW | R | 0 | Start of Gap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 4 | RTMIL | RW | R | 0 | Register Time Mark Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 5 | TTMIL | RW | R | 0 | Trigger Time Mark Event Internal Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 6 | SWEL | RW | R | 0 | Stop Watch Event Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 7 | GTWL | RW | R | 0 | Global Time Wrap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 8 | GTDL | RW | R | 0 | Global Time Discontinuity Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 9 | GTEL | RW | R | 0 | Global Time Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 10 | TXUL | RW | R | 0 | Tx Count Underflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 11 | TXOL | RW | R | 0 | Tx Count Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 12 | SE1L | RW | R | 0 | Scheduling Error 1 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 13 | SE2L | RW | R | 0 | Scheduling Error 2 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 14 | ELCL | RW | R | 0 | Change Error Level Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 15 | IWTL | RW | R | 0 | Initialization Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 16 | WTL | RW | R | 0 | Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 17 | AWL_ | RW | R | 0 | Application Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |
| 18 | CERL | RW | R | 0 | Configuration Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 |

2.3.9.6.58 CANFD_CH_TTOST

Description: TT Operation Status
Address: 0x4052012C
Offset: 0x12C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|------------|-----------|---|----------|---|----------|---|
| Name | QCS [7:7] | QGTP [6:6] | SYS [5:4] | | MS [3:2] | | EL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | RTO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|--------------|--------------|----|----|----|----|----|
| Name | GFI [23:23] | WGTD [22:22] | None [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|--------------|-------------|-------------|-------------|-------------|----|----|
| Name | SPL [31:31] | WECS [30:30] | AWE [29:29] | WFE [28:28] | GSI [27:27] | TMP [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:1 | EL | R | RW | 0 | Error Level 00= Severity 0 - No Error 01= Severity 1 - Warning 10= Severity 2 - Error 11= Severity 3 - Severe Error |
| 2:3 | MS | R | RW | 0 | Master State 00= Master_Off, no master properties relevant 01= Operating as Time Slave 10= Operating as Backup Time Master 11= Operating as current Time Master |
| 4:5 | SYS | R | RW | 0 | Synchronization State 00= Out of Synchronization 01= Synchronizing to TTCAN communication 10= Schedule suspended by Gap (In_Gap) 11= Synchronized to schedule (In_Schedule) |
| 6 | QGTP | R | RW | 0 | Quality of Global Time Phase Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'. 0= Global time not valid 1= Global time in phase with Time Master |
| 7 | QCS | R | RW | 0 | Quality of Clock Speed Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'. 0= Local clock speed not synchronized to Time Master clock speed 1= Synchronization Deviation <= SDL |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 8:15 | RTO | R | RW | 0 | Reference Trigger Offset The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF Actual Reference Trigger offset value |
| 22 | WGTD | R | RW | 0 | Wait for Global Time Discontinuity 0= No global time preset pending 1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. |
| 23 | GFI | R | RW | 0 | Gap Finished Indicator Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcn_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0= Reset at the end of each reference message 1= Gap finished by M_TTCAN |
| 24:26 | TMP | R | RW | 0 | Time Master Priority 0x0-7 Priority of actual Time Master |
| 27 | GSI | R | RW | 0 | Gap Started Indicator 0= No Gap in schedule, reset by each reference message and for all time slaves 1= Gap time after Basic Cycle has started |
| 28 | WFE | R | RW | 0 | Wait for Event 0= No Gap announced, reset by a reference message with Next_is_Gap = '0' 1= Reference message with Next_is_Gap = '1' received |
| 29 | AWE | R | RW | 0 | Application Watchdog Event The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. 0= Application Watchdog served in time 1= Failed to serve Application Watchdog in time |
| 30 | WECS | R | RW | 0 | Wait for External Clock Synchronization 0= No external clock synchronization pending 1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. |
| 31 | SPL | R | RW | 0 | Schedule Phase Lock The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcn_evt is less or equal 9 NTU (see Section 4.11). 0= Phase outside range 1= Phase inside range |

2.3.9.6.59 CANFD_CH_TURNA

Description: TUR Numerator Actual
Address: 0x40520130
Offset: 0x130
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|-------------|----|
| Name | NAV [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | NAV [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:18] | | | | | | NAV [17:16] | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:17 | NAV | R | RW | 65536 | Numerator Actual Value 0x0EFFF reserved 0x0F000-20FFF Actual numerator value 0x21000 reserved |

2.3.9.6.60 CANFD_CH_TTLGT

Description: TT Local & Global Time
Address: 0x40520134
Offset: 0x134
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----|----|----|----|----|----|----|
| Name | LT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | LT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | GT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | GT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:15 | LT | R | RW | 0 | Local Time Non-fractional part of local time, incremented once each local NTU (see Section 4.5). 0x0000-FFFF Local time value of TTCAN node |
| 16:31 | GT | R | RW | 0 | Global Time Non-fractional part of the sum of the node's local time and its local offset (see Section 4.5). 0x0000-FFFF Global time value of TTCAN network |

2.3.9.6.61 CANFD_CH_TTCTC

Description: TT Cycle Time & Count
Address: 0x40520138
Offset: 0x138
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3F0000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|------------|----|----|----|----|----|
| Name | CT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:22] | | CC [21:16] | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|---|
| 0:15 | CT | R | RW | 0 | Cycle Time Non-fractional part of the difference of the node's local time and Ref_Mark (see Section 4.5). 0x0000-FFFF Cycle time value of TTCAN Basic Cycle |
| 16:21 | CC | R | RW | 63 | Cycle Count 0x00-3F Number of actual Basic Cycle in the System Matrix |

2.3.9.6.62 CANFD_CH_TTCPT

Description: TT Capture Time
Address: 0x4052013C
Offset: 0x13C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|-----------|---|---|---|---|---|
| Name | None [7:6] | | CCV [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | SWV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | SWV [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:5 | CCV | R | RW | 0 | Cycle Count Value Cycle count value captured together with SWV. 0x00-3F Captured cycle count value |
| 16:31 | SWV | R | RW | 0 | Stop Watch Value On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF Captured Stop Watch value |

2.3.9.6.63 CANFD_CH_TTCSM

Description: TT Cycle Sync Mark
Address: 0x40520140
Offset: 0x140
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | CSM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | CSM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:15 | CSM | R | RW | 0 | Cycle Sync Mark The Cycle Sync Mark is measured |

3 CM0P

| | |
|---------------------|-------------------------------|
| Description | Cortex-M0+ specific registers |
| Base Address | 0xE0000000 |
| Size | 0x20000000 |
| Slave Num | SYSTEM |

3.1 DWT

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--|
| CM0P_DWT_DWT_CTRL | 0xE0001000 | FULL | Watchpoint Comparator Configuration |
| CM0P_DWT_DWT_PCSR | 0xE000101C | FULL | Watchpoint Comparator PC Sample |
| CM0P_DWT_DWT_COMP0 | 0xE0001020 | FULL | Watchpoint Comparator Compare Value |
| CM0P_DWT_DWT_MASK0 | 0xE0001024 | FULL | Watchpoint Comparator Mask |
| CM0P_DWT_DWT_FUNCTION0 | 0xE0001028 | FULL | Watchpoint Comparator Function |
| CM0P_DWT_DWT_COMP1 | 0xE0001030 | FULL | Watchpoint Comparator Compare Value |
| CM0P_DWT_DWT_MASK1 | 0xE0001034 | FULL | Watchpoint Comparator Mask |
| CM0P_DWT_DWT_FUNCTION1 | 0xE0001038 | FULL | Watchpoint Comparator Function |
| CM0P_DWT_DWT_PID4 | 0xE0001FD0 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #4 |
| CM0P_DWT_DWT_PID0 | 0xE0001FE0 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #0 |
| CM0P_DWT_DWT_PID1 | 0xE0001FE4 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #1 |
| CM0P_DWT_DWT_PID2 | 0xE0001FE8 | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #2 |
| CM0P_DWT_DWT_PID3 | 0xE0001FEC | FULL | Watchpoint Unit CoreSight ROM Table Peripheral ID #3 |
| CM0P_DWT_DWT_CID0 | 0xE0001FF0 | FULL | Watchpoint Unit CoreSight ROM Table Component ID #0 |
| CM0P_DWT_DWT_CID1 | 0xE0001FF4 | FULL | Watchpoint Unit CoreSight ROM Table Component ID #1 |
| CM0P_DWT_DWT_CID2 | 0xE0001FF8 | FULL | Watchpoint Unit CoreSight ROM Table Component ID #2 |
| CM0P_DWT_DWT_CID3 | 0xE0001FFC | FULL | Watchpoint Unit CoreSight ROM Table Component ID #3 |

3.2 BP

| Register Name | Address | Permission | Description |
|------------------|------------|------------|--|
| CM0P_BP_BP_CTRL | 0xE0002000 | FULL | Breakpoint Unit Control |
| CM0P_BP_BP_COMP0 | 0xE0002008 | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_COMP1 | 0xE000200C | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_COMP2 | 0xE0002010 | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_COMP3 | 0xE0002014 | FULL | Breakpoint Compare Register |
| CM0P_BP_BP_PID4 | 0xE0002FD0 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #4 |
| CM0P_BP_BP_PID0 | 0xE0002FE0 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #0 |
| CM0P_BP_BP_PID1 | 0xE0002FE4 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #1 |
| CM0P_BP_BP_PID2 | 0xE0002FE8 | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #2 |
| CM0P_BP_BP_PID3 | 0xE0002FEC | FULL | Breakpoint Unit CoreSight ROM Table Peripheral ID #3 |
| CM0P_BP_BP_CID0 | 0xE0002FF0 | FULL | Breakpoint Unit CoreSight ROM Table Component ID #0 |
| CM0P_BP_BP_CID1 | 0xE0002FF4 | FULL | Breakpoint Unit CoreSight ROM Table Component ID #1 |
| CM0P_BP_BP_CID2 | 0xE0002FF8 | FULL | Breakpoint Unit CoreSight ROM Table Component ID #2 |
| CM0P_BP_BP_CID3 | 0xE0002FFC | FULL | Breakpoint Unit CoreSight ROM Table Component ID #3 |

3.3 SCS

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|--|
| CM0P_SCS_SYST_CSR | 0xE000E010 | FULL | SysTick Control & Status |
| CM0P_SCS_SYST_RVR | 0xE000E014 | FULL | SysTick Reload Value |
| CM0P_SCS_SYST_CVR | 0xE000E018 | FULL | SysTick Current Value |
| CM0P_SCS_SYST_CALIB | 0xE000E01C | FULL | SysTick Calibration Value |
| CM0P_SCS_ISER | 0xE000E100 | FULL | Interrupt Set-Enable Register |
| CM0P_SCS_ICER | 0xE000E180 | FULL | Interrupt Clear Enable Register |
| CM0P_SCS_ISPR | 0xE000E200 | FULL | Interrupt Set-Pending Register |
| CM0P_SCS_ICPR | 0xE000E280 | FULL | Interrupt Clear-Pending Register |
| CM0P_SCS_IPR0 | 0xE000E400 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR1 | 0xE000E404 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR2 | 0xE000E408 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR3 | 0xE000E40C | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR4 | 0xE000E410 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR5 | 0xE000E414 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR6 | 0xE000E418 | FULL | Interrupt Priority Registers |
| CM0P_SCS_IPR7 | 0xE000E41C | FULL | Interrupt Priority Registers |
| CM0P_SCS_CPUID | 0xE000ED00 | FULL | CPUID Register |
| CM0P_SCS_ICSR | 0xE000ED04 | FULL | Interrupt Control State Register |
| CM0P_SCS_VTOR | 0xE000ED08 | FULL | Vector Table Offset Register |
| CM0P_SCS_AIRCR | 0xE000ED0C | FULL | Application Interrupt and Reset Control Register |
| CM0P_SCS_SCR | 0xE000ED10 | FULL | System Control Register |
| CM0P_SCS_CCR | 0xE000ED14 | FULL | Configuration and Control Register |
| CM0P_SCS_SHPR2 | 0xE000ED1C | FULL | System Handler Priority Register 2 |
| CM0P_SCS_SHPR3 | 0xE000ED20 | FULL | System Handler Priority Register 3 |
| CM0P_SCS_SHCSR | 0xE000ED24 | FULL | System Handler Control and State Register |
| CM0P_SCS_DFSR | 0xE000ED30 | FULL | Debug Fault Status Register |
| CM0P_SCS_MPU_TYPE | 0xE000ED90 | FULL | MPU Type Register |
| CM0P_SCS_MPU_CTRL | 0xE000ED94 | FULL | MPU Control Register |
| CM0P_SCS_MPU_RNR | 0xE000ED98 | FULL | MPU Region Number Register |
| CM0P_SCS_MPU_RBAR | 0xE000ED9C | FULL | MPU Region Base Address Register |
| CM0P_SCS_MPU_RASR | 0xE000EDA0 | FULL | MPU Region Attribute and Size Register |
| CM0P_SCS_DHCSR | 0xE000EDF0 | FULL | Debug Halting Control and Status Register |
| CM0P_SCS_DCRSR | 0xE000EDF4 | FULL | Debug Core Register Selector Register |
| CM0P_SCS_DCRDR | 0xE000EDF8 | FULL | Debug Core Register Data Register |
| CM0P_SCS_DEMCR | 0xE000EDFC | FULL | Debug Exception and Monitor Control Register |
| CM0P_SCS_SCS_PID4 | 0xE000EFD0 | FULL | System Control Space ROM Table Peripheral ID #4 |
| CM0P_SCS_SCS_PID0 | 0xE000EFE0 | FULL | System Control Space ROM Table Peripheral ID #0 |
| CM0P_SCS_SCS_PID1 | 0xE000EFE4 | FULL | System Control Space ROM Table Peripheral ID #1 |
| CM0P_SCS_SCS_PID2 | 0xE000EFE8 | FULL | System Control Space ROM Table Peripheral ID #2 |
| CM0P_SCS_SCS_PID3 | 0xE000EFEC | FULL | System Control Space ROM Table Peripheral ID #3 |
| CM0P_SCS_SCS_CID0 | 0xE000EFF0 | FULL | System Control Space ROM Table Component ID #0 |
| CM0P_SCS_SCS_CID1 | 0xE000EFF4 | FULL | System Control Space ROM Table Component ID #1 |
| CM0P_SCS_SCS_CID2 | 0xE000EFF8 | FULL | System Control Space ROM Table Component ID #2 |
| CM0P_SCS_SCS_CID3 | 0xE000EFFC | FULL | System Control Space ROM Table Component ID #3 |

3.4 ROM

| Register Name | Address | Permission | Description |
|------------------|------------|------------|--|
| CM0P_ROM_ROM_SCS | 0xE00FF000 | FULL | CM0+ CoreSight ROM Table Peripheral #0 |
| CM0P_ROM_ROM_DWT | 0xE00FF004 | FULL | CM0+ CoreSight ROM Table Peripheral #1 |
| CM0P_ROM_ROM_BPU | 0xE00FF008 | FULL | CM0+ CoreSight ROM Table Peripheral #2 |
| CM0P_ROM_ROM_END | 0xE00FF00C | FULL | CM0+ CoreSight ROM Table End Marker |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|---|
| CM0P_ROM_ROM_CSMT | 0xE00FFFC0 | FULL | CM0+ CoreSight ROM Table Memory Type |
| CM0P_ROM_ROM_PID4 | 0xE00FFFD0 | FULL | CM0+ CoreSight ROM Table Peripheral ID #4 |
| CM0P_ROM_ROM_PID0 | 0xE00FFFE0 | FULL | CM0+ CoreSight ROM Table Peripheral ID #0 |
| CM0P_ROM_ROM_PID1 | 0xE00FFFE4 | FULL | CM0+ CoreSight ROM Table Peripheral ID #1 |
| CM0P_ROM_ROM_PID2 | 0xE00FFFE8 | FULL | CM0+ CoreSight ROM Table Peripheral ID #2 |
| CM0P_ROM_ROM_PID3 | 0xE00FFFE0 | FULL | CM0+ CoreSight ROM Table Peripheral ID #3 |
| CM0P_ROM_ROM_CID0 | 0xE00FFFF0 | FULL | CM0+ CoreSight ROM Table Component ID #0 |
| CM0P_ROM_ROM_CID1 | 0xE00FFFF4 | FULL | CM0+ CoreSight ROM Table Component ID #1 |
| CM0P_ROM_ROM_CID2 | 0xE00FFFF8 | FULL | CM0+ CoreSight ROM Table Component ID #2 |
| CM0P_ROM_ROM_CID3 | 0xE00FFFFC | FULL | CM0+ CoreSight ROM Table Component ID #3 |

3.5 ROMTABLE

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|---------------------------------------|
| CM0P_ROMTABLE_ADDR0 | 0xF0000000 | FULL | Link to Cortex M0+ ROM Table. |
| CM0P_ROMTABLE_ADDR1 | 0xF0000004 | FULL | Link to CoreSight CTI Table. |
| CM0P_ROMTABLE_ADDR2 | 0xF0000008 | FULL | Link to Cortex M0+ MTB Table. |
| CM0P_ROMTABLE_DID | 0xF0000FCC | FULL | Device Type Identifier register. |
| CM0P_ROMTABLE_PID4 | 0xF0000FD0 | FULL | Peripheral Identification Register 4. |
| CM0P_ROMTABLE_PID5 | 0xF0000FD4 | FULL | Peripheral Identification Register 5. |
| CM0P_ROMTABLE_PID6 | 0xF0000FD8 | FULL | Peripheral Identification Register 6. |
| CM0P_ROMTABLE_PID7 | 0xF0000FDC | FULL | Peripheral Identification Register 7. |
| CM0P_ROMTABLE_PID0 | 0xF0000FE0 | FULL | Peripheral Identification Register 0. |
| CM0P_ROMTABLE_PID1 | 0xF0000FE4 | FULL | Peripheral Identification Register 1. |
| CM0P_ROMTABLE_PID2 | 0xF0000FE8 | FULL | Peripheral Identification Register 2. |
| CM0P_ROMTABLE_PID3 | 0xF0000FEC | FULL | Peripheral Identification Register 3. |
| CM0P_ROMTABLE_CID0 | 0xF0000FF0 | FULL | Component Identification Register 0. |
| CM0P_ROMTABLE_CID1 | 0xF0000FF4 | FULL | Component Identification Register 1. |
| CM0P_ROMTABLE_CID2 | 0xF0000FF8 | FULL | Component Identification Register 2. |
| CM0P_ROMTABLE_CID3 | 0xF0000FFC | FULL | Component Identification Register 3. |

3.6 CTI

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| CM0P_CTI_CTLCONTROL | 0xF0002000 | FULL | CTI Control Register |
| CM0P_CTI_CTIINTACK | 0xF0002010 | FULL | CTI Interrupt Acknowledge Register |
| CM0P_CTI_CTIAPPSET | 0xF0002014 | FULL | CTI Application Trigger Set Register |
| CM0P_CTI_CTIAPPCLEAR | 0xF0002018 | FULL | CTI Application Trigger Clear Register |
| CM0P_CTI_CTIAPPULSE | 0xF000201C | FULL | CTI Application Pulse Register |
| CM0P_CTI_CTIENEN0 | 0xF0002020 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN1 | 0xF0002024 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN2 | 0xF0002028 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN3 | 0xF000202C | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN4 | 0xF0002030 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN5 | 0xF0002034 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN6 | 0xF0002038 | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIENEN7 | 0xF000203C | FULL | CTI Trigger to Channel Enable Registers |
| CM0P_CTI_CTIOUTEN0 | 0xF00020A0 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN1 | 0xF00020A4 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN2 | 0xF00020A8 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN3 | 0xF00020AC | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN4 | 0xF00020B0 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN5 | 0xF00020B4 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN6 | 0xF00020B8 | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIOUTEN7 | 0xF00020BC | FULL | CTI Channel to Trigger Enable Registers |
| CM0P_CTI_CTIINSTATUS | 0xF0002130 | FULL | CTI Trigger In Status Register |
| CM0P_CTI_CTIOUTSTATUS | 0xF0002134 | FULL | CTI Trigger Out Status Register |
| CM0P_CTI_CTIINSTATUS | 0xF0002138 | FULL | CTI Channel In Status Register |
| CM0P_CTI_CTIOUTSTATUS | 0xF000213C | FULL | CTI Channel Out Status Register |
| CM0P_CTI_CTIENEN | 0xF0002140 | FULL | Enable CTI Channel Gate Register |
| CM0P_CTI_ASICCTL | 0xF0002144 | FULL | External Multiplexor Control Register |
| CM0P_CTI_ITCHINACK | 0xF0002EDC | FULL | ITCHINACK Register |
| CM0P_CTI_ITTRIGINACK | 0xF0002EE0 | FULL | ITTRIGINACK Register |
| CM0P_CTI_ITCHOUT | 0xF0002EE4 | FULL | ITCHOUT Register |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|--------------------------------------|
| CMOP_CTI_ITTRIGOUT | 0xF0002EE8 | FULL | ITTRIGOUT Register |
| CMOP_CTI_ITCHOUTACK | 0xF0002EEC | FULL | ITCHOUTACK Register |
| CMOP_CTI_ITTRIGOUTACK | 0xF0002EF0 | FULL | ITTRIGOUTACK Register |
| CMOP_CTI_ITCHIN | 0xF0002EF4 | FULL | ITCHIN Register |
| CMOP_CTI_ITTRIGIN | 0xF0002EF8 | FULL | ITTRIGIN Register |
| CMOP_CTI_ITCTRL | 0xF0002F00 | FULL | Integration Mode Control Register |
| CMOP_CTI_CLAIMSET | 0xF0002FA0 | FULL | Claim Tag Set Register |
| CMOP_CTI_CLAIMCLR | 0xF0002FA4 | FULL | Claim Tag Clear Register |
| CMOP_CTI_LOCKACCESS | 0xF0002FB0 | FULL | Lock Access Register |
| CMOP_CTI_LOCKSTATUS | 0xF0002FB4 | FULL | Lock Status Register |
| CMOP_CTI_AUTHSTATUS | 0xF0002FB8 | FULL | Authentication Status Register |
| CMOP_CTI_DEVID | 0xF0002FC8 | FULL | Device Configuration Register |
| CMOP_CTI_DEVTYPE | 0xF0002FCC | FULL | Device Type Identifier Register |
| CMOP_CTI_PID4 | 0xF0002FD0 | FULL | Peripheral Identification Register 4 |
| CMOP_CTI_PID5 | 0xF0002FD4 | FULL | Peripheral Identification Register 5 |
| CMOP_CTI_PID6 | 0xF0002FD8 | FULL | Peripheral Identification Register 6 |
| CMOP_CTI_PID7 | 0xF0002FDC | FULL | Peripheral Identification Register 7 |
| CMOP_CTI_PID0 | 0xF0002FE0 | FULL | Peripheral Identification Register 0 |
| CMOP_CTI_PID1 | 0xF0002FE4 | FULL | Peripheral Identification Register 1 |
| CMOP_CTI_PID2 | 0xF0002FE8 | FULL | Peripheral Identification Register 2 |
| CMOP_CTI_PID3 | 0xF0002FEC | FULL | Peripheral Identification Register 3 |
| CMOP_CTI_CID0 | 0xF0002FF0 | FULL | Component Identification Register 0 |
| CMOP_CTI_CID1 | 0xF0002FF4 | FULL | Component Identification Register 1 |
| CMOP_CTI_CID2 | 0xF0002FF8 | FULL | Component Identification Register 2 |
| CMOP_CTI_CID3 | 0xF0002FFC | FULL | Component Identification Register 3 |

3.7 MTB

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|---------------------------------------|
| CMOP_MTB_POSITION | 0xF0003000 | FULL | POSITION register |
| CMOP_MTB_MASTER | 0xF0003004 | FULL | MASTER register |
| CMOP_MTB_FLOW | 0xF0003008 | FULL | FLOW register |
| CMOP_MTB_BASE | 0xF000300C | FULL | BASE register |
| CMOP_MTB_LA | 0xF0003FB0 | FULL | Lock Access register |
| CMOP_MTB_LS | 0xF0003FB4 | FULL | Lock Status register |
| CMOP_MTB_AS | 0xF0003FB8 | FULL | Authentication Status register |
| CMOP_MTB_DARCH | 0xF0003FBC | FULL | Device Architecture register |
| CMOP_MTB_DCFG | 0xF0003FC8 | FULL | Device Configuration register |
| CMOP_MTB_DID | 0xF0003FCC | FULL | Device Type Identifier register. |
| CMOP_MTB_PID4 | 0xF0003FD0 | FULL | Peripheral Identification Register 4. |
| CMOP_MTB_PID5 | 0xF0003FD4 | FULL | Peripheral Identification Register 5. |
| CMOP_MTB_PID6 | 0xF0003FD8 | FULL | Peripheral Identification Register 6. |
| CMOP_MTB_PID7 | 0xF0003FDC | FULL | Peripheral Identification Register 7. |
| CMOP_MTB_PID0 | 0xF0003FE0 | FULL | Peripheral Identification Register 0. |
| CMOP_MTB_PID1 | 0xF0003FE4 | FULL | Peripheral Identification Register 1. |
| CMOP_MTB_PID2 | 0xF0003FE8 | FULL | Peripheral Identification Register 2. |
| CMOP_MTB_PID3 | 0xF0003FEC | FULL | Peripheral Identification Register 3. |
| CMOP_MTB_CID0 | 0xF0003FF0 | FULL | Component Identification Register 0. |
| CMOP_MTB_CID1 | 0xF0003FF4 | FULL | Component Identification Register 1. |
| CMOP_MTB_CID2 | 0xF0003FF8 | FULL | Component Identification Register 2. |
| CMOP_MTB_CID3 | 0xF0003FFC | FULL | Component Identification Register 3. |

3.8 Register Details

3.8.1 DWT

3.8.1.1 CM0P_DWT_DWT_CTRL

Description: Watchpoint Comparator Configuration
Address: 0xE0001000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Defines the number of comparators implemented
Default: 0x20000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|--------------|----|----|----|
| Name | NUMCOMP [31:28] | | | | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|---------------------------------|
| 28:31 | NUMCOMP | R | | 2 | Number of comparators available |

3.8.1.2 CM0P_DWT_DWT_PCSR

Description: Watchpoint Comparator PC Sample
Address: 0xE000101C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: Samples the current value of the program counter. Unless DWT_PCSR reads as 0xFFFFFFFF, under the conditions described in Program counter sampling support on Arm TRM page C1-344, bit [0] is RAZ. When RAZ, bit [0] does not reflect instruction set state as is the case with similar functionality in other ARM architecture profiles.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | EIASAMPLE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | EIASAMPLE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | EIASAMPLE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | EIASAMPLE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:31 | EIASAMPLE | R | W | X | Executed Instruction Address sample value |

3.8.1.3 CM0P_DWT_DWT_COMP0

Description: Watchpoint Comparator Compare Value
Address: 0xE0001020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: Provides a reference value for use by comparator
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | COMP [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | COMP [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | COMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | COMP | RW | R | X | Reference value for comparison. See The DWT comparators on Arm TRM page C1-341. |

3.8.1.4 CM0P_DWT_DWT_MASK0

Description: Watchpoint Comparator Mask
Address: 0xE0001024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: Provides the size of the ignore mask applied to the access address range matching
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | MASK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | MASK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | MASK [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | MASK | RW | R | X | The size of the ignore mask applied to address range matching. See The DWT comparators on page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. |

3.8.1.5 CM0P_DWT_DWT_FUNCTION0

Description: Watchpoint Comparator Function
Address: 0xE0001028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Controls the operation of the comparator
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------|---|---|---|
| Name | None [7:4] | | | | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|-----------------|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:3 | FUNCTION | RW | R | 0 | Select action on comparator match. |
| | DISABLE | | | 0 | Disabled |
| | IADDR | | | 4 | PC watchpoint event |
| | DADDR_RO | | | 5 | Watchpoint event |
| | DADDR_WO | | | 6 | Watchpoint event |
| | DADDR_RW | | | 7 | Watchpoint event |
| 24 | MATCHED | R | RW | 0 | Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0. |

3.8.1.6 CM0P_DWT_DWT_COMP1

Description: Watchpoint Comparator Compare Value
Address: 0xE0001030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: Provides a reference value for use by comparator
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | COMP | RW | R | X | Reference value for comparison. See The DWT comparators on Arm TRM page C1-341. |

3.8.1.7 CM0P_DWT_DWT_MASK1

Description: Watchpoint Comparator Mask
Address: 0xE0001034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment: Provides the size of the ignore mask applied to the access address range matching
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | MASK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | MASK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | MASK [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | MASK | RW | R | X | The size of the ignore mask applied to address range matching. See The DWT comparators on Arm TRM page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. |

3.8.1.8 CM0P_DWT_DWT_FUNCTION1

Description: Watchpoint Comparator Function
Address: 0xE0001038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment: Controls the operation of the comparator
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------|---|---|---|
| Name | None [7:4] | | | | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|-----------------|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:3 | FUNCTION | RW | R | 0 | Select action on comparator match. |
| | DISABLE | | | 0 | Disabled |
| | IADDR | | | 4 | PC watchpoint event |
| | DADDR_RO | | | 5 | Watchpoint event |
| | DADDR_WO | | | 6 | Watchpoint event |
| | DADDR_RW | | | 7 | Watchpoint event |
| 24 | MATCHED | R | RW | 0 | Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0. |

3.8.1.9 CM0P_DWT_DWT_PID4

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0001FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

3.8.1.10 CM0P_DWT_DWT_PID0

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0001FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 10 | Peripheral ID #0 |

3.8.1.11 CM0P_DWT_DWT_PID1

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0001FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 176 | Peripheral ID #1 |

3.8.1.12 CM0P_DWT_DWT_PID2

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0001FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

3.8.1.13 CM0P_DWT_DWT_PID3

Description: Watchpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0001FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

3.8.1.14 CM0P_DWT_DWT_CID0

Description: Watchpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0001FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

3.8.1.15 CM0P_DWT_DWT_CID1

Description: Watchpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0001FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 224 | Component ID #1 |

3.8.1.16 CM0P_DWT_DWT_CID2

Description: Watchpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0001FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

3.8.1.17 CM0P_DWT_DWT_CID3

Description: Watchpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0001FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

3.8.2 BP

3.8.2.1 CM0P_BP_BP_CTRL

Description: Breakpoint Unit Control
Address: 0xE0002000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Provides BPU implementation information, and the global enable for the BPU.
Default: 0x40

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|------------|---|-----------|--------------|
| Name | NUM_CODE [7:4] | | | | None [3:2] | | KEY [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0 | ENABLE | RW | R | 0 | Enables the BPU: 0 BPU is disabled. 1 BPU is enabled. |
| 1 | KEY | RW | R | 0 | RAZ on reads, SBO for writes. If written as zero, the write to the register is ignored. |
| 4:7 | NUM_CODE | R | | 4 | The number of breakpoint comparators. If NUM_CODE is zero, the implementation does not support any comparators. |

3.8.2.2 CM0P_BP_BP_COMP0

Description: Breakpoint Compare Register
Address: 0xE0002008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|--------------|
| Name | | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|--------------|-------------------|----|----|----|----|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

3.8.2.3 CM0P_BP_BP_COMP1

Description: Breakpoint Compare Register
Address: 0xE000200C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|--------------|
| Name | | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|--------------|-------------------|----|----|----|----|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

3.8.2.4 CM0P_BP_BP_COMP2

Description: Breakpoint Compare Register
Address: 0xE0002010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|--------------|
| Name | | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|--------------|-------------------|----|----|----|----|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

3.8.2.5 CM0P_BP_BP_COMP3

Description: Breakpoint Compare Register
Address: 0xE0002014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Holds a breakpoint address for comparison with instruction addresses in the Code memory region, see The system address map on Arm TRM page B3-258 for more information.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|--------------|
| Name | | | | | | | None [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COMP_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | COMP_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|--------------|-------------------|----|----|----|----|
| Name | MATCH [31:30] | | None [29:29] | COMP_ADDR [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|---|
| 0 | ENABLE | RW | R | 0 | Enables the comparator. Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. |
| 2:28 | COMP_ADDR | RW | R | X | Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. |
| 30:31 | MATCH | RW | R | X | BP_MATCH defines the behavior when the COMP address is matched. |
| | NONE | | | 0 | No breakpoint matching |
| | LOWER | | | 1 | Breakpoint on lower halfword, upper is unaffected. |
| | UPPER | | | 2 | Breakpoint on upper halfword, lower is unaffected. |
| | BOTH | | | 3 | Breakpoint on both lower and upper halfwords. |

3.8.2.6 CM0P_BP_BP_PID4

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0002FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

3.8.2.7 CM0P_BP_BP_PID0

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0002FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #0 |

3.8.2.8 CM0P_BP_BP_PID1

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0002FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 176 | Peripheral ID #1 |

3.8.2.9 CM0P_BP_BP_PID2

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0002FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

3.8.2.10 CM0P_BP_BP_PID3

Description: Breakpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0002FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

3.8.2.11 CM0P_BP_BP_CID0

Description: Breakpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0002FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

3.8.2.12 CM0P_BP_BP_CID1

Description: Breakpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0002FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 224 | Component ID #1 |

3.8.2.13 CM0P_BP_BP_CID2

Description: Breakpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0002FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

3.8.2.14 CM0P_BP_BP_CID3

Description: Breakpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0002FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

3.8.3 SCS

3.8.3.1 CM0P_SCS_SYST_CSR

Description: SysTick Control & Status
Address: 0xE000E010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Controls the SysTick counter and provides status data. The SysTick counter is functional in the Active and Sleep power modes (and not functional in the DeepSleep, and Hibernate power modes).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--------------------|------------------|-----------------|
| Name | None [7:3] | | | | | CLKSOURCE [2:2] | TICKINT [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----------------------|
| Name | None [23:17] | | | | | | | COUNTFLAG [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | ENABLE | RW | R | 0 | Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. |
| 1 | TICKINT | RW | R | 0 | Indicates whether counting to '0' causes the status of the SysTick exception to change to pending: '0': count to '0' does not affect the SysTick exception status. '1': count to '0' changes the SysTick exception status to pending. Changing the value of the counter to '0' by writing zero to the SYST_CVR register to '0' never changes the status of the SysTick exception. |
| 2 | CLKSOURCE | RW | R | 0 | Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock. For this mode to function, the low frequency clock should be less than half the frequency of 'clk_sys'. '1': SysTick uses the system/processor clock 'clk_sys'. Note: Low frequency clock can be selected using CPUSS_SYSTICK_CTL.CLOCK_SOURCE field. |
| 16 | COUNTFLAG | R | RW | 0 | Indicates whether the counter has counted to '0' since the last read of this register: '0': counter has not counted to '0'. '1': counter has counted to '0'. COUNTFLAG is set to '1' by a count transition from '1' to '0'. COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. |

3.8.3.2 CM0P_SCS_SYST_RVR

Description: SysTick Reload Value
Address: 0xE000E014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Sets or reads the reload value of the SYST_CVR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | RELOAD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | RELOAD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | RELOAD [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:23 | RELOAD | RW | R | X | The value to load into the SYST_CVR register when the counter reaches 0. |

3.8.3.3 CM0P_SCS_SYST_CVR

Description: SysTick Current Value
Address: 0xE000E018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: Reads or clears the current counter value. Any write to the register clears the register to 0.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | CURRENT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CURRENT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CURRENT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:23 | CURRENT | RW | R | X | Current counter value. This is the value of the counter at the time it is sampled. |

3.8.3.4 CM0P_SCS_SYST_CALIB

Description: SysTick Calibration Value
Address: 0xE000E01C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: Reads the calibration value and parameters for SysTick.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|--------------|----|----|----|----|----|
| Name | TENMS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TENMS [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TENMS [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | NOREF [31:31] | SKEW [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:23 | TENMS | R | RW | X | Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is '0', the calibration value is not known. This field is controlled by CPUSS_SYSTICK_CTL.TENMS field. |
| 30 | SKEW | R | RW | X | Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. This field is controlled by CPUSS_SYSTICK_CTL.SKEW field. |
| 31 | NOREF | R | | 0 | Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCE is forced to '1' and cannot be cleared to '0'. This field is controlled by CPUSS_SYSTICK_CTL.NOREF field. |

3.8.3.5 CM0P_SCS_ISR

Description: Interrupt Set-Enable Register
Address: 0xE000E100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment: Enables, or reads the enabled state of one or more interrupts.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SETENA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | SETENA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | SETENA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SETENA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|------|----|-----------------|---|
| 0:31 | SETENA | RW1S | R | 0 | Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. |

3.8.3.6 CM0P_SCS_ICER

Description: Interrupt Clear Enable Register
Address: 0xE000E180
Offset: 0x180
Retention: Retained
IsDeepSleep: No
Comment: Disables, or reads the enabled state of one or more interrupts
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | CLRENA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CLRENA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CLRENA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CLRENA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|------|----|-----------------|--|
| 0:31 | CLRENA | RW1C | R | 0 | Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. |

3.8.3.7 CM0P_SCS_ISPR

Description: Interrupt Set-Pending Register
Address: 0xE000E200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment: On writes, sets the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | SETPEND [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | SETPEND [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | SETPEND [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SETPEND [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|----|-----------------|--|
| 0:31 | SETPEND | RW1S | R | 0 | Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. |

3.8.3.8 CM0P_SCS_ICPR

Description: Interrupt Clear-Pending Register
Address: 0xE000E280
Offset: 0x280
Retention: Retained
IsDeepSleep: No
Comment: On writes, clears the status of one or more interrupts to pending. On reads, shows the pending status of the interrupts.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | CLRPEND [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CLRPEND [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CLRPEND [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CLRPEND [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|----|-----------------|--|
| 0:31 | CLRPEND | RW1C | R | 0 | Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. |

3.8.3.9 CM0P_SCS_IPR

Description: Interrupt Priority Registers
Address: 0xE000E400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment: Sets or reads interrupt priorities. Register n contains priorities for interrupts $N=4n \dots 4n+3$
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|------------|---|---|---|---|---|
| Name | PRI_N0 [7:6] | | None [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|-------------|----|----|----|---|---|
| Name | PRI_N1 [15:14] | | None [13:8] | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|--------------|----|----|----|----|----|
| Name | PRI_N2 [23:22] | | None [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|--------------|----|----|----|----|----|
| Name | PRI_N3 [31:30] | | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|-----------------------------------|
| 6:7 | PRI_N0 | RW | R | 0 | Priority of interrupt number N. |
| 14:15 | PRI_N1 | RW | R | 0 | Priority of interrupt number N+1. |
| 22:23 | PRI_N2 | RW | R | 0 | Priority of interrupt number N+2. |
| 30:31 | PRI_N3 | RW | R | 0 | Priority of interrupt number N+3. |

3.8.3.10 CM0P_SCS_CPUID

Description: CPUID Register
Address: 0xE000ED00
Offset: 0xD00
Retention: Retained
IsDeepSleep: No
Comment: Contains the part number, version, and implementation information that is specific to this processor.
Default: 0x410CC601

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|------------------|----|----|----|
| Name | REVISION [3:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PARTNO [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | VARIANT [23:20] | | | | CONSTANT [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | IMPLEMENTER [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 0:3 | REVISION | R | | 1 | Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on Arm TRM page xii. For release r0p1. |
| 4:15 | PARTNO | R | | 3168 | Indicates part number, Cortex-M0+ |
| 16:19 | CONSTANT | R | | 12 | Indicates the architecture, ARMv6-M |
| 20:23 | VARIANT | R | | 0 | Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on Arm TRM page xii. |
| 24:31 | IMPLEMENTER | R | | 65 | Implementer code for ARM. |

3.8.3.11 CM0P_SCS_ICSR

Description: Interrupt Control State Register
Address: 0xE000ED04
Offset: 0xD04
Retention: Retained
IsDeepSleep: No
Comment: Controls and provides status information for the ARMv6-M.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|---|---|---|---|---|---|
| Name | VECTACTIVE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----|----|----|----|-------------|----|---|----------------------|
| Name | | | | | None [11:9] | | | VECTACTIV E [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------------|------------------------|-----------------|---------------------|----|----|----|----|
| Name | ISRPREEMP T [23:23] | ISRPENDIN G [22:22] | None [21:21] | VECTPENDING [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------------|--------------|----|----------------------|----------------------|------------------------|----------------------|-----------------|
| Name | NMIPENDSE T [31:31] | None [30:29] | | PENDSVSET [28:28] | PENDSVCLR [27:27] | PENDSTSET B [26:26] | PENDSTCLR [25:25] | None [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|------|----|-----------------|--|
| 0:8 | VECTACTIVE | R | RW | 0 | The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] |
| 12:20 | VECTPENDING | R | RW | 0 | The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. |
| 22 | ISRPENDING | R | RW | 0 | Indicates if an external configurable, NVIC generated, interrupt is pending. |
| 23 | ISRPREEMPT | R | RW | 0 | Indicates whether a pending exception will be serviced on exit from debug halt state. |
| 25 | PENDSTCLR | RW1C | R | 0 | Clears a pending SysTick, whether set here or by the timer hardware. |
| 26 | PENDSTSETB | RW1S | RW | 0 | Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. |
| 27 | PENDSVCLR | RW1C | R | 0 | Clears a pending PendSV interrupt. |
| 28 | PENDSVSET | RW1S | RW | 0 | Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE. |
| 31 | NMIPENDSET | RW1S | RW | 0 | Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. |

3.8.3.12 CM0P_SCS_VTOR

Description: Vector Table Offset Register
Address: 0xE000ED08
Offset: 0xD08
Retention: Retained
IsDeepSleep: No
Comment: Holds the vector table offset address
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | TBLOFF [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | TBLOFF [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | TBLOFF [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 8:31 | TBLOFF | RW | R | 0 | Table offset address. All bits of the Vector table address that are not defined by the VTOR are zero. |

3.8.3.13 CM0P_SCS_AIRCR

Description: Application Interrupt and Reset Control Register
Address: 0xE000ED0C
Offset: 0xD0C
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns interrupt control data.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------------|---------------------|------------|
| Name | None [7:3] | | | | | SYSRESETREQ [2:2] | VECTCLRACTIVE [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|-------------|----|----|----|----|---|---|
| Name | ENDIANNESS [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | VECTKEY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | VECTKEY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|------|----|-----------------|--|
| 1 | VECTCLRACTIVE | RW1C | R | 0 | Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. |
| 2 | SYSRESETREQ | RW1S | R | 0 | System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on Arm TRM page B1-240 for more information. |
| 15 | ENDIANNESS | R | | 0 | Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. |
| 16:31 | VECTKEY | RW | R | X | Vector Key. The value 0x05FA must be written to this register, otherwise the register write is not performed. |

3.8.3.14 CM0P_SCS_SCR

Description: System Control Register
Address: 0xE000ED10
Offset: 0xD10
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns system control data.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|------------|-----------------|-------------------|------------|
| Name | None [7:5] | | | SEVONPEND [4:4] | None [3:3] | SLEEPDEEP [2:2] | SLEEPONEXIT [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 1 | SLEEPONEXIT | RW | R | 0 | Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on Arm TRM page B1-240 for more information. |
| 2 | SLEEPDEEP | RW | R | 0 | An implementation can use this bit to select DeepSleep power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep |
| 4 | SEVONPEND | RW | R | 0 | Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on Arm TRM page A6-197 for more information. |

3.8.3.15 CM0P_SCS_CCR

Description: Configuration and Control Register
Address: 0xE000ED14
Offset: 0xD14
Retention: Retained
IsDeepSleep: No
Comment: Returns configuration and control data.
Default: 0x208

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-------------------|------------|---|---|
| Name | None [7:4] | | | | UNALIGN_TRP [3:3] | None [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------|------------|
| Name | None [15:10] | | | | | | STKALIGN [9:9] | None [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 3 | UNALIGN_TRP | R | | 1 | 1: unaligned word and halfword accesses generate a HardFault exception. |
| 9 | STKALIGN | R | | 1 | 1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. |

3.8.3.16 CM0P_SCS_SHPR2

Description: System Handler Priority Register 2
Address: 0xE000ED1C
Offset: 0xD1C
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns priority for system handler 11
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|--------------|----|----|----|----|----|
| Name | PRI_11 [31:30] | | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|---------------------------------------|
| 30:31 | PRI_11 | RW | R | 0 | Priority of system handler 11, SVCall |

3.8.3.17 CM0P_SCS_SHPR3

Description: System Handler Priority Register 3
Address: 0xE000ED20
Offset: 0xD20
Retention: Retained
IsDeepSleep: No
Comment: Sets or returns priority for system handlers 14-15.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|--------------|----|----|----|----|----|
| Name | PRI_14 [23:22] | | None [21:16] | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|--------------|----|----|----|----|----|
| Name | PRI_15 [31:30] | | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|--|
| 22:23 | PRI_14 | RW | R | 0 | Priority of system handler 14, PendSV |
| 30:31 | PRI_15 | RW | R | 0 | Priority of system handler 15, SysTick |

3.8.3.18 CM0P_SCS_SHCSR

Description: System Handler Control and State Register
Address: 0xE000ED24
Offset: 0xD24
Retention: Retained
IsDeepSleep: No
Comment: Controls and provides the status of system handlers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------------|-------------|----|----|----|----|---|---|
| Name | SVCALLPEN DED [15:15] | None [14:8] | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 15 | SVCALLPEN DED | RW | RW | 0 | 0 SVCAll is not pending. 1 SVCAll is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) |

3.8.3.19 CM0P_SCS_DFSR

Description: Debug Fault Status Register
Address: 0xE000ED30
Offset: 0xD30
Retention: Retained
IsDeepSleep: No
Comment: Provides the top level reason why a debug event has occurred. Writing 1 to a register bit clears that bit to 0. A read of the HALTED bit by an instruction executed by stepping returns an UNKNOWN value, For more information see Debug stepping on Arm TRM page C1-325.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|--------------|---------------|------------|--------------|
| Name | None [7:5] | | | EXTERNAL [4:4] | VCATCH [3:3] | DWTTRAP [2:2] | BKPT [1:1] | HALTED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|------|-----------------|--|
| 0 | HALTED | RW1C | RW1S | 0 | Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR: 0 no active halt request debug event. 1 halt request debug event active. See Debug Halting Control and Status Register, DHCSR for more information. |
| 1 | BKPT | RW1C | RW1S | 0 | Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU: 0 no breakpoint debug event. 1 at least one breakpoint debug event. |
| 2 | DWTTRAP | RW1C | RW1S | 0 | Indicates a debug event generated by the DWT: 0 no debug events generated by the DWT. 1 at least one debug event generated by the DWT. |
| 3 | VCATCH | RW1C | RW1S | 0 | Indicates whether a vector catch debug event was generated: 0 no vector catch debug event generated. 1 vector catch debug event generated. The corresponding FSR shows the primary cause of the exception. |
| 4 | EXTERNAL | RW1C | RW1S | 0 | Indicates an asynchronous debug event generated because of EDBGRRQ being asserted: 0 no EDBGRRQ debug event. 1 EDBGRRQ debug event. |

3.8.3.20 CM0P_SCS_MPU_TYPE

Description: MPU Type Register

Address: 0xE000ED90

Offset: 0xD90

Retention: Retained

IsDeepSleep: No

Comment: The MPU Type Register indicates how many regions the MPU supports. Software can use it to determine if the processor implements an MPU

Default: 0x800

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------|
| Name | None [7:1] | | | | | | | SEPARATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | DREGION [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | IREGION [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 0 | SEPARATE | R | R | 0 | Indicates support for separate instruction and data address maps. RAZ. ARMv6-M only supports a unified MPU. |
| 8:15 | DREGION | R | R | 8 | Number of regions supported by the MPU. If this field reads-as-zero the processor does not implement an MPU. |
| 16:23 | IREGION | R | R | 0 | Instruction region. RAZ. ARMv6-M only supports a unified MPU. |

3.8.3.21 CM0P_SCS_MPU_CTRL

Description: MPU Control Register

Address: 0xE000ED94

Offset: 0xD94

Retention: Retained

IsDeepSleep: No

Comment: Enables the MPU, and when the MPU is enabled, controls whether the default memory map is enabled as a background region for privileged accesses, and whether the MPU is enabled for HardFaults and NMI.

If no regions are enabled and the PRIVDEFENA and ENABLE bits are set, only privileged code can execute from the system address map.

If the MPU is not implemented, this register is RAZ/WI.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|------------------|---------------|--------------|
| Name | None [7:3] | | | | | PRIVDEFENA [2:2] | HFNMENA [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0 | ENABLE | RW | R | 0 | Enables the MPU: 0: The MPU is disabled. Privileged and unprivileged accesses use the default memory map. 1: The MPU is enabled. |
| 1 | HFNMENA | RW | R | 0 | The meaning of this bit is: 0: disables the MPU for HardFaults and NMIs. 1: when the ENABLE bit is set to 1, enables the MPU for HardFaults and NMIs. Note: If HFNMENA is set to 1 when ENABLE is set to 0, behavior is UNPREDICTABLE. |
| 2 | PRIVDEFENA | RW | R | 0 | When the ENABLE bit is set to 1, the meaning of this bit is: 0: Disables the default memory map. Any instruction or data access that does not access a defined region faults. 1: Enables the default memory map as a background region for privileged access. The system address map on Arm TRM page B3-258 describes the default memory map. When the ENABLE bit is set to 0, the processor ignores the PRIVDEFENA bit. |

3.8.3.22 CM0P_SCS_MPU_RNR

Description: MPU Region Number Register

Address: 0xE000ED98

Offset: 0xD98

Retention: Retained

IsDeepSleep: No

Comment: Selects the region currently accessed by MPU_RBAR and MPU_RASR.
Used with MPU_RBAR and MPU_RASR, see MPU Region Base Address Register, MPU_RBAR, and MPU Region Attribute and Size Register, MPU_RASR.
If an implementation supports N regions then the regions number from 0 to (N-1), and the effect of writing a value of N or greater to the REGION field is UNPREDICTABLE.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | REGION_M [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:7 | REGION_M | RW | R | X | Indicates the memory region accessed by MPU_RBAR and MPU_RSAR. Normally, software must write the required region number to MPU_RNR to select the required memory region, before accessing MPU_RBAR or MPU_RSAR. However, the MPU_RBAR.VALID bit provides an alternative way of writing to MPU_RBAR to update a region base address without first writing the region number to MPU_RNR, see MPU Region Base Address Register, MPU_RBAR. |

3.8.3.23 CM0P_SCS_MPU_RBAR

Description: MPU Region Base Address Register

Address: 0xE000ED9C

Offset: 0xD9C

Retention: Retained

IsDeepSleep: No

Comment: Holds the base address of the region identified by MPU_RNR. On a write, can also be used to update the base address of a specified region, in the range 0 to 15, updating MPU_RNR with the new region number.

Normally, used with MPU_RBAR, see MPU Region Number Register, MPU_RNR.

If an implementation supports N regions then the regions number from 0 to (N-1). If N is less than 16 the effect of writing a value of N or greater to the REGION field is UNPREDICTABLE. Software can find the minimum size of region supported by an MPU region by writing all ones to MPURBAR[31:5] for that region, and then reading the register to find the value saved to bits [31:5]. The number of trailing zeros in this bit field indicates the minimum supported alignment and therefore the supported region size. An implementation must support all region size values from the minimum supported to 4GB, see the description of the MPU_RASR.SIZE field in MPU Region Attribute and Size Register, MPU_RASR.

Software must ensure that the value written to the ADDR field aligns with the size of the selected region.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-------------|--------------|---|---|---|
| Name | None [7:5] | | | VALID [4:4] | REGION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:3 | REGION | RW | R | X | On writes, can specify the number of the region to update, see VALID field description. On reads, returns bits [3:0] of MPU_RNR. |
| 4 | VALID | RW | R | X | On writes to the register, indicates whether the write must update the base address of the region identified by the REGION field. updating the MPU_RNR to indicate this new region: 0 Update the base address of the region indicated by MPU_RNR, ignoring the value of the REGION field. 1 Update the least-significant four bits of the MPU_RNR.REGION field with MPU_RBAR.REGION field value, writing 0b0000 to bits [7:4] of the MPU_RBAR.REGION field, and updating the base address of that region. This bit reads as zero |
| 8:31 | ADDR | RW | R | X | Base address of the region. |

3.8.3.24 CM0P_SCS_MPU_RASR

Description: MPU Region Attribute and Size Register

Address: 0xE000EDA0

Offset: 0xDA0

Retention: Retained

IsDeepSleep: No

Comment: Defines the size, access behavior, and memory type of the region identified by MPU_RNR, and enables that region.

Used with MPU_RBAR, see MPU Region Number Register, MPU_RNR on. Writing a SIZE value greater than the maximum size supported by the corresponding MPU_RBAR has an UNPREDICTABLE effect. The smallest supported region size is 256 bytes. This restricts the lowest possible value of SIZE.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------|---|---|---|---|--------------|
| Name | None [7:6] | | SIZE [5:1] | | | | | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | SRD [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | ATTRS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | ATTRS [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|--|
| 0 | ENABLE | RW | R | X | Enables this region: 0: when the MPU is enabled, this region is disabled. 1: When the MPU is enabled, this region is enabled. Enabling a region has no effect unless the MPU_CTRL.ENABLE bit is set to 1, to enable the MPU. |
| 1:5 | SIZE | RW | R | X | Indicates the region size. The permitted values for SIZE are 7-31, that is 0b00111-0b11111. The associated region size, in bytes, is 2 ^(SIZE+1) . SIZE field values less than 7 are reserved, because the smallest supported region size is 256 bytes. |
| 8:15 | SRD | RW | R | X | Subregion Disable. For regions of 256 bytes or larger, each bit of this field controls whether one of the eight equal subregions is enabled. 0: subregion enabled. 1: subregion disabled. |
| 16:31 | ATTRS | RW | R | X | The MPU Region Attribute field, This field has the following subfields, defined in Region attribute control on Arm TRM page B3-300 of the ARMv6M Architecture manual (September 2010 version): XN MPU_RASR[28] AP[2:0] MPU_RASR[26:24] TEX[2:0] MPU_RASR[21:19] S MPU_RASR[18] C MPU_RASR[17] B MPU_RASR[16] |

3.8.3.25 CM0P_SCS_DHCSR

Description: Debug Halting Control and Status Register
Address: 0xE000EDF0
Offset: 0xDF0
Retention: Retained
IsDeepSleep: No
Comment: Controls halting debug. When C_DEBUGEN is set to 1, C_STEP and C_MASKINTS must not be modified when the processor is running. Note: S_HALT is 0 when the processor is running. When C_DEBUGEN is set to 0, the processor ignores the values of all other bits in this register. For more information on the use of DHCSR, see Debug stepping on Arm TRM page C1-325.
Note: any write to this register must have [31:16]=0xA05F - if not, the write is ignored.
Default: 0x2000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|------------------|-----------------|--------------------|---------------------|
| Name | None [7:4] | | | | C_MASKINTS [3:3] | C_STEP [2:2] | C_HALT [1:1] | C_DEBUGEN [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DBG_KEY_P1 [23:20] | | | | S_LOCKUP [19:19] | S_SLEEP [18:18] | S_HALT [17:17] | S_REGRDY [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DBG_KEY_P2 [31:26] | | | | | | S_RESET_ST [25:25] | S_RETIRE_ST [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | C_DEBUGEN | RW | R | 0 | Halting debug enable bit. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP. Access to the DHCSR from software running on the processor is IMPLEMENTATION DEFINED. However, writes to this bit from software running on the processor are ignored. |
| 1 | C_HALT | RW | R | X | Processor halt bit. The effects of writes to this bit are: 0 Request a halted processor to run. 1 Request a running processor to halt. Table C1-7 on Arm TRM page C1-326 shows the effect of writes to this bit when the processor is in Debug state. |
| 2 | C_STEP | RW | R | X | Processor step bit. The effects of writes to this bit are: 0 Single-stepping disabled. 1 Single-stepping enabled. For more information about the use of this bit see Table C1-7 on Arm TRM page C1-326. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 3 | C_MASKINTS | RW | R | X | When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: - before the write to DHCSR, the value of the C_HALT bit is 1 - the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. For more information about the use of this bit see Table C1-7 on Arm TRM page C1-326. |
| 16 | S_REGRDY | R | RW | X | A handshake flag for transfers through the DCRDR: - Writing to DCRSR clears the bit to 0. - Completion of the DCRDR transfer then sets the bit to 1. For more information about DCRDR transfers see Debug Core Register Data Register, DCRDR on Arm TRM page C1-337. 0: There has been a write to the DCRDR, but the transfer is not complete. 1: The transfer to or from the DCRDR is complete. This bit is only valid when the processor is in Debug state, otherwise the bit is UNKNOWN. |
| 17 | S_HALT | R | RW | 0 | Indicates whether the processor is in Debug state. |
| 18 | S_SLEEP | R | RW | 0 | Indicates whether the processor is sleeping. The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or wait for an interrupt or other wakeup event to wakeup the system. |
| 19 | S_LOCKUP | R | RW | 0 | Indicates whether the processor is locked up because of an unrecoverable exception. See Unrecoverable exception cases on Arm TRM page B1-238 for more information. This bit can only read as 1 when accessed by a remote debugger using the DAP. The bit clears to 0 when the processor enters Debug state. |
| 20:23 | DBG_KEY_P1 | W | R | X | Debug key: Software must write 0xA05F to [31:16] to enable write accesses to bits [15:0], otherwise the processor ignores the write access. |
| 24 | S_RETIRE_ST | R | RW | X | When not in Debug state, indicates whether the processor has completed execution of at least one instruction since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR. This bit is UNKNOWN: - after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction - when S_LOCKUP is set to 1 - when S_HALT is set to 1. When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load, store or fetch access. |
| 25 | S_RESET_ST | R | RW | 1 | Indicates whether the processor has been reset since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR |
| 26:31 | DBG_KEY_P2 | W | R | X | See description for Bit 20 |

3.8.3.26 CM0P_SCS_DCRSR

Description: Debug Core Register Selector Register
Address: 0xE00EDF4
Offset: 0xDF4
Retention: Retained
IsDeepSleep: No
Comment: With the DCRDR, see Debug Core Register Data Register, DCRDR on Arm TRM page C1-337, the DCRSR provides debug access to the ARM core registers and special-purpose registers. A write to DCRSR specifies the register to transfer, whether the transfer is a read or a write, and starts the transfer. This register is only accessible in Debug state. When the processor is in Debug state, the debugger must preserve the Exception number bits in the IPSR, otherwise behavior is UNPREDICTABLE
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------|---|---|---|---|
| Name | None [7:5] | | | REGSEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----------------|
| Name | None [23:17] | | | | | | | REGWNR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:4 | REGSEL | RW | R | X | Specifies the ARM core register or special-purpose register to transfer. |
| | R0 | | | 0 | CPU R0 |
| | R1 | | | 1 | CPU R1 |
| | R2 | | | 2 | CPU R2 |
| | R3 | | | 3 | CPU R3 |
| | R4 | | | 4 | CPU R4 |
| | R5 | | | 5 | CPU R5 |
| | R6 | | | 6 | CPU R6 |
| | R7 | | | 7 | CPU R7 |
| | R8 | | | 8 | CPU R8 |
| | R9 | | | 9 | CPU R9 |
| | R10 | | | 10 | CPU R10 |
| | R11 | | | 11 | CPU R11 |
| | R12 | | | 12 | CPU R12 |
| | SP | | | 13 | Current Stack Pointer |
| | LR | | | 14 | CPU LR |
| | DBG_RA | | | 15 | DebugReturnAddress: the address of the first instruction to be executed on exit from Debug state. |
| | XPSR | | | 16 | xPSR |
| | MSP | | | 17 | Main stack pointer, MSP. |
| | PSP | | | 18 | Process stack pointer, PSP |
| | C_P | | | 20 | [31:24]: CONTROL [7:0]: PRIMASK. |
| 16 | REGWNR | RW | R | X | Specifies the type of access for the transfer. |
| | READ | | | 0 | Read transfer |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|----------------|
| | WRITE | | | 1 | Write transfer |

3.8.3.27 CM0P_SCS_DCRDR

Description: Debug Core Register Data Register
Address: 0xE000EDF8
Offset: 0xDF8
Retention: Retained
IsDeepSleep: No
Comment: With the DCRSR, see Debug Core Register Selector Register, DCRSR on Arm TRM page C1-335, the DCRDR provides debug access to the ARM core registers and special-purpose registers. The DCRDR is the data register for these accesses.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DBGTMP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DBGTMP [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DBGTMP [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DBGTMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:31 | DBGTMP | RW | RW | X | Data temporary cache, for reading and writing CPU registers. This register is UNKNOWN: - on reset - when DHCSR.S_HALT = 0. - when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register |

3.8.3.28 CM0P_SCS_DEMCR

Description: Debug Exception and Monitor Control Register
Address: 0xE000EDFC
Offset: 0xDFC
Retention: Retained
IsDeepSleep: No
Comment: Manages vector catch behavior and enables the DWT.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|--------------------|
| Name | None [7:1] | | | | | | | VC_CORERESET [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------|------------|---|
| Name | None [15:11] | | | | | VC_HARDERR [10:10] | None [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----------------|
| Name | None [31:25] | | | | | | | DWTENA [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0 | VC_CORERESET | RW | R | 0 | Enable Reset Vector Catch. This causes a Local reset to halt a running system. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. |
| 10 | VC_HARDERR | RW | R | 0 | Enable halting debug trap on a HardFault exception. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. |
| 24 | DWTENA | RW | R | 0 | Global enable for all features configured and controlled by the DWT unit. When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition, it is IMPLEMENTATION DEFINED whether the processor ignores writes to the DWT while DWTENA is 0. |

3.8.3.29 CM0P_SCS_SCS_PID4

Description: System Control Space ROM Table Peripheral ID #4
Address: 0xE000EFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

3.8.3.30 CM0P_SCS_SCS_PID0

Description: System Control Space ROM Table Peripheral ID #0
Address: 0xE000EFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x8

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 8 | Peripheral ID #0 |

3.8.3.31 CM0P_SCS_SCS_PID1

Description: System Control Space ROM Table Peripheral ID #1
Address: 0xE000EFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 176 | Peripheral ID #1 |

3.8.3.32 CM0P_SCS_SCS_PID2

Description: System Control Space ROM Table Peripheral ID #2
Address: 0xE000EFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

3.8.3.33 CM0P_SCS_SCS_PID3

Description: System Control Space ROM Table Peripheral ID #3
Address: 0xE000EFEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

3.8.3.34 CM0P_SCS_SCS_CID0

Description: System Control Space ROM Table Component ID #0
Address: 0xE000EFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

3.8.3.35 CM0P_SCS_SCS_CID1

Description: System Control Space ROM Table Component ID #1
Address: 0xE000EFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 224 | Component ID #1 |

3.8.3.36 CM0P_SCS_SCS_CID2

Description: System Control Space ROM Table Component ID #2
Address: 0xE000EFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

3.8.3.37 CM0P_SCS_SCS_CID3

Description: System Control Space ROM Table Component ID #3
Address: 0xE000E0FC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

3.8.4 ROM

3.8.4.1 CM0P_ROM_ROM_SCS

Description: CM0+ CoreSight ROM Table Peripheral #0
Address: 0xE00FF000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF0F003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429398016 3 | Offset to SCS ROM Table |

3.8.4.2 CM0P_ROM_ROM_DWT

Description: CM0+ CoreSight ROM Table Peripheral #1
Address: 0xE00FF004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF02003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 4293926915 | Offset to DWT ROM Table |

3.8.4.3 CM0P_ROM_ROM_BPU

Description: CM0+ CoreSight ROM Table Peripheral #2
Address: 0xE00FF008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF03003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429393101 1 | Offset to BPU ROM Table |

3.8.4.4 CM0P_ROM_ROM_END

Description: CM0+ CoreSight ROM Table End Marker
Address: 0xE00FF00C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------------|
| 0:31 | VALUE | R | | 0 | End marker in peripheral list |

3.8.4.5 CM0P_ROM_ROM_CSMT

Description: CM0+ CoreSight ROM Table Memory Type
Address: 0xE00FFFCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | | 1 | Memory Type |

3.8.4.6 CM0P_ROM_ROM_PID4

Description: CM0+ CoreSight ROM Table Peripheral ID #4
Address: 0xE00FFFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

3.8.4.7 CM0P_ROM_ROM_PID0

Description: CM0+ CoreSight ROM Table Peripheral ID #0
Address: 0xE00FFFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 192 | Peripheral ID #0 |

3.8.4.8 CM0P_ROM_ROM_PID1

Description: CM0+ CoreSight ROM Table Peripheral ID #1
Address: 0xE00FFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

3.8.4.9 CM0P_ROM_ROM_PID2

Description: CM0+ CoreSight ROM Table Peripheral ID #2
Address: 0xE00FFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

3.8.4.10 CM0P_ROM_ROM_PID3

Description: CM0+ CoreSight ROM Table Peripheral ID #3
Address: 0xE00FFFE0
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

3.8.4.11 CM0P_ROM_ROM_CID0

Description: CM0+ CoreSight ROM Table Component ID #0
Address: 0xE00FFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

3.8.4.12 CM0P_ROM_ROM_CID1

Description: CM0+ CoreSight ROM Table Component ID #1
Address: 0xE00FFFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

3.8.4.13 CM0P_ROM_ROM_CID2

Description: CM0+ CoreSight ROM Table Component ID #2
Address: 0xE00FFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

3.8.4.14 CM0P_ROM_ROM_CID3

Description: CM0+ CoreSight ROM Table Component ID #3
Address: 0xE00FFFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

3.8.5 ROMTABLE

3.8.5.1 CM0P_ROMTABLE_ADDR0

Description: Link to Cortex M0+ ROM Table.
Address: 0xF0000000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF00FF003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------------|---------------|
| Name | None [7:2] | | | | | | FORMAT_32BIT [1:1] | PRESENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [11:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ADDR_OFFSET [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ADDR_OFFSET [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0 | PRESENT | R | R | 1 | Entry present. |
| 1 | FORMAT_32BIT | R | R | 1 | ROM Table format: '0': 8-bit format. '1': 32-bit format. |
| 12:31 | ADDR_OFFSET | R | R | 983295 | Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. |

3.8.5.2 CM0P_ROMTABLE_ADDR1

Description: Link to CoreSight CTI Table.
Address: 0xF0000004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------------|---------------|
| Name | None [7:2] | | | | | | FORMAT_32BIT [1:1] | PRESENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [11:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ADDR_OFFSET [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ADDR_OFFSET [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0 | PRESENT | R | R | 1 | Entry present. |
| 1 | FORMAT_32BIT | R | R | 1 | ROM Table format: '0': 8-bit format. '1': 32-bit format. |
| 12:31 | ADDR_OFFSET | R | R | 2 | Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. |

3.8.5.3 CM0P_ROMTABLE_ADDR2

Description: Link to Cortex M0+ MTB Table.
Address: 0xF0000008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------------|---------------|
| Name | None [7:2] | | | | | | FORMAT_32BIT [1:1] | PRESENT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [11:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ADDR_OFFSET [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ADDR_OFFSET [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0 | PRESENT | R | R | 1 | Entry present. |
| 1 | FORMAT_32BIT | R | R | 1 | ROM Table format: '0': 8-bit format. '1': 32-bit format. |
| 12:31 | ADDR_OFFSET | R | R | 3 | Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. |

3.8.5.4 CM0P_ROMTABLE_DID

Description: Device Type Identifier register.
Address: 0xF0000FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 1 | . |

3.8.5.5 CM0P_ROMTABLE_PID4

Description: Peripheral Identification Register 4.
Address: 0xF000FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|------------------------|---|---|---|
| Name | COUNT [7:4] | | | | JEP_CONTINUATION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:3 | JEP_CONTINUATION | R | R | Undefined | JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. |
| 4:7 | COUNT | R | R | 0 | Size of ROM Table is $2^{\text{COUNT}} \times 4$ KByte. |

3.8.5.6 CM0P_ROMTABLE_PID5

Description: Peripheral Identification Register 5.
Address: 0xF0000FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | . |

3.8.5.7 CM0P_ROMTABLE_PID6

Description: Peripheral Identification Register 6.
Address: 0xF0000FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | . |

3.8.5.8 CM0P_ROMTABLE_PID7

Description: Peripheral Identification Register 7.
Address: 0xF0000FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | . |

3.8.5.9 CM0P_ROMTABLE_PID0

Description: Peripheral Identification Register 0.
Address: 0xF0000FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | PN_MIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:7 | PN_MIN | R | R | Undefined | JEP106 part number. 4 lsb of CPUSS.PARTNUMBER parameter. |

3.8.5.10 CM0P_ROMTABLE_PID1

Description: Peripheral Identification Register 1.
Address: 0xF0000FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|--------------|---|---|---|
| Name | JEPID_MIN [7:4] | | | | PN_MAJ [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:3 | PN_MAJ | R | R | Undefined | JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. |
| 4:7 | JEPID_MIN | R | R | Undefined | JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. |

3.8.5.11 CM0P_ROMTABLE_PID2

Description: Peripheral Identification Register 2.
Address: 0xF0000FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|------------|-----------------|---|---|
| Name | REV [7:4] | | | | None [3:3] | JEPID_MAJ [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:2 | JEPID_MAJ | R | R | Undefined | JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. |
| 4:7 | REV | R | R | Undefined | Major REVersion number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. |

3.8.5.12 CM0P_ROMTABLE_PID3

Description: Peripheral Identification Register 3.
Address: 0xF0000FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|----------|---|---|---|
| Name | REV_AND [7:4] | | | | CM [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:3 | CM | R | R | 0 | N/A |
| 4:7 | REV_AND | R | R | Undefined | Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs. |

3.8.5.13 CM0P_ROMTABLE_CID0

Description: Component Identification Register 0.
Address: 0xF0000FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 13 | Component identification byte 0 of 4-byte component identification 0xB105:100D. |

3.8.5.14 CM0P_ROMTABLE_CID1

Description: Component Identification Register 1.
Address: 0xF0000FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 16 | Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: 'ROM Table'. |

3.8.5.15 CM0P_ROMTABLE_CID2

Description: Component Identification Register 2.
Address: 0xF0000FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 5 | Component identification byte 2 of 4-byte component identification 0xB105:100D. |

3.8.5.16 CM0P_ROMTABLE_CID3

Description: Component Identification Register 3.
Address: 0xF0000FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 177 | Component identification byte 3 of 4-byte component identification 0xB105:100D. |

3.8.6 CTI

3.8.6.1 CM0P_CTI_CTICONTROL

Description: CTI Control Register
Address: 0xF0002000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: The CTI Control Register enables the CTI.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | GLBEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | GLBEN | RW | R | 0 | Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. |

3.8.6.2 CM0P_CTLI_INTACK

Description: CTI Interrupt Acknowledge Register
Address: 0xF0002010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the CTITRIGOUT output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the CTITRIGOUT is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | INTACK [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | INTACK | W | R | 0 | Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. |

3.8.6.3 CM0P_CTLIAPPSET

Description: CTI Application Trigger Set Register
Address: 0xF0002014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|--------------|----|----|----|
| Name | None [7:4] | | | | APPSET [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:3 | APPSET | RW | R | 0 | Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. |

3.8.6.4 CM0P_CTI_APPCLEAR

Description: CTI Application Trigger Clear Register
Address: 0xF0002018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: The CTI Application Trigger Clear Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----------------|----|----|----|
| Name | None [7:4] | | | | APPCLEAR [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | APPCLEAR | W | R | 0 | Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. |

3.8.6.5 CM0P_CTI_CTIAPPULSE

Description: CTI Application Pulse Register

Address: 0xF000201C

Offset: 0x1C

Retention: Retained

IsDeepSleep: No

Comment: The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | APPULSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:3 | APPULSE | W | R | 0 | Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. |

3.8.6.6 CM0P_CTI_CTIINEN

Description: CTI Trigger to Channel Enable Registers

Address: 0xF0002020

Offset: 0x20

Retention: Retained

IsDeepSleep: No

Comment: The CTI Trigger to Channel Enable Registers enable the signaling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI. There is one register for each of the eight CTITRIGIN inputs. Within each register there is one bit for each of the four channels implemented. These registers do not affect the application trigger operations.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------|---|---|---|
| Name | None [7:4] | | | | TRIGINEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:3 | TRIGINEN | RW | R | 0 | Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. |

3.8.6.7 CM0P_CTLIOUTEN

Description: CTI Channel to Trigger Enable Registers

Address: 0xF00020A0

Offset: 0xA0

Retention: Retained

IsDeepSleep: No

Comment: The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output. There is one register for each of the eight CTITRIGOUT outputs. Within each register there is one bit for each of the four channels implemented. These registers affect the mapping from application trigger to trigger outputs.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------------|---|---|---|
| Name | None [7:4] | | | | TRIGOUTEN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:3 | TRIGOUTEN | RW | R | 0 | Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. |

3.8.6.8 CM0P_CTL_CTITRIGINSTATUS

Description: CTI Trigger In Status Register
Address: 0xF0002130
Offset: 0x130
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger In Status Register provides the status of the CTITRIGIN inputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | TRIGINSTATUS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:7 | TRIGINSTATUS | R | RW | 0 | Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. |

3.8.6.9 CM0P_CTL_CTITRIGOUTSTATUS

Description: CTI Trigger Out Status Register
Address: 0xF0002134
Offset: 0x134
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger Out Status Register provides the status of the CTITRIGOUT outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | TRIGOUTSTATUS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:7 | TRIGOUTSTATUS | R | RW | 0 | Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. |

3.8.6.10 CM0P_CTICHIINSTAТUS

Description: CTI Channel In Status Register
Address: 0xF0002138
Offset: 0x138
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel In Status Register provides the status of the CTI CTICHIN inputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------------|---|---|---|
| Name | None [7:4] | | | | CTICHINSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:3 | CTICHINSTATUS | R | RW | 0 | Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. |

3.8.6.11 CM0P_CTICHIOUTSTATUS

Description: CTI Channel Out Status Register
Address: 0xF000213C
Offset: 0x13C
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel Out Status Register provides the status of the CTI CTICHOUT outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------------|---|---|---|
| Name | None [7:4] | | | | CTICHOUTSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:3 | CTICHOUTSTATUS | R | RW | 0 | Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. |

3.8.6.12 CM0P_CTI_CTIGATE

Description: Enable CTI Channel Gate Register

Address: 0xF0002140

Offset: 0x140

Retention: Retained

IsDeepSleep: No

Comment: The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|------------------|------------------|------------------|------------------|
| Name | None [7:4] | | | | CTIGATEEN3 [3:3] | CTIGATEEN2 [2:2] | CTIGATEEN1 [1:1] | CTIGATEEN0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | CTIGATEEN0 | RW | R | 1 | Enable CTICHOUT0. Set to 0 to disable channel propagation. |
| 1 | CTIGATEEN1 | RW | R | 1 | Enable CTICHOUT1. Set to 0 to disable channel propagation. |
| 2 | CTIGATEEN2 | RW | R | 1 | Enable CTICHOUT2. Set to 0 to disable channel propagation. |
| 3 | CTIGATEEN3 | RW | R | 1 | Enable CTICHOUT3. Set to 0 to disable channel propagation. |

3.8.6.13 CM0P_CTL_ASICCTL

Description: External Multiplexor Control Register
Address: 0xF0002144
Offset: 0x144
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | ASICCTL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | ASICCTL | RW | R | 0 | Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. |

3.8.6.14 CM0P_CTLITCHINACK

Description: ITCHINACK Register
Address: 0xF0002EDC
Offset: 0xEDC
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------------|---|---|---|
| Name | None [7:4] | | | | CTCHINACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:3 | CTCHINACK | W | R | 0 | Set the value of the CTCHINACK outputs |

3.8.6.15 CM0P_CTL_ITTRIGINACK

Description: ITTRIGINACK Register
Address: 0xF0002EE0
Offset: 0xEE0
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | CTTRIGINACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:7 | CTTRIGINACK | W | R | 0 | Set the value of the CTTRIGINACK outputs |

3.8.6.16 CM0P_CTLITCHOUT

Description: ITCHOUT Register
Address: 0xF0002EE4
Offset: 0xEE4
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | CTCHOUT [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--------------------------------------|
| 0:3 | CTCHOUT | W | R | 0 | Set the value of the CTCHOUT outputs |

3.8.6.17 CM0P_CTL_ITTRIGOUT

Description: ITTRIGOUT Register
Address: 0xF0002EE8
Offset: 0xEE8
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | CTTRIGOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:7 | CTTRIGOUT | W | R | 0 | Set the value of the CTTRIGOUT outputs |

3.8.6.18 CM0P_CTLITCHOUTACK

Description: ITCHOUTACK Register
Address: 0xF0002EEC
Offset: 0xEEC
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|------------------|---|---|---|
| Name | None [7:4] | | | | CTCHOUTACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:3 | CTCHOUTACK | R | W | 0 | Read the values of the CTCHOUTACK inputs |

3.8.6.19 CM0P_CTI_ITTRIGOUTACK

Description: ITTRIGOUTACK Register
Address: 0xF0002EF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | CTTRIGOUTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:7 | CTTRIGOUTACK | R | W | 0 | Read the values of the CTTRIGOUTACK inputs |

3.8.6.20 CM0P_CTI_ITCHIN

Description: ITCHIN Register
Address: 0xF0002EF4
Offset: 0xEF4
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------|---|---|---|
| Name | None [7:4] | | | | CTCHIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--------------------------------------|
| 0:3 | CTCHIN | R | W | 0 | Read the values of the CTCHIN inputs |

3.8.6.21 CM0P_CTL_ITTRIGIN

Description: ITTRIGIN Register
Address: 0xF0002EF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | CTTRIGIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:7 | CTTRIGIN | R | W | 0 | Read the values of the CTTRIGIN inputs |

3.8.6.22 CM0P_CTI_ITCTRL

Description: Integration Mode Control Register
Address: 0xF0002F00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment: This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|------------|
| Name | None [7:1] | | | | | | | MODE [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

3.8.6.23 CM0P_CTI_CLAIMSET

Description: Claim Tag Set Register

Address: 0xF0002FA0

Offset: 0xFA0

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.

Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

3.8.6.24 CM0P_CTI_CLAIMCLR

Description: Claim Tag Clear Register
Address: 0xF0002FA4
Offset: 0xFA4
Retention: Retained
IsDeepSleep: No
Comment: This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

3.8.6.25 CM0P_CTI_LOCKACCESS

Description: Lock Access Register

Address: 0xF0002FB0

Offset: 0xFB0

Retention: Retained

IsDeepSleep: No

Comment: This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-------------------|---|---|---|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

3.8.6.26 CM0P_CTI_LOCKSTATUS

Description: Lock Status Register

Address: 0xF0002FB4

Offset: 0xFB4

Retention: Retained

IsDeepSleep: No

Comment: This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.

This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------------------|----------------------------------|-----------------|
| Name | None [7:3] | | | | | IMPLEMENT S_8B [2:2] | ACCESS _PE MITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

3.8.6.28 CM0P_CTI_DEVID

Description: Device Configuration Register

Address: 0xF0002FC8

Offset: 0xFC8

Retention: Retained

IsDeepSleep: No

Comment: This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.

Default: 0x40800

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----------------|----------------|----|----|----|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | NRTRIG [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 0:4 | NRMUXING | R | R | 0 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

3.8.6.29 CM0P_CTI_DEVTYPE

Description: Device Type Identifier Register
Address: 0xF0002FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment: 0x14 indicates this device has a major type of debug control logic component (0x4) and sub-type corresponding to cross trigger (0x1).
Default: 0x14

Bit-field Table

Bit-field Table

| | | | | | | | | |
|------|----------------|---|---|---|-------------|---|---|---|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| | | | | | | | | |
|------|-------------|----|----|----|----|----|---|---|
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |

| | | | | | | | | |
|------|--------------|----|----|----|----|----|----|----|
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |

| | | | | | | | | |
|------|--------------|----|----|----|----|----|----|----|
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|-------------------------------|
| 0:3 | CLASS | R | R | 4 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

3.8.6.30 CM0P_CTI_PID4

Description: Peripheral Identification Register 4
Address: 0xF0002FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

3.8.6.31 CM0P_CTL_PID5

Description: Peripheral Identification Register 5
Address: 0xF0002FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.6.32 CM0P_CTL_PID6

Description: Peripheral Identification Register 6
Address: 0xF0002FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.6.33 CM0P_CTL_PID7

Description: Peripheral Identification Register 7
Address: 0xF0002FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.6.34 CM0P_CTI_PID0

Description: Peripheral Identification Register 0
Address: 0xF0002FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA6

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 166 | N/A |

3.8.6.35 CM0P_CTL_PID1

Description: Peripheral Identification Register 1
Address: 0xF0002FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 185 | N/A |

3.8.6.36 CM0P_CTL_PID2

Description: Peripheral Identification Register 2
Address: 0xF0002FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 11 | N/A |

3.8.6.37 CM0P_CTI_PID3

Description: Peripheral Identification Register 3
Address: 0xF0002FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|----------------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

3.8.6.38 CM0P_CTI_CID0

Description: Component Identification Register 0
Address: 0xF0002FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

3.8.6.39 CM0P_CTI_CID1

Description: Component Identification Register 1
Address: 0xF0002FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 144 | N/A |

3.8.6.40 CM0P_CTI_CID2

Description: Component Identification Register 2
Address: 0xF0002FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

3.8.6.41 CM0P_CTI_CID3

Description: Component Identification Register 3
Address: 0xF0002FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

3.8.7 MTB

3.8.7.1 CM0P_MTB_POSITION

Description: POSITION register

Address: 0xF0003000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: Contains the trace write pointer and the wrap bit. Available in all MTB configurations. You can modify all fields by software. Automatic hardware mechanisms update all fields. A debug agent might use the WRAP bit to determine whether the trace information above and below the pointer address is valid.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|------------|------------|---|
| Name | | | | | | WRAP [2:2] | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | POINTER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | POINTER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | POINTER [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 2 | WRAP | RW | RW | X | This bit is set to 1 automatically when the POINTER value wraps as determined by the MASTER.MASK field in the MASTER Trace Control Register. |
| 3:31 | POINTER | RW | RW | X | <p>Trace packet location pointer. Because a packet consists of two words, the POINTER field is the location of the first word of a packet. This field contains bits [31:3] of the address, in the SRAM, where the next trace packet will be written. The field points to an unused location and is automatically incremented.</p> <p>A debug agent can calculate the system address, on the AHB-Lite bus, of the SRAM location pointed to by the POSITION register using the following equation:</p> $\text{system address} = \text{BASE} + ((\text{P} + (2^{\text{AWIDTH}} - (\text{BASE} \bmod 2^{\text{AWIDTH}}))) \bmod 2^{\text{AWIDTH}}).$ <p>Where P = POSITION AND 0xFFFF_FFF8. Where BASE is the BASE register value.</p> <p>Note:</p> <ul style="list-style-type: none"> - The size of the SRAM is parameterized and the most significant bits of the POINTER field can be RAZ/WI, depending on the AWIDTH parameter value. - POSITION register bits greater than or equal to AWIDTH are RAZ/WI, therefore, the active POINTER field bits are [AWIDTH-4:0]. - The POINTER field value is relative to the base address of the SRAM in the system memory map. |

3.8.7.2 CM0P_MTB_MASTER

Description: MASTER register

Address: 0xF0003004

Offset: 0x4

Retention: Retained

IsDeepSleep: No

Comment: Contains:

- The main trace enable bit.

- Other trace control fields.

Usage constraints - Before the MASTER.EN or MASTER.TSTARTEN bits are set to 1, software must initialize the POSITION and FLOW registers.

- If the FLOW.WATERMARK field is used to stop tracing or to halt the processor, the MASTER.MASK field must still be set to a value that prevents the POSITION.POINTER field from wrapping before it reaches the FLOW.WATERMARK value.

- The EDBGREQ output value is also affected by the Debug authentication interface.

Configurations: Available in all MTB configurations.

Attributes:

- You can modify all fields by software.

- Automatic hardware mechanisms update the EN and HALTREQ bits.

Following example MASK and POINTER values to illustrate the effect of the MASK field on the POINTER.

MASK POINTER POINTER + 1 POINTER next

0x0 0x1 0x2 0x0

0x0 0x5 0x6 0x4

0x3 0xF 0x10 0x0

0x3 0x1F 0x20 0x10

Default: 0x80

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|------------------|-------------------|------------|---|---|---|---|
| Name | SFRWPRIV [7:7] | TSTOPEN [6:6] | TSTARTEN [5:5] | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------------|------------------|
| Name | None [15:10] | | | | | | HALTREQ [9:9] | RAMPRIV [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|--------------|----|----|----|----|----|----|
| Name | EN [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:4 | MASK | RW | R | X | <p>This value determines the maximum size of the trace buffer in SRAM. It specifies the most-significant bit of the POSITION.POINTER field that can be updated by automatic increment. If the trace tries to advance past this power of two, the POSITION.WRAP bit is set to 1, the POSITION.POINTER[MASK:0] bits are set to zero, and the POSITION.POINTER[AWIDTH-4:MASK+1] bits remain unchanged.</p> <p>This field causes the trace packet information to be stored in a circular buffer of size 2(MASK+4) bytes, that can be positioned in memory at multiples of this size.</p> <p>Valid values of this field are zero to AWIDTH-4. Values greater than the maximum have the same effect as the maximum.</p> |
| 5 | TSTARTEN | RW | R | 0 | Trace start input enable. If this bit is 1 and the TSTART signal is HIGH, then the EN bit is set to 1. Tracing continues until a stop condition occurs. |
| 6 | TSTOPEN | RW | R | 0 | Trace stop input enable. If this bit is 1 and the TSTOP signal is HIGH, then the EN bit is set to 0. If a trace packet is being written to memory, the write is completed before tracing is stopped. |
| 7 | SFRWPRIV | RW | R | 1 | <p>Special Function Register Write Privilege bit. If this bit is 0, then User or Privileged AHB-Lite read and write accesses to the Special Function Registers are permitted. If this bit is 1, then only Privileged write accesses are permitted and User write accesses are ignored. The HPROT[1] signal determines if an access is User or Privileged.</p> <p>Note</p> <ul style="list-style-type: none"> - SFR read accesses are not controlled by this bit and are always permitted. - This bit is implemented only if User/Privilege support is present in the MTB configuration. If User/Privilege support is absent, then the behavior of this bit is RAZ/WI and the value of the HPROT[1] signal is ignored. |
| 8 | RAMPRIV | RW | R | 0 | <p>SRAM Privilege bit. If this bit is 0, then User or Privileged AHB-Lite read and write accesses to the SRAM are permitted. If this bit is 1, then only Privileged AHB-Lite read and write accesses to the SRAM are permitted and User accesses are RAZ/WI. The HPROT[1] signal determines if an access is User or Privileged.</p> <p>Note</p> <p>This bit is implemented only if User/Privilege support is present in the MTB configuration. If User/Privilege support is absent, then the behavior of this bit is RAZ/WI and the value of the HPROT[1] signal is ignored.</p> |
| 9 | HALTREQ | RW | RW | 0 | <p>Halt request bit. This bit is connected to the halt request signal of the trace logic, EDBGRQ. When HALTREQ is set to 1, EDBGRQ is asserted if DBGEN is also HIGH.</p> <p>The HALTREQ bit can be automatically set to 1 using the FLOW.WATERMARK field.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 31 | EN | RW | RW | 0 | <p>Main trace enable bit.</p> <p>When this bit is 1 trace data is written into the SRAM memory location addressed by POSITION.POINTER.</p> <p>The POSITION.POINTER value auto increments after the trace data packet is written.</p> <p>The EN bit can be automatically set to 0 using the FLOW.WATERMARK field and the FLOW.AUTOSTOP bit.</p> <p>The EN bit is automatically set to 1 if the TSTARTEN bit is 1 and the TSTART signal is HIGH.</p> <p>The EN bit is automatically set to 0 if TSTOPEN bit is 1 and the TSTOP signal is HIGH.</p> <p>Note:</p> <p>If the EN bit is set to 0 because the FLOW.WATERMARK field is set, then it is not automatically set to 1 if the TSTARTEN bit is 1 and the TSTART input is HIGH. In this case tracing can only be restarted if the FLOW.WATERMARK or POSITION.POINTER value is changed by software.</p> |

3.8.7.3 CM0P_MTB_FLOW

Description: FLOW register

Address: 0xF0003008

Offset: 0x8

Retention: Retained

IsDeepSleep: No

Comment: Contains:

- The WATERMARK address.

- The AUTOSTOP and AUTOHALT control bits.

Usage constraints: There are no additional usage constraints.

Configurations: Available in all MTB configurations.

Attributes: You can modify all fields by software.

Note

- If you stop tracing, using the watermark auto stop feature, you cannot restart tracing until software clears the watermark auto stop. You can achieve this in one of the following ways:

- Changing the POSITION.POINTER field value to point to the beginning of the trace buffer.

- Setting the FLOW.AUTOSTOP bit to 0.

- A debug agent can use the AUTOSTOP bit to fill the trace buffer once only without halting the processor.

- A debug agent can use the AUTOHALT bit to fill the trace buffer once before causing the Cortex-M0+ processor to enter the Debug state. To enter Debug state, the Cortex-M0+ processor might have to perform additional branch type operations. Therefore you must set the WATERMARK field below the final entry in the trace buffer region.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|------------|----------------|----------------|
| Name | | | | | | None [2:2] | AUTOHALT [1:1] | AUTOSTOP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | WATERMARK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | WATERMARK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | WATERMARK [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | AUTOSTOP | RW | R | 0 | If this bit is 1 and WATERMARK is equal to POSITION.POINTER, then the MASTER.EN bit is automatically set to 0. This stops tracing. |
| 1 | AUTOHALT | RW | R | 0 | If this bit is 1 and WATERMARK is equal to POSITION.POINTER, then the MASTER.HALTREQ bit is automatically set to 1. If the DBGGEN signal is HIGH, the MTB asserts this halt request to the Cortex-M0+ processor by asserting the EDBGREQ signal. |
| 3:31 | WATERMARK | RW | R | X | WATERMARK value. This field contains an address in the same format as the POSITION.POINTER field. When the POSITION.POINTER matches the WATERMARK field value, actions defined by the AUTOHALT and AUTOSTOP bits are performed. |

3.8.7.4 CM0P_MTB_BASE

Description: BASE register
Address: 0xF000300C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Purpose: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.
Usage constraints: There are no additional usage constraints.
Configurations: Available in all MTB configurations.
Default: 0xF0010000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | BASE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | BASE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | BASE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | BASE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | BASE | R | R | 4026597376 | The value provided is the value of the SRAMBASEADDR[31:0] signal. MTB SRAM base address in the processor memory map, which is fixed for this platform. |

3.8.7.5 CM0P_MTB_LA

Description: Lock Access register
Address: 0xF0003FB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.7.6 CM0P_MTB_LS

Description: Lock Status register
Address: 0xF0003FB4
Offset: 0xFB4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.7.7 CM0P_MTB_AS

Description: Authentication Status register
Address: 0xF0003FB8
Offset: 0xFB8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|------------|-------------|------------|-------------|
| Name | | | | | AS_3 [3:3] | NIDEN [2:2] | AS_1 [1:1] | DBGEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | AS_31TO4 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | AS_31TO4 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | AS_31TO4 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---------------------------|
| 0 | DBGEN | R | R | 0 | Invasive debug enable |
| 1 | AS_1 | R | R | 1 | N/A |
| 2 | NIDEN | R | R | 0 | Non-invasive debug enable |
| 3 | AS_3 | R | R | 1 | N/A |
| 4:31 | AS_31TO4 | R | R | 0 | N/A |

3.8.7.8 CM0P_MTB_DARCH

Description: Device Architecture register
Address: 0xF0003FBC
Offset: 0xFBC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x47700A31

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|-------------------|------------------|----|----|----|
| Name | ARCH_ID [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | ARCH_ID [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | | | | RES_20 [20:20] | REVISION [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ARCHITECT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 0:15 | ARCH_ID | R | R | 2609 | Basic Trace Router Architecture Major Architecture Revision 0 |
| 16:19 | REVISION | R | R | 0 | Minor Architecture Revision |
| 20 | RES_20 | R | R | 1 | Reserved |
| 21:31 | ARCHITECT | R | R | 571 | Architect ARM |

3.8.7.9 CM0P_MTB_DCFG

Description: Device Configuration register
Address: 0xF0003FC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.7.10 CM0P_MTB_DID

Description: Device Type Identifier register.
Address: 0xF0003FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x31

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|-------------|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--------------------|
| 0:3 | CLASS | R | R | 1 | Trace Sink |
| 4:7 | SUB_TYPE | R | R | 3 | Basic Trace Router |

3.8.7.11 CM0P_MTB_PID4

Description: Peripheral Identification Register 4.
Address: 0xF0003FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

3.8.7.12 CM0P_MTB_PID5

Description: Peripheral Identification Register 5.
Address: 0xF0003FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.7.13 CM0P_MTB_PID6

Description: Peripheral Identification Register 6.
Address: 0xF0003FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.7.14 CM0P_MTB_PID7

Description: Peripheral Identification Register 7.
Address: 0xF0003FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

3.8.7.15 CM0P_MTB_PID0

Description: Peripheral Identification Register 0.
Address: 0xF0003FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x32

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 50 | N/A |

3.8.7.16 CM0P_MTB_PID1

Description: Peripheral Identification Register 1.
Address: 0xF0003FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 185 | N/A |

3.8.7.17 CM0P_MTB_PID2

Description: Peripheral Identification Register 2.
Address: 0xF0003FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 27 | N/A |

3.8.7.18 CM0P_MTB_PID3

Description: Peripheral Identification Register 3.
Address: 0xF0003FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|----------------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

3.8.7.19 CM0P_MTB_CID0

Description: Component Identification Register 0.
Address: 0xF0003FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

3.8.7.20 CM0P_MTB_CID1

Description: Component Identification Register 1.
Address: 0xF0003FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 144 | N/A |

3.8.7.21 CM0P_MTB_CID2

Description: Component Identification Register 2.
Address: 0xF0003FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

3.8.7.22 CM0P_MTB_CID3

Description: Component Identification Register 3.
Address: 0xF0003FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

4 CM4

| | |
|---------------------|------------------------------|
| Description | Cortex-M4 specific registers |
| Base Address | 0xE0000000 |
| Size | 0x20000000 |
| Slave Num | SYSTEM |

4.1 ITM

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------------------------------|
| CM4_ITM_STIM0 | 0xE0000000 | FULL | Stimulus Port registers |
| CM4_ITM_STIM1 | 0xE0000004 | FULL | Stimulus Port registers |
| CM4_ITM_STIM2 | 0xE0000008 | FULL | Stimulus Port registers |
| CM4_ITM_STIM3 | 0xE000000C | FULL | Stimulus Port registers |
| CM4_ITM_STIM4 | 0xE0000010 | FULL | Stimulus Port registers |
| CM4_ITM_STIM5 | 0xE0000014 | FULL | Stimulus Port registers |
| CM4_ITM_STIM6 | 0xE0000018 | FULL | Stimulus Port registers |
| CM4_ITM_STIM7 | 0xE000001C | FULL | Stimulus Port registers |
| CM4_ITM_STIM8 | 0xE0000020 | FULL | Stimulus Port registers |
| CM4_ITM_STIM9 | 0xE0000024 | FULL | Stimulus Port registers |
| CM4_ITM_STIM10 | 0xE0000028 | FULL | Stimulus Port registers |
| CM4_ITM_STIM11 | 0xE000002C | FULL | Stimulus Port registers |
| CM4_ITM_STIM12 | 0xE0000030 | FULL | Stimulus Port registers |
| CM4_ITM_STIM13 | 0xE0000034 | FULL | Stimulus Port registers |
| CM4_ITM_STIM14 | 0xE0000038 | FULL | Stimulus Port registers |
| CM4_ITM_STIM15 | 0xE000003C | FULL | Stimulus Port registers |
| CM4_ITM_STIM16 | 0xE0000040 | FULL | Stimulus Port registers |
| CM4_ITM_STIM17 | 0xE0000044 | FULL | Stimulus Port registers |
| CM4_ITM_STIM18 | 0xE0000048 | FULL | Stimulus Port registers |
| CM4_ITM_STIM19 | 0xE000004C | FULL | Stimulus Port registers |
| CM4_ITM_STIM20 | 0xE0000050 | FULL | Stimulus Port registers |
| CM4_ITM_STIM21 | 0xE0000054 | FULL | Stimulus Port registers |
| CM4_ITM_STIM22 | 0xE0000058 | FULL | Stimulus Port registers |
| CM4_ITM_STIM23 | 0xE000005C | FULL | Stimulus Port registers |
| CM4_ITM_STIM24 | 0xE0000060 | FULL | Stimulus Port registers |
| CM4_ITM_STIM25 | 0xE0000064 | FULL | Stimulus Port registers |
| CM4_ITM_STIM26 | 0xE0000068 | FULL | Stimulus Port registers |
| CM4_ITM_STIM27 | 0xE000006C | FULL | Stimulus Port registers |
| CM4_ITM_STIM28 | 0xE0000070 | FULL | Stimulus Port registers |
| CM4_ITM_STIM29 | 0xE0000074 | FULL | Stimulus Port registers |
| CM4_ITM_STIM30 | 0xE0000078 | FULL | Stimulus Port registers |
| CM4_ITM_STIM31 | 0xE000007C | FULL | Stimulus Port registers |
| CM4_ITM_TER | 0xE0000E00 | FULL | Trace Enable Register |
| CM4_ITM_TPR | 0xE0000E40 | FULL | ITM Trace Privilege Register |
| CM4_ITM_TCR | 0xE0000E80 | FULL | Trace Control Register |
| CM4_ITM_LAR | 0xE0000FB0 | FULL | Lock Access Register |
| CM4_ITM_LSR | 0xE0000FB4 | FULL | Lock Status Register |
| CM4_ITM_PID4 | 0xE0000FD0 | FULL | Peripheral Identification Register 4. |
| CM4_ITM_PID5 | 0xE0000FD4 | FULL | Peripheral Identification Register 5. |
| CM4_ITM_PID6 | 0xE0000FD8 | FULL | Peripheral Identification Register 6. |
| CM4_ITM_PID7 | 0xE0000FDC | FULL | Peripheral Identification Register 7. |
| CM4_ITM_PID0 | 0xE0000FE0 | FULL | Peripheral Identification Register 0. |
| CM4_ITM_PID1 | 0xE0000FE4 | FULL | Peripheral Identification Register 1. |
| CM4_ITM_PID2 | 0xE0000FE8 | FULL | Peripheral Identification Register 2. |
| CM4_ITM_PID3 | 0xE0000FEC | FULL | Peripheral Identification Register 3. |
| CM4_ITM_CID0 | 0xE0000FF0 | FULL | Component Identification Register 0. |
| CM4_ITM_CID1 | 0xE0000FF4 | FULL | Component Identification Register 1. |
| CM4_ITM_CID2 | 0xE0000FF8 | FULL | Component Identification Register 2. |
| CM4_ITM_CID3 | 0xE0000FFC | FULL | Component Identification Register 3. |

4.2 DWT

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|---------------------------------------|
| CM4_DWT_CTRL | 0xE0001000 | FULL | Control register |
| CM4_DWT_CYCCNT | 0xE0001004 | FULL | Cycle Count register |
| CM4_DWT_CPICNT | 0xE0001008 | FULL | CPI Count register |
| CM4_DWT_EXCCNT | 0xE000100C | FULL | Exception Overhead Count register |
| CM4_DWT_SLEEPCNT | 0xE0001010 | FULL | Sleep Count register |
| CM4_DWT_LSUCNT | 0xE0001014 | FULL | LSU Count register |
| CM4_DWT_FOLDCNT | 0xE0001018 | FULL | Folded-instruction Count register |
| CM4_DWT_PCSR | 0xE000101C | FULL | Program Counter Sample Register |
| CM4_DWT_COMP0 | 0xE0001020 | FULL | Comparator registers |
| CM4_DWT_MASK0 | 0xE0001024 | FULL | Comparator Mask registers |
| CM4_DWT_FUNCTION0 | 0xE0001028 | FULL | Comparator Function registers |
| CM4_DWT_COMP1 | 0xE0001030 | FULL | Comparator registers |
| CM4_DWT_MASK1 | 0xE0001034 | FULL | Comparator Mask registers |
| CM4_DWT_FUNCTION1 | 0xE0001038 | FULL | Comparator Function registers |
| CM4_DWT_COMP2 | 0xE0001040 | FULL | Comparator registers |
| CM4_DWT_MASK2 | 0xE0001044 | FULL | Comparator Mask registers |
| CM4_DWT_FUNCTION2 | 0xE0001048 | FULL | Comparator Function registers |
| CM4_DWT_COMP3 | 0xE0001050 | FULL | Comparator registers |
| CM4_DWT_MASK3 | 0xE0001054 | FULL | Comparator Mask registers |
| CM4_DWT_FUNCTION3 | 0xE0001058 | FULL | Comparator Function registers |
| CM4_DWT_PID4 | 0xE0001FD0 | FULL | Peripheral Identification Register 4. |
| CM4_DWT_PID5 | 0xE0001FD4 | FULL | Peripheral Identification Register 5. |
| CM4_DWT_PID6 | 0xE0001FD8 | FULL | Peripheral Identification Register 6. |
| CM4_DWT_PID7 | 0xE0001FDC | FULL | Peripheral Identification Register 7. |
| CM4_DWT_PID0 | 0xE0001FE0 | FULL | Peripheral Identification Register 0. |
| CM4_DWT_PID1 | 0xE0001FE4 | FULL | Peripheral Identification Register 1. |
| CM4_DWT_PID2 | 0xE0001FE8 | FULL | Peripheral Identification Register 2. |
| CM4_DWT_PID3 | 0xE0001FEC | FULL | Peripheral Identification Register 3. |
| CM4_DWT_CID0 | 0xE0001FF0 | FULL | Component Identification Register 0. |
| CM4_DWT_CID1 | 0xE0001FF4 | FULL | Component Identification Register 1. |
| CM4_DWT_CID2 | 0xE0001FF8 | FULL | Component Identification Register 2. |
| CM4_DWT_CID3 | 0xE0001FFC | FULL | Component Identification Register 3. |

4.3 FPB

| Register Name | Address | Permission | Description |
|---------------|------------|------------|---------------------------------------|
| CM4_FPB_CTRL | 0xE0002000 | FULL | FlashPatch Control Register |
| CM4_FPB_REMAP | 0xE0002004 | FULL | FlashPatch Remap register |
| CM4_FPB_COMP0 | 0xE0002008 | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP1 | 0xE000200C | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP2 | 0xE0002010 | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP3 | 0xE0002014 | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP4 | 0xE0002018 | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP5 | 0xE000201C | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP6 | 0xE0002020 | FULL | FlashPatch Comparator register |
| CM4_FPB_COMP7 | 0xE0002024 | FULL | FlashPatch Comparator register |
| CM4_FPB_PID4 | 0xE0002FD0 | FULL | Peripheral Identification Register 4. |
| CM4_FPB_PID5 | 0xE0002FD4 | FULL | Peripheral Identification Register 5. |
| CM4_FPB_PID6 | 0xE0002FD8 | FULL | Peripheral Identification Register 6. |
| CM4_FPB_PID7 | 0xE0002FDC | FULL | Peripheral Identification Register 7. |
| CM4_FPB_PID0 | 0xE0002FE0 | FULL | Peripheral Identification Register 0. |
| CM4_FPB_PID1 | 0xE0002FE4 | FULL | Peripheral Identification Register 1. |
| CM4_FPB_PID2 | 0xE0002FE8 | FULL | Peripheral Identification Register 2. |
| CM4_FPB_PID3 | 0xE0002FEC | FULL | Peripheral Identification Register 3. |
| CM4_FPB_CID0 | 0xE0002FF0 | FULL | Component Identification Register 0. |
| CM4_FPB_CID1 | 0xE0002FF4 | FULL | Component Identification Register 1. |
| CM4_FPB_CID2 | 0xE0002FF8 | FULL | Component Identification Register 2. |
| CM4_FPB_CID3 | 0xE0002FFC | FULL | Component Identification Register 3. |

4.4 SCS

| Register Name | Address | Permission | Description |
|------------------|------------|------------|-------------------------------------|
| CM4_SCS_ACTLR | 0xE000E008 | FULL | Auxiliary Control Register |
| CM4_SCS_SYST_CSR | 0xE000E010 | FULL | SysTick Control and Status Register |

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|------------------------------------|
| CM4_SCS_SYST_RVR | 0xE000E014 | FULL | SysTick Reload Value Register |
| CM4_SCS_SYST_CVR | 0xE000E018 | FULL | SysTick Current Value Register |
| CM4_SCS_SYST_CALIB | 0xE000E01C | FULL | SysTick Calibration value Register |
| CM4_SCS_NVIC_ISER0 | 0xE000E100 | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER1 | 0xE000E104 | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER2 | 0xE000E108 | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER3 | 0xE000E10C | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER4 | 0xE000E110 | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER5 | 0xE000E114 | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER6 | 0xE000E118 | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ISER7 | 0xE000E11C | FULL | Interrupt Set-Enable Registers |
| CM4_SCS_NVIC_ICER0 | 0xE000E180 | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER1 | 0xE000E184 | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER2 | 0xE000E188 | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER3 | 0xE000E18C | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER4 | 0xE000E190 | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER5 | 0xE000E194 | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER6 | 0xE000E198 | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ICER7 | 0xE000E19C | FULL | Interrupt Clear-Enable Registers |
| CM4_SCS_NVIC_ISPR0 | 0xE000E200 | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR1 | 0xE000E204 | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR2 | 0xE000E208 | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR3 | 0xE000E20C | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR4 | 0xE000E210 | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR5 | 0xE000E214 | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR6 | 0xE000E218 | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ISPR7 | 0xE000E21C | FULL | Interrupt Set-Pending Registers |
| CM4_SCS_NVIC_ICPR0 | 0xE000E280 | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR1 | 0xE000E284 | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR2 | 0xE000E288 | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR3 | 0xE000E28C | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR4 | 0xE000E290 | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR5 | 0xE000E294 | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR6 | 0xE000E298 | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_ICPR7 | 0xE000E29C | FULL | Interrupt Clear-Pending Registers |
| CM4_SCS_NVIC_IABR0 | 0xE000E300 | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR1 | 0xE000E304 | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR2 | 0xE000E308 | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR3 | 0xE000E30C | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR4 | 0xE000E310 | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR5 | 0xE000E314 | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR6 | 0xE000E318 | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IABR7 | 0xE000E31C | FULL | Interrupt Active Bit Registers |
| CM4_SCS_NVIC_IPR0 | 0xE000E400 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR1 | 0xE000E404 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR2 | 0xE000E408 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR3 | 0xE000E40C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR4 | 0xE000E410 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR5 | 0xE000E414 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR6 | 0xE000E418 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR7 | 0xE000E41C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR8 | 0xE000E420 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR9 | 0xE000E424 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR10 | 0xE000E428 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR11 | 0xE000E42C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR12 | 0xE000E430 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR13 | 0xE000E434 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR14 | 0xE000E438 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR15 | 0xE000E43C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR16 | 0xE000E440 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR17 | 0xE000E444 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR18 | 0xE000E448 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR19 | 0xE000E44C | FULL | Interrupt Priority Registers |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|--|
| CM4_SCS_NVIC_IPR20 | 0xE000E450 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR21 | 0xE000E454 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR22 | 0xE000E458 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR23 | 0xE000E45C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR24 | 0xE000E460 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR25 | 0xE000E464 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR26 | 0xE000E468 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR27 | 0xE000E46C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR28 | 0xE000E470 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR29 | 0xE000E474 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR30 | 0xE000E478 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR31 | 0xE000E47C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR32 | 0xE000E480 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR33 | 0xE000E484 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR34 | 0xE000E488 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR35 | 0xE000E48C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR36 | 0xE000E490 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR37 | 0xE000E494 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR38 | 0xE000E498 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR39 | 0xE000E49C | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR40 | 0xE000E4A0 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR41 | 0xE000E4A4 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR42 | 0xE000E4A8 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR43 | 0xE000E4AC | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR44 | 0xE000E4B0 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR45 | 0xE000E4B4 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR46 | 0xE000E4B8 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR47 | 0xE000E4BC | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR48 | 0xE000E4C0 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR49 | 0xE000E4C4 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR50 | 0xE000E4C8 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR51 | 0xE000E4CC | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR52 | 0xE000E4D0 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR53 | 0xE000E4D4 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR54 | 0xE000E4D8 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR55 | 0xE000E4DC | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR56 | 0xE000E4E0 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR57 | 0xE000E4E4 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR58 | 0xE000E4E8 | FULL | Interrupt Priority Registers |
| CM4_SCS_NVIC_IPR59 | 0xE000E4EC | FULL | Interrupt Priority Registers |
| CM4_SCS_CPUID | 0xE000ED00 | FULL | CPUID Base Register |
| CM4_SCS_ICSR | 0xE000ED04 | FULL | Interrupt Control and State Register |
| CM4_SCS_VTOR | 0xE000ED08 | FULL | Vector Table Offset Register |
| CM4_SCS_AIRCR | 0xE000ED0C | FULL | Application Interrupt and Reset Control Register |
| CM4_SCS_SCR | 0xE000ED10 | FULL | System Control Register |
| CM4_SCS_CCR | 0xE000ED14 | FULL | Configuration and Control Register |
| CM4_SCS_SHPR1 | 0xE000ED18 | FULL | System Handler Priority Register 1 |
| CM4_SCS_SHPR2 | 0xE000ED1C | FULL | System Handler Priority Register 2 |
| CM4_SCS_SHPR3 | 0xE000ED20 | FULL | System Handler Priority Register 3 |
| CM4_SCS_SHCSR | 0xE000ED24 | FULL | System Handler Control and State Register |
| CM4_SCS_CFSR | 0xE000ED28 | FULL | Configurable Fault Status Register |
| CM4_SCS_HFSR | 0xE000ED2C | FULL | HardFault Status Register |
| CM4_SCS_DFSR | 0xE000ED30 | FULL | Debug Fault Status Register |
| CM4_SCS_MMFAR | 0xE000ED34 | FULL | MemManage Fault Address Register |
| CM4_SCS_BFAR | 0xE000ED38 | FULL | BusFault Address Register |
| CM4_SCS_AFSR | 0xE000ED3C | FULL | Auxiliary Fault Status Register |
| CM4_SCS_CPACR | 0xE000ED88 | FULL | Coprocessor Access Control Register |
| CM4_SCS_MPU_TYPE | 0xE000ED90 | FULL | MPU Type Register |
| CM4_SCS_MPU_CTRL | 0xE000ED94 | FULL | MPU Control Register |
| CM4_SCS_MPU_RNR | 0xE000ED98 | FULL | MPU Region Number Register |
| CM4_SCS_MPU_RBAR | 0xE000ED9C | FULL | MPU Region Base Address Register |
| CM4_SCS_MPU_RASR | 0xE000EDA0 | FULL | MPU Region Attribute and Size Register |
| CM4_SCS_MPU_RBAR_A1 | 0xE000EDA4 | FULL | MPU alias registers |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|--|
| CM4_SCS_MPU_RASR_A1 | 0xE000EDA8 | FULL | MPU alias registers |
| CM4_SCS_MPU_RBAR_A2 | 0xE000EDAC | FULL | MPU alias registers |
| CM4_SCS_MPU_RASR_A2 | 0xE000EDB0 | FULL | MPU alias registers |
| CM4_SCS_MPU_RBAR_A3 | 0xE000EDB4 | FULL | MPU alias registers |
| CM4_SCS_MPU_RASR_A3 | 0xE000EDB8 | FULL | MPU alias registers |
| CM4_SCS_DHCSR | 0xE000EDF0 | FULL | Debug Halting Control and Status Register |
| CM4_SCS_DCRSR | 0xE000EDF4 | FULL | Debug Core Register Selector Register |
| CM4_SCS_DCRDR | 0xE000EDF8 | FULL | Debug Core Register Data Register |
| CM4_SCS_DEMCR | 0xE000EDFC | FULL | Debug Exception and Monitor Control Register |
| CM4_SCS_STIR | 0xE000EF00 | FULL | Software Triggered Interrupt Register |
| CM4_SCS_FPCCR | 0xE000EF34 | FULL | FP Context Control Register |
| CM4_SCS_FPCAR | 0xE000EF38 | FULL | FP Context Control Register |
| CM4_SCS_FPDSCR | 0xE000EF3C | FULL | FP Context Control Register |
| CM4_SCS_PID4 | 0xE000EFD0 | FULL | Peripheral Identification Register 4 |
| CM4_SCS_PID5 | 0xE000EFD4 | FULL | Peripheral Identification Register 5 |
| CM4_SCS_PID6 | 0xE000EFD8 | FULL | Peripheral Identification Register 6 |
| CM4_SCS_PID7 | 0xE000EFD0 | FULL | Peripheral Identification Register 7 |
| CM4_SCS_PID0 | 0xE000EFE0 | FULL | Peripheral Identification Register 0 |
| CM4_SCS_PID1 | 0xE000EFE4 | FULL | Peripheral Identification Register 1 |
| CM4_SCS_PID2 | 0xE000EFE8 | FULL | Peripheral Identification Register 2 |
| CM4_SCS_PID3 | 0xE000EFEC | FULL | Peripheral Identification Register 3 |
| CM4_SCS_CID0 | 0xE000EFF0 | FULL | Component Identification Register 0 |
| CM4_SCS_CID1 | 0xE000EFF4 | FULL | Component Identification Register 1 |
| CM4_SCS_CID2 | 0xE000EFF8 | FULL | Component Identification Register 2 |
| CM4_SCS_CID3 | 0xE000EFFC | FULL | Component Identification Register 3 |

4.5 ETM

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|---|
| CM4_ETM_CR | 0xE0041000 | FULL | Main Control Register |
| CM4_ETM_CCR | 0xE0041004 | FULL | Main Control Register |
| CM4_ETM_TRIGGER | 0xE0041008 | FULL | Trigger Event Register |
| CM4_ETM_SR | 0xE0041010 | FULL | ETM Status Register |
| CM4_ETM_SCR | 0xE0041014 | FULL | System Configuration Register |
| CM4_ETM_TEEVR | 0xE0041020 | FULL | TraceEnable Event Register |
| CM4_ETM_TECR1 | 0xE0041024 | FULL | TraceEnable Control 1 Register |
| CM4_ETM_FFLR | 0xE0041028 | FULL | FIFOFULL Level Register |
| CM4_ETM_CNTRLDVR1 | 0xE0041140 | FULL | Free-running counter reload value |
| CM4_ETM_SYNCFR | 0xE00411E0 | FULL | Synchronization Frequency Register |
| CM4_ETM_IDR | 0xE00411E4 | FULL | ID Register |
| CM4_ETM_CCER | 0xE00411E8 | FULL | Configuration Code Extension Register |
| CM4_ETM_TESSEICR | 0xE00411F0 | FULL | TraceEnable Start/Stop EmbeddedICE Control Register |
| CM4_ETM_TSEVR | 0xE00411F8 | FULL | Timestamp Event Register |
| CM4_ETM_TRACEIDR | 0xE0041200 | FULL | CoreSight Trace ID Register |
| CM4_ETM_IDR2 | 0xE0041208 | FULL | ETM ID Register 2 |
| CM4_ETM_PDSR | 0xE0041314 | FULL | Device Power-Down Status Register |
| CM4_ETM_ITMISCIN | 0xE0041EE0 | FULL | Integration Test Miscellaneous Inputs |
| CM4_ETM_ITTRIGOUT | 0xE0041EE8 | FULL | Integration Test Trigger Out |
| CM4_ETM_ITATBCTR2 | 0xE0041EF0 | FULL | ETM Integration Test ATB Control 2 |
| CM4_ETM_ITATBCTR0 | 0xE0041EF8 | FULL | ETM Integration Test ATB Control 0 |
| CM4_ETM_ITCTRL | 0xE0041F00 | FULL | Integration Mode Control Register |
| CM4_ETM_CLAIMSET | 0xE0041FA0 | FULL | Claim Tag Set Register |
| CM4_ETM_CLAIMCLR | 0xE0041FA4 | FULL | Claim Tag Clear Register |
| CM4_ETM_LAR | 0xE0041FB0 | FULL | Lock Access Register |
| CM4_ETM_LSR | 0xE0041FB4 | FULL | Lock Status Register |
| CM4_ETM_AUTHSTATUS | 0xE0041FB8 | FULL | Authentication Status Register |
| CM4_ETM_DEVTYPE | 0xE0041FCC | FULL | CoreSight Device Type Register |
| CM4_ETM_PID4 | 0xE0041FD0 | FULL | Peripheral Identification Register 4. |
| CM4_ETM_PID5 | 0xE0041FD4 | FULL | Peripheral Identification Register 5. |
| CM4_ETM_PID6 | 0xE0041FD8 | FULL | Peripheral Identification Register 6. |
| CM4_ETM_PID7 | 0xE0041FDC | FULL | Peripheral Identification Register 7. |
| CM4_ETM_PID0 | 0xE0041FE0 | FULL | Peripheral Identification Register 0. |
| CM4_ETM_PID1 | 0xE0041FE4 | FULL | Peripheral Identification Register 1. |

| Register Name | Address | Permission | Description |
|---------------|------------|------------|---------------------------------------|
| CM4_ETM_PID2 | 0xE0041FE8 | FULL | Peripheral Identification Register 2. |
| CM4_ETM_PID3 | 0xE0041FEC | FULL | Peripheral Identification Register 3. |
| CM4_ETM_CID0 | 0xE0041FF0 | FULL | Component Identification Register 0. |
| CM4_ETM_CID1 | 0xE0041FF4 | FULL | Component Identification Register 1. |
| CM4_ETM_CID2 | 0xE0041FF8 | FULL | Component Identification Register 2. |
| CM4_ETM_CID3 | 0xE0041FFC | FULL | Component Identification Register 3. |

4.6 CM4CTI

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|---|
| CM4_CM4CTI_CTICONTROL | 0xE0042000 | FULL | CTI Control Register |
| CM4_CM4CTI_CTIINTACK | 0xE0042010 | FULL | CTI Interrupt Acknowledge Register |
| CM4_CM4CTI_CTIAPPSET | 0xE0042014 | FULL | CTI Application Trigger Set Register |
| CM4_CM4CTI_CTIAPPCLEAR | 0xE0042018 | FULL | CTI Application Trigger Clear Register |
| CM4_CM4CTI_CTIAPPPULSE | 0xE004201C | FULL | CTI Application Pulse Register |
| CM4_CM4CTI_CTIINEN0 | 0xE0042020 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN1 | 0xE0042024 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN2 | 0xE0042028 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN3 | 0xE004202C | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN4 | 0xE0042030 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN5 | 0xE0042034 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN6 | 0xE0042038 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIINEN7 | 0xE004203C | FULL | CTI Trigger to Channel Enable Registers |
| CM4_CM4CTI_CTIOUTEN0 | 0xE00420A0 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN1 | 0xE00420A4 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN2 | 0xE00420A8 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN3 | 0xE00420AC | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN4 | 0xE00420B0 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN5 | 0xE00420B4 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN6 | 0xE00420B8 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTIOUTEN7 | 0xE00420BC | FULL | CTI Channel to Trigger Enable Registers |
| CM4_CM4CTI_CTITRIGINSTATUS | 0xE0042130 | FULL | CTI Trigger In Status Register |
| CM4_CM4CTI_CTITRIGOUTSTATUS | 0xE0042134 | FULL | CTI Trigger Out Status Register |
| CM4_CM4CTI_CTICHINSTATUS | 0xE0042138 | FULL | CTI Channel In Status Register |
| CM4_CM4CTI_CTICHOUTSTATUS | 0xE004213C | FULL | CTI Channel Out Status Register |
| CM4_CM4CTI_CTIGATE | 0xE0042140 | FULL | Enable CTI Channel Gate Register |
| CM4_CM4CTI_ASICCTL | 0xE0042144 | FULL | External Multiplexor Control Register |
| CM4_CM4CTI_ITCHINACK | 0xE0042EDC | FULL | ITCHINACK Register |
| CM4_CM4CTI_ITTRIGINACK | 0xE0042EE0 | FULL | ITTRIGINACK Register |
| CM4_CM4CTI_ITCHOUT | 0xE0042EE4 | FULL | ITCHOUT Register |
| CM4_CM4CTI_ITTRIGOUT | 0xE0042EE8 | FULL | ITTRIGOUT Register |
| CM4_CM4CTI_ITCHOUTACK | 0xE0042EEC | FULL | ITCHOUTACK Register |
| CM4_CM4CTI_ITTRIGOUTACK | 0xE0042EF0 | FULL | ITTRIGOUTACK Register |
| CM4_CM4CTI_ITCHIN | 0xE0042EF4 | FULL | ITCHIN Register |
| CM4_CM4CTI_ITTRIGIN | 0xE0042EF8 | FULL | ITTRIGIN Register |
| CM4_CM4CTI_ITCTRL | 0xE0042F00 | FULL | Integration Mode Control Register |
| CM4_CM4CTI_CLAIMSET | 0xE0042FA0 | FULL | Claim Tag Set Register |
| CM4_CM4CTI_CLAIMCLR | 0xE0042FA4 | FULL | Claim Tag Clear Register |
| CM4_CM4CTI_LOCKACCESS | 0xE0042FB0 | FULL | Lock Access Register |
| CM4_CM4CTI_LOCKSTATUS | 0xE0042FB4 | FULL | Lock Status Register |
| CM4_CM4CTI_AUTHSTATUS | 0xE0042FB8 | FULL | Authentication Status Register |
| CM4_CM4CTI_DEVID | 0xE0042FC8 | FULL | Device Configuration Register |
| CM4_CM4CTI_DEVTYPE | 0xE0042FCC | FULL | Device Type Identifier Register |
| CM4_CM4CTI_PID4 | 0xE0042FD0 | FULL | Peripheral Identification Register 4 |
| CM4_CM4CTI_PID5 | 0xE0042FD4 | FULL | Peripheral Identification Register 5 |
| CM4_CM4CTI_PID6 | 0xE0042FD8 | FULL | Peripheral Identification Register 6 |
| CM4_CM4CTI_PID7 | 0xE0042FDC | FULL | Peripheral Identification Register 7 |
| CM4_CM4CTI_PID0 | 0xE0042FE0 | FULL | Peripheral Identification Register 0 |
| CM4_CM4CTI_PID1 | 0xE0042FE4 | FULL | Peripheral Identification Register 1 |
| CM4_CM4CTI_PID2 | 0xE0042FE8 | FULL | Peripheral Identification Register 2 |
| CM4_CM4CTI_PID3 | 0xE0042FEC | FULL | Peripheral Identification Register 3 |
| CM4_CM4CTI_CID0 | 0xE0042FF0 | FULL | Component Identification Register 0 |
| CM4_CM4CTI_CID1 | 0xE0042FF4 | FULL | Component Identification Register 1 |
| CM4_CM4CTI_CID2 | 0xE0042FF8 | FULL | Component Identification Register 2 |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|-------------------------------------|
| CM4_CM4CTI_CID3 | 0xE0042FFC | FULL | Component Identification Register 3 |

4.7 ROM

| Register Name | Address | Permission | Description |
|---------------|------------|------------|--|
| CM4_ROM_SCS | 0xE007F000 | FULL | CM4 CoreSight ROM Table Peripheral #0 |
| CM4_ROM_DWT | 0xE007F004 | FULL | CM4 CoreSight ROM Table Peripheral #1 |
| CM4_ROM_FPB | 0xE007F008 | FULL | CM4 CoreSight ROM Table Peripheral #2 |
| CM4_ROM_ITM | 0xE007F00C | FULL | CM4 CoreSight ROM Table Peripheral #3 |
| CM4_ROM_CTI | 0xE007F010 | FULL | CM4 CoreSight ROM Table Peripheral #4 |
| CM4_ROM_ETM | 0xE007F014 | FULL | CM4 CoreSight ROM Table Peripheral #5 |
| CM4_ROM_CSMT | 0xE007FFC0 | FULL | CM4 CoreSight ROM Table Memory Type |
| CM4_ROM_PID4 | 0xE007FFD0 | FULL | CM4 CoreSight ROM Table Peripheral ID #4 |
| CM4_ROM_PID0 | 0xE007FFE0 | FULL | CM4 CoreSight ROM Table Peripheral ID #0 |
| CM4_ROM_PID1 | 0xE007FFE4 | FULL | CM4 CoreSight ROM Table Peripheral ID #1 |
| CM4_ROM_PID2 | 0xE007FFE8 | FULL | CM4 CoreSight ROM Table Peripheral ID #2 |
| CM4_ROM_PID3 | 0xE007FFEC | FULL | CM4 CoreSight ROM Table Peripheral ID #3 |
| CM4_ROM_CID0 | 0xE007FFF0 | FULL | CM4 CoreSight ROM Table Component ID #0 |
| CM4_ROM_CID1 | 0xE007FFF4 | FULL | CM4 CoreSight ROM Table Component ID #1 |
| CM4_ROM_CID2 | 0xE007FFF8 | FULL | CM4 CoreSight ROM Table Component ID #2 |
| CM4_ROM_CID3 | 0xE007FFFC | FULL | CM4 CoreSight ROM Table Component ID #3 |

4.8 TRCCTI

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| CM4_TRCCTI_CTICONTROL | 0xE0080000 | FULL | CTI Control Register |
| CM4_TRCCTI_CTIINTACK | 0xE0080010 | FULL | CTI Interrupt Acknowledge Register |
| CM4_TRCCTI_CTIAPPSET | 0xE0080014 | FULL | CTI Application Trigger Set Register |
| CM4_TRCCTI_CTIAPPCLEAR | 0xE0080018 | FULL | CTI Application Trigger Clear Register |
| CM4_TRCCTI_CTIAPPULSE | 0xE008001C | FULL | CTI Application Pulse Register |
| CM4_TRCCTI_CTIENEN0 | 0xE0080020 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN1 | 0xE0080024 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN2 | 0xE0080028 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN3 | 0xE008002C | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN4 | 0xE0080030 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN5 | 0xE0080034 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN6 | 0xE0080038 | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIENEN7 | 0xE008003C | FULL | CTI Trigger to Channel Enable Registers |
| CM4_TRCCTI_CTIOUTEN0 | 0xE00800A0 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN1 | 0xE00800A4 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN2 | 0xE00800A8 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN3 | 0xE00800AC | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN4 | 0xE00800B0 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN5 | 0xE00800B4 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN6 | 0xE00800B8 | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIOUTEN7 | 0xE00800BC | FULL | CTI Channel to Trigger Enable Registers |
| CM4_TRCCTI_CTIINSTATUS | 0xE0080130 | FULL | CTI Trigger In Status Register |
| CM4_TRCCTI_CTIOUTSTATUS | 0xE0080134 | FULL | CTI Trigger Out Status Register |
| CM4_TRCCTI_CTIINSTATUS | 0xE0080138 | FULL | CTI Channel In Status Register |
| CM4_TRCCTI_CTIOUTSTATUS | 0xE008013C | FULL | CTI Channel Out Status Register |
| CM4_TRCCTI_CTIIGATE | 0xE0080140 | FULL | Enable CTI Channel Gate Register |
| CM4_TRCCTI_ASICCTL | 0xE0080144 | FULL | External Multiplexor Control Register |
| CM4_TRCCTI_ITCHINACK | 0xE0080EDC | FULL | ITCHINACK Register |
| CM4_TRCCTI_ITTRIGINACK | 0xE0080EE0 | FULL | ITTRIGINACK Register |
| CM4_TRCCTI_ITCHOUT | 0xE0080EE4 | FULL | ITCHOUT Register |
| CM4_TRCCTI_ITTRIGOUT | 0xE0080EE8 | FULL | ITTRIGOUT Register |
| CM4_TRCCTI_ITCHOUTACK | 0xE0080EEC | FULL | ITCHOUTACK Register |
| CM4_TRCCTI_ITTRIGOUTACK | 0xE0080EF0 | FULL | ITTRIGOUTACK Register |
| CM4_TRCCTI_ITCHIN | 0xE0080EF4 | FULL | ITCHIN Register |
| CM4_TRCCTI_ITTRIGIN | 0xE0080EF8 | FULL | ITTRIGIN Register |
| CM4_TRCCTI_ITCTRL | 0xE0080F00 | FULL | Integration Mode Control Register |
| CM4_TRCCTI_CLAIMSET | 0xE0080FA0 | FULL | Claim Tag Set Register |
| CM4_TRCCTI_CLAIMCLR | 0xE0080FA4 | FULL | Claim Tag Clear Register |
| CM4_TRCCTI_LOCKACCESS | 0xE0080FB0 | FULL | Lock Access Register |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|--------------------------------------|
| CM4_TRCCTI_LOCKSTATUS | 0xE0080FB4 | FULL | Lock Status Register |
| CM4_TRCCTI_AUTHSTATUS | 0xE0080FB8 | FULL | Authentication Status Register |
| CM4_TRCCTI_DEVID | 0xE0080FC8 | FULL | Device Configuration Register |
| CM4_TRCCTI_DEVTYPE | 0xE0080FCC | FULL | Device Type Identifier Register |
| CM4_TRCCTI_PID4 | 0xE0080FD0 | FULL | Peripheral Identification Register 4 |
| CM4_TRCCTI_PID5 | 0xE0080FD4 | FULL | Peripheral Identification Register 5 |
| CM4_TRCCTI_PID6 | 0xE0080FD8 | FULL | Peripheral Identification Register 6 |
| CM4_TRCCTI_PID7 | 0xE0080FDC | FULL | Peripheral Identification Register 7 |
| CM4_TRCCTI_PID0 | 0xE0080FE0 | FULL | Peripheral Identification Register 0 |
| CM4_TRCCTI_PID1 | 0xE0080FE4 | FULL | Peripheral Identification Register 1 |
| CM4_TRCCTI_PID2 | 0xE0080FE8 | FULL | Peripheral Identification Register 2 |
| CM4_TRCCTI_PID3 | 0xE0080FEC | FULL | Peripheral Identification Register 3 |
| CM4_TRCCTI_CID0 | 0xE0080FF0 | FULL | Component Identification Register 0 |
| CM4_TRCCTI_CID1 | 0xE0080FF4 | FULL | Component Identification Register 1 |
| CM4_TRCCTI_CID2 | 0xE0080FF8 | FULL | Component Identification Register 2 |
| CM4_TRCCTI_CID3 | 0xE0080FFC | FULL | Component Identification Register 3 |

4.9 CSTF

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|--------------------------------------|
| CM4_CSTF_CSTFCTL | 0xE008C000 | FULL | Funnel Control Register |
| CM4_CSTF_CSTFPCTL | 0xE008C004 | FULL | Priority Control Register |
| CM4_CSTF_ITATBDATA0 | 0xE008CEE0 | FULL | Integration Register |
| CM4_CSTF_ITATBCTR2 | 0xE008CEF0 | FULL | Integration Register |
| CM4_CSTF_ITATBCTR1 | 0xE008CEF4 | FULL | Integration Register |
| CM4_CSTF_ITATBCTR0 | 0xE008CEF8 | FULL | Integration Register |
| CM4_CSTF_ITCTRL | 0xE008CF00 | FULL | Integration Mode Control Register |
| CM4_CSTF_CLAIMSET | 0xE008CFA0 | FULL | Claim Tag Set Register |
| CM4_CSTF_CLAIMCLR | 0xE008CFA4 | FULL | Claim Tag Clear Register |
| CM4_CSTF_LOCKACCESS | 0xE008CFB0 | FULL | Lock Access Register |
| CM4_CSTF_LOCKSTATUS | 0xE008CFB4 | FULL | Lock Status Register |
| CM4_CSTF_AUTHSTATUS | 0xE008CFB8 | FULL | Authentication Status Register |
| CM4_CSTF_DEVID | 0xE008CFC8 | FULL | Device ID |
| CM4_CSTF_DEVTYPE | 0xE008CFCC | FULL | Device Type Identifier Register |
| CM4_CSTF_PID4 | 0xE008CFD0 | FULL | Peripheral Identification Register 4 |
| CM4_CSTF_PID5 | 0xE008CFD4 | FULL | Peripheral Identification Register 5 |
| CM4_CSTF_PID6 | 0xE008CFD8 | FULL | Peripheral Identification Register 6 |
| CM4_CSTF_PID7 | 0xE008CFDC | FULL | Peripheral Identification Register 7 |
| CM4_CSTF_PID0 | 0xE008CFE0 | FULL | Peripheral Identification Register 0 |
| CM4_CSTF_PID1 | 0xE008CFE4 | FULL | Peripheral Identification Register 1 |
| CM4_CSTF_PID2 | 0xE008CFE8 | FULL | Peripheral Identification Register 2 |
| CM4_CSTF_PID3 | 0xE008CFEC | FULL | Peripheral Identification Register 3 |
| CM4_CSTF_CID0 | 0xE008CFF0 | FULL | Component Identification Register 0 |
| CM4_CSTF_CID1 | 0xE008CFF4 | FULL | Component Identification Register 1 |
| CM4_CSTF_CID2 | 0xE008CFF8 | FULL | Component Identification Register 2 |
| CM4_CSTF_CID3 | 0xE008CFFC | FULL | Component Identification Register 3 |

4.10 ETB

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|--------------------------------------|
| CM4_ETB_ETBRDP | 0xE008D004 | FULL | RAM Depth Register |
| CM4_ETB_ETBSTS | 0xE008D00C | FULL | Status Register |
| CM4_ETB_ETBRRD | 0xE008D010 | FULL | RAM Read Data Register |
| CM4_ETB_ETBRRP | 0xE008D014 | FULL | RAM Read Pointer Register |
| CM4_ETB_ETBRWP | 0xE008D018 | FULL | RAM Write Pointer Register |
| CM4_ETB_ETBTRG | 0xE008D01C | FULL | Trigger Counter Register |
| CM4_ETB_ETBCTL | 0xE008D020 | FULL | Control Register |
| CM4_ETB_ETBRWD | 0xE008D024 | FULL | RAM Write Data Register |
| CM4_ETB_ETBFFSR | 0xE008D300 | FULL | Formatter and Flush Status Register |
| CM4_ETB_ETBFFCR | 0xE008D304 | FULL | Formatter and Flush Control Register |
| CM4_ETB_ITMISCOPO | 0xE008DEE0 | FULL | Integration Register |
| CM4_ETB_ITTRFLINACK | 0xE008DEE4 | FULL | Integration Register |
| CM4_ETB_ITTRFLIN | 0xE008DEE8 | FULL | Integration Register |
| CM4_ETB_ITATBDATA0 | 0xE008DEEC | FULL | Integration Register |

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|--------------------------------------|
| CM4_ETB_ITATBCTR2 | 0xE008DEF0 | FULL | Integration Register |
| CM4_ETB_ITATBCTR1 | 0xE008DEF4 | FULL | Integration Register |
| CM4_ETB_ITATBCTR0 | 0xE008DEF8 | FULL | Integration Register |
| CM4_ETB_ITCTRL | 0xE008DF00 | FULL | Integration Mode Control Register |
| CM4_ETB_CLAIMSET | 0xE008DFA0 | FULL | Claim Tag Set Register |
| CM4_ETB_CLAIMCLR | 0xE008DFA4 | FULL | Claim Tag Clear Register |
| CM4_ETB_LOCKACCESS | 0xE008DFB0 | FULL | Lock Access Register |
| CM4_ETB_LOCKSTATUS | 0xE008DFB4 | FULL | Lock Status Register |
| CM4_ETB_AUTHSTATUS | 0xE008DFB8 | FULL | Authentication Status Register |
| CM4_ETB_DEVID | 0xE008DFC8 | FULL | Device ID |
| CM4_ETB_DEVTYPE | 0xE008DFCC | FULL | Device Type Identifier Register |
| CM4_ETB_PID4 | 0xE008DFD0 | FULL | Peripheral Identification Register 4 |
| CM4_ETB_PID5 | 0xE008DFD4 | FULL | Peripheral Identification Register 5 |
| CM4_ETB_PID6 | 0xE008DFD8 | FULL | Peripheral Identification Register 6 |
| CM4_ETB_PID7 | 0xE008DFDC | FULL | Peripheral Identification Register 7 |
| CM4_ETB_PID0 | 0xE008DFE0 | FULL | Peripheral Identification Register 0 |
| CM4_ETB_PID1 | 0xE008DFE4 | FULL | Peripheral Identification Register 1 |
| CM4_ETB_PID2 | 0xE008DFE8 | FULL | Peripheral Identification Register 2 |
| CM4_ETB_PID3 | 0xE008DFEC | FULL | Peripheral Identification Register 3 |
| CM4_ETB_CID0 | 0xE008DFF0 | FULL | Component Identification Register 0 |
| CM4_ETB_CID1 | 0xE008DFF4 | FULL | Component Identification Register 1 |
| CM4_ETB_CID2 | 0xE008DFF8 | FULL | Component Identification Register 2 |
| CM4_ETB_CID3 | 0xE008DFFC | FULL | Component Identification Register 3 |

4.11 TPIU

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|--|
| CM4_TPIU_TPIU_SSPPSR | 0xE008E000 | FULL | Supported Parallel Port Size Register |
| CM4_TPIU_TPIU_CSPSR | 0xE008E004 | FULL | Current Parallel Port Size Register |
| CM4_TPIU_TPIU_ACPR | 0xE008E010 | FULL | Asynchronous Clock Prescaler Register |
| CM4_TPIU_TPIU_SPPR | 0xE008E0F0 | FULL | Selected Pin Protocol Register |
| CM4_TPIU_TPIU_FFSR | 0xE008E300 | FULL | Formatter and Flush Status Register |
| CM4_TPIU_TPIU_FFCR | 0xE008E304 | FULL | Formatter and Flush Control Register |
| CM4_TPIU_TPIU_FSCR | 0xE008E308 | FULL | Formatter Synchronization Counter Register |
| CM4_TPIU_TRIGGER | 0xE008EEE8 | FULL | TRIGGER register |
| CM4_TPIU_FIFO_DATA_0 | 0xE008EEEC | FULL | Integration ETM Data |
| CM4_TPIU_ITATBCTR2 | 0xE008EEF0 | FULL | Integration Register |
| CM4_TPIU_ITATBCTR0 | 0xE008EEF8 | FULL | Integration Register |
| CM4_TPIU_FIFO_DATA_1 | 0xE008EEFC | FULL | Integration ITM Data |
| CM4_TPIU_ITCTRL | 0xE008EF00 | FULL | Integration Mode Control Register |
| CM4_TPIU_CLAIMSET | 0xE008EFA0 | FULL | Claim Tag Set Register |
| CM4_TPIU_CLAIMCLR | 0xE008EFA4 | FULL | Claim Tag Clear Register |
| CM4_TPIU_DEVID | 0xE008EFC8 | FULL | Device ID |
| CM4_TPIU_DEVTYPE | 0xE008EFC0 | FULL | Device Type Identifier Register |
| CM4_TPIU_PID4 | 0xE008EFD0 | FULL | Peripheral Identification Register 4 |
| CM4_TPIU_PID5 | 0xE008EFD4 | FULL | Peripheral Identification Register 5 |
| CM4_TPIU_PID6 | 0xE008EFD8 | FULL | Peripheral Identification Register 6 |
| CM4_TPIU_PID7 | 0xE008EFD0 | FULL | Peripheral Identification Register 7 |
| CM4_TPIU_PID0 | 0xE008EFE0 | FULL | Peripheral Identification Register 0 |
| CM4_TPIU_PID1 | 0xE008EFE4 | FULL | Peripheral Identification Register 1 |
| CM4_TPIU_PID2 | 0xE008EFE8 | FULL | Peripheral Identification Register 2 |
| CM4_TPIU_PID3 | 0xE008EFEC | FULL | Peripheral Identification Register 3 |
| CM4_TPIU_CID0 | 0xE008EFF0 | FULL | Component Identification Register 0 |
| CM4_TPIU_CID1 | 0xE008EFF4 | FULL | Component Identification Register 1 |
| CM4_TPIU_CID2 | 0xE008EFF8 | FULL | Component Identification Register 2 |
| CM4_TPIU_CID3 | 0xE008EFFC | FULL | Component Identification Register 3 |

4.12 ROMTABLE

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---------------------------------------|
| CM4_ROMTABLE_TRC_CTI | 0xE00FF000 | FULL | CM4 CoreSight ROM Table Peripheral #0 |
| CM4_ROMTABLE_TRC_CSTF | 0xE00FF004 | FULL | CM4 CoreSight ROM Table Peripheral #1 |
| CM4_ROMTABLE_TRC_ETB | 0xE00FF008 | FULL | CM4 CoreSight ROM Table Peripheral #2 |
| CM4_ROMTABLE_TRC_TPIU | 0xE00FF00C | FULL | CM4 CoreSight ROM Table Peripheral #3 |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| CM4_ROMTABLE_CM4 | 0xE00FF010 | FULL | CM4 CoreSight ROM Table Peripheral #4 |
| CM4_ROMTABLE_CSMT | 0xE00FFFC0 | FULL | CM4 CoreSight ROM Table Memory Type |
| CM4_ROMTABLE_PID4 | 0xE00FFFD0 | FULL | CM4 CoreSight ROM Table Peripheral ID #4 |
| CM4_ROMTABLE_PID0 | 0xE00FFFE0 | FULL | CM4 CoreSight ROM Table Peripheral ID #0 |
| CM4_ROMTABLE_PID1 | 0xE00FFFE4 | FULL | CM4 CoreSight ROM Table Peripheral ID #1 |
| CM4_ROMTABLE_PID2 | 0xE00FFFE8 | FULL | CM4 CoreSight ROM Table Peripheral ID #2 |
| CM4_ROMTABLE_PID3 | 0xE00FFFE0 | FULL | CM4 CoreSight ROM Table Peripheral ID #3 |
| CM4_ROMTABLE_CID0 | 0xE00FFF00 | FULL | CM4 CoreSight ROM Table Component ID #0 |
| CM4_ROMTABLE_CID1 | 0xE00FFF04 | FULL | CM4 CoreSight ROM Table Component ID #1 |
| CM4_ROMTABLE_CID2 | 0xE00FFF08 | FULL | CM4 CoreSight ROM Table Component ID #2 |
| CM4_ROMTABLE_CID3 | 0xE00FFF0C | FULL | CM4 CoreSight ROM Table Component ID #3 |

4.13 Register Details

4.13.1 ITM

4.13.1.1 CM4_ITM_STIM

Description: Stimulus Port registers

Address: 0xE0000000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: The ITM_STIMx register characteristics are:

Purpose: Provide the interface for generating instrumentation messages.

Usage constraints:

- Accessible by word-aligned byte, halfword, and word accesses.

- The number of ITM_STIM registers is an IMPLEMENTATION DEFINED multiple of eight, see Trace Privilege Register, ITM_TPR on page C1-775.

- When DEMCR.TRCENA is 0, the ITM_STIM registers are UNKNOWN on reads and ignore writes.

Configurations: Always implemented.

Attributes: See Arm TRM Table C1-11 on page C1-773, and the register field descriptions.

The address of ITM_STIMn is (0xE0000000 + 4n).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | STIMULUS [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | STIMULUS [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | STIMULUS [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | STIMULUS [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:31 | STIMULUS | RW | R | X | Data write to the stimulus port FIFO, for forwarding as a software event packet. When read, bit[0] indicates whether the stimulus port FIFO can accept data: 0: Stimulus port FIFO full. 1: Stimulus port FIFO can accept at least one word. This bit is UNKNOWN after a Power-on reset. |

4.13.1.2 CM4_ITM_TER

Description: Trace Enable Register

Address: 0xE0000E00

Offset: 0xE00

Retention: Retained

IsDeepSleep: No

Comment: The ITM_TERx characteristics are:

Purpose: Provide an individual enable bit for each ITM_STIM register.

Usage constraints

- Each ITM_TER provides enable bits for 32 ITM_STIM registers.

- Bits corresponding to unimplemented ITM_STIM registers are RAZ/WI. See Trace Privilege Register, ITM_TPR on page C1-775 for information about the number of implemented ITM_STIM registers.

- The processor ignores any unprivileged write to an ITM_TERx bit if the corresponding ITM_TPR.PRIVMASK bit is set to 1, see Trace Privilege Register, ITM_TPR on Arm TRM page C1-775.

Configurations: Always implemented.

Attributes: See Table C1-11 on page C1-773.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | STIMENA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | STIMENA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | STIMENA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | STIMENA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:31 | STIMENA | RW | R | 0 | For bit STIMENA[n]: 0: Stimulus port (n) disabled 1: Stimulus port (n) enabled |

4.13.1.3 CM4_ITM_TPR

Description: ITM Trace Privilege Register
Address: 0xE0000E40
Offset: 0xE40
Retention: Retained
IsDeepSleep: No
Comment: Characteristics and bit assignments of the ITM_TPR register.
Purpose: Enables an operating system to control the stimulus ports that are accessible by user code.
Usage constraints: You can only write to this register in privileged mode.
Configurations: This register is available if the ITM is configured in your implementation.
Attributes: Refer to the ITM register summary table.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----------------|----|----|----|
| Name | None [7:4] | | | | PRIVMASK [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | PRIVMASK | RW | R | 0 | Bit mask to enable tracing on ITM stimulus ports: bit [0] = stimulus ports [7:0] bit [1] = stimulus ports [15:8] bit [2] = stimulus ports [23:16] bit [3] = stimulus ports [31:24] |

4.13.1.4 CM4_ITM_TCR

Description: Trace Control Register

Address: 0xE0000E80

Offset: 0xE80

Retention: Retained

IsDeepSleep: No

Comment: The ITM_TCR characteristics are:

Purpose: Configures and controls transfers through the ITM interface.

Usage constraints: For information about constraints that apply in a system that supports multiple trace streams

see CoreSight requirements for the TraceBusID field on page C1-778.

Configurations: Always implemented.

Attributes: See Table C1-11 on Arm TRM page C1-773, and the register field descriptions.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|----------------|------------------|----------------|-----------------|
| Name | None [7:5] | | | SWOENA [4:4] | TXENA [3:3] | SYNCENA [2:2] | TSENA [1:1] | ITMENA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-----------------|----|------------------|---|
| Name | None [15:12] | | | | GTSFREQ [11:10] | | TSPRESCALE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|--------------------|----|----|----|----|----|----|
| Name | BUSY [23:23] | TRACEBUSID [22:16] | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0 | ITMENA | RW | R | 0 | Enables the ITM: 0 Disabled. 1 Enabled. This is the master enable for the ITM unit. A debugger must set this bit to 1 to permit writes to all Stimulus Port registers. A Power-on reset clears this bit to 0. |
| 1 | TSENA | RW | R | 0 | Enables Local timestamp generation: 0 Disabled. 1 Enabled. A Power-on reset clears this bit to 0. |
| 2 | SYNCENA | RW | R | 0 | Enables Synchronization packet transmission for a synchronous TPIU: 0 Disabled. 1 Enabled. A Power-on reset clears this bit to 0. Note: If a debugger sets this bit to 1 it must also configure DWT_CTRL.SYNCTAP for the correct synchronization speed, see Control register, DWT_CTRL on Arm TRM page C1-797. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|--|
| 3 | TXENA | RW | R | 0 | Enables forwarding of hardware event packet from the DWT unit to the ITM for output to the TPIU: 0 Disabled. 1 Enabled. It is IMPLEMENTATION DEFINED whether the DWT discards packets that it cannot forward to the ITM. Note: If a debugger changes this bit from 0 to 1, the DWT might forward a hardware event packet that it has previously generated. A Power-on reset clears this bit to 0. |
| 4 | SWOENA | RW | R | 0 | Enables asynchronous clocking of the timestamp counter: 0 Timestamp counter uses the processor system clock. 1 Timestamp counter uses asynchronous clock from the TPIU interface. The timestamp counter is held in reset while the output line is idle. Which clocking modes are implemented is IMPLEMENTATION DEFINED. If the implementation does not support both modes this bit is either RAZ or RAO, to indicate the implemented mode. When this is a RW bit, on a Power-on reset, the value of this bit is UNKNOWN |
| 8:9 | TSPRESCALE | RW | R | 0 | Local timestamp prescaler, used with the trace packet reference clock. The possible values are: 00 No prescaling. 01 Divide by 4. 10 Divide by 16. 11 Divide by 64. If implemented, a Power-on reset clears this field to zero. If the processor does not implement the timestamp prescaler then these bits are reserved, RAZ/WI. |
| 10:11 | GTSFREQ | RW | R | 0 | Global timestamp frequency. Defines how often the ITM generates a global timestamp, based on the global timestamp clock frequency, or disables generation of global timestamps. The possible values are: 00 Disable generation of global timestamps. 01 Generate timestamp request whenever the ITM detects a change in global timestamp counter bits[47:7]. This is approximately every 128 cycles. 10 Generate timestamp request whenever the ITM detects a change in global timestamp counter bits[47:13]. This is approximately every 8192 cycles. 11 Generate a timestamp after every packet, if the output FIFO is empty. For more information see Global timestamping on Arm TRM page C1-771. A Power-on reset clears this field to zero. If the implementation does not support global timestamping then these bits are reserved, RAZ/WI. |
| 16:22 | TRACEBUSID | RW | R | 0 | Identifier for multi-source trace stream formatting. If multi-source trace is in use, the debugger must write a non-zero value to this field. For more information see CoreSight requirements for the TraceBusID field on TRM page C1-778. On a Power-on reset, the value of this field is UNKNOWN. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 23 | BUSY | RW | R | 0 | Indicates whether the ITM is currently processing events: 0 ITM is not processing any events. 1 ITM events present and being drained. These bits are read-only. |

4.13.1.5 CM4_ITM_LAR

Description: Lock Access Register
Address: 0xE0000FB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment: This is used to enable write access to device registers. If LSR[0] == 0x0 then this register is not present.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-------------------|----|----|----|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

4.13.1.6 CM4_ITM_LSR

Description: Lock Status Register

Address: 0xE0000FB4

Offset: 0xFB4

Retention: Retained

IsDeepSleep: No

Comment: This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.

This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------------------|----------------------------------|-----------------|
| Name | None [7:3] | | | | | IMPLEMENT S_8B [2:2] | ACCESS _PE MITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

4.13.1.7 CM4_ITM_PID4

Description: Peripheral Identification Register 4.
Address: 0xE0000FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

4.13.1.8 CM4_ITM_PID5

Description: Peripheral Identification Register 5.
Address: 0xE0000FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.1.9 CM4_ITM_PID6

Description: Peripheral Identification Register 6.
Address: 0xE0000FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.1.10 CM4_ITM_PID7

Description: Peripheral Identification Register 7.
Address: 0xE0000FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.1.11 CM4_ITM_PID0

Description: Peripheral Identification Register 0.
Address: 0xE0000FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 1 | N/A |

4.13.1.12 CM4_ITM_PID1

Description: Peripheral Identification Register 1.
Address: 0xE0000FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 176 | N/A |

4.13.1.13 CM4_ITM_PID2

Description: Peripheral Identification Register 2.
Address: 0xE0000FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 59 | N/A |

4.13.1.14 CM4_ITM_PID3

Description: Peripheral Identification Register 3.
Address: 0xE0000FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision |

4.13.1.15 CM4_ITM_CID0

Description: Component Identification Register 0.
Address: 0xE0000FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

4.13.1.16 CM4_ITM_CID1

Description: Component Identification Register 1.
Address: 0xE0000FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 224 | N/A |

4.13.1.17 CM4_ITM_CID2

Description: Component Identification Register 2.
Address: 0xE0000FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

4.13.1.18 CM4_ITM_CID3

Description: Component Identification Register 3.
Address: 0xE0000FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

4.13.2 DWT

4.13.2.1 CM4_DWT_CTRL

Description: Control register
Address: 0xE0001000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: The CTRL register characteristics are:
Purpose: Provides configuration and status information for the DWT unit, and used to control features of the unit.
Usage constraints: There are no usage constraints.
Configurations: Always implemented.
Attributes: See Table C1-21 and the register field descriptions.
Default: 0x40000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|------------------|---|---|---|-----------------|
| Name | | | | POSTPRESET [4:1] | | | | CYCCNTENA [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|---------------------|-----------------|----|--------------|----------------|
| Name | None [15:13] | | | PCSAMPLEN A [12:12] | SYNCTAP [11:10] | | CYCTAP [9:9] | POSTINIT [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------------|----------------------|-------------------|----------------------|-------------------|-------------------|-------------------|
| Name | None [23:23] | CYCEVTENA [22:22] | FOLDEVTE N A [21:21] | LSUEVTENA [20:20] | SLEEPEVTE NA [19:19] | EXCEVTENA [18:18] | CPIEVTENA [17:17] | EXCTRCENA [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|------------------|-------------------|------------------|------------------|
| Name | NUMCOMP [31:28] | | | | NOTRCPKT [27:27] | NOEXTTRIG [26:26] | NOCYCCNT [25:25] | NOPRFCNT [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | CYCCNTENA | RW | R | 0 | Enables CYCCNT: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOCYCCNT bit is RAO. |
| 1:4 | POSTPRESET | RW | R | 0 | Reload value for the POSTCNT counter. For more information see The POSTCNT timer on Arm TRM page C1-792. This field is UNK/SBZP if the NOCYCCNT bit is RAO. |
| 5:8 | POSTINIT | RW | R | 0 | Initial value for the POSTCNT counter. For more information see Enabling POSTCNT, and behavior of accesses to the DWT_CTRL.POSTINIT field and The POSTCNT timer on Arm TRM page C1-792. This field is UNK/SBZP if the NOCYCCNT bit is RAO. Note This field was previously called POSTCNT. The changed name gives a better indication of its function. |
| 9 | CYCTAP | RW | R | 0 | Selects the position of the POSTCNT tap on the CYCCNT counter: 0 POSTCNT tap at CYCCNT[6]. 1 POSTCNT tap at CYCCNT[10]. For more information see The POSTCNT timer on page C1-792. This bit is UNK/SBZP if the NOCYCCNT bit is RAO. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 10:11 | SYNCTAP | RW | R | 0 | Selects the position of the synchronization packet counter tap on the CYCCNT counter. This determines the Synchronization packet rate: 00 Disabled. No Synchronization packets. 01 Synchronization counter tap at CYCCNT[24]. 10 Synchronization counter tap at CYCCNT[26]. 11 Synchronization counter tap at CYCCNT[28]. For more information see The synchronization packet timer on Arm TRM page C1-794. This field is UNK/SBZP if the NOCYCCNT bit is RAO. |
| 12 | PCSAMPLENA | RW | R | 0 | Enables use of POSTCNT counter as a timer for Periodic PC sample packet generation: 0 No Periodic PC sample packets generated. 1 Periodic PC sample packets generated. See The POSTCNT timer on Arm TRM page C1-792 for more information. This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO. |
| 16 | EXCTRCENA | RW | R | 0 | Enables generation of exception trace: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOTRCPKT bit is RAO. |
| 17 | CPIEVTENA | RW | R | 0 | Enables generation of the CPI counter overflow event: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 18 | EXCEVTENA | RW | R | 0 | Enables generation of the Exception overhead counter overflow event: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 19 | SLEEPEVTENA | RW | R | 0 | Enables generation of the Sleep counter overflow event. 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 20 | LSUEVTENA | RW | R | 0 | Enables generation of the LSU counter overflow event. 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 21 | FOLDEVTENA | RW | R | 0 | Enables generation of the Folded-instruction counter overflow event: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. |
| 22 | CYCEVTENA | RW | R | 0 | Enables POSTCNT underflow Event counter packets generation: 0 No POSTCNT underflow packets generated. 1 POSTCNT underflow packets generated, if PCSAMPLENA set to 0. See The POSTCNT timer on Arm TRM page C1-792 for more information. This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO. |
| 24 | NOPRFCNT | RW | R | 0 | Shows whether the implementation supports the profiling counters: 0 Supported. 1 Not supported. For more information see Profiling counter support on Arm TRM page C1-794. This bit is read-only. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 25 | NOCYCCNT | RW | R | 0 | Shows whether the implementation supports a cycle counter: 0 Cycle counter supported. 1 Cycle counter not supported. For more information see CYCCNT cycle counter and related timers on Arm TRM page C1-792. This bit is read-only. |
| 26 | NOEXTTRIG | RW | R | 0 | Shows whether the implementation includes external match signals, CMPMATCH[N]: 0 CMPMATCH[N] supported. 1 CMPMATCH[N] not supported. This bit is read-only. |
| 27 | NOTRCPKT | RW | R | 0 | Shows whether the implementation supports trace sampling and exception tracing: 0 Trace sampling and exception tracing supported. 1 Trace sampling and exception tracing not supported. If this bit is RAZ, the NOCYCCNT bit must also RAZ. This bit is read-only. |
| 28:31 | NUMCOMP | RW | R | 4 | Number of comparators implemented. A value of zero indicates no comparator support. These bits are read-only. |

4.13.2.2 CM4_DWT_CYCCNT

Description: Cycle Count register
Address: 0xE0001004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: The CYCCNT register characteristics are:
Purpose: Shows or sets the value of the processor cycle counter, CYCCNT.
Usage constraints: The DWT unit suspends CYCCNT counting when the processor is in Debug state.
Configurations:
Implemented only when CTRL.NOCYCCNT is RAZ, see Control register, CTRL on page C1-797.
When CTRL.NOCYCCNT is RAO no cycle counter is implemented and this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | CYCNT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CYCNT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CYCNT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CYCNT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | CYCNT | RW | RW | 0 | Incrementing cycle counter value. When enabled, CYCCNT increments on each processor clock cycle. On overflow, CYCCNT wraps to zero. |

4.13.2.3 CM4_DWT_CPICNT

Description: CPI Count register

Address: 0xE0001008

Offset: 0x8

Retention: Retained

IsDeepSleep: No

Comment: The CPICNT register characteristics are:

Purpose: Counts additional cycles required to execute multi-cycle instructions and instruction fetch stalls.

Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.CPIEVTENA bit to 1.

Configurations:

Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on Arm TRM page C1-797.

If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.

Attributes: See Table C1-21 on page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | CPICNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:7 | CPICNT | RW | RW | 0 | Base instruction overhead counter. Counts one on each cycle when all of the following are true: <ul style="list-style-type: none"> - No instruction is executed. - No load-store operation is in progress, see LSU Count register, DWT_LSUCNT on page C1-803. - No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802. - Not in a power saving mode, see Sleep Count register, DWT_SLEPCNT on page C1-802. The definition of 'no instruction is executed' is IMPLEMENTATION DEFINED. ARM recommends that this counts each cycle on which no instruction is retired. An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.CPIEVTENA transitions from 0 to 1. |

4.13.2.4 CM4_DWT_EXCCNT

Description: Exception Overhead Count register

Address: 0xE000100C

Offset: 0xC

Retention: Retained

IsDeepSleep: No

Comment: The EXCCNT register characteristics are:
Purpose: Counts the total cycles spent in exception processing.
Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.EXCEVTENA bit to 1.
Configurations
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on Arm TRM page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | EXCCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:7 | EXCCNT | RW | RW | 0 | <p>The exception overhead counter. Counts one on each cycle when all of the following are true:</p> <ul style="list-style-type: none"> - No instruction is executed, see CPI Count register, DWT_CPICNT on Arm TRM page C1-801. - An exception-entry or exception-exit related operation is in progress. <p>Exception-entry or exception-exit related operations include the stacking of registers on exception entry, unstacking of registers on exception exit, and preemption.</p> <p>An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.EXCEVTENA transitions from 0 to 1.</p> |

4.13.2.5 CM4_DWT_SLEPCNT

Description: Sleep Count register

Address: 0xE0001010

Offset: 0x10

Retention: Retained

IsDeepSleep: No

Comment: The SLEPCNT register characteristics are:

Purpose: Counts the total number of cycles that the processor is sleeping.

Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.SLEEPEVTENA bit to 1.

Configurations:

Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on Arm TRM page C1-797.

If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.

Attributes: See Table C1-21 on page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | SLEPCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | SLEPCNT | RW | RW | 0 | <p>Sleep counter. Counts one on each cycle when all of the following are true:</p> <ul style="list-style-type: none"> - No instruction is executed, see CPI Count register, DWT_CPICNT on page C1-801. - No load-store operation is in progress, see LSU Count register, DWT_LSUCNT. - No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802. - In a power saving mode. <p>Power saving modes include WFI, WFE, and Sleep on exit, see Power management on page B1-616.</p> |

4.13.2.6 CM4_DWT_LSUCNT

Description: LSU Count register

Address: 0xE0001014

Offset: 0x14

Retention: Retained

IsDeepSleep: No

Comment: The LSUCNT register characteristics are:
Purpose: Increments on the additional cycles required to execute all load or store instructions
Usage constraints: The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.LSUEVTENA bit to 1.
Configurations:
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | LSUCNT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | LSUCNT | RW | RW | 0 | Load-store overhead counter. Counts one on each cycle when all of the following are true: - No instruction is executed, see CPI Count register, DWT_CPICNT on page C1-801. - No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802. - A load-store operation is in progress. |

4.13.2.7 CM4_DWT_FOLDCNT

Description: Folded-instruction Count register

Address: 0xE0001018

Offset: 0x18

Retention: Retained

IsDeepSleep: No

Comment: The FOLDCNT register characteristics are:
Purpose: Increments on each instruction that takes 0 cycles.
Usage constraints:
- The counter initializes to 0 when software enables its counter overflow event by setting the CTRL.FOLDEVTENA bit to 1.
- If an implementation includes profiling counters but does not support instruction folding, this counter can be RAZ/WI.
Configurations:
Implemented only when CTRL.NOPRFCNT is RAZ, see Control register, CTRL on Arm TRM page C1-797.
If CTRL.NOPRFCNT is RAO, indicating that the implementation does not include the profiling counters, this register is UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | FOLDCNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | FOLDCNT | RW | RW | 0 | Folded instruction counter. Counts one each cycle when at least two instructions are executed. The counter is incremented by the number of instructions executed, minus one. At least one instruction is executed is the opposite of No instruction is executed. See CPI Count register, DWT_CPICNT on Arm TRM page C1-801. An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.LSUEVTENA transitions from 0 to 1. |

4.13.2.8 CM4_DWT_PCSR

Description: Program Counter Sample Register

Address: 0xE000101C

Offset: 0x1C

Retention: Retained

IsDeepSleep: No

Comment: The PCSR characteristics are:

Purpose: Samples the current value of the program counter.

Usage constraints: There are no usage constraints.

Note: Bit[0] of any sampled value is RAZ and does not reflect instruction set state as it does in a PC sample on the ARMv7-A and ARMv7-R architecture profiles.

Configurations: An optional feature. Register is RAZ/WI if not implemented.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | EIASAMPLE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | EIASAMPLE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | EIASAMPLE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | EIASAMPLE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:31 | EIASAMPLE | RW | RW | 0 | Executed Instruction Address sample value. |

4.13.2.9 CM4_DWT_COMP0

Description: Comparator registers

Address: 0xE0001020

Offset: 0x20

Retention: Retained

IsDeepSleep: No

Comment: The COMPn register characteristics are:

Purpose: Provides a reference value for use by comparator n.

Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on page C1-806.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------------------|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

4.13.2.10 CM4_DWT_MASK0

Description: Comparator Mask registers

Address: 0xE0001024

Offset: 0x24

Retention: Retained

IsDeepSleep: No

Comment: The MASKn register characteristics are:

Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.

Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on page C1-797.

CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

4.13.2.11 CM4_DWT_FUNCTION0

Description: Comparator Function registers

Address: 0xE0001028

Offset: 0x28

Retention: Retained

IsDeepSleep: No

Comment: The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.

Usage constraints:

The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.

Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|------------|-----------------|------------|----------------|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|----|----|----|-------------------|----|---------------|------------------|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|--------------------|----|----|----|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|-----------------|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | FUNCTION | RW | R | 0 | <p>Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.</p> <p>For non-zero values:</p> <ul style="list-style-type: none"> - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. <p>This field resets to zero.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 24 | MATCHED | RW | R | 0 | <p>Comparator match:</p> <p>0 No match.</p> <p>1 Match.</p> <p>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register</p> <p>Reading the register clears this bit to 0. This bit is read-only.</p> |

4.13.2.12 CM4_DWT_COMP1

Description: Comparator registers

Address: 0xE0001030

Offset: 0x30

Retention: Retained

IsDeepSleep: No

Comment: The COMPn register characteristics are:
Purpose: Provides a reference value for use by comparator n.
Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------------------|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

4.13.2.13 CM4_DWT_MASK1

Description: Comparator Mask registers

Address: 0xE0001034

Offset: 0x34

Retention: Retained

IsDeepSleep: No

Comment: The MASKn register characteristics are:

Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.

Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

4.13.2.14 CM4_DWT_FUNCTION1

Description: Comparator Function registers

Address: 0xE0001038

Offset: 0x38

Retention: Retained

IsDeepSleep: No

Comment: The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.

Usage constraints:

The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.

Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|------------|-----------------|------------|----------------|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|----|----|----|-------------------|----|---------------|------------------|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|--------------------|----|----|----|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|-----------------|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | FUNCTION | RW | R | 0 | <p>Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.</p> <p>For non-zero values:</p> <ul style="list-style-type: none"> - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. <p>This field resets to zero.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 24 | MATCHED | RW | R | 0 | <p>Comparator match:</p> <p>0 No match.</p> <p>1 Match.</p> <p>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register</p> <p>Reading the register clears this bit to 0. This bit is read-only.</p> |

4.13.2.15 CM4_DWT_COMP2

Description: Comparator registers

Address: 0xE0001040

Offset: 0x40

Retention: Retained

IsDeepSleep: No

Comment: The COMPn register characteristics are:
Purpose: Provides a reference value for use by comparator n.
Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.
Configurations:
Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.
CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.
Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------------------|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

4.13.2.16 CM4_DWT_MASK2

Description: Comparator Mask registers

Address: 0xE0001044

Offset: 0x44

Retention: Retained

IsDeepSleep: No

Comment: The MASKn register characteristics are:

Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.

Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

4.13.2.17 CM4_DWT_FUNCTION2

Description: Comparator Function registers

Address: 0xE0001048

Offset: 0x48

Retention: Retained

IsDeepSleep: No

Comment: The FUNCTIONn register characteristics are:

Purpose: Controls the operation of comparator n.

Usage constraints:

The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.

Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|------------|-----------------|------------|----------------|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|----|----|----|-------------------|----|---------------|------------------|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|--------------------|----|----|----|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|-----------------|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:3 | FUNCTION | RW | R | 0 | <p>Selects action taken on comparator match:</p> <p>0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.</p> <p>For non-zero values:</p> <ul style="list-style-type: none"> - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. <p>This field resets to zero.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 24 | MATCHED | RW | R | 0 | <p>Comparator match:</p> <p>0 No match.</p> <p>1 Match.</p> <p>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register</p> <p>Reading the register clears this bit to 0. This bit is read-only.</p> |

4.13.2.18 CM4_DWT_COMP3

Description: Comparator registers

Address: 0xE0001050

Offset: 0x50

Retention: Retained

IsDeepSleep: No

Comment: The COMPn register characteristics are:

Purpose: Provides a reference value for use by comparator n.

Usage constraints: The operation of comparator n depends also on the registers MASKn and FUNCTIONn, see Comparator Mask registers, MASKn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented COMPn registers. Implemented

COMPn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | COMP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | COMP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | COMP [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------------------|
| 0:31 | COMP | RW | R | 0 | Reference value for comparison. |

4.13.2.19 CM4_DWT_MASK3

Description: Comparator Mask registers

Address: 0xE0001054

Offset: 0x54

Retention: Retained

IsDeepSleep: No

Comment: The MASKn register characteristics are:

Purpose: Provides the size of the ignore mask applied to the access address for address range matching by comparator n.

Usage constraints: The operation of comparator n depends also on the registers COMPn and FUNCTIONn, see Comparator registers, COMPn and Comparator Function registers, FUNCTIONn on Arm TRM page C1-806.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented MASKn registers. Implemented MASKn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------|---|---|---|---|
| Name | None [7:5] | | | MASK [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:4 | MASK | RW | R | 0 | The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. |

4.13.2.20 CM4_DWT_FUNCTION3

Description: Comparator Function registers

Address: 0xE0001058

Offset: 0x58

Retention: Retained

IsDeepSleep: No

Comment: The FUNCTIONn register characteristics are:
Purpose: Controls the operation of comparator n.

Usage constraints:

The operation of comparator n depends also on the registers COMPn and MASKn, see Comparator registers, COMPn on Arm TRM page C1-805 and Comparator Mask registers, MASKn on Arm TRM page C1-805.

Reading this register clears some fields to zero. See the register field descriptions for more information, and for the usage constraints of individual fields.

Configurations:

Implemented only when CTRL.NUMCOMP is nonzero, see Control register, CTRL on Arm TRM page C1-797.

CTRL.NUMCOMP defines the number of implemented FUNCTIONn registers. Implemented FUNCTIONn registers number from 0 to (NUMCOMP-1). Unimplemented registers are UNK/SBZP.

Attributes: See Table C1-21 on Arm TRM page C1-797. See the register field descriptions for information about the values of the RO bits in the register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|------------|-----------------|------------|----------------|---|---|---|
| Name | CYCMATCH [7:7] | None [6:6] | EMITRANGE [5:5] | None [4:4] | FUNCTION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|----|----|----|-------------------|----|---------------|------------------|
| Name | DATAVADDR0 [15:12] | | | | DATAVSIZE [11:10] | | LNK1ENA [9:9] | DATAVMATCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|--------------------|----|----|----|
| Name | None [23:20] | | | | DATAVADDR1 [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|-----------------|
| Name | None [31:25] | | | | | | | MATCHED [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | FUNCTION | RW | R | 0 | <p>Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789.</p> <p>For non-zero values:</p> <ul style="list-style-type: none"> - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. <p>This field resets to zero.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|---|
| 5 | EMITRANGE | RW | R | 0 | If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. |
| 7 | CYCMATCH | RW | R | 0 | DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. |
| 8 | DATAVMATCH | RW | R | 0 | Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. |
| 9 | LNK1ENA | RW | R | 0 | Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only |
| 10:11 | DATAVSIZE | RW | R | 0 | For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. |
| 12:15 | DATAVADDR0 | RW | R | 0 | When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. |
| 16:19 | DATAVADDR1 | RW | R | 0 | When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 24 | MATCHED | RW | R | 0 | <p>Comparator match:</p> <p>0 No match.</p> <p>1 Match.</p> <p>A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register</p> <p>Reading the register clears this bit to 0. This bit is read-only.</p> |

4.13.2.21 CM4_DWT_PID4

Description: Peripheral Identification Register 4.
Address: 0xE0001FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

4.13.2.22 CM4_DWT_PID5

Description: Peripheral Identification Register 5.
Address: 0xE0001FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.2.23 CM4_DWT_PID6

Description: Peripheral Identification Register 6.
Address: 0xE0001FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.2.24 CM4_DWT_PID7

Description: Peripheral Identification Register 7.
Address: 0xE0001FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.2.25 CM4_DWT_PID0

Description: Peripheral Identification Register 0.
Address: 0xE0001FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 2 | N/A |

4.13.2.26 CM4_DWT_PID1

Description: Peripheral Identification Register 1.
Address: 0xE0001FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 176 | N/A |

4.13.2.27 CM4_DWT_PID2

Description: Peripheral Identification Register 2.
Address: 0xE0001FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 59 | N/A |

4.13.2.28 CM4_DWT_PID3

Description: Peripheral Identification Register 3.
Address: 0xE0001FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision |

4.13.2.29 CM4_DWT_CID0

Description: Component Identification Register 0.
Address: 0xE0001FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

4.13.2.30 CM4_DWT_CID1

Description: Component Identification Register 1.
Address: 0xE0001FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 224 | N/A |

4.13.2.31 CM4_DWT_CID2

Description: Component Identification Register 2.
Address: 0xE0001FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

4.13.2.32 CM4_DWT_CID3

Description: Component Identification Register 3.
Address: 0xE0001FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

4.13.3 FPB

4.13.3.1 CM4_FPB_CTRL

Description: FlashPatch Control Register

Address: 0xE0002000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: The FP_CTRL Register characteristics are:

Purpose: Provides FPB implementation information, and the global enable for the FPB unit.

Usage constraints: There are no usage constraints.

Configurations: Always implemented.

Attributes: See Table C1-23.

Default: 0x260

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|------------|---|-----------|--------------|
| Name | NUM_CODE_LO [7:4] | | | | None [3:2] | | KEY [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|---------------------|----|----|----------------|----|---|---|
| Name | None [15:15] | NUM_CODE_HI [14:12] | | | NUM_LIT [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|--------------|----|----|----|
| Name | REV [31:28] | | | | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 0 | ENABLE | RW | R | 0 | Enable bit for the FPB: 0 Flash Patch Breakpoint disabled. 1 Flash Patch Breakpoint enabled. A Power-on reset clears this bit to 0. |
| 1 | KEY | RW | R | 0 | On any write to FP_CTRL, this bit must be 1. A write to the register with this bit set to zero is ignored. The Flash Patch Breakpoint unit ignores the write unless this bit is 1. This bit is RAZ. |
| 4:7 | NUM_CODE_LO | RW | R | 6 | The least significant bits, being bits[3:0], of NUM_CODE, the number of instruction address comparators. If NUM_CODE[6:0] is zero, the implementation does not support any instruction address comparators. These bits are read only. |
| 8:11 | NUM_LIT | RW | R | 2 | The number of literal address comparators supported, starting from NUM_CODE upwards. UNK/SBZP if Flash Patch is not implemented. Flash Patch is not implemented if FP_REMAP[29] is 0. If this field is zero, the implementation does not support literal comparators. These bits are read-only. |
| 12:14 | NUM_CODE_HI | RW | R | 0 | The most significant bits, being bits[6:4], of NUM_CODE, the number of instruction address comparators, see bits[7:4]. These bits are read only. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 28:31 | REV | RW | R | 0 | Flash Patch Breakpoint architecture revision: 0000 Flash Patch Breakpoint version 1. 0001 Flash Patch Breakpoint version 2. Supports breakpoints on any location in the 4GB address range. |

4.13.3.2 CM4_FPB_REMAP

Description: FlashPatch Remap register

Address: 0xE0002004

Offset: 0x4

Retention: Retained

IsDeepSleep: No

Comment: The FP_REMAP register characteristics are:

Purpose: Indicates whether the implementation supports flash patch remap, and if it does, holds the SRAM address for remap.

Usage constraints: There are no usage constraints.

Configurations: Always implemented.

Attributes: See Table C1-23 on Arm TRM page C1-816.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|------------|---|---|
| Name | | | | | | None [4:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | REMAP [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | REMAP [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|--------------|---------------|----|----|----|----|
| Name | RMPSP [31:30] | | None [29:29] | REMAP [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--|
| 5:28 | REMAP | RW | R | 0 | If the FPB supports flash patch remap, this field: - Holds bits[28:5] of the base address in SRAM to which the FPB remaps the address. - Has an UNKNOWN value on reset. If the FPB only supports breakpoint functionality this field is UNK/SBZP. |
| 30:31 | RMPSP | RW | R | 0 | Indicates whether the FPB unit supports flash patch remap: 0 Remapping not supported. The FPB only supports breakpoint functionality. 1 Hard-wired remap to SRAM region. These bits are read only. |

4.13.3.3 CM4_FPB_COMP

Description: FlashPatch Comparator register

Address: 0xE0002008

Offset: 0x8

Retention: Retained

IsDeepSleep: No

Comment: The FP_COMPn register characteristics are:

Purpose:

Holds an address for comparison with addresses in the Code memory region, see The system address map on page B3-648. The effect of a match depends on whether the comparator is an instruction address comparator or a literal address comparator:

Instruction address comparators

Either:

- Defines an instruction address to remap to an address based on the address specified in the FP_REMAP register.

- Defines a breakpoint address.

Literal address comparators

Defines a literal address to remap to an address based on the address specified in the FP_REMAP register.

The FP_CTRL register determines which comparators are instruction address comparators and which are literal address comparators. The version of the FPB unit determines the bit assignment for the FP_COMP register. The FP_CTRL.REV field determines which version of the FPB unit is attached. See FlashPatch Control Register, FP_CTRL on Arm TRM page C1-816.

The FP_REMAP.RMPSPT field determines if the FPB unit supports Flash Patch. For more information about address remapping see FlashPatch Remap register, FP_REMAP on page C1-818.

If the FPB unit is configured for remap then FP_COMPn defines a 29-bit word-aligned address.

If the FPB unit is configured for breakpoints, version 1 defines a 29-bit word-aligned address and the breakpoint can be set on either or both half-words at this address. For version 2 FPB units configured for breakpoints, FP_COMPn defines a 32-bit half-word aligned address.

Usage constraints: To enable a comparator, both the FP_CTRL.ENABLE bit and the required FP_COMPn.ENABLE bit must be set to 1.

Configuration: Always implemented. see FlashPatch Control Register, FP_CTRL on Arm TRM page C1-816 for information about the number of implemented FlashPatch comparator registers.

Attributes: See Table C1-23 on Arm TRM page C1-816.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VALUE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | VALUE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------------------------|
| 0:31 | VALUE | RW | R | 0 | See ARM documentation for details. |

4.13.3.4 CM4_FPB_PID4

Description: Peripheral Identification Register 4.
Address: 0xE0002FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

4.13.3.5 CM4_FPB_PID5

Description: Peripheral Identification Register 5.
Address: 0xE0002FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.3.6 CM4_FPB_PID6

Description: Peripheral Identification Register 6.
Address: 0xE0002FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.3.7 CM4_FPB_PID7

Description: Peripheral Identification Register 7.
Address: 0xE0002FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.3.8 CM4_FPB_PID0

Description: Peripheral Identification Register 0.
Address: 0xE0002FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 3 | N/A |

4.13.3.9 CM4_FPB_PID1

Description: Peripheral Identification Register 1.
Address: 0xE0002FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 176 | N/A |

4.13.3.10 CM4_FPB_PID2

Description: Peripheral Identification Register 2.
Address: 0xE0002FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 43 | N/A |

4.13.3.11 CM4_FPB_PID3

Description: Peripheral Identification Register 3.
Address: 0xE0002FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision |

4.13.3.12 CM4_FPB_CID0

Description: Component Identification Register 0.
Address: 0xE0002FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

4.13.3.13 CM4_FPB_CID1

Description: Component Identification Register 1.
Address: 0xE0002FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 224 | N/A |

4.13.3.14 CM4_FPB_CID2

Description: Component Identification Register 2.
Address: 0xE0002FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

4.13.3.15 CM4_FPB_CID3

Description: Component Identification Register 3.
Address: 0xE0002FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

4.13.4 SCS

4.13.4.1 CM4_SCS_ACTLR

Description: Auxiliary Control Register
Address: 0xE000E008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VALUE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | VALUE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer the following ARM documents for details about CPU register descriptions: ARMV7M : http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi04 CM4 TRM : http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.10010 |

4.13.4.2 CM4_SCS_SYST_CSR

Description: SysTick Control and Status Register
Address: 0xE000E010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.3 CM4_SCS_SYST_RVR

Description: SysTick Reload Value Register
Address: 0xE000E014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VALUE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | VALUE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.4 CM4_SCS_SYST_CVR

Description: SysTick Current Value Register
Address: 0xE000E018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.5 CM4_SCS_SYST_CALIB

Description: SysTick Calibration value Register
Address: 0xE000E01C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.6 CM4_SCS_NVIC_ISER

Description: Interrupt Set-Enable Registers
Address: 0xE000E100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.7 CM4_SCS_NVIC_ICER

Description: Interrupt Clear-Enable Registers
Address: 0xE000E180
Offset: 0x180
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.8 CM4_SCS_NVIC_ISPR

Description: Interrupt Set-Pending Registers
Address: 0xE000E200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.9 CM4_SCS_NVIC_ICPR

Description: Interrupt Clear-Pending Registers
Address: 0xE000E280
Offset: 0x280
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.10 CM4_SCS_NVIC_IABR

Description: Interrupt Active Bit Registers
Address: 0xE000E300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.11 CM4_SCS_NVIC_IPR

Description: Interrupt Priority Registers
Address: 0xE000E400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.12 CM4_SCS_CPUID

Description: CPUID Base Register
Address: 0xE000ED00
Offset: 0xD00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.13 CM4_SCS_ICSR

Description: Interrupt Control and State Register
Address: 0xE000ED04
Offset: 0xD04
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.14 CM4_SCS_VTOR

Description: Vector Table Offset Register
Address: 0xE000ED08
Offset: 0xD08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.15 CM4_SCS_AIRCR

Description: Application Interrupt and Reset Control Register
Address: 0xE000ED0C
Offset: 0xD0C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.16 CM4_SCS_SCR

Description: System Control Register
Address: 0xE000ED10
Offset: 0xD10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.17 CM4_SCS_CCR

Description: Configuration and Control Register
Address: 0xE000ED14
Offset: 0xD14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.18 CM4_SCS_SHPR1

Description: System Handler Priority Register 1
Address: 0xE000ED18
Offset: 0xD18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.19 CM4_SCS_SHPR2

Description: System Handler Priority Register 2
Address: 0xE000ED1C
Offset: 0xD1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.20 CM4_SCS_SHPR3

Description: System Handler Priority Register 3
Address: 0xE000ED20
Offset: 0xD20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.21 CM4_SCS_SHCSR

Description: System Handler Control and State Register
Address: 0xE000ED24
Offset: 0xD24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.22 CM4_SCS_CFSR

Description: Configurable Fault Status Register
Address: 0xE000ED28
Offset: 0xD28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.23 CM4_SCS_HFSR

Description: HardFault Status Register
Address: 0xE000ED2C
Offset: 0xD2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.24 CM4_SCS_DFSR

Description: Debug Fault Status Register
Address: 0xE000ED30
Offset: 0xD30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.25 CM4_SCS_MM FAR

Description: MemManage Fault Address Register
Address: 0xE000ED34
Offset: 0xD34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.26 CM4_SCS_BFAR

Description: BusFault Address Register
Address: 0xE000ED38
Offset: 0xD38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.27 CM4_SCS_AFSR

Description: Auxiliary Fault Status Register
Address: 0xE000ED3C
Offset: 0xD3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.28 CM4_SCS_CPACR

Description: Coprocessor Access Control Register
Address: 0xE000ED88
Offset: 0xD88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.29 CM4_SCS_MPU_TYPE

Description: MPU Type Register
Address: 0xE000ED90
Offset: 0xD90
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.30 CM4_SCS_MPU_CTRL

Description: MPU Control Register
Address: 0xE000ED94
Offset: 0xD94
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.31 CM4_SCS_MPU_RNR

Description: MPU Region Number Register
Address: 0xE000ED98
Offset: 0xD98
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.32 CM4_SCS_MPU_RBAR

Description: MPU Region Base Address Register
Address: 0xE000ED9C
Offset: 0xD9C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.33 CM4_SCS_MPU_RASR

Description: MPU Region Attribute and Size Register
Address: 0xE000EDA0
Offset: 0xDA0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.34 CM4_SCS_MPU_RBAR_A1

Description: MPU alias registers
Address: 0xE000EDA4
Offset: 0xDA4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.35 CM4_SCS_MPU_RASR_A1

Description: MPU alias registers
Address: 0xE000EDA8
Offset: 0xDA8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.36 CM4_SCS_MPU_RBAR_A2

Description: MPU alias registers
Address: 0xE000EDAC
Offset: 0xDAC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.37 CM4_SCS_MPU_RASR_A2

Description: MPU alias registers
Address: 0xE000EDB0
Offset: 0xDB0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.38 CM4_SCS_MPU_RBAR_A3

Description: MPU alias registers
Address: 0xE000EDB4
Offset: 0xDB4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.39 CM4_SCS_MPU_RASR_A3

Description: MPU alias registers
Address: 0xE000EDB8
Offset: 0xDB8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.40 CM4_SCS_DHCSR

Description: Debug Halting Control and Status Register
Address: 0xE000EDF0
Offset: 0xDF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.41 CM4_SCS_DCRSR

Description: Debug Core Register Selector Register
Address: 0xE000EDF4
Offset: 0xDF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.42 CM4_SCS_DCRDR

Description: Debug Core Register Data Register
Address: 0xE000EDF8
Offset: 0xDF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.43 CM4_SCS_DEMCR

Description: Debug Exception and Monitor Control Register
Address: 0xE000EDFC
Offset: 0xDFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.44 CM4_SCS_STIR

Description: Software Triggered Interrupt Register
Address: 0xE000EF00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.45 CM4_SCS_FPCCR

Description: FP Context Control Register
Address: 0xE000EF34
Offset: 0xF34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.46 CM4_SCS_FPCAR

Description: FP Context Control Register
Address: 0xE000EF38
Offset: 0xF38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.47 CM4_SCS_FPDSCR

Description: FP Context Control Register
Address: 0xE000EF3C
Offset: 0xF3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.48 CM4_SCS_PID4

Description: Peripheral Identification Register 4
Address: 0xE000EFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 4 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.49 CM4_SCS_PID5

Description: Peripheral Identification Register 5
Address: 0xE000EFD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.50 CM4_SCS_PID6

Description: Peripheral Identification Register 6
Address: 0xE000EFD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.51 CM4_SCS_PID7

Description: Peripheral Identification Register 7
Address: 0xE000EFDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.52 CM4_SCS_PID0

Description: Peripheral Identification Register 0
Address: 0xE000EFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 12 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.53 CM4_SCS_PID1

Description: Peripheral Identification Register 1
Address: 0xE000EFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 176 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.54 CM4_SCS_PID2

Description: Peripheral Identification Register 2
Address: 0xE000EFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 11 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.55 CM4_SCS_PID3

Description: Peripheral Identification Register 3
Address: 0xE000EFEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 4:7 | ECOREVNUM | R | R | 0 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.56 CM4_SCS_CID0

Description: Component Identification Register 0
Address: 0xE000EFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 13 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.57 CM4_SCS_CID1

Description: Component Identification Register 1
Address: 0xE000EFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xE0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 224 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.58 CM4_SCS_CID2

Description: Component Identification Register 2
Address: 0xE000EFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 5 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.4.59 CM4_SCS_CID3

Description: Component Identification Register 3
Address: 0xE000E0FC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 177 | Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. |

4.13.5 ETM

4.13.5.1 CM4_ETM_CR

Description: Main Control Register
Address: 0xE0041000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer the following ARM CM4 ETM TRM for register description: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi04 |

4.13.5.2 CM4_ETM_CCR

Description: Main Control Register
Address: 0xE0041004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.3 CM4_ETM_TRIGGER

Description: Trigger Event Register
Address: 0xE0041008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.4 CM4_ETM_SR

Description: ETM Status Register
Address: 0xE0041010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.5 CM4_ETM_SCR

Description: System Configuration Register
Address: 0xE0041014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.6 CM4_ETM_TEEVR

Description: TraceEnable Event Register
Address: 0xE0041020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.7 CM4_ETM_TECR1

Description: TraceEnable Control 1 Register
Address: 0xE0041024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.8 CM4_ETM_FFLR

Description: FIFOFULL Level Register
Address: 0xE0041028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.9 CM4_ETM_CNTRLDVR1

Description: Free-running counter reload value
Address: 0xE0041140
Offset: 0x140
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.10 CM4_ETM_SYNCFR

Description: Synchronization Frequency Register
Address: 0xE00411E0
Offset: 0x1E0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.11 CM4_ETM_IDR

Description: ID Register
Address: 0xE00411E4
Offset: 0x1E4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.12 CM4_ETM_CCER

Description: Configuration Code Extension Register
Address: 0xE00411E8
Offset: 0x1E8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.13 CM4_ETM_TESSEICR

Description: TraceEnable Start/Stop EmbeddedICE Control Register
Address: 0xE00411F0
Offset: 0x1F0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.14 CM4_ETM_TSEVR

Description: Timestamp Event Register
Address: 0xE00411F8
Offset: 0x1F8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.15 CM4_ETM_TRACEIDR

Description: CoreSight Trace ID Register
Address: 0xE0041200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.16 CM4_ETM_IDR2

Description: ETM ID Register 2
Address: 0xE0041208
Offset: 0x208
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.17 CM4_ETM_PDSR

Description: Device Power-Down Status Register
Address: 0xE0041314
Offset: 0x314
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.18 CM4_ETM_ITMISCIN

Description: Integration Test Miscellaneous Inputs
Address: 0xE0041EE0
Offset: 0xEE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.19 CM4_ETM_ITTRIGOUT

Description: Integration Test Trigger Out
Address: 0xE0041EE8
Offset: 0xEE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.20 CM4_ETM_ITATBCTR2

Description: ETM Integration Test ATB Control 2
Address: 0xE0041EF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.21 CM4_ETM_ITATBCTR0

Description: ETM Integration Test ATB Control 0
Address: 0xE0041EF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.22 CM4_ETM_ITCTRL

Description: Integration Mode Control Register
Address: 0xE0041F00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.23 CM4_ETM_CLAIMSET

Description: Claim Tag Set Register
Address: 0xE0041FA0
Offset: 0xFA0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.24 CM4_ETM_CLAIMCLR

Description: Claim Tag Clear Register
Address: 0xE0041FA4
Offset: 0xFA4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.25 CM4_ETM_LAR

Description: Lock Access Register
Address: 0xE0041FB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.26 CM4_ETM_LSR

Description: Lock Status Register
Address: 0xE0041FB4
Offset: 0xFB4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.27 CM4_ETM_AUTHSTATUS

Description: Authentication Status Register
Address: 0xE0041FB8
Offset: 0xFB8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.28 CM4_ETM_DEVTYPE

Description: CoreSight Device Type Register
Address: 0xE0041FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x13

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 19 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.29 CM4_ETM_PID4

Description: Peripheral Identification Register 4.
Address: 0xE0041FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 4 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.30 CM4_ETM_PID5

Description: Peripheral Identification Register 5.
Address: 0xE0041FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.31 CM4_ETM_PID6

Description: Peripheral Identification Register 6.
Address: 0xE0041FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.32 CM4_ETM_PID7

Description: Peripheral Identification Register 7.
Address: 0xE0041FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.33 CM4_ETM_PID0

Description: Peripheral Identification Register 0.
Address: 0xE0041FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x25

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 37 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.34 CM4_ETM_PID1

Description: Peripheral Identification Register 1.
Address: 0xE0041FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 185 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.35 CM4_ETM_PID2

Description: Peripheral Identification Register 2.
Address: 0xE0041FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 11 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.36 CM4_ETM_PID3

Description: Peripheral Identification Register 3.
Address: 0xE0041FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 4:7 | ECOREVNUM | R | R | 0 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.37 CM4_ETM_CID0

Description: Component Identification Register 0.
Address: 0xE0041FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 13 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.38 CM4_ETM_CID1

Description: Component Identification Register 1.
Address: 0xE0041FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 144 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.39 CM4_ETM_CID2

Description: Component Identification Register 2.
Address: 0xE0041FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 5 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.5.40 CM4_ETM_CID3

Description: Component Identification Register 3.
Address: 0xE0041FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 177 | Refer ARM documentation. See links in CM4_ETM.CR register. |

4.13.6 CM4CTI

4.13.6.1 CM4_CM4CTI_CTICONTROL

Description: CTI Control Register
Address: 0xE0042000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: The CTI Control Register enables the CTI.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | GLBEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | GLBEN | RW | R | 0 | Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. |

4.13.6.2 CM4_CM4CTI_CTIINTACK

Description: CTI Interrupt Acknowledge Register
Address: 0xE0042010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the CTITRIGOUT output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the CTITRIGOUT is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | INTACK [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | INTACK | W | R | 0 | Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. |

4.13.6.3 CM4_CM4CTI_CTIAPPSET

Description: CTI Application Trigger Set Register
Address: 0xE0042014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------|---|---|---|
| Name | None [7:4] | | | | APPSET [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:3 | APPSET | RW | R | 0 | Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. |

4.13.6.4 CM4_CM4CTI_CTIAPPCLEAR

Description: CTI Application Trigger Clear Register
Address: 0xE0042018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: The CTI Application Trigger Clear Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----------------|----|----|----|
| Name | None [7:4] | | | | APPCLEAR [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | APPCLEAR | W | R | 0 | Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. |

4.13.6.5 CM4_CM4CTI_CTIAPPPULSE

Description: CTI Application Pulse Register

Address: 0xE004201C

Offset: 0x1C

Retention: Retained

IsDeepSleep: No

Comment: The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | APPULSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:3 | APPULSE | W | R | 0 | Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. |

4.13.6.6 CM4_CM4CTI_CTIINEN

Description: CTI Trigger to Channel Enable Registers
Address: 0xE0042020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger to Channel Enable Registers enable the signaling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI. There is one register for each of the eight CTITRIGIN inputs. Within each register there is one bit for each of the four channels implemented. These registers do not affect the application trigger operations.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----------------|----|----|----|
| Name | None [7:4] | | | | TRIGINEN [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | TRIGINEN | RW | R | 0 | Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. |

4.13.6.7 CM4_CM4CTI_CTIOUTEN

Description: CTI Channel to Trigger Enable Registers

Address: 0xE00420A0

Offset: 0xA0

Retention: Retained

IsDeepSleep: No

Comment: The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output. There is one register for each of the eight CTITRIGOUT outputs. Within each register there is one bit for each of the four channels implemented. These registers affect the mapping from application trigger to trigger outputs.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-----------------|----|----|----|
| Name | None [7:4] | | | | TRIGOUTEN [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:3 | TRIGOUTEN | RW | R | 0 | Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. |

4.13.6.8 CM4_CM4CTI_CTITRIGINSTATUS

Description: CTI Trigger In Status Register
Address: 0xE0042130
Offset: 0x130
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger In Status Register provides the status of the CTITRIGIN inputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | TRIGINSTATUS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:7 | TRIGINSTATUS | R | RW | 0 | Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. |

4.13.6.9 CM4_CM4CTI_CTITRIGOUTSTATUS

Description: CTI Trigger Out Status Register
Address: 0xE0042134
Offset: 0x134
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger Out Status Register provides the status of the CTITRIGOUT outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | TRIGOUTSTATUS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:7 | TRIGOUTSTATUS | R | RW | 0 | Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. |

4.13.6.10 CM4_CM4CTI_CTICHINSTATUS

Description: CTI Channel In Status Register
Address: 0xE0042138
Offset: 0x138
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel In Status Register provides the status of the CTI CTICHIN inputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------------|---|---|---|
| Name | None [7:4] | | | | CTICHINSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:3 | CTICHINSTATUS | R | RW | 0 | Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. |

4.13.6.11 CM4_CM4CTI_CTICHOUTSTATUS

Description: CTI Channel Out Status Register
Address: 0xE004213C
Offset: 0x13C
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel Out Status Register provides the status of the CTI CTICHOUT outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------------|---|---|---|
| Name | None [7:4] | | | | CTICHOUTSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:3 | CTICHOUTSTATUS | R | RW | 0 | Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. |

4.13.6.12 CM4_CM4CTI_CTIGATE

Description: Enable CTI Channel Gate Register
Address: 0xE0042140
Offset: 0x140
Retention: Retained
IsDeepSleep: No
Comment: The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.
Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|------------------|------------------|------------------|------------------|
| Name | None [7:4] | | | | CTIGATEEN3 [3:3] | CTIGATEEN2 [2:2] | CTIGATEEN1 [1:1] | CTIGATEEN0 [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | CTIGATEEN0 | RW | R | 1 | Enable CTICHOUT0. Set to 0 to disable channel propagation. |
| 1 | CTIGATEEN1 | RW | R | 1 | Enable CTICHOUT1. Set to 0 to disable channel propagation. |
| 2 | CTIGATEEN2 | RW | R | 1 | Enable CTICHOUT2. Set to 0 to disable channel propagation. |
| 3 | CTIGATEEN3 | RW | R | 1 | Enable CTICHOUT3. Set to 0 to disable channel propagation. |

4.13.6.13 CM4_CM4CTI_ASICCTL

Description: External Multiplexor Control Register
Address: 0xE0042144
Offset: 0x144
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | ASICCTL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | ASICCTL | RW | R | 0 | Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. |

4.13.6.14 CM4_CM4CTI_ITCHINACK

Description: ITCHINACK Register
Address: 0xE0042EDC
Offset: 0xEDC
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------------|---|---|---|
| Name | None [7:4] | | | | CTCHINACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:3 | CTCHINACK | W | R | 0 | Set the value of the CTCHINACK outputs |

4.13.6.15 CM4_CM4CTI_ITTRIGINACK

Description: ITTRIGINACK Register
Address: 0xE0042EE0
Offset: 0xEE0
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | CTTRIGINACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:7 | CTTRIGINACK | W | R | 0 | Set the value of the CTTRIGINACK outputs |

4.13.6.16 CM4_CM4CTI_ITCHOUT

Description: ITCHOUT Register
Address: 0xE0042EE4
Offset: 0xEE4
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | CTCHOUT [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--------------------------------------|
| 0:3 | CTCHOUT | W | R | 0 | Set the value of the CTCHOUT outputs |

4.13.6.17 CM4_CM4CTI_ITTRIGOUT

Description: ITTRIGOUT Register
Address: 0xE0042EE8
Offset: 0xEE8
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | CTTRIGOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:7 | CTTRIGOUT | W | R | 0 | Set the value of the CTTRIGOUT outputs |

4.13.6.18 CM4_CM4CTI_ITCHOUTACK

Description: ITCHOUTACK Register
Address: 0xE0042EEC
Offset: 0xEEC
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|------------------|---|---|---|
| Name | None [7:4] | | | | CTCHOUTACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:3 | CTCHOUTACK | R | W | 0 | Read the values of the CTCHOUTACK inputs |

4.13.6.19 CM4_CM4CTI_ITTRIGOUTACK

Description: ITTRIGOUTACK Register
Address: 0xE0042EF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | CTTRIGOUTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:7 | CTTRIGOUTACK | R | W | 0 | Read the values of the CTTRIGOUTACK inputs |

4.13.6.20 CM4_CM4CTI_ITCHIN

Description: ITCHIN Register
Address: 0xE0042EF4
Offset: 0xEF4
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------|---|---|---|
| Name | None [7:4] | | | | CTCHIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--------------------------------------|
| 0:3 | CTCHIN | R | W | 0 | Read the values of the CTCHIN inputs |

4.13.6.21 CM4_CM4CTI_ITTRIGIN

Description: ITTRIGIN Register
Address: 0xE0042EF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | CTTRIGIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:7 | CTTRIGIN | R | W | 0 | Read the values of the CTTRIGIN inputs |

4.13.6.22 CM4_CM4CTI_ITCTRL

Description: Integration Mode Control Register

Address: 0xE0042F00

Offset: 0xF00

Retention: Retained

IsDeepSleep: No

Comment: This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------|
| Name | None [7:1] | | | | | | | MODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

4.13.6.23 CM4_CM4CTI_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE0042FA0

Offset: 0xFA0

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.

Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

4.13.6.24 CM4_CM4CTI_CLAIMCLR

Description: Claim Tag Clear Register
Address: 0xE0042FA4
Offset: 0xFA4
Retention: Retained
IsDeepSleep: No
Comment: This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

4.13.6.25 CM4_CM4CTI_LOCKACCESS

Description: Lock Access Register
Address: 0xE0042FB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment: This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-------------------|----|----|----|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

4.13.6.26 CM4_CM4CTI_LOCKSTATUS

Description: Lock Status Register

Address: 0xE0042FB4

Offset: 0xFB4

Retention: Retained

IsDeepSleep: No

Comment: This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.

This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|-------------------------|----------------------------------|-----------------|
| Name | None [7:3] | | | | | IMPLEMENT S_8B [2:2] | ACCESS _PE MITTED [1:1] | EXISTS [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

4.13.6.27 CM4_CM4CTI_AUTHSTATUS

Description: Authentication Status Register
Address: 0xE0042FB8
Offset: 0xFB8
Retention: Retained
IsDeepSleep: No
Comment: Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register
Default: 0x5

Bit-field Table

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|-------------|---|---------------|---|--------------|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:1 | NSIDBG | R | W | 1 | Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 1 | Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |

4.13.6.28 CM4_CM4CTI_DEVID

Description: Device Configuration Register

Address: 0xE0042FC8

Offset: 0xFC8

Retention: Retained

IsDeepSleep: No

Comment: This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.

Default: 0x40800

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----------------|----------------|----|----|----|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | NRTRIG [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 0:4 | NRMUXING | R | R | 0 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

4.13.6.29 CM4_CM4CTI_DEVTYPE

Description: Device Type Identifier Register
Address: 0xE0042FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment: 0x14 indicates this device has a major type of debug control logic component (0x4) and sub-type corresponding to cross trigger (0x1).
Default: 0x14

Bit-field Table

Bit-field Table

| | | | | | | | | |
|------|----------------|---|---|---|-------------|---|---|---|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| | | | | | | | | |
|------|-------------|----|----|----|----|----|---|---|
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |

| | | | | | | | | |
|------|--------------|----|----|----|----|----|----|----|
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |

| | | | | | | | | |
|------|--------------|----|----|----|----|----|----|----|
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|-------------------------------|
| 0:3 | CLASS | R | R | 4 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

4.13.6.30 CM4_CM4CTI_PID4

Description: Peripheral Identification Register 4
Address: 0xE0042FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

4.13.6.31 CM4_CM4CTI_PID5

Description: Peripheral Identification Register 5
Address: 0xE0042FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.6.32 CM4_CM4CTI_PID6

Description: Peripheral Identification Register 6
Address: 0xE0042FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.6.33 CM4_CM4CTI_PID7

Description: Peripheral Identification Register 7
Address: 0xE0042FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.6.34 CM4_CM4CTI_PID0

Description: Peripheral Identification Register 0
Address: 0xE0042FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x6

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 6 | N/A |

4.13.6.35 CM4_CM4CTI_PID1

Description: Peripheral Identification Register 1
Address: 0xE0042FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 185 | N/A |

4.13.6.36 CM4_CM4CTI_PID2

Description: Peripheral Identification Register 2
Address: 0xE0042FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 75 | N/A |

4.13.6.37 CM4_CM4CTI_PID3

Description: Peripheral Identification Register 3
Address: 0xE0042FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|----------------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

4.13.6.38 CM4_CM4CTI_CID0

Description: Component Identification Register 0
Address: 0xE0042FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

4.13.6.39 CM4_CM4CTI_CID1

Description: Component Identification Register 1
Address: 0xE0042FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 144 | N/A |

4.13.6.40 CM4_CM4CTI_CID2

Description: Component Identification Register 2
Address: 0xE0042FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

4.13.6.41 CM4_CM4CTI_CID3

Description: Component Identification Register 3
Address: 0xE0042FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

4.13.7 ROM

4.13.7.1 CM4_ROM_SCS

Description: CM4 CoreSight ROM Table Peripheral #0
Address: 0xE007F000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF8F003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429450445 1 | Offset to SCS ROM Table |

4.13.7.2 CM4_ROM_DWT

Description: CM4 CoreSight ROM Table Peripheral #1
Address: 0xE007F004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF82003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 4294451203 | Offset to DWT ROM Table |

4.13.7.3 CM4_ROM_FPB

Description: CM4 CoreSight ROM Table Peripheral #2
Address: 0xE007F008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF83003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429445529 9 | Offset to FPB ROM Table |

4.13.7.4 CM4_ROM_ITM

Description: CM4 CoreSight ROM Table Peripheral #3
Address: 0xE007F00C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF81003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 4294447107 | Offset to ITM ROM Table |

4.13.7.5 CM4_ROM_CTI

Description: CM4 CoreSight ROM Table Peripheral #4
Address: 0xE007F010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFC3003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429471744 3 | Offset to CTI ROM Table |

4.13.7.6 CM4_ROM_ETM

Description: CM4 CoreSight ROM Table Peripheral #5
Address: 0xE007F014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFC2003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429471334 7 | Offset to ETM ROM Table |

4.13.7.7 CM4_ROM_CSMT

Description: CM4 CoreSight ROM Table Memory Type
Address: 0xE007FFCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | | 1 | Memory Type |

4.13.7.8 CM4_ROM_PID4

Description: CM4 CoreSight ROM Table Peripheral ID #4
Address: 0xE007FFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

4.13.7.9 CM4_ROM_PID0

Description: CM4 CoreSight ROM Table Peripheral ID #0
Address: 0xE007FFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 192 | Peripheral ID #0 |

4.13.7.10 CM4_ROM_PID1

Description: CM4 CoreSight ROM Table Peripheral ID #1
Address: 0xE007FFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

4.13.7.11 CM4_ROM_PID2

Description: CM4 CoreSight ROM Table Peripheral ID #2
Address: 0xE007FFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

4.13.7.12 CM4_ROM_PID3

Description: CM4 CoreSight ROM Table Peripheral ID #3
Address: 0xE007FFEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

4.13.7.13 CM4_ROM_CID0

Description: CM4 CoreSight ROM Table Component ID #0
Address: 0xE007FFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

4.13.7.14 CM4_ROM_CID1

Description: CM4 CoreSight ROM Table Component ID #1
Address: 0xE007FFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

4.13.7.15 CM4_ROM_CID2

Description: CM4 CoreSight ROM Table Component ID #2
Address: 0xE007FFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

4.13.7.16 CM4_ROM_CID3

Description: CM4 CoreSight ROM Table Component ID #3
Address: 0xE007FFFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

4.13.8 TRCCTI

4.13.8.1 CM4_TRCCTI_CTICONTROL

Description: CTI Control Register
Address: 0xE0080000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: The CTI Control Register enables the CTI.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | GLBEN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | GLBEN | RW | R | 0 | Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. |

4.13.8.2 CM4_TRCCTI_CTIINTACK

Description: CTI Interrupt Acknowledge Register
Address: 0xE0080010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The CTI Interrupt Acknowledge Register is write-only. Any bits written as a 1 cause the CTITRIGOUT output signal to be acknowledged. The acknowledgement is cleared when MAPTRIGOUT is deactivated. This register is used when the CTITRIGOUT is used as a sticky output, that is, no hardware acknowledge is supplied, and a software acknowledge is required.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | INTACK [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | INTACK | W | R | 0 | Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. |

4.13.8.3 CM4_TRCCTI_CTIAPPSET

Description: CTI Application Trigger Set Register
Address: 0xE0080014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: The CTI Application Trigger Set Register is read/write. A write to this register causes a channel event to be raised, corresponding to the bit written to.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------|---|---|---|
| Name | None [7:4] | | | | APPSET [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:3 | APPSET | RW | R | 0 | Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. |

4.13.8.4 CM4_TRCCTI_CTIAPPCLEAR

Description: CTI Application Trigger Clear Register
Address: 0xE0080018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment: The CTI Application Trigger Clear Register is write-only. A write to this register causes a channel event to be cleared, corresponding to the bit written to.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----------------|----|----|----|
| Name | None [7:4] | | | | APPCLEAR [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | APPCLEAR | W | R | 0 | Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. |

4.13.8.5 CM4_TRCCTI_CTIAPPULSE

Description: CTI Application Pulse Register

Address: 0xE008001C

Offset: 0x1C

Retention: Retained

IsDeepSleep: No

Comment: The CTI Application Pulse Register is write-only. A write to this register causes a channel event pulse, one CTICLK period, to be generated, corresponding to the bit written to. The pulse external to the ECT can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | APPULSE [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:3 | APPULSE | W | R | 0 | Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. |

4.13.8.6 CM4_TRCCTI_CTIINEN

Description: CTI Trigger to Channel Enable Registers
Address: 0xE0080020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger to Channel Enable Registers enable the signaling of an event on CTM channels when the core issues a trigger, CTITRIGIN, to the CTI. There is one register for each of the eight CTITRIGIN inputs. Within each register there is one bit for each of the four channels implemented. These registers do not affect the application trigger operations.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----------------|----|----|----|
| Name | None [7:4] | | | | TRIGINEN [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | TRIGINEN | RW | R | 0 | Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. |

4.13.8.7 CM4_TRCCTI_CTIOUTEN

Description: CTI Channel to Trigger Enable Registers
Address: 0xE00800A0
Offset: 0xA0
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel to Trigger Enable Registers define which channels can generate a CTITRIGOUT output. There is one register for each of the eight CTITRIGOUT outputs. Within each register there is one bit for each of the four channels implemented. These registers affect the mapping from application trigger to trigger outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-----------------|----|----|----|
| Name | None [7:4] | | | | TRIGOUTEN [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:3 | TRIGOUTEN | RW | R | 0 | Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. |

4.13.8.8 CM4_TRCCTI_CTITRIGINSTATUS

Description: CTI Trigger In Status Register
Address: 0xE0080130
Offset: 0x130
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger In Status Register provides the status of the CTITRIGIN inputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | TRIGINSTATUS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:7 | TRIGINSTATUS | R | RW | 0 | Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. |

4.13.8.9 CM4_TRCCTI_CTITRIGOUTSTATUS

Description: CTI Trigger Out Status Register
Address: 0xE0080134
Offset: 0x134
Retention: Retained
IsDeepSleep: No
Comment: The CTI Trigger Out Status Register provides the status of the CTITRIGOUT outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | TRIGOUTSTATUS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:7 | TRIGOUTSTATUS | R | RW | 0 | Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. |

4.13.8.10 CM4_TRCCTI_CTICHINSTATUS

Description: CTI Channel In Status Register
Address: 0xE0080138
Offset: 0x138
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel In Status Register provides the status of the CTI CTICHIN inputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------------|---|---|---|
| Name | None [7:4] | | | | CTICHINSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:3 | CTICHINSTATUS | R | RW | 0 | Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. |

4.13.8.11 CM4_TRCCTI_CTICHOUTSTATUS

Description: CTI Channel Out Status Register
Address: 0xE008013C
Offset: 0x13C
Retention: Retained
IsDeepSleep: No
Comment: The CTI Channel Out Status Register provides the status of the CTI CTICHOUT outputs.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------------|---|---|---|
| Name | None [7:4] | | | | CTICHOUTSTATUS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:3 | CTICHOUTSTATUS | R | RW | 0 | Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. |

4.13.8.12 CM4_TRCCTI_CTIGATE

Description: Enable CTI Channel Gate Register
Address: 0xE0080140
Offset: 0x140
Retention: Retained
IsDeepSleep: No
Comment: The Gate Enable Register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.
Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|------------------|------------------|------------------|------------------|
| Name | None [7:4] | | | | CTIGATEEN3 [3:3] | CTIGATEEN2 [2:2] | CTIGATEEN1 [1:1] | CTIGATEEN0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | CTIGATEEN0 | RW | R | 1 | Enable CTICHOUT0. Set to 0 to disable channel propagation. |
| 1 | CTIGATEEN1 | RW | R | 1 | Enable CTICHOUT1. Set to 0 to disable channel propagation. |
| 2 | CTIGATEEN2 | RW | R | 1 | Enable CTICHOUT2. Set to 0 to disable channel propagation. |
| 3 | CTIGATEEN3 | RW | R | 1 | Enable CTICHOUT3. Set to 0 to disable channel propagation. |

4.13.8.13 CM4_TRCCTI_ASICCTL

Description: External Multiplexor Control Register
Address: 0xE0080144
Offset: 0x144
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | ASICCTL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | ASICCTL | RW | R | 0 | Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. |

4.13.8.14 CM4_TRCCTI_ITCHINACK

Description: ITCHINACK Register
Address: 0xE0080EDC
Offset: 0xEDC
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------------|---|---|---|
| Name | None [7:4] | | | | CTCHINACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:3 | CTCHINACK | W | R | 0 | Set the value of the CTCHINACK outputs |

4.13.8.15 CM4_TRCCTI_ITTRIGINACK

Description: ITTRIGINACK Register
Address: 0xE0080EE0
Offset: 0xEE0
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | CTTRIGINACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:7 | CTTRIGINACK | W | R | 0 | Set the value of the CTTRIGINACK outputs |

4.13.8.16 CM4_TRCCTI_ITCHOUT

Description: ITCHOUT Register
Address: 0xE0080EE4
Offset: 0xEE4
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | CTCHOUT [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--------------------------------------|
| 0:3 | CTCHOUT | W | R | 0 | Set the value of the CTCHOUT outputs |

4.13.8.17 CM4_TRCCTI_ITTRIGOUT

Description: ITTRIGOUT Register
Address: 0xE0080EE8
Offset: 0xEE8
Retention: Retained
IsDeepSleep: No
Comment: This register is a write-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | CTTRIGOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:7 | CTTRIGOUT | W | R | 0 | Set the value of the CTTRIGOUT outputs |

4.13.8.18 CM4_TRCCTI_ITCHOUTACK

Description: ITCHOUTACK Register
Address: 0xE0080EEC
Offset: 0xEEC
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|------------------|---|---|---|
| Name | None [7:4] | | | | CTCHOUTACK [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:3 | CTCHOUTACK | R | W | 0 | Read the values of the CTCHOUTACK inputs |

4.13.8.19 CM4_TRCCTI_ITTRIGOUTACK

Description: ITTRIGOUTACK Register
Address: 0xE0080EF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | CTTRIGOUTACK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:7 | CTTRIGOUTACK | R | W | 0 | Read the values of the CTTRIGOUTACK inputs |

4.13.8.20 CM4_TRCCTI_ITCHIN

Description: ITCHIN Register
Address: 0xE0080EF4
Offset: 0xEF4
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------|---|---|---|
| Name | None [7:4] | | | | CTCHIN [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--------------------------------------|
| 0:3 | CTCHIN | R | W | 0 | Read the values of the CTCHIN inputs |

4.13.8.21 CM4_TRCCTI_ITTRIGIN

Description: ITTRIGIN Register
Address: 0xE0080EF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment: This register is a read-only register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | CTTRIGIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:7 | CTTRIGIN | R | W | 0 | Read the values of the CTTRIGIN inputs |

4.13.8.22 CM4_TRCCTI_ITCTRL

Description: Integration Mode Control Register
Address: 0xE0080F00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment: This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|------------|
| Name | None [7:1] | | | | | | | MODE [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

4.13.8.23 CM4_TRCCTI_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE0080FA0

Offset: 0xFA0

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.

Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

4.13.8.24 CM4_TRCCTI_CLAIMCLR

Description: Claim Tag Clear Register
Address: 0xE0080FA4
Offset: 0xFA4
Retention: Retained
IsDeepSleep: No
Comment: This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-----------|----|----|----|
| Name | None [7:4] | | | | TAG [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

4.13.8.25 CM4_TRCCTI_LOCKACCESS

Description: Lock Access Register
Address: 0xE0080FB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment: This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-------------------|----|----|----|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

4.13.8.26 CM4_TRCCTI_LOCKSTATUS

Description: Lock Status Register

Address: 0xE0080FB4

Offset: 0xFB4

Retention: Retained

IsDeepSleep: No

Comment: This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.

This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------------------|----------------------------------|-----------------|
| Name | None [7:3] | | | | | IMPLEMENT S_8B [2:2] | ACCESS _PE MITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | EXISTS | R | W | 0 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 0 | The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

4.13.8.28 CM4_TRCCTI_DEVID

Description: Device Configuration Register

Address: 0xE0080FC8

Offset: 0xFC8

Retention: Retained

IsDeepSleep: No

Comment: This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.

Default: 0x40800

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----------------|----------------|----|----|----|
| Name | None [7:5] | | | NRMUXING [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | NRTRIG [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | NRCHAN [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 0:4 | NRMUXING | R | R | 0 | Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. |
| 8:15 | NRTRIG | R | R | 8 | Number of ECT triggers available. |
| 16:19 | NRCHAN | R | R | 4 | Number of ECT channels available. |

4.13.8.29 CM4_TRCCTI_DEVTYPE

Description: Device Type Identifier Register
Address: 0xE0080FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment: 0x14 indicates this device has a major type of debug control logic component (0x4) and sub-type corresponding to cross trigger (0x1).
Default: 0x14

Bit-field Table

Bit-field Table

| | | | | | | | | |
|------|----------------|---|---|---|-------------|---|---|---|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| | | | | | | | | |
|------|-------------|----|----|----|----|----|---|---|
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |

| | | | | | | | | |
|------|--------------|----|----|----|----|----|----|----|
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |

| | | | | | | | | |
|------|--------------|----|----|----|----|----|----|----|
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|-------------------------------|
| 0:3 | CLASS | R | R | 4 | debug control logic component |
| 4:7 | SUB_TYPE | R | R | 1 | cross trigger |

4.13.8.30 CM4_TRCCTI_PID4

Description: Peripheral Identification Register 4
Address: 0xE0080FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 4 | N/A |

4.13.8.31 CM4_TRCCTI_PID5

Description: Peripheral Identification Register 5
Address: 0xE0080FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.8.32 CM4_TRCCTI_PID6

Description: Peripheral Identification Register 6
Address: 0xE0080FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.8.33 CM4_TRCCTI_PID7

Description: Peripheral Identification Register 7
Address: 0xE0080FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | N/A |

4.13.8.34 CM4_TRCCTI_PID0

Description: Peripheral Identification Register 0
Address: 0xE0080FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x6

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 6 | N/A |

4.13.8.35 CM4_TRCCTI_PID1

Description: Peripheral Identification Register 1
Address: 0xE0080FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 185 | N/A |

4.13.8.36 CM4_TRCCTI_PID2

Description: Peripheral Identification Register 2
Address: 0xE0080FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 75 | N/A |

4.13.8.37 CM4_TRCCTI_PID3

Description: Peripheral Identification Register 3
Address: 0xE0080FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|----------------------|
| 4:7 | ECOREVNUM | R | R | 0 | ECO revision for MTB |

4.13.8.38 CM4_TRCCTL_CID0

Description: Component Identification Register 0
Address: 0xE0080FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 13 | N/A |

4.13.8.39 CM4_TRCCTL_CID1

Description: Component Identification Register 1
Address: 0xE0080FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 144 | N/A |

4.13.8.40 CM4_TRCCTL_CID2

Description: Component Identification Register 2
Address: 0xE0080FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 5 | N/A |

4.13.8.41 CM4_TRCCTL_CID3

Description: Component Identification Register 3
Address: 0xE0080FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 177 | N/A |

4.13.9 CSTF

4.13.9.1 CM4_CSTF_CSTFCTL

Description: Funnel Control Register
Address: 0xE008C000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.10053 |

4.13.9.2 CM4_CSTF_CSTFCTL

Description: Priority Control Register
Address: 0xE008C004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.3 CM4_CSTF_ITATBDATA0

Description: Integration Register
Address: 0xE008CEEC
Offset: 0xEEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.4 CM4_CSTF_ITATBCTR2

Description: Integration Register
Address: 0xE008CEF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.5 CM4_CSTF_ITATBCTR1

Description: Integration Register
Address: 0xE008CEF4
Offset: 0xEF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.6 CM4_CSTF_ITATBCTR0

Description: Integration Register
Address: 0xE008CEF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.7 CM4_CSTF_ITCTRL

Description: Integration Mode Control Register
Address: 0xE008CF00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.8 CM4_CSTF_CLAIMSET

Description: Claim Tag Set Register
Address: 0xE008CFA0
Offset: 0xFA0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.9 CM4_CSTF_CLAIMCLR

Description: Claim Tag Clear Register
Address: 0xE008CFA4
Offset: 0xFA4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.10 CM4_CSTF_LOCKACCESS

Description: Lock Access Register
Address: 0xE008CFB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.11 CM4_CSTF_LOCKSTATUS

Description: Lock Status Register
Address: 0xE008CFB4
Offset: 0xFB4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 3 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.12 CM4_CSTF_AUTHSTATUS

Description: Authentication Status Register
Address: 0xE008CFB8
Offset: 0xFB8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.13 CM4_CSTF_DEVID

Description: Device ID
Address: 0xE008CFC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x38

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 56 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.14 CM4_CSTF_DEVTYPE

Description: Device Type Identifier Register
Address: 0xE008CFCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x12

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 18 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.15 CM4_CSTF_PID4

Description: Peripheral Identification Register 4
Address: 0xE008CFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 4 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.16 CM4_CSTF_PID5

Description: Peripheral Identification Register 5
Address: 0xE008CFD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.17 CM4_CSTF_PID6

Description: Peripheral Identification Register 6
Address: 0xE008CFD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.18 CM4_CSTF_PID7

Description: Peripheral Identification Register 7
Address: 0xE008CFDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.19 CM4_CSTF_PID0

Description: Peripheral Identification Register 0
Address: 0xE008CFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x8

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 8 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.20 CM4_CSTF_PID1

Description: Peripheral Identification Register 1
Address: 0xE008CFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 185 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.21 CM4_CSTF_PID2

Description: Peripheral Identification Register 2
Address: 0xE008CFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 43 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.22 CM4_CSTF_PID3

Description: Peripheral Identification Register 3
Address: 0xE008CFEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 4:7 | ECOREVNUM | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.23 CM4_CSTF_CID0

Description: Component Identification Register 0
Address: 0xE008CFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 13 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.24 CM4_CSTF_CID1

Description: Component Identification Register 1
Address: 0xE008CFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 144 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.25 CM4_CSTF_CID2

Description: Component Identification Register 2
Address: 0xE008CFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 5 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.9.26 CM4_CSTF_CID3

Description: Component Identification Register 3
Address: 0xE008CFFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 177 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10 ETB

4.13.10.1 CM4_ETB_ETBRDP

Description: RAM Depth Register
Address: 0xE008D004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.2 CM4_ETB_ETBSTS

Description: Status Register
Address: 0xE008D00C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x8

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 8 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.3 CM4_ETB_ETBRD

Description: RAM Read Data Register
Address: 0xE008D010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.4 CM4_ETB_ETBRRP

Description: RAM Read Pointer Register
Address: 0xE008D014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.5 CM4_ETB_ETBRWP

Description: RAM Write Pointer Register
Address: 0xE008D018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.6 CM4_ETB_ETBTRG

Description: Trigger Counter Register
Address: 0xE008D01C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.7 CM4_ETB_ETBCTL

Description: Control Register
Address: 0xE008D020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.8 CM4_ETB_ETBRWD

Description: RAM Write Data Register
Address: 0xE008D024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.9 CM4_ETB_ETBFFSR

Description: Formatter and Flush Status Register
Address: 0xE008D300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 2 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.10 CM4_ETB_ETBFFCR

Description: Formatter and Flush Control Register
Address: 0xE008D304
Offset: 0x304
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.11 CM4_ETB_ITMISCOP0

Description: Integration Register
Address: 0xE008DEE0
Offset: 0xEE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.12 CM4_ETB_ITTRFLINACK

Description: Integration Register
Address: 0xE008DEE4
Offset: 0xEE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.13 CM4_ETB_ITTRFLIN

Description: Integration Register
Address: 0xE008DEE8
Offset: 0xEE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.14 CM4_ETB_ITATBDATA0

Description: Integration Register
Address: 0xE008DEEC
Offset: 0xEEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.15 CM4_ETB_ITATBCTR2

Description: Integration Register
Address: 0xE008DEF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.16 CM4_ETB_ITATBCTR1

Description: Integration Register
Address: 0xE008DEF4
Offset: 0xEF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.17 CM4_ETB_ITATBCTR0

Description: Integration Register
Address: 0xE008DEF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.18 CM4_ETB_ITCTRL

Description: Integration Mode Control Register
Address: 0xE008DF00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | RW | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.19 CM4_ETB_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE008DFA0

Offset: 0xFA0

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.

Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

4.13.10.20 CM4_ETB_CLAIMCLR

Description: Claim Tag Clear Register

Address: 0xE008DFA4

Offset: 0xFA4

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

4.13.10.21 CM4_ETB_LOCKACCESS

Description: Lock Access Register
Address: 0xE008DFB0
Offset: 0xFB0
Retention: Retained
IsDeepSleep: No
Comment: This is used to enable write access to device registers. If LOCKSTATUS[0] == 0x0 then this register is not present.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|-------------------|----|----|----|
| Name | None [7:4] | | | | ACCESS_CODE [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:3 | ACCESS_CODE | RW | R | 0 | Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. |

4.13.10.22 CM4_ETB_LOCKSTATUS

Description: Lock Status Register

Address: 0xE008DFB4

Offset: 0xFB4

Retention: Retained

IsDeepSleep: No

Comment: This indicates the status of the Lock control mechanism. This lock prevents accidental writes by code under debug.

This register must always be present although there might not be any lock-access control mechanism. The lock mechanism, where present and locked, must block write accesses to any control register, except the Lock Access Register. For most components this covers all registers except for the Lock Access Register 0xFB0.

Default: 0x3

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------------------|----------------------------------|-----------------|
| Name | None [7:3] | | | | | IMPLEMENT S_8B [2:2] | ACCESS _PE MITTED [1:1] | EXISTS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | EXISTS | R | W | 1 | Indicates that a lock control mechanism exists for this device |
| 1 | ACCESS_PERMITTED | R | W | 1 | The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted |
| 2 | IMPLEMENTS_8B | R | W | 0 | This component implements an 8-bit Lock Access Register. |

4.13.10.23 CM4_ETB_AUTHSTATUS

Description: Authentication Status Register

Address: 0xE008DFB8

Offset: 0xFB8

Retention: Retained

IsDeepSleep: No

Comment: Reports the required security level and current status of those enables. Where functionality changes on a given security level then this change in status must be reported in this register

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|-------------|---|---------------|---|--------------|---|
| Name | SNIDBG [7:6] | | SIDBG [5:4] | | NSNIDBG [3:2] | | NSIDBG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:1 | NSIDBG | R | W | 0 | Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |
| 2:3 | NSNIDBG | R | W | 0 | Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |
| 4:5 | SIDBG | R | W | 0 | Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |
| 6:7 | SNIDBG | R | W | 0 | Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled |

4.13.10.24 CM4_ETB_DEVID

Description: Device ID
Address: 0xE008DFC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment: This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|--------------|-----------------|---|---|---|---|
| Name | None [7:6] | | RAMCLK [5:5] | EXTMUXNUM [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:4 | EXTMUXNUM | R | R | 0 | Number of external multiplexing available. Non-zero values indicate the type of ATB multiplexing on the input to the ATB. Only 0x00 is supported, that is, no multiplexing is present. This value helps detect the ATB structure. |
| 5 | RAMCLK | R | R | 0 | This bit returns 0 on reads to indicate that the ETB RAM operates synchronously to atclk. |

4.13.10.25 CM4_ETB_DEVTYPE

Description: Device Type Identifier Register
Address: 0xE008DFCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x21

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|-------------|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|----------------------|
| 0:3 | CLASS | R | R | 1 | Trace sink component |
| 4:7 | SUB_TYPE | R | R | 2 | Trace buffer. |

4.13.10.26 CM4_ETB_PID4

Description: Peripheral Identification Register 4
Address: 0xE008DFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 4 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.27 CM4_ETB_PID5

Description: Peripheral Identification Register 5
Address: 0xE008DFD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.28 CM4_ETB_PID6

Description: Peripheral Identification Register 6
Address: 0xE008DFD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.29 CM4_ETB_PID7

Description: Peripheral Identification Register 7
Address: 0xE008DFDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.30 CM4_ETB_PID0

Description: Peripheral Identification Register 0
Address: 0xE008DFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x7

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 7 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.31 CM4_ETB_PID1

Description: Peripheral Identification Register 1
Address: 0xE008DFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 185 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.32 CM4_ETB_PID2

Description: Peripheral Identification Register 2
Address: 0xE008DFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 59 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.33 CM4_ETB_PID3

Description: Peripheral Identification Register 3
Address: 0xE008DFEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 4:7 | ECOREVNUM | R | R | 0 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.34 CM4_ETB_CID0

Description: Component Identification Register 0
Address: 0xE008DFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 13 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.35 CM4_ETB_CID1

Description: Component Identification Register 1
Address: 0xE008DFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 144 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.36 CM4_ETB_CID2

Description: Component Identification Register 2
Address: 0xE008DFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 5 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.10.37 CM4_ETB_CID3

Description: Component Identification Register 3
Address: 0xE008DFFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 177 | Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. |

4.13.11 TPIU

4.13.11.1 CM4_TPIU_TPIU_SSPSR

Description: Supported Parallel Port Size Register
Address: 0xE008E000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | CM4 TPIU is used as TPIU. Refer CM4 TRM register descriptions: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.10016 |

4.13.11.2 CM4_TPIU_TPIU_CSPSR

Description: Current Parallel Port Size Register
Address: 0xE008E004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 1 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.3 CM4_TPIU_TPIU_ACPR

Description: Asynchronous Clock Prescaler Register
Address: 0xE008E010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.4 CM4_TPIU_TPIU_SPPR

Description: Selected Pin Protocol Register
Address: 0xE008E0F0
Offset: 0xF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 1 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.5 CM4_TPIU_TPIU_FFSR

Description: Formatter and Flush Status Register
Address: 0xE008E300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x8

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 8 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.6 CM4_TPIU_TPIU_FFCR

Description: Formatter and Flush Control Register
Address: 0xE008E304
Offset: 0x304
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x102

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | RW | R | 258 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.7 CM4_TPIU_TPIU_FSCR

Description: Formatter Synchronization Counter Register
Address: 0xE008E308
Offset: 0x308
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.8 CM4_TPIU_TRIGGER

Description: TRIGGER register
Address: 0xE008EEE8
Offset: 0xEE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.9 CM4_TPIU_FIFO_DATA_0

Description: Integration ETM Data
Address: 0xE008EEEE
Offset: 0xEEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.10 CM4_TPIU_ITATBCTR2

Description: Integration Register
Address: 0xE008EEF0
Offset: 0xEF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.11 CM4_TPIU_ITATBCTR0

Description: Integration Register
Address: 0xE008EEF8
Offset: 0xEF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.12 CM4_TPIU_FIFO_DATA_1

Description: Integration ITM Data
Address: 0xE008EEFC
Offset: 0xEFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.13 CM4_TPIU_ITCTRL

Description: Integration Mode Control Register
Address: 0xE008EF00
Offset: 0xF00
Retention: Retained
IsDeepSleep: No
Comment: This register enables the component to switch from a functional mode, the default behavior, to integration mode where the inputs and outputs of the component can be directly controlled for the purpose of integration testing and topology solving.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|------------|
| Name | None [7:1] | | | | | | | MODE [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | MODE | RW | R | 0 | When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. |

4.13.11.14 CM4_TPIU_CLAIMSET

Description: Claim Tag Set Register

Address: 0xE008EFA0

Offset: 0xFA0

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location allows individual bits to be set, write, and returns the number of bits that can be set, read.
You can determine how many claim bits are implemented by reading this register. For example, if 4 bits are implemented, a read of this register will return 0x0000000F. If no claim tag is implemented, then a read of this register will return 0x00000000.

Default: 0xF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:3 | TAG | RW1S | R | 15 | A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. |

4.13.11.15 CM4_TPIU_CLAIMCLR

Description: Claim Tag Clear Register

Address: 0xE008EFA4

Offset: 0xFA4

Retention: Retained

IsDeepSleep: No

Comment: This register forms one half of the Claim Tag value. This location enables individual bits to be cleared, write, and returns the current Claim Tag value, read. The width (n) of this register can be determined from reading the Claim Tag Set Register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | TAG [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:3 | TAG | RW1C | R | 0 | A bit programmable register bank that is zero at reset. |

4.13.11.16 CM4_TPIU_DEVID

Description: Device ID
Address: 0xE008EFC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment: This register is implementation-defined for each Part Number and Designer. This indicates the capabilities of the component. The entire 32-bit field can be used because the data width is determined by the particular component. Unused bits must read as zero.
If the component is configurable then it is recommended that this register reflects any changes to a standard configuration.
Default: 0xCA0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|----------------|--------------|---|---|---|---|
| Name | | | CLKRELAT [5:5] | MUXNUM [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|--------------------|----------------|----------------|----------------|
| Name | None [15:12] | | | | SWOUARTNRZ [11:11] | SWOMAN [10:10] | TCLKDATA [9:9] | FIFOSIZE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:4 | MUXNUM | R | R | 0 | Indicates the level of input multiplexing. When non-zero, this value indicates the type of multiplexing on the input to the ATB. Currently only 0x00 is supported, that is, no multiplexing is present. This value helps detect the ATB structure. |
| 5 | CLKRELAT | R | R | 1 | Indicates the relationship between atclk and traceclk. This bit is '1' indicating traceclk can be asynchronous to atclk. |
| 6:8 | FIFOSIZE | R | R | 2 | TPIU buffer size. This field value is 0b010 indicating 4 Bytes. |
| 9 | TCLKDATA | R | R | 0 | This bit Reads-As-Zero (RAZ), indicating that trace data and clock modes are supported |
| 10 | SWOMAN | R | R | 1 | Indicates whether Serial Wire Output, Manchester encoded format, is supported. |
| 11 | SWOUARTNRZ | R | R | 1 | Indicates whether Serial Wire Output, UART or NRZ, is supported. |

4.13.11.17 CM4_TPIU_DEVTYPE

Description: Device Type Identifier Register
Address: 0xE008EFCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x11

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|-------------|---|---|---|
| Name | SUB_TYPE [7:4] | | | | CLASS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:3 | CLASS | R | R | 1 | Indicates that this is trace sink component. |
| 4:7 | SUB_TYPE | R | R | 1 | Indicates that this component is a trace port component. |

4.13.11.18 CM4_TPIU_PID4

Description: Peripheral Identification Register 4
Address: 0xE008EFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 4 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.19 CM4_TPIU_PID5

Description: Peripheral Identification Register 5
Address: 0xE008EFD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.20 CM4_TPIU_PID6

Description: Peripheral Identification Register 6
Address: 0xE008EFD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.21 CM4_TPIU_PID7

Description: Peripheral Identification Register 7
Address: 0xE008EFDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.22 CM4_TPIU_PID0

Description: Peripheral Identification Register 0
Address: 0xE008EFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x23

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 35 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. PID0 indicates this is M3-TPIU (but this is a non-issue) |

4.13.11.23 CM4_TPIU_PID1

Description: Peripheral Identification Register 1
Address: 0xE008EFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB9

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 185 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.24 CM4_TPIU_PID2

Description: Peripheral Identification Register 2
Address: 0xE008EFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3B

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 59 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.25 CM4_TPIU_PID3

Description: Peripheral Identification Register 3
Address: 0xE008EFEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|------------|---|---|---|
| Name | ECOREVNUM [7:4] | | | | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 4:7 | ECOREVNUM | R | R | 0 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.26 CM4_TPIU_CID0

Description: Component Identification Register 0
Address: 0xE008EFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 13 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.27 CM4_TPIU_CID1

Description: Component Identification Register 1
Address: 0xE008EFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x90

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 144 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.28 CM4_TPIU_CID2

Description: Component Identification Register 2
Address: 0xE008EFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 5 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.11.29 CM4_TPIU_CID3

Description: Component Identification Register 3
Address: 0xE008EFFF
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | VALUE | R | R | 177 | Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. |

4.13.12 ROMTABLE

4.13.12.1 CM4_ROMTABLE_TRC_CTI

Description: CM4 CoreSight ROM Table Peripheral #0
Address: 0xE00FF000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF81003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------------------|
| 0:31 | VALUE | R | | 4294447107 | Offset to TRC CTI component |

4.13.12.2 CM4_ROMTABLE_TRC_CSTF

Description: CM4 CoreSight ROM Table Peripheral #1
Address: 0xE00FF004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF8D003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---------------------------------|
| 0:31 | VALUE | R | | 4294496259 | Offset to TRC funnel component. |

4.13.12.3 CM4_ROMTABLE_TRC_ETB

Description: CM4 CoreSight ROM Table Peripheral #2
Address: 0xE00FF008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF8E003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--------------------------|
| 0:31 | VALUE | R | | 429450035 5 | Offset to ETB component. |

4.13.12.4 CM4_ROMTABLE_TRC_TPIU

Description: CM4 CoreSight ROM Table Peripheral #3
Address: 0xE00FF00C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF8F003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--------------------------|
| 0:31 | VALUE | R | | 429450445 1 | Offset to TPIU ROM Table |

4.13.12.5 CM4_ROMTABLE_CM4

Description: CM4 CoreSight ROM Table Peripheral #4
Address: 0xE00FF010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF80003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------------------|
| 0:31 | VALUE | R | | 429444301 1 | Offset to CM4 ROM Table |

4.13.12.6 CM4_ROMTABLE_CSMT

Description: CM4 CoreSight ROM Table Memory Type
Address: 0xE00FFFCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | | 1 | Memory Type |

4.13.12.7 CM4_ROMTABLE_PID4

Description: CM4 CoreSight ROM Table Peripheral ID #4
Address: 0xE00FFFD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 4 | Peripheral ID #4 |

4.13.12.8 CM4_ROMTABLE_PID0

Description: CM4 CoreSight ROM Table Peripheral ID #0
Address: 0xE00FFFE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 192 | Peripheral ID #0 |

4.13.12.9 CM4_ROMTABLE_PID1

Description: CM4 CoreSight ROM Table Peripheral ID #1
Address: 0xE00FFFE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 180 | Peripheral ID #1 |

4.13.12.10 CM4_ROMTABLE_PID2

Description: CM4 CoreSight ROM Table Peripheral ID #2
Address: 0xE00FFFE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 11 | Peripheral ID #2 |

4.13.12.11 CM4_ROMTABLE_PID3

Description: CM4 CoreSight ROM Table Peripheral ID #3
Address: 0xE00FFFE0
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|------------------|
| 0:31 | VALUE | R | | 0 | Peripheral ID #3 |

4.13.12.12 CM4_ROMTABLE_CID0

Description: CM4 CoreSight ROM Table Component ID #0
Address: 0xE00FFFF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 13 | Component ID #0 |

4.13.12.13 CM4_ROMTABLE_CID1

Description: CM4 CoreSight ROM Table Component ID #1
Address: 0xE00FFFF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 16 | Component ID #1 |

4.13.12.14 CM4_ROMTABLE_CID2

Description: CM4 CoreSight ROM Table Component ID #2
Address: 0xE00FFF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 5 | Component ID #2 |

4.13.12.15 CM4_ROMTABLE_CID3

Description: CM4 CoreSight ROM Table Component ID #3
Address: 0xE00FFFFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-----------------|
| 0:31 | VALUE | R | | 177 | Component ID #3 |

5 CPUSS

Description CPU subsystem (CPUSS)
Base Address 0x40200000
Size 0x10000
Slave Num MMIO2 - 0

| Register Name | Address | Permission | Description |
|---|------------|------------|--|
| CPUSS_IDENTITY | 0x40200000 | FULL | Identity |
| CPUSS_CM4_STATUS | 0x40200004 | FULL | CM4 status |
| CPUSS_CM4_CLOCK_CTL | 0x40200008 | FULL | CM4 clock control |
| CPUSS_CM4_CTL | 0x4020000C | FULL | CM4 control |
| CPUSS_CM4_INT0_STATUS | 0x40200100 | FULL | CM4 interrupt 0 status |
| CPUSS_CM4_INT1_STATUS | 0x40200104 | FULL | CM4 interrupt 1 status |
| CPUSS_CM4_INT2_STATUS | 0x40200108 | FULL | CM4 interrupt 2 status |
| CPUSS_CM4_INT3_STATUS | 0x4020010C | FULL | CM4 interrupt 3 status |
| CPUSS_CM4_INT4_STATUS | 0x40200110 | FULL | CM4 interrupt 4 status |
| CPUSS_CM4_INT5_STATUS | 0x40200114 | FULL | CM4 interrupt 5 status |
| CPUSS_CM4_INT6_STATUS | 0x40200118 | FULL | CM4 interrupt 6 status |
| CPUSS_CM4_INT7_STATUS | 0x4020011C | FULL | CM4 interrupt 7 status |
| CPUSS_CM4_VECTOR_TABLE_BASE | 0x40200200 | FULL | CM4 vector table base |
| CPUSS_CM4_NMI_CTL0 | 0x40200240 | FULL | CM4 NMI control |
| CPUSS_CM4_NMI_CTL1 | 0x40200244 | FULL | CM4 NMI control |
| CPUSS_CM4_NMI_CTL2 | 0x40200248 | FULL | CM4 NMI control |
| CPUSS_CM4_NMI_CTL3 | 0x4020024C | FULL | CM4 NMI control |
| CPUSS_CM0_CTL | 0x40201000 | FULL | CM0+ control |
| CPUSS_CM0_STATUS | 0x40201004 | FULL | CM0+ status |
| CPUSS_CM0_CLOCK_CTL | 0x40201008 | FULL | CM0+ clock control |
| CPUSS_CM0_INT0_STATUS | 0x40201100 | FULL | CM0+ interrupt 0 status |
| CPUSS_CM0_INT1_STATUS | 0x40201104 | FULL | CM0+ interrupt 1 status |
| CPUSS_CM0_INT2_STATUS | 0x40201108 | FULL | CM0+ interrupt 2 status |
| CPUSS_CM0_INT3_STATUS | 0x4020110C | FULL | CM0+ interrupt 3 status |
| CPUSS_CM0_INT4_STATUS | 0x40201110 | FULL | CM0+ interrupt 4 status |
| CPUSS_CM0_INT5_STATUS | 0x40201114 | FULL | CM0+ interrupt 5 status |
| CPUSS_CM0_INT6_STATUS | 0x40201118 | FULL | CM0+ interrupt 6 status |
| CPUSS_CM0_INT7_STATUS | 0x4020111C | FULL | CM0+ interrupt 7 status |
| CPUSS_CM0_VECTOR_TABLE_BASE | 0x40201120 | FULL | CM0+ vector table base |
| CPUSS_CM0_NMI_CTL0 | 0x40201140 | FULL | CM0+ NMI control |
| CPUSS_CM0_NMI_CTL1 | 0x40201144 | FULL | CM0+ NMI control |
| CPUSS_CM0_NMI_CTL2 | 0x40201148 | FULL | CM0+ NMI control |
| CPUSS_CM0_NMI_CTL3 | 0x4020114C | FULL | CM0+ NMI control |
| CPUSS_CM4_PWR_CTL | 0x40201200 | FULL | CM4 power control |
| CPUSS_CM4_PWR_DELAY_CTL | 0x40201204 | FULL | CM4 power control |
| CPUSS_RAM0_CTL0 | 0x40201300 | FULL | RAM 0 control |
| CPUSS_RAM0_STATUS | 0x40201304 | FULL | RAM 0 status |
| CPUSS_RAM0_PWR_MACRO_CTL0 | 0x40201340 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL1 | 0x40201344 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL2 | 0x40201348 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL3 | 0x4020134C | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL4 | 0x40201350 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL5 | 0x40201354 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL6 | 0x40201358 | FULL | RAM 0 power control |
| CPUSS_RAM0_PWR_MACRO_CTL7 | 0x4020135C | FULL | RAM 0 power control |
| CPUSS_RAM1_CTL0 | 0x40201380 | FULL | RAM 1 control |
| CPUSS_RAM1_STATUS | 0x40201384 | FULL | RAM 1 status |
| CPUSS_RAM1_PWR_CTL | 0x40201388 | FULL | RAM 1 power control |
| CPUSS_RAM_PWR_DELAY_CTL | 0x402013C0 | FULL | Power up delay used for all SRAM power domains |
| CPUSS_ROM_CTL | 0x402013C4 | FULL | ROM control |
| CPUSS_ECC_CTL | 0x402013C8 | FULL | ECC control |
| CPUSS_PRODUCT_ID | 0x40201400 | FULL | Product identifier and version (same as CoreSight RomTables) |
| CPUSS_DP_STATUS | 0x40201410 | FULL | Debug port status |
| CPUSS_AP_CTL | 0x40201414 | FULL | Access port control |

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-------------------------------------|
| CPUSS_BUFF_CTL | 0x40201500 | FULL | Buffer control |
| CPUSS_SYSTICK_CTL | 0x40201600 | FULL | SysTick timer control |
| CPUSS_CAL_SUP_SET | 0x40201800 | FULL | Calibration support set and read |
| CPUSS_CAL_SUP_CLR | 0x40201804 | FULL | Calibration support clear and reset |
| CPUSS_CM0_PC_CTL | 0x40202000 | READ | CM0+ protection context control |
| CPUSS_CM0_PC0_HANDLER | 0x40202040 | READ | CM0+ protection context 0 handler |
| CPUSS_CM0_PC1_HANDLER | 0x40202044 | READ | CM0+ protection context 1 handler |
| CPUSS_CM0_PC2_HANDLER | 0x40202048 | READ | CM0+ protection context 2 handler |
| CPUSS_CM0_PC3_HANDLER | 0x4020204C | READ | CM0+ protection context 3 handler |
| CPUSS_PROTECTION | 0x402020C4 | READ | Protection status |
| CPUSS_TRIM_ROM_CTL | 0x40202100 | READ | ROM trim control |
| CPUSS_TRIM_RAM_CTL | 0x40202104 | READ | RAM trim control |
| CPUSS_CM0_SYSTEM_INT_CTL0 | 0x40208000 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL1 | 0x40208004 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL2 | 0x40208008 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL3 | 0x4020800C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL4 | 0x40208010 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL5 | 0x40208014 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL6 | 0x40208018 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL7 | 0x4020801C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL8 | 0x40208020 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL9 | 0x40208024 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL10 | 0x40208028 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL11 | 0x4020802C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL12 | 0x40208030 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL13 | 0x40208034 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL14 | 0x40208038 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL15 | 0x4020803C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL16 | 0x40208040 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL17 | 0x40208044 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL18 | 0x40208048 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL19 | 0x4020804C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL20 | 0x40208050 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL21 | 0x40208054 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL22 | 0x40208058 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL23 | 0x4020805C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL24 | 0x40208060 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL25 | 0x40208064 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL26 | 0x40208068 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL27 | 0x4020806C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL28 | 0x40208070 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL29 | 0x40208074 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL30 | 0x40208078 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL31 | 0x4020807C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL32 | 0x40208080 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL33 | 0x40208084 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL34 | 0x40208088 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL35 | 0x4020808C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL36 | 0x40208090 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL37 | 0x40208094 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL38 | 0x40208098 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL39 | 0x4020809C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL40 | 0x402080A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL41 | 0x402080A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL42 | 0x402080A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL43 | 0x402080AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL44 | 0x402080B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL45 | 0x402080B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL46 | 0x402080B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL47 | 0x402080BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL48 | 0x402080C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL49 | 0x402080C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL50 | 0x402080C8 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-------------------------------|
| CPUSS_CM0_SYSTEM_INT_CTL51 | 0x402080CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL52 | 0x402080D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL53 | 0x402080D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL54 | 0x402080D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL55 | 0x402080DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL56 | 0x402080E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL57 | 0x402080E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL58 | 0x402080E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL59 | 0x402080EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL60 | 0x402080F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL61 | 0x402080F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL62 | 0x402080F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL63 | 0x402080FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL64 | 0x40208100 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL65 | 0x40208104 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL66 | 0x40208108 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL67 | 0x4020810C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL68 | 0x40208110 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL69 | 0x40208114 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL70 | 0x40208118 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL71 | 0x4020811C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL72 | 0x40208120 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL73 | 0x40208124 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL74 | 0x40208128 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL75 | 0x4020812C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL76 | 0x40208130 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL77 | 0x40208134 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL78 | 0x40208138 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL79 | 0x4020813C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL80 | 0x40208140 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL81 | 0x40208144 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL82 | 0x40208148 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL83 | 0x4020814C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL84 | 0x40208150 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL85 | 0x40208154 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL86 | 0x40208158 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL87 | 0x4020815C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL88 | 0x40208160 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL89 | 0x40208164 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL90 | 0x40208168 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL91 | 0x4020816C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL92 | 0x40208170 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL93 | 0x40208174 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL94 | 0x40208178 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL95 | 0x4020817C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL96 | 0x40208180 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL97 | 0x40208184 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL98 | 0x40208188 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL99 | 0x4020818C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL100 | 0x40208190 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL101 | 0x40208194 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL102 | 0x40208198 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL103 | 0x4020819C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL104 | 0x402081A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL105 | 0x402081A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL106 | 0x402081A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL107 | 0x402081AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL108 | 0x402081B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL109 | 0x402081B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL110 | 0x402081B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL111 | 0x402081BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL112 | 0x402081C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL113 | 0x402081C4 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-------------------------------|
| CPUSS_CM0_SYSTEM_INT_CTL114 | 0x402081C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL115 | 0x402081CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL116 | 0x402081D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL117 | 0x402081D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL118 | 0x402081D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL119 | 0x402081DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL120 | 0x402081E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL121 | 0x402081E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL122 | 0x402081E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL123 | 0x402081EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL124 | 0x402081F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL125 | 0x402081F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL126 | 0x402081F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL127 | 0x402081FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL128 | 0x40208200 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL129 | 0x40208204 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL130 | 0x40208208 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL131 | 0x4020820C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL132 | 0x40208210 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL133 | 0x40208214 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL134 | 0x40208218 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL135 | 0x4020821C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL136 | 0x40208220 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL137 | 0x40208224 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL138 | 0x40208228 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL139 | 0x4020822C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL140 | 0x40208230 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL141 | 0x40208234 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL142 | 0x40208238 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL143 | 0x4020823C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL144 | 0x40208240 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL145 | 0x40208244 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL146 | 0x40208248 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL147 | 0x4020824C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL148 | 0x40208250 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL149 | 0x40208254 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL150 | 0x40208258 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL151 | 0x4020825C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL152 | 0x40208260 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL153 | 0x40208264 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL154 | 0x40208268 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL155 | 0x4020826C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL156 | 0x40208270 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL157 | 0x40208274 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL158 | 0x40208278 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL159 | 0x4020827C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL160 | 0x40208280 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL161 | 0x40208284 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL162 | 0x40208288 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL163 | 0x4020828C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL164 | 0x40208290 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL165 | 0x40208294 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL166 | 0x40208298 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL167 | 0x4020829C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL168 | 0x402082A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL169 | 0x402082A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL170 | 0x402082A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL171 | 0x402082AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL172 | 0x402082B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL173 | 0x402082B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL174 | 0x402082B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL175 | 0x402082BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL176 | 0x402082C0 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-------------------------------|
| CPUSS_CM0_SYSTEM_INT_CTL177 | 0x402082C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL178 | 0x402082C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL179 | 0x402082CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL180 | 0x402082D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL181 | 0x402082D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL182 | 0x402082D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL183 | 0x402082DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL184 | 0x402082E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL185 | 0x402082E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL186 | 0x402082E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL187 | 0x402082EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL188 | 0x402082F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL189 | 0x402082F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL190 | 0x402082F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL191 | 0x402082FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL192 | 0x40208300 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL193 | 0x40208304 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL194 | 0x40208308 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL195 | 0x4020830C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL196 | 0x40208310 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL197 | 0x40208314 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL198 | 0x40208318 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL199 | 0x4020831C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL200 | 0x40208320 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL201 | 0x40208324 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL202 | 0x40208328 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL203 | 0x4020832C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL204 | 0x40208330 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL205 | 0x40208334 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL206 | 0x40208338 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL207 | 0x4020833C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL208 | 0x40208340 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL209 | 0x40208344 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL210 | 0x40208348 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL211 | 0x4020834C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL212 | 0x40208350 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL213 | 0x40208354 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL214 | 0x40208358 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL215 | 0x4020835C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL216 | 0x40208360 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL217 | 0x40208364 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL218 | 0x40208368 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL219 | 0x4020836C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL220 | 0x40208370 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL221 | 0x40208374 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL222 | 0x40208378 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL223 | 0x4020837C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL224 | 0x40208380 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL225 | 0x40208384 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL226 | 0x40208388 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL227 | 0x4020838C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL228 | 0x40208390 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL229 | 0x40208394 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL230 | 0x40208398 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL231 | 0x4020839C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL232 | 0x402083A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL233 | 0x402083A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL234 | 0x402083A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL235 | 0x402083AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL236 | 0x402083B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL237 | 0x402083B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL238 | 0x402083B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL239 | 0x402083BC | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-------------------------------|
| CPUSS_CM0_SYSTEM_INT_CTL240 | 0x402083C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL241 | 0x402083C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL242 | 0x402083C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL243 | 0x402083CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL244 | 0x402083D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL245 | 0x402083D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL246 | 0x402083D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL247 | 0x402083DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL248 | 0x402083E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL249 | 0x402083E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL250 | 0x402083E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL251 | 0x402083EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL252 | 0x402083F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL253 | 0x402083F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL254 | 0x402083F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL255 | 0x402083FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL256 | 0x40208400 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL257 | 0x40208404 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL258 | 0x40208408 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL259 | 0x4020840C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL260 | 0x40208410 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL261 | 0x40208414 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL262 | 0x40208418 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL263 | 0x4020841C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL264 | 0x40208420 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL265 | 0x40208424 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL266 | 0x40208428 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL267 | 0x4020842C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL268 | 0x40208430 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL269 | 0x40208434 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL270 | 0x40208438 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL271 | 0x4020843C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL272 | 0x40208440 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL273 | 0x40208444 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL274 | 0x40208448 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL275 | 0x4020844C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL276 | 0x40208450 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL277 | 0x40208454 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL278 | 0x40208458 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL279 | 0x4020845C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL280 | 0x40208460 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL281 | 0x40208464 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL282 | 0x40208468 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL283 | 0x4020846C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL284 | 0x40208470 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL285 | 0x40208474 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL286 | 0x40208478 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL287 | 0x4020847C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL288 | 0x40208480 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL289 | 0x40208484 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL290 | 0x40208488 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL291 | 0x4020848C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL292 | 0x40208490 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL293 | 0x40208494 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL294 | 0x40208498 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL295 | 0x4020849C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL296 | 0x402084A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL297 | 0x402084A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL298 | 0x402084A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL299 | 0x402084AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL300 | 0x402084B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL301 | 0x402084B4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL302 | 0x402084B8 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-------------------------------|
| CPUSS_CM0_SYSTEM_INT_CTL303 | 0x402084BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL304 | 0x402084C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL305 | 0x402084C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL306 | 0x402084C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL307 | 0x402084CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL308 | 0x402084D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL309 | 0x402084D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL310 | 0x402084D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL311 | 0x402084DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL312 | 0x402084E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL313 | 0x402084E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL314 | 0x402084E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL315 | 0x402084EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL316 | 0x402084F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL317 | 0x402084F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL318 | 0x402084F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL319 | 0x402084FC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL320 | 0x40208500 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL321 | 0x40208504 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL322 | 0x40208508 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL323 | 0x4020850C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL324 | 0x40208510 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL325 | 0x40208514 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL326 | 0x40208518 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL327 | 0x4020851C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL328 | 0x40208520 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL329 | 0x40208524 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL330 | 0x40208528 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL331 | 0x4020852C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL332 | 0x40208530 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL333 | 0x40208534 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL334 | 0x40208538 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL335 | 0x4020853C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL336 | 0x40208540 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL337 | 0x40208544 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL338 | 0x40208548 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL339 | 0x4020854C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL340 | 0x40208550 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL341 | 0x40208554 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL342 | 0x40208558 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL343 | 0x4020855C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL344 | 0x40208560 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL345 | 0x40208564 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL346 | 0x40208568 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL347 | 0x4020856C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL348 | 0x40208570 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL349 | 0x40208574 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL350 | 0x40208578 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL351 | 0x4020857C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL352 | 0x40208580 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL353 | 0x40208584 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL354 | 0x40208588 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL355 | 0x4020858C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL356 | 0x40208590 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL357 | 0x40208594 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL358 | 0x40208598 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL359 | 0x4020859C | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL360 | 0x402085A0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL361 | 0x402085A4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL362 | 0x402085A8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL363 | 0x402085AC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL364 | 0x402085B0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL365 | 0x402085B4 | FULL | CM0+ system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-------------------------------|
| CPUSS_CM0_SYSTEM_INT_CTL366 | 0x402085B8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL367 | 0x402085BC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL368 | 0x402085C0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL369 | 0x402085C4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL370 | 0x402085C8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL371 | 0x402085CC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL372 | 0x402085D0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL373 | 0x402085D4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL374 | 0x402085D8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL375 | 0x402085DC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL376 | 0x402085E0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL377 | 0x402085E4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL378 | 0x402085E8 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL379 | 0x402085EC | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL380 | 0x402085F0 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL381 | 0x402085F4 | FULL | CM0+ system interrupt control |
| CPUSS_CM0_SYSTEM_INT_CTL382 | 0x402085F8 | FULL | CM0+ system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL0 | 0x4020A000 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL1 | 0x4020A004 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL2 | 0x4020A008 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL3 | 0x4020A00C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL4 | 0x4020A010 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL5 | 0x4020A014 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL6 | 0x4020A018 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL7 | 0x4020A01C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL8 | 0x4020A020 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL9 | 0x4020A024 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL10 | 0x4020A028 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL11 | 0x4020A02C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL12 | 0x4020A030 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL13 | 0x4020A034 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL14 | 0x4020A038 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL15 | 0x4020A03C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL16 | 0x4020A040 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL17 | 0x4020A044 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL18 | 0x4020A048 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL19 | 0x4020A04C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL20 | 0x4020A050 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL21 | 0x4020A054 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL22 | 0x4020A058 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL23 | 0x4020A05C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL24 | 0x4020A060 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL25 | 0x4020A064 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL26 | 0x4020A068 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL27 | 0x4020A06C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL28 | 0x4020A070 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL29 | 0x4020A074 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL30 | 0x4020A078 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL31 | 0x4020A07C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL32 | 0x4020A080 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL33 | 0x4020A084 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL34 | 0x4020A088 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL35 | 0x4020A08C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL36 | 0x4020A090 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL37 | 0x4020A094 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL38 | 0x4020A098 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL39 | 0x4020A09C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL40 | 0x4020A0A0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL41 | 0x4020A0A4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL42 | 0x4020A0A8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL43 | 0x4020A0AC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL44 | 0x4020A0B0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL45 | 0x4020A0B4 | FULL | CM4 system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------|
| CPUSS_CM4_SYSTEM_INT_CTL46 | 0x4020A0B8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL47 | 0x4020A0BC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL48 | 0x4020A0C0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL49 | 0x4020A0C4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL50 | 0x4020A0C8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL51 | 0x4020A0CC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL52 | 0x4020A0D0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL53 | 0x4020A0D4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL54 | 0x4020A0D8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL55 | 0x4020A0DC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL56 | 0x4020A0E0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL57 | 0x4020A0E4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL58 | 0x4020A0E8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL59 | 0x4020A0EC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL60 | 0x4020A0F0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL61 | 0x4020A0F4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL62 | 0x4020A0F8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL63 | 0x4020A0FC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL64 | 0x4020A100 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL65 | 0x4020A104 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL66 | 0x4020A108 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL67 | 0x4020A10C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL68 | 0x4020A110 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL69 | 0x4020A114 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL70 | 0x4020A118 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL71 | 0x4020A11C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL72 | 0x4020A120 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL73 | 0x4020A124 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL74 | 0x4020A128 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL75 | 0x4020A12C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL76 | 0x4020A130 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL77 | 0x4020A134 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL78 | 0x4020A138 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL79 | 0x4020A13C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL80 | 0x4020A140 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL81 | 0x4020A144 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL82 | 0x4020A148 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL83 | 0x4020A14C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL84 | 0x4020A150 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL85 | 0x4020A154 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL86 | 0x4020A158 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL87 | 0x4020A15C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL88 | 0x4020A160 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL89 | 0x4020A164 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL90 | 0x4020A168 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL91 | 0x4020A16C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL92 | 0x4020A170 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL93 | 0x4020A174 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL94 | 0x4020A178 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL95 | 0x4020A17C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL96 | 0x4020A180 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL97 | 0x4020A184 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL98 | 0x4020A188 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL99 | 0x4020A18C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL100 | 0x4020A190 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL101 | 0x4020A194 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL102 | 0x4020A198 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL103 | 0x4020A19C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL104 | 0x4020A1A0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL105 | 0x4020A1A4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL106 | 0x4020A1A8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL107 | 0x4020A1AC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL108 | 0x4020A1B0 | FULL | CM4 system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------|
| CPUSS_CM4_SYSTEM_INT_CTL109 | 0x4020A1B4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL110 | 0x4020A1B8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL111 | 0x4020A1BC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL112 | 0x4020A1C0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL113 | 0x4020A1C4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL114 | 0x4020A1C8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL115 | 0x4020A1CC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL116 | 0x4020A1D0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL117 | 0x4020A1D4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL118 | 0x4020A1D8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL119 | 0x4020A1DC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL120 | 0x4020A1E0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL121 | 0x4020A1E4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL122 | 0x4020A1E8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL123 | 0x4020A1EC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL124 | 0x4020A1F0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL125 | 0x4020A1F4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL126 | 0x4020A1F8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL127 | 0x4020A1FC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL128 | 0x4020A200 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL129 | 0x4020A204 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL130 | 0x4020A208 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL131 | 0x4020A20C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL132 | 0x4020A210 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL133 | 0x4020A214 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL134 | 0x4020A218 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL135 | 0x4020A21C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL136 | 0x4020A220 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL137 | 0x4020A224 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL138 | 0x4020A228 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL139 | 0x4020A22C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL140 | 0x4020A230 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL141 | 0x4020A234 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL142 | 0x4020A238 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL143 | 0x4020A23C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL144 | 0x4020A240 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL145 | 0x4020A244 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL146 | 0x4020A248 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL147 | 0x4020A24C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL148 | 0x4020A250 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL149 | 0x4020A254 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL150 | 0x4020A258 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL151 | 0x4020A25C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL152 | 0x4020A260 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL153 | 0x4020A264 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL154 | 0x4020A268 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL155 | 0x4020A26C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL156 | 0x4020A270 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL157 | 0x4020A274 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL158 | 0x4020A278 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL159 | 0x4020A27C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL160 | 0x4020A280 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL161 | 0x4020A284 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL162 | 0x4020A288 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL163 | 0x4020A28C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL164 | 0x4020A290 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL165 | 0x4020A294 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL166 | 0x4020A298 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL167 | 0x4020A29C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL168 | 0x4020A2A0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL169 | 0x4020A2A4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL170 | 0x4020A2A8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL171 | 0x4020A2AC | FULL | CM4 system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------|
| CPUSS_CM4_SYSTEM_INT_CTL172 | 0x4020A2B0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL173 | 0x4020A2B4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL174 | 0x4020A2B8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL175 | 0x4020A2BC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL176 | 0x4020A2C0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL177 | 0x4020A2C4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL178 | 0x4020A2C8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL179 | 0x4020A2CC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL180 | 0x4020A2D0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL181 | 0x4020A2D4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL182 | 0x4020A2D8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL183 | 0x4020A2DC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL184 | 0x4020A2E0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL185 | 0x4020A2E4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL186 | 0x4020A2E8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL187 | 0x4020A2EC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL188 | 0x4020A2F0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL189 | 0x4020A2F4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL190 | 0x4020A2F8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL191 | 0x4020A2FC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL192 | 0x4020A300 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL193 | 0x4020A304 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL194 | 0x4020A308 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL195 | 0x4020A30C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL196 | 0x4020A310 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL197 | 0x4020A314 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL198 | 0x4020A318 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL199 | 0x4020A31C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL200 | 0x4020A320 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL201 | 0x4020A324 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL202 | 0x4020A328 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL203 | 0x4020A32C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL204 | 0x4020A330 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL205 | 0x4020A334 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL206 | 0x4020A338 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL207 | 0x4020A33C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL208 | 0x4020A340 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL209 | 0x4020A344 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL210 | 0x4020A348 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL211 | 0x4020A34C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL212 | 0x4020A350 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL213 | 0x4020A354 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL214 | 0x4020A358 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL215 | 0x4020A35C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL216 | 0x4020A360 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL217 | 0x4020A364 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL218 | 0x4020A368 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL219 | 0x4020A36C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL220 | 0x4020A370 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL221 | 0x4020A374 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL222 | 0x4020A378 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL223 | 0x4020A37C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL224 | 0x4020A380 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL225 | 0x4020A384 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL226 | 0x4020A388 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL227 | 0x4020A38C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL228 | 0x4020A390 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL229 | 0x4020A394 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL230 | 0x4020A398 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL231 | 0x4020A39C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL232 | 0x4020A3A0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL233 | 0x4020A3A4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL234 | 0x4020A3A8 | FULL | CM4 system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------|
| CPUSS_CM4_SYSTEM_INT_CTL235 | 0x4020A3AC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL236 | 0x4020A3B0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL237 | 0x4020A3B4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL238 | 0x4020A3B8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL239 | 0x4020A3BC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL240 | 0x4020A3C0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL241 | 0x4020A3C4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL242 | 0x4020A3C8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL243 | 0x4020A3CC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL244 | 0x4020A3D0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL245 | 0x4020A3D4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL246 | 0x4020A3D8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL247 | 0x4020A3DC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL248 | 0x4020A3E0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL249 | 0x4020A3E4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL250 | 0x4020A3E8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL251 | 0x4020A3EC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL252 | 0x4020A3F0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL253 | 0x4020A3F4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL254 | 0x4020A3F8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL255 | 0x4020A3FC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL256 | 0x4020A400 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL257 | 0x4020A404 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL258 | 0x4020A408 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL259 | 0x4020A40C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL260 | 0x4020A410 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL261 | 0x4020A414 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL262 | 0x4020A418 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL263 | 0x4020A41C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL264 | 0x4020A420 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL265 | 0x4020A424 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL266 | 0x4020A428 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL267 | 0x4020A42C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL268 | 0x4020A430 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL269 | 0x4020A434 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL270 | 0x4020A438 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL271 | 0x4020A43C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL272 | 0x4020A440 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL273 | 0x4020A444 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL274 | 0x4020A448 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL275 | 0x4020A44C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL276 | 0x4020A450 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL277 | 0x4020A454 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL278 | 0x4020A458 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL279 | 0x4020A45C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL280 | 0x4020A460 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL281 | 0x4020A464 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL282 | 0x4020A468 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL283 | 0x4020A46C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL284 | 0x4020A470 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL285 | 0x4020A474 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL286 | 0x4020A478 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL287 | 0x4020A47C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL288 | 0x4020A480 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL289 | 0x4020A484 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL290 | 0x4020A488 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL291 | 0x4020A48C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL292 | 0x4020A490 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL293 | 0x4020A494 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL294 | 0x4020A498 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL295 | 0x4020A49C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL296 | 0x4020A4A0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL297 | 0x4020A4A4 | FULL | CM4 system interrupt control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------|
| CPUSS_CM4_SYSTEM_INT_CTL298 | 0x4020A4A8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL299 | 0x4020A4AC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL300 | 0x4020A4B0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL301 | 0x4020A4B4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL302 | 0x4020A4B8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL303 | 0x4020A4BC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL304 | 0x4020A4C0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL305 | 0x4020A4C4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL306 | 0x4020A4C8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL307 | 0x4020A4CC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL308 | 0x4020A4D0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL309 | 0x4020A4D4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL310 | 0x4020A4D8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL311 | 0x4020A4DC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL312 | 0x4020A4E0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL313 | 0x4020A4E4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL314 | 0x4020A4E8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL315 | 0x4020A4EC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL316 | 0x4020A4F0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL317 | 0x4020A4F4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL318 | 0x4020A4F8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL319 | 0x4020A4FC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL320 | 0x4020A500 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL321 | 0x4020A504 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL322 | 0x4020A508 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL323 | 0x4020A50C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL324 | 0x4020A510 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL325 | 0x4020A514 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL326 | 0x4020A518 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL327 | 0x4020A51C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL328 | 0x4020A520 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL329 | 0x4020A524 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL330 | 0x4020A528 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL331 | 0x4020A52C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL332 | 0x4020A530 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL333 | 0x4020A534 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL334 | 0x4020A538 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL335 | 0x4020A53C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL336 | 0x4020A540 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL337 | 0x4020A544 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL338 | 0x4020A548 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL339 | 0x4020A54C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL340 | 0x4020A550 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL341 | 0x4020A554 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL342 | 0x4020A558 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL343 | 0x4020A55C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL344 | 0x4020A560 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL345 | 0x4020A564 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL346 | 0x4020A568 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL347 | 0x4020A56C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL348 | 0x4020A570 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL349 | 0x4020A574 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL350 | 0x4020A578 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL351 | 0x4020A57C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL352 | 0x4020A580 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL353 | 0x4020A584 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL354 | 0x4020A588 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL355 | 0x4020A58C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL356 | 0x4020A590 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL357 | 0x4020A594 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL358 | 0x4020A598 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL359 | 0x4020A59C | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL360 | 0x4020A5A0 | FULL | CM4 system interrupt control |

| Register Name | Address | Permission | Description |
|---|------------|------------|------------------------------|
| CPUSS_CM4_SYSTEM_INT_CTL361 | 0x4020A5A4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL362 | 0x4020A5A8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL363 | 0x4020A5AC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL364 | 0x4020A5B0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL365 | 0x4020A5B4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL366 | 0x4020A5B8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL367 | 0x4020A5BC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL368 | 0x4020A5C0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL369 | 0x4020A5C4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL370 | 0x4020A5C8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL371 | 0x4020A5CC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL372 | 0x4020A5D0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL373 | 0x4020A5D4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL374 | 0x4020A5D8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL375 | 0x4020A5DC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL376 | 0x4020A5E0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL377 | 0x4020A5E4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL378 | 0x4020A5E8 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL379 | 0x4020A5EC | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL380 | 0x4020A5F0 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL381 | 0x4020A5F4 | FULL | CM4 system interrupt control |
| CPUSS_CM4_SYSTEM_INT_CTL382 | 0x4020A5F8 | FULL | CM4 system interrupt control |

5.1 Register Details

5.1.1 CPUSS_IDENTITY

| | |
|---------------------|--|
| Description: | Identity |
| Address: | 0x40200000 |
| Offset: | 0x0 |
| Retention: | Not Retained |
| IsDeepSleep: | No |
| Comment: | This register is typically used by SW that is executed on different bus masters or with different protection contexts. |
| Default: | 0x0 |

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|------------|----|----------|---------|
| Name | PC [7:4] | | | | None [3:2] | | NS [1:1] | P [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | MS [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | P | R | W | Undefined | This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. |
| 1 | NS | R | W | Undefined | This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. |
| 4:7 | PC | R | W | Undefined | This field specifies the protection context of the transfer that reads the register. |
| 8:11 | MS | R | W | Undefined | This field specifies the bus master identifier of the transfer that reads the register. |

5.1.2 CPUSS_CM4_STATUS

Description: CM4 status
Address: 0x40200004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x13

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|------------|---|-----------------|----------------|
| Name | None [7:5] | | | PWR_DONE [4:4] | None [3:2] | | SLEEPDEEP [1:1] | SLEEPING [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | SLEEPING | R | W | 1 | Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. |
| 1 | SLEEPDEEP | R | W | 1 | Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. |
| 4 | PWR_DONE | R | W | 1 | After a PWR_MODE change this flag indicates if the new power mode has taken effect or not. Note: this flag can also change as a result of a change in debug power up req |

5.1.3 CPUSS_CM4_CLOCK_CTL

Description: CM4 clock control
Address: 0x40200008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | FAST_INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 8:15 | FAST_INT_DIV | RW | R | 0 | <p>Specifies the fast clock divider (from the high frequency clock 'clk_hf' to the peripheral clock 'clk_fast'). Integer division by (1+FAST_INT_DIV). Allows for integer divisions in the range [1, 256] (FAST_INT_DIV is in the range [0, 255]).</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> |

5.1.4 CPUSS_CM4_CTL

Description: CM4 control
Address: 0x4020000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|--------------|----|------------------|------------------|------------------|------------------|------------------|
| Name | IDC_MASK [31:31] | None [30:29] | | IXC_MASK [28:28] | UFC_MASK [27:27] | OFC_MASK [26:26] | DZC_MASK [25:25] | IOC_MASK [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 24 | IOC_MASK | RW | R | 0 | <p>CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC 'invalid operation' exception condition:</p> <p>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.</p> <p>'1': the CPU's exception condition activates the CPU's floating point interrupt.</p> <p>Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are 'masked' with the fields a provide by this register (CM7_0_CTL). The 'masked' signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions.</p> <p>Note: the CPU's FPCSR exception conditions are 'sticky'. Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'.</p> <p>Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt.</p> |
| 25 | DZC_MASK | RW | R | 0 | <p>CPU FPU exception mask for the CPU's FPCSR.DZC 'divide by zero' exception condition:</p> <p>'0': The CPU's exception condition does NOT activate the CPU's floating point interrupt.</p> <p>'1': the CPU's exception condition activates the CPU's floating point interrupt.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 26 | OFC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.OFC 'overflow' exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. |
| 27 | UFC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.UFC 'underflow' exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. |
| 28 | IXC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.IXC 'inexact' exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the 'inexact' condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. |
| 31 | IDC_MASK | RW | R | 0 | CPU FPU exception mask for the CPU's FPCSR.IDC 'input denormalized' exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are 'flushed to zero'. Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. |

5.1.5 CPUSS_CM4_INT0_STATUS

Description: CM4 interrupt 0 status
Address: 0x40200100
Offset: 0x100
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 0. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.6 CPUSS_CM4_INT1_STATUS

Description: CM4 interrupt 1 status
Address: 0x40200104
Offset: 0x104
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 1. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.7 CPUSS_CM4_INT2_STATUS

Description: CM4 interrupt 2 status
Address: 0x40200108
Offset: 0x108
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 2. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.8 CPUSS_CM4_INT3_STATUS

Description: CM4 interrupt 3 status
Address: 0x4020010C
Offset: 0x10C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 3. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.9 CPUSS_CM4_INT4_STATUS

Description: CM4 interrupt 4 status
Address: 0x40200110
Offset: 0x110
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 4. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.10 CPUSS_CM4_INT5_STATUS

Description: CM4 interrupt 5 status
Address: 0x40200114
Offset: 0x114
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 5. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.11 CPUSS_CM4_INT6_STATUS

Description: CM4 interrupt 6 status
Address: 0x40200118
Offset: 0x118
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 6. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.12 CPUSS_CM4_INT7_STATUS

Description: CM4 interrupt 7 status
Address: 0x4020011C
Offset: 0x11C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM4 activated system interrupt index for CPU interrupt 7. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.13 CPUSS_CM4_VECTOR_TABLE_BASE

Description: CM4 vector table base
Address: 0x40200200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | None [9:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR22 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR22 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|--|
| 10:31 | ADDR22 | RW | | 0 | <p>Address of CM4 vector table. This register is used for CM4 warm and cold boot purposes: the CM0+ CPU initializes the CM4_VECTOR_TABLE_BASE register and the CM4 boot code uses the register to initialize the CM4 internal VTOR register.</p> <p>Note: the CM4 vector table is at an address that is a 1024 B multiple.</p> |

5.1.14 CPUSS_CM4_NMI_CTL

Description: CM4 NMI control

Address: 0x40200240

Offset: 0x240

Retention: Retained

IsDeepSleep: No

Comment: Note that multiple (four) CM4_NMI_CTL registers exist, allowing for multiple (four) system interrupts to be connected to the CPU NMI. The four selected system interrupts are logically OR'd into a single CPU NMI input. The NMI handler may need to investigate all selected system interrupt sources to identify the source of CPU NMI.

Default: 0x3FF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------------|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | RW | R | 1023 | System interrupt select for CPU NMI. The reset value ('1023') ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. |

5.1.15 CPUSS_CM0_CTL

Description: CM0+ control
Address: 0x40201000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFA050002

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---------------|-----------------|
| Name | None [7:2] | | | | | | ENABLED [1:1] | SLV_STALL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|------|-----------------|--|
| 0 | SLV_STALL | RW | R | 0 | <p>Processor debug access control:</p> <p>'0': Access.</p> <p>'1': Stall access.</p> <p>This field is used to stall/delay debug accesses. This is useful to protect execution of code that needs to be protected from debug accesses.</p> |
| 1 | ENABLED | RW | RW1S | 1 | <p>Processor enable:</p> <p>'0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM0+ reset, followed by a CM0+ warm boot.</p> <p>'1': Enabled.</p> <p>Note: The intent is that this bit is modified only through an external probe or by the CM4 while the CM0+ is in Sleep or DeepSleep power mode. If this field is cleared to '0' by the CM0+ itself, it should be done under controlled conditions (such that undesirable side effects can be prevented).</p> <p>Note: The CM0+ CPU has a AIRCR.SYSRESETREQ register field that allows the CM0+ to reset the complete device (ENABLED only disables/enables the CM0+), resulting in a warm boot. This CPU register field has similar 'built-in protection' as this CM0_CTL register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details).</p> |
| 16:31 | VECTKEYSTAT | R | | 64005 | <p>Register key (to prevent accidental writes).</p> <ul style="list-style-type: none"> - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. |

5.1.16 CPUSS_CM0_STATUS

Description: CM0+ status
Address: 0x40201004
Offset: 0x1004
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-----------------|----------------|
| Name | None [7:2] | | | | | | SLEEPDEEP [1:1] | SLEEPING [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | SLEEPING | R | W | 0 | Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. |
| 1 | SLEEPDEEP | R | W | 0 | Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. |

5.1.17 CPUSS_CM0_CLOCK_CTL

Description: CM0+ clock control
Address: 0x40201008
Offset: 0x1008
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | SLOW_INT_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | PERI_INT_DIV [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| 8:15 | SLOW_INT_DIV | RW | R | 0 | <p>Specifies the slow clock divider (from the peripheral clock 'clk_peri' to the slow clock 'clk_slow'). Integer division by (1+SLOW_INT_DIV). Allows for integer divisions in the range [1, 256] (SLOW_INT_DIV is in the range [0, 255]).</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> |
| 24:31 | PERI_INT_DIV | RW | R | 0 | <p>Specifies the peripheral clock divider (from the high frequency clock 'clk_hf' to the peripheral clock 'clk_peri'). Integer division by (1+PERI_INT_DIV). Allows for integer divisions in the range [1, 256] (PERI_INT_DIV is in the range [0, 255]).</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> <p>Note that $F_{peri} \leq F_{peri_max}$. F_{peri_max} is likely to be smaller than F_{hf_max}. In other words, if $F_{hf} = F_{hf_max}$, PERI_INT_DIV should not be set to '0'.</p> |

5.1.18 CPUSS_CM0_INT0_STATUS

Description: CM0+ interrupt 0 status
Address: 0x40201100
Offset: 0x1100
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | <p>Lowest CM0+ activated system interrupt index for CPU interrupt 0.</p> <p>Multiple system interrupts can be mapped on the same CPU interrupt. The selected system interrupt is the system interrupt with the lowest system interrupt index that has an activated interrupt request at the time of the fetch (system_interrupts[SYSTEM_INT_IDX] is '1').</p> <p>The CPU interrupt handler SW can read SYSTEM_INT_IDX to determine the system interrupt that activated the handler.</p> |
| 31 | SYSTEM_INT_VALID | R | W | 0 | Valid indication for SYSTEM_INT_IDX. When '0', no system interrupt for CPU interrupt 0 is valid/activated. |

5.1.19 CPUSS_CM0_INT1_STATUS

Description: CM0+ interrupt 1 status
Address: 0x40201104
Offset: 0x1104
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 1. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.20 CPUSS_CM0_INT2_STATUS

Description: CM0+ interrupt 2 status
Address: 0x40201108
Offset: 0x1108
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------------|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------------|--------------|----|----|----|----|----|----|
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 2. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.21 CPUSS_CM0_INT3_STATUS

Description: CM0+ interrupt 3 status
Address: 0x4020110C
Offset: 0x110C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 3. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.22 CPUSS_CM0_INT4_STATUS

Description: CM0+ interrupt 4 status
Address: 0x40201110
Offset: 0x1110
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 4. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.23 CPUSS_CM0_INT5_STATUS

Description: CM0+ interrupt 5 status
Address: 0x40201114
Offset: 0x1114
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 5. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.24 CPUSS_CM0_INT6_STATUS

Description: CM0+ interrupt 6 status
Address: 0x40201118
Offset: 0x1118
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 6. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.25 CPUSS_CM0_INT7_STATUS

Description: CM0+ interrupt 7 status
Address: 0x4020111C
Offset: 0x111C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----------------------|----|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SYSTEM_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | R | W | Undefined | Lowest CM0+ activated system interrupt index for CPU interrupt 7. See description of CM0_INT0_STATUS. |
| 31 | SYSTEM_INT_VALID | R | W | 0 | See description of CM0_INT0_STATUS. |

5.1.26 CPUSS_CM0_VECTOR_TABLE_BASE

Description: CM0+ vector table base
Address: 0x40201120
Offset: 0x1120
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | ADDR24 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR24 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR24 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 8:31 | ADDR24 | RW | | 0 | Address of CM0+ vector table. This register is used for CM0+ warm boot purposes: the CM0+ warm boot code uses the register to initialize the CM0+ internal VTOR register. Note: the CM0+ vector table is at an address that is a 256 B multiple. |

5.1.27 CPUSS_CM0_NMI_CTL

Description: CM0+ NMI control

Address: 0x40201140

Offset: 0x1140

Retention: Retained

IsDeepSleep: No

Comment: Note that multiple (four) CM0_NMI_CTL registers exist, allowing for multiple (four) system interrupts to be connected to the CPU NMI. The four selected system interrupts are logically OR'd into a single CPU NMI input. The NMI handler may need to investigate all selected system interrupt sources to identify the source of CPU NMI.

Default: 0x3FF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|---|---|---|---|---|---|---|
| Name | SYSTEM_INT_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------------|---|
| Name | None [15:10] | | | | | | SYSTEM_INT_IDX [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0:9 | SYSTEM_INT_IDX | RW | R | 1023 | System interrupt select for CPU NMI. The reset value ('1023') ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. |

5.1.28 CPUSS_CM4_PWR_CTL

Description: CM4 power control

Address: 0x40201200

Offset: 0x1200

Retention: Retained

IsDeepSleep: No

Comment: This register controls the CM4 power state. Please note that this register must not be modified while the CM4 is executing; doing so may corrupt/abort pending bus transaction by the CM4 and cause unexpected behaviors in the system, including deadlock. The intended usage of this register is by the CM0+ while the CM4 is in DeepSleep mode.

Default: 0xFA050001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 0:1 | PWR_MODE | RW | R | 1 | Power mode. |
| | OFF | | | 0 | Switch CM4 off Power off, clock off, isolate, reset and no retain. |
| | RESET | | | 1 | Reset CM4 Clock off, no isolated, no retain and reset. Note: The CM4 CPU has a AIRCR.SYSRESETREQ register field that allows the CM4 to reset the complete device (RESET only resets the CM4), resulting in a warm boot. |
| | RETAINED | | | 2 | Put CM4 in Retained mode This can only become effective if CM4 is in SleepDeep mode. Check PWR_DONE flag to see if CM4 RETAINED state has been reached. Power off, clock off, isolate, no reset and retain. |
| | ENABLED | | | 3 | Switch CM4 on. Power on, clock on, no isolate, no reset and no retain. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. |

5.1.29 CPUSS_CM4_PWR_DELAY_CTL

Description: CM4 power control
Address: 0x40201204
Offset: 0x1204
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x12C

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | UP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------|---|
| Name | None [15:10] | | | | | | UP [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:9 | UP | RW | R | 300 | Number clock cycles delay needed after power domain power up |

5.1.30 CPUSS_RAM0_CTL0

Description: RAM 0 control
Address: 0x40201300
Offset: 0x1300
Retention: Retained
IsDeepSleep: No
Comment: This register is for the CPUSS system SRAM controller 0.
Default: 0x30001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---------------|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---------------|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|--------------------|--------------------------|----------------|
| Name | None [23:19] | | | | | ECC_INJ_EN [18:18] | ECC_AUTO_CORRECT [17:17] | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:1 | SLOW_WS | RW | R | 1 | Memory wait states for the slow clock domain ('clk_slow'). The number of wait states is expressed in 'clk_hf' clock domain cycles. |
| 8:9 | FAST_WS | RW | R | 0 | Memory wait states for the fast clock domain ('clk_fast'). The number of wait states is expressed in 'clk_hf' clock domain cycles. |
| 16 | ECC_EN | RW | R | 1 | Enable ECC checking: '0': Disabled. '1': Enabled. |
| 17 | ECC_AUTO_CORRECT | RW | R | 1 | HW ECC autocorrect functionality: '0': Disabled. '1': Enabled. HW automatically writes back SRAM with corrected data when a recoverable ECC error is detected. |
| 18 | ECC_INJ_EN | RW | R | 0 | Enable error injection for system SRAM 0. When '1', the parity (ECC_CTL.PARITY) is used when a full 32-bit write is done to the ECC_CTL.WORD_ADDR word address of system SRAM 0. |

5.1.31 CPUSS_RAM0_STATUS

Description: RAM 0 status
Address: 0x40201304
Offset: 0x1304
Retention: Retained
IsDeepSleep: No
Comment: This register is for the CPUSS system SRAM controller 0.
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------|
| Name | None [7:1] | | | | | | | WB_EMPTY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0 | WB_EMPTY | R | W | 1 | Write buffer empty. This information is used when entering DeepSleep power mode: WB_EMPTY must be '1' before a transition to system DeepSleep power mode. '0': Write buffer NOT empty. '1': Write buffer empty. Note: the SRAM controller write buffer is only used when ECC checking is enabled. (RAMi_CTL.ECC_EN is '1'). |

5.1.32 CPUSS_RAM0_PWR_MACRO_CTL

Description: RAM 0 power control
Address: 0x40201340
Offset: 0x1340
Retention: Retained
IsDeepSleep: No
Comment: These registers control the system SRAM 0 power states of a single macro. System SRAM 0 consists of up to sixteen 32 kB macros. Each macro is a single power partition and is controlled through a dedicated control field in one of these registers.
Default: 0xFA050003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 0:1 | PWR_MODE | RW | R | 3 | SRAM Power mode. |
| | OFF | | | 0 | Turn OFF the SRAM. This will turn OFF both array and periphery power of the SRAM and SRAM memory contents are lost. |
| | RESERVED | | | 1 | undefined |
| | RETAINED | | | 2 | Keep SRAM in Retained mode. This will turn OFF the SRAM periphery power, but array power is ON to retain memory contents. The SRAM contents will be retained in DeepSleep system power mode. |
| | ENABLED | | | 3 | Enable SRAM for regular operation. The SRAM contents will be retained in DeepSleep system power mode. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. |

5.1.33 CPUSS_RAM1_CTL0

Description: RAM 1 control
Address: 0x40201380
Offset: 0x1380
Retention: Retained
IsDeepSleep: No
Comment: This register is for the CPUSS system SRAM controller 1.
Default: 0x30001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---------------|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---------------|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|--------------------|--------------------------|----------------|
| Name | None [23:19] | | | | | ECC_INJ_EN [18:18] | ECC_AUTO_CORRECT [17:17] | ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---------------|
| 0:1 | SLOW_WS | RW | R | 1 | See RAM0_CTL. |
| 8:9 | FAST_WS | RW | R | 0 | See RAM0_CTL. |
| 16 | ECC_EN | RW | R | 1 | See RAM0_CTL. |
| 17 | ECC_AUTO_CORRECT | RW | R | 1 | See RAM0_CTL. |
| 18 | ECC_INJ_EN | RW | R | 0 | See RAM0_CTL. |

5.1.34 CPUSS_RAM1_STATUS

Description: RAM 1 status
Address: 0x40201384
Offset: 0x1384
Retention: Retained
IsDeepSleep: No
Comment: This register is for the CPUSS system SRAM controller 1.
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------|
| Name | None [7:1] | | | | | | | WB_EMPTY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|------------------|
| 0 | WB_EMPTY | R | W | 1 | See RAM0_STATUS. |

5.1.35 CPUSS_RAM1_PWR_CTL

Description: RAM 1 power control

Address: 0x40201388

Offset: 0x1388

Retention: Retained

IsDeepSleep: No

Comment: This register controls the system SRAM 1 power states. System SRAM 1 consists of a single power partition.

Default: 0xFA050003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|-------------------------|
| 0:1 | PWR_MODE | RW | R | 3 | Power mode. |
| | OFF | | | 0 | See RAM0_PWR_MACRO_CTL. |
| | RESERVED | | | 1 | undefined |
| | RETAINED | | | 2 | See RAM0_PWR_MACRO_CTL. |
| | ENABLED | | | 3 | See RAM0_PWR_MACRO_CTL. |
| 16:31 | VECTKEYSTAT | R | | 64005 | See RAM0_PWR_MACRO_CTL. |

5.1.36 CPUSS_RAM_PWR_DELAY_CTL

Description: Power up delay used for all SRAM power domains
Address: 0x402013C0
Offset: 0x13C0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x96

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | UP [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------|---|
| Name | None [15:10] | | | | | | UP [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:9 | UP | RW | R | 150 | Number clock cycles delay needed after power domain power up |

5.1.37 CPUSS_ROM_CTL

Description: ROM control
Address: 0x402013C4
Offset: 0x13C4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---------------|---|
| Name | None [7:2] | | | | | | SLOW_WS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---------------|---|
| Name | None [15:10] | | | | | | FAST_WS [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:1 | SLOW_WS | RW | R | 1 | <p>Memory wait states for the slow clock domain ('clk_slow'). The number of wait states is expressed in 'clk_hf' clock domain cycles.</p> <p>Timing paths to and from the memory have a (fixed) minimum duration that always needs to be considered/met. The 'clk_hf' clock domain frequency determines this field's value such that the timing paths minimum duration is met. A table/formula will be provided for this field's values for different 'clk_hf' frequencies.</p> |
| 8:9 | FAST_WS | RW | R | 0 | <p>Memory wait states for the fast clock domain ('clk_fast'). The number of wait states is expressed in 'clk_hf' clock domain cycles.</p> |

5.1.38 CPUSS_ECC_CTL

Description: ECC control
Address: 0x402013C8
Offset: 0x13C8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|----|----|----|----|-------------------|
| Name | WORD_ADDR [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | WORD_ADDR [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | WORD_ADDR [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PARITY [31:25] | | | | | | | |
| | | | | | | | | WORD_ADDR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 0:24 | WORD_ADDR | RW | R | 0 | Specifies the word address where an error will be injected. - On a write transfer to this SRAM address and when the corresponding RAM0/RAM1/RAM2_CTL0.ECC_INJ_EN bit is '1', the parity (PARITY) is injected. This field needs to be written with the offset address within the memory, divided by 4. For example, if the RAM1 start address is 0x08010000, and an error is to be injected to address 0x08010040, then this field needs to be configured to 0x000010. |
| 25:31 | PARITY | RW | R | 0 | ECC parity to use for ECC error injection at address WORD_ADDR. |

5.1.39 CPUSS_PRODUCT_ID

Description: Product identifier and version (same as CoreSight RomTables)
Address: 0x40201400
Offset: 0x1400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | FAMILY_ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|------------------|----|---|---|
| Name | None [15:12] | | | | FAMILY_ID [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|-------------------|----|----|----|
| Name | MINOR_REV [23:20] | | | | MAJOR_REV [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 0:11 | FAMILY_ID | R | W | FAMILYID | Family ID a.k.a. Partnumber a.k.a. Silicon ID |
| 16:19 | MAJOR_REV | R | W | Undefined | Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) |
| 20:23 | MINOR_REV | R | W | Undefined | Minor Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) |

5.1.40 CPUSS_DP_STATUS

Description: Debug port status
Address: 0x40201410
Offset: 0x1410
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x4

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--------------------|--------------------|---------------------|
| Name | None [7:3] | | | | | SWJ_JTAG_SEL [2:2] | SWJ_DEBUG_EN [1:1] | SWJ_CONNECTED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | SWJ_CONNECTED | R | W | 0 | Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. |
| 1 | SWJ_DEBUG_EN | R | W | 0 | Specifies if SWJ debug is enabled, i.e. CDBGWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. |
| 2 | SWJ_JTAG_SEL | R | W | 1 | Specifies if the JTAG or SWD interface is selected. This signal is valid when DP_CTL.PTM_SEL is '0' (SWJ mode selected) and SWJ_CONNECTED is '1' (SWJ is connected). '0': SWD selected. '1': JTAG selected. |

5.1.41 CPUSS_AP_CTL

Description: Access port control

Address: 0x40201414

Offset: 0x1414

Retention: Retained

IsDeepSleep: No

Comment: This register enables individual test controller access ports (AP). Note that the system AP is further controlled by a AP specific MPU, the SMPU and PPU. The system AP MPU may be programmed to provide no or limited test controller access capabilities.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|------------------|------------------|------------------|
| Name | None [7:3] | | | | | SYS_ENABLE [2:2] | CM4_ENABLE [1:1] | CM0_ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|---------------------|---------------------|---------------------|
| Name | None [23:19] | | | | | SYS_DISABLE [18:18] | CM4_DISABLE [17:17] | CM0_DISABLE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|------|----|-----------------|--|
| 0 | CM0_ENABLE | RW | R | 0 | Enables the CM0 AP interface: '0': Disabled. '1': Enabled. |
| 1 | CM4_ENABLE | RW | R | 0 | Enables the CM4 AP interface: '0': Disabled. '1': Enabled. |
| 2 | SYS_ENABLE | RW | R | 0 | Enables the system AP interface: '0': Disabled. '1': Enabled. |
| 16 | CM0_DISABLE | RW1S | R | 0 | Disables the CM0 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM0_DISABLE is '0' and CM0_ENABLE is '1'. |
| 17 | CM4_DISABLE | RW1S | R | 0 | Disables the CM4 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM4_DISABLE is '0' and CM4_ENABLE is '1'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|------|----|-----------------|--|
| 18 | SYS_DISABLE | RW1S | R | 0 | <p>Disables the system AP interface: '0': Enabled. '1': Disabled.</p> <p>Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when SYS_DISABLE is '0' and SYS_ENABLE is '1'.</p> |

5.1.42 CPUSS_BUFF_CTL

Description: Buffer control

Address: 0x40201500

Offset: 0x1500

Retention: Retained

IsDeepSleep: No

Comment: The ARM CM0+ and CM4 CPUs use bufferable write transfers to the peripherals by default. As a result, CPU completion of the write transfer does not guarantee that the write transfer reached its destination, as the transfer may be buffered/posted in the bus infrastructure. Moreover, it is possible that the write transfer does not take place at all due to a PPU violation or a slave error, and in this case the resulting bus error response is not passed to the CPU. This may cause complications if the CPU assumes that completion of the write transfer implies that the write transfer has taken effect in a peripheral (e.g. clearing a peripheral's interrupt cause field). There are multiple possibilities to address this complication:

- Follow the write transfer with a read transfer from the same address, and check that the read data matches the expectation.
- Configure a fault structure such that the following faults are reported: MS_PPU_0 to MS_PPU_3 to report PPU violations, timeout or bus errors in the PERI master interfaces, and GROUP_FAULT_0 to GROUP_FAULT_15 (only for the existing peripheral groups) to report decoder or peripheral bus errors in the peripheral groups. The CPU can perform a read transfer after a series of write transfers to the same peripheral group. If the read transfer completes and no faults are reported, then the write transfers have been executed. Note that the fault reporting has some latency, so the faults may be reported after the completion of the read transfer.
- Use the CPU MPU to set write transfers to non-bufferable/non-posted.
- Use BUFF_CTL.WRITE_BUFF to ensure that all write transfers are non-bufferable/non-posted

Note: the CM4 CPU has an internal ACTLR.DISDEFWBUF register field that controls write transfers (the CM0_ CPU does NOT have this register).

Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------------|
| Name | None [7:1] | | | | | | | WRITE_BUFF [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | WRITE_BUFF | RW | R | 1 | Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. |

5.1.43 CPUSS_SYSTICK_CTL

Description: SysTick timer control

Address: 0x40201600

Offset: 0x1600

Retention: Retained

IsDeepSleep: No

Comment: The CPUSS SYSTICK_CTL MMIO NOREF, SKEW, TENMS register fields are reflected in the CPU's SysTick timer calibration register: SYST_CALIB (the CLOCK_SOURCE field is NOT reflected and only SW accessible through the CPUSS SYSTICK_CTL MMIO register).

Default: 0x40000147

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|--------------|----|----|----|----------------------|----|
| Name | TENMS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TENMS [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TENMS [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | NOREF [31:31] | SKEW [30:30] | None [29:26] | | | | CLOCK_SOURCE [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| 0:23 | TENMS | RW | R | 327 | Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. |
| 24:25 | CLOCK_SOURCE | RW | R | 0 | Specifies an external clock source: '0': The low frequency clock 'clk_lf' is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). '1': The internal main oscillator (IMO) clock 'clk_imo' is selected. The MXS40 platform uses a fixed frequency IMO clock. o '2': The external crystal oscillator (ECO) clock 'clk_eco' is selected. '3': The SRSS 'clk_timer' is selected ('clk_timer' is a divided/gated version of 'clk_hf' or 'clk_imo'). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. |
| 30 | SKEW | RW | R | 1 | Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. |
| 31 | NOREF | RW | R | 0 | Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. |

5.1.44 CPUSS_CAL_SUP_SET

Description: Calibration support set and read
Address: 0x40201800
Offset: 0x1800
Retention: Retained
IsDeepSleep: No
Comment: For ETAS support
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0:31 | DATA | RW1S | RW | 0 | Read without side effect, write 1 to set |

5.1.45 CPUSS_CAL_SUP_CLR

Description: Calibration support clear and reset
Address: 0x40201804
Offset: 0x1804
Retention: Retained
IsDeepSleep: No
Comment: Read side effect: reset on read (even when read from debug host)
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|---|
| 0:31 | DATA | RW1C | A | 0 | Read side effect: when read all bits are cleared, write 1 to clear a specific bit Note: no exception for the debug host, it also causes the read side effect |

5.1.46 CPUSS_CM0_PC_CTL

Description: CM0+ protection context control
Address: 0x40202000
Offset: 0x2000
Retention: Retained
IsDeepSleep: No
Comment: The CM0_PC_CTL and CM0_Pci_HANDLER register are typically initialized by the boot code.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-------------|---|---|---|
| Name | None [7:4] | | | | VALID [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:3 | VALID | RW | R | 0 | Valid fields for the protection context handler CM0_Pci_HANDLER registers: Bit 0: Valid field for CM0_PC0_HANDLER. Bit 1: Valid field for CM0_PC1_HANDLER. Bit 2: Valid field for CM0_PC2_HANDLER. Bit 3: Valid field for CM0_PC3_HANDLER. |

5.1.47 CPUSS_CM0_PC0_HANDLER

Description: CM0+ protection context 0 handler
Address: 0x40202040
Offset: 0x2040
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | ADDR [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | ADDR [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 0 handler. This field is used to detect entry to Cypress 'trusted' code through an exception/interrupt. |

5.1.48 CPUSS_CM0_PC1_HANDLER

Description: CM0+ protection context 1 handler
Address: 0x40202044
Offset: 0x2044
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 1 handler. |

5.1.49 CPUSS_CM0_PC2_HANDLER

Description: CM0+ protection context 2 handler
Address: 0x40202048
Offset: 0x2048
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 2 handler. |

5.1.50 CPUSS_CM0_PC3_HANDLER

Description: CM0+ protection context 3 handler
Address: 0x4020204C
Offset: 0x204C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | ADDR | RW | R | 0 | Address of the protection context 3 handler. |

5.1.51 CPUSS_PROTECTION

Description: Protection status
Address: 0x402020C4
Offset: 0x20C4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------|---|---|
| Name | None [7:3] | | | | | STATE [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:2 | STATE | RW | R | 0 | Protection state: '0': UNKNOWN. '1': VIRGIN. '2': NORMAL. '3': SECURE. '4': DEAD. The following state transitions are allowed (and enforced by HW): - UNKNOWN => VIRGIN/NORMAL/SECURE/DEAD - NORMAL => DEAD - SECURE => DEAD An attempt to make a NOT allowed state transition will NOT affect this register field. |

5.1.52 CPUSS_TRIM_ROM_CTL

Description: ROM trim control

Address: 0x40202100

Offset: 0x2100

Retention: Retained

IsDeepSleep: No

Comment: This register is used to trim ALL ROM memories in the device. Different operating Voltages may require different trim settings.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | TRIM [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TRIM [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TRIM [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TRIM [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|------------------|---|
| 0:31 | TRIM | RW | R | ROM_TRIM_DEFAULT | <p>For ARM ROMs the bits are defined as follows [2:0] EMA: Extra Margin Adjustment (0 is the fastest setting) Recommended default value: EMA=2 (ROM_TRIM_DEFAULT=0x0000_0002, ROM_TRIM_WIDTH=3)</p> <p>For Synopsys ROMs the bits are defined as follows: [3:0] RM: Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = '0' is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to '0'. [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external pin Read-Write margin setting. Recommended default value for LP: RME=1, RM=2 (ROM_TRIM_DEFAULT=0x0000_0012, ROM_TRIM_WIDTH=5) Recommended default value for ULP: RME=1, RM=3 (ROM_TRIM_DEFAULT=0x0000_0013, ROM_TRIM_WIDTH=5)</p> |

5.1.53 CPUSS_TRIM_RAM_CTL

Description: RAM trim control
Address: 0x40202104
Offset: 0x2104
Retention: Retained
IsDeepSleep: No
Comment: This register is used to trim ALL RAM memories in the device. Different operating Voltages may require different trim settings.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | TRIM [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | TRIM [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TRIM [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TRIM [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|------------------|--|
| 0:31 | TRIM | RW | R | RAM_TRIM_DEFAULT | <p>For ARM RAMs the bits are defined as follows</p> <p>[2:0] EMA: Extra Margin Adjustment (0 is the fastest setting)</p> <p>[4:3] EMAW: Extra Margin Adjustment for Writes (0 is the fastest setting)</p> <p>[7:5] CTL_BIAS: Control the bias circuit in the SRAM power switches for SRAMC0: 0=OFF, 7=max Recommended default value: CTL_BIAS=3, EMAW=0, EMA=2 (RAM_TRIM_DEFAULT=0x0000_0062, RAM_TRIM_WIDTH=8)</p> <p>For Synopsys RAMs the bits are defined as follows:</p> <p>[3:0] Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness.</p> <p>- RM[1:0] values control access time and cycle time of the memory. RM[1:0] = '0' is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation.</p> <p>- RM[3:2] are factory pins reserved for debug mode and should be set to '0'.</p> <p>[4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external RM[3:0] Read-Write margin setting.</p> <p>[7:5] WPULSE: Write Assist Pulse to control pulse width of negative voltage on SRAM bitline.</p> <p>[9:8] RA: Read Assist control for WL under-drive.</p> <p>[14:12] WA: Write assist enable control (Active High).</p> <p>- WA[2:0] Write Assist pins to control negative voltage on SRAM bitline.</p> <p>Recommended default value for LP: WA=4, RA=0, WPULSE=0, RME=1, RM=3 (RAM_TRIM_DEFAULT=0x0000_4013, RAM_TRIM_WIDTH=15)</p> <p>Recommended default value for ULP: WA=6, RA=0, WPULSE=0, RME=1, RM=2 (RAM_TRIM_DEFAULT=0x0000_6012, RAM_TRIM_WIDTH=15)</p> |

5.1.54 CPUSS_CM0_SYSTEM_INT_CTL

Description: CM0+ system interrupt control
Address: 0x40208000
Offset: 0x8000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|--------------|----|----|----|-------------------|----|----|
| Name | None [7:3] | | | | | CPU_INT_IDX [2:0] | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CPU_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:2 | CPU_INT_IDX | RW | R | Undefined | <p>CPU interrupt index (legal range [0, 7]). This field specifies to which CPU interrupt the system interrupt is mapped. E.g., if CPU_INT_IDX is '6', the system interrupt is mapped to CPU interrupt '6'.</p> <p>Note: it is possible to map multiple system interrupts to the same CPU interrupt. It is advised to assign different priorities to the CPU interrupts and to assign system interrupts to CPU interrupts accordingly.</p> |
| 31 | CPU_INT_VALID | RW | R | 0 | <p>Interrupt enable: '0': Disabled. The system interrupt will NOT be mapped to any CPU interrupt. '1': Enabled. The system interrupt is mapped on CPU interrupt CPU_INT_IDX.</p> <p>Note: the CPUs have dedicated XXX_SYSTEM_INT_CTL registers. In other words, the CPUs can use different CPU interrupts for the same system interrupt. However, typically only one of the CPUs will have the ENABLED field of a specific system interrupt set to '1'.</p> |

5.1.55 CPUSS_CM4_SYSTEM_INT_CTL

Description: CM4 system interrupt control
Address: 0x4020A000
Offset: 0xA000
Retention: Retained
IsDeepSleep: No
Comment: Only present when SYSTEM_IRQ_PRESENT is '1'
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-------------------|---|---|
| Name | None [7:3] | | | | | CPU_INT_IDX [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------------|--------------|----|----|----|----|----|----|
| Name | CPU_INT_VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|-------------|
| 0:2 | CPU_INT_IDX | RW | R | Undefined | N/A |
| 31 | CPU_INT_VALID | RW | R | 0 | N/A |

6 CRYPTO

Description Cryptography component
Base Address 0x40100000
Size 0x10000
Slave Num MMIO1 - 0

7 CXPI

Description CXPI
Base Address 0x40510000
Size 0x10000
Slave Num MMIO5 - 1

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---------------|
| CXPI0_ERROR_CTL | 0x40510000 | FULL | Error control |
| CXPI0_TEST_CTL | 0x40510004 | FULL | Test control |

7.1 CH 0

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| CXPI0_CH0_CTL0 | 0x40518000 | FULL | Control 0 |
| CXPI0_CH0_CTL1 | 0x40518004 | FULL | Control 1 |
| CXPI0_CH0_CTL2 | 0x40518008 | FULL | Control 2 |
| CXPI0_CH0_STATUS | 0x4051800C | FULL | Status |
| CXPI0_CH0_CMD | 0x40518010 | FULL | Command |
| CXPI0_CH0_TX_RX_STATUS | 0x40518040 | FULL | TX/RX status |
| CXPI0_CH0_TXPID_FI | 0x40518050 | FULL | TXPID and Frame Information |
| CXPI0_CH0_RXPID_FI | 0x40518054 | FULL | RXPID and Frame Information |
| CXPI0_CH0_CRC | 0x40518058 | FULL | CRC |
| CXPI0_CH0_TX_FIFO_CTL | 0x40518080 | FULL | TX FIFO control |
| CXPI0_CH0_TX_FIFO_STATUS | 0x40518084 | FULL | TX FIFO status |
| CXPI0_CH0_TX_FIFO_WR | 0x40518088 | FULL | TX FIFO write |
| CXPI0_CH0_RX_FIFO_CTL | 0x405180A0 | FULL | RX FIFO control |
| CXPI0_CH0_RX_FIFO_STATUS | 0x405180A4 | FULL | RX FIFO status |
| CXPI0_CH0_RX_FIFO_RD | 0x405180A8 | FULL | RX FIFO read |
| CXPI0_CH0_RX_FIFO_RD_SILENT | 0x405180AC | FULL | RX FIFO silent read |
| CXPI0_CH0_INTR | 0x405180C0 | FULL | Interrupt |
| CXPI0_CH0_INTR_SET | 0x405180C4 | FULL | Interrupt set |
| CXPI0_CH0_INTR_MASK | 0x405180C8 | FULL | Interrupt mask |
| CXPI0_CH0_INTR_MASKED | 0x405180CC | FULL | Interrupt masked |

7.2 CH 1

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| CXPI0_CH1_CTL0 | 0x40518100 | FULL | Control 0 |
| CXPI0_CH1_CTL1 | 0x40518104 | FULL | Control 1 |
| CXPI0_CH1_CTL2 | 0x40518108 | FULL | Control 2 |
| CXPI0_CH1_STATUS | 0x4051810C | FULL | Status |
| CXPI0_CH1_CMD | 0x40518110 | FULL | Command |
| CXPI0_CH1_TX_RX_STATUS | 0x40518140 | FULL | TX/RX status |
| CXPI0_CH1_TXPID_FI | 0x40518150 | FULL | TXPID and Frame Information |
| CXPI0_CH1_RXPID_FI | 0x40518154 | FULL | RXPID and Frame Information |
| CXPI0_CH1_CRC | 0x40518158 | FULL | CRC |
| CXPI0_CH1_TX_FIFO_CTL | 0x40518180 | FULL | TX FIFO control |
| CXPI0_CH1_TX_FIFO_STATUS | 0x40518184 | FULL | TX FIFO status |
| CXPI0_CH1_TX_FIFO_WR | 0x40518188 | FULL | TX FIFO write |
| CXPI0_CH1_RX_FIFO_CTL | 0x405181A0 | FULL | RX FIFO control |
| CXPI0_CH1_RX_FIFO_STATUS | 0x405181A4 | FULL | RX FIFO status |
| CXPI0_CH1_RX_FIFO_RD | 0x405181A8 | FULL | RX FIFO read |
| CXPI0_CH1_RX_FIFO_RD_SILENT | 0x405181AC | FULL | RX FIFO silent read |
| CXPI0_CH1_INTR | 0x405181C0 | FULL | Interrupt |
| CXPI0_CH1_INTR_SET | 0x405181C4 | FULL | Interrupt set |
| CXPI0_CH1_INTR_MASK | 0x405181C8 | FULL | Interrupt mask |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| CXPI0_CH1_INTR_MASKED | 0x405181CC | FULL | Interrupt masked |

7.3 CH 2

This instance is not available in the following part numbers:

CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE.

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------|
| CXPI0_CH2_CTL0 | 0x40518200 | FULL | Control 0 |
| CXPI0_CH2_CTL1 | 0x40518204 | FULL | Control 1 |
| CXPI0_CH2_CTL2 | 0x40518208 | FULL | Control 2 |
| CXPI0_CH2_STATUS | 0x4051820C | FULL | Status |
| CXPI0_CH2_CMD | 0x40518210 | FULL | Command |
| CXPI0_CH2_TX_RX_STATUS | 0x40518240 | FULL | TX/RX status |
| CXPI0_CH2_TXPID_FI | 0x40518250 | FULL | TXPID and Frame Information |
| CXPI0_CH2_RXPID_FI | 0x40518254 | FULL | RXPID and Frame Information |
| CXPI0_CH2_CRC | 0x40518258 | FULL | CRC |
| CXPI0_CH2_TX_FIFO_CTL | 0x40518280 | FULL | TX FIFO control |
| CXPI0_CH2_TX_FIFO_STATUS | 0x40518284 | FULL | TX FIFO status |
| CXPI0_CH2_TX_FIFO_WR | 0x40518288 | FULL | TX FIFO write |
| CXPI0_CH2_RX_FIFO_CTL | 0x405182A0 | FULL | RX FIFO control |
| CXPI0_CH2_RX_FIFO_STATUS | 0x405182A4 | FULL | RX FIFO status |
| CXPI0_CH2_RX_FIFO_RD | 0x405182A8 | FULL | RX FIFO read |
| CXPI0_CH2_RX_FIFO_RD_SILENT | 0x405182AC | FULL | RX FIFO silent read |
| CXPI0_CH2_INTR | 0x405182C0 | FULL | Interrupt |
| CXPI0_CH2_INTR_SET | 0x405182C4 | FULL | Interrupt set |
| CXPI0_CH2_INTR_MASK | 0x405182C8 | FULL | Interrupt mask |
| CXPI0_CH2_INTR_MASKED | 0x405182CC | FULL | Interrupt masked |

7.4 CH 3

This instance is not available in the following part numbers:

CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE, CYT2BL4BAS, CYT2BL4BAE, CYT2BL4CAS, CYT2BL4CAE, CYT2BL5BAS, CYT2BL5BAE, CYT2BL5CAS, CYT2BL5CAE, CYT2BL7BAS, CYT2BL7BAE, CYT2BL7CAS, CYT2BL7CAE, CYT2BL8BAS, CYT2BL8BAE, CYT2BL8CAS, CYT2BL8CAE.

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------|
| CXPI0_CH3_CTL0 | 0x40518300 | FULL | Control 0 |
| CXPI0_CH3_CTL1 | 0x40518304 | FULL | Control 1 |
| CXPI0_CH3_CTL2 | 0x40518308 | FULL | Control 2 |
| CXPI0_CH3_STATUS | 0x4051830C | FULL | Status |
| CXPI0_CH3_CMD | 0x40518310 | FULL | Command |
| CXPI0_CH3_TX_RX_STATUS | 0x40518340 | FULL | TX/RX status |
| CXPI0_CH3_TXPID_FI | 0x40518350 | FULL | TXPID and Frame Information |
| CXPI0_CH3_RXPID_FI | 0x40518354 | FULL | RXPID and Frame Information |
| CXPI0_CH3_CRC | 0x40518358 | FULL | CRC |
| CXPI0_CH3_TX_FIFO_CTL | 0x40518380 | FULL | TX FIFO control |
| CXPI0_CH3_TX_FIFO_STATUS | 0x40518384 | FULL | TX FIFO status |
| CXPI0_CH3_TX_FIFO_WR | 0x40518388 | FULL | TX FIFO write |
| CXPI0_CH3_RX_FIFO_CTL | 0x405183A0 | FULL | RX FIFO control |
| CXPI0_CH3_RX_FIFO_STATUS | 0x405183A4 | FULL | RX FIFO status |
| CXPI0_CH3_RX_FIFO_RD | 0x405183A8 | FULL | RX FIFO read |
| CXPI0_CH3_RX_FIFO_RD_SILENT | 0x405183AC | FULL | RX FIFO silent read |
| CXPI0_CH3_INTR | 0x405183C0 | FULL | Interrupt |
| CXPI0_CH3_INTR_SET | 0x405183C4 | FULL | Interrupt set |
| CXPI0_CH3_INTR_MASK | 0x405183C8 | FULL | Interrupt mask |
| CXPI0_CH3_INTR_MASKED | 0x405183CC | FULL | Interrupt masked |

7.5 Register Details

7.5.1 CXPI_ERROR_CTL

Description: Error control
Address: 0x40510000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register supports error functionality: it enables HW injected channel transmitter errors. The receiver should detect these errors and report these errors through activation of corresponding interrupt causes.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------|---|---|---|---|
| Name | None [7:5] | | | CH_IDX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|------------------------------|-----------------------------|----------------------|--------------|----|
| Name | None [23:21] | | | TX_DATA_LENGTH_ERROR [20:20] | TX_PID_PARITY_ERROR [19:19] | TX_CRC_ERROR [18:18] | None [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|----|----|----------------------------|--------------|
| Name | ENABLED [31:31] | None [30:26] | | | | | TX_DATA_STOP_ERROR [25:25] | None [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|---|
| 0:4 | CH_IDX | RW | R | 0 | Specifies the channel index of the channel to which HW injected channel transmitter errors applies. |
| 18 | TX_CRC_ERROR | RW | R | 0 | The crc field is inverted. At the receiver, this should result in INTR.RX_CRC_ERROR activation. |
| 19 | TX_PID_PARITY_ERROR | RW | R | 0 | In cspi mode, the PID parity bit P[1] is inverted from $!(ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[1])$ to $(ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[1])$. At the receiver, this should result in INTR.RX_HEADER_PARITY_ERROR activation. |
| 20 | TX_DATA_LENGTH_ERROR | RW | R | 0 | The transmitter continues to send logical '0' (during IFS) after CRC field is transmitted. At the receiver, this should result in INTR.RX_DATA_LENGTH_ERROR activation. At the transmitter, this should result in INTR.TX_DATA_LENGTH_ERROR activation. |
| 25 | TX_DATA_STOP_ERROR | RW | R | 0 | The data field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_FRAME_ERROR activation. At the transmitter, this should result in INTR.TX_FRAME_ERROR activation. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 31 | ENABLED | RW | R | 0 | Error injection enable: '0': Disabled. '1': Enabled. |

7.5.2 CXPL_TEST_CTL

Description: Test control
Address: 0x40510004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register support test functionality.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------|---|---|---|---|
| Name | None [7:5] | | | CH_IDX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|--------------|
| Name | None [23:17] | | | | | | | MODE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:4 | CH_IDX | RW | R | 0 | <p>Specifies the channel index of the channel to which test applies. The channel IO signals of channel indices CH_IDX and CH_NR-1 are connected as specified by MODE. CH_IDX should be in the range [0, CH_NR-2], as channel index CH_NR-1 is always involved in test and cannot be connected to itself. The test mode allows BOTH of the two connected channels to be tested.</p> <p>Note: this testing functionality simplifies SW development, but may also be used in the field to verify correct channel functionality.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|----|----|-----------------|---|
| 16 | MODE | RW | R | 0 | <p>Test mode:</p> <p>'0': Partial disconnect from IOSS. This mode's isolation allows for device test without relying on an external cspi transceiver. The IOSS 'tx' IO cell can be used to observe messages outside of the device.</p> <ul style="list-style-type: none"> - tx_in[CH_IDX] = IOSS cspi_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS cspi_tx_in[CH_IDX]. - rx_in[CH_IDX] = IOSS cspi_tx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS cspi_tx_in[CH_IDX]. - cspi_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - cspi_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. <p>'1': Full disconnect from IOSS (the IOSS/HSIOM should disconnect 'tx_out' from the 'tx' IO cell). This mode's isolation allows for device test without effecting an operational cspi cluster.</p> <ul style="list-style-type: none"> - tx_in[CH_IDX] = cspi_tx_out[CH_IDX]. - tx_in[CH_NR-1] = cspi_tx_out[CH_IDX]. - rx_in[CH_IDX] = cspi_tx_out[CH_IDX]. - rx_in[CH_NR-1] = cspi_tx_out[CH_IDX]. - cspi_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - cspi_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. |
| | PARTIAL_DISCONNECT | | | 0 | Partial disconnect |
| | FULL_DISCONNECT | | | 1 | Full disconnect |
| 31 | ENABLED | RW | R | 0 | <p>Test enable:</p> <p>'0': Disabled. Functional mode.</p> <ul style="list-style-type: none"> - tx_in[CH_IDX] = IOSS cspi_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS cspi_tx_in[CH_NR-1]. - rx_in[CH_IDX] = IOSS cspi_rx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS cspi_rx_in[CH_NR-1]. - cspi_tx_out[CH_IDX] = tx_out[CH_IDX]. - cspi_tx_out[CH_NR-1] = tx_out[CH_NR-1]. <p>'1': Enabled. Test mode, specific test mode is specified by MODE.</p> |
| | FUNCTIONAL_MODE | | | 0 | Functional mode |
| | TEST_MODE | | | 1 | Test mode |

7.5.3 CH

7.5.3.1 CXPI_CH_CTL0

Description: Control 0

Address: 0x40518000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: This register contains controls for CXPI such as modes, offset, or master/slave.
This register is programmed before the start of a transaction and not to be change inflight of any transaction. It can only be change during CXPI controller is quiescent.

Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|----------------|--------------|---------------|--------------------------|--------------|----|-----------------|
| Name | RXPIDZERO_CHECK_EN [7:7] | None [6:5] | | AUTO_EN [4:4] | None [3:1] | | | MODE [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:9] | | | | | | | FILTER_EN [8:8] |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | IFS [20:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | MASTER [30:30] | None [29:28] | | BIT_ERROR_IGNORE [27:27] | None [26:25] | | IBS [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|----|----|-----------------|---|
| 0 | MODE | RW | R | 0 | Mode of operation: '0': NRZ mode. '1': PWM mode. |
| | NRZ | | | 0 | NRZ mode |
| | PWM | | | 1 | PWM mode |
| 4 | AUTO_EN | RW | R | 1 | CXPI transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW. |
| 7 | RXPIDZERO_CHECK_EN | RW | R | 0 | Receive PID Zero Check Enable. 0 - No action if received PID[6:0] = 0 and PID[7]=1'b1. 1 - If received PID[6:0] = 0 and PID[7]=1'b1, HW (slave) does not clear CMD.RX_HEADER and will anticipate receiving header again (CMD.TX_HEADER=0). If CMD.TX_HEADER=1 in the same scenario, then HW (slave) clears CMD.RX_HEADER upon receiving the header follow by transmit PID. This mode is useful for case where polling method is used and CXPI controller is configured as slave. This would reduce dependency on SW to react to the header received within IBS=1. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 8 | FILTER_EN | RW | R | 0 | <p>RX filter enable (for 'cxpi_rx_in')</p> <p>'0': No filter</p> <p>'1': Median 3 (default value) operates on the last three 'cxpi_rx_in' values. The sequences '000', '001', '010', and '100' result in a filtered value '0'. The sequences '111', '110', '101', and '011' result in a filtered value '1'.</p> |
| 16:20 | IFS | RW | R | 0 | <p>Inter Frame Space in bit periods:</p> <p>'0' Invalid.</p> <p>...</p> <p>'10': 10 bit periods</p> <p>...</p> <p>'31': 31 bit periods</p> <p>Values of <10 are not allowed.</p> <p>This field is used for transmission/reception for adding waiting inter frame space.</p> <p>Note that after a valid transaction (after CRC), HW waits for 10 bits as EOF. Hence, by setting CTL0.IFS=0xA means that HW will wait for 10bits before transmitting a new transaction (not including the EOF).</p> <p>Note: 0 is not allowed when IFS_WAIT=1. SW needs to ensure it has program valid values before it can set IFS_WAIT=1.</p> <p>If IFS_WAIT=1 after timeout occurs, the value of CTL0.IFS would need to consider the timeout count i.e. (IFS needed - CTL2.TIMEOUT_LENGTH-1) to get the total idle time. For example if TIMEOUT_LENGTH=9 and IFS needed is 20, then CTL0.IFS is set to 10.</p> |
| 21:24 | IBS | RW | R | 0 | <p>Inter Byte Space in bit periods:</p> <p>'0' No offset.</p> <p>'1' 1 IBS is inserted per every byte frame.</p> <p>...</p> <p>'9' 9 IBS are inserted per every byte frame.</p> <p>Values >9 are invalid per spec.</p> <p>This field is used to control number of IBS after every byte frame when transmitting message frame.</p> <p>Note that this field is the minimum IBS inserted for every byte frame as the SW may require some time to prepare the response when it receives the PID.</p> <p>When receiving, this field is ignored with the exception of receiving header and transmitting response. For receiving header and transmitting response, SW can enable IBS insertion by setting TIMEOUT_SEL=1/2 prior to setting CMD.RX_HEADER=1 and CMD.RX_RESPONSE=1. If the received header corresponds to transmit response, SW clears CMD.RX_RESPONSE =0 and sets TX FIFO and CMD.TX_RESPONSE=1. HW waits for minimum IBS before transmit response (if timeout has not occurred yet). It is prohibit to program IBS>TIMEOUT_LENGTH.</p> <p>This field should not be changed during inflight transaction including EOF.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 27 | BIT_ERROR_IGNORE | RW | R | 0 | Specifies behavior on a detected bit error during header or response transmission: '0': Message transfer is aborted. '1': Message transfer is NOT aborted. Note: This field does NOT effect the reporting of the bit error through INTR/STATUS.TX_BIT_ERROR; i.e. bit errors are always reported. Note: This field must not be set to '1' when it is NRZ mode. This is due to delay in transceiver will cause the transmitter behavior undefined when error occurs. |
| | ABORT_TX_MSG | | | 0 | Message transfer is aborted |
| | CONT_TX_MSG | | | 1 | Message transfer is NOT aborted |
| 30 | MASTER | RW | R | 0 | CXPI master mode. '0': Indicates CXPI as slave node. '1': Indicates CXPI as master node. This bit is only valid if ENABLED=1. SW needs to set only 1 node as master within the same CXPI cluster. SW needs to set this bit either at the same time as ENABLED or before ENABLED is set. If SW needs to change the controller to different mode, it needs to make sure that HW is quiescent before doing so. |
| | SLAVE_MODE | | | 0 | Slave mode |
| | MASTER_MODE | | | 1 | Master mode |
| 31 | ENABLED | RW | R | 0 | Channel enable: '0': Disabled. If a channel is disabled, CMD, STATUS, INTR MMIO registers will have their fields reset to their default value. '1': Enabled. |
| | DISABLED | | | 0 | Disabled |
| | ENABLED | | | 1 | Enabled |

7.5.3.2 CXPI_CH_CTL1

Description: Control 1

Address: 0x40518004

Offset: 0x4

Retention: Retained

IsDeepSleep: No

Comment: This register contains controls on configuring different timing controls at Data link layer.
This register is programmed before the start of a transaction and not to be change inflight of any transaction. It can only be change during CXPI controller is quiescent.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|------------------|--------------|----------------|-------------|----|----|--------------|
| Name | T_LOW1 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | | | | | None [11:9] | | | T_LOW1 [8:8] |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | | | None [21:21] | T_LOW0 [20:16] | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:31] | T_OFFSET [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|--|
| 0:8 | T_LOW1 | RW | R | 0 | Low count for logic 1. This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '1'. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks. .. 399: means 400 clocks. Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that this field is used for TX. |
| 12:20 | T_LOW0 | RW | R | 0 | Low count for logic 0. This is valid only for PWM mode. The count value here indicates the number of clocks per clk_cxpi_ch to drive a '0' at CXPI bus before releasing it to indicate a logical '0'. 0: means 1 clock. 1: means 2 clocks .. 15: means 16 clocks .. 399: means 400 clocks Any value above 399 is invalid. Note that for NRZ mode, this field is ignored. Note that this field is used for TX. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 22:30 | T_OFFSET | RW | R | 0 | <p>The value of offset that is used for sampling the 'rx'. The value of this counter is used in HW as below.</p> <ul style="list-style-type: none"> - 0 : means 1 clock after detecting falling edge of 'rx' - 1 : means 2 clocks after detecting falling edge of 'rx' .. - 7 : means 8 clocks after detecting falling edge of 'rx' .. - 15 : means 16 clocks after detecting falling edge of 'rx' .. - 399 : means 400 clocks after detecting falling edge of 'rx' <p>Any value above 399 is invalid.</p> |

7.5.3.3 CXPI_CH_CTL2

Description: Control 2
Address: 0x40518008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: This register contains fields for number of retries.
These registers are programmed before the start of a transaction and not to be change inflight of any transaction. It can only be change during CXPI controller is quiescent.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|------------------------|----|------------------------|----|-------------|----|
| Name | None [7:2] | | | | | | RETRY [1:0] | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:14] | | T_WAKEUP_LENGTH [13:8] | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | TIMEOUT_LENGTH [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TIMEOUT_SEL [31:30] | | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 0:1 | RETRY | RW | R | 0 | Number of retries after arbitration lost. '0': No retries. .. '3': 3 retries. HW will immediately retry after arbitration lost i.e. after the message frame that won the arbitration is complete and fulfilled IFS. If SW wants to manage the retransmission then SW can program RETRY =0. In this case, HW will not retry after arbitration lost and will set TX_HEADER_ARB_LOST bit. SW needs to trigger HW to resend by programming the CMD fields again. |
| 8:13 | T_WAKEUP_LENGTH | RW | R | 0 | Specifies the wake up pulse low period in Tbits that is transmitted during Standby mode. '0': 1 bit period '1': 2 bit period .. '49': 50 bit period Any value above 49 is invalid. This field is only valid if TX_WAKE_PULSE is set to 1. |
| 16:19 | TIMEOUT_LENGTH | RW | R | 0 | Timeout Length (in Tbits). Specifies the number of Tbits to exceed timeout between frame bytes within a message frame. CXPI spec states that the maximum allowed inter byte space (IBS) is 9Tbits. This field is valid only when TIMEOUT_SEL=1/2. '0' - 1Tbit '1' - 2Tbits .. '9' - 10Tbits Values >9 is invalid per CXPI spec. Note for NRZ mode, although there are propagation delay from transceiver to CXPI controller, the delay is cancelled out as the timeout is compared on the RX (for transmit case, HW waits for the feedback on RX). |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------------------|----|----|-----------------|--|
| 30:31 | TIMEOUT_SEL | RW | R | 0 | <p>Timeout Select.</p> <p>'0' - Timeout check is disabled. HW clears timeout counter.</p> <p>'1' - Timeout check is enabled and HW will refer to TIMEOUT_LENGTH as number of Tbits allowed between header and response.</p> <p>'2' - Timeout check is enabled to check header-header, header-response, and header-header-response within a message frame to be space within TIMEOUT_LENGTH bit time.</p> <p>'3' - invalid</p> <p>For '1', HW will restart/start timeout counter after transmitting/receiving header. HW will hold the counter if timeout until the next header is transmitted or received. Timeout will cause HW to stop transmission of the current message frame together with interrupt to SW. For receive, HW abort reception of the frame if timeout occurs while waiting for receiving response and notify SW with interrupt.</p> <p>For '2', HW will re-start/start timeout counter after receiving any frame bytes within a message frame. HW will hold the counter if timeout until the IFS. Timeout will cause HW to stop transmission of the current message frame and notify SW with interrupt. For receive, HW will abort reception of the message frame if timeout occurs while waiting for receiving response and notify SW with interrupt.</p> <p>For all cases, HW stops counting when it is out of a message frame such as IFS or CXPI bus IDLE. If the timeout counter > TIMEOUT_LENGTH, then it will set the INTR.TIMEOUT=1.</p> <p>Note that, TIMEOUT_SEL=1/2 also enables the count for IBS between receive header and transmit response on top of timeout check.</p> |
| | TIMEOUT_DISABLED | | | 0 | Timeout check is disabled. |
| | TIMEOUT_CHECK_BTW_HDR_RSP | | | 1 | Timeout check is enabled and HW will refer to TIMEOUT_LENGTH as number of Tbits allowed between header and response. |
| | TIMEOUT_CHECK_BTW_HDR_HDR_RSP | | | 2 | Timeout check is enabled to check header-header, header-response, and header-header-response within a message frame to be space within TIMEOUT_LENGTH bit time. |

7.5.3.4 CXPI_CH_STATUS

Description: Status
Address: 0x4051800C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

Default: This is a non-retained register; setting CTL0.ENABLED to '0' clears all status fields to '0'.
0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------------|------------|---|---------------------|---|
| Name | None [7:5] | | | HEADER_RESPONSE [4:4] | None [3:2] | | RETRIES_COUNT [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|-----------------|-----------------|--------------|----|---------------|---------------|
| Name | None [15:14] | | RX_DONE [13:13] | TX_DONE [12:12] | None [11:10] | | RX_BUSY [9:9] | TX_BUSY [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------------------|--------------------------------|----------------------|----------------------|----------------------------|-----------------|--------------|----|
| Name | RX_DATA_LENGTH_ERROR [23:23] | RX_HEADER_PARITY_ERROR [22:22] | RX_CRC_ERROR [21:21] | TX_BIT_ERROR [20:20] | TX_HEADER_ARB_LOST [19:19] | TIMEOUT [18:18] | None [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|------------------------|------------------------|----------------------------|----------------------------|---------------------------|---------------------------|------------------------------|
| Name | None [31:31] | TX_FRAME_ERROR [30:30] | RX_FRAME_ERROR [29:29] | TX_UNDERFLOW_ERROR [28:28] | RX_UNDERFLOW_ERROR [27:27] | TX_OVERFLOW_ERROR [26:26] | RX_OVERFLOW_ERROR [25:25] | TX_DATA_LENGTH_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|---|
| 0:1 | RETRIES_COUNT | R | W | 0 | Retries count. The value reflects the number of retries that HW tries to transmit a header/response. HW will reset counter (either case below): 1. after successfully transmit the retry attempt 2. SW clears the CMD.TX_HEADER='0' 3. HW clearing CMD.TX_HEADER=0 due to errors (TX_BIT_ERROR, TX_HEADER_ARB_LOST, TX_OVERFLOW_ERROR, TX_UNDERFLOW_ERROR, TX_DATA_LENGTH_ERROR, and TX_FRAME_ERROR) |
| 4 | HEADER_RESPONSE | R | W | 0 | Frame header/response identifier (only valid when TX_BUSY or RX_BUSY is '1') '0' - Frame header being transferred. '1' - Frame response being transferred. |
| 8 | TX_BUSY | R | W | 0 | Transmitter busy. - Set to '1' on the start of the following commands: TX_HEADER, TX_RESPONSE. - Set to '0' on successful completion of previous commands or when an error is detected. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|----|----|-----------------|---|
| 9 | RX_BUSY | R | W | 0 | Receiver busy. - Set to '1' on the start of the following commands: RX_HEADER, RX_RESPONSE. - Set to '0' on successful completion of previous commands or when an error is detected. |
| 12 | TX_DONE | R | W | 0 | Transmitter done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences: - TX_HEADER. - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE. |
| 13 | RX_DONE | R | W | 0 | Receiver done: - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences: - RX_HEADER, RX_RESPONSE. - TX_HEADER, RX_RESPONSE. |
| 18 | TIMEOUT | R | W | 0 | Copy of INTR.TIMEOUT |
| 19 | TX_HEADER_ARB_LOST | R | W | 0 | Copy of INTR.TX_HEADER_ARB_LOST |
| 20 | TX_BIT_ERROR | R | W | 0 | Copy of INTR.TX_BIT_ERROR. |
| 21 | RX_CRC_ERROR | R | W | 0 | Copy of INTR.RX_CRC_ERROR. |
| 22 | RX_HEADER_PARITY_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_PARITY_ERROR. |
| 23 | RX_DATA_LENGTH_ERROR | R | W | 0 | Copy of INTR.RX_DATA_LENGTH_ERROR. |
| 24 | TX_DATA_LENGTH_ERROR | R | W | 0 | Copy of INTR.TX_DATA_LENGTH_ERROR. |
| 25 | RX_OVERFLOW_ERROR | R | W | 0 | Copy of INTR.RX_OVERFLOW_ERROR. |
| 26 | TX_OVERFLOW_ERROR | R | W | 0 | Copy of INTR.TX_OVERFLOW_ERROR. |
| 27 | RX_UNDERFLOW_ERROR | R | W | 0 | Copy of INTR.RX_UNDERFLOW_ERROR. |
| 28 | TX_UNDERFLOW_ERROR | R | W | 0 | Copy of INTR.TX_UNDERFLOW_ERROR. |
| 29 | RX_FRAME_ERROR | R | W | 0 | Copy of INTR.RX_FRAME_ERROR. |
| 30 | TX_FRAME_ERROR | R | W | 0 | Copy of INTR.TX_FRAME_ERROR. |

7.5.3.5 CXPI_CH_CMD

Description: Command
Address: 0x40518010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The register fields are retained. When a CXPI channel is disabled (CTL0.ENABLED is set to '0'), HW sets all the register fields to '0'.

The following restrictions apply when programming the commands:

- If both TX_HEADER and RX_HEADER are set to 1'b1 together with both IFS_WAIT and RXPIDZERO_CHECK_EN set to 1'b0, TX_HEADER will have higher precedence.
- If TX_HEADER, RX_HEADER, and (IFS_WAIT or RXPIDZERO_CHECK_EN) are all set together, RX_HEADER will have higher priority.
- TX_RESPONSE and RX_RESPONSE are NOT mutually exclusive, but are evaluated in the following order (of decreasing priority): TX_RESPONSE, RX_RESPONSE.
- During normal mode the CMDs below are allowed
RX_HEADER, IFS_WAIT, TX_HEADER, TX_RESPONSE, RX_RESPONSE, SLEEP (Higher priority -> lower priority if all are set at the same time).
Note that after executing TX_HEADER, TX_RESPONSE would be higher priority compare to RX_RESPONSE.
- Note that after executing RX_HEADER or after arbitration loss while attempting to execute TX_HEADER, RX_RESPONSE would be higher priority compare to TX_RESPONSE.
- During Standby mode the CMDs below are allowed
SLEEP, WAKE_TO_STANDBY, TX_WAKE_PULSE (Higher priority -> lower priority). Note that WAKE_TO_STANDBY and TX_WAKE_PULSE does not have conflict in priority.
- During Sleep mode the CMDs below are allowed
WAKE_TO_STANDBY.

The use case for the combination commands to transmit/receive message frames are as below:

TX_HEADER, RX_HEADER, RX_RESPONSE, WAIT_IFS: for master/slave in event trigger that is performing transmit PID and follow by receiving response. For master in polling that is performing transmit PTYPE and receive PID follow by receiving/transmitting response. For transmitting response, SW needs to clear RX_RESPONSE and set TX_RESPONSE after decoding PID. For master in polling that is performing transmit PID follow by receive response. TX_HEADER, RX_HEADER, TX_RESPONSE, RX_RESPONSE, WAIT_IFS: for master/slave in event trigger that is performing transmit PID and follow by transmit response. For master in polling that is transmitting PID and transmit response.

RX_HEADER, RX_RESPONSE: For master/slave in event trigger that is receiving PID. This would be use for both transmit response and receive response since SW needs to decode the PID first before initiating transmit response.

RX_HEADER, RX_RESPONSE, CTL0.RXPIDZERO_CHECK_EN: For slave in polling mode to receive PTYPE and PID. Both transmit and receive response will use this combination as SW needs to decode the PID first before initiating transmit response.

TX_HEADER, RX_HEADER, RX_RESPONSE, CTL0.RXPIDZERO_CHECK_EN: For slave in polling mode to receive PTYPE and transmit PID and receive response.

TX_HEADER, RX_HEADER, TX_RESPONSE, RX_RESPONSE, CTL0.RXPIDZERO_CHECK_EN: For slave in polling mode to receive PTYPE and transmit PID and transmit response.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----|----------------|---------------------|-----------------------|-------------|-------------------|-----------------|
| Name | None [7:6] | | IFS_WAIT [5:5] | TX_WAKE_PULSE [4:4] | WAKE_TO_STANDBY [3:3] | SLEEP [2:2] | TX_RESPONSE [1:1] | TX_HEADER [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |

| | | | | | | | | |
|-------------|--------------|--|--|--|--|--|---------------------------|------------------------|
| Name | None [15:10] | | | | | | RX _RESPON SE [9:9] | RX _HEADER [8:8] |
|-------------|--------------|--|--|--|--|--|---------------------------|------------------------|

| | | | | | | | | |
|-------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |

| | | | | | | | | |
|-------------|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|------|-----------------|---|
| 0 | TX_HEADER | RW | RW | 0 | <p>SW sets this field to '1' to transmit a header. HW sets this field to '0' on successful completion of ANY of the following legal command sequences (also set to '0' when an error (such as bit error if bit_ignore=0, arbitration loss, tx data length error. For timeout please refer to SAS) is detected):</p> <ul style="list-style-type: none"> - TX_HEADER - TX_HEADER, TX_RESPONSE. - TX_HEADER, RX_RESPONSE. <p>The above is for transmission of PID without prior transmission of PTYPE.</p> <p>The header is transmitted when the PID field STOP bits are transmitted (INTR.TX_HEADER_DONE).</p> <p>HW sets this field to '1', when the 'tr_cmd_tx_header' input trigger is activated. This allows for time triggered CXPI message transfer. HW driven time triggered transfer eliminates the jitter that is typically associated with SW driven transfer.</p> <p>SW clears this field to '0', when it wants to cancel a pending request. Note that if SW clears this field to '0' while HW is already in the middle of the request, then the cancel will be ignored. The cancel request can happen when HW is pending a retry when it is still servicing the current transaction. Or the cancel request can occur when HW is checking IFS/bus idle-ness. Note that if PTYPE (TX_HEADER) is transmitted follow by receive response (RX_RESPONSE) or no response, HW clears TX_HEADER right after transmitting PTYPE.</p> |
| 1 | TX_RESPONSE | RW | RW1C | 0 | <p>SW sets this field to '1' to transmit a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected).</p> <ul style="list-style-type: none"> - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE. <p>SW can also clear this field to '0' if SW wants to cancel the TX_RESPONSE.</p> <p>The response is transmitted when the CRC are transmitted (INTR.TX_RESPONSE_DONE).</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|------|------|-----------------|--|
| 2 | SLEEP | RW1S | RW1C | 0 | <p>SW sets this field to '1' to direct HW to sleep mode. HW transits from Normal to Sleep upon SLEEP=1 and both TX and RX is idle. HW sets this field to '0' when it is in Sleep mode.</p> <p>Note that, SW needs to manage the entry to sleep mode by checking the conditions are met before initiating sleep mode e.g. all slave nodes supports sleep and on transmitting sleep frames to indicate sleep to all slave nodes. SW shall not program SLEEP=1 when HW is executing TX_WAKEUP_PULSE command. If SW programs SLEEP=1 during HW executing TX_WAKEUP_PULSE command, it will cause HW to abruptly stop transmitting wakeup pulse as below:</p> <ol style="list-style-type: none"> 1. HW not clearing TX_WAKEUP_PULSE 2. HW not setting TX_WAKEUP_DONE 3. HW outputting TX_OUT=0. |
| 3 | WAKE_TO_STANDBY | RW | RW1C | 0 | <p>SW sets this field to '1' to direct HW to wake up from Sleep mode to Standby mode. SW clears this field to '0' from '1' when it wants to direct HW from Standby to Normal mode. HW clears this field to '0' when it is in Normal mode or back to Sleep mode from Standby mode.</p> <p>For the case of CXPI master mode, HW will move its power mode from Sleep->Standby when this field is set to '1'. When SW clears this field is from '1' to '0' in Standby mode, HW will move to Normal mode while HW starts transmitting clock. To transmit wake pulse, SW need to program TX_WAKE_PULSE accordingly in Standby mode before entering Normal.</p> <p>For the case of CXPI slave mode and PWM mode, HW will move power mode from Sleep->Standby when this field is set to '1'. HW will wait for detection of clock before moving from Standby->Normal. SW clearing this field to '0' will have no effect.</p> <p>For the case of CXPI slave mode and NRZ mode, HW will move power mode from Sleep->Standby when this field is set to '1'. HW needs to be directed by SW by clearing this field to '0' to move from Standby->Normal after SW has detected clock through another IP (e.g. MXTCPWM).</p> |
| 4 | TX_WAKE_PULSE | RW | RW1C | 0 | <p>SW sets this field to '1' to direct HW to send wake up pulse. HW will transmit wake up pulse in Standby state only. HW will ignore this field when it's not in Standby state.</p> <p>'1' - HW will drive CXPI bus to low for period dictated by T_WAKEUP_LENGTH.</p> <p>'0':- No wake up pulse</p> <p>HW clears this field to '0' after it transmit the pulse per T_WAKEUP_LENGTH.</p> <p>For the case where more than 1 wake pulses are required, SW is expected to set this field to '1' again (after this field is cleared to '0') per the number of times the wake pulse is required.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|------|-----------------|---|
| 5 | IFS_WAIT | RW | RW1C | 0 | <p>SW sets this field to '1' to wait for IFS. HW clears this field to '0' after it detects logical '1' based on IFS.</p> <p>HW will keep this field to '1' if it detects logical '0' before fulfilling the number of logical '1' required.</p> <p>The intention of this bit is to provide capability for SW to direct HW to check bus idle-ness before transmitting. Without setting this bit before directing HW to send header, HW will not check bus idle before transmitting. Besides that, this bit will also provide SW an option to configure HW to wait for IFS before sending again PTYPE or PID to fulfill IFS if there is no response from other nodes. Note: SW needs to configure valid IFS values before setting IFS_WAIT=1.</p> |
| 8 | RX_HEADER | RW | RW1C | 0 | <p>SW sets this field to '1' to receive a header. HW sets this field to '0' on successful completion of the ANY of the legal command sequences. (Not set to '0' when an error is detected).</p> <p>-RX_HEADER -RX_HEADER, TX_RESPONSE -RX_HEADER, RX_RESPONSE</p> <p>The above applies for cases of receiving PID without prior receiving PTYPE. The header is received when the PID field STOP bits are received (INTR.RX_HEADER_PID_DONE and INTR.RX_HEADER_DONE).</p> <p>Typically, a slave node SW sets both RX_HEADER and RX_RESPONSE to '1', anticipating a transfer of a response from the master node to this slave node. After receipt of the header PID/PTYPE field (INTR.RX_HEADER_PID_DONE is activated), the slave node may decide to set TX_RESPONSE to '1' (which has lower priority than RX_RESPONSE hence RX_RESPONSE need to be clear to '0' by SW) to transmit a response. Note that, for cases with RXPIDZERO_CHECK_EN=1 for slave in polling mode, RX_HEADER is cleared upon receiving PTYPE if the next course of action is to transmit PID. If the next course of action is to receive PID, then the RX_HEADER is cleared upon completion of response.</p> |
| 9 | RX_RESPONSE | RW | RW1C | 0 | <p>SW sets this field to '1' to receive a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (NOT set to '0' when an error is detected).</p> <p>-TX_HEADER, RX_RESPONSE -RX_HEADER, RX_RESPONSE</p> <p>SW can set this field to '1' to be conservative on receiving response i.e. IBS=0 whenever it is receiving PID. If the PID corresponds to transmit response, the SW can then clear this field to '0' and set TX_RESPONSE=1 to direct HW to send response.</p> <p>The response is received after CRC are received (INTR.RX_RESPONSE_DONE).</p> |

7.5.3.6 CXPI_CH_TX_RX_STATUS

Description: TX/RX status
Address: 0x40518040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x5000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|---------------|---------------|
| Name | None [23:18] | | | | | | RX_IN [17:17] | TX_IN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----------------|--------------|----------------|
| Name | None [31:27] | | | | | EN_OUT [26:26] | None [25:25] | TX_OUT [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 16 | TX_IN | R | W | Undefined | CXPI transmitter input ('tx_in', 'cxpi_tx_in' in functional mode). TX_IN and RX_IN can be used to determine a wakeup source. Note that wakeup source detection relies on the external transceiver functionality. |
| 17 | RX_IN | R | W | Undefined | CXPI receiver input ('rx_in', 'cxpi_rx_in' in functional mode). |
| 24 | TX_OUT | R | W | 1 | CXPI transmitter output ('tx_out', 'cxpi_tx_out'). |
| 26 | EN_OUT | RW | RW | 1 | <p>CXPI transceiver enable ('en_out', 'cxpi_en_out'). This field controls the enable (or low active sleep enable) of the external transceiver:</p> <p>'0': Disabled.</p> <p>'1': Enabled.</p> <p>If CTL0.AUTO_EN is '0', SW controls this field to enable the external transceiver. If CTL0.AUTO_EN is '1', HW controls this field to enable the external transceiver:</p> <p>- HW sets this field to '1' when it is out of Sleep state. If it moves to Sleep state, HW will clear this field to '0'.</p> |

7.5.3.7 CXPI_CH_TXPID_FI

Description: TXPID and Frame Information
Address: 0x40518050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: This registers holds information on TX's PID, FI and DLCEXT
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | PID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | FI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DLCEXT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|---|
| 0:7 | PID | RW | R | Undefined | <p>Header protected identifier (PID).</p> <ul style="list-style-type: none"> - Bits 6 down to 0: frame identifier ID[6:0]. - Bits 7: is odd parity bit. - $PID[7] = ! (ID[6] \wedge ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[2] \wedge ID[1] \wedge ID[0])$ <p>Software does not need to program the parity bit i.e. bit[7]. HW will calculate the odd parity bit and ignore the bit[7] if SW occupies this bit.</p> <p>Transmission: To be transmitted PID field. HW will ignore bit[7] and compute the parity bit based on bits[6:0]</p> <p>Note that, this field can be use by SW to send PType byte as the HW handles both PID and PType the same way. The frame type would occupy bit[6:0] and the odd parity will be calculated by the HW.</p> |
| 8:15 | FI | RW | R | Undefined | <p>Frame Information.</p> <p>This is the byte that will be transmitted as Frame Information. Per CXPI spec,</p> <ul style="list-style-type: none"> FI[7:4] denotes the data length count (DLC). FI[3:2] denotes Network Management. Bit[3] - wakeup.ind Bit[2] - sleep.ind FI[1:0] denotes CT. Please program to 2'b11 if no support of counter. |
| 16:23 | DLCEXT | RW | R | Undefined | <p>Data Length Count Extension.</p> <p>This field is intended for payload of more than 12B. This field is only valid if DLC=4'b1111 (FI[7:4]).</p> <p>The value specified in this field will be the new payload size. Valid values are 0-255.</p> |

7.5.3.8 CXPI_CH_RXPID_FI

Description: RXPID and Frame Information
Address: 0x40518054
Offset: 0x54
Retention: Not Retained
IsDeepSleep: No
Comment: This register holds information on RX's PID, Frame Information, and DLCEXT.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | PID [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | FI [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DLCEXT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|---|
| 0:7 | PID | R | RW | Undefined | <p>Header protected identifier (PID).</p> <ul style="list-style-type: none"> - Bits 6 down to 0: frame identifier ID[6:0]. - Bits 7: is odd parity bit. - $PID[7] = ! (ID[6] \wedge ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[2] \wedge ID[1] \wedge ID[0])$ <p>Reception: Received PID field. SW uses the PID field to determine how to handle the response for a received frame header: TX_RESPONSE or RX_RESPONSE.</p> <p>Note that, this field can be use by SW to check PType byte as the HW handles both PID and PType the same way. The frame type would occupy bit[6:0] and bit[7] is the parity bit of the frame type. This parity bit is send by the transmitting node.</p> |
| 8:15 | FI | R | RW | Undefined | <p>Frame Information.</p> <p>This is the byte that is received as Frame Information. Per CXPI spec, FI[7:4] denotes the data length count (DLC). FI[3:2] denotes Network Management. Bit[3] - wakeup.ind Bit[2] - sleep.ind FI[1:0] denotes CT.</p> |
| 16:23 | DLCEXT | R | RW | Undefined | <p>Data Length Count Extension.</p> <p>This field is intended for payload of more than 12B. This field is only valid if DLC=4'b1111 (FI[15:12]).</p> <p>The value specified in this field will be the new payload size. Valid values are 0-255.</p> |

7.5.3.9 CXPI_CH_CRC

Description: CRC
Address: 0x40518058
Offset: 0x58
Retention: Not Retained
IsDeepSleep: No
Comment: This register holds the CRC bytes for RX and TX.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | RXCRC1 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | RXCRC2 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TXCRC1 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TXCRC2 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------|----|----|-----------------|---|
| 0:7 | RXCRC1 | R | RW | Undefined | CRC first byte for both CRC8 and CRC16. This is valid for both Normal frame and Long frame. HW will load this field with first byte of CRC upon receiving it. |
| 8:15 | RXCRC2 | R | RW | Undefined | CRC second byte of CRC16. This is valid only for Long frames. HW will load this field with second byte of CRC upon receiving it. |
| 16:23 | TXCRC1 | R | RW | Undefined | CRC first byte for both CRC8 and CRC16. This is valid for both Normal frame and Long frame. HW will load this field with first byte of CRC for transmit. |
| 24:31 | TXCRC2 | R | RW | Undefined | CRC second byte of CRC16. This is valid only for Long frames. HW will load this field with second byte of CRC for transmit. |

7.5.3.10 CXPI_CH_TX_FIFO_CTL

Description: TX FIFO control
Address: 0x40518080
Offset: 0x80
Retention: Not Retained
IsDeepSleep: No
Comment: This is the transmit fifo control register
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---------------------|---|---|---|---|
| Name | None [7:5] | | | TRIGGER_LEVEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----------------|---------------|
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:4 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the TX FIFO has less entries than the number of this field, a transmitter trigger event is generated: -INTR.TX_FIFO_TRIGGER = (#FIFO entries < TRIGGER_LEVEL) |
| 16 | CLEAR | RW | R | 0 | This is a synchronous clear signal to the TX FIFO. When '1', the TX FIFO content are cleared. If a quick clear is required, the field should be set to '1' and followed by '0'. If a clear is required for an extended time, the field should be set to 1 during the complete time. |
| 17 | FREEZE | RW | R | 0 | Freeze functionality: '0': HW uses TX FIFO data and pops the data from the TX FIFO for every HW read. '1': HW read from TX FIFO does not pop the data from the TX FIFO. Note: Freeze functionality is for debug purpose only. |

7.5.3.11 CXPI_CH_TX_FIFO_STATUS

Description: TX FIFO status
Address: 0x40518084
Offset: 0x84
Retention: Not Retained
IsDeepSleep: No
Comment: This is the transmit fifo control register
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|---------------|----|----|----|----|
| Name | None [7:5] | | | USED [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:21] | | | AVAIL [20:16] | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 0:4 | USED | R | W | 0 | Number of used/occupied entries in the TX FIFO. The field value is in the range [0, 16]. When '0', the TX FIFO is empty. When '16', the TX FIFO is full. |
| 16:20 | AVAIL | R | W | Undefined | TX FIFO Avail 0-No available slot in TX FIFO 1-1 available slot in TX FIFO. 2-2 available slot in TX FIFO. .. 16-16 available slot in TX FIFO. Note that the Fifo Width is 1Byte and each slot in this context is 1 depth of the Fifo. The number of bytes are determine through the number of data bytes in a message frame. (TXPID_FI.FI/TXPID_FI.DLCEXT) |

7.5.3.12 CXPI_CH_TX_FIFO_WR

Description: TX FIFO write
Address: 0x40518088
Offset: 0x88
Retention: Not Retained
IsDeepSleep: No
Comment: This register supports 32-bit access only
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:7 | DATA | W | R | 0 | <p>Transmit Data field.</p> <p>Transmission: To be transmitted data field. SW provides data field.</p> <p>HW shadows over the write data to TX FIFO after SW performs a write to this field.</p> <p>HW shadows the whole 8 bits to the TX FIFO and relies on the TXPID_FI.FI/TXPID_FI.DCLEXT to determine the number of bytes.</p> <p>SW needs to ensure that TX FIFO is not overwritten before the content is consumed by HW by checking TX_FIFO_STATUS.AVAIL. Otherwise, the previous content would be overwritten and resulting in TX FIFO's overflow error (INTR.TX_OVERFLOW_ERROR).</p> |

7.5.3.13 CXPI_CH_RX_FIFO_CTL

Description: RX FIFO control
Address: 0x405180A0
Offset: 0xA0
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains RX FIFO control
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|---------------------|----|----|----------------|---------------|
| Name | None [7:5] | | | TRIGGER_LEVEL [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:4 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When RX FIFO has more entries than the number of this field, a receiver trigger event is generated. - INTR_RX_FIFO_TRIGGER = (#FIFO entries > TRIGGER_LEVEL) |
| 16 | CLEAR | RW | R | 0 | When '1', the RX FIFO content are popped. If a quick clear is required, the field should be set to '1' and followed by '0'. If a clear is required for an extended time, the field should be set to 1 during the complete time. |
| 17 | FREEZE | RW | R | 0 | Freeze functionality: '0': HW writes to RX FIFO and push the data to RX FIFO. '1': HW write to RX FIFO does not push the data to the RX FIFO. Note: Freeze functionality is for debug purpose only. |

7.5.3.14 CXPI_CH_RX_FIFO_STATUS

Description: RX FIFO status
Address: 0x405180A4
Offset: 0xA4
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains RX FIFO control
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------|---|---|---|---|
| Name | None [7:5] | | | USED [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|---------------|----|----|----|----|
| Name | None [23:21] | | | AVAIL [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 0:4 | USED | R | W | 0 | Number of used/occupied entries in the RX FIFO. The field value is in the range [0, 16]. When '0', the RX FIFO is empty. When '16', the RX FIFO is full. |
| 16:20 | AVAIL | R | W | Undefined | RX FIFO avail 0-No content in RX FIFO 1-1 available content in RX FIFO. 2-2 available content in RX FIFO. .. 16-16 available content in RX FIFO. Note that the Fifo Width is 1Byte and each content in this context means 1 fifo slot. The number of bytes in each slot are determine through the number of data bytes in a message frame. (RXPID_FI.FI/RXPID_FI.DLCEXT) |

7.5.3.15 CXPI_CH_RX_FIFO_RD

Description: RX FIFO read
Address: 0x405180A8
Offset: 0xA8
Retention: Not Retained
IsDeepSleep: No
Comment: This register supports a single 32-bit access to read data fields.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:7 | DATA | R | W | Undefined | <p>Received Data field. Software uses this data field.</p> <p>HW shadows the first content of the RX FIFO to this field. Software reading this field will remove the content from the RX FIFO and the next content of the RX FIFO will be shadowed over to this field. This field is 8bits and reflects the width of the RX FIFO. Software needs to rely on the RXPID_FI.FI/RXPID_FI.DLCNEXT fields to determine number of bytes. Note that, during debug, a read from test controller would not remove/destory the content.</p> <p>Software needs to ensure it does not read from this field if there is no available content (from RX_FIFO_STATUS.USED). Otherwise, the content is undefined and it would result in RX FIFO underflow error. (INTR.RX_UNDERFLOW_ERROR).</p> |

7.5.3.16 CXPI_CH_RX_FIFO_RD_SILENT

Description: RX FIFO silent read
Address: 0x405180AC
Offset: 0xAC
Retention: Not Retained
IsDeepSleep: No
Comment: This register supports a single 32-bit access to read data fields.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:7 | DATA | R | W | Undefined | Data read from the RX FIFO. Reading data from this field would not pop the data from RX FIFO. This register is for debug purpose. |

7.5.3.17 CXPI_CH_INTR

Description: Interrupt
Address: 0x405180C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL0.ENABLED to '0' clears all command fields to '0'.

An activated error interrupt cause aborts an ongoing frame transfer (except for bit errors when CTL0.BIT_ERROR_IGNORE is '1').

Note that, if there is noise sample after the sampling of the stop bit of CRC byte, the TX_HEADER_DONE, TX_RESPONSE_DONE, RX_HEADER_DONE, or RX_RESPONSE_DONE (which ever corresponding done to be set during the transaction) may assert before the full Tbit of the stop bit.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------------|----------------------|------------|------------------------|----------------------|
| Name | None [7:5] | | | TX_FIFO_TRIGGER [4:4] | TX_WAKEUP_DONE [3:3] | None [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|-----------------------|----------------------------|-------------------------|--------------------------|------------------------|----------------------|
| Name | None [15:14] | | TXRX_COMPLETE [13:13] | RX_HEADER_PID_DONE [12:12] | RX_FIFO_TRIGGER [11:11] | RX_WAKEUP_DETECT [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------------------|--------------------------------|----------------------|----------------------|----------------------------|-----------------|--------------|----|
| Name | RX_DATA_LENGTH_ERROR [23:23] | RX_HEADER_PARITY_ERROR [22:22] | RX_CRC_ERROR [21:21] | TX_BIT_ERROR [20:20] | TX_HEADER_ARB_LOST [19:19] | TIMEOUT [18:18] | None [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|------------------------|------------------------|----------------------------|----------------------------|---------------------------|---------------------------|------------------------------|
| Name | None [31:31] | TX_FRAME_ERROR [30:30] | RX_FRAME_ERROR [29:29] | TX_UNDERFLOW_ERROR [28:28] | RX_UNDERFLOW_ERROR [27:27] | TX_OVERFLOW_ERROR [26:26] | RX_OVERFLOW_ERROR [25:25] | TX_DATA_LENGTH_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|------|------|-----------------|---|
| 0 | TX_HEADER_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame header (PID field or PType field) is transmitted (the CMD.TX_HEADER is completed). Specifically: - For PID transmission only and without prior transmission of PTYPE, when followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the message frame transfer. - For PID transmission only and without prior transmission of PTYPE, when not followed by a response command, this field is set to '1' after completion of the header transfer. -Note for the case of PTYPE is transmitted follow by CMD.RX_RESPONSE or no following response, HW sets this field to '1' after transmitting PTYPE. |
| 1 | TX_RESPONSE_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame response (frame information fields, data fields, and crc field) is transmitted (the CMD.TX_RESPONSE is completed). |
| 3 | TX_WAKEUP_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a wakeup signal is transmitted (per CTL2.T_WAKEUP_LENGTH). This interrupt cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal. |
| 4 | TX_FIFO_TRIGGER | RW1C | RW1S | 0 | HW sets this field to '1', when TX trigger is generated (#used TX FIFO < TRIGGER_LEVEL). |
| 8 | RX_HEADER_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame header (PID field or PType field) is received (the CMD.RX_HEADER is completed). Specifically: - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the message frame transfer. - When not followed by a response command, this field is set to '1' after completion of the header transfer if RXPIDZERO_CHECK_EN=1 and header received is PID. If RXPIDZERO_CHECK_EN=0 and response commands are not set, HW will set this field to '1' after receiving PID or PTYPE. |
| 9 | RX_RESPONSE_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when a frame response (frame information fields, data fields, and crc field) is received (the CMD.RX_RESPONSE is completed). |
| 10 | RX_WAKEUP_DETECT | RW1C | RW1S | 0 | HW sets this field to '1', when RX fall is detected in Sleep mode. |
| 11 | RX_FIFO_TRIGGER | RW1C | RW1S | 0 | HW sets this field to '1', when RX trigger is generated (#used RX FIFO > TRIGGER_LEVEL). |
| 12 | RX_HEADER_PID_DONE | RW1C | RW1S | 0 | HW sets this field to '1', when RX header (PID/PTYPE field) is received. |
| 13 | TXRX_COMPLETE | RW1C | RW1S | 0 | HW sets this field to '1', when message frame ends after EOF is completed and TX/RX_DATA_LENGTH_ERROR=0. |
| 18 | TIMEOUT | RW1C | RW1S | 0 | HW sets this field to '1', when the transmitted/received bytes space within a message frame is > TIMEOUT_LENGTH. SW needs to set TIMEOUT_SEL=0 before clearing TIMEOUT=0 to ensure HW does not immediately sets back the interrupt. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|------|------|-----------------|---|
| 19 | TX_HEADER_ARB_LOST | RW1C | RW1S | 0 | <p>HW sets this field to '1', when it detects arbitration lost after the number of retries has exceed the maximum allowed retries.</p> <p>Note: The ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated and the TX_HEADER and TX_RESPONSE command is cleared to 0).</p> |
| 20 | TX_BIT_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a transmitted 'cspi_tx_out' value does NOT match a received 'cspi_rx_in' value.</p> <p>The match is performed for the PID fields or PType (for the START bit and STOP bit only) and for the rest of the response i.e. frame information fields, data fields and the crc field (for the START bit, DATA bits, and STOP bits).</p> <p>Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.</p> |
| 21 | RX_CRC_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when received CRC is not matching with the compute CRC from header and response.</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated).</p> |
| 22 | RX_HEADER_PARITY_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the received PID field or PType field has a parity error.</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_HEADER_PID_DONE is NOT activated).</p> |
| 23 | RX_DATA_LENGTH_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the received message frame's data fields are more than the value specified in DLC (for normal frame) or DLCEXT (for long frame) i.e. after receiving CRC byte(s), HW is receiving logical '0' during EOF. For the case of receiving data length less than DLC/DLCEXT, HW will also set this field to '1'. This is the case where IBS>9 before the number of data reaches data length, then HW will report as data length error. HW starts checking after frame information byte.</p> <p>Note: SW needs to handle the message transfer i.e. discard or flush out. HW will still set the RX_RESPONSE_DONE.</p> |
| 24 | TX_DATA_LENGTH_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the transmit message frame's data fields are more than the value specified in DLC (for normal frame) or DLCEXT (for long frame) i.e. after transmitting CRC(s) byte, HW is receiving logical '0' during EOF.</p> <p>Note: HW will still set TX_RESPONSE_DONE and the TX_HEADER and TX_RESPONSE commands are set to '0'.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|------|------|-----------------|--|
| 25 | RX_OVERFLOW_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the RX data is overwritten by HW before the SW reads from it. In CXPI spec, this error is denoted as overrun error.</p> <p>Note: Upon this error, SW should discard the RX data in RX FIFO.</p> |
| 26 | TX_OVERFLOW_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the TX data is overwritten by SW before the HW reads from it to transmit to CXPI bus.</p> <p>Note: The ongoing message transfer will continue when this error happens however, data transferred at CXPI bus will be bogus and HW will invert the CRC to invalidate the message at the receiving node. TX_HEADER and TX_RESPONSE commands are set to '0'.</p> |
| 27 | RX_UNDERFLOW_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when RX FIFO is empty and SW reads from it.</p> <p>Note: Upon this error, SW should discard the RX data in RX FIFO.</p> |
| 28 | TX_UNDERFLOW_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when TX FIFO is empty and HW reads from it.</p> <p>Note: The ongoing message transfer will continue when this error happens however, data transferred at CXPI will be bogus and HW will invert the CRC to invalidate the message at the receiving node. TX_HEADER and TX_RESPONSE commands are set to '0'.</p> |
| 29 | RX_FRAME_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the stop bit of a byte frame is incorrect.</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated and the INTR.RX_HEADER_DONE/TX_HEADER_DONE is NOT activated if the frame error occurs during header byte or if frame error occurs during response byte (if the HEADER and RESPONSE commands are set together)).</p> |
| 30 | TX_FRAME_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the stop bit of a byte frame is incorrect.</p> <p>This error would be a subset of TX_BIT_ERROR and also subjected to BIT_ERROR_IGNORE field.</p> <p>Note: The ongoing message transfer is aborted (INTR.TX_HEADER_DONE/RX_HEADER_DONE and INTR.TX_RESPONSE_DONE are NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'.</p> <p>Note: When CTL0.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE and INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER and TX_RESPONSE commands are set to '0'. When CTL0.BIT_ERROR_IGNORE is '1', the ongoing message transfer would be transferred.</p> |

7.5.3.18 CXPI_CH_INTR_SET

Description: Interrupt set
Address: 0x405180C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------------------|-------------------------|------------|---------------------------|-------------------------|
| Name | None [7:5] | | | TX_FIFO_TRIGGER [4:4] | TX_WAKEUP_DONE [3:3] | None [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|--------------------------|-------------------------------|----------------------------|-----------------------------|---------------------------|-------------------------|
| Name | None [15:14] | | TXRX_COMPLETE [13:13] | RX_HEADER_PID_DONE [12:12] | RX_FIFO_TRIGGER [11:11] | RX_WAKEUP_DETECT [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------------------|-----------------------------------|-------------------------|-------------------------|-------------------------------|--------------------|--------------|----|
| Name | RX_DATA_LENGTH_ERROR [23:23] | RX_HEADER_PARITY_ERROR [22:22] | RX_CRC_ERROR [21:21] | TX_BIT_ERROR [20:20] | TX_HEADER_ARB_LOST [19:19] | TIMEOUT [18:18] | None [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|---------------------------|---------------------------|-------------------------------|-------------------------------|------------------------------|------------------------------|---------------------------------|
| Name | None [31:31] | TX_FRAME_ERROR [30:30] | RX_FRAME_ERROR [29:29] | TX_UNDERFLOW_ERROR [28:28] | RX_UNDERFLOW_ERROR [27:27] | TX_OVERFLOW_ERROR [26:26] | RX_OVERFLOW_ERROR [25:25] | TX_DATA_LENGTH_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|------|----|-----------------|---|
| 0 | TX_HEADER_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 1 | TX_RESPONSE_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 3 | TX_WAKEUP_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 4 | TX_FIFO_TRIGGER | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 8 | RX_HEADER_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 9 | RX_RESPONSE_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 10 | RX_WAKEUP_DETECT | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 11 | RX_FIFO_TRIGGER | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 12 | RX_HEADER_PID_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 13 | TXRX_COMPLETE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|------|----|-----------------|---|
| 18 | TIMEOUT | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 19 | TX_HEADER_ARB_LOST | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 20 | TX_BIT_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 21 | RX_CRC_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 22 | RX_HEADER_PARITY_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 23 | RX_DATA_LENGTH_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 24 | TX_DATA_LENGTH_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 25 | RX_OVERFLOW_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 26 | TX_OVERFLOW_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 27 | RX_UNDERFLOW_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 28 | TX_UNDERFLOW_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 29 | RX_FRAME_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 30 | TX_FRAME_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

7.5.3.19 CXPI_CH_INTR_MASK

Description: Interrupt mask
Address: 0x405180C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------------------|-------------------------|------------|---------------------------|-------------------------|
| Name | None [7:5] | | | TX_FIFO_TRIGGER [4:4] | TX_WAKEUP_DONE [3:3] | None [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|--------------------------|-------------------------------|----------------------------|-----------------------------|---------------------------|-------------------------|
| Name | None [15:14] | | TXRX_COMPLETE [13:13] | RX_HEADER_PID_DONE [12:12] | RX_FIFO_TRIGGER [11:11] | RX_WAKEUP_DETECT [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------------------|-----------------------------------|-------------------------|-------------------------|-------------------------------|--------------------|--------------|----|
| Name | RX_DATA_LENGTH_ERROR [23:23] | RX_HEADER_PARITY_ERROR [22:22] | RX_CRC_ERROR [21:21] | TX_BIT_ERROR [20:20] | TX_HEADER_ARB_LOST [19:19] | TIMEOUT [18:18] | None [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|---------------------------|---------------------------|-------------------------------|-------------------------------|------------------------------|------------------------------|---------------------------------|
| Name | None [31:31] | TX_FRAME_ERROR [30:30] | RX_FRAME_ERROR [29:29] | TX_UNDERFLOW_ERROR [28:28] | RX_UNDERFLOW_ERROR [27:27] | TX_OVERFLOW_ERROR [26:26] | RX_OVERFLOW_ERROR [25:25] | TX_DATA_LENGTH_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|----|----|-----------------|--|
| 0 | TX_HEADER_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 1 | TX_RESPONSE_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 3 | TX_WAKEUP_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 4 | TX_FIFO_TRIGGER | RW | R | 0 | Mask for corresponding field in INTR register. |
| 8 | RX_HEADER_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 9 | RX_RESPONSE_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 10 | RX_WAKEUP_DETECT | RW | R | 0 | Mask for corresponding field in INTR register. |
| 11 | RX_FIFO_TRIGGER | RW | R | 0 | Mask for corresponding field in INTR register. |
| 12 | RX_HEADER_PID_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 13 | TXRX_COMPLETE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 18 | TIMEOUT | RW | R | 0 | Mask for corresponding field in INTR register. |
| 19 | TX_HEADER_ARB_LOST | RW | R | 0 | Mask for corresponding field in INTR register. |
| 20 | TX_BIT_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 21 | RX_CRC_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 22 | RX_HEADER_PARITY_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 23 | RX_DATA_LENGTH_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|--|
| 24 | TX_DATA_LENGTH_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 25 | RX_OVERFLOW_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 26 | TX_OVERFLOW_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 27 | RX_UNDERFLOW_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 28 | TX_UNDERFLOW_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 29 | RX_FRAME_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 30 | TX_FRAME_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |

7.5.3.20 CXPI_CH_INTR_MASKED

Description: Interrupt masked

Address: 0x405180CC

Offset: 0xCC

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------------------|-------------------------|------------|---------------------------|-------------------------|
| Name | None [7:5] | | | TX_FIFO_TRIGGER [4:4] | TX_WAKEUP_DONE [3:3] | None [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|--------------------------|-------------------------------|----------------------------|-----------------------------|---------------------------|-------------------------|
| Name | None [15:14] | | TXRX_COMPLETE [13:13] | RX_HEADER_PID_DONE [12:12] | RX_FIFO_TRIGGER [11:11] | RX_WAKEUP_DETECT [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------------------|-----------------------------------|-------------------------|-------------------------|-------------------------------|--------------------|--------------|----|
| Name | RX_DATA_LENGTH_ERROR [23:23] | RX_HEADER_PARITY_ERROR [22:22] | RX_CRC_ERROR [21:21] | TX_BIT_ERROR [20:20] | TX_HEADER_ARB_LOST [19:19] | TIMEOUT [18:18] | None [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|---------------------------|---------------------------|-------------------------------|-------------------------------|------------------------------|------------------------------|---------------------------------|
| Name | None [31:31] | TX_FRAME_ERROR [30:30] | RX_FRAME_ERROR [29:29] | TX_UNDERFLOW_ERROR [28:28] | RX_UNDERFLOW_ERROR [27:27] | TX_OVERFLOW_ERROR [26:26] | RX_OVERFLOW_ERROR [25:25] | TX_DATA_LENGTH_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | TX_HEADER_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 1 | TX_RESPONSE_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 3 | TX_WAKEUP_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 4 | TX_FIFO_TRIGGER | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 8 | RX_HEADER_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 9 | RX_RESPONSE_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 10 | RX_WAKEUP_DETECT | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 11 | RX_FIFO_TRIGGER | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|----|----|-----------------|---|
| 12 | RX_HEADER_PID_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 13 | TXRX_COMPLETE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 18 | TIMEOUT | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 19 | TX_HEADER_ARB_LOST | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 20 | TX_BIT_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 21 | RX_CRC_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 22 | RX_HEADER_PARITY_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 23 | RX_DATA_LENGTH_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 24 | TX_DATA_LENGTH_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 25 | RX_OVERFLOW_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 26 | TX_OVERFLOW_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 27 | RX_UNDERFLOW_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 28 | TX_UNDERFLOW_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 29 | RX_FRAME_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 30 | TX_FRAME_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |

8 DMAC

| | |
|---------------------|------------|
| Description | DMAC |
| Base Address | 0x402A0000 |
| Size | 0x10000 |
| Slave Num | MMIO2 - 9 |

| Register Name | Address | Permission | Description |
|---------------|------------|------------|-----------------|
| DMAC_CTL | 0x402A0000 | FULL | Control |
| DMAC_ACTIVE | 0x402A0008 | FULL | Active channels |

8.1 CH 0

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|-------------------------------------|
| DMAC_CH0_CTL | 0x402A1000 | FULL | Channel control |
| DMAC_CH0_IDX | 0x402A1010 | FULL | Channel current indices |
| DMAC_CH0_SRC | 0x402A1014 | FULL | Channel current source address |
| DMAC_CH0_DST | 0x402A1018 | FULL | Channel current destination address |
| DMAC_CH0_CURR | 0x402A1020 | FULL | Channel current descriptor pointer |
| DMAC_CH0_TR_CMD | 0x402A1028 | FULL | Channel software trigger |
| DMAC_CH0_DESCR_STATUS | 0x402A1040 | FULL | Channel descriptor status |
| DMAC_CH0_DESCR_CTL | 0x402A1060 | FULL | Channel descriptor control |
| DMAC_CH0_DESCR_SRC | 0x402A1064 | FULL | Channel descriptor source |
| DMAC_CH0_DESCR_DST | 0x402A1068 | FULL | Channel descriptor destination |
| DMAC_CH0_DESCR_X_SIZE | 0x402A106C | FULL | Channel descriptor X size |
| DMAC_CH0_DESCR_X_INCR | 0x402A1070 | FULL | Channel descriptor X increment |
| DMAC_CH0_DESCR_Y_SIZE | 0x402A1074 | FULL | Channel descriptor Y size |
| DMAC_CH0_DESCR_Y_INCR | 0x402A1078 | FULL | Channel descriptor Y increment |
| DMAC_CH0_DESCR_NEXT | 0x402A107C | FULL | Channel descriptor next pointer |
| DMAC_CH0_INTR | 0x402A1080 | FULL | Interrupt |
| DMAC_CH0_INTR_SET | 0x402A1084 | FULL | Interrupt set |
| DMAC_CH0_INTR_MASK | 0x402A1088 | FULL | Interrupt mask |
| DMAC_CH0_INTR_MASKED | 0x402A108C | FULL | Interrupt masked |

8.2 CH 1

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|-------------------------------------|
| DMAC_CH1_CTL | 0x402A1100 | FULL | Channel control |
| DMAC_CH1_IDX | 0x402A1110 | FULL | Channel current indices |
| DMAC_CH1_SRC | 0x402A1114 | FULL | Channel current source address |
| DMAC_CH1_DST | 0x402A1118 | FULL | Channel current destination address |
| DMAC_CH1_CURR | 0x402A1120 | FULL | Channel current descriptor pointer |
| DMAC_CH1_TR_CMD | 0x402A1128 | FULL | Channel software trigger |
| DMAC_CH1_DESCR_STATUS | 0x402A1140 | FULL | Channel descriptor status |
| DMAC_CH1_DESCR_CTL | 0x402A1160 | FULL | Channel descriptor control |
| DMAC_CH1_DESCR_SRC | 0x402A1164 | FULL | Channel descriptor source |
| DMAC_CH1_DESCR_DST | 0x402A1168 | FULL | Channel descriptor destination |
| DMAC_CH1_DESCR_X_SIZE | 0x402A116C | FULL | Channel descriptor X size |
| DMAC_CH1_DESCR_X_INCR | 0x402A1170 | FULL | Channel descriptor X increment |
| DMAC_CH1_DESCR_Y_SIZE | 0x402A1174 | FULL | Channel descriptor Y size |
| DMAC_CH1_DESCR_Y_INCR | 0x402A1178 | FULL | Channel descriptor Y increment |
| DMAC_CH1_DESCR_NEXT | 0x402A117C | FULL | Channel descriptor next pointer |
| DMAC_CH1_INTR | 0x402A1180 | FULL | Interrupt |
| DMAC_CH1_INTR_SET | 0x402A1184 | FULL | Interrupt set |
| DMAC_CH1_INTR_MASK | 0x402A1188 | FULL | Interrupt mask |
| DMAC_CH1_INTR_MASKED | 0x402A118C | FULL | Interrupt masked |

8.3 CH 2

| Register Name | Address | Permission | Description |
|---------------|------------|------------|-------------------------------------|
| DMAC_CH2_CTL | 0x402A1200 | FULL | Channel control |
| DMAC_CH2_IDX | 0x402A1210 | FULL | Channel current indices |
| DMAC_CH2_SRC | 0x402A1214 | FULL | Channel current source address |
| DMAC_CH2_DST | 0x402A1218 | FULL | Channel current destination address |
| DMAC_CH2_CURR | 0x402A1220 | FULL | Channel current descriptor pointer |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---------------------------------|
| DMAC_CH2_TR_CMD | 0x402A1228 | FULL | Channel software trigger |
| DMAC_CH2_DESCR_STATUS | 0x402A1240 | FULL | Channel descriptor status |
| DMAC_CH2_DESCR_CTL | 0x402A1260 | FULL | Channel descriptor control |
| DMAC_CH2_DESCR_SRC | 0x402A1264 | FULL | Channel descriptor source |
| DMAC_CH2_DESCR_DST | 0x402A1268 | FULL | Channel descriptor destination |
| DMAC_CH2_DESCR_X_SIZE | 0x402A126C | FULL | Channel descriptor X size |
| DMAC_CH2_DESCR_X_INCR | 0x402A1270 | FULL | Channel descriptor X increment |
| DMAC_CH2_DESCR_Y_SIZE | 0x402A1274 | FULL | Channel descriptor Y size |
| DMAC_CH2_DESCR_Y_INCR | 0x402A1278 | FULL | Channel descriptor Y increment |
| DMAC_CH2_DESCR_NEXT | 0x402A127C | FULL | Channel descriptor next pointer |
| DMAC_CH2_INTR | 0x402A1280 | FULL | Interrupt |
| DMAC_CH2_INTR_SET | 0x402A1284 | FULL | Interrupt set |
| DMAC_CH2_INTR_MASK | 0x402A1288 | FULL | Interrupt mask |
| DMAC_CH2_INTR_MASKED | 0x402A128C | FULL | Interrupt masked |

8.4 CH 3

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|-------------------------------------|
| DMAC_CH3_CTL | 0x402A1300 | FULL | Channel control |
| DMAC_CH3_IDX | 0x402A1310 | FULL | Channel current indices |
| DMAC_CH3_SRC | 0x402A1314 | FULL | Channel current source address |
| DMAC_CH3_DST | 0x402A1318 | FULL | Channel current destination address |
| DMAC_CH3_CURR | 0x402A1320 | FULL | Channel current descriptor pointer |
| DMAC_CH3_TR_CMD | 0x402A1328 | FULL | Channel software trigger |
| DMAC_CH3_DESCR_STATUS | 0x402A1340 | FULL | Channel descriptor status |
| DMAC_CH3_DESCR_CTL | 0x402A1360 | FULL | Channel descriptor control |
| DMAC_CH3_DESCR_SRC | 0x402A1364 | FULL | Channel descriptor source |
| DMAC_CH3_DESCR_DST | 0x402A1368 | FULL | Channel descriptor destination |
| DMAC_CH3_DESCR_X_SIZE | 0x402A136C | FULL | Channel descriptor X size |
| DMAC_CH3_DESCR_X_INCR | 0x402A1370 | FULL | Channel descriptor X increment |
| DMAC_CH3_DESCR_Y_SIZE | 0x402A1374 | FULL | Channel descriptor Y size |
| DMAC_CH3_DESCR_Y_INCR | 0x402A1378 | FULL | Channel descriptor Y increment |
| DMAC_CH3_DESCR_NEXT | 0x402A137C | FULL | Channel descriptor next pointer |
| DMAC_CH3_INTR | 0x402A1380 | FULL | Interrupt |
| DMAC_CH3_INTR_SET | 0x402A1384 | FULL | Interrupt set |
| DMAC_CH3_INTR_MASK | 0x402A1388 | FULL | Interrupt mask |
| DMAC_CH3_INTR_MASKED | 0x402A138C | FULL | Interrupt masked |

8.5 Register Details

8.5.1 DMAC_CTL

Description: Control
Address: 0x402A0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 31 | ENABLED | RW | R | 0 | IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. |
| | DISABLED | | | 0 | N/A |
| | ENABLED | | | 1 | N/A |

8.5.2 DMAC_ACTIVE

Description: Active channels
Address: 0x402A0008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | ACTIVE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | ACTIVE | R | W | 0 | Specifies active channels; i.e. enabled channels whose trigger got activated. |

8.5.3 CH

8.5.3.1 DMAC_CH_CTL

Description: Channel control
Address: 0x402A1000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|------------|---------|----------|---------|
| Name | PC [7:4] | | | | None [3:3] | B [2:2] | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | P | RW | R | 0 | <p>User/privileged access control: '0': user mode. '1': privileged mode.</p> <p>This field is set with the user/privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data.</p> <p>All transactions for this channel use the P field for the user/privileged access control ('hprot[1]').</p> |
| 1 | NS | RW | R | 1 | <p>Secure/on-secure access control: '0': secure. '1': non-secure.</p> <p>This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data.</p> <p>All transactions for this channel use the NS field for the secure/non-secure access control ('hprot[4]').</p> |
| 2 | B | RW | R | 0 | <p>Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable.</p> <p>This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data.</p> <p>All transactions for this channel uses the B field for the non-bufferable/bufferable access control ('hprot[2]').</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|------|-----------------|--|
| 4:7 | PC | RW | R | 0 | <p>Protection context.</p> <p>This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data.</p> <p>All transactions for this channel uses the PC field for the protection context.</p> |
| 8:9 | PRI0 | RW | R | 0 | <p>Channel priority:</p> <p>'0': highest priority.</p> <p>'1'</p> <p>'2'</p> <p>'3': lowest priority.</p> <p>Channels with the same priority constitute a priority group and within this priority group, the following 'roundrobin' arbitration is applied.</p> <p>A 'round' consists of a contiguous sequence of channel activations, within this priority group, without any repetition. Within a round, higher priority is given to the lower channel indices. The notion of a round guarantees that within a group, higher channel indices do not yield to lower indices indefinitely.</p> |
| 31 | ENABLED | RW | RW1C | 0 | <p>Channel enable:</p> <p>'0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed).</p> <p>'1': Enabled.</p> <p>SW sets this field to '1' to enable a specific channel.</p> <p>HW sets this field to '0' when an error interrupt cause is activated.</p> |

8.5.3.2 DMAC_CH_IDX

Description: Channel current indices
Address: 0x402A1010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------|---|---|---|---|---|---|---|
| Name | X [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------|----|----|----|----|----|---|---|
| Name | X [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------|----|----|----|----|----|----|----|
| Name | Y [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------|----|----|----|----|----|----|----|
| Name | Y [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:15 | X | R | W | Undefined | Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to '0' when it loads a descriptor. |
| 16:31 | Y | R | W | Undefined | Specifies the Y loop index, with Y_COUNT taken from the current descriptor. Note: HW sets this field to '0' when it loads a descriptor.. |

8.5.3.3 DMAC_CH_SRC

Description: Channel current source address
Address: 0x402A1014
Offset: 0x14
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|-------------------------------------|
| 0:31 | ADDR | R | W | Undefined | Current address of source location. |

8.5.3.4 DMAC_CH_DST

Description: Channel current destination address
Address: 0x402A1018
Offset: 0x18
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | ADDR | R | W | Undefined | Current address of destination location. |

8.5.3.5 DMAC_CH_CURR

Description: Channel current descriptor pointer
Address: 0x402A1020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | PTR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 2:31 | PTR | RW | RW | Undefined | Address of current descriptor. When this field is '0', there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. |

8.5.3.6 DMAC_CH_TR_CMD

Description: Channle software trigger
Address: 0x402A1028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------|
| Name | None [7:1] | | | | | | | ACTIVATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|----|-----------------|---|
| 0 | ACTIVATE | RW1S | A | 0 | Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. |

8.5.3.7 DMAC_CH_DESCR_STATUS

Description: Channel descriptor status
Address: 0x402A1040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|--------------|----|----|----|----|----|----|
| Name | VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 31 | VALID | R | W | 0 | Indicates whether the descriptor information present in DESCR_CTL, DESCR_SRC, DESCR_DST, DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE, DESCR_Y_INCR, DESCR_NEXT status registers is valid or not. |

8.5.3.8 DMAC_CH_DESCR_CTL

Description: Channel descriptor control
Address: 0x402A1060
Offset: 0x60
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_CTL of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|-------------------|---|-----------------|---|----------------------|---|
| Name | TR_IN_TYPE [7:6] | | TR_OUT_TYPE [5:4] | | INTR_TYPE [3:2] | | WAIT_FOR_DEACT [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|----------------------|
| Name | None [15:9] | | | | | | | DATA_PREF ETCH [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------------|----|
| Name | None [23:18] | | | | | | DATA_SIZE [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------------|----|----|----------------------------|----------------------------|--------------|--------------------|
| Name | None [31:31] | DESCR_TYPE [30:28] | | | DST_TRANS FER_SIZE [27:27] | SRC_TRANS FER_SIZE [26:26] | None [25:25] | CH_DISABLE [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:1 | WAIT_FOR_DEACT | R | W | Undefined | <p>Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to '0'). The wait cycles incurred by this field reduce DW controller performance.</p> <p>'0': Do not wait for trigger de-activation (for pulse sensitive triggers). '1': Wait for up to 4 cycles. '2': Wait for up to 16 cycles. '3': Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 2:3 | INTR_TYPE | R | W | Undefined | <p>Specifies when a completion interrupt is generated (CH_STATUS.INTR_CAUSE is set to COMPLETION):</p> <p>'0': An interrupt is generated after a single transfer.</p> <p>'1': An interrupt is generated after a single 1D transfer or a memory copy transfer</p> <ul style="list-style-type: none"> - If the descriptor type is 'single', the interrupt is generated after a single transfer. - If the descriptor type is '1D' or '2D', the interrupt is generated after the execution of a 1D transfer. - If the descriptor type is 'memory copy', the interrupt is generated after the execution of a memory copy transfer. - If the descriptor type is 'scatter' the interrupt is generated after the execution of a scatter transfer. <p>'2': An interrupt is generated after the execution of the current descriptor (independent of the value of DESCR_NEXT_PTR.ADDR of the current descriptor).</p> <p>'3': An interrupt is generated after the execution of the current descriptor and the current descriptor's DESCR_NEXT_PTR.ADDR is '0'.</p> |
| 4:5 | TR_OUT_TYPE | R | W | Undefined | <p>Specifies when an output trigger is generated:</p> <p>'0': An output trigger is generated after a single transfer.</p> <p>'1': An output trigger is generated after a single 1D transfer or a memory copy transfer.</p> <ul style="list-style-type: none"> - If the descriptor type is 'single', the output trigger is generated after a single transfer. - If the descriptor type is '1D' or '2D', the output trigger is generated after the execution of a 1D transfer. - If the descriptor type is 'memory copy', the output trigger is generated after the execution of a memory copy transfer. - If the descriptor type is 'scatter', the output trigger is generated after the execution of a scatter transfer. <p>'2': An output trigger is generated after the execution of the current descriptor.</p> <p>'3': An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor's DESCR_NEXT_PTR.ADDR is '0'.</p> |
| 6:7 | TR_IN_TYPE | R | W | Undefined | <p>Specifies the input trigger type (not to be confused with the descriptor type):</p> <p>'0': A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D.</p> <p>'1': A trigger results in the execution of a single 1D transfer.</p> <ul style="list-style-type: none"> - If the descriptor type is 'single', the trigger results in the execution of a single transfer. - If the descriptor type is '1D' or '2D', the trigger results in the execution of a 1D transfer. - If the descriptor type is 'memory copy', the trigger results in the execution of a memory copy transfer. - If the descriptor type is 'scatter', the trigger results in the execution of an scatter transfer. <p>'2': A trigger results in the execution of the current descriptor.</p> <p>'3': A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|---|
| 8 | DATA_PREFETCH | R | W | Undefined | <p>Source data prefetch:</p> <p>'0': No source data prefetch. Source data transfers are only initiated AFTER the input trigger is activated.</p> <p>'1': Source data prefetch. Source data transfers are initiated as soon as the channel is enabled, the current descriptor pointer is NOT '0' and there is space available in the channel's data FIFO. When the input trigger is activated, the trigger can initiate destination data transfers with data that is already in the channel's data FIFO. This effectively shortens the initial delay of the data transfer.</p> <p>Note: data prefetch should be used with care, to ensure that data coherency is guaranteed and that prefetches do not cause undesired side effects.</p> |
| 16:17 | DATA_SIZE | R | W | Undefined | <p>Specifies the data element size:</p> <p>'0': Byte (8 bits).</p> <p>'1': Halfword (16 bits).</p> <p>'2': Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made '0'). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made '0'). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made '0'). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made '0'). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. <p>Note: this field is not used for a 'memory copy' descriptor type. Note: this field must be set to '2' for a 'initialization' descriptor type.</p> |
| 24 | CH_DISABLE | R | W | Undefined | <p>Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value):</p> <p>'0': Channel is not disabled.</p> <p>'1': Channel is disabled.</p> |
| 26 | SRC_TRANSFER_SIZE | R | W | Undefined | <p>Specifies the bus transfer size to the source location:</p> <p>'0': As specified by DATA_SIZE.</p> <p>'1': Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Note: this field is not used for a 'memory copy' descriptor type. Note: this field must be set to '1' for a 'scatter' descriptor type.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|---|
| 27 | DST_TRANSFER_SIZE | R | W | Undefined | <p>Specifies the bus transfer size to the destination location:</p> <p>'0': As specified by DATA_SIZE.</p> <p>'1': Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Note: this field is not used for a 'memory copy' descriptor type. Note: this field must be set to '1' for a 'scatter' descriptor type.</p> |
| 28:30 | DESCR_TYPE | R | W | Undefined | <p>Specifies the descriptor type (not to be confused with the trigger type):</p> <p>'0': Single transfer.</p> <p>The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are NOT present. The DESCR_NEXT_PTR is at offset 0x0c.</p> <p>'1': 1D transfer.</p> <p>The DESCR_X_SIZE and DESCR_X_INCR registers are present, the DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A 1D transfer consists out of DESCR_X_SIZE.X_COUNT+1 single transfers. The DESCR_NEXT_PTR is at offset 0x14.</p> <p>'2': 2D transfer.</p> <p>The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are present. A 2D transfer consists of $(DESCR_X_SIZE.X_COUNT+1) \times (DESCR_Y_SIZE.Y_COUNT+1)$ single transfers. The DESCR_NEXT_PTR is at offset 0x1c.</p> <p>'3': Memory copy.</p> <p>The DESCR_X_SIZE register is present, the DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A memory copy transfer copies DESCR_X_SIZE.X_COUNT+1 Bytes and may use Byte, halfword and word transfers. The DESCR_NEXT_PTR is at offset 0x10.</p> <p>'4': Scatter transfer. The DESCR_X_SIZE register is present, the DESCR_DST, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present.</p> <p>'5'-'7': Undefined.</p> <p>After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to '0'.</p> |

8.5.3.9 DMAC_CH_DESCR_SRC

Description: Channel descriptor source
Address: 0x402A1064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_SRC of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|----------------------------------|
| 0:31 | ADDR | R | W | Undefined | Base address of source location. |

8.5.3.10 DMAC_CH_DESCR_DST

Description: Channel descriptor destination
Address: 0x402A1068
Offset: 0x68
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_DST of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------------------------|
| 0:31 | ADDR | R | W | Undefined | Base address of destination location. |

8.5.3.11 DMAC_CH_DESCR_X_SIZE

Description: Channel descriptor X size
Address: 0x402A106C
Offset: 0x6C
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_X_SIZE of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | X_COUNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | X_COUNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:15 | X_COUNT | R | W | Undefined | <p>Number of iterations (minus 1) of the 'X loop' (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations.</p> <p>For the 'memory copy' descriptor type, (X_COUNT + 1) is the number of transferred Bytes. For the 'scatter' descriptor type, ceiling(X_COUNT/2) is the number of (address, write data) initialization pairs processed.</p> |

8.5.3.12 DMAC_CH_DESCR_X_INCR

Description: Channel descriptor X increment
Address: 0x402A1070
Offset: 0x70
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_X_INCR of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | SRC_X [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | SRC_X [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DST_X [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DST_X [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 0:15 | SRC_X | R | W | Undefined | Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is '0', the source address is not incremented. This is useful for reading from RX FIFO structures. |
| 16:31 | DST_X | R | W | Undefined | Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is '0', the destination address is not incremented. This is useful for writing to TX FIFO structures. |

8.5.3.13 DMAC_CH_DESCR_Y_SIZE

Description: Channel descriptor Y size
Address: 0x402A1074
Offset: 0x74
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_Y_SIZE of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | Y_COUNT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | Y_COUNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:15 | Y_COUNT | R | W | Undefined | Number of iterations (minus 1) of the 'Y loop' (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations. |

8.5.3.14 DMAC_CH_DESCR_Y_INCR

Description: Channel descriptor Y increment
Address: 0x402A1078
Offset: 0x78
Retention: Not Retained
IsDeepSleep: No
Comment: Copy of DESCR_Y_INCR of the currently active descriptor.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | SRC_Y [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | SRC_Y [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DST_Y [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DST_Y [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 0:15 | SRC_Y | R | W | Undefined | Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. |
| 16:31 | DST_Y | R | W | Undefined | Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. |

8.5.3.15 DMAC_CH_DESCR_NEXT

Description: Channel descriptor next pointer

Address: 0x402A107C

Offset: 0x7C

Retention: Not Retained

IsDeepSleep: No

Comment: Copy of DESCR_NEXT_PTR of the currently active descriptor. For a single transfer descriptor type, this register is at offset 0x0c. For a 1D transfer descriptor type, this register is at offset 0x14. For a 2D transfer descriptor type, this register is at offset 0x1c. For a memory copy transfer descriptor type, this register is at offset 0x10. For a scatter transfer descriptor type, this register is at offset 0x0c.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | PTR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | PTR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 2:31 | PTR | R | W | Undefined | Address of next descriptor in descriptor list. When this field is '0', this is the last descriptor in the descriptor list. |

8.5.3.16 DMAC_CH_INTR

Description: Interrupt
Address: 0x402A1080
Offset: 0x80
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|--------------------------|---------------------|-----------------|-----------------|---------------------|---------------------|------------------|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|------|------|-----------------|---|
| 0 | COMPLETION | RW1C | RW1S | 0 | Activated (set to '1') on completion of data transfer(s) as specified by the descriptor's CH_DESCR_CTL.INTR_TYPE. |
| 1 | SRC_BUS_ERROR | RW1C | RW1S | 0 | Activated (set to '1') on a bus error for a load from the source. |
| 2 | DST_BUS_ERROR | RW1C | RW1S | 0 | Activated (set to '1') on a bus error for a store to the destination. |
| 3 | SRC_MISAL | RW1C | RW1S | 0 | Activated (set to '1') on a misalignment of the source address. |
| 4 | DST_MISAL | RW1C | RW1S | 0 | Activated (set to '1') on a misalignment of the destination address. |
| 5 | CURR_PTR_NULL | RW1C | RW1S | 0 | Activated (set to '1') when the channel is enabled (CH_CTL.ENABLED is '1') and CH_CURR_PTR is '0'. |
| 6 | ACTIVE_CH_DISABLED | RW1C | RW1S | 0 | Activated (set to '1') if the channel is disabled by SW (accidentally/incorrectly) when the data transfer engine is busy. |
| 7 | DESCR_BUS_ERROR | RW1C | RW1S | 0 | Activated (set to '1') on a bus error for a load of the descriptor. |

8.5.3.17 DMAC_CH_INTR_SET

Description: Interrupt set
Address: 0x402A1084
Offset: 0x84
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|--------------------------|---------------------|-----------------|-----------------|---------------------|---------------------|------------------|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|------|----|-----------------|--|
| 0 | COMPLETION | RW1S | A | 0 | Write this field with '1' to set INTR.COMPLETION field to '1' (a write of '0' has no effect). |
| 1 | SRC_BUS_ERROR | RW1S | A | 0 | Write this field with '1' to set INTR.SRC_BUS_ERROR field to '1' (a write of '0' has no effect). |
| 2 | DST_BUS_ERROR | RW1S | A | 0 | Write this field with '1' to set INTR.DST_BUS_ERROR field to '1' (a write of '0' has no effect). |
| 3 | SRC_MISAL | RW1S | A | 0 | Write this field with '1' to set INTR.SRC_MISAL field to '1' (a write of '0' has no effect). |
| 4 | DST_MISAL | RW1S | A | 0 | Write this field with '1' to set INTR.DST_MISAL field to '1' (a write of '0' has no effect). |
| 5 | CURR_PTR_NULL | RW1S | A | 0 | Write this field with '1' to set INTR.CURR_PTR_NULL field to '1' (a write of '0' has no effect). |
| 6 | ACTIVE_CH_DISABLED | RW1S | A | 0 | Write this field with '1' to set INTR.ACT_CH_DISABLED field to '1' (a write of '0' has no effect). |
| 7 | DESCR_BUS_ERROR | RW1S | A | 0 | Write this field with '1' to set INTR.DESCR_BUS_ERROR field to '1' (a write of '0' has no effect). |

8.5.3.18 DMAC_CH_INTR_MASK

Description: Interrupt mask
Address: 0x402A1088
Offset: 0x88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|--------------------------|---------------------|-----------------|-----------------|---------------------|---------------------|------------------|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|----|----|-----------------|---|
| 0 | COMPLETION | RW | R | 0 | Mask for INTR.COMPLETION interrupt. |
| 1 | SRC_BUS_ERROR | RW | R | 0 | Mask for INTR.SRC_BUS_ERROR interrupt. |
| 2 | DST_BUS_ERROR | RW | R | 0 | Mask for INTR.DST_BUS_ERROR interrupt. |
| 3 | SRC_MISAL | RW | R | 0 | Mask for INTR.SRC_MISAL interrupt. |
| 4 | DST_MISAL | RW | R | 0 | Mask for INTR.DST_MISAL interrupt. |
| 5 | CURR_PTR_NULL | RW | R | 0 | Mask for INTR.CURR_PTR_NULL interrupt. |
| 6 | ACTIVE_CH_DISABLED | RW | R | 0 | Mask for INTR.ACTIVE_CH_DISABLED interrupt. |
| 7 | DESCR_BUS_ERROR | RW | R | 0 | Mask for INTR.DESCR_BUS_ERROR interrupt. |

8.5.3.19 DMAC_CH_INTR_MASKED

Description: Interrupt masked

Address: 0x402A108C

Offset: 0x8C

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|--------------------------|---------------------|-----------------|-----------------|---------------------|---------------------|------------------|
| Name | DESCR_BUS_ERROR [7:7] | ACTIVE_CH_DISABLED [6:6] | CURR_PTR_NULL [5:5] | DST_MISAL [4:4] | SRC_MISAL [3:3] | DST_BUS_ERROR [2:2] | SRC_BUS_ERROR [1:1] | COMPLETION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|----|----|-----------------|---|
| 0 | COMPLETION | R | W | 0 | Logical and of corresponding INTR.COMPLETION and INTR_MASK.COMPLETION fields. |
| 1 | SRC_BUS_ERROR | R | W | 0 | Logical and of corresponding INTR.SRC_BUS_ERROR and INTR_MASK.SRC_BUS_ERROR fields. |
| 2 | DST_BUS_ERROR | R | W | 0 | Logical and of corresponding INTR.DST_BUS_ERROR and INTR_MASK.DST_BUS_ERROR fields. |
| 3 | SRC_MISAL | R | W | 0 | Logical and of corresponding INTR.SRC_MISAL and INTR_MASK.SRC_MISAL fields. |
| 4 | DST_MISAL | R | W | 0 | Logical and of corresponding INTR.DST_MISAL and INTR_MASK.DST_MISAL fields. |
| 5 | CURR_PTR_NULL | R | W | 0 | Logical and of corresponding INTR.CURR_PTR_NULL and INTR_MASK.CURR_PTR_NULL fields. |
| 6 | ACTIVE_CH_DISABLED | R | W | 0 | Logical and of corresponding INTR.ACTIVE_CH_DISABLED and INTR_MASK.ACTIVE_CH_DISABLED fields. |
| 7 | DESCR_BUS_ERROR | R | W | 0 | Logical and of corresponding INTR.DESCR_BUS_ERROR and INTR_MASK.DESCR_BUS_ERROR fields. |

9 DW

9.1 DW 0

| | |
|---------------------|---------------------|
| Description | Datawire Controller |
| Base Address | 0x40280000 |
| Size | 0x10000 |
| Slave Num | MMIO2 - 7 |

9.1.1 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|----------------------------------|
| DW0_CTL0 | 0x40280000 | FULL | Control |
| DW0_STATUS0 | 0x40280004 | FULL | Status |
| DW0_ACT_DESCR_CTL0 | 0x40280020 | FULL | Active descriptor control |
| DW0_ACT_DESCR_SRC0 | 0x40280024 | FULL | Active descriptor source |
| DW0_ACT_DESCR_DST0 | 0x40280028 | FULL | Active descriptor destination |
| DW0_ACT_DESCR_X_CTL0 | 0x40280030 | FULL | Active descriptor X loop control |
| DW0_ACT_DESCR_Y_CTL0 | 0x40280034 | FULL | Active descriptor Y loop control |
| DW0_ACT_DESCR_NEXT_PTR0 | 0x40280038 | FULL | Active descriptor next pointer |
| DW0_ACT_SRC0 | 0x40280040 | FULL | Active source |
| DW0_ACT_DST0 | 0x40280044 | FULL | Active destination |
| DW0_ECC_CTL0 | 0x40280080 | FULL | ECC control |
| DW0_CRC_CTL0 | 0x40280100 | FULL | CRC control |
| DW0_CRC_DATA_CTL0 | 0x40280110 | FULL | CRC data control |
| DW0_CRC_POL_CTL0 | 0x40280120 | FULL | CRC polynomial control |
| DW0_CRC_LFSR_CTL0 | 0x40280130 | FULL | CRC LFSR control |
| DW0_CRC_REM_CTL0 | 0x40280140 | FULL | CRC remainder control |
| DW0_CRC_REM_RESULT0 | 0x40280148 | FULL | CRC remainder result |

9.1.1.1 CH_STRUCT 0

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT0_CH_CTL | 0x40288000 | FULL | Channel control |
| DW0_CH_STRUCT0_CH_STATUS | 0x40288004 | FULL | Channel status |
| DW0_CH_STRUCT0_CH_IDX | 0x40288008 | FULL | Channel current indices |
| DW0_CH_STRUCT0_CH_CURR_PTR | 0x4028800C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT0_INTR | 0x40288010 | FULL | Interrupt |
| DW0_CH_STRUCT0_INTR_SET | 0x40288014 | FULL | Interrupt set |
| DW0_CH_STRUCT0_INTR_MASK | 0x40288018 | FULL | Interrupt mask |
| DW0_CH_STRUCT0_INTR_MASKED | 0x4028801C | FULL | Interrupt masked |
| DW0_CH_STRUCT0_SRAM_DATA0 | 0x40288020 | FULL | SRAM data 0 |
| DW0_CH_STRUCT0_SRAM_DATA1 | 0x40288024 | FULL | SRAM data 1 |
| DW0_CH_STRUCT0_TR_CMD | 0x40288028 | FULL | Channel software trigger |

9.1.1.2 CH_STRUCT 1

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT1_CH_CTL | 0x40288040 | FULL | Channel control |
| DW0_CH_STRUCT1_CH_STATUS | 0x40288044 | FULL | Channel status |
| DW0_CH_STRUCT1_CH_IDX | 0x40288048 | FULL | Channel current indices |
| DW0_CH_STRUCT1_CH_CURR_PTR | 0x4028804C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT1_INTR | 0x40288050 | FULL | Interrupt |
| DW0_CH_STRUCT1_INTR_SET | 0x40288054 | FULL | Interrupt set |
| DW0_CH_STRUCT1_INTR_MASK | 0x40288058 | FULL | Interrupt mask |
| DW0_CH_STRUCT1_INTR_MASKED | 0x4028805C | FULL | Interrupt masked |
| DW0_CH_STRUCT1_SRAM_DATA0 | 0x40288060 | FULL | SRAM data 0 |
| DW0_CH_STRUCT1_SRAM_DATA1 | 0x40288064 | FULL | SRAM data 1 |
| DW0_CH_STRUCT1_TR_CMD | 0x40288068 | FULL | Channel software trigger |

9.1.1.3 CH_STRUCT 2

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT2_CH_CTL | 0x40288080 | FULL | Channel control |
| DW0_CH_STRUCT2_CH_STATUS | 0x40288084 | FULL | Channel status |
| DW0_CH_STRUCT2_CH_IDX | 0x40288088 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT2_CH_CURR_PTR | 0x4028808C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT2_INTR | 0x40288090 | FULL | Interrupt |
| DW0_CH_STRUCT2_INTR_SET | 0x40288094 | FULL | Interrupt set |
| DW0_CH_STRUCT2_INTR_MASK | 0x40288098 | FULL | Interrupt mask |
| DW0_CH_STRUCT2_INTR_MASKED | 0x4028809C | FULL | Interrupt masked |
| DW0_CH_STRUCT2_SRAM_DATA0 | 0x402880A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT2_SRAM_DATA1 | 0x402880A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT2_TR_CMD | 0x402880A8 | FULL | Channel software trigger |

9.1.1.4 CH_STRUCT 3

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT3_CH_CTL | 0x402880C0 | FULL | Channel control |
| DW0_CH_STRUCT3_CH_STATUS | 0x402880C4 | FULL | Channel status |
| DW0_CH_STRUCT3_CH_IDX | 0x402880C8 | FULL | Channel current indices |
| DW0_CH_STRUCT3_CH_CURR_PTR | 0x402880CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT3_INTR | 0x402880D0 | FULL | Interrupt |
| DW0_CH_STRUCT3_INTR_SET | 0x402880D4 | FULL | Interrupt set |
| DW0_CH_STRUCT3_INTR_MASK | 0x402880D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT3_INTR_MASKED | 0x402880DC | FULL | Interrupt masked |
| DW0_CH_STRUCT3_SRAM_DATA0 | 0x402880E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT3_SRAM_DATA1 | 0x402880E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT3_TR_CMD | 0x402880E8 | FULL | Channel software trigger |

9.1.1.5 CH_STRUCT 4

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT4_CH_CTL | 0x40288100 | FULL | Channel control |
| DW0_CH_STRUCT4_CH_STATUS | 0x40288104 | FULL | Channel status |
| DW0_CH_STRUCT4_CH_IDX | 0x40288108 | FULL | Channel current indices |
| DW0_CH_STRUCT4_CH_CURR_PTR | 0x4028810C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT4_INTR | 0x40288110 | FULL | Interrupt |
| DW0_CH_STRUCT4_INTR_SET | 0x40288114 | FULL | Interrupt set |
| DW0_CH_STRUCT4_INTR_MASK | 0x40288118 | FULL | Interrupt mask |
| DW0_CH_STRUCT4_INTR_MASKED | 0x4028811C | FULL | Interrupt masked |
| DW0_CH_STRUCT4_SRAM_DATA0 | 0x40288120 | FULL | SRAM data 0 |
| DW0_CH_STRUCT4_SRAM_DATA1 | 0x40288124 | FULL | SRAM data 1 |
| DW0_CH_STRUCT4_TR_CMD | 0x40288128 | FULL | Channel software trigger |

9.1.1.6 CH_STRUCT 5

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT5_CH_CTL | 0x40288140 | FULL | Channel control |
| DW0_CH_STRUCT5_CH_STATUS | 0x40288144 | FULL | Channel status |
| DW0_CH_STRUCT5_CH_IDX | 0x40288148 | FULL | Channel current indices |
| DW0_CH_STRUCT5_CH_CURR_PTR | 0x4028814C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT5_INTR | 0x40288150 | FULL | Interrupt |
| DW0_CH_STRUCT5_INTR_SET | 0x40288154 | FULL | Interrupt set |
| DW0_CH_STRUCT5_INTR_MASK | 0x40288158 | FULL | Interrupt mask |
| DW0_CH_STRUCT5_INTR_MASKED | 0x4028815C | FULL | Interrupt masked |
| DW0_CH_STRUCT5_SRAM_DATA0 | 0x40288160 | FULL | SRAM data 0 |
| DW0_CH_STRUCT5_SRAM_DATA1 | 0x40288164 | FULL | SRAM data 1 |
| DW0_CH_STRUCT5_TR_CMD | 0x40288168 | FULL | Channel software trigger |

9.1.1.7 CH_STRUCT 6

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT6_CH_CTL | 0x40288180 | FULL | Channel control |
| DW0_CH_STRUCT6_CH_STATUS | 0x40288184 | FULL | Channel status |
| DW0_CH_STRUCT6_CH_IDX | 0x40288188 | FULL | Channel current indices |
| DW0_CH_STRUCT6_CH_CURR_PTR | 0x4028818C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT6_INTR | 0x40288190 | FULL | Interrupt |
| DW0_CH_STRUCT6_INTR_SET | 0x40288194 | FULL | Interrupt set |
| DW0_CH_STRUCT6_INTR_MASK | 0x40288198 | FULL | Interrupt mask |
| DW0_CH_STRUCT6_INTR_MASKED | 0x4028819C | FULL | Interrupt masked |
| DW0_CH_STRUCT6_SRAM_DATA0 | 0x402881A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT6_SRAM_DATA1 | 0x402881A4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT6_TR_CMD | 0x402881A8 | FULL | Channel software trigger |

9.1.1.8 CH_STRUCT 7

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT7_CH_CTL | 0x402881C0 | FULL | Channel control |
| DW0_CH_STRUCT7_CH_STATUS | 0x402881C4 | FULL | Channel status |
| DW0_CH_STRUCT7_CH_IDX | 0x402881C8 | FULL | Channel current indices |
| DW0_CH_STRUCT7_CH_CURR_PTR | 0x402881CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT7_INTR | 0x402881D0 | FULL | Interrupt |
| DW0_CH_STRUCT7_INTR_SET | 0x402881D4 | FULL | Interrupt set |
| DW0_CH_STRUCT7_INTR_MASK | 0x402881D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT7_INTR_MASKED | 0x402881DC | FULL | Interrupt masked |
| DW0_CH_STRUCT7_SRAM_DATA0 | 0x402881E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT7_SRAM_DATA1 | 0x402881E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT7_TR_CMD | 0x402881E8 | FULL | Channel software trigger |

9.1.1.9 CH_STRUCT 8

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT8_CH_CTL | 0x40288200 | FULL | Channel control |
| DW0_CH_STRUCT8_CH_STATUS | 0x40288204 | FULL | Channel status |
| DW0_CH_STRUCT8_CH_IDX | 0x40288208 | FULL | Channel current indices |
| DW0_CH_STRUCT8_CH_CURR_PTR | 0x4028820C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT8_INTR | 0x40288210 | FULL | Interrupt |
| DW0_CH_STRUCT8_INTR_SET | 0x40288214 | FULL | Interrupt set |
| DW0_CH_STRUCT8_INTR_MASK | 0x40288218 | FULL | Interrupt mask |
| DW0_CH_STRUCT8_INTR_MASKED | 0x4028821C | FULL | Interrupt masked |
| DW0_CH_STRUCT8_SRAM_DATA0 | 0x40288220 | FULL | SRAM data 0 |
| DW0_CH_STRUCT8_SRAM_DATA1 | 0x40288224 | FULL | SRAM data 1 |
| DW0_CH_STRUCT8_TR_CMD | 0x40288228 | FULL | Channel software trigger |

9.1.1.10 CH_STRUCT 9

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT9_CH_CTL | 0x40288240 | FULL | Channel control |
| DW0_CH_STRUCT9_CH_STATUS | 0x40288244 | FULL | Channel status |
| DW0_CH_STRUCT9_CH_IDX | 0x40288248 | FULL | Channel current indices |
| DW0_CH_STRUCT9_CH_CURR_PTR | 0x4028824C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT9_INTR | 0x40288250 | FULL | Interrupt |
| DW0_CH_STRUCT9_INTR_SET | 0x40288254 | FULL | Interrupt set |
| DW0_CH_STRUCT9_INTR_MASK | 0x40288258 | FULL | Interrupt mask |
| DW0_CH_STRUCT9_INTR_MASKED | 0x4028825C | FULL | Interrupt masked |
| DW0_CH_STRUCT9_SRAM_DATA0 | 0x40288260 | FULL | SRAM data 0 |
| DW0_CH_STRUCT9_SRAM_DATA1 | 0x40288264 | FULL | SRAM data 1 |
| DW0_CH_STRUCT9_TR_CMD | 0x40288268 | FULL | Channel software trigger |

9.1.1.11 CH_STRUCT 10

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT10_CH_CTL | 0x40288280 | FULL | Channel control |
| DW0_CH_STRUCT10_CH_STATUS | 0x40288284 | FULL | Channel status |
| DW0_CH_STRUCT10_CH_IDX | 0x40288288 | FULL | Channel current indices |
| DW0_CH_STRUCT10_CH_CURR_PTR | 0x4028828C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT10_INTR | 0x40288290 | FULL | Interrupt |
| DW0_CH_STRUCT10_INTR_SET | 0x40288294 | FULL | Interrupt set |
| DW0_CH_STRUCT10_INTR_MASK | 0x40288298 | FULL | Interrupt mask |
| DW0_CH_STRUCT10_INTR_MASKED | 0x4028829C | FULL | Interrupt masked |
| DW0_CH_STRUCT10_SRAM_DATA0 | 0x402882A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT10_SRAM_DATA1 | 0x402882A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT10_TR_CMD | 0x402882A8 | FULL | Channel software trigger |

9.1.1.12 CH_STRUCT 11

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT11_CH_CTL | 0x402882C0 | FULL | Channel control |
| DW0_CH_STRUCT11_CH_STATUS | 0x402882C4 | FULL | Channel status |
| DW0_CH_STRUCT11_CH_IDX | 0x402882C8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT11_CH_CURR_PTR | 0x402882CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT11_INTR | 0x402882D0 | FULL | Interrupt |
| DW0_CH_STRUCT11_INTR_SET | 0x402882D4 | FULL | Interrupt set |
| DW0_CH_STRUCT11_INTR_MASK | 0x402882D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT11_INTR_MASKED | 0x402882DC | FULL | Interrupt masked |
| DW0_CH_STRUCT11_SRAM_DATA0 | 0x402882E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT11_SRAM_DATA1 | 0x402882E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT11_TR_CMD | 0x402882E8 | FULL | Channel software trigger |

9.1.1.13 CH_STRUCT 12

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT12_CH_CTL | 0x40288300 | FULL | Channel control |
| DW0_CH_STRUCT12_CH_STATUS | 0x40288304 | FULL | Channel status |
| DW0_CH_STRUCT12_CH_IDX | 0x40288308 | FULL | Channel current indices |
| DW0_CH_STRUCT12_CH_CURR_PTR | 0x4028830C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT12_INTR | 0x40288310 | FULL | Interrupt |
| DW0_CH_STRUCT12_INTR_SET | 0x40288314 | FULL | Interrupt set |
| DW0_CH_STRUCT12_INTR_MASK | 0x40288318 | FULL | Interrupt mask |
| DW0_CH_STRUCT12_INTR_MASKED | 0x4028831C | FULL | Interrupt masked |
| DW0_CH_STRUCT12_SRAM_DATA0 | 0x40288320 | FULL | SRAM data 0 |
| DW0_CH_STRUCT12_SRAM_DATA1 | 0x40288324 | FULL | SRAM data 1 |
| DW0_CH_STRUCT12_TR_CMD | 0x40288328 | FULL | Channel software trigger |

9.1.1.14 CH_STRUCT 13

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT13_CH_CTL | 0x40288340 | FULL | Channel control |
| DW0_CH_STRUCT13_CH_STATUS | 0x40288344 | FULL | Channel status |
| DW0_CH_STRUCT13_CH_IDX | 0x40288348 | FULL | Channel current indices |
| DW0_CH_STRUCT13_CH_CURR_PTR | 0x4028834C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT13_INTR | 0x40288350 | FULL | Interrupt |
| DW0_CH_STRUCT13_INTR_SET | 0x40288354 | FULL | Interrupt set |
| DW0_CH_STRUCT13_INTR_MASK | 0x40288358 | FULL | Interrupt mask |
| DW0_CH_STRUCT13_INTR_MASKED | 0x4028835C | FULL | Interrupt masked |
| DW0_CH_STRUCT13_SRAM_DATA0 | 0x40288360 | FULL | SRAM data 0 |
| DW0_CH_STRUCT13_SRAM_DATA1 | 0x40288364 | FULL | SRAM data 1 |
| DW0_CH_STRUCT13_TR_CMD | 0x40288368 | FULL | Channel software trigger |

9.1.1.15 CH_STRUCT 14

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT14_CH_CTL | 0x40288380 | FULL | Channel control |
| DW0_CH_STRUCT14_CH_STATUS | 0x40288384 | FULL | Channel status |
| DW0_CH_STRUCT14_CH_IDX | 0x40288388 | FULL | Channel current indices |
| DW0_CH_STRUCT14_CH_CURR_PTR | 0x4028838C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT14_INTR | 0x40288390 | FULL | Interrupt |
| DW0_CH_STRUCT14_INTR_SET | 0x40288394 | FULL | Interrupt set |
| DW0_CH_STRUCT14_INTR_MASK | 0x40288398 | FULL | Interrupt mask |
| DW0_CH_STRUCT14_INTR_MASKED | 0x4028839C | FULL | Interrupt masked |
| DW0_CH_STRUCT14_SRAM_DATA0 | 0x402883A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT14_SRAM_DATA1 | 0x402883A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT14_TR_CMD | 0x402883A8 | FULL | Channel software trigger |

9.1.1.16 CH_STRUCT 15

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT15_CH_CTL | 0x402883C0 | FULL | Channel control |
| DW0_CH_STRUCT15_CH_STATUS | 0x402883C4 | FULL | Channel status |
| DW0_CH_STRUCT15_CH_IDX | 0x402883C8 | FULL | Channel current indices |
| DW0_CH_STRUCT15_CH_CURR_PTR | 0x402883CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT15_INTR | 0x402883D0 | FULL | Interrupt |
| DW0_CH_STRUCT15_INTR_SET | 0x402883D4 | FULL | Interrupt set |
| DW0_CH_STRUCT15_INTR_MASK | 0x402883D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT15_INTR_MASKED | 0x402883DC | FULL | Interrupt masked |
| DW0_CH_STRUCT15_SRAM_DATA0 | 0x402883E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT15_SRAM_DATA1 | 0x402883E4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT15_TR_CMD | 0x402883E8 | FULL | Channel software trigger |

9.1.1.17 CH_STRUCT 16

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT16_CH_CTL | 0x40288400 | FULL | Channel control |
| DW0_CH_STRUCT16_CH_STATUS | 0x40288404 | FULL | Channel status |
| DW0_CH_STRUCT16_CH_IDX | 0x40288408 | FULL | Channel current indices |
| DW0_CH_STRUCT16_CH_CURR_PTR | 0x4028840C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT16_INTR | 0x40288410 | FULL | Interrupt |
| DW0_CH_STRUCT16_INTR_SET | 0x40288414 | FULL | Interrupt set |
| DW0_CH_STRUCT16_INTR_MASK | 0x40288418 | FULL | Interrupt mask |
| DW0_CH_STRUCT16_INTR_MASKED | 0x4028841C | FULL | Interrupt masked |
| DW0_CH_STRUCT16_SRAM_DATA0 | 0x40288420 | FULL | SRAM data 0 |
| DW0_CH_STRUCT16_SRAM_DATA1 | 0x40288424 | FULL | SRAM data 1 |
| DW0_CH_STRUCT16_TR_CMD | 0x40288428 | FULL | Channel software trigger |

9.1.1.18 CH_STRUCT 17

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT17_CH_CTL | 0x40288440 | FULL | Channel control |
| DW0_CH_STRUCT17_CH_STATUS | 0x40288444 | FULL | Channel status |
| DW0_CH_STRUCT17_CH_IDX | 0x40288448 | FULL | Channel current indices |
| DW0_CH_STRUCT17_CH_CURR_PTR | 0x4028844C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT17_INTR | 0x40288450 | FULL | Interrupt |
| DW0_CH_STRUCT17_INTR_SET | 0x40288454 | FULL | Interrupt set |
| DW0_CH_STRUCT17_INTR_MASK | 0x40288458 | FULL | Interrupt mask |
| DW0_CH_STRUCT17_INTR_MASKED | 0x4028845C | FULL | Interrupt masked |
| DW0_CH_STRUCT17_SRAM_DATA0 | 0x40288460 | FULL | SRAM data 0 |
| DW0_CH_STRUCT17_SRAM_DATA1 | 0x40288464 | FULL | SRAM data 1 |
| DW0_CH_STRUCT17_TR_CMD | 0x40288468 | FULL | Channel software trigger |

9.1.1.19 CH_STRUCT 18

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT18_CH_CTL | 0x40288480 | FULL | Channel control |
| DW0_CH_STRUCT18_CH_STATUS | 0x40288484 | FULL | Channel status |
| DW0_CH_STRUCT18_CH_IDX | 0x40288488 | FULL | Channel current indices |
| DW0_CH_STRUCT18_CH_CURR_PTR | 0x4028848C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT18_INTR | 0x40288490 | FULL | Interrupt |
| DW0_CH_STRUCT18_INTR_SET | 0x40288494 | FULL | Interrupt set |
| DW0_CH_STRUCT18_INTR_MASK | 0x40288498 | FULL | Interrupt mask |
| DW0_CH_STRUCT18_INTR_MASKED | 0x4028849C | FULL | Interrupt masked |
| DW0_CH_STRUCT18_SRAM_DATA0 | 0x402884A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT18_SRAM_DATA1 | 0x402884A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT18_TR_CMD | 0x402884A8 | FULL | Channel software trigger |

9.1.1.20 CH_STRUCT 19

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT19_CH_CTL | 0x402884C0 | FULL | Channel control |
| DW0_CH_STRUCT19_CH_STATUS | 0x402884C4 | FULL | Channel status |
| DW0_CH_STRUCT19_CH_IDX | 0x402884C8 | FULL | Channel current indices |
| DW0_CH_STRUCT19_CH_CURR_PTR | 0x402884CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT19_INTR | 0x402884D0 | FULL | Interrupt |
| DW0_CH_STRUCT19_INTR_SET | 0x402884D4 | FULL | Interrupt set |
| DW0_CH_STRUCT19_INTR_MASK | 0x402884D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT19_INTR_MASKED | 0x402884DC | FULL | Interrupt masked |
| DW0_CH_STRUCT19_SRAM_DATA0 | 0x402884E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT19_SRAM_DATA1 | 0x402884E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT19_TR_CMD | 0x402884E8 | FULL | Channel software trigger |

9.1.1.21 CH_STRUCT 20

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT20_CH_CTL | 0x40288500 | FULL | Channel control |
| DW0_CH_STRUCT20_CH_STATUS | 0x40288504 | FULL | Channel status |
| DW0_CH_STRUCT20_CH_IDX | 0x40288508 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT20_CH_CURR_PTR | 0x4028850C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT20_INTR | 0x40288510 | FULL | Interrupt |
| DW0_CH_STRUCT20_INTR_SET | 0x40288514 | FULL | Interrupt set |
| DW0_CH_STRUCT20_INTR_MASK | 0x40288518 | FULL | Interrupt mask |
| DW0_CH_STRUCT20_INTR_MASKED | 0x4028851C | FULL | Interrupt masked |
| DW0_CH_STRUCT20_SRAM_DATA0 | 0x40288520 | FULL | SRAM data 0 |
| DW0_CH_STRUCT20_SRAM_DATA1 | 0x40288524 | FULL | SRAM data 1 |
| DW0_CH_STRUCT20_TR_CMD | 0x40288528 | FULL | Channel software trigger |

9.1.1.22 CH_STRUCT 21

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT21_CH_CTL | 0x40288540 | FULL | Channel control |
| DW0_CH_STRUCT21_CH_STATUS | 0x40288544 | FULL | Channel status |
| DW0_CH_STRUCT21_CH_IDX | 0x40288548 | FULL | Channel current indices |
| DW0_CH_STRUCT21_CH_CURR_PTR | 0x4028854C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT21_INTR | 0x40288550 | FULL | Interrupt |
| DW0_CH_STRUCT21_INTR_SET | 0x40288554 | FULL | Interrupt set |
| DW0_CH_STRUCT21_INTR_MASK | 0x40288558 | FULL | Interrupt mask |
| DW0_CH_STRUCT21_INTR_MASKED | 0x4028855C | FULL | Interrupt masked |
| DW0_CH_STRUCT21_SRAM_DATA0 | 0x40288560 | FULL | SRAM data 0 |
| DW0_CH_STRUCT21_SRAM_DATA1 | 0x40288564 | FULL | SRAM data 1 |
| DW0_CH_STRUCT21_TR_CMD | 0x40288568 | FULL | Channel software trigger |

9.1.1.23 CH_STRUCT 22

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT22_CH_CTL | 0x40288580 | FULL | Channel control |
| DW0_CH_STRUCT22_CH_STATUS | 0x40288584 | FULL | Channel status |
| DW0_CH_STRUCT22_CH_IDX | 0x40288588 | FULL | Channel current indices |
| DW0_CH_STRUCT22_CH_CURR_PTR | 0x4028858C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT22_INTR | 0x40288590 | FULL | Interrupt |
| DW0_CH_STRUCT22_INTR_SET | 0x40288594 | FULL | Interrupt set |
| DW0_CH_STRUCT22_INTR_MASK | 0x40288598 | FULL | Interrupt mask |
| DW0_CH_STRUCT22_INTR_MASKED | 0x4028859C | FULL | Interrupt masked |
| DW0_CH_STRUCT22_SRAM_DATA0 | 0x402885A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT22_SRAM_DATA1 | 0x402885A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT22_TR_CMD | 0x402885A8 | FULL | Channel software trigger |

9.1.1.24 CH_STRUCT 23

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT23_CH_CTL | 0x402885C0 | FULL | Channel control |
| DW0_CH_STRUCT23_CH_STATUS | 0x402885C4 | FULL | Channel status |
| DW0_CH_STRUCT23_CH_IDX | 0x402885C8 | FULL | Channel current indices |
| DW0_CH_STRUCT23_CH_CURR_PTR | 0x402885CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT23_INTR | 0x402885D0 | FULL | Interrupt |
| DW0_CH_STRUCT23_INTR_SET | 0x402885D4 | FULL | Interrupt set |
| DW0_CH_STRUCT23_INTR_MASK | 0x402885D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT23_INTR_MASKED | 0x402885DC | FULL | Interrupt masked |
| DW0_CH_STRUCT23_SRAM_DATA0 | 0x402885E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT23_SRAM_DATA1 | 0x402885E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT23_TR_CMD | 0x402885E8 | FULL | Channel software trigger |

9.1.1.25 CH_STRUCT 24

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT24_CH_CTL | 0x40288600 | FULL | Channel control |
| DW0_CH_STRUCT24_CH_STATUS | 0x40288604 | FULL | Channel status |
| DW0_CH_STRUCT24_CH_IDX | 0x40288608 | FULL | Channel current indices |
| DW0_CH_STRUCT24_CH_CURR_PTR | 0x4028860C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT24_INTR | 0x40288610 | FULL | Interrupt |
| DW0_CH_STRUCT24_INTR_SET | 0x40288614 | FULL | Interrupt set |
| DW0_CH_STRUCT24_INTR_MASK | 0x40288618 | FULL | Interrupt mask |
| DW0_CH_STRUCT24_INTR_MASKED | 0x4028861C | FULL | Interrupt masked |
| DW0_CH_STRUCT24_SRAM_DATA0 | 0x40288620 | FULL | SRAM data 0 |
| DW0_CH_STRUCT24_SRAM_DATA1 | 0x40288624 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT24_TR_CMD | 0x40288628 | FULL | Channel software trigger |

9.1.1.26 CH_STRUCT 25

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT25_CH_CTL | 0x40288640 | FULL | Channel control |
| DW0_CH_STRUCT25_CH_STATUS | 0x40288644 | FULL | Channel status |
| DW0_CH_STRUCT25_CH_IDX | 0x40288648 | FULL | Channel current indices |
| DW0_CH_STRUCT25_CH_CURR_PTR | 0x4028864C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT25_INTR | 0x40288650 | FULL | Interrupt |
| DW0_CH_STRUCT25_INTR_SET | 0x40288654 | FULL | Interrupt set |
| DW0_CH_STRUCT25_INTR_MASK | 0x40288658 | FULL | Interrupt mask |
| DW0_CH_STRUCT25_INTR_MASKED | 0x4028865C | FULL | Interrupt masked |
| DW0_CH_STRUCT25_SRAM_DATA0 | 0x40288660 | FULL | SRAM data 0 |
| DW0_CH_STRUCT25_SRAM_DATA1 | 0x40288664 | FULL | SRAM data 1 |
| DW0_CH_STRUCT25_TR_CMD | 0x40288668 | FULL | Channel software trigger |

9.1.1.27 CH_STRUCT 26

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT26_CH_CTL | 0x40288680 | FULL | Channel control |
| DW0_CH_STRUCT26_CH_STATUS | 0x40288684 | FULL | Channel status |
| DW0_CH_STRUCT26_CH_IDX | 0x40288688 | FULL | Channel current indices |
| DW0_CH_STRUCT26_CH_CURR_PTR | 0x4028868C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT26_INTR | 0x40288690 | FULL | Interrupt |
| DW0_CH_STRUCT26_INTR_SET | 0x40288694 | FULL | Interrupt set |
| DW0_CH_STRUCT26_INTR_MASK | 0x40288698 | FULL | Interrupt mask |
| DW0_CH_STRUCT26_INTR_MASKED | 0x4028869C | FULL | Interrupt masked |
| DW0_CH_STRUCT26_SRAM_DATA0 | 0x402886A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT26_SRAM_DATA1 | 0x402886A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT26_TR_CMD | 0x402886A8 | FULL | Channel software trigger |

9.1.1.28 CH_STRUCT 27

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT27_CH_CTL | 0x402886C0 | FULL | Channel control |
| DW0_CH_STRUCT27_CH_STATUS | 0x402886C4 | FULL | Channel status |
| DW0_CH_STRUCT27_CH_IDX | 0x402886C8 | FULL | Channel current indices |
| DW0_CH_STRUCT27_CH_CURR_PTR | 0x402886CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT27_INTR | 0x402886D0 | FULL | Interrupt |
| DW0_CH_STRUCT27_INTR_SET | 0x402886D4 | FULL | Interrupt set |
| DW0_CH_STRUCT27_INTR_MASK | 0x402886D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT27_INTR_MASKED | 0x402886DC | FULL | Interrupt masked |
| DW0_CH_STRUCT27_SRAM_DATA0 | 0x402886E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT27_SRAM_DATA1 | 0x402886E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT27_TR_CMD | 0x402886E8 | FULL | Channel software trigger |

9.1.1.29 CH_STRUCT 28

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT28_CH_CTL | 0x40288700 | FULL | Channel control |
| DW0_CH_STRUCT28_CH_STATUS | 0x40288704 | FULL | Channel status |
| DW0_CH_STRUCT28_CH_IDX | 0x40288708 | FULL | Channel current indices |
| DW0_CH_STRUCT28_CH_CURR_PTR | 0x4028870C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT28_INTR | 0x40288710 | FULL | Interrupt |
| DW0_CH_STRUCT28_INTR_SET | 0x40288714 | FULL | Interrupt set |
| DW0_CH_STRUCT28_INTR_MASK | 0x40288718 | FULL | Interrupt mask |
| DW0_CH_STRUCT28_INTR_MASKED | 0x4028871C | FULL | Interrupt masked |
| DW0_CH_STRUCT28_SRAM_DATA0 | 0x40288720 | FULL | SRAM data 0 |
| DW0_CH_STRUCT28_SRAM_DATA1 | 0x40288724 | FULL | SRAM data 1 |
| DW0_CH_STRUCT28_TR_CMD | 0x40288728 | FULL | Channel software trigger |

9.1.1.30 CH_STRUCT 29

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT29_CH_CTL | 0x40288740 | FULL | Channel control |
| DW0_CH_STRUCT29_CH_STATUS | 0x40288744 | FULL | Channel status |
| DW0_CH_STRUCT29_CH_IDX | 0x40288748 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT29_CH_CURR_PTR | 0x4028874C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT29_INTR | 0x40288750 | FULL | Interrupt |
| DW0_CH_STRUCT29_INTR_SET | 0x40288754 | FULL | Interrupt set |
| DW0_CH_STRUCT29_INTR_MASK | 0x40288758 | FULL | Interrupt mask |
| DW0_CH_STRUCT29_INTR_MASKED | 0x4028875C | FULL | Interrupt masked |
| DW0_CH_STRUCT29_SRAM_DATA0 | 0x40288760 | FULL | SRAM data 0 |
| DW0_CH_STRUCT29_SRAM_DATA1 | 0x40288764 | FULL | SRAM data 1 |
| DW0_CH_STRUCT29_TR_CMD | 0x40288768 | FULL | Channel software trigger |

9.1.1.31 CH_STRUCT 30

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT30_CH_CTL | 0x40288780 | FULL | Channel control |
| DW0_CH_STRUCT30_CH_STATUS | 0x40288784 | FULL | Channel status |
| DW0_CH_STRUCT30_CH_IDX | 0x40288788 | FULL | Channel current indices |
| DW0_CH_STRUCT30_CH_CURR_PTR | 0x4028878C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT30_INTR | 0x40288790 | FULL | Interrupt |
| DW0_CH_STRUCT30_INTR_SET | 0x40288794 | FULL | Interrupt set |
| DW0_CH_STRUCT30_INTR_MASK | 0x40288798 | FULL | Interrupt mask |
| DW0_CH_STRUCT30_INTR_MASKED | 0x4028879C | FULL | Interrupt masked |
| DW0_CH_STRUCT30_SRAM_DATA0 | 0x402887A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT30_SRAM_DATA1 | 0x402887A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT30_TR_CMD | 0x402887A8 | FULL | Channel software trigger |

9.1.1.32 CH_STRUCT 31

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT31_CH_CTL | 0x402887C0 | FULL | Channel control |
| DW0_CH_STRUCT31_CH_STATUS | 0x402887C4 | FULL | Channel status |
| DW0_CH_STRUCT31_CH_IDX | 0x402887C8 | FULL | Channel current indices |
| DW0_CH_STRUCT31_CH_CURR_PTR | 0x402887CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT31_INTR | 0x402887D0 | FULL | Interrupt |
| DW0_CH_STRUCT31_INTR_SET | 0x402887D4 | FULL | Interrupt set |
| DW0_CH_STRUCT31_INTR_MASK | 0x402887D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT31_INTR_MASKED | 0x402887DC | FULL | Interrupt masked |
| DW0_CH_STRUCT31_SRAM_DATA0 | 0x402887E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT31_SRAM_DATA1 | 0x402887E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT31_TR_CMD | 0x402887E8 | FULL | Channel software trigger |

9.1.1.33 CH_STRUCT 32

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT32_CH_CTL | 0x40288800 | FULL | Channel control |
| DW0_CH_STRUCT32_CH_STATUS | 0x40288804 | FULL | Channel status |
| DW0_CH_STRUCT32_CH_IDX | 0x40288808 | FULL | Channel current indices |
| DW0_CH_STRUCT32_CH_CURR_PTR | 0x4028880C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT32_INTR | 0x40288810 | FULL | Interrupt |
| DW0_CH_STRUCT32_INTR_SET | 0x40288814 | FULL | Interrupt set |
| DW0_CH_STRUCT32_INTR_MASK | 0x40288818 | FULL | Interrupt mask |
| DW0_CH_STRUCT32_INTR_MASKED | 0x4028881C | FULL | Interrupt masked |
| DW0_CH_STRUCT32_SRAM_DATA0 | 0x40288820 | FULL | SRAM data 0 |
| DW0_CH_STRUCT32_SRAM_DATA1 | 0x40288824 | FULL | SRAM data 1 |
| DW0_CH_STRUCT32_TR_CMD | 0x40288828 | FULL | Channel software trigger |

9.1.1.34 CH_STRUCT 33

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT33_CH_CTL | 0x40288840 | FULL | Channel control |
| DW0_CH_STRUCT33_CH_STATUS | 0x40288844 | FULL | Channel status |
| DW0_CH_STRUCT33_CH_IDX | 0x40288848 | FULL | Channel current indices |
| DW0_CH_STRUCT33_CH_CURR_PTR | 0x4028884C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT33_INTR | 0x40288850 | FULL | Interrupt |
| DW0_CH_STRUCT33_INTR_SET | 0x40288854 | FULL | Interrupt set |
| DW0_CH_STRUCT33_INTR_MASK | 0x40288858 | FULL | Interrupt mask |
| DW0_CH_STRUCT33_INTR_MASKED | 0x4028885C | FULL | Interrupt masked |
| DW0_CH_STRUCT33_SRAM_DATA0 | 0x40288860 | FULL | SRAM data 0 |
| DW0_CH_STRUCT33_SRAM_DATA1 | 0x40288864 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT33_TR_CMD | 0x40288868 | FULL | Channel software trigger |

9.1.1.35 CH_STRUCT 34

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT34_CH_CTL | 0x40288880 | FULL | Channel control |
| DW0_CH_STRUCT34_CH_STATUS | 0x40288884 | FULL | Channel status |
| DW0_CH_STRUCT34_CH_IDX | 0x40288888 | FULL | Channel current indices |
| DW0_CH_STRUCT34_CH_CURR_PTR | 0x4028888C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT34_INTR | 0x40288890 | FULL | Interrupt |
| DW0_CH_STRUCT34_INTR_SET | 0x40288894 | FULL | Interrupt set |
| DW0_CH_STRUCT34_INTR_MASK | 0x40288898 | FULL | Interrupt mask |
| DW0_CH_STRUCT34_INTR_MASKED | 0x4028889C | FULL | Interrupt masked |
| DW0_CH_STRUCT34_SRAM_DATA0 | 0x402888A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT34_SRAM_DATA1 | 0x402888A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT34_TR_CMD | 0x402888A8 | FULL | Channel software trigger |

9.1.1.36 CH_STRUCT 35

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT35_CH_CTL | 0x402888C0 | FULL | Channel control |
| DW0_CH_STRUCT35_CH_STATUS | 0x402888C4 | FULL | Channel status |
| DW0_CH_STRUCT35_CH_IDX | 0x402888C8 | FULL | Channel current indices |
| DW0_CH_STRUCT35_CH_CURR_PTR | 0x402888CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT35_INTR | 0x402888D0 | FULL | Interrupt |
| DW0_CH_STRUCT35_INTR_SET | 0x402888D4 | FULL | Interrupt set |
| DW0_CH_STRUCT35_INTR_MASK | 0x402888D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT35_INTR_MASKED | 0x402888DC | FULL | Interrupt masked |
| DW0_CH_STRUCT35_SRAM_DATA0 | 0x402888E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT35_SRAM_DATA1 | 0x402888E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT35_TR_CMD | 0x402888E8 | FULL | Channel software trigger |

9.1.1.37 CH_STRUCT 36

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT36_CH_CTL | 0x40288900 | FULL | Channel control |
| DW0_CH_STRUCT36_CH_STATUS | 0x40288904 | FULL | Channel status |
| DW0_CH_STRUCT36_CH_IDX | 0x40288908 | FULL | Channel current indices |
| DW0_CH_STRUCT36_CH_CURR_PTR | 0x4028890C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT36_INTR | 0x40288910 | FULL | Interrupt |
| DW0_CH_STRUCT36_INTR_SET | 0x40288914 | FULL | Interrupt set |
| DW0_CH_STRUCT36_INTR_MASK | 0x40288918 | FULL | Interrupt mask |
| DW0_CH_STRUCT36_INTR_MASKED | 0x4028891C | FULL | Interrupt masked |
| DW0_CH_STRUCT36_SRAM_DATA0 | 0x40288920 | FULL | SRAM data 0 |
| DW0_CH_STRUCT36_SRAM_DATA1 | 0x40288924 | FULL | SRAM data 1 |
| DW0_CH_STRUCT36_TR_CMD | 0x40288928 | FULL | Channel software trigger |

9.1.1.38 CH_STRUCT 37

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT37_CH_CTL | 0x40288940 | FULL | Channel control |
| DW0_CH_STRUCT37_CH_STATUS | 0x40288944 | FULL | Channel status |
| DW0_CH_STRUCT37_CH_IDX | 0x40288948 | FULL | Channel current indices |
| DW0_CH_STRUCT37_CH_CURR_PTR | 0x4028894C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT37_INTR | 0x40288950 | FULL | Interrupt |
| DW0_CH_STRUCT37_INTR_SET | 0x40288954 | FULL | Interrupt set |
| DW0_CH_STRUCT37_INTR_MASK | 0x40288958 | FULL | Interrupt mask |
| DW0_CH_STRUCT37_INTR_MASKED | 0x4028895C | FULL | Interrupt masked |
| DW0_CH_STRUCT37_SRAM_DATA0 | 0x40288960 | FULL | SRAM data 0 |
| DW0_CH_STRUCT37_SRAM_DATA1 | 0x40288964 | FULL | SRAM data 1 |
| DW0_CH_STRUCT37_TR_CMD | 0x40288968 | FULL | Channel software trigger |

9.1.1.39 CH_STRUCT 38

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT38_CH_CTL | 0x40288980 | FULL | Channel control |
| DW0_CH_STRUCT38_CH_STATUS | 0x40288984 | FULL | Channel status |
| DW0_CH_STRUCT38_CH_IDX | 0x40288988 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT38_CH_CURR_PTR | 0x4028898C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT38_INTR | 0x40288990 | FULL | Interrupt |
| DW0_CH_STRUCT38_INTR_SET | 0x40288994 | FULL | Interrupt set |
| DW0_CH_STRUCT38_INTR_MASK | 0x40288998 | FULL | Interrupt mask |
| DW0_CH_STRUCT38_INTR_MASKED | 0x4028899C | FULL | Interrupt masked |
| DW0_CH_STRUCT38_SRAM_DATA0 | 0x402889A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT38_SRAM_DATA1 | 0x402889A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT38_TR_CMD | 0x402889A8 | FULL | Channel software trigger |

9.1.1.40 CH_STRUCT 39

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT39_CH_CTL | 0x402889C0 | FULL | Channel control |
| DW0_CH_STRUCT39_CH_STATUS | 0x402889C4 | FULL | Channel status |
| DW0_CH_STRUCT39_CH_IDX | 0x402889C8 | FULL | Channel current indices |
| DW0_CH_STRUCT39_CH_CURR_PTR | 0x402889CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT39_INTR | 0x402889D0 | FULL | Interrupt |
| DW0_CH_STRUCT39_INTR_SET | 0x402889D4 | FULL | Interrupt set |
| DW0_CH_STRUCT39_INTR_MASK | 0x402889D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT39_INTR_MASKED | 0x402889DC | FULL | Interrupt masked |
| DW0_CH_STRUCT39_SRAM_DATA0 | 0x402889E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT39_SRAM_DATA1 | 0x402889E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT39_TR_CMD | 0x402889E8 | FULL | Channel software trigger |

9.1.1.41 CH_STRUCT 40

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT40_CH_CTL | 0x40288A00 | FULL | Channel control |
| DW0_CH_STRUCT40_CH_STATUS | 0x40288A04 | FULL | Channel status |
| DW0_CH_STRUCT40_CH_IDX | 0x40288A08 | FULL | Channel current indices |
| DW0_CH_STRUCT40_CH_CURR_PTR | 0x40288A0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT40_INTR | 0x40288A10 | FULL | Interrupt |
| DW0_CH_STRUCT40_INTR_SET | 0x40288A14 | FULL | Interrupt set |
| DW0_CH_STRUCT40_INTR_MASK | 0x40288A18 | FULL | Interrupt mask |
| DW0_CH_STRUCT40_INTR_MASKED | 0x40288A1C | FULL | Interrupt masked |
| DW0_CH_STRUCT40_SRAM_DATA0 | 0x40288A20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT40_SRAM_DATA1 | 0x40288A24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT40_TR_CMD | 0x40288A28 | FULL | Channel software trigger |

9.1.1.42 CH_STRUCT 41

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT41_CH_CTL | 0x40288A40 | FULL | Channel control |
| DW0_CH_STRUCT41_CH_STATUS | 0x40288A44 | FULL | Channel status |
| DW0_CH_STRUCT41_CH_IDX | 0x40288A48 | FULL | Channel current indices |
| DW0_CH_STRUCT41_CH_CURR_PTR | 0x40288A4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT41_INTR | 0x40288A50 | FULL | Interrupt |
| DW0_CH_STRUCT41_INTR_SET | 0x40288A54 | FULL | Interrupt set |
| DW0_CH_STRUCT41_INTR_MASK | 0x40288A58 | FULL | Interrupt mask |
| DW0_CH_STRUCT41_INTR_MASKED | 0x40288A5C | FULL | Interrupt masked |
| DW0_CH_STRUCT41_SRAM_DATA0 | 0x40288A60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT41_SRAM_DATA1 | 0x40288A64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT41_TR_CMD | 0x40288A68 | FULL | Channel software trigger |

9.1.1.43 CH_STRUCT 42

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT42_CH_CTL | 0x40288A80 | FULL | Channel control |
| DW0_CH_STRUCT42_CH_STATUS | 0x40288A84 | FULL | Channel status |
| DW0_CH_STRUCT42_CH_IDX | 0x40288A88 | FULL | Channel current indices |
| DW0_CH_STRUCT42_CH_CURR_PTR | 0x40288A8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT42_INTR | 0x40288A90 | FULL | Interrupt |
| DW0_CH_STRUCT42_INTR_SET | 0x40288A94 | FULL | Interrupt set |
| DW0_CH_STRUCT42_INTR_MASK | 0x40288A98 | FULL | Interrupt mask |
| DW0_CH_STRUCT42_INTR_MASKED | 0x40288A9C | FULL | Interrupt masked |
| DW0_CH_STRUCT42_SRAM_DATA0 | 0x40288AA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT42_SRAM_DATA1 | 0x40288AA4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT42_TR_CMD | 0x40288AA8 | FULL | Channel software trigger |

9.1.1.44 CH_STRUCT 43

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT43_CH_CTL | 0x40288AC0 | FULL | Channel control |
| DW0_CH_STRUCT43_CH_STATUS | 0x40288AC4 | FULL | Channel status |
| DW0_CH_STRUCT43_CH_IDX | 0x40288AC8 | FULL | Channel current indices |
| DW0_CH_STRUCT43_CH_CURR_PTR | 0x40288ACC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT43_INTR | 0x40288AD0 | FULL | Interrupt |
| DW0_CH_STRUCT43_INTR_SET | 0x40288AD4 | FULL | Interrupt set |
| DW0_CH_STRUCT43_INTR_MASK | 0x40288AD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT43_INTR_MASKED | 0x40288ADC | FULL | Interrupt masked |
| DW0_CH_STRUCT43_SRAM_DATA0 | 0x40288AE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT43_SRAM_DATA1 | 0x40288AE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT43_TR_CMD | 0x40288AE8 | FULL | Channel software trigger |

9.1.1.45 CH_STRUCT 44

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT44_CH_CTL | 0x40288B00 | FULL | Channel control |
| DW0_CH_STRUCT44_CH_STATUS | 0x40288B04 | FULL | Channel status |
| DW0_CH_STRUCT44_CH_IDX | 0x40288B08 | FULL | Channel current indices |
| DW0_CH_STRUCT44_CH_CURR_PTR | 0x40288B0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT44_INTR | 0x40288B10 | FULL | Interrupt |
| DW0_CH_STRUCT44_INTR_SET | 0x40288B14 | FULL | Interrupt set |
| DW0_CH_STRUCT44_INTR_MASK | 0x40288B18 | FULL | Interrupt mask |
| DW0_CH_STRUCT44_INTR_MASKED | 0x40288B1C | FULL | Interrupt masked |
| DW0_CH_STRUCT44_SRAM_DATA0 | 0x40288B20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT44_SRAM_DATA1 | 0x40288B24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT44_TR_CMD | 0x40288B28 | FULL | Channel software trigger |

9.1.1.46 CH_STRUCT 45

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT45_CH_CTL | 0x40288B40 | FULL | Channel control |
| DW0_CH_STRUCT45_CH_STATUS | 0x40288B44 | FULL | Channel status |
| DW0_CH_STRUCT45_CH_IDX | 0x40288B48 | FULL | Channel current indices |
| DW0_CH_STRUCT45_CH_CURR_PTR | 0x40288B4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT45_INTR | 0x40288B50 | FULL | Interrupt |
| DW0_CH_STRUCT45_INTR_SET | 0x40288B54 | FULL | Interrupt set |
| DW0_CH_STRUCT45_INTR_MASK | 0x40288B58 | FULL | Interrupt mask |
| DW0_CH_STRUCT45_INTR_MASKED | 0x40288B5C | FULL | Interrupt masked |
| DW0_CH_STRUCT45_SRAM_DATA0 | 0x40288B60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT45_SRAM_DATA1 | 0x40288B64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT45_TR_CMD | 0x40288B68 | FULL | Channel software trigger |

9.1.1.47 CH_STRUCT 46

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT46_CH_CTL | 0x40288B80 | FULL | Channel control |
| DW0_CH_STRUCT46_CH_STATUS | 0x40288B84 | FULL | Channel status |
| DW0_CH_STRUCT46_CH_IDX | 0x40288B88 | FULL | Channel current indices |
| DW0_CH_STRUCT46_CH_CURR_PTR | 0x40288B8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT46_INTR | 0x40288B90 | FULL | Interrupt |
| DW0_CH_STRUCT46_INTR_SET | 0x40288B94 | FULL | Interrupt set |
| DW0_CH_STRUCT46_INTR_MASK | 0x40288B98 | FULL | Interrupt mask |
| DW0_CH_STRUCT46_INTR_MASKED | 0x40288B9C | FULL | Interrupt masked |
| DW0_CH_STRUCT46_SRAM_DATA0 | 0x40288BA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT46_SRAM_DATA1 | 0x40288BA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT46_TR_CMD | 0x40288BA8 | FULL | Channel software trigger |

9.1.1.48 CH_STRUCT 47

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT47_CH_CTL | 0x40288BC0 | FULL | Channel control |
| DW0_CH_STRUCT47_CH_STATUS | 0x40288BC4 | FULL | Channel status |
| DW0_CH_STRUCT47_CH_IDX | 0x40288BC8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT47_CH_CURR_PTR | 0x40288BCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT47_INTR | 0x40288BD0 | FULL | Interrupt |
| DW0_CH_STRUCT47_INTR_SET | 0x40288BD4 | FULL | Interrupt set |
| DW0_CH_STRUCT47_INTR_MASK | 0x40288BD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT47_INTR_MASKED | 0x40288BDC | FULL | Interrupt masked |
| DW0_CH_STRUCT47_SRAM_DATA0 | 0x40288BE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT47_SRAM_DATA1 | 0x40288BE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT47_TR_CMD | 0x40288BE8 | FULL | Channel software trigger |

9.1.1.49 CH_STRUCT 48

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT48_CH_CTL | 0x40288C00 | FULL | Channel control |
| DW0_CH_STRUCT48_CH_STATUS | 0x40288C04 | FULL | Channel status |
| DW0_CH_STRUCT48_CH_IDX | 0x40288C08 | FULL | Channel current indices |
| DW0_CH_STRUCT48_CH_CURR_PTR | 0x40288C0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT48_INTR | 0x40288C10 | FULL | Interrupt |
| DW0_CH_STRUCT48_INTR_SET | 0x40288C14 | FULL | Interrupt set |
| DW0_CH_STRUCT48_INTR_MASK | 0x40288C18 | FULL | Interrupt mask |
| DW0_CH_STRUCT48_INTR_MASKED | 0x40288C1C | FULL | Interrupt masked |
| DW0_CH_STRUCT48_SRAM_DATA0 | 0x40288C20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT48_SRAM_DATA1 | 0x40288C24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT48_TR_CMD | 0x40288C28 | FULL | Channel software trigger |

9.1.1.50 CH_STRUCT 49

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT49_CH_CTL | 0x40288C40 | FULL | Channel control |
| DW0_CH_STRUCT49_CH_STATUS | 0x40288C44 | FULL | Channel status |
| DW0_CH_STRUCT49_CH_IDX | 0x40288C48 | FULL | Channel current indices |
| DW0_CH_STRUCT49_CH_CURR_PTR | 0x40288C4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT49_INTR | 0x40288C50 | FULL | Interrupt |
| DW0_CH_STRUCT49_INTR_SET | 0x40288C54 | FULL | Interrupt set |
| DW0_CH_STRUCT49_INTR_MASK | 0x40288C58 | FULL | Interrupt mask |
| DW0_CH_STRUCT49_INTR_MASKED | 0x40288C5C | FULL | Interrupt masked |
| DW0_CH_STRUCT49_SRAM_DATA0 | 0x40288C60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT49_SRAM_DATA1 | 0x40288C64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT49_TR_CMD | 0x40288C68 | FULL | Channel software trigger |

9.1.1.51 CH_STRUCT 50

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT50_CH_CTL | 0x40288C80 | FULL | Channel control |
| DW0_CH_STRUCT50_CH_STATUS | 0x40288C84 | FULL | Channel status |
| DW0_CH_STRUCT50_CH_IDX | 0x40288C88 | FULL | Channel current indices |
| DW0_CH_STRUCT50_CH_CURR_PTR | 0x40288C8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT50_INTR | 0x40288C90 | FULL | Interrupt |
| DW0_CH_STRUCT50_INTR_SET | 0x40288C94 | FULL | Interrupt set |
| DW0_CH_STRUCT50_INTR_MASK | 0x40288C98 | FULL | Interrupt mask |
| DW0_CH_STRUCT50_INTR_MASKED | 0x40288C9C | FULL | Interrupt masked |
| DW0_CH_STRUCT50_SRAM_DATA0 | 0x40288CA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT50_SRAM_DATA1 | 0x40288CA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT50_TR_CMD | 0x40288CA8 | FULL | Channel software trigger |

9.1.1.52 CH_STRUCT 51

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT51_CH_CTL | 0x40288CC0 | FULL | Channel control |
| DW0_CH_STRUCT51_CH_STATUS | 0x40288CC4 | FULL | Channel status |
| DW0_CH_STRUCT51_CH_IDX | 0x40288CC8 | FULL | Channel current indices |
| DW0_CH_STRUCT51_CH_CURR_PTR | 0x40288CCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT51_INTR | 0x40288CD0 | FULL | Interrupt |
| DW0_CH_STRUCT51_INTR_SET | 0x40288CD4 | FULL | Interrupt set |
| DW0_CH_STRUCT51_INTR_MASK | 0x40288CD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT51_INTR_MASKED | 0x40288CDC | FULL | Interrupt masked |
| DW0_CH_STRUCT51_SRAM_DATA0 | 0x40288CE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT51_SRAM_DATA1 | 0x40288CE4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT51_TR_CMD | 0x40288CE8 | FULL | Channel software trigger |

9.1.1.53 CH_STRUCT 52

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT52_CH_CTL | 0x40288D00 | FULL | Channel control |
| DW0_CH_STRUCT52_CH_STATUS | 0x40288D04 | FULL | Channel status |
| DW0_CH_STRUCT52_CH_IDX | 0x40288D08 | FULL | Channel current indices |
| DW0_CH_STRUCT52_CH_CURR_PTR | 0x40288D0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT52_INTR | 0x40288D10 | FULL | Interrupt |
| DW0_CH_STRUCT52_INTR_SET | 0x40288D14 | FULL | Interrupt set |
| DW0_CH_STRUCT52_INTR_MASK | 0x40288D18 | FULL | Interrupt mask |
| DW0_CH_STRUCT52_INTR_MASKED | 0x40288D1C | FULL | Interrupt masked |
| DW0_CH_STRUCT52_SRAM_DATA0 | 0x40288D20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT52_SRAM_DATA1 | 0x40288D24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT52_TR_CMD | 0x40288D28 | FULL | Channel software trigger |

9.1.1.54 CH_STRUCT 53

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT53_CH_CTL | 0x40288D40 | FULL | Channel control |
| DW0_CH_STRUCT53_CH_STATUS | 0x40288D44 | FULL | Channel status |
| DW0_CH_STRUCT53_CH_IDX | 0x40288D48 | FULL | Channel current indices |
| DW0_CH_STRUCT53_CH_CURR_PTR | 0x40288D4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT53_INTR | 0x40288D50 | FULL | Interrupt |
| DW0_CH_STRUCT53_INTR_SET | 0x40288D54 | FULL | Interrupt set |
| DW0_CH_STRUCT53_INTR_MASK | 0x40288D58 | FULL | Interrupt mask |
| DW0_CH_STRUCT53_INTR_MASKED | 0x40288D5C | FULL | Interrupt masked |
| DW0_CH_STRUCT53_SRAM_DATA0 | 0x40288D60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT53_SRAM_DATA1 | 0x40288D64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT53_TR_CMD | 0x40288D68 | FULL | Channel software trigger |

9.1.1.55 CH_STRUCT 54

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT54_CH_CTL | 0x40288D80 | FULL | Channel control |
| DW0_CH_STRUCT54_CH_STATUS | 0x40288D84 | FULL | Channel status |
| DW0_CH_STRUCT54_CH_IDX | 0x40288D88 | FULL | Channel current indices |
| DW0_CH_STRUCT54_CH_CURR_PTR | 0x40288D8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT54_INTR | 0x40288D90 | FULL | Interrupt |
| DW0_CH_STRUCT54_INTR_SET | 0x40288D94 | FULL | Interrupt set |
| DW0_CH_STRUCT54_INTR_MASK | 0x40288D98 | FULL | Interrupt mask |
| DW0_CH_STRUCT54_INTR_MASKED | 0x40288D9C | FULL | Interrupt masked |
| DW0_CH_STRUCT54_SRAM_DATA0 | 0x40288DA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT54_SRAM_DATA1 | 0x40288DA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT54_TR_CMD | 0x40288DA8 | FULL | Channel software trigger |

9.1.1.56 CH_STRUCT 55

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT55_CH_CTL | 0x40288DC0 | FULL | Channel control |
| DW0_CH_STRUCT55_CH_STATUS | 0x40288DC4 | FULL | Channel status |
| DW0_CH_STRUCT55_CH_IDX | 0x40288DC8 | FULL | Channel current indices |
| DW0_CH_STRUCT55_CH_CURR_PTR | 0x40288DCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT55_INTR | 0x40288DD0 | FULL | Interrupt |
| DW0_CH_STRUCT55_INTR_SET | 0x40288DD4 | FULL | Interrupt set |
| DW0_CH_STRUCT55_INTR_MASK | 0x40288DD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT55_INTR_MASKED | 0x40288DDC | FULL | Interrupt masked |
| DW0_CH_STRUCT55_SRAM_DATA0 | 0x40288DE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT55_SRAM_DATA1 | 0x40288DE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT55_TR_CMD | 0x40288DE8 | FULL | Channel software trigger |

9.1.1.57 CH_STRUCT 56

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT56_CH_CTL | 0x40288E00 | FULL | Channel control |
| DW0_CH_STRUCT56_CH_STATUS | 0x40288E04 | FULL | Channel status |
| DW0_CH_STRUCT56_CH_IDX | 0x40288E08 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT56_CH_CURR_PTR | 0x40288E0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT56_INTR | 0x40288E10 | FULL | Interrupt |
| DW0_CH_STRUCT56_INTR_SET | 0x40288E14 | FULL | Interrupt set |
| DW0_CH_STRUCT56_INTR_MASK | 0x40288E18 | FULL | Interrupt mask |
| DW0_CH_STRUCT56_INTR_MASKED | 0x40288E1C | FULL | Interrupt masked |
| DW0_CH_STRUCT56_SRAM_DATA0 | 0x40288E20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT56_SRAM_DATA1 | 0x40288E24 | FULL | SRAM data 1 |
| DW0_CH_STRUCT56_TR_CMD | 0x40288E28 | FULL | Channel software trigger |

9.1.1.58 CH_STRUCT 57

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT57_CH_CTL | 0x40288E40 | FULL | Channel control |
| DW0_CH_STRUCT57_CH_STATUS | 0x40288E44 | FULL | Channel status |
| DW0_CH_STRUCT57_CH_IDX | 0x40288E48 | FULL | Channel current indices |
| DW0_CH_STRUCT57_CH_CURR_PTR | 0x40288E4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT57_INTR | 0x40288E50 | FULL | Interrupt |
| DW0_CH_STRUCT57_INTR_SET | 0x40288E54 | FULL | Interrupt set |
| DW0_CH_STRUCT57_INTR_MASK | 0x40288E58 | FULL | Interrupt mask |
| DW0_CH_STRUCT57_INTR_MASKED | 0x40288E5C | FULL | Interrupt masked |
| DW0_CH_STRUCT57_SRAM_DATA0 | 0x40288E60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT57_SRAM_DATA1 | 0x40288E64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT57_TR_CMD | 0x40288E68 | FULL | Channel software trigger |

9.1.1.59 CH_STRUCT 58

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT58_CH_CTL | 0x40288E80 | FULL | Channel control |
| DW0_CH_STRUCT58_CH_STATUS | 0x40288E84 | FULL | Channel status |
| DW0_CH_STRUCT58_CH_IDX | 0x40288E88 | FULL | Channel current indices |
| DW0_CH_STRUCT58_CH_CURR_PTR | 0x40288E8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT58_INTR | 0x40288E90 | FULL | Interrupt |
| DW0_CH_STRUCT58_INTR_SET | 0x40288E94 | FULL | Interrupt set |
| DW0_CH_STRUCT58_INTR_MASK | 0x40288E98 | FULL | Interrupt mask |
| DW0_CH_STRUCT58_INTR_MASKED | 0x40288E9C | FULL | Interrupt masked |
| DW0_CH_STRUCT58_SRAM_DATA0 | 0x40288EA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT58_SRAM_DATA1 | 0x40288EA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT58_TR_CMD | 0x40288EA8 | FULL | Channel software trigger |

9.1.1.60 CH_STRUCT 59

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT59_CH_CTL | 0x40288EC0 | FULL | Channel control |
| DW0_CH_STRUCT59_CH_STATUS | 0x40288EC4 | FULL | Channel status |
| DW0_CH_STRUCT59_CH_IDX | 0x40288EC8 | FULL | Channel current indices |
| DW0_CH_STRUCT59_CH_CURR_PTR | 0x40288ECC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT59_INTR | 0x40288ED0 | FULL | Interrupt |
| DW0_CH_STRUCT59_INTR_SET | 0x40288ED4 | FULL | Interrupt set |
| DW0_CH_STRUCT59_INTR_MASK | 0x40288ED8 | FULL | Interrupt mask |
| DW0_CH_STRUCT59_INTR_MASKED | 0x40288EDC | FULL | Interrupt masked |
| DW0_CH_STRUCT59_SRAM_DATA0 | 0x40288EE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT59_SRAM_DATA1 | 0x40288EE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT59_TR_CMD | 0x40288EE8 | FULL | Channel software trigger |

9.1.1.61 CH_STRUCT 60

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT60_CH_CTL | 0x40288F00 | FULL | Channel control |
| DW0_CH_STRUCT60_CH_STATUS | 0x40288F04 | FULL | Channel status |
| DW0_CH_STRUCT60_CH_IDX | 0x40288F08 | FULL | Channel current indices |
| DW0_CH_STRUCT60_CH_CURR_PTR | 0x40288F0C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT60_INTR | 0x40288F10 | FULL | Interrupt |
| DW0_CH_STRUCT60_INTR_SET | 0x40288F14 | FULL | Interrupt set |
| DW0_CH_STRUCT60_INTR_MASK | 0x40288F18 | FULL | Interrupt mask |
| DW0_CH_STRUCT60_INTR_MASKED | 0x40288F1C | FULL | Interrupt masked |
| DW0_CH_STRUCT60_SRAM_DATA0 | 0x40288F20 | FULL | SRAM data 0 |
| DW0_CH_STRUCT60_SRAM_DATA1 | 0x40288F24 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT60_TR_CMD | 0x40288F28 | FULL | Channel software trigger |

9.1.1.62 CH_STRUCT 61

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT61_CH_CTL | 0x40288F40 | FULL | Channel control |
| DW0_CH_STRUCT61_CH_STATUS | 0x40288F44 | FULL | Channel status |
| DW0_CH_STRUCT61_CH_IDX | 0x40288F48 | FULL | Channel current indices |
| DW0_CH_STRUCT61_CH_CURR_PTR | 0x40288F4C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT61_INTR | 0x40288F50 | FULL | Interrupt |
| DW0_CH_STRUCT61_INTR_SET | 0x40288F54 | FULL | Interrupt set |
| DW0_CH_STRUCT61_INTR_MASK | 0x40288F58 | FULL | Interrupt mask |
| DW0_CH_STRUCT61_INTR_MASKED | 0x40288F5C | FULL | Interrupt masked |
| DW0_CH_STRUCT61_SRAM_DATA0 | 0x40288F60 | FULL | SRAM data 0 |
| DW0_CH_STRUCT61_SRAM_DATA1 | 0x40288F64 | FULL | SRAM data 1 |
| DW0_CH_STRUCT61_TR_CMD | 0x40288F68 | FULL | Channel software trigger |

9.1.1.63 CH_STRUCT 62

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT62_CH_CTL | 0x40288F80 | FULL | Channel control |
| DW0_CH_STRUCT62_CH_STATUS | 0x40288F84 | FULL | Channel status |
| DW0_CH_STRUCT62_CH_IDX | 0x40288F88 | FULL | Channel current indices |
| DW0_CH_STRUCT62_CH_CURR_PTR | 0x40288F8C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT62_INTR | 0x40288F90 | FULL | Interrupt |
| DW0_CH_STRUCT62_INTR_SET | 0x40288F94 | FULL | Interrupt set |
| DW0_CH_STRUCT62_INTR_MASK | 0x40288F98 | FULL | Interrupt mask |
| DW0_CH_STRUCT62_INTR_MASKED | 0x40288F9C | FULL | Interrupt masked |
| DW0_CH_STRUCT62_SRAM_DATA0 | 0x40288FA0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT62_SRAM_DATA1 | 0x40288FA4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT62_TR_CMD | 0x40288FA8 | FULL | Channel software trigger |

9.1.1.64 CH_STRUCT 63

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT63_CH_CTL | 0x40288FC0 | FULL | Channel control |
| DW0_CH_STRUCT63_CH_STATUS | 0x40288FC4 | FULL | Channel status |
| DW0_CH_STRUCT63_CH_IDX | 0x40288FC8 | FULL | Channel current indices |
| DW0_CH_STRUCT63_CH_CURR_PTR | 0x40288FCC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT63_INTR | 0x40288FD0 | FULL | Interrupt |
| DW0_CH_STRUCT63_INTR_SET | 0x40288FD4 | FULL | Interrupt set |
| DW0_CH_STRUCT63_INTR_MASK | 0x40288FD8 | FULL | Interrupt mask |
| DW0_CH_STRUCT63_INTR_MASKED | 0x40288FDC | FULL | Interrupt masked |
| DW0_CH_STRUCT63_SRAM_DATA0 | 0x40288FE0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT63_SRAM_DATA1 | 0x40288FE4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT63_TR_CMD | 0x40288FE8 | FULL | Channel software trigger |

9.1.1.65 CH_STRUCT 64

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT64_CH_CTL | 0x40289000 | FULL | Channel control |
| DW0_CH_STRUCT64_CH_STATUS | 0x40289004 | FULL | Channel status |
| DW0_CH_STRUCT64_CH_IDX | 0x40289008 | FULL | Channel current indices |
| DW0_CH_STRUCT64_CH_CURR_PTR | 0x4028900C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT64_INTR | 0x40289010 | FULL | Interrupt |
| DW0_CH_STRUCT64_INTR_SET | 0x40289014 | FULL | Interrupt set |
| DW0_CH_STRUCT64_INTR_MASK | 0x40289018 | FULL | Interrupt mask |
| DW0_CH_STRUCT64_INTR_MASKED | 0x4028901C | FULL | Interrupt masked |
| DW0_CH_STRUCT64_SRAM_DATA0 | 0x40289020 | FULL | SRAM data 0 |
| DW0_CH_STRUCT64_SRAM_DATA1 | 0x40289024 | FULL | SRAM data 1 |
| DW0_CH_STRUCT64_TR_CMD | 0x40289028 | FULL | Channel software trigger |

9.1.1.66 CH_STRUCT 65

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT65_CH_CTL | 0x40289040 | FULL | Channel control |
| DW0_CH_STRUCT65_CH_STATUS | 0x40289044 | FULL | Channel status |
| DW0_CH_STRUCT65_CH_IDX | 0x40289048 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT65_CH_CURR_PTR | 0x4028904C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT65_INTR | 0x40289050 | FULL | Interrupt |
| DW0_CH_STRUCT65_INTR_SET | 0x40289054 | FULL | Interrupt set |
| DW0_CH_STRUCT65_INTR_MASK | 0x40289058 | FULL | Interrupt mask |
| DW0_CH_STRUCT65_INTR_MASKED | 0x4028905C | FULL | Interrupt masked |
| DW0_CH_STRUCT65_SRAM_DATA0 | 0x40289060 | FULL | SRAM data 0 |
| DW0_CH_STRUCT65_SRAM_DATA1 | 0x40289064 | FULL | SRAM data 1 |
| DW0_CH_STRUCT65_TR_CMD | 0x40289068 | FULL | Channel software trigger |

9.1.1.67 CH_STRUCT 66

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT66_CH_CTL | 0x40289080 | FULL | Channel control |
| DW0_CH_STRUCT66_CH_STATUS | 0x40289084 | FULL | Channel status |
| DW0_CH_STRUCT66_CH_IDX | 0x40289088 | FULL | Channel current indices |
| DW0_CH_STRUCT66_CH_CURR_PTR | 0x4028908C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT66_INTR | 0x40289090 | FULL | Interrupt |
| DW0_CH_STRUCT66_INTR_SET | 0x40289094 | FULL | Interrupt set |
| DW0_CH_STRUCT66_INTR_MASK | 0x40289098 | FULL | Interrupt mask |
| DW0_CH_STRUCT66_INTR_MASKED | 0x4028909C | FULL | Interrupt masked |
| DW0_CH_STRUCT66_SRAM_DATA0 | 0x402890A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT66_SRAM_DATA1 | 0x402890A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT66_TR_CMD | 0x402890A8 | FULL | Channel software trigger |

9.1.1.68 CH_STRUCT 67

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT67_CH_CTL | 0x402890C0 | FULL | Channel control |
| DW0_CH_STRUCT67_CH_STATUS | 0x402890C4 | FULL | Channel status |
| DW0_CH_STRUCT67_CH_IDX | 0x402890C8 | FULL | Channel current indices |
| DW0_CH_STRUCT67_CH_CURR_PTR | 0x402890CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT67_INTR | 0x402890D0 | FULL | Interrupt |
| DW0_CH_STRUCT67_INTR_SET | 0x402890D4 | FULL | Interrupt set |
| DW0_CH_STRUCT67_INTR_MASK | 0x402890D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT67_INTR_MASKED | 0x402890DC | FULL | Interrupt masked |
| DW0_CH_STRUCT67_SRAM_DATA0 | 0x402890E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT67_SRAM_DATA1 | 0x402890E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT67_TR_CMD | 0x402890E8 | FULL | Channel software trigger |

9.1.1.69 CH_STRUCT 68

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT68_CH_CTL | 0x40289100 | FULL | Channel control |
| DW0_CH_STRUCT68_CH_STATUS | 0x40289104 | FULL | Channel status |
| DW0_CH_STRUCT68_CH_IDX | 0x40289108 | FULL | Channel current indices |
| DW0_CH_STRUCT68_CH_CURR_PTR | 0x4028910C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT68_INTR | 0x40289110 | FULL | Interrupt |
| DW0_CH_STRUCT68_INTR_SET | 0x40289114 | FULL | Interrupt set |
| DW0_CH_STRUCT68_INTR_MASK | 0x40289118 | FULL | Interrupt mask |
| DW0_CH_STRUCT68_INTR_MASKED | 0x4028911C | FULL | Interrupt masked |
| DW0_CH_STRUCT68_SRAM_DATA0 | 0x40289120 | FULL | SRAM data 0 |
| DW0_CH_STRUCT68_SRAM_DATA1 | 0x40289124 | FULL | SRAM data 1 |
| DW0_CH_STRUCT68_TR_CMD | 0x40289128 | FULL | Channel software trigger |

9.1.1.70 CH_STRUCT 69

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT69_CH_CTL | 0x40289140 | FULL | Channel control |
| DW0_CH_STRUCT69_CH_STATUS | 0x40289144 | FULL | Channel status |
| DW0_CH_STRUCT69_CH_IDX | 0x40289148 | FULL | Channel current indices |
| DW0_CH_STRUCT69_CH_CURR_PTR | 0x4028914C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT69_INTR | 0x40289150 | FULL | Interrupt |
| DW0_CH_STRUCT69_INTR_SET | 0x40289154 | FULL | Interrupt set |
| DW0_CH_STRUCT69_INTR_MASK | 0x40289158 | FULL | Interrupt mask |
| DW0_CH_STRUCT69_INTR_MASKED | 0x4028915C | FULL | Interrupt masked |
| DW0_CH_STRUCT69_SRAM_DATA0 | 0x40289160 | FULL | SRAM data 0 |
| DW0_CH_STRUCT69_SRAM_DATA1 | 0x40289164 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT69_TR_CMD | 0x40289168 | FULL | Channel software trigger |

9.1.1.71 CH_STRUCT 70

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT70_CH_CTL | 0x40289180 | FULL | Channel control |
| DW0_CH_STRUCT70_CH_STATUS | 0x40289184 | FULL | Channel status |
| DW0_CH_STRUCT70_CH_IDX | 0x40289188 | FULL | Channel current indices |
| DW0_CH_STRUCT70_CH_CURR_PTR | 0x4028918C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT70_INTR | 0x40289190 | FULL | Interrupt |
| DW0_CH_STRUCT70_INTR_SET | 0x40289194 | FULL | Interrupt set |
| DW0_CH_STRUCT70_INTR_MASK | 0x40289198 | FULL | Interrupt mask |
| DW0_CH_STRUCT70_INTR_MASKED | 0x4028919C | FULL | Interrupt masked |
| DW0_CH_STRUCT70_SRAM_DATA0 | 0x402891A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT70_SRAM_DATA1 | 0x402891A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT70_TR_CMD | 0x402891A8 | FULL | Channel software trigger |

9.1.1.72 CH_STRUCT 71

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT71_CH_CTL | 0x402891C0 | FULL | Channel control |
| DW0_CH_STRUCT71_CH_STATUS | 0x402891C4 | FULL | Channel status |
| DW0_CH_STRUCT71_CH_IDX | 0x402891C8 | FULL | Channel current indices |
| DW0_CH_STRUCT71_CH_CURR_PTR | 0x402891CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT71_INTR | 0x402891D0 | FULL | Interrupt |
| DW0_CH_STRUCT71_INTR_SET | 0x402891D4 | FULL | Interrupt set |
| DW0_CH_STRUCT71_INTR_MASK | 0x402891D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT71_INTR_MASKED | 0x402891DC | FULL | Interrupt masked |
| DW0_CH_STRUCT71_SRAM_DATA0 | 0x402891E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT71_SRAM_DATA1 | 0x402891E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT71_TR_CMD | 0x402891E8 | FULL | Channel software trigger |

9.1.1.73 CH_STRUCT 72

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT72_CH_CTL | 0x40289200 | FULL | Channel control |
| DW0_CH_STRUCT72_CH_STATUS | 0x40289204 | FULL | Channel status |
| DW0_CH_STRUCT72_CH_IDX | 0x40289208 | FULL | Channel current indices |
| DW0_CH_STRUCT72_CH_CURR_PTR | 0x4028920C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT72_INTR | 0x40289210 | FULL | Interrupt |
| DW0_CH_STRUCT72_INTR_SET | 0x40289214 | FULL | Interrupt set |
| DW0_CH_STRUCT72_INTR_MASK | 0x40289218 | FULL | Interrupt mask |
| DW0_CH_STRUCT72_INTR_MASKED | 0x4028921C | FULL | Interrupt masked |
| DW0_CH_STRUCT72_SRAM_DATA0 | 0x40289220 | FULL | SRAM data 0 |
| DW0_CH_STRUCT72_SRAM_DATA1 | 0x40289224 | FULL | SRAM data 1 |
| DW0_CH_STRUCT72_TR_CMD | 0x40289228 | FULL | Channel software trigger |

9.1.1.74 CH_STRUCT 73

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT73_CH_CTL | 0x40289240 | FULL | Channel control |
| DW0_CH_STRUCT73_CH_STATUS | 0x40289244 | FULL | Channel status |
| DW0_CH_STRUCT73_CH_IDX | 0x40289248 | FULL | Channel current indices |
| DW0_CH_STRUCT73_CH_CURR_PTR | 0x4028924C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT73_INTR | 0x40289250 | FULL | Interrupt |
| DW0_CH_STRUCT73_INTR_SET | 0x40289254 | FULL | Interrupt set |
| DW0_CH_STRUCT73_INTR_MASK | 0x40289258 | FULL | Interrupt mask |
| DW0_CH_STRUCT73_INTR_MASKED | 0x4028925C | FULL | Interrupt masked |
| DW0_CH_STRUCT73_SRAM_DATA0 | 0x40289260 | FULL | SRAM data 0 |
| DW0_CH_STRUCT73_SRAM_DATA1 | 0x40289264 | FULL | SRAM data 1 |
| DW0_CH_STRUCT73_TR_CMD | 0x40289268 | FULL | Channel software trigger |

9.1.1.75 CH_STRUCT 74

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT74_CH_CTL | 0x40289280 | FULL | Channel control |
| DW0_CH_STRUCT74_CH_STATUS | 0x40289284 | FULL | Channel status |
| DW0_CH_STRUCT74_CH_IDX | 0x40289288 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT74_CH_CURR_PTR | 0x4028928C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT74_INTR | 0x40289290 | FULL | Interrupt |
| DW0_CH_STRUCT74_INTR_SET | 0x40289294 | FULL | Interrupt set |
| DW0_CH_STRUCT74_INTR_MASK | 0x40289298 | FULL | Interrupt mask |
| DW0_CH_STRUCT74_INTR_MASKED | 0x4028929C | FULL | Interrupt masked |
| DW0_CH_STRUCT74_SRAM_DATA0 | 0x402892A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT74_SRAM_DATA1 | 0x402892A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT74_TR_CMD | 0x402892A8 | FULL | Channel software trigger |

9.1.1.76 CH_STRUCT 75

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT75_CH_CTL | 0x402892C0 | FULL | Channel control |
| DW0_CH_STRUCT75_CH_STATUS | 0x402892C4 | FULL | Channel status |
| DW0_CH_STRUCT75_CH_IDX | 0x402892C8 | FULL | Channel current indices |
| DW0_CH_STRUCT75_CH_CURR_PTR | 0x402892CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT75_INTR | 0x402892D0 | FULL | Interrupt |
| DW0_CH_STRUCT75_INTR_SET | 0x402892D4 | FULL | Interrupt set |
| DW0_CH_STRUCT75_INTR_MASK | 0x402892D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT75_INTR_MASKED | 0x402892DC | FULL | Interrupt masked |
| DW0_CH_STRUCT75_SRAM_DATA0 | 0x402892E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT75_SRAM_DATA1 | 0x402892E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT75_TR_CMD | 0x402892E8 | FULL | Channel software trigger |

9.1.1.77 CH_STRUCT 76

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT76_CH_CTL | 0x40289300 | FULL | Channel control |
| DW0_CH_STRUCT76_CH_STATUS | 0x40289304 | FULL | Channel status |
| DW0_CH_STRUCT76_CH_IDX | 0x40289308 | FULL | Channel current indices |
| DW0_CH_STRUCT76_CH_CURR_PTR | 0x4028930C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT76_INTR | 0x40289310 | FULL | Interrupt |
| DW0_CH_STRUCT76_INTR_SET | 0x40289314 | FULL | Interrupt set |
| DW0_CH_STRUCT76_INTR_MASK | 0x40289318 | FULL | Interrupt mask |
| DW0_CH_STRUCT76_INTR_MASKED | 0x4028931C | FULL | Interrupt masked |
| DW0_CH_STRUCT76_SRAM_DATA0 | 0x40289320 | FULL | SRAM data 0 |
| DW0_CH_STRUCT76_SRAM_DATA1 | 0x40289324 | FULL | SRAM data 1 |
| DW0_CH_STRUCT76_TR_CMD | 0x40289328 | FULL | Channel software trigger |

9.1.1.78 CH_STRUCT 77

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT77_CH_CTL | 0x40289340 | FULL | Channel control |
| DW0_CH_STRUCT77_CH_STATUS | 0x40289344 | FULL | Channel status |
| DW0_CH_STRUCT77_CH_IDX | 0x40289348 | FULL | Channel current indices |
| DW0_CH_STRUCT77_CH_CURR_PTR | 0x4028934C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT77_INTR | 0x40289350 | FULL | Interrupt |
| DW0_CH_STRUCT77_INTR_SET | 0x40289354 | FULL | Interrupt set |
| DW0_CH_STRUCT77_INTR_MASK | 0x40289358 | FULL | Interrupt mask |
| DW0_CH_STRUCT77_INTR_MASKED | 0x4028935C | FULL | Interrupt masked |
| DW0_CH_STRUCT77_SRAM_DATA0 | 0x40289360 | FULL | SRAM data 0 |
| DW0_CH_STRUCT77_SRAM_DATA1 | 0x40289364 | FULL | SRAM data 1 |
| DW0_CH_STRUCT77_TR_CMD | 0x40289368 | FULL | Channel software trigger |

9.1.1.79 CH_STRUCT 78

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT78_CH_CTL | 0x40289380 | FULL | Channel control |
| DW0_CH_STRUCT78_CH_STATUS | 0x40289384 | FULL | Channel status |
| DW0_CH_STRUCT78_CH_IDX | 0x40289388 | FULL | Channel current indices |
| DW0_CH_STRUCT78_CH_CURR_PTR | 0x4028938C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT78_INTR | 0x40289390 | FULL | Interrupt |
| DW0_CH_STRUCT78_INTR_SET | 0x40289394 | FULL | Interrupt set |
| DW0_CH_STRUCT78_INTR_MASK | 0x40289398 | FULL | Interrupt mask |
| DW0_CH_STRUCT78_INTR_MASKED | 0x4028939C | FULL | Interrupt masked |
| DW0_CH_STRUCT78_SRAM_DATA0 | 0x402893A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT78_SRAM_DATA1 | 0x402893A4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT78_TR_CMD | 0x402893A8 | FULL | Channel software trigger |

9.1.1.80 CH_STRUCT 79

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT79_CH_CTL | 0x402893C0 | FULL | Channel control |
| DW0_CH_STRUCT79_CH_STATUS | 0x402893C4 | FULL | Channel status |
| DW0_CH_STRUCT79_CH_IDX | 0x402893C8 | FULL | Channel current indices |
| DW0_CH_STRUCT79_CH_CURR_PTR | 0x402893CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT79_INTR | 0x402893D0 | FULL | Interrupt |
| DW0_CH_STRUCT79_INTR_SET | 0x402893D4 | FULL | Interrupt set |
| DW0_CH_STRUCT79_INTR_MASK | 0x402893D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT79_INTR_MASKED | 0x402893DC | FULL | Interrupt masked |
| DW0_CH_STRUCT79_SRAM_DATA0 | 0x402893E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT79_SRAM_DATA1 | 0x402893E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT79_TR_CMD | 0x402893E8 | FULL | Channel software trigger |

9.1.1.81 CH_STRUCT 80

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT80_CH_CTL | 0x40289400 | FULL | Channel control |
| DW0_CH_STRUCT80_CH_STATUS | 0x40289404 | FULL | Channel status |
| DW0_CH_STRUCT80_CH_IDX | 0x40289408 | FULL | Channel current indices |
| DW0_CH_STRUCT80_CH_CURR_PTR | 0x4028940C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT80_INTR | 0x40289410 | FULL | Interrupt |
| DW0_CH_STRUCT80_INTR_SET | 0x40289414 | FULL | Interrupt set |
| DW0_CH_STRUCT80_INTR_MASK | 0x40289418 | FULL | Interrupt mask |
| DW0_CH_STRUCT80_INTR_MASKED | 0x4028941C | FULL | Interrupt masked |
| DW0_CH_STRUCT80_SRAM_DATA0 | 0x40289420 | FULL | SRAM data 0 |
| DW0_CH_STRUCT80_SRAM_DATA1 | 0x40289424 | FULL | SRAM data 1 |
| DW0_CH_STRUCT80_TR_CMD | 0x40289428 | FULL | Channel software trigger |

9.1.1.82 CH_STRUCT 81

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT81_CH_CTL | 0x40289440 | FULL | Channel control |
| DW0_CH_STRUCT81_CH_STATUS | 0x40289444 | FULL | Channel status |
| DW0_CH_STRUCT81_CH_IDX | 0x40289448 | FULL | Channel current indices |
| DW0_CH_STRUCT81_CH_CURR_PTR | 0x4028944C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT81_INTR | 0x40289450 | FULL | Interrupt |
| DW0_CH_STRUCT81_INTR_SET | 0x40289454 | FULL | Interrupt set |
| DW0_CH_STRUCT81_INTR_MASK | 0x40289458 | FULL | Interrupt mask |
| DW0_CH_STRUCT81_INTR_MASKED | 0x4028945C | FULL | Interrupt masked |
| DW0_CH_STRUCT81_SRAM_DATA0 | 0x40289460 | FULL | SRAM data 0 |
| DW0_CH_STRUCT81_SRAM_DATA1 | 0x40289464 | FULL | SRAM data 1 |
| DW0_CH_STRUCT81_TR_CMD | 0x40289468 | FULL | Channel software trigger |

9.1.1.83 CH_STRUCT 82

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT82_CH_CTL | 0x40289480 | FULL | Channel control |
| DW0_CH_STRUCT82_CH_STATUS | 0x40289484 | FULL | Channel status |
| DW0_CH_STRUCT82_CH_IDX | 0x40289488 | FULL | Channel current indices |
| DW0_CH_STRUCT82_CH_CURR_PTR | 0x4028948C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT82_INTR | 0x40289490 | FULL | Interrupt |
| DW0_CH_STRUCT82_INTR_SET | 0x40289494 | FULL | Interrupt set |
| DW0_CH_STRUCT82_INTR_MASK | 0x40289498 | FULL | Interrupt mask |
| DW0_CH_STRUCT82_INTR_MASKED | 0x4028949C | FULL | Interrupt masked |
| DW0_CH_STRUCT82_SRAM_DATA0 | 0x402894A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT82_SRAM_DATA1 | 0x402894A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT82_TR_CMD | 0x402894A8 | FULL | Channel software trigger |

9.1.1.84 CH_STRUCT 83

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-------------------------|
| DW0_CH_STRUCT83_CH_CTL | 0x402894C0 | FULL | Channel control |
| DW0_CH_STRUCT83_CH_STATUS | 0x402894C4 | FULL | Channel status |
| DW0_CH_STRUCT83_CH_IDX | 0x402894C8 | FULL | Channel current indices |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT83_CH_CURR_PTR | 0x402894CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT83_INTR | 0x402894D0 | FULL | Interrupt |
| DW0_CH_STRUCT83_INTR_SET | 0x402894D4 | FULL | Interrupt set |
| DW0_CH_STRUCT83_INTR_MASK | 0x402894D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT83_INTR_MASKED | 0x402894DC | FULL | Interrupt masked |
| DW0_CH_STRUCT83_SRAM_DATA0 | 0x402894E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT83_SRAM_DATA1 | 0x402894E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT83_TR_CMD | 0x402894E8 | FULL | Channel software trigger |

9.1.1.85 CH_STRUCT 84

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT84_CH_CTL | 0x40289500 | FULL | Channel control |
| DW0_CH_STRUCT84_CH_STATUS | 0x40289504 | FULL | Channel status |
| DW0_CH_STRUCT84_CH_IDX | 0x40289508 | FULL | Channel current indices |
| DW0_CH_STRUCT84_CH_CURR_PTR | 0x4028950C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT84_INTR | 0x40289510 | FULL | Interrupt |
| DW0_CH_STRUCT84_INTR_SET | 0x40289514 | FULL | Interrupt set |
| DW0_CH_STRUCT84_INTR_MASK | 0x40289518 | FULL | Interrupt mask |
| DW0_CH_STRUCT84_INTR_MASKED | 0x4028951C | FULL | Interrupt masked |
| DW0_CH_STRUCT84_SRAM_DATA0 | 0x40289520 | FULL | SRAM data 0 |
| DW0_CH_STRUCT84_SRAM_DATA1 | 0x40289524 | FULL | SRAM data 1 |
| DW0_CH_STRUCT84_TR_CMD | 0x40289528 | FULL | Channel software trigger |

9.1.1.86 CH_STRUCT 85

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT85_CH_CTL | 0x40289540 | FULL | Channel control |
| DW0_CH_STRUCT85_CH_STATUS | 0x40289544 | FULL | Channel status |
| DW0_CH_STRUCT85_CH_IDX | 0x40289548 | FULL | Channel current indices |
| DW0_CH_STRUCT85_CH_CURR_PTR | 0x4028954C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT85_INTR | 0x40289550 | FULL | Interrupt |
| DW0_CH_STRUCT85_INTR_SET | 0x40289554 | FULL | Interrupt set |
| DW0_CH_STRUCT85_INTR_MASK | 0x40289558 | FULL | Interrupt mask |
| DW0_CH_STRUCT85_INTR_MASKED | 0x4028955C | FULL | Interrupt masked |
| DW0_CH_STRUCT85_SRAM_DATA0 | 0x40289560 | FULL | SRAM data 0 |
| DW0_CH_STRUCT85_SRAM_DATA1 | 0x40289564 | FULL | SRAM data 1 |
| DW0_CH_STRUCT85_TR_CMD | 0x40289568 | FULL | Channel software trigger |

9.1.1.87 CH_STRUCT 86

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT86_CH_CTL | 0x40289580 | FULL | Channel control |
| DW0_CH_STRUCT86_CH_STATUS | 0x40289584 | FULL | Channel status |
| DW0_CH_STRUCT86_CH_IDX | 0x40289588 | FULL | Channel current indices |
| DW0_CH_STRUCT86_CH_CURR_PTR | 0x4028958C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT86_INTR | 0x40289590 | FULL | Interrupt |
| DW0_CH_STRUCT86_INTR_SET | 0x40289594 | FULL | Interrupt set |
| DW0_CH_STRUCT86_INTR_MASK | 0x40289598 | FULL | Interrupt mask |
| DW0_CH_STRUCT86_INTR_MASKED | 0x4028959C | FULL | Interrupt masked |
| DW0_CH_STRUCT86_SRAM_DATA0 | 0x402895A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT86_SRAM_DATA1 | 0x402895A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT86_TR_CMD | 0x402895A8 | FULL | Channel software trigger |

9.1.1.88 CH_STRUCT 87

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT87_CH_CTL | 0x402895C0 | FULL | Channel control |
| DW0_CH_STRUCT87_CH_STATUS | 0x402895C4 | FULL | Channel status |
| DW0_CH_STRUCT87_CH_IDX | 0x402895C8 | FULL | Channel current indices |
| DW0_CH_STRUCT87_CH_CURR_PTR | 0x402895CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT87_INTR | 0x402895D0 | FULL | Interrupt |
| DW0_CH_STRUCT87_INTR_SET | 0x402895D4 | FULL | Interrupt set |
| DW0_CH_STRUCT87_INTR_MASK | 0x402895D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT87_INTR_MASKED | 0x402895DC | FULL | Interrupt masked |
| DW0_CH_STRUCT87_SRAM_DATA0 | 0x402895E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT87_SRAM_DATA1 | 0x402895E4 | FULL | SRAM data 1 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------|
| DW0_CH_STRUCT87_TR_CMD | 0x402895E8 | FULL | Channel software trigger |

9.1.1.89 CH_STRUCT 88

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT88_CH_CTL | 0x40289600 | FULL | Channel control |
| DW0_CH_STRUCT88_CH_STATUS | 0x40289604 | FULL | Channel status |
| DW0_CH_STRUCT88_CH_IDX | 0x40289608 | FULL | Channel current indices |
| DW0_CH_STRUCT88_CH_CURR_PTR | 0x4028960C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT88_INTR | 0x40289610 | FULL | Interrupt |
| DW0_CH_STRUCT88_INTR_SET | 0x40289614 | FULL | Interrupt set |
| DW0_CH_STRUCT88_INTR_MASK | 0x40289618 | FULL | Interrupt mask |
| DW0_CH_STRUCT88_INTR_MASKED | 0x4028961C | FULL | Interrupt masked |
| DW0_CH_STRUCT88_SRAM_DATA0 | 0x40289620 | FULL | SRAM data 0 |
| DW0_CH_STRUCT88_SRAM_DATA1 | 0x40289624 | FULL | SRAM data 1 |
| DW0_CH_STRUCT88_TR_CMD | 0x40289628 | FULL | Channel software trigger |

9.1.1.90 CH_STRUCT 89

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT89_CH_CTL | 0x40289640 | FULL | Channel control |
| DW0_CH_STRUCT89_CH_STATUS | 0x40289644 | FULL | Channel status |
| DW0_CH_STRUCT89_CH_IDX | 0x40289648 | FULL | Channel current indices |
| DW0_CH_STRUCT89_CH_CURR_PTR | 0x4028964C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT89_INTR | 0x40289650 | FULL | Interrupt |
| DW0_CH_STRUCT89_INTR_SET | 0x40289654 | FULL | Interrupt set |
| DW0_CH_STRUCT89_INTR_MASK | 0x40289658 | FULL | Interrupt mask |
| DW0_CH_STRUCT89_INTR_MASKED | 0x4028965C | FULL | Interrupt masked |
| DW0_CH_STRUCT89_SRAM_DATA0 | 0x40289660 | FULL | SRAM data 0 |
| DW0_CH_STRUCT89_SRAM_DATA1 | 0x40289664 | FULL | SRAM data 1 |
| DW0_CH_STRUCT89_TR_CMD | 0x40289668 | FULL | Channel software trigger |

9.1.1.91 CH_STRUCT 90

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT90_CH_CTL | 0x40289680 | FULL | Channel control |
| DW0_CH_STRUCT90_CH_STATUS | 0x40289684 | FULL | Channel status |
| DW0_CH_STRUCT90_CH_IDX | 0x40289688 | FULL | Channel current indices |
| DW0_CH_STRUCT90_CH_CURR_PTR | 0x4028968C | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT90_INTR | 0x40289690 | FULL | Interrupt |
| DW0_CH_STRUCT90_INTR_SET | 0x40289694 | FULL | Interrupt set |
| DW0_CH_STRUCT90_INTR_MASK | 0x40289698 | FULL | Interrupt mask |
| DW0_CH_STRUCT90_INTR_MASKED | 0x4028969C | FULL | Interrupt masked |
| DW0_CH_STRUCT90_SRAM_DATA0 | 0x402896A0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT90_SRAM_DATA1 | 0x402896A4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT90_TR_CMD | 0x402896A8 | FULL | Channel software trigger |

9.1.1.92 CH_STRUCT 91

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW0_CH_STRUCT91_CH_CTL | 0x402896C0 | FULL | Channel control |
| DW0_CH_STRUCT91_CH_STATUS | 0x402896C4 | FULL | Channel status |
| DW0_CH_STRUCT91_CH_IDX | 0x402896C8 | FULL | Channel current indices |
| DW0_CH_STRUCT91_CH_CURR_PTR | 0x402896CC | FULL | Channel current descriptor pointer |
| DW0_CH_STRUCT91_INTR | 0x402896D0 | FULL | Interrupt |
| DW0_CH_STRUCT91_INTR_SET | 0x402896D4 | FULL | Interrupt set |
| DW0_CH_STRUCT91_INTR_MASK | 0x402896D8 | FULL | Interrupt mask |
| DW0_CH_STRUCT91_INTR_MASKED | 0x402896DC | FULL | Interrupt masked |
| DW0_CH_STRUCT91_SRAM_DATA0 | 0x402896E0 | FULL | SRAM data 0 |
| DW0_CH_STRUCT91_SRAM_DATA1 | 0x402896E4 | FULL | SRAM data 1 |
| DW0_CH_STRUCT91_TR_CMD | 0x402896E8 | FULL | Channel software trigger |

9.2 DW 1

| | |
|--------------|---------------------|
| Description | Datavire Controller |
| Base Address | 0x40290000 |
| Size | 0x10000 |

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9.2.1 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|----------------------------------|
| DW1_CTL0 | 0x40290000 | FULL | Control |
| DW1_STATUS0 | 0x40290004 | FULL | Status |
| DW1_ACT_DESCR_CTL0 | 0x40290020 | FULL | Active descriptor control |
| DW1_ACT_DESCR_SRC0 | 0x40290024 | FULL | Active descriptor source |
| DW1_ACT_DESCR_DST0 | 0x40290028 | FULL | Active descriptor destination |
| DW1_ACT_DESCR_X_CTL0 | 0x40290030 | FULL | Active descriptor X loop control |
| DW1_ACT_DESCR_Y_CTL0 | 0x40290034 | FULL | Active descriptor Y loop control |
| DW1_ACT_DESCR_NEXT_PTR0 | 0x40290038 | FULL | Active descriptor next pointer |
| DW1_ACT_SRC0 | 0x40290040 | FULL | Active source |
| DW1_ACT_DST0 | 0x40290044 | FULL | Active destination |
| DW1_ECC_CTL0 | 0x40290080 | FULL | ECC control |
| DW1_CRC_CTL0 | 0x40290100 | FULL | CRC control |
| DW1_CRC_DATA_CTL0 | 0x40290110 | FULL | CRC data control |
| DW1_CRC_POL_CTL0 | 0x40290120 | FULL | CRC polynomial control |
| DW1_CRC_LFSR_CTL0 | 0x40290130 | FULL | CRC LFSR control |
| DW1_CRC_REM_CTL0 | 0x40290140 | FULL | CRC remainder control |
| DW1_CRC_REM_RESULT0 | 0x40290148 | FULL | CRC remainder result |

9.2.1.1 CH_STRUCT 0

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT0_CH_CTL | 0x40298000 | FULL | Channel control |
| DW1_CH_STRUCT0_CH_STATUS | 0x40298004 | FULL | Channel status |
| DW1_CH_STRUCT0_CH_IDX | 0x40298008 | FULL | Channel current indices |
| DW1_CH_STRUCT0_CH_CURR_PTR | 0x4029800C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT0_INTR | 0x40298010 | FULL | Interrupt |
| DW1_CH_STRUCT0_INTR_SET | 0x40298014 | FULL | Interrupt set |
| DW1_CH_STRUCT0_INTR_MASK | 0x40298018 | FULL | Interrupt mask |
| DW1_CH_STRUCT0_INTR_MASKED | 0x4029801C | FULL | Interrupt masked |
| DW1_CH_STRUCT0_SRAM_DATA0 | 0x40298020 | FULL | SRAM data 0 |
| DW1_CH_STRUCT0_SRAM_DATA1 | 0x40298024 | FULL | SRAM data 1 |
| DW1_CH_STRUCT0_TR_CMD | 0x40298028 | FULL | Channel software trigger |

9.2.1.2 CH_STRUCT 1

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT1_CH_CTL | 0x40298040 | FULL | Channel control |
| DW1_CH_STRUCT1_CH_STATUS | 0x40298044 | FULL | Channel status |
| DW1_CH_STRUCT1_CH_IDX | 0x40298048 | FULL | Channel current indices |
| DW1_CH_STRUCT1_CH_CURR_PTR | 0x4029804C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT1_INTR | 0x40298050 | FULL | Interrupt |
| DW1_CH_STRUCT1_INTR_SET | 0x40298054 | FULL | Interrupt set |
| DW1_CH_STRUCT1_INTR_MASK | 0x40298058 | FULL | Interrupt mask |
| DW1_CH_STRUCT1_INTR_MASKED | 0x4029805C | FULL | Interrupt masked |
| DW1_CH_STRUCT1_SRAM_DATA0 | 0x40298060 | FULL | SRAM data 0 |
| DW1_CH_STRUCT1_SRAM_DATA1 | 0x40298064 | FULL | SRAM data 1 |
| DW1_CH_STRUCT1_TR_CMD | 0x40298068 | FULL | Channel software trigger |

9.2.1.3 CH_STRUCT 2

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT2_CH_CTL | 0x40298080 | FULL | Channel control |
| DW1_CH_STRUCT2_CH_STATUS | 0x40298084 | FULL | Channel status |
| DW1_CH_STRUCT2_CH_IDX | 0x40298088 | FULL | Channel current indices |
| DW1_CH_STRUCT2_CH_CURR_PTR | 0x4029808C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT2_INTR | 0x40298090 | FULL | Interrupt |
| DW1_CH_STRUCT2_INTR_SET | 0x40298094 | FULL | Interrupt set |
| DW1_CH_STRUCT2_INTR_MASK | 0x40298098 | FULL | Interrupt mask |
| DW1_CH_STRUCT2_INTR_MASKED | 0x4029809C | FULL | Interrupt masked |
| DW1_CH_STRUCT2_SRAM_DATA0 | 0x402980A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT2_SRAM_DATA1 | 0x402980A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT2_TR_CMD | 0x402980A8 | FULL | Channel software trigger |

9.2.1.4 CH_STRUCT 3

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT3_CH_CTL | 0x402980C0 | FULL | Channel control |
| DW1_CH_STRUCT3_CH_STATUS | 0x402980C4 | FULL | Channel status |
| DW1_CH_STRUCT3_CH_IDX | 0x402980C8 | FULL | Channel current indices |
| DW1_CH_STRUCT3_CH_CURR_PTR | 0x402980CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT3_INTR | 0x402980D0 | FULL | Interrupt |
| DW1_CH_STRUCT3_INTR_SET | 0x402980D4 | FULL | Interrupt set |
| DW1_CH_STRUCT3_INTR_MASK | 0x402980D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT3_INTR_MASKED | 0x402980DC | FULL | Interrupt masked |
| DW1_CH_STRUCT3_SRAM_DATA0 | 0x402980E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT3_SRAM_DATA1 | 0x402980E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT3_TR_CMD | 0x402980E8 | FULL | Channel software trigger |

9.2.1.5 CH_STRUCT 4

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT4_CH_CTL | 0x40298100 | FULL | Channel control |
| DW1_CH_STRUCT4_CH_STATUS | 0x40298104 | FULL | Channel status |
| DW1_CH_STRUCT4_CH_IDX | 0x40298108 | FULL | Channel current indices |
| DW1_CH_STRUCT4_CH_CURR_PTR | 0x4029810C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT4_INTR | 0x40298110 | FULL | Interrupt |
| DW1_CH_STRUCT4_INTR_SET | 0x40298114 | FULL | Interrupt set |
| DW1_CH_STRUCT4_INTR_MASK | 0x40298118 | FULL | Interrupt mask |
| DW1_CH_STRUCT4_INTR_MASKED | 0x4029811C | FULL | Interrupt masked |
| DW1_CH_STRUCT4_SRAM_DATA0 | 0x40298120 | FULL | SRAM data 0 |
| DW1_CH_STRUCT4_SRAM_DATA1 | 0x40298124 | FULL | SRAM data 1 |
| DW1_CH_STRUCT4_TR_CMD | 0x40298128 | FULL | Channel software trigger |

9.2.1.6 CH_STRUCT 5

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT5_CH_CTL | 0x40298140 | FULL | Channel control |
| DW1_CH_STRUCT5_CH_STATUS | 0x40298144 | FULL | Channel status |
| DW1_CH_STRUCT5_CH_IDX | 0x40298148 | FULL | Channel current indices |
| DW1_CH_STRUCT5_CH_CURR_PTR | 0x4029814C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT5_INTR | 0x40298150 | FULL | Interrupt |
| DW1_CH_STRUCT5_INTR_SET | 0x40298154 | FULL | Interrupt set |
| DW1_CH_STRUCT5_INTR_MASK | 0x40298158 | FULL | Interrupt mask |
| DW1_CH_STRUCT5_INTR_MASKED | 0x4029815C | FULL | Interrupt masked |
| DW1_CH_STRUCT5_SRAM_DATA0 | 0x40298160 | FULL | SRAM data 0 |
| DW1_CH_STRUCT5_SRAM_DATA1 | 0x40298164 | FULL | SRAM data 1 |
| DW1_CH_STRUCT5_TR_CMD | 0x40298168 | FULL | Channel software trigger |

9.2.1.7 CH_STRUCT 6

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT6_CH_CTL | 0x40298180 | FULL | Channel control |
| DW1_CH_STRUCT6_CH_STATUS | 0x40298184 | FULL | Channel status |
| DW1_CH_STRUCT6_CH_IDX | 0x40298188 | FULL | Channel current indices |
| DW1_CH_STRUCT6_CH_CURR_PTR | 0x4029818C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT6_INTR | 0x40298190 | FULL | Interrupt |
| DW1_CH_STRUCT6_INTR_SET | 0x40298194 | FULL | Interrupt set |
| DW1_CH_STRUCT6_INTR_MASK | 0x40298198 | FULL | Interrupt mask |
| DW1_CH_STRUCT6_INTR_MASKED | 0x4029819C | FULL | Interrupt masked |
| DW1_CH_STRUCT6_SRAM_DATA0 | 0x402981A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT6_SRAM_DATA1 | 0x402981A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT6_TR_CMD | 0x402981A8 | FULL | Channel software trigger |

9.2.1.8 CH_STRUCT 7

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT7_CH_CTL | 0x402981C0 | FULL | Channel control |
| DW1_CH_STRUCT7_CH_STATUS | 0x402981C4 | FULL | Channel status |
| DW1_CH_STRUCT7_CH_IDX | 0x402981C8 | FULL | Channel current indices |
| DW1_CH_STRUCT7_CH_CURR_PTR | 0x402981CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT7_INTR | 0x402981D0 | FULL | Interrupt |

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--------------------------|
| DW1_CH_STRUCT7_INTR_SET | 0x402981D4 | FULL | Interrupt set |
| DW1_CH_STRUCT7_INTR_MASK | 0x402981D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT7_INTR_MASKED | 0x402981DC | FULL | Interrupt masked |
| DW1_CH_STRUCT7_SRAM_DATA0 | 0x402981E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT7_SRAM_DATA1 | 0x402981E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT7_TR_CMD | 0x402981E8 | FULL | Channel software trigger |

9.2.1.9 CH_STRUCT 8

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT8_CH_CTL | 0x40298200 | FULL | Channel control |
| DW1_CH_STRUCT8_CH_STATUS | 0x40298204 | FULL | Channel status |
| DW1_CH_STRUCT8_CH_IDX | 0x40298208 | FULL | Channel current indices |
| DW1_CH_STRUCT8_CH_CURR_PTR | 0x4029820C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT8_INTR | 0x40298210 | FULL | Interrupt |
| DW1_CH_STRUCT8_INTR_SET | 0x40298214 | FULL | Interrupt set |
| DW1_CH_STRUCT8_INTR_MASK | 0x40298218 | FULL | Interrupt mask |
| DW1_CH_STRUCT8_INTR_MASKED | 0x4029821C | FULL | Interrupt masked |
| DW1_CH_STRUCT8_SRAM_DATA0 | 0x40298220 | FULL | SRAM data 0 |
| DW1_CH_STRUCT8_SRAM_DATA1 | 0x40298224 | FULL | SRAM data 1 |
| DW1_CH_STRUCT8_TR_CMD | 0x40298228 | FULL | Channel software trigger |

9.2.1.10 CH_STRUCT 9

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT9_CH_CTL | 0x40298240 | FULL | Channel control |
| DW1_CH_STRUCT9_CH_STATUS | 0x40298244 | FULL | Channel status |
| DW1_CH_STRUCT9_CH_IDX | 0x40298248 | FULL | Channel current indices |
| DW1_CH_STRUCT9_CH_CURR_PTR | 0x4029824C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT9_INTR | 0x40298250 | FULL | Interrupt |
| DW1_CH_STRUCT9_INTR_SET | 0x40298254 | FULL | Interrupt set |
| DW1_CH_STRUCT9_INTR_MASK | 0x40298258 | FULL | Interrupt mask |
| DW1_CH_STRUCT9_INTR_MASKED | 0x4029825C | FULL | Interrupt masked |
| DW1_CH_STRUCT9_SRAM_DATA0 | 0x40298260 | FULL | SRAM data 0 |
| DW1_CH_STRUCT9_SRAM_DATA1 | 0x40298264 | FULL | SRAM data 1 |
| DW1_CH_STRUCT9_TR_CMD | 0x40298268 | FULL | Channel software trigger |

9.2.1.11 CH_STRUCT 10

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT10_CH_CTL | 0x40298280 | FULL | Channel control |
| DW1_CH_STRUCT10_CH_STATUS | 0x40298284 | FULL | Channel status |
| DW1_CH_STRUCT10_CH_IDX | 0x40298288 | FULL | Channel current indices |
| DW1_CH_STRUCT10_CH_CURR_PTR | 0x4029828C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT10_INTR | 0x40298290 | FULL | Interrupt |
| DW1_CH_STRUCT10_INTR_SET | 0x40298294 | FULL | Interrupt set |
| DW1_CH_STRUCT10_INTR_MASK | 0x40298298 | FULL | Interrupt mask |
| DW1_CH_STRUCT10_INTR_MASKED | 0x4029829C | FULL | Interrupt masked |
| DW1_CH_STRUCT10_SRAM_DATA0 | 0x402982A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT10_SRAM_DATA1 | 0x402982A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT10_TR_CMD | 0x402982A8 | FULL | Channel software trigger |

9.2.1.12 CH_STRUCT 11

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT11_CH_CTL | 0x402982C0 | FULL | Channel control |
| DW1_CH_STRUCT11_CH_STATUS | 0x402982C4 | FULL | Channel status |
| DW1_CH_STRUCT11_CH_IDX | 0x402982C8 | FULL | Channel current indices |
| DW1_CH_STRUCT11_CH_CURR_PTR | 0x402982CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT11_INTR | 0x402982D0 | FULL | Interrupt |
| DW1_CH_STRUCT11_INTR_SET | 0x402982D4 | FULL | Interrupt set |
| DW1_CH_STRUCT11_INTR_MASK | 0x402982D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT11_INTR_MASKED | 0x402982DC | FULL | Interrupt masked |
| DW1_CH_STRUCT11_SRAM_DATA0 | 0x402982E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT11_SRAM_DATA1 | 0x402982E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT11_TR_CMD | 0x402982E8 | FULL | Channel software trigger |

9.2.1.13 CH_STRUCT 12

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT12_CH_CTL | 0x40298300 | FULL | Channel control |
| DW1_CH_STRUCT12_CH_STATUS | 0x40298304 | FULL | Channel status |
| DW1_CH_STRUCT12_CH_IDX | 0x40298308 | FULL | Channel current indices |
| DW1_CH_STRUCT12_CH_CURR_PTR | 0x4029830C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT12_INTR | 0x40298310 | FULL | Interrupt |
| DW1_CH_STRUCT12_INTR_SET | 0x40298314 | FULL | Interrupt set |
| DW1_CH_STRUCT12_INTR_MASK | 0x40298318 | FULL | Interrupt mask |
| DW1_CH_STRUCT12_INTR_MASKED | 0x4029831C | FULL | Interrupt masked |
| DW1_CH_STRUCT12_SRAM_DATA0 | 0x40298320 | FULL | SRAM data 0 |
| DW1_CH_STRUCT12_SRAM_DATA1 | 0x40298324 | FULL | SRAM data 1 |
| DW1_CH_STRUCT12_TR_CMD | 0x40298328 | FULL | Channel software trigger |

9.2.1.14 CH_STRUCT 13

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT13_CH_CTL | 0x40298340 | FULL | Channel control |
| DW1_CH_STRUCT13_CH_STATUS | 0x40298344 | FULL | Channel status |
| DW1_CH_STRUCT13_CH_IDX | 0x40298348 | FULL | Channel current indices |
| DW1_CH_STRUCT13_CH_CURR_PTR | 0x4029834C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT13_INTR | 0x40298350 | FULL | Interrupt |
| DW1_CH_STRUCT13_INTR_SET | 0x40298354 | FULL | Interrupt set |
| DW1_CH_STRUCT13_INTR_MASK | 0x40298358 | FULL | Interrupt mask |
| DW1_CH_STRUCT13_INTR_MASKED | 0x4029835C | FULL | Interrupt masked |
| DW1_CH_STRUCT13_SRAM_DATA0 | 0x40298360 | FULL | SRAM data 0 |
| DW1_CH_STRUCT13_SRAM_DATA1 | 0x40298364 | FULL | SRAM data 1 |
| DW1_CH_STRUCT13_TR_CMD | 0x40298368 | FULL | Channel software trigger |

9.2.1.15 CH_STRUCT 14

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT14_CH_CTL | 0x40298380 | FULL | Channel control |
| DW1_CH_STRUCT14_CH_STATUS | 0x40298384 | FULL | Channel status |
| DW1_CH_STRUCT14_CH_IDX | 0x40298388 | FULL | Channel current indices |
| DW1_CH_STRUCT14_CH_CURR_PTR | 0x4029838C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT14_INTR | 0x40298390 | FULL | Interrupt |
| DW1_CH_STRUCT14_INTR_SET | 0x40298394 | FULL | Interrupt set |
| DW1_CH_STRUCT14_INTR_MASK | 0x40298398 | FULL | Interrupt mask |
| DW1_CH_STRUCT14_INTR_MASKED | 0x4029839C | FULL | Interrupt masked |
| DW1_CH_STRUCT14_SRAM_DATA0 | 0x402983A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT14_SRAM_DATA1 | 0x402983A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT14_TR_CMD | 0x402983A8 | FULL | Channel software trigger |

9.2.1.16 CH_STRUCT 15

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT15_CH_CTL | 0x402983C0 | FULL | Channel control |
| DW1_CH_STRUCT15_CH_STATUS | 0x402983C4 | FULL | Channel status |
| DW1_CH_STRUCT15_CH_IDX | 0x402983C8 | FULL | Channel current indices |
| DW1_CH_STRUCT15_CH_CURR_PTR | 0x402983CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT15_INTR | 0x402983D0 | FULL | Interrupt |
| DW1_CH_STRUCT15_INTR_SET | 0x402983D4 | FULL | Interrupt set |
| DW1_CH_STRUCT15_INTR_MASK | 0x402983D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT15_INTR_MASKED | 0x402983DC | FULL | Interrupt masked |
| DW1_CH_STRUCT15_SRAM_DATA0 | 0x402983E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT15_SRAM_DATA1 | 0x402983E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT15_TR_CMD | 0x402983E8 | FULL | Channel software trigger |

9.2.1.17 CH_STRUCT 16

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT16_CH_CTL | 0x40298400 | FULL | Channel control |
| DW1_CH_STRUCT16_CH_STATUS | 0x40298404 | FULL | Channel status |
| DW1_CH_STRUCT16_CH_IDX | 0x40298408 | FULL | Channel current indices |
| DW1_CH_STRUCT16_CH_CURR_PTR | 0x4029840C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT16_INTR | 0x40298410 | FULL | Interrupt |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|--------------------------|
| DW1_CH_STRUCT16_INTR_SET | 0x40298414 | FULL | Interrupt set |
| DW1_CH_STRUCT16_INTR_MASK | 0x40298418 | FULL | Interrupt mask |
| DW1_CH_STRUCT16_INTR_MASKED | 0x4029841C | FULL | Interrupt masked |
| DW1_CH_STRUCT16_SRAM_DATA0 | 0x40298420 | FULL | SRAM data 0 |
| DW1_CH_STRUCT16_SRAM_DATA1 | 0x40298424 | FULL | SRAM data 1 |
| DW1_CH_STRUCT16_TR_CMD | 0x40298428 | FULL | Channel software trigger |

9.2.1.18 CH_STRUCT 17

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT17_CH_CTL | 0x40298440 | FULL | Channel control |
| DW1_CH_STRUCT17_CH_STATUS | 0x40298444 | FULL | Channel status |
| DW1_CH_STRUCT17_CH_IDX | 0x40298448 | FULL | Channel current indices |
| DW1_CH_STRUCT17_CH_CURR_PTR | 0x4029844C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT17_INTR | 0x40298450 | FULL | Interrupt |
| DW1_CH_STRUCT17_INTR_SET | 0x40298454 | FULL | Interrupt set |
| DW1_CH_STRUCT17_INTR_MASK | 0x40298458 | FULL | Interrupt mask |
| DW1_CH_STRUCT17_INTR_MASKED | 0x4029845C | FULL | Interrupt masked |
| DW1_CH_STRUCT17_SRAM_DATA0 | 0x40298460 | FULL | SRAM data 0 |
| DW1_CH_STRUCT17_SRAM_DATA1 | 0x40298464 | FULL | SRAM data 1 |
| DW1_CH_STRUCT17_TR_CMD | 0x40298468 | FULL | Channel software trigger |

9.2.1.19 CH_STRUCT 18

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT18_CH_CTL | 0x40298480 | FULL | Channel control |
| DW1_CH_STRUCT18_CH_STATUS | 0x40298484 | FULL | Channel status |
| DW1_CH_STRUCT18_CH_IDX | 0x40298488 | FULL | Channel current indices |
| DW1_CH_STRUCT18_CH_CURR_PTR | 0x4029848C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT18_INTR | 0x40298490 | FULL | Interrupt |
| DW1_CH_STRUCT18_INTR_SET | 0x40298494 | FULL | Interrupt set |
| DW1_CH_STRUCT18_INTR_MASK | 0x40298498 | FULL | Interrupt mask |
| DW1_CH_STRUCT18_INTR_MASKED | 0x4029849C | FULL | Interrupt masked |
| DW1_CH_STRUCT18_SRAM_DATA0 | 0x402984A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT18_SRAM_DATA1 | 0x402984A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT18_TR_CMD | 0x402984A8 | FULL | Channel software trigger |

9.2.1.20 CH_STRUCT 19

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT19_CH_CTL | 0x402984C0 | FULL | Channel control |
| DW1_CH_STRUCT19_CH_STATUS | 0x402984C4 | FULL | Channel status |
| DW1_CH_STRUCT19_CH_IDX | 0x402984C8 | FULL | Channel current indices |
| DW1_CH_STRUCT19_CH_CURR_PTR | 0x402984CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT19_INTR | 0x402984D0 | FULL | Interrupt |
| DW1_CH_STRUCT19_INTR_SET | 0x402984D4 | FULL | Interrupt set |
| DW1_CH_STRUCT19_INTR_MASK | 0x402984D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT19_INTR_MASKED | 0x402984DC | FULL | Interrupt masked |
| DW1_CH_STRUCT19_SRAM_DATA0 | 0x402984E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT19_SRAM_DATA1 | 0x402984E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT19_TR_CMD | 0x402984E8 | FULL | Channel software trigger |

9.2.1.21 CH_STRUCT 20

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT20_CH_CTL | 0x40298500 | FULL | Channel control |
| DW1_CH_STRUCT20_CH_STATUS | 0x40298504 | FULL | Channel status |
| DW1_CH_STRUCT20_CH_IDX | 0x40298508 | FULL | Channel current indices |
| DW1_CH_STRUCT20_CH_CURR_PTR | 0x4029850C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT20_INTR | 0x40298510 | FULL | Interrupt |
| DW1_CH_STRUCT20_INTR_SET | 0x40298514 | FULL | Interrupt set |
| DW1_CH_STRUCT20_INTR_MASK | 0x40298518 | FULL | Interrupt mask |
| DW1_CH_STRUCT20_INTR_MASKED | 0x4029851C | FULL | Interrupt masked |
| DW1_CH_STRUCT20_SRAM_DATA0 | 0x40298520 | FULL | SRAM data 0 |
| DW1_CH_STRUCT20_SRAM_DATA1 | 0x40298524 | FULL | SRAM data 1 |
| DW1_CH_STRUCT20_TR_CMD | 0x40298528 | FULL | Channel software trigger |

9.2.1.22 CH_STRUCT 21

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT21_CH_CTL | 0x40298540 | FULL | Channel control |
| DW1_CH_STRUCT21_CH_STATUS | 0x40298544 | FULL | Channel status |
| DW1_CH_STRUCT21_CH_IDX | 0x40298548 | FULL | Channel current indices |
| DW1_CH_STRUCT21_CH_CURR_PTR | 0x4029854C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT21_INTR | 0x40298550 | FULL | Interrupt |
| DW1_CH_STRUCT21_INTR_SET | 0x40298554 | FULL | Interrupt set |
| DW1_CH_STRUCT21_INTR_MASK | 0x40298558 | FULL | Interrupt mask |
| DW1_CH_STRUCT21_INTR_MASKED | 0x4029855C | FULL | Interrupt masked |
| DW1_CH_STRUCT21_SRAM_DATA0 | 0x40298560 | FULL | SRAM data 0 |
| DW1_CH_STRUCT21_SRAM_DATA1 | 0x40298564 | FULL | SRAM data 1 |
| DW1_CH_STRUCT21_TR_CMD | 0x40298568 | FULL | Channel software trigger |

9.2.1.23 CH_STRUCT 22

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT22_CH_CTL | 0x40298580 | FULL | Channel control |
| DW1_CH_STRUCT22_CH_STATUS | 0x40298584 | FULL | Channel status |
| DW1_CH_STRUCT22_CH_IDX | 0x40298588 | FULL | Channel current indices |
| DW1_CH_STRUCT22_CH_CURR_PTR | 0x4029858C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT22_INTR | 0x40298590 | FULL | Interrupt |
| DW1_CH_STRUCT22_INTR_SET | 0x40298594 | FULL | Interrupt set |
| DW1_CH_STRUCT22_INTR_MASK | 0x40298598 | FULL | Interrupt mask |
| DW1_CH_STRUCT22_INTR_MASKED | 0x4029859C | FULL | Interrupt masked |
| DW1_CH_STRUCT22_SRAM_DATA0 | 0x402985A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT22_SRAM_DATA1 | 0x402985A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT22_TR_CMD | 0x402985A8 | FULL | Channel software trigger |

9.2.1.24 CH_STRUCT 23

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT23_CH_CTL | 0x402985C0 | FULL | Channel control |
| DW1_CH_STRUCT23_CH_STATUS | 0x402985C4 | FULL | Channel status |
| DW1_CH_STRUCT23_CH_IDX | 0x402985C8 | FULL | Channel current indices |
| DW1_CH_STRUCT23_CH_CURR_PTR | 0x402985CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT23_INTR | 0x402985D0 | FULL | Interrupt |
| DW1_CH_STRUCT23_INTR_SET | 0x402985D4 | FULL | Interrupt set |
| DW1_CH_STRUCT23_INTR_MASK | 0x402985D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT23_INTR_MASKED | 0x402985DC | FULL | Interrupt masked |
| DW1_CH_STRUCT23_SRAM_DATA0 | 0x402985E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT23_SRAM_DATA1 | 0x402985E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT23_TR_CMD | 0x402985E8 | FULL | Channel software trigger |

9.2.1.25 CH_STRUCT 24

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT24_CH_CTL | 0x40298600 | FULL | Channel control |
| DW1_CH_STRUCT24_CH_STATUS | 0x40298604 | FULL | Channel status |
| DW1_CH_STRUCT24_CH_IDX | 0x40298608 | FULL | Channel current indices |
| DW1_CH_STRUCT24_CH_CURR_PTR | 0x4029860C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT24_INTR | 0x40298610 | FULL | Interrupt |
| DW1_CH_STRUCT24_INTR_SET | 0x40298614 | FULL | Interrupt set |
| DW1_CH_STRUCT24_INTR_MASK | 0x40298618 | FULL | Interrupt mask |
| DW1_CH_STRUCT24_INTR_MASKED | 0x4029861C | FULL | Interrupt masked |
| DW1_CH_STRUCT24_SRAM_DATA0 | 0x40298620 | FULL | SRAM data 0 |
| DW1_CH_STRUCT24_SRAM_DATA1 | 0x40298624 | FULL | SRAM data 1 |
| DW1_CH_STRUCT24_TR_CMD | 0x40298628 | FULL | Channel software trigger |

9.2.1.26 CH_STRUCT 25

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT25_CH_CTL | 0x40298640 | FULL | Channel control |
| DW1_CH_STRUCT25_CH_STATUS | 0x40298644 | FULL | Channel status |
| DW1_CH_STRUCT25_CH_IDX | 0x40298648 | FULL | Channel current indices |
| DW1_CH_STRUCT25_CH_CURR_PTR | 0x4029864C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT25_INTR | 0x40298650 | FULL | Interrupt |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|--------------------------|
| DW1_CH_STRUCT25_INTR_SET | 0x40298654 | FULL | Interrupt set |
| DW1_CH_STRUCT25_INTR_MASK | 0x40298658 | FULL | Interrupt mask |
| DW1_CH_STRUCT25_INTR_MASKED | 0x4029865C | FULL | Interrupt masked |
| DW1_CH_STRUCT25_SRAM_DATA0 | 0x40298660 | FULL | SRAM data 0 |
| DW1_CH_STRUCT25_SRAM_DATA1 | 0x40298664 | FULL | SRAM data 1 |
| DW1_CH_STRUCT25_TR_CMD | 0x40298668 | FULL | Channel software trigger |

9.2.1.27 CH_STRUCT 26

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT26_CH_CTL | 0x40298680 | FULL | Channel control |
| DW1_CH_STRUCT26_CH_STATUS | 0x40298684 | FULL | Channel status |
| DW1_CH_STRUCT26_CH_IDX | 0x40298688 | FULL | Channel current indices |
| DW1_CH_STRUCT26_CH_CURR_PTR | 0x4029868C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT26_INTR | 0x40298690 | FULL | Interrupt |
| DW1_CH_STRUCT26_INTR_SET | 0x40298694 | FULL | Interrupt set |
| DW1_CH_STRUCT26_INTR_MASK | 0x40298698 | FULL | Interrupt mask |
| DW1_CH_STRUCT26_INTR_MASKED | 0x4029869C | FULL | Interrupt masked |
| DW1_CH_STRUCT26_SRAM_DATA0 | 0x402986A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT26_SRAM_DATA1 | 0x402986A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT26_TR_CMD | 0x402986A8 | FULL | Channel software trigger |

9.2.1.28 CH_STRUCT 27

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT27_CH_CTL | 0x402986C0 | FULL | Channel control |
| DW1_CH_STRUCT27_CH_STATUS | 0x402986C4 | FULL | Channel status |
| DW1_CH_STRUCT27_CH_IDX | 0x402986C8 | FULL | Channel current indices |
| DW1_CH_STRUCT27_CH_CURR_PTR | 0x402986CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT27_INTR | 0x402986D0 | FULL | Interrupt |
| DW1_CH_STRUCT27_INTR_SET | 0x402986D4 | FULL | Interrupt set |
| DW1_CH_STRUCT27_INTR_MASK | 0x402986D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT27_INTR_MASKED | 0x402986DC | FULL | Interrupt masked |
| DW1_CH_STRUCT27_SRAM_DATA0 | 0x402986E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT27_SRAM_DATA1 | 0x402986E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT27_TR_CMD | 0x402986E8 | FULL | Channel software trigger |

9.2.1.29 CH_STRUCT 28

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT28_CH_CTL | 0x40298700 | FULL | Channel control |
| DW1_CH_STRUCT28_CH_STATUS | 0x40298704 | FULL | Channel status |
| DW1_CH_STRUCT28_CH_IDX | 0x40298708 | FULL | Channel current indices |
| DW1_CH_STRUCT28_CH_CURR_PTR | 0x4029870C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT28_INTR | 0x40298710 | FULL | Interrupt |
| DW1_CH_STRUCT28_INTR_SET | 0x40298714 | FULL | Interrupt set |
| DW1_CH_STRUCT28_INTR_MASK | 0x40298718 | FULL | Interrupt mask |
| DW1_CH_STRUCT28_INTR_MASKED | 0x4029871C | FULL | Interrupt masked |
| DW1_CH_STRUCT28_SRAM_DATA0 | 0x40298720 | FULL | SRAM data 0 |
| DW1_CH_STRUCT28_SRAM_DATA1 | 0x40298724 | FULL | SRAM data 1 |
| DW1_CH_STRUCT28_TR_CMD | 0x40298728 | FULL | Channel software trigger |

9.2.1.30 CH_STRUCT 29

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT29_CH_CTL | 0x40298740 | FULL | Channel control |
| DW1_CH_STRUCT29_CH_STATUS | 0x40298744 | FULL | Channel status |
| DW1_CH_STRUCT29_CH_IDX | 0x40298748 | FULL | Channel current indices |
| DW1_CH_STRUCT29_CH_CURR_PTR | 0x4029874C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT29_INTR | 0x40298750 | FULL | Interrupt |
| DW1_CH_STRUCT29_INTR_SET | 0x40298754 | FULL | Interrupt set |
| DW1_CH_STRUCT29_INTR_MASK | 0x40298758 | FULL | Interrupt mask |
| DW1_CH_STRUCT29_INTR_MASKED | 0x4029875C | FULL | Interrupt masked |
| DW1_CH_STRUCT29_SRAM_DATA0 | 0x40298760 | FULL | SRAM data 0 |
| DW1_CH_STRUCT29_SRAM_DATA1 | 0x40298764 | FULL | SRAM data 1 |
| DW1_CH_STRUCT29_TR_CMD | 0x40298768 | FULL | Channel software trigger |

9.2.1.31 CH_STRUCT 30

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT30_CH_CTL | 0x40298780 | FULL | Channel control |
| DW1_CH_STRUCT30_CH_STATUS | 0x40298784 | FULL | Channel status |
| DW1_CH_STRUCT30_CH_IDX | 0x40298788 | FULL | Channel current indices |
| DW1_CH_STRUCT30_CH_CURR_PTR | 0x4029878C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT30_INTR | 0x40298790 | FULL | Interrupt |
| DW1_CH_STRUCT30_INTR_SET | 0x40298794 | FULL | Interrupt set |
| DW1_CH_STRUCT30_INTR_MASK | 0x40298798 | FULL | Interrupt mask |
| DW1_CH_STRUCT30_INTR_MASKED | 0x4029879C | FULL | Interrupt masked |
| DW1_CH_STRUCT30_SRAM_DATA0 | 0x402987A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT30_SRAM_DATA1 | 0x402987A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT30_TR_CMD | 0x402987A8 | FULL | Channel software trigger |

9.2.1.32 CH_STRUCT 31

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT31_CH_CTL | 0x402987C0 | FULL | Channel control |
| DW1_CH_STRUCT31_CH_STATUS | 0x402987C4 | FULL | Channel status |
| DW1_CH_STRUCT31_CH_IDX | 0x402987C8 | FULL | Channel current indices |
| DW1_CH_STRUCT31_CH_CURR_PTR | 0x402987CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT31_INTR | 0x402987D0 | FULL | Interrupt |
| DW1_CH_STRUCT31_INTR_SET | 0x402987D4 | FULL | Interrupt set |
| DW1_CH_STRUCT31_INTR_MASK | 0x402987D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT31_INTR_MASKED | 0x402987DC | FULL | Interrupt masked |
| DW1_CH_STRUCT31_SRAM_DATA0 | 0x402987E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT31_SRAM_DATA1 | 0x402987E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT31_TR_CMD | 0x402987E8 | FULL | Channel software trigger |

9.2.1.33 CH_STRUCT 32

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT32_CH_CTL | 0x40298800 | FULL | Channel control |
| DW1_CH_STRUCT32_CH_STATUS | 0x40298804 | FULL | Channel status |
| DW1_CH_STRUCT32_CH_IDX | 0x40298808 | FULL | Channel current indices |
| DW1_CH_STRUCT32_CH_CURR_PTR | 0x4029880C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT32_INTR | 0x40298810 | FULL | Interrupt |
| DW1_CH_STRUCT32_INTR_SET | 0x40298814 | FULL | Interrupt set |
| DW1_CH_STRUCT32_INTR_MASK | 0x40298818 | FULL | Interrupt mask |
| DW1_CH_STRUCT32_INTR_MASKED | 0x4029881C | FULL | Interrupt masked |
| DW1_CH_STRUCT32_SRAM_DATA0 | 0x40298820 | FULL | SRAM data 0 |
| DW1_CH_STRUCT32_SRAM_DATA1 | 0x40298824 | FULL | SRAM data 1 |
| DW1_CH_STRUCT32_TR_CMD | 0x40298828 | FULL | Channel software trigger |

9.2.1.34 CH_STRUCT 33

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT33_CH_CTL | 0x40298840 | FULL | Channel control |
| DW1_CH_STRUCT33_CH_STATUS | 0x40298844 | FULL | Channel status |
| DW1_CH_STRUCT33_CH_IDX | 0x40298848 | FULL | Channel current indices |
| DW1_CH_STRUCT33_CH_CURR_PTR | 0x4029884C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT33_INTR | 0x40298850 | FULL | Interrupt |
| DW1_CH_STRUCT33_INTR_SET | 0x40298854 | FULL | Interrupt set |
| DW1_CH_STRUCT33_INTR_MASK | 0x40298858 | FULL | Interrupt mask |
| DW1_CH_STRUCT33_INTR_MASKED | 0x4029885C | FULL | Interrupt masked |
| DW1_CH_STRUCT33_SRAM_DATA0 | 0x40298860 | FULL | SRAM data 0 |
| DW1_CH_STRUCT33_SRAM_DATA1 | 0x40298864 | FULL | SRAM data 1 |
| DW1_CH_STRUCT33_TR_CMD | 0x40298868 | FULL | Channel software trigger |

9.2.1.35 CH_STRUCT 34

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT34_CH_CTL | 0x40298880 | FULL | Channel control |
| DW1_CH_STRUCT34_CH_STATUS | 0x40298884 | FULL | Channel status |
| DW1_CH_STRUCT34_CH_IDX | 0x40298888 | FULL | Channel current indices |
| DW1_CH_STRUCT34_CH_CURR_PTR | 0x4029888C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT34_INTR | 0x40298890 | FULL | Interrupt |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|--------------------------|
| DW1_CH_STRUCT34_INTR_SET | 0x40298894 | FULL | Interrupt set |
| DW1_CH_STRUCT34_INTR_MASK | 0x40298898 | FULL | Interrupt mask |
| DW1_CH_STRUCT34_INTR_MASKED | 0x4029889C | FULL | Interrupt masked |
| DW1_CH_STRUCT34_SRAM_DATA0 | 0x402988A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT34_SRAM_DATA1 | 0x402988A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT34_TR_CMD | 0x402988A8 | FULL | Channel software trigger |

9.2.1.36 CH_STRUCT 35

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT35_CH_CTL | 0x402988C0 | FULL | Channel control |
| DW1_CH_STRUCT35_CH_STATUS | 0x402988C4 | FULL | Channel status |
| DW1_CH_STRUCT35_CH_IDX | 0x402988C8 | FULL | Channel current indices |
| DW1_CH_STRUCT35_CH_CURR_PTR | 0x402988CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT35_INTR | 0x402988D0 | FULL | Interrupt |
| DW1_CH_STRUCT35_INTR_SET | 0x402988D4 | FULL | Interrupt set |
| DW1_CH_STRUCT35_INTR_MASK | 0x402988D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT35_INTR_MASKED | 0x402988DC | FULL | Interrupt masked |
| DW1_CH_STRUCT35_SRAM_DATA0 | 0x402988E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT35_SRAM_DATA1 | 0x402988E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT35_TR_CMD | 0x402988E8 | FULL | Channel software trigger |

9.2.1.37 CH_STRUCT 36

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT36_CH_CTL | 0x40298900 | FULL | Channel control |
| DW1_CH_STRUCT36_CH_STATUS | 0x40298904 | FULL | Channel status |
| DW1_CH_STRUCT36_CH_IDX | 0x40298908 | FULL | Channel current indices |
| DW1_CH_STRUCT36_CH_CURR_PTR | 0x4029890C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT36_INTR | 0x40298910 | FULL | Interrupt |
| DW1_CH_STRUCT36_INTR_SET | 0x40298914 | FULL | Interrupt set |
| DW1_CH_STRUCT36_INTR_MASK | 0x40298918 | FULL | Interrupt mask |
| DW1_CH_STRUCT36_INTR_MASKED | 0x4029891C | FULL | Interrupt masked |
| DW1_CH_STRUCT36_SRAM_DATA0 | 0x40298920 | FULL | SRAM data 0 |
| DW1_CH_STRUCT36_SRAM_DATA1 | 0x40298924 | FULL | SRAM data 1 |
| DW1_CH_STRUCT36_TR_CMD | 0x40298928 | FULL | Channel software trigger |

9.2.1.38 CH_STRUCT 37

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT37_CH_CTL | 0x40298940 | FULL | Channel control |
| DW1_CH_STRUCT37_CH_STATUS | 0x40298944 | FULL | Channel status |
| DW1_CH_STRUCT37_CH_IDX | 0x40298948 | FULL | Channel current indices |
| DW1_CH_STRUCT37_CH_CURR_PTR | 0x4029894C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT37_INTR | 0x40298950 | FULL | Interrupt |
| DW1_CH_STRUCT37_INTR_SET | 0x40298954 | FULL | Interrupt set |
| DW1_CH_STRUCT37_INTR_MASK | 0x40298958 | FULL | Interrupt mask |
| DW1_CH_STRUCT37_INTR_MASKED | 0x4029895C | FULL | Interrupt masked |
| DW1_CH_STRUCT37_SRAM_DATA0 | 0x40298960 | FULL | SRAM data 0 |
| DW1_CH_STRUCT37_SRAM_DATA1 | 0x40298964 | FULL | SRAM data 1 |
| DW1_CH_STRUCT37_TR_CMD | 0x40298968 | FULL | Channel software trigger |

9.2.1.39 CH_STRUCT 38

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT38_CH_CTL | 0x40298980 | FULL | Channel control |
| DW1_CH_STRUCT38_CH_STATUS | 0x40298984 | FULL | Channel status |
| DW1_CH_STRUCT38_CH_IDX | 0x40298988 | FULL | Channel current indices |
| DW1_CH_STRUCT38_CH_CURR_PTR | 0x4029898C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT38_INTR | 0x40298990 | FULL | Interrupt |
| DW1_CH_STRUCT38_INTR_SET | 0x40298994 | FULL | Interrupt set |
| DW1_CH_STRUCT38_INTR_MASK | 0x40298998 | FULL | Interrupt mask |
| DW1_CH_STRUCT38_INTR_MASKED | 0x4029899C | FULL | Interrupt masked |
| DW1_CH_STRUCT38_SRAM_DATA0 | 0x402989A0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT38_SRAM_DATA1 | 0x402989A4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT38_TR_CMD | 0x402989A8 | FULL | Channel software trigger |

9.2.1.40 CH_STRUCT 39

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT39_CH_CTL | 0x402989C0 | FULL | Channel control |
| DW1_CH_STRUCT39_CH_STATUS | 0x402989C4 | FULL | Channel status |
| DW1_CH_STRUCT39_CH_IDX | 0x402989C8 | FULL | Channel current indices |
| DW1_CH_STRUCT39_CH_CURR_PTR | 0x402989CC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT39_INTR | 0x402989D0 | FULL | Interrupt |
| DW1_CH_STRUCT39_INTR_SET | 0x402989D4 | FULL | Interrupt set |
| DW1_CH_STRUCT39_INTR_MASK | 0x402989D8 | FULL | Interrupt mask |
| DW1_CH_STRUCT39_INTR_MASKED | 0x402989DC | FULL | Interrupt masked |
| DW1_CH_STRUCT39_SRAM_DATA0 | 0x402989E0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT39_SRAM_DATA1 | 0x402989E4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT39_TR_CMD | 0x402989E8 | FULL | Channel software trigger |

9.2.1.41 CH_STRUCT 40

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT40_CH_CTL | 0x40298A00 | FULL | Channel control |
| DW1_CH_STRUCT40_CH_STATUS | 0x40298A04 | FULL | Channel status |
| DW1_CH_STRUCT40_CH_IDX | 0x40298A08 | FULL | Channel current indices |
| DW1_CH_STRUCT40_CH_CURR_PTR | 0x40298A0C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT40_INTR | 0x40298A10 | FULL | Interrupt |
| DW1_CH_STRUCT40_INTR_SET | 0x40298A14 | FULL | Interrupt set |
| DW1_CH_STRUCT40_INTR_MASK | 0x40298A18 | FULL | Interrupt mask |
| DW1_CH_STRUCT40_INTR_MASKED | 0x40298A1C | FULL | Interrupt masked |
| DW1_CH_STRUCT40_SRAM_DATA0 | 0x40298A20 | FULL | SRAM data 0 |
| DW1_CH_STRUCT40_SRAM_DATA1 | 0x40298A24 | FULL | SRAM data 1 |
| DW1_CH_STRUCT40_TR_CMD | 0x40298A28 | FULL | Channel software trigger |

9.2.1.42 CH_STRUCT 41

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT41_CH_CTL | 0x40298A40 | FULL | Channel control |
| DW1_CH_STRUCT41_CH_STATUS | 0x40298A44 | FULL | Channel status |
| DW1_CH_STRUCT41_CH_IDX | 0x40298A48 | FULL | Channel current indices |
| DW1_CH_STRUCT41_CH_CURR_PTR | 0x40298A4C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT41_INTR | 0x40298A50 | FULL | Interrupt |
| DW1_CH_STRUCT41_INTR_SET | 0x40298A54 | FULL | Interrupt set |
| DW1_CH_STRUCT41_INTR_MASK | 0x40298A58 | FULL | Interrupt mask |
| DW1_CH_STRUCT41_INTR_MASKED | 0x40298A5C | FULL | Interrupt masked |
| DW1_CH_STRUCT41_SRAM_DATA0 | 0x40298A60 | FULL | SRAM data 0 |
| DW1_CH_STRUCT41_SRAM_DATA1 | 0x40298A64 | FULL | SRAM data 1 |
| DW1_CH_STRUCT41_TR_CMD | 0x40298A68 | FULL | Channel software trigger |

9.2.1.43 CH_STRUCT 42

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT42_CH_CTL | 0x40298A80 | FULL | Channel control |
| DW1_CH_STRUCT42_CH_STATUS | 0x40298A84 | FULL | Channel status |
| DW1_CH_STRUCT42_CH_IDX | 0x40298A88 | FULL | Channel current indices |
| DW1_CH_STRUCT42_CH_CURR_PTR | 0x40298A8C | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT42_INTR | 0x40298A90 | FULL | Interrupt |
| DW1_CH_STRUCT42_INTR_SET | 0x40298A94 | FULL | Interrupt set |
| DW1_CH_STRUCT42_INTR_MASK | 0x40298A98 | FULL | Interrupt mask |
| DW1_CH_STRUCT42_INTR_MASKED | 0x40298A9C | FULL | Interrupt masked |
| DW1_CH_STRUCT42_SRAM_DATA0 | 0x40298AA0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT42_SRAM_DATA1 | 0x40298AA4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT42_TR_CMD | 0x40298AA8 | FULL | Channel software trigger |

9.2.1.44 CH_STRUCT 43

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|------------------------------------|
| DW1_CH_STRUCT43_CH_CTL | 0x40298AC0 | FULL | Channel control |
| DW1_CH_STRUCT43_CH_STATUS | 0x40298AC4 | FULL | Channel status |
| DW1_CH_STRUCT43_CH_IDX | 0x40298AC8 | FULL | Channel current indices |
| DW1_CH_STRUCT43_CH_CURR_PTR | 0x40298ACC | FULL | Channel current descriptor pointer |
| DW1_CH_STRUCT43_INTR | 0x40298AD0 | FULL | Interrupt |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|--------------------------|
| DW1_CH_STRUCT43_INTR_SET | 0x40298AD4 | FULL | Interrupt set |
| DW1_CH_STRUCT43_INTR_MASK | 0x40298AD8 | FULL | Interrupt mask |
| DW1_CH_STRUCT43_INTR_MASKED | 0x40298ADC | FULL | Interrupt masked |
| DW1_CH_STRUCT43_SRAM_DATA0 | 0x40298AE0 | FULL | SRAM data 0 |
| DW1_CH_STRUCT43_SRAM_DATA1 | 0x40298AE4 | FULL | SRAM data 1 |
| DW1_CH_STRUCT43_TR_CMD | 0x40298AE8 | FULL | Channel software trigger |

9.3 Register Details

9.3.1 DW_CTL

Description: Control
Address: 0x40280000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|------------------|--------------|
| Name | None [7:2] | | | | | | ECC_INJ_EN [1:1] | ECC_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | ECC_EN | RW | R | 1 | Enable ECC checking: '0': Disabled. '1': Enabled. |
| 1 | ECC_INJ_EN | RW | R | 0 | Enable parity injection for SRAM. When '1', the parity (ECC_CTL.PARITY) is used when a full 32-bit write is done to the ECC_CTL.WORD_ADDR word address of the SRAM. |
| 31 | ENABLED | RW | R | 0 | IP enable: '0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected). '1': Enabled. |

9.3.2 DW_STATUS

Description: Status
Address: 0x40280004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|------------|---------|----------|---------|
| Name | PC [7:4] | | | | None [3:3] | B [2:2] | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|---------------------|--------------|------------|---|
| Name | None [15:12] | | | | PREEMPTABLE [11:11] | None [10:10] | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | CH_IDX [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|---------------|----|----|--------------|----|----|----------------|
| Name | ACTIVE [31:31] | STATE [30:28] | | | None [27:25] | | | CH_IDX [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 0 | P | R | RW | Undefined | Active channel, user/privileged access control: '0': user mode. '1': privileged mode. |
| 1 | NS | R | RW | Undefined | Active channel, secure/non-secure access control: '0': secure. '1': non-secure. |
| 2 | B | R | RW | Undefined | Active channel, non-bufferable/bufferable access control: '0': non-bufferable '1': bufferable. |
| 4:7 | PC | R | RW | Undefined | Active channel protection context. |
| 8:9 | PRIO | R | W | Undefined | Active channel priority. |
| 11 | PREEMPTABLE | R | W | Undefined | Active channel preemptable. |
| 16:24 | CH_IDX | R | W | Undefined | Active channel index. |
| 28:30 | STATE | R | W | 0 | State of the DW controller. '0': Default/inactive state. '1': Loading descriptor. '2': Loading data element from source location. '3': Storing data element to destination location. '4': CRC functionality (only used for CRC transfer descriptor type). '5': Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation. '6': Error. |
| 31 | ACTIVE | R | W | 0 | Active channel present: '0': No. '1': Yes. |

9.3.3 DW_ACT_DESCR_CTL

Description: Active descriptor control
Address: 0x40280020
Offset: 0x20
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | DATA | R | W | Undefined | <p>Copy of DESCR_CTL of the currently active descriptor.</p> <p>[1:0] WAIT_FOR_DEACT Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to '0'). The wait cycles incurred by this field reduce DW controller performance. '0': Do not wait for trigger de-activation (for pulse sensitive triggers). '1': Wait for up to 4 cycles. '2': Wait for up to 16 cycles. '3': Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated.</p> <p>[3:2] INTR_TYPE Specifies the input trigger type (not to be confused with the descriptor type): '0': A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. '1': A trigger results in the execution of a single 1D transfer. - If the descriptor type is 'single', the trigger results in the execution of a single transfer. - If the descriptor type is '1D' or '2D', the trigger results in the execution of a 1D transfer. '2': A trigger results in the execution of the current descriptor. '3': A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information.</p> <p>[5:4] TR_OUT_TYPE Specifies when an output trigger is generated: '0': An output trigger is generated after a single transfer. '1': An output trigger is generated after a single 1D transfer. - If the descriptor type is 'single', the output trigger is generated after a single transfer. - If the descriptor type is '1D', 'CRC' or '2D', the output trigger is generated after the execution of a 1D transfer. '2': An output trigger is generated after the execution of the current descriptor. '3': An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor DESCR_NEXT_PTR.ADDR is '0'.</p> <p>[7:6] TR_IN_TYPE Specifies the input trigger type (not to be confused with the descriptor type): '0': A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. '1': A trigger results in the execution of a single 1D transfer.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| | | | | | <p>(Continuation)</p> <ul style="list-style-type: none"> - If the descriptor type is 'single', the trigger results in the execution of a single transfer. - If the descriptor type is '1D' or '2D', the trigger results in the execution of a 1D transfer. <p>'2': A trigger results in the execution of the current descriptor.</p> <p>'3': A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information.</p> <p>[24] CH_DISABLE Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled.</p> <p>Note: a disabled channel will ignore its input trigger.</p> <p>[26] SRC_TRANSFER_SIZE Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>[27] DST_TRANSFER_SIZE Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>[29:28] DATA_SIZE Specifies the data element size: '0': Byte (8 bits). '1': Halfword (16 bits). '2': Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: <ul style="list-style-type: none"> - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24bits are made '0'). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made '0'). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made '0'). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made '0'). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. </p> <p>[31:30] DESCR_TYPE Specifies the descriptor type (not to be confused with the trigger type): '0': Single transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are not present and DESCR_NEXT_PTR is at offset 0x0c.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| | | | | | <p>(Continuation)</p> <p>'1': 1D transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A 1D transfer consists out of DESCR_X_CTL.X_COUNT single transfers.</p> <p>'2': 2D transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are present and DESCR_NEXT_PTR is at offset 0x14. A 2D transfer consists of DESCR_X_CTL.X_COUNT*DESCR_Y_CTL.Y_COUNT single transfers.</p> <p>'3': CRC transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A CRC transfer consists out of DESCR_X_CTL.X_COUNT single transfers.</p> <p>After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to '0'.</p> |

9.3.4 DW_ACT_DESCR_SRC

Description: Active descriptor source
Address: 0x40280024
Offset: 0x24
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | DATA | R | W | Undefined | Copy of DESCR_SRC of the currently active descriptor. Base address of source location. |

9.3.5 DW_ACT_DESCR_DST

Description: Active descriptor destination
Address: 0x40280028
Offset: 0x28
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | DATA | R | W | Undefined | <p>Copy of DESCR_DST of the currently active descriptor.</p> <p>Base address of destination location.</p> <p>Note: For a CRC transfer descriptor, this field should be programmed with the address of the CRC_LFSR_CTL register. The calculated CRC LFSR state is written to this address (through the CRYPTO AHB-Lite master interface) when the input trigger is processed. The write transfer will be submitted to the CPUSS and PERI protection schemes.</p> |

9.3.6 DW_ACT_DESCR_X_CTL

Description: Active descriptor X loop control
Address: 0x40280030
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment: If the currently active descriptor has not X_CTL register, this MMIO register provides undefined information.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | DATA | R | W | Undefined | <p>Copy of DESCR_X_CTL of the currently active descriptor.</p> <p>[11:0] SRC_X_INCR Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is '0', the source address is not incremented. This is useful for reading from RX FIFO structures.</p> <p>[23:12] DST_X_INCR Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is '0', the destination address is not incremented. This is useful for writing to TX FIFO structures.</p> <p>Note: this field is not used for CRC transfer descriptors and must be set to '0'.</p> <p>[31:24] X_COUNT Number of iterations (minus 1) of the 'X loop' (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations.</p> <p>For a single transfer descriptor type, descriptor will not have X_CTL.</p> |

9.3.7 DW_ACT_DESCR_Y_CTL

Description: Active descriptor Y loop control
Address: 0x40280034
Offset: 0x34
Retention: Not Retained
IsDeepSleep: No
Comment: If the currently active descriptor has not Y_CTL register, this MMIO register provides undefined information.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | DATA | R | W | Undefined | <p>Copy of DESCR_Y_CTL of the currently active descriptor.</p> <p>[11:0] SRC_Y_INCR Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047].</p> <p>[23:12] DST_Y_INCR Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047].</p> <p>[31:24] Y_COUNT Number of iterations (minus 1) of the 'Y loop' (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations.</p> <p>For single, 1D and CRC transfer descriptor types, descriptor will not have Y_CTL.</p> |

9.3.8 DW_ACT_DESCR_NEXT_PTR

Description: Active descriptor next pointer
Address: 0x40280038
Offset: 0x38
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 2:31 | ADDR | R | W | Undefined | Copy of DESCR_NEXT_PTR of the currently active descriptor. [31:2] ADDR Address of next descriptor in descriptor list. When this field is '0', this is the last descriptor in the descriptor list. |

9.3.9 DW_ACT_SRC

Description: Active source
Address: 0x40280040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | SRC_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | SRC_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | SRC_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | SRC_ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|-------------------------------------|
| 0:31 | SRC_ADDR | R | W | Undefined | Current address of source location. |

9.3.10 DW_ACT_DST

Description: Active destination
Address: 0x40280044
Offset: 0x44
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | DST_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | DST_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | DST_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | DST_ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:31 | DST_ADDR | R | W | Undefined | Current address of destination location. |

9.3.11 DW_ECC_CTL

Description: ECC control
Address: 0x40280080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|----|-----------------|--------------|
| Name | WORD_ADDR [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | WORD_ADDR [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PARITY [31:25] | | | | | | | None [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|---|
| 0:9 | WORD_ADDR | RW | R | 0 | Specifies the word address where an error will be injected. - On a write transfer to this SRAM word address and when CTL.ECC_INJ_EN bit is '1', the parity (PARITY) is injected. |
| 25:31 | PARITY | RW | R | 0 | ECC parity to use for ECC error injection at address WORD_ADDR. |

9.3.12 DW_CRC_CTL

Description: CRC control
Address: 0x40280100
Offset: 0x100
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|--------------------|
| Name | None [7:1] | | | | | | | DATA_REVERSE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-------------------|
| Name | None [15:9] | | | | | | | REM_REVERSE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0 | DATA_REVERSE | RW | R | 0 | Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. |
| 8 | REM_REVERSE | RW | R | 0 | Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. |

9.3.13 DW_CRC_DATA_CTL

Description: CRC data control
Address: 0x40280110
Offset: 0x110
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | DATA_XOR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:7 | DATA_XOR | RW | R | 0 | Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. |

9.3.14 DW_CRC_POL_CTL

Description: CRC polynomial control
Address: 0x40280120
Offset: 0x120
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | POLYNOMIAL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | POLYNOMIAL [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | POLYNOMIAL [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | POLYNOMIAL [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:31 | POLYNOMIAL | RW | R | 0 | CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 ($x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$). - CRC16: POLYNOMIAL is 0x80050000 ($x^{16} + x^{15} + x^2 + 1$, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 ($x^{16} + x^{12} + x^5 + 1$, shifted by 16 bit positions). |

9.3.15 DW_CRC_LFSR_CTL

Description: CRC LFSR control
Address: 0x40280130
Offset: 0x130
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | LFSR32 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | LFSR32 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | LFSR32 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | LFSR32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | LFSR32 | RW | RW | 0 | <p>State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value.</p> <p>The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's.</p> <p>Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT).</p> |

9.3.16 DW_CRC_REM_CTL

Description: CRC remainder control
Address: 0x40280140
Offset: 0x140
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | REM_XOR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | REM_XOR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | REM_XOR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | REM_XOR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:31 | REM_XOR | RW | R | 0 | Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. |

9.3.17 DW_CRC_REM_RESULT

Description: CRC remainder result
Address: 0x40280148
Offset: 0x148
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | REM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | REM [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | REM [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | REM [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | REM | R | W | 0 | <p>Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder.</p> <p>Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_CTL.REM_REVERSE and CRC_REM_CTL.REM_XOR.</p> |

9.3.18 CH_STRUCT

9.3.18.1 DW_CH_STRUCT_CH_CTL

Description: Channel control
Address: 0x40288000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|------------|---------|----------|---------|
| Name | PC [7:4] | | | | None [3:3] | B [2:2] | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-------------------------|-----------------|------------|---|
| Name | None [15:12] | | | | PREEMPTAB LE [11:11] | None [10:10] | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|--------------|----|----|----|----|----|----|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | P | RW | R | Undefined | User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the P field for the user/privileged access control ('hprot[1]'). |
| 1 | NS | RW | R | Undefined | Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the NS field for the secure/non-secure access control ('hprot[4]'). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|------|-----------------|--|
| 2 | B | RW | R | Undefined | <p>Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable.</p> <p>This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data.</p> <p>All transactions for this channel uses the B field for the non-bufferable/bufferable access control ('hprot[2]').</p> |
| 4:7 | PC | RW | R | Undefined | <p>Protection context.</p> <p>This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R).</p> <p>All transactions for this channel uses the PC field for the protection context.</p> |
| 8:9 | PRI0 | RW | R | 0 | <p>Channel priority: '0': highest priority. '1' '2' '3': lowest priority.</p> <p>Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group).</p> |
| 11 | PREEMPTABLE | RW | R | Undefined | <p>Specifies if the channel is preemptable. '0': Not preemptable. '1': Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between 'single transfers' (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated.</p> |
| 31 | ENABLED | RW | RW1C | 0 | <p>Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled.</p> <p>SW sets this field to '1' to enable a specific channel.</p> <p>HW sets this field to '0' on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE).</p> |

9.3.18.2 DW_CH_STRUCT_CH_STATUS

Description: Channel status
Address: 0x40288004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|----|------------------|----|----|----|
| Name | None [7:4] | | | | INTR_CAUSE [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PENDING [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:3 | INTR_CAUSE | R | W | Undefined | <p>Specifies the source of the interrupt cause:</p> <ul style="list-style-type: none"> '0': No interrupt generated '1': Interrupt based on transfer completion configuration based on INTR_TYPE '2': Source transfer bus error '3': Destination transfer bus error '4': Source address misalignment '5': Destination address misalignment '6': Current descriptor pointer is null '7': Active channel is disabled '8': Descriptor bus error '9'-'15': Not used. <p>For error related interrupt causes (INTR_CAUSE is '2', '3', ..., '8'), the channel is disabled (HW sets CH_CTL.ENABLED to '0').</p> |
| 31 | PENDING | R | W | 0 | <p>Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)).</p> |

9.3.18.3 DW_CH_STRUCT_CH_IDX

Description: Channel current indices
Address: 0x40288008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Note that this register is retained during DeepSleep system power mode.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | X_IDX [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | Y_IDX [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:7 | X_IDX | RW | RW | Undefined | Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to '0' when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to '0' when it updates CH_CURR_PTR. |
| 8:15 | Y_IDX | RW | RW | Undefined | Specifies the Y loop index, with X_COUNT taken from the current descriptor. Note: HW sets this field to '0' when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to '0' when it updates CH_CURR_PTR. |

9.3.18.4 DW_CH_STRUCT_CH_CURR_PTR

Description: Channel current descriptor pointer
Address: 0x4028800C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 2:31 | ADDR | RW | RW | Undefined | Address of current descriptor. When this field is '0', there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to '0'. |

9.3.18.5 DW_CH_STRUCT_INTR

Description: Interrupt
Address: 0x40288010
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----------|
| Name | None [7:1] | | | | | | | CH [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|------|-----------------|--|
| 0 | CH | RW1C | RW1S | 0 | Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. |

9.3.18.6 DW_CH_STRUCT_INTR_SET

Description: Interrupt set
Address: 0x40288014
Offset: 0x14
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0 | CH | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). |

9.3.18.7 DW_CH_STRUCT_INTR_MASK

Description: Interrupt mask
Address: 0x40288018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | CH | RW | R | 0 | Mask for corresponding field in INTR register. |

9.3.18.8 DW_CH_STRUCT_INTR_MASKED

Description: Interrupt masked

Address: 0x4028801C

Offset: 0x1C

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------|
| Name | None [7:1] | | | | | | | CH [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | CH | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

9.3.18.9 DW_CH_STRUCT_SRAM_DATA0

Description: SRAM data 0
Address: 0x40288020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: SRAM_DATA0 and SRAM_DATA1 are provided for ECC fault injection functionality. These register should NOT be used to control regular functionality (except that they can be used for initialization of DW SRAMs).

Some of the CH_CTL, CH_STATUS, CH_IDX and CH_CURR_PTR fields are implemented using SRAM storage. Each channel uses two 32-bit SRAM data words. The fields of a register that are implemented using SRAM storage are mapped on a subset of either of the two 32-bit SRAM data words. Specifically, the first 32-bit SRAM data word implements CH_CTL.P, CH_CTL.NS, CH_CTL.B, CH_CTL.PC, CH_CTL.PREEMPTABLE, CH_IDX.X_IDX and CH_IDX.Y_IDX fields and the second 32-bit SRAM data word implements the CH_CURR_PTR.ADDR field. As a result, CH_CTL, CH_IDX and CH_CURR_PTR writes only update a subset of a 32-bit SRAM data word.

For ECC fault injection, it is required to update a complete 32-bit SRAM data word with a user provided ECC parity (specified by ECC_CTL.PARITY) at a specific SRAM location (specified by ECC_CTL.WORD_ADDR). Therefore, SRAM_DATA0 and SRAM_DATA1 provide access to specific SRAM locations. For a channel i , SRAM_DATA0 provides access to SRAM word address $2*i$ and SRAM_DATA1 provides access to SRAM word address $2*i + 1$. E.g., to inject a fault at SRAM word address '13', CTL.ECC_INJ_EN is set to '1', ECC_CTL.WORD_ADDR is set to '13', and ECC_CTL.PARITY is set to the faulting parity. Next, the SW performs a 32-bit write to SRAM_DATA1 of channel 6 ($2*6 + 1 = 13$). The write data and the faulting parity is written to SRAM word address '13'.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|-------------|
| 0:31 | DATA | RW | RW | Undefined | N/A |

9.3.18.10 DW_CH_STRUCT_SRAM_DATA1

Description: SRAM data 1
Address: 0x40288024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|-------------|
| 0:31 | DATA | RW | RW | Undefined | N/A |

9.3.18.11 DW_CH_STRUCT_TR_CMD

Description: Channel software trigger
Address: 0x40288028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------|
| Name | None [7:1] | | | | | | | ACTIVATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|----|-----------------|---|
| 0 | ACTIVATE | RW1S | A | 0 | Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. |

10 EFUSE

Description EFUSE MXS40 registers
Base Address 0x402C0000
Size 0x200
Slave Num MMIO2 - 10

11 EFUSE_DATA

Description eFUSE memory
Base Address 0x402C0800
Size 0x200
Slave Num MMIO2 - 10

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| EFUSE_DATA_CUSTOMER_DATA0 | 0x402C0868 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA1 | 0x402C086C | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA2 | 0x402C0870 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA3 | 0x402C0874 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA4 | 0x402C0878 | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| EFUSE_DATA_CUSTOMER_DATA5 | 0x402C087C | NO-ACCESS | Available EFUSE bits for customer usage.They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |

11.1 Register Details

11.1.1 EFUSE_DATA_CUSTOMER_DATA

| | |
|---------------------|---|
| Description: | Available EFUSE bits for customer usage. They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |
| Address: | 0x402C0868 |
| Offset: | 0x68 |
| Retention: | Retained |
| IsDeepSleep: | No |
| Comment: | The eFUSE memory consists of an array of eFUSE macros. The memory can only be read with AHB-Lite Byte read transfers. A non-Byte AHB-Lite read transfer results in an AHB-Lite bus error. An AHB-Lite write transfer results in an AHB-Lite bus error. Furthermore, an AHB-Lite read transfer while a program operation is in progress (CMD.START is '1') results in an AHB-Lite bus error. |
| | The number of eFUSE memory Bytes is determined by the EFUSE_NR configuration parameter. This parameter specifies the number of instantiated eFUSE macros. Each macro has 16 Bytes. E.g., if EFUSE_NR is 8, the eFUSE memory has 8*16 Bytes = 128 Bytes. |
| Default: | 0x0 |

Bit-field Table

| | | | | | | | | |
|-------------|-------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DATA_BYTE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA_BYTE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA_BYTE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA_BYTE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------------|-------------|-----------|-----------|------------------------|--|
| 0:31 | DATA_BYTE | RW | R | 0 | Available EFUSE bits for customer usage. They can be programmed in NORMAL protection state via CMx/DAP and in SECURE protection state via CMx. |

12 EVTGEN

Description Event generator
Base Address 0x403F0000
Size 0x1000
Slave Num MMIO3 - 4

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| EVTGEN0_CTL | 0x403F0000 | FULL | Control |
| EVTGEN0_COMP0_STATUS | 0x403F0004 | FULL | Comparator structures comparator 0 status |
| EVTGEN0_COMP1_STATUS | 0x403F0008 | FULL | Comparator structures comparator 1 status |
| EVTGEN0_COUNTER_STATUS | 0x403F0010 | FULL | Counter status |
| EVTGEN0_COUNTER | 0x403F0014 | FULL | Counter |
| EVTGEN0_RATIO_CTL | 0x403F0020 | FULL | Ratio control |
| EVTGEN0_RATIO | 0x403F0024 | FULL | Ratio |
| EVTGEN0_REF_CLOCK_CTL | 0x403F0030 | FULL | Reference clock control |
| EVTGEN0_INTR | 0x403F0700 | FULL | Interrupt |
| EVTGEN0_INTR_SET | 0x403F0704 | FULL | Interrupt set |
| EVTGEN0_INTR_MASK | 0x403F0708 | FULL | Interrupt mask |
| EVTGEN0_INTR_MASKED | 0x403F070C | FULL | Interrupt masked |
| EVTGEN0_INTR_DPSLP | 0x403F0710 | FULL | DeepSleep interrupt |
| EVTGEN0_INTR_DPSLP_SET | 0x403F0714 | FULL | DeepSleep interrupt set |
| EVTGEN0_INTR_DPSLP_MASK | 0x403F0718 | FULL | DeepSleep interrupt mask |
| EVTGEN0_INTR_DPSLP_MASKED | 0x403F071C | FULL | DeepSleep interrupt masked |

12.1 COMP_STRUCT 0

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| EVTGEN0_COMP_STRUCT0_COMP_CTL | 0x403F0800 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT0_COMP0 | 0x403F0804 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT0_COMP1 | 0x403F0808 | FULL | Comparator 1 (DeepSleep functionality) |

12.2 COMP_STRUCT 1

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| EVTGEN0_COMP_STRUCT1_COMP_CTL | 0x403F0820 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT1_COMP0 | 0x403F0824 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT1_COMP1 | 0x403F0828 | FULL | Comparator 1 (DeepSleep functionality) |

12.3 COMP_STRUCT 2

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| EVTGEN0_COMP_STRUCT2_COMP_CTL | 0x403F0840 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT2_COMP0 | 0x403F0844 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT2_COMP1 | 0x403F0848 | FULL | Comparator 1 (DeepSleep functionality) |

12.4 COMP_STRUCT 3

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| EVTGEN0_COMP_STRUCT3_COMP_CTL | 0x403F0860 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT3_COMP0 | 0x403F0864 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT3_COMP1 | 0x403F0868 | FULL | Comparator 1 (DeepSleep functionality) |

12.5 COMP_STRUCT 4

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| EVTGEN0_COMP_STRUCT4_COMP_CTL | 0x403F0880 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT4_COMP0 | 0x403F0884 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT4_COMP1 | 0x403F0888 | FULL | Comparator 1 (DeepSleep functionality) |

12.6 COMP_STRUCT 5

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| EVTGEN0_COMP_STRUCT5_COMP_CTL | 0x403F08A0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT5_COMP0 | 0x403F08A4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT5_COMP1 | 0x403F08A8 | FULL | Comparator 1 (DeepSleep functionality) |

12.7 COMP_STRUCT 6

| Register Name | Address | Permission | Description |
|---|------------|------------|--|
| EVTGEN0_COMP_STRUCT6_COMP_CTL | 0x403F08C0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT6_COMP0 | 0x403F08C4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT6_COMP1 | 0x403F08C8 | FULL | Comparator 1 (DeepSleep functionality) |

12.8 COMP_STRUCT 7

| Register Name | Address | Permission | Description |
|---|------------|------------|--|
| EVTGEN0_COMP_STRUCT7_COMP_CTL | 0x403F08E0 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT7_COMP0 | 0x403F08E4 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT7_COMP1 | 0x403F08E8 | FULL | Comparator 1 (DeepSleep functionality) |

12.9 COMP_STRUCT 8

| Register Name | Address | Permission | Description |
|---|------------|------------|--|
| EVTGEN0_COMP_STRUCT8_COMP_CTL | 0x403F0900 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT8_COMP0 | 0x403F0904 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT8_COMP1 | 0x403F0908 | FULL | Comparator 1 (DeepSleep functionality) |

12.10 COMP_STRUCT 9

| Register Name | Address | Permission | Description |
|---|------------|------------|--|
| EVTGEN0_COMP_STRUCT9_COMP_CTL | 0x403F0920 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT9_COMP0 | 0x403F0924 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT9_COMP1 | 0x403F0928 | FULL | Comparator 1 (DeepSleep functionality) |

12.11 COMP_STRUCT 10

| Register Name | Address | Permission | Description |
|--|------------|------------|--|
| EVTGEN0_COMP_STRUCT10_COMP_CTL | 0x403F0940 | FULL | Comparator control |
| EVTGEN0_COMP_STRUCT10_COMP0 | 0x403F0944 | FULL | Comparator 0 (Active functionality) |
| EVTGEN0_COMP_STRUCT10_COMP1 | 0x403F0948 | FULL | Comparator 1 (DeepSleep functionality) |

12.12 Register Details

12.12.1 EVTGEN_CTL

Description: Control
Address: 0x403F0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 31 | ENABLED | RW | R | 0 | IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. |
| | DISABLED | | | 0 | N/A |
| | ENABLED | | | 1 | N/A |

12.12.2 EVTGEN_COMP0_STATUS

Description: Comparator structures comparator 0 status
Address: 0x403F0004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | COMP0_OUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COMP0_OUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:15 | COMP0_OUT | R | W | 0 | Active comparator 'comp0_out[]' outputs. |

12.12.3 EVTGEN_COMP1_STATUS

Description: Comparator structures comparator 1 status
Address: 0x403F0008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | COMP1_OUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COMP1_OUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:15 | COMP1_OUT | R | W | 0 | DeepSleep comparator 'comp1_out_if[]' outputs (synchronized from clk_if to the IP clock). |

12.12.4 EVTGEN_COUNTER_STATUS

Description: Counter status
Address: 0x403F0010
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|----|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 31 | VALID | R | W | 0 | <p>Active counter validity: '0': Invalid. '1': Valid.</p> <p>The COUNTER register field INT32 is only valid when VALID is '1'.</p> <p>The COUNTER_STATUS and COUNTER registers are non-retention registers; i.e. the COUNTER_STATUS and COUNTER registers are reset during DeepSleep power mode. After entering the Active power mode, the Active counter is initialized with the DeepSleep counter. This initialization may take up to 1 clk_Lf cycle.</p> |

12.12.5 EVTGEN_COUNTER

Description: Counter
Address: 0x403F0014
Offset: 0x14
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | INT32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | INT32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | INT32 | R | W | Undefined | Active counter 'counter_int[31:0]' on clk_ref_div. |

12.12.6 EVTGEN_RATIO_CTL

Description: Ratio control
Address: 0x403F0020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----------------------|----|----|
| Name | None [23:19] | | | | | DYNAMIC_MODE [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|-----------------|--------------|----|----|----|----|----|
| Name | VALID [31:31] | DYNAMIC [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| 16:18 | DYNAMIC_MODE | RW | R | 0 | Weighted average calculation (only used when DYNAMIC is '1'): '0': new RATIO value = (RATIO + measurement + 1) / 2. '1': new RATIO value = (3*RATIO + measurement + 2) / 4. '2': new RATIO value = (7*RATIO + measurement + 4) / 8. '3': new RATIO value = (15*RATIO + measurement + 8) / 16. '4': new RATIO value = (31*RATIO + measurement + 16) / 32. '5': new RATIO value = (63*RATIO + measurement + 32) / 64. '6': new RATIO value = (127*RATIO + measurement + 64) / 128. '7': new RATIO value = (255*RATIO + measurement + 128) / 256. Note: 'measurement' (integer component only) is defined as: 256 * 'number of measured clk_ref_div cycles per clk_if cycle'. The RATIO value (integer and fractional component) is defined as: 256*RATIO.INT16 + RATIO.FRAC8 (RATIO.INT16 = RATIO >> 8 and RATIO.FRAC8 = RATIO percent 256). |
| 30 | DYNAMIC | RW | R | 0 | Specifies if RATIO_CTL.VALID and RATIO are under SW or HW control: '0': SW control. '1': HW control. Auto calibration is used to derive the RATIO value. HW measures the number of clk_ref_div cycles per clk_if cycle. This measurement is combined with the current ratio value to calculate a new ratio value. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|------|-----------------|--|
| 31 | VALID | RW | RW1S | 0 | <p>Ratio value valid: '0': Invalid. '1': Valid.</p> <p>The RATIO register fields INT16 and FRAC8 are only valid when VALID is '1'.</p> |

12.12.7 EVTGEN_RATIO

Description: Ratio
Address: 0x403F0024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: This register contains a ratio value expressing the relative frequency of the DeepSleep clock clk_lf wrt. the Active clock clk_ref_div. Specifically, this registers contains the average number of clk_ref_div cycles per clk_lf cycle.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | FRAC8 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT16 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT16 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--------------------------------------|
| 8:15 | FRAC8 | RW | RW | Undefined | Fractional component of ratio value. |
| 16:31 | INT16 | RW | RW | Undefined | Integer component of ratio value. |

12.12.8 EVTGEN_REF_CLOCK_CTL

Description: Reference clock control
Address: 0x403F0030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | INT_DIV [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:7 | INT_DIV | RW | R | 0 | Divider control for clk_ref_div: '0': Divide by 1. ... '255': Divide by '256'. $Fclk_ref_div = Fclk_ref / (INT_DIV + 1)$ |

12.12.9 EVTGEN_INTR

Description: Interrupt
Address: 0x403F0700
Offset: 0x700
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|------|-----------------|---|
| 0:15 | COMP0 | RW1C | RW1S | 0 | This interrupt cause field is activated (HW sets the field to '1') when a comparator 0 event is generated (Active counter 'counter_int[31:0]' becomes greater or equal to COMP0.INT[31:0]). |

12.12.10 EVTGEN_INTR_SET

Description: Interrupt set

Address: 0x403F0704

Offset: 0x704

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).

Default: The interrupt causes are deactivated when the IP is disabled (CTL.ENABLED is '0').
0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|--|
| 0:15 | COMP0 | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

12.12.11 EVTGEN_INTR_MASK

Description: Interrupt mask
Address: 0x403F0708
Offset: 0x708
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:15 | COMP0 | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

12.12.12 EVTGEN_INTR_MASKED

Description: Interrupt masked
Address: 0x403F070C
Offset: 0x70C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP0 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP0 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:15 | COMP0 | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

12.12.13 EVTGEN_INTR_DPSLP

Description: DeepSleep interrupt
Address: 0x403F0710
Offset: 0x710
Retention: Retained
IsDeepSleep: No
Comment: The interrupt causes are deactivated when the IP is disabled (CTL.ENABLED is '0').
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|---|
| 0:15 | COMP1 | RW1C | A | 0 | This interrupt cause field is activated (HW sets the field to '1') when a comparator 1 event is generated (DeepSleep counter 'counter_int_lf[31:0]' becomes greater or equal to COMP1.INT[31:0]). |

12.12.14 EVTGEN_INTR_DPSLP_SET

Description: DeepSleep interrupt set
Address: 0x403F0714
Offset: 0x714
Retention: Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|--|
| 0:15 | COMP1 | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

12.12.15 EVTGEN_INTR_DPSLP_MASK

Description: DeepSleep interrupt mask
Address: 0x403F0718
Offset: 0x718
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:15 | COMP1 | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

12.12.16 EVTGEN_INTR_DPSLP_MASKED

Description: DeepSleep interrupt masked
Address: 0x403F071C
Offset: 0x71C
Retention: Retained
IsDeepSleep: No
Comment: When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | COMP1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | COMP1 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:15 | COMP1 | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

12.12.17 COMP_STRUCT

12.12.17.1 EVTGEN_COMP_STRUCT_COMP_CTL

Description: Comparator control
Address: 0x403F0800
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|----------------|
| Name | None [7:2] | | | | | | COMP1_EN [1:1] | COMP0_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|---------------------|
| Name | None [23:17] | | | | | | | TR_OUT_EDGE [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0 | COMP0_EN | RW | R | 0 | Active comparator (COMP0) enable: '0': Disabled. The comparator output 'comp0_out' is '0'. '1': Enabled. |
| 1 | COMP1_EN | RW | R | 0 | DeepSleep comparator (COMP1) enable: '0': Disabled. The comparator output 'comp1_out_lf' is '0'. '1': Enabled. |
| 16 | TR_OUT_EDGE | RW | R | 0 | Specifies the 'tr_out' output trigger: '0': The trigger is a level sensitive trigger. The Active comparator output ('comp0_out') is reflected on 'tr_out'. '1': The trigger is an edge sensitive trigger. Activation of the Active comparator output (rising edge on 'comp0_out') results in a two cycle '1'/high pulse on 'tr_out'. |
| 31 | ENABLED | RW | R | 0 | Comparator structure enable: '0': Disabled. '1': Enabled. |

12.12.17.2 EVTGEN_COMP_STRUCT_COMP0

Description: Comparator 0 (Active functionality)
Address: 0x403F0804
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT32 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | INT32 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | INT32 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | INT32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | INT32 | RW | R | Undefined | <p>This value is a 32-bit unsigned integer in the range [0, 2³²-1]. The comparator 'comp0_out' output is activated when the Active counter 'counter_int[31:0]' becomes greater or equal to COMP0.</p> <p>Note: SW must ensure that COMP_CTL.COMP_EN[0] is '0' when COMP0 is written.</p> |

12.12.17.3 EVTGEN_COMP_STRUCT_COMP1

Description: Comparator 1 (DeepSleep functionality)
Address: 0x403F0808
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | INT32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | INT32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | INT32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0:31 | INT32 | RW | R | Undefined | <p>This value is a 32-bit unsigned integer in the range [0, 2³²-1]. The comparator 'comp1_out_if' output is activated when the DeepSleep counter 'counter_int_if[31:0]' becomes greater or equal to COMP1.</p> <p>Note: SW must ensure that COMP_CTL.COMP_EN[1] is '0' when COMP1 is written.</p> |

13 FAULT

| | |
|---------------------|------------------|
| Description | Fault structures |
| Base Address | 0x40210000 |
| Size | 0x10000 |
| Slave Num | MMIO2 - 1 |

13.1 STRUCT 0

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|------------------|
| FAULT_STRUCT0_CTL | 0x40210000 | FULL | Fault control |
| FAULT_STRUCT0_STATUS | 0x4021000C | FULL | Fault status |
| FAULT_STRUCT0_DATA0 | 0x40210010 | FULL | Fault data |
| FAULT_STRUCT0_DATA1 | 0x40210014 | FULL | Fault data |
| FAULT_STRUCT0_DATA2 | 0x40210018 | FULL | Fault data |
| FAULT_STRUCT0_DATA3 | 0x4021001C | FULL | Fault data |
| FAULT_STRUCT0_PENDING0 | 0x40210040 | FULL | Fault pending 0 |
| FAULT_STRUCT0_PENDING1 | 0x40210044 | FULL | Fault pending 1 |
| FAULT_STRUCT0_PENDING2 | 0x40210048 | FULL | Fault pending 2 |
| FAULT_STRUCT0_MASK0 | 0x40210050 | FULL | Fault mask 0 |
| FAULT_STRUCT0_MASK1 | 0x40210054 | FULL | Fault mask 1 |
| FAULT_STRUCT0_MASK2 | 0x40210058 | FULL | Fault mask 2 |
| FAULT_STRUCT0_INTR | 0x402100C0 | FULL | Interrupt |
| FAULT_STRUCT0_INTR_SET | 0x402100C4 | FULL | Interrupt set |
| FAULT_STRUCT0_INTR_MASK | 0x402100C8 | FULL | Interrupt mask |
| FAULT_STRUCT0_INTR_MASKED | 0x402100CC | FULL | Interrupt masked |

13.2 STRUCT 1

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|------------------|
| FAULT_STRUCT1_CTL | 0x40210100 | FULL | Fault control |
| FAULT_STRUCT1_STATUS | 0x4021010C | FULL | Fault status |
| FAULT_STRUCT1_DATA0 | 0x40210110 | FULL | Fault data |
| FAULT_STRUCT1_DATA1 | 0x40210114 | FULL | Fault data |
| FAULT_STRUCT1_DATA2 | 0x40210118 | FULL | Fault data |
| FAULT_STRUCT1_DATA3 | 0x4021011C | FULL | Fault data |
| FAULT_STRUCT1_PENDING0 | 0x40210140 | FULL | Fault pending 0 |
| FAULT_STRUCT1_PENDING1 | 0x40210144 | FULL | Fault pending 1 |
| FAULT_STRUCT1_PENDING2 | 0x40210148 | FULL | Fault pending 2 |
| FAULT_STRUCT1_MASK0 | 0x40210150 | FULL | Fault mask 0 |
| FAULT_STRUCT1_MASK1 | 0x40210154 | FULL | Fault mask 1 |
| FAULT_STRUCT1_MASK2 | 0x40210158 | FULL | Fault mask 2 |
| FAULT_STRUCT1_INTR | 0x402101C0 | FULL | Interrupt |
| FAULT_STRUCT1_INTR_SET | 0x402101C4 | FULL | Interrupt set |
| FAULT_STRUCT1_INTR_MASK | 0x402101C8 | FULL | Interrupt mask |
| FAULT_STRUCT1_INTR_MASKED | 0x402101CC | FULL | Interrupt masked |

13.3 STRUCT 2

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|-----------------|
| FAULT_STRUCT2_CTL | 0x40210200 | FULL | Fault control |
| FAULT_STRUCT2_STATUS | 0x4021020C | FULL | Fault status |
| FAULT_STRUCT2_DATA0 | 0x40210210 | FULL | Fault data |
| FAULT_STRUCT2_DATA1 | 0x40210214 | FULL | Fault data |
| FAULT_STRUCT2_DATA2 | 0x40210218 | FULL | Fault data |
| FAULT_STRUCT2_DATA3 | 0x4021021C | FULL | Fault data |
| FAULT_STRUCT2_PENDING0 | 0x40210240 | FULL | Fault pending 0 |
| FAULT_STRUCT2_PENDING1 | 0x40210244 | FULL | Fault pending 1 |
| FAULT_STRUCT2_PENDING2 | 0x40210248 | FULL | Fault pending 2 |
| FAULT_STRUCT2_MASK0 | 0x40210250 | FULL | Fault mask 0 |
| FAULT_STRUCT2_MASK1 | 0x40210254 | FULL | Fault mask 1 |
| FAULT_STRUCT2_MASK2 | 0x40210258 | FULL | Fault mask 2 |
| FAULT_STRUCT2_INTR | 0x402102C0 | FULL | Interrupt |
| FAULT_STRUCT2_INTR_SET | 0x402102C4 | FULL | Interrupt set |

| Register Name | Address | Permission | Description |
|---|------------|------------|------------------|
| FAULT_STRUCT2_INTR_MASK | 0x402102C8 | FULL | Interrupt mask |
| FAULT_STRUCT2_INTR_MASKED | 0x402102CC | FULL | Interrupt masked |

13.4 STRUCT 3

| Register Name | Address | Permission | Description |
|---|------------|------------|------------------|
| FAULT_STRUCT3_CTL | 0x40210300 | FULL | Fault control |
| FAULT_STRUCT3_STATUS | 0x4021030C | FULL | Fault status |
| FAULT_STRUCT3_DATA0 | 0x40210310 | FULL | Fault data |
| FAULT_STRUCT3_DATA1 | 0x40210314 | FULL | Fault data |
| FAULT_STRUCT3_DATA2 | 0x40210318 | FULL | Fault data |
| FAULT_STRUCT3_DATA3 | 0x4021031C | FULL | Fault data |
| FAULT_STRUCT3_PENDING0 | 0x40210340 | FULL | Fault pending 0 |
| FAULT_STRUCT3_PENDING1 | 0x40210344 | FULL | Fault pending 1 |
| FAULT_STRUCT3_PENDING2 | 0x40210348 | FULL | Fault pending 2 |
| FAULT_STRUCT3_MASK0 | 0x40210350 | FULL | Fault mask 0 |
| FAULT_STRUCT3_MASK1 | 0x40210354 | FULL | Fault mask 1 |
| FAULT_STRUCT3_MASK2 | 0x40210358 | FULL | Fault mask 2 |
| FAULT_STRUCT3_INTR | 0x402103C0 | FULL | Interrupt |
| FAULT_STRUCT3_INTR_SET | 0x402103C4 | FULL | Interrupt set |
| FAULT_STRUCT3_INTR_MASK | 0x402103C8 | FULL | Interrupt mask |
| FAULT_STRUCT3_INTR_MASKED | 0x402103CC | FULL | Interrupt masked |

13.5 Register Details

13.5.1 STRUCT

13.5.1.1 FAULT_STRUCT_CTL

Description: Fault control
Address: 0x40210000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register uses DeepSleep reset. Therefore, a DeepSleep reset (possibly as a result of CTL.RESET_EN) resets this register (including setting CTL.RESET_EN to '0').
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--------------------|--------------|-------------|
| Name | None [7:3] | | | | | RESET_REQ_EN [2:2] | OUT_EN [1:1] | TR_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0 | TR_EN | RW | R | 0 | Trigger output enable: '0': Disabled. The trigger output 'tr_fault' is '0'. '1': Enabled. The trigger output 'tr_fault' reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). |
| 1 | OUT_EN | RW | R | 0 | IO output signal enable: '0': Disabled. The IO output signal 'fault_out' is '0'. The IO output enable signal 'fault_out_en' is '0'. '1': Enabled. The IO output signal 'fault_out' reflects STATUS.VALID. The IO output enable signal 'fault_out_en' is '1'. |
| 2 | RESET_REQ_EN | RW | R | 0 | Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal 'fault_reset_req' reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis). The 'fault_reset_req' signals of the individual fault report structures are combined (logically OR'd) into a single SRSS 'fault_reset_req' signal. |

13.5.1.2 FAULT_STRUCT_STATUS

Description: Fault status
Address: 0x4021000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: This register uses cold reset (and is NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|----|----|----|----|----|
| Name | None [7:7] | IDX [6:0] | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:6 | IDX | RW | W | Undefined | The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below. Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. |
| | MPU_0 | | | 0 | Bus master 0 MPU/SMPU. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation. |
| | MPU_1 | | | 1 | Bus master 1 MPU. See MPU_0 description. |
| | MPU_2 | | | 2 | Bus master 2 MPU. See MPU_0 description. |
| | MPU_3 | | | 3 | Bus master 3 MPU. See MPU_0 description. |
| | MPU_4 | | | 4 | Bus master 4 MPU. See MPU_0 description. |
| | MPU_5 | | | 5 | Bus master 5 MPU. See MPU_0 description. |
| | MPU_6 | | | 6 | Bus master 6 MPU. See MPU_0 description. |
| | MPU_7 | | | 7 | Bus master 7 MPU. See MPU_0 description. |
| | MPU_8 | | | 8 | Bus master 8 MPU. See MPU_0 description. |
| | MPU_9 | | | 9 | Bus master 9 MPU. See MPU_0 description. |
| | MPU_10 | | | 10 | Bus master 10 MPU. See MPU_0 description. |
| | MPU_11 | | | 11 | Bus master 11 MPU. See MPU_0 description. |
| | MPU_12 | | | 12 | Bus master 12 MPU. See MPU_0 description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------------|----|----|-----------------|---|
| | MPU_13 | | | 13 | Bus master 13 MPU. See MPU_0 description. |
| | MPU_14 | | | 14 | Bus master 14 MPU. See MPU_0 description. |
| | MPU_15 | | | 15 | Bus master 15 MPU. See MPU_0 description. |
| | CM4_SYS_MPU | | | 16 | CM4 system bus AHB-Lite interface MPU. See MPU_0 description. |
| | CM4_CODE_MPU | | | 17 | CM4 code bus AHB-Lite interface MPU for non flash controller accesses. See MPU_0 description. |
| | CM4_CODE_FLASHC_MPU | | | 18 | CM4 code bus AHB-Lite interface MPU for flash controller accesses. See MPU_0 description. |
| | MS_PPU_4 | | | 25 | Peripheral interconnect, master interface 4 PPU. See MS_PPU_0 description. |
| | PERI_ECC | | | 26 | Peripheral interconnect, protection structures SRAM, correctable ECC error: DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word. |
| | PERI_NC_ECC | | | 27 | Peripheral interconnect, protection structures SRAM, non-correctable ECC error. See PERI_ECC description. |
| | MS_PPU_0 | | | 28 | Peripheral interconnect, master interface 0 PPU. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: '0': master interface, PPU violation, '1': timeout detected, '2': bus error, other: undefined. |
| | MS_PPU_1 | | | 29 | Peripheral interconnect, master interface 1 PPU. See MS_PPU_0 description. |
| | MS_PPU_2 | | | 30 | Peripheral interconnect, master interface 2 PPU. See MS_PPU_0 description. |
| | MS_PPU_3 | | | 31 | Peripheral interconnect, master interface 3 PPU. See MS_PPU_0 description. |
| | GROUP_FAULT_0 | | | 32 | Peripheral group 0 fault detection. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: '0': decoder or peripheral bus error, other: undefined. |
| | GROUP_FAULT_1 | | | 33 | Peripheral group 1 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_2 | | | 34 | Peripheral group 2 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_3 | | | 35 | Peripheral group 3 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_4 | | | 36 | Peripheral group 4 fault detection. See GROUP_FAULT_0 description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------------|----|----|-----------------|---|
| | GROUP_FAULT_5 | | | 37 | Peripheral group 5 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_6 | | | 38 | Peripheral group 6 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_7 | | | 39 | Peripheral group 7 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_8 | | | 40 | Peripheral group 8 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_9 | | | 41 | Peripheral group 9 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_10 | | | 42 | Peripheral group 10 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_11 | | | 43 | Peripheral group 11 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_12 | | | 44 | Peripheral group 12 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_13 | | | 45 | Peripheral group 13 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_14 | | | 46 | Peripheral group 14 fault detection. See GROUP_FAULT_0 description. |
| | GROUP_FAULT_15 | | | 47 | Peripheral group 15 fault detection. See GROUP_FAULT_0 description. |
| | FLASHC_MAIN_BUS_ERROR | | | 48 | Flash controller, main interface, bus error: FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier. |
| | FLASHC_MAIN_C_ECC | | | 49 | Flash controller, main interface, correctable ECC error: DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18). |
| | FLASHC_MAIN_NC_ECC | | | 50 | Flash controller, main interface, non-correctable ECC error. See FLASHC_MAIN_C_ECC description. |
| | FLASHC_WORK_BUS_ERROR | | | 51 | Flash controller, work interface, bus error. FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier. |
| | FLASHC_WORK_C_ECC | | | 52 | Flash controller, work interface, correctable ECC error: DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word. |
| | FLASHC_WORK_NC_ECC | | | 53 | Flash controller, work interface, non-correctable ECC error. See FLASHC_WORK_C_ECC description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|--|
| | FLASHC_CM0_CA_C_ECC | | | 54 | Flash controller, CM0+ cache, correctable ECC error: DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc). |
| | FLASHC_CM0_CA_NC_ECC | | | 55 | Flash controller, CM0+ cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description. |
| | FLASHC_CM4_CA_C_ECC | | | 56 | Flash controller, CM4 cache, correctable ECC error. See FLASHC_CM0_CA_C_ECC description. |
| | FLASHC_CM4_CA_NC_ECC | | | 57 | Flash controller, CM4 cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description. |
| | RAMC0_C_ECC | | | 58 | System SRAM 0 correctable ECC error: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| | RAMC0_NC_ECC | | | 59 | System SRAM 0 non-correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC1_C_ECC | | | 60 | System SRAM 1 correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC1_NC_ECC | | | 61 | System SRAM 1 non-correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC2_C_ECC | | | 62 | System SRAM 2 correctable ECC error. See RAMC0_C_ECC description. |
| | RAMC2_NC_ECC | | | 63 | System SRAM 2 non-correctable ECC error. See RAMC0_C_ECC description. |
| | CRYPTO_C_ECC | | | 64 | Cryptography SRAM correctable ECC error. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM. |
| | CRYPTO_NC_ECC | | | 65 | Cryptography SRAM non-correctable ECC error. See CRYPTO_C_ECC description. |
| | DW0_C_ECC | | | 70 | DataWire 0 SRAM 1 correctable ECC error: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| | DW0_NC_ECC | | | 71 | DataWire 0 SRAM 1 non-correctable ECC error. See DW0_C_ECC description. |
| | DW1_C_ECC | | | 72 | DataWire 1 SRAM 1 correctable ECC error. See DW0_C_ECC description. |
| | DW1_NC_ECC | | | 73 | DataWire 1 SRAM 1 non-correctable ECC error. See DW0_C_ECC description. |
| | FM_SRAM_C_ECC | | | 74 | eCT Flash SRAM (for embedded operations) correctable ECC error: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word. |
| | FM_SRAM_NC_ECC | | | 75 | eCT Flash SRAM non-correctable ECC error: See FM_SRAM_C_ECC description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| | CAN0_C_ECC | | | 80 | CAN controller 0 MRAM correctable ECC error: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM. |
| | CAN0_NC_ECC | | | 81 | CAN controller 0 MRAM non-correctable ECC error: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error). |
| | CAN1_C_ECC | | | 82 | CAN controller 1 MRAM correctable ECC error. See CAN0_C_ECC description. |
| | CAN1_NC_ECC | | | 83 | CAN controller 1 MRAM non-correctable ECC error. See CAN0_NC_ECC description. |
| | CAN2_C_ECC | | | 84 | CAN controller 2 MRAM correctable ECC error. See CAN0_C_ECC description. |
| | CAN2_NC_ECC | | | 85 | CAN controller 2 MRAM non-correctable ECC error. See CAN0_NC_ECC description. |
| | SRSS_CSV | | | 90 | SRSS Clock SuperVisor (CSV) violation detected. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CSV violation occurred on corresponding clk_hf* root clock DATA0[24]: CSV violation occurred on reference clock for clk_hf CSVs DATA0[25]: CSV violation occurred on clk_lf DATA0[26]: CSV violation occurred on clk_ilo0 |
| | SRSS_SSV | | | 91 | SRSS Supply SuperVisor (SSV) violation detected. Multiple SSV can detect a violation at the same time. DATA0[0]: BOD detected on VDDA DATA0[1]: OVD detected on VDDA DATA0[16]: violation detected on LVD/HVD #1 DATA0[17]: violation detected on LVD/HVD #2 |
| | SRSS_MCWDT0 | | | 92 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #0 violation detected. Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT subcounter 0 LOWER_LIMIT DATA0[1]: MCWDT subcounter 0 UPPER_LIMIT DATA0[2]: MCWDT subcounter 1 LOWER_LIMIT DATA0[3]: MCWDT subcounter 1 UPPER_LIMIT |
| | SRSS_MCWDT1 | | | 93 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #1 violation detected. See SRSS_MCWDT0 description. |
| | SRSS_MCWDT2 | | | 94 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #2 violation detected. See SRSS_MCWDT0 description. |
| | SRSS_MCWDT3 | | | 95 | SRSS Multi-Counter Watch Dog Timer (MCWDT) #3 violation detected. See SRSS_MCWDT0 description. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|------|-----------------|---|
| 31 | VALID | RW | RW1S | 0 | <p>Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA3 specify the fault.</p> <p>Note: Typically, HW sets this field to '1' (on an activated HW fault source that is 'enabled' by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA3 when the VALID field is set to '1'.</p> <p>An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA3 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register.</p> <p>Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be 'interrupted' by a HW fault capture. In this case, the SW DATA register updates are overwritten by the HW update (and the STATUS.IDX field will reflect the HW capture)</p> |

13.5.1.3 FAULT_STRUCT_DATA

Description: Fault data
Address: 0x40210010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The DATA registers capture fault information.

These register use cold reset (and are NOT affected by Active or DeepSleep reset). This allows for failure analysis after a warm reset (DeepSleep reset).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | DATA | RW | W | Undefined | Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers. |

13.5.1.4 FAULT_STRUCT_PENDING0

Description: Fault pending 0

Address: 0x40210040

Offset: 0x40

Retention: Not Retained

IsDeepSleep: No

Comment: The PENDING0, PENDING1, PENDING2 registers specify pending (not captured) fault sources. The fault source for which data is captured in DATA0 through DATA3 and which is validated by STATUS.VALID and identified by STATUS.IDX is NOT included in this list of pending fault sources. When a fault source is captured, its corresponding bit field in PENDING0/1/2 is set to '0'.

Note that the pending fault sources are the same for ALL fault structures; i.e. these registers are NOT qualified by the fault structure specific MASK0, MASK1 and MASK2 registers.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | SOURCE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | SOURCE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SOURCE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:31 | SOURCE | R | W | Undefined | This field specifies the following sources: Bit 0: CM0 MPU. Bit 1: CRYPTO MPU. Bit 2: DW 0 MPU. Bit 3: DW 1 MPU. Bit 4: DMA controller MPU. ... Bit 15: DAP MPU. Bit 16: CM4 system bus MPU. Bit 17: CM4 code bus MPU (for non FLASH controller accesses). Bit 18: CM4 code bus MPU (for FLASH controller accesses). |

13.5.1.5 FAULT_STRUCT_PENDING1

Description: Fault pending 1
Address: 0x40210044
Offset: 0x44
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | SOURCE | R | W | Undefined | This field specifies the following sources: Bit 0: Peripheral group 0 PPU. Bit 1: Peripheral group 1 PPU. Bit 2: Peripheral group 2 PPU. Bit 3: Peripheral group 3 PPU. Bit 4: Peripheral group 4 PPU. Bit 5: Peripheral group 5 PPU. Bit 6: Peripheral group 6 PPU. Bit 7: Peripheral group 7 PPU. ... Bit 15: Peripheral group 15 PPU. Bit 16 - 31: See STATUS register. |

13.5.1.6 FAULT_STRUCT_PENDING2

Description: Fault pending 2
Address: 0x40210048
Offset: 0x48
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | SOURCE | R | W | Undefined | This field specifies the following sources: Bit 0 - 31: See STATUS register. |

13.5.1.7 FAULT_STRUCT_MASK0

Description: Fault mask 0

Address: 0x40210050

Offset: 0x50

Retention: Retained

IsDeepSleep: No

Comment: The MASK0, MASK1, MASK2 registers specify 'enables' for fault sources. Only 'enabled' fault sources will be captured by this fault structure (and result in STATUS.VALID and INTR.FAULT being set to '1'). When a fault source is captured, its corresponding bit field in PENDING0/1/2 is set to '0'.

When multiple fault structures are present and the mask fields of the fault structures overlap (the same source is 'enabled' for multiple fault structures), an overlapping enabled pending fault source is captured by a single fault structure that has not captured a fault (the fault structure with the lowest index has precedence).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | SOURCE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | SOURCE [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SOURCE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:31 | SOURCE | RW | R | 0 | Fault source enables: Bits 31-0: Fault sources 31 to 0. |

13.5.1.8 FAULT_STRUCT_MASK1

Description: Fault mask 1
Address: 0x40210054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | SOURCE | RW | R | 0 | Fault source enables: Bits 31-0: Fault sources 63 to 32. |

13.5.1.9 FAULT_STRUCT_MASK2

Description: Fault mask 2
Address: 0x40210058
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | SOURCE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | SOURCE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | SOURCE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | SOURCE | RW | R | 0 | Fault source enables: Bits 31-0: Fault sources 95 to 64. |

13.5.1.10 FAULT_STRUCT_INTR

Description: Interrupt
Address: 0x402100C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|------|-----------------|--|
| 0 | FAULT | RW1C | RW1S | 0 | <p>This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured:</p> <ul style="list-style-type: none"> - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA3 captures the fault source data. <p>SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1').</p> |

13.5.1.11 FAULT_STRUCT_INTR_SET

Description: Interrupt set
Address: 0x402100C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|--|
| 0 | FAULT | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

13.5.1.12 FAULT_STRUCT_INTR_MASK

Description: Interrupt mask
Address: 0x402100C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|--|
| 0 | FAULT | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

13.5.1.13 FAULT_STRUCT_INTR_MASKED

Description: Interrupt masked
Address: 0x402100CC
Offset: 0xCC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | FAULT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0 | FAULT | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

14 FLASHC

Description Flash controller
Base Address 0x40240000
Size 0x10000
Slave Num MMIO2 - 4

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-------------------------------|
| FLASHC_FLASH_CTL | 0x40240000 | FULL | Control |
| FLASHC_FLASH_PWR_CTL | 0x40240004 | FULL | Flash power control |
| FLASHC_FLASH_CMD | 0x40240008 | FULL | Command |
| FLASHC_ECC_CTL | 0x402402A0 | READ | ECC control |
| FLASHC_FM_SRAM_ECC_CTL0 | 0x402402B0 | READ | eCT Flash SRAM ECC control 0 |
| FLASHC_FM_SRAM_ECC_CTL1 | 0x402402B4 | READ | eCT Flash SRAM ECC control 1 |
| FLASHC_FM_SRAM_ECC_CTL2 | 0x402402B8 | READ | eCT Flash SRAM ECC control 2 |
| FLASHC_FM_SRAM_ECC_CTL3 | 0x402402BC | READ | eCT Flash SRAM ECC control 3 |
| FLASHC_CM0_CA_CTL0 | 0x40240400 | FULL | CM0+ cache control |
| FLASHC_CM0_CA_CTL1 | 0x40240404 | FULL | CM0+ cache control |
| FLASHC_CM0_CA_CTL2 | 0x40240408 | FULL | CM0+ cache control |
| FLASHC_CM0_CA_STATUS0 | 0x40240440 | FULL | CM0+ cache status 0 |
| FLASHC_CM0_CA_STATUS1 | 0x40240444 | FULL | CM0+ cache status 1 |
| FLASHC_CM0_CA_STATUS2 | 0x40240448 | FULL | CM0+ cache status 2 |
| FLASHC_CM0_STATUS | 0x40240460 | FULL | CM0+ interface status |
| FLASHC_CM4_CA_CTL0 | 0x40240480 | FULL | CM4 cache control |
| FLASHC_CM4_CA_CTL1 | 0x40240484 | FULL | CM4 cache control |
| FLASHC_CM4_CA_CTL2 | 0x40240488 | FULL | CM4 cache control |
| FLASHC_CM4_CA_STATUS0 | 0x402404C0 | FULL | CM4 cache status 0 |
| FLASHC_CM4_CA_STATUS1 | 0x402404C4 | FULL | CM4 cache status 1 |
| FLASHC_CM4_CA_STATUS2 | 0x402404C8 | FULL | CM4 cache status 2 |
| FLASHC_CM4_STATUS | 0x402404E0 | FULL | CM4 interface status |
| FLASHC_CRYPT0_BUFF_CTL | 0x40240500 | FULL | Cryptography buffer control |
| FLASHC_DW0_BUFF_CTL | 0x40240580 | FULL | Datawire 0 buffer control |
| FLASHC_DW1_BUFF_CTL | 0x40240600 | FULL | Datawire 1 buffer control |
| FLASHC_DMAL_BUFF_CTL | 0x40240680 | FULL | DMA controller buffer control |

14.1 FM_CTL_ECT

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| FLASHC_FM_CTL | 0x4024F000 | NO-ACCESS | Flash Macro Control |
| FLASHC_FM_CODE_MARGIN | 0x4024F004 | NO-ACCESS | Flash Macro Margin Mode on Code Flash |
| FLASHC_FM_ADDR | 0x4024F008 | NO-ACCESS | Flash Macro Address |
| FLASHC_INTR | 0x4024F020 | NO-ACCESS | Interrupt |
| FLASHC_INTR_SET | 0x4024F024 | NO-ACCESS | Interrupt Set |
| FLASHC_INTR_MASK | 0x4024F028 | NO-ACCESS | Interrupt Mask |
| FLASHC_INTR_MASKED | 0x4024F02C | NO-ACCESS | Interrupt Masked |
| FLASHC_ECC_OVERRIDE | 0x4024F030 | NO-ACCESS | ECC Data In override information and control bits |
| FLASHC_FM_DATA | 0x4024F040 | NO-ACCESS | Flash macro data_in[31 to 0] both Code and Work Flash |
| FLASHC_BOOKMARK | 0x4024F064 | NO-ACCESS | Bookmark register - keeps the current FW HV seq |
| FLASHC_MAIN_FLASH_SAFETY | 0x4024F400 | FULL | Main (Code) Flash Security enable |
| FLASHC_STATUS | 0x4024F404 | FULL | Status read from Flash Macro |
| FLASHC_WORK_FLASH_SAFETY | 0x4024F500 | FULL | Work Flash Security enable |

14.2 Register Details

14.2.1 FLASHC_FLASH_CTL

Description: Control
Address: 0x40240000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x110000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---------------|---|---|---|
| Name | None [7:4] | | | | MAIN_WS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|------------------------|------------------------|--------------|----|----------------|----------------|
| Name | None [15:14] | | WORK_BANK_MODE [13:13] | MAIN_BANK_MODE [12:12] | None [11:10] | | WORK_MAP [9:9] | MAIN_MAP [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|-------------------------|-------------------------|---------------------|--------------|-------------------------|-------------------------|---------------------|
| Name | None [23:23] | WORK_ERR_SILENT [22:22] | WORK_ECC_INJ_EN [21:21] | WORK_ECC_EN [20:20] | None [19:19] | MAIN_ERR_SILENT [18:18] | MAIN_ECC_INJ_EN [17:17] | MAIN_ECC_EN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:3 | MAIN_WS | RW | R | 0 | FLASH macro main interface wait states: '0': 0 wait states. ... '15': 15 wait states |
| 8 | MAIN_MAP | RW | R | 0 | Specifies mapping of FLASH macro main array. 0: Mapping A. 1: Mapping B. This field is only used when MAIN_BANK_MODE is '1' (dual bank mode). |
| 9 | WORK_MAP | RW | R | 0 | Specifies mapping of FLASH macro work array. 0: Mapping A. 1: Mapping B. This field is only used when WORK_BANK_MODE is '1' (dual bank mode). |
| 12 | MAIN_BANK_MODE | RW | R | 0 | Specifies bank mode of FLASH macro main array. 0: Single bank mode. 1: Dual bank mode. |
| 13 | WORK_BANK_MODE | RW | R | 0 | Specifies bank mode of FLASH macro work array. 0: Single bank mode. 1: Dual bank mode. |
| 16 | MAIN_ECC_EN | RW | R | 1 | Enable ECC checking for FLASH main interface: 0: Disabled. ECC checking/reporting on FLASH main interface is disabled. No correctable or non-correctable faults are reported. 1: Enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| 17 | MAIN_ECC_INJ_EN | RW | R | 0 | Enable error injection for FLASH main interface. When '1', the parity (ECC_CTL.PARITY[7:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address. |
| 18 | MAIN_ERR_SILENT | RW | R | 0 | <p>Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access):</p> <p>0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is 'silent'</p> <p>In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer.</p> <p>This field is ONLY used by CPU (and debug i.e. SYS_AP/CM0_AP/CM4_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error.</p> <p>Note: All CPU bus masters have dedicated status registers (CM0_STATUS and CM4_STATUS) to register the occurrence of FLASH macro main interface internal errors (non-correctable ECC errors and memory hole errors are NOT registered).</p> <p>Note: fault reporting can be used to identify the error that occurred:</p> <ul style="list-style-type: none"> - FLASH macro main interface internal error. - FLASH macro main interface non-recoverable ECC error. - FLASH macro main interface recoverable ECC error. - FLASH macro main interface memory hole error. |
| 20 | WORK_ECC_EN | RW | R | 1 | <p>Enable ECC checking for FLASH work interface:</p> <p>0: Disabled. ECC checking/reporting on FLASH work interface is disabled. No correctable or non-correctable faults are reported. 1: Enabled.</p> |
| 21 | WORK_ECC_INJ_EN | RW | R | 0 | Enable error injection for FLASH work interface. When '1', the parity (ECC_CTL.PARITY[6:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| 22 | WORK_ERR_SILENT | RW | R | 0 | <p>Specifies bus transfer behavior for a non-recoverable error on the FLASH macro work interface (either a non-correctable ECC error, a FLASH macro work interface internal error, a FLASH macro work interface memory hole access):</p> <p>0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is 'silent'</p> <p>In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer.</p> <p>This field is ONLY used by CPU (and debug i.e. SYS_AP/CM0_AP/CM4_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error.</p> <p>Note: All CPU bus masters have dedicated status registers (CM0_STATUS and CM4_STATUS) to register the occurrence of FLASH macro work interface internal errors (non-correctable ECC errors and memory hole errors are NOT registered).</p> <p>Note: fault reporting can be used to identify the error that occurred:</p> <ul style="list-style-type: none"> - FLASH macro work interface internal error. - FLASH macro work interface non-recoverable ECC error. - FLASH macro work interface recoverable ECC error. - FLASH macro work interface memory hole error. |

14.2.2 FLASHC_FLASH_PWR_CTL

Description: Flash power control

Address: 0x40240004

Offset: 0x4

Retention: Retained

IsDeepSleep: No

Comment: This register controls Flash memory power control input pins 'enable' and 'enable_hv'. Flash memory can be turned OFF through SW in LPACTIVE power mode by making ENABLE=0 and ENABLE_HV=0. The wakeup time of the Flash memory is 10us (Twake1). So, SW has to wait for 10us to read from Flash after turning the Flash memory ON through this register.

Default: 0x3

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-----------------|--------------|
| Name | None [7:2] | | | | | | ENABLE_HV [1:1] | ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--------------------------------------|
| 0 | ENABLE | RW | R | 1 | Enables power to the flash memory |
| 1 | ENABLE_HV | RW | R | 1 | Enables HV power to the flash memory |

14.2.3 FLASHC_FLASH_CMD

Description: Command
Address: 0x40240008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|-----------|
| Name | None [7:2] | | | | | | BUFF_INV [1:1] | INV [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|------|-----------------|--|
| 0 | INV | RW1S | RW1C | 0 | Invalidation of ALL caches (for CM0+ and CM4) and ALL buffers. SW writes a '1' to clear the caches. HW sets this field to '0' when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. The caches' LRU structures are also reset to their default state. |
| 1 | BUFF_INV | RW1S | RW1C | 0 | Invalidation of ALL buffers (does not invalidate the caches). SW writes a '1' to clear the buffers. HW sets this field to '0' when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. Note: the caches only capture FLASH macro main array data. Therefore, invalidating just the buffers (BUFF_INV) does not invalidate captures main array data in the caches. |

14.2.4 FLASHC_ECC_CTL

Description: ECC control
Address: 0x402402A0
Offset: 0x2A0
Retention: Retained
IsDeepSleep: No
Comment: Note that for cache SRAM and FLASH work interface ECC, the word address is for a 32-bit word. For FLASH main interface ECC, the word address is for a 64-bit word.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | WORD_ADDR [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | WORD_ADDR [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | WORD_ADDR [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PARITY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------|----|----|-----------------|--|
| 0:23 | WORD_ADDR | RW | R | 0 | <p>Specifies the word address where an error will be injected.</p> <ul style="list-style-type: none"> - For cache SRAM ECC, the word address WORD_ADDR[23:0] is device address A[25:2]. On a FLASH macro refill to this word address and when the corresponding CM0/4_CA_CTL.RAM_ECC_INJ_EN bit is '1', the parity (PARITY[6:0]) is injected and stored in the cache. - For FLASH main interface ECC, the word address WORD_ADDR[23:0] is device address A[26:3]. On a FLASH main interface read and when FLASH_CTL.MAIN_ECC_INJ_EN bit is '1', the parity (PARITY[7:0]) replaces the FLASH macro parity (FLASH main interface read path is manipulated). - For FLASH work interface ECC, the word address WORD_ADDR[23:0] is device address A[24:2]. On a FLASH work interface read and when FLASH_CTL.WORK_ECC_INJ_EN bit is '1', the parity (PARITY[6:0]) replaces the FLASH macro parity (FLASH work interface read path is manipulated). |
| 24:31 | PARITY | RW | R | 0 | <p>ECC parity to use for ECC error injection at address WORD_ADDR.</p> <ul style="list-style-type: none"> - For cache SRAM ECC, the 7-bit parity PARITY[6:0] is for a 32-bit word. - For FLASH main interface ECC, the 8-bit parity PARITY[7:0] is for a 64-bit word. - For FLASH work interface ECC, the 7-bit parity PARITY[6:0] is for a 32-bit word. |

14.2.5 FLASHC_FM_SRAM_ECC_CTL0

Description: eCT Flash SRAM ECC control 0
Address: 0x402402B0
Offset: 0x2B0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | ECC_INJ_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | ECC_INJ_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | ECC_INJ_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | ECC_INJ_DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:31 | ECC_INJ_DATA | RW | R | 0 | 32-bit data for ECC error injection test of eCT Flash SRAM ECC logic. |

14.2.6 FLASHC_FM_SRAM_ECC_CTL1

Description: eCT Flash SRAM ECC control 1
Address: 0x402402B4
Offset: 0x2B4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------------|
| Name | None [7:7] | | | | | | | ECC_INJ_PARITY [6:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0:6 | ECC_INJ_PARITY | RW | R | 0 | 7-bit parity for ECC error injection test of eCT Flash SRAM ECC logic. |

14.2.7 FLASHC_FM_SRAM_ECC_CTL2

Description: eCT Flash SRAM ECC control 2
Address: 0x402402B8
Offset: 0x2B8
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|---|---|---|---|---|---|---|
| Name | CORRECTED_DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------------|----|----|----|----|----|---|---|
| Name | CORRECTED_DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------------|----|----|----|----|----|----|----|
| Name | CORRECTED_DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------------|----|----|----|----|----|----|----|
| Name | CORRECTED_DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:31 | CORRECTED_DATA | R | W | 0 | 32-bit corrected data output of the ECC syndrome logic. |

14.2.8 FLASHC_FM_SRAM_ECC_CTL3

Description: eCT Flash SRAM ECC control 3
Address: 0x402402BC
Offset: 0x2BC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|------------|---|---|------------------|
| Name | None [7:5] | | | ECC_INJ_EN [4:4] | None [3:1] | | | ECC_ENABLE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---------------------|
| Name | None [15:9] | | | | | | | ECC_TEST_FAIL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|------|-----------------|---|
| 0 | ECC_ENABLE | RW | R | 1 | ECC generation/check enable for eCT Flash SRAM memory. |
| 4 | ECC_INJ_EN | RW | RW1C | 0 | eCT Flash SRAM ECC error injection test enable. Follow the steps below for ECC logic test: 1. Write corrupted or uncorrupted 39-bit data to FM_SRAM_ECC_CTL0/1 registers. 2. Set the ECC_INJ_EN bit to '1'. 3. Confirm that the bit ECC_TEST_FAIL is '0'. If this is not the case, start over at item 1 because the eCT Flash was not idle. 4. Check the corrected data in FM_SRAM_ECC_CTL2. 5. Confirm that fault was reported to fault structure, and check syndrome (only applicable if corrupted data was written in step 1). 6. If not finished, start over at 1 with different data. |
| 8 | ECC_TEST_FAIL | R | W | 0 | Status of ECC test. 1 : ECC test failed because eCT Flash macro is busy and using the SRAM. 0: ECC was performed. |

14.2.9 FLASHC_CM0_CA_CTL0

Description: CM0+ cache control
Address: 0x40240400
Offset: 0x400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0000001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------------|------------------|
| Name | None [7:2] | | | | | | RAM_ECC_INJ_EN [1:1] | RAM_ECC_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------|----|
| Name | None [23:18] | | | | | | WAY [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|-----------------|--------------|----|----|------------------|----|----|
| Name | CA_EN [31:31] | PREF_EN [30:30] | None [29:27] | | | SET_ADDR [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------|----|----|-----------------|--|
| 0 | RAM_ECC_EN | RW | R | 1 | Enable ECC checking for cache accesses: 0: Disabled. 1: Enabled. |
| 1 | RAM_ECC_INJ_EN | RW | R | 0 | Enable error injection for cache. When '1', the parity (ECC_CTL.PARITY[6:0]) is used when a refill is done from the FLASH macro to the ECC_CTL.WORD_ADDR[23:0] word address. |
| 16:17 | WAY | RW | R | 0 | Specifies the cache way for which cache information is provided in CM0_CA_STATUS0/1/2. |
| 24:26 | SET_ADDR | RW | R | 0 | Specifies the cache set for which cache information is provided in CM0_CA_STATUS0/1/2. |
| 30 | PREF_EN | RW | R | 1 | Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. |
| 31 | CA_EN | RW | R | 1 | Cache enable: 0: Disabled. The cache tag valid bits are reset to '0's and the cache LRU information is set to '1's (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. |

14.2.10 FLASHC_CM0_CA_CTL1

Description: CM0+ cache control

Address: 0x40240404

Offset: 0x404

Retention: Retained

IsDeepSleep: No

Comment: This register controls the CM0 Cache SRAM power states. CM0 Cache SRAM consists of a single power partition.

Default: 0xFA050003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 0:1 | PWR_MODE | RW | R | 3 | Specifies power mode for CM0 cache. The following sequence should be followed for turning OFF/ON the cache SRAM. Turn OFF sequence: a) Write CM0_CA_CTL0 to disable cache. b) Write CM0_CA_CTL1 to turn OFF cache SRAM. Turn ON sequence: a) Write CM0_CA_CTL1 to turn ON cache SRAM. b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM0_CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles. c) Write CM0_CA_CTL0 to enable cache. |
| | OFF | | | 0 | Power OFF the CM0 cache, no retain |
| | RESERVED | | | 1 | Undefined |
| | RETAINED | | | 2 | Put the CM0 cache in retained mode |
| | ENABLED | | | 3 | Enable/Turn ON the CM0 cache SRAM. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says "R", SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. |

14.2.11 FLASHC_CM0_CA_CTL2

Description: CM0+ cache control
Address: 0x40240408
Offset: 0x408
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x12C

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | PWRUP_DELAY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|-------------------|---|
| Name | None [15:10] | | | | | | PWRUP_DELAY [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:9 | PWRUP_DELAY | RW | R | 300 | Number clock cycles delay needed after power domain power up |

14.2.12 FLASHC_CM0_CA_STATUS0

Description: CM0+ cache status 0
Address: 0x40240440
Offset: 0x440
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | VALID32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | VALID32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | VALID32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | VALID32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:31 | VALID32 | R | W | 0 | Sixteen valid bits of the cache line specified by CM0_CA_CTL.WAY and CM0_CA_CTL.SET_ADDR. |

14.2.13 FLASHC_CM0_CA_STATUS1

Description: CM0+ cache status 1
Address: 0x40240444
Offset: 0x444
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | TAG [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | TAG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TAG [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TAG [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | TAG | R | W | Undefined | Cache line address of the cache line specified by CM0_CA_CTL.WAY and CM0_CA_CTL.SET_ADDR. |

14.2.14 FLASHC_CM0_CA_STATUS2

Description: CM0+ cache status 2
Address: 0x40240448
Offset: 0x448
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|-----------|---|---|---|---|---|
| Name | None [7:6] | | LRU [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:5 | LRU | R | W | Undefined | Six bit LRU representation of the cache set specified by CM0_CA_CTL.SET_ADDR. The encoding of the field is as follows ('X_LRU_Y' indicates that way X is Less Recently Used than way Y): Bit 5: 0_LRU_1: way 0 less recently used than way 1. Bit 4: 0_LRU_2. Bit 3: 0_LRU_3. Bit 2: 1_LRU_2. Bit 1: 1_LRU_3. Bit 0: 2_LRU_3. |

14.2.15 FLASHC_CM0_STATUS

Description: CM0+ interface status
Address: 0x40240460
Offset: 0x460
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------------------------|--------------------------------|
| Name | None [7:2] | | | | | | WORK_INTE RNAL_ERR [1:1] | MAIN_INTE RNAL_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|-----|-----------------|--|
| 0 | MAIN_INTERNAL_ERR | RW1C | W1S | 0 | <p>Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM0+ access (or debug access via SYS_AP/CM0_AP).</p> <p>SW clears this field to '0'. HW sets this field to '1' on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error.</p> <p>Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT.</p> |
| 1 | WORK_INTERNAL_ERR | RW1C | W1S | 0 | See CM0_STATUS.MAIN_INTERNAL_ERROR. |

14.2.16 FLASHC_CM4_CA_CTL0

Description: CM4 cache control
Address: 0x40240480
Offset: 0x480
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xC0000001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------------|------------------|
| Name | None [7:2] | | | | | | RAM_ECC_INJ_EN [1:1] | RAM_ECC_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------|----|
| Name | None [23:18] | | | | | | WAY [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|-----------------|--------------|----|----|------------------|----|----|
| Name | CA_EN [31:31] | PREF_EN [30:30] | None [29:27] | | | SET_ADDR [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------|----|----|-----------------|--|
| 0 | RAM_ECC_EN | RW | R | 1 | See CM0_CA_CTL. |
| 1 | RAM_ECC_INJ_EN | RW | R | 0 | See CM0_CA_CTL. |
| 16:17 | WAY | RW | R | 0 | Specifies the cache way for which cache information is provided in CM4_CA_STATUS0/1/2. |
| 24:26 | SET_ADDR | RW | R | 0 | Specifies the cache set for which cache information is provided in CM4_CA_STATUS0/1/2. |
| 30 | PREF_EN | RW | R | 1 | Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. |
| 31 | CA_EN | RW | R | 1 | Cache enable: 0: Disabled. The cache tag valid bits are reset to '0's and the cache LRU information is set to '1's (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. |

14.2.17 FLASHC_CM4_CA_CTL1

Description: CM4 cache control

Address: 0x40240484

Offset: 0x484

Retention: Retained

IsDeepSleep: No

Comment: This register controls the CM4 Cache SRAM power states. CM4 Cache SRAM consists of a single power partition.

Default: 0xFA050003

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|---|
| Name | None [7:2] | | | | | | PWR_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | VECTKEYSTAT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 0:1 | PWR_MODE | RW | R | 3 | Specifies power mode for CM4 cache. The following sequence should be followed for turning OFF/ON the cache SRAM. Turn OFF sequence: a) Write CM4_CA_CTL0 to disable cache. b) Write CM4_CA_CTL1 to turn OFF cache SRAM. Turn ON sequence: a) Write CM4_CA_CTL1 to turn ON cache SRAM. b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM4_CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles. c) Write CM4_CA_CTL0 to enable cache. |
| | OFF | | | 0 | Power OFF the CM4 cache, not retained. |
| | RESERVED | | | 1 | Undefined |
| | RETAINED | | | 2 | Put the CM4 cache in retained mode. |
| | ENABLED | | | 3 | Enable/Turn ON the CM4 cache. |
| 16:31 | VECTKEYSTAT | R | | 64005 | Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says "R", SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. |

14.2.18 FLASHC_CM4_CA_CTL2

Description: CM4 cache control
Address: 0x40240488
Offset: 0x488
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x12C

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | PWRUP_DELAY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|-------------------|---|
| Name | None [15:10] | | | | | | PWRUP_DELAY [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:9 | PWRUP_DELAY | RW | R | 300 | Number clock cycles delay needed after power domain power up |

14.2.19 FLASHC_CM4_CA_STATUS0

Description: CM4 cache status 0
Address: 0x402404C0
Offset: 0x4C0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | VALID32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | VALID32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | VALID32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | VALID32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---------------------|
| 0:31 | VALID32 | R | W | 0 | See CM0_CA_STATUS0. |

14.2.20 FLASHC_CM4_CA_STATUS1

Description: CM4 cache status 1
Address: 0x402404C4
Offset: 0x4C4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | TAG [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------|----|----|----|----|----|---|---|
| Name | TAG [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TAG [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------|----|----|----|----|----|----|----|
| Name | TAG [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------|
| 0:31 | TAG | R | W | Undefined | See CM0_CA_STATUS1. |

14.2.21 FLASHC_CM4_CA_STATUS2

Description: CM4 cache status 2
Address: 0x402404C8
Offset: 0x4C8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|-----------|---|---|---|---|---|
| Name | None [7:6] | | LRU [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---------------------|
| 0:5 | LRU | R | W | Undefined | See CM0_CA_STATUS2. |

14.2.22 FLASHC_CM4_STATUS

Description: CM4 interface status
Address: 0x402404E0
Offset: 0x4E0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------------------------|--------------------------------|
| Name | None [7:2] | | | | | | WORK_INTE RNAL_ERR [1:1] | MAIN_INTE RNAL_ERR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|-----|-----------------|---|
| 0 | MAIN_INTERNAL_ERR | RW1C | W1S | 0 | <p>Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM4 access (or debug access via SYS_AP/CM4_AP).</p> <p>SW clears this field to '0'. HW sets this field to '1' on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error.</p> <p>Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT.</p> |
| 1 | WORK_INTERNAL_ERR | RW1C | W1S | 0 | See CM4_STATUS.MAIN_INTERNAL_ERROR. |

14.2.23 FLASHC_CRYPTC_BUFF_CTL

Description: Cryptography buffer control
Address: 0x40240500
Offset: 0x500
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|-----------------|--------------|----|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 30 | PREF_EN | RW | R | 1 | Prefetch enable: 0: Disabled. 1: Enabled. A prefetch will be done when there is read 'hit' on the last 32-bit word of the buffer. For eCT work Flash, prefetch will not be done. |

14.2.24 FLASHC_DW0_BUFF_CTL

Description: Datawire 0 buffer control
Address: 0x40240580
Offset: 0x580
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|-----------------|--------------|----|----|----|----|----|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|----------------------|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

14.2.25 FLASHC_DW1_BUFF_CTL

Description: Datawire 1 buffer control
Address: 0x40240600
Offset: 0x600
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|-----------------|--------------|----|----|----|----|----|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|----------------------|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

14.2.26 FLASHC_DMAC_BUFF_CTL

Description: DMA controller buffer control
Address: 0x40240680
Offset: 0x680
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x40000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|-----------------|--------------|----|----|----|----|----|
| Name | None [31:31] | PREF_EN [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|----------------------|
| 30 | PREF_EN | RW | R | 1 | See CRYPTO_BUFF_CTL. |

14.2.27 FM_CTL_ECT

14.2.27.1 FLASHC_FM_CTL

Description: Flash Macro Control
Address: 0x4024F000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are related to C interface functionality
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|--------------|----|---------------|----|----|----|----|
| Name | None [7:5] | | | FM_MODE [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | EMB_START [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:4 | FM_MODE | RW | R | 0 | Flash macro mode selection: d0: Read/Idle - Normal mode, read array enabled d1: Not Used - the 1st analog POR is done by enable/enable_hv d2 - POR FUR Download - Downloads critical Flash initialization data from OTP (BG, rd, redu, etc....) d3 - POR IRAM MMR Download - Downloads from OTP region the MMR / IRAM into to the 8051 RDL shadows d4 - POR SW Download - Downloads from OTP region the SW code into to the 8051 MCU SRAM d5 - POR Code_Work Prepare - Loads the Code and Work Flash MG's to be ready for user mode operation d6 - Not Used d7 - Program 32b (WORK) - Used as program confirm command for 32 (Work) bits program d8 - Program 64b (CODE) - Used as program confirm command for 64 (Code) bits program d9 - Program 256b (CODE) - Used as program confirm command for 256 (Code) bits program d10: Program Page (CODE) - Used as program confirm command for page program for Code flash d11: Not Used d12 - Sector Erase - Erase for all kinds of sectors (Code/Work/SMS) d13 - Blank check Entry (UBC) d14 - Blank Check Read 32bit (WORK) - Blank check mode d15 - Blank check Exit d16 - Not Used d17 - Erase Suspend - Suspend command to the Erase operation d18 - Erase Resume - Resume command to Erase suspended operation d19 - Not Used d20- Not Used d21- Not Used d22- Not Used d23- Not Used d24- Not Used d25- Not Used d26- Not Used d27- Not Used d28- Not Used d29- Not Used d30: Not Used d31: Not Used |
| 31 | EMB_START | RW | R | 0 | '0': not active '1': starts the actual embedded operation |

14.2.27.2 FLASHC_FM_CODE_MARGIN

Description: Flash Macro Margin Mode on Code Flash

Address: 0x4024F004

Offset: 0x4

Retention: Not Retained

IsDeepSleep: No

Comment: This register shall be used when Margin read is applied to the s40ect Flash IP. One should set the DCS trim that serves as the reference current to the area between 4-8uA (around the 6uA normal static ref current) and set the enable. After that one should wait ~10uSec before starting to read any data in the Code Flash. Once Finished the MARGIN_MODE_EN should be reset. Again, user should wait ~10uSec before continue to work with the Flash normally.

Default: 0x3943

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|---|---|---|---|---|---|---|
| Name | MARGIN_DCS_TRIM [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------------|----|----|----|----|----|--------------------------|-----------------------|
| Name | MARGIN_RDREG_TRIM [15:10] | | | | | | MARGIN_DCS_TRIM_EN [9:9] | MARGIN_DCS_TRIM [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------------|-----------------------------------|--------------------------|--------------|----|----|----|----|
| Name | MARGIN_MODE_EN [31:31] | MARGIN_MODE_RDREG_CHNG_EN [30:30] | MARGIN_PGM_ERS_B [29:29] | None [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------------------|----|----|-----------------|--|
| 0:8 | MARGIN_DCS_TRIM | RW | R | 323 | see above table to set the DCS reference current value to be used during Margin mode. (default set to 5uS = 0x143) which gives a Margin to the Erase side. 7uA would probably be used for Margin to the PGM side |
| 9 | MARGIN_DCS_TRIM_EN | RW | R | 0 | 0: internal device defaults used from Margin reads reference current 1: MARGIN_DCS_TRIM configuration is used during Margin read |
| 10:15 | MARGIN_RDREG_TRIM | RW | R | 14 | rdreg_c trim to be used in Margin mode if enabled by MARGIN_MODE_RDREG_CHNG_EN |
| 29 | MARGIN_PGM_ERS_B | RW | R | 0 | 0: ERS Margin is checked 1: PGM Margin is checked |
| 30 | MARGIN_MODE_RDREG_CHNG_EN | RW | R | 0 | when set will also use the MARGIN_RDREG_TRIM from above. Default is not to use |
| 31 | MARGIN_MODE_EN | RW | R | 0 | when set puts the s40ect Flash IP In Margin mode |

14.2.27.3 FLASHC_FM_ADDR

Description: Flash Macro Address

Address: 0x4024F008

Offset: 0x8

Retention: Not Retained

IsDeepSleep: No

Comment: This register specifies the flash memory address till the byte resolution. This register defines the address space for both Code and Work Flash and it works according to the address scheme tables defined below (also used as the address definition for R-bus (code_r_addr and work_r_addr))

This FM_ADDR should be used whenever a user mode embedded operation is done on the Flash i.e. PGM/ERS

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | FM_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | FM_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | FM_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | FM_ADDR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:31 | FM_ADDR | W | R | 0 | Code or Work Flash Address to be used during write operations (PGM/ERS) |

14.2.27.4 FLASHC_INTR

Description: Interrupt
Address: 0x4024F020
Offset: 0x20
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------|
| Name | None [7:1] | | | | | | | INTR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|------|-----------------|---|
| 0 | INTR | RW1C | RW1S | 0 | Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. |

14.2.27.5 FLASHC_INTR_SET

Description: Interrupt Set
Address: 0x4024F024
Offset: 0x24
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------------|
| Name | None [7:1] | | | | | | | INTR_SET [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|----|-----------------|---|
| 0 | INTR_SET | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

14.2.27.6 FLASHC_INTR_MASK

Description: Interrupt Mask
Address: 0x4024F028
Offset: 0x28
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-----------------|
| Name | None [7:1] | | | | | | | INTR_MASK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0 | INTR_MASK | RW | R | 0 | Mask for corresponding field in the INTR register |

14.2.27.7 FLASHC_INTR_MASKED

Description: Interrupt Masked
Address: 0x4024F02C
Offset: 0x2C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------------|
| Name | None [7:1] | | | | | | | INTR_MASKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0 | INTR_MASKED | R | W | 0 | Logical and of corresponding request and mask fields. |

14.2.27.8 FLASHC_ECC_OVERRIDE

Description: ECC Data In override information and control bits
Address: 0x4024F030
Offset: 0x30
Retention: Not Retained
IsDeepSleep: No
Comment: The replacement can be either to the Code syndrome or the work flash syndrome. It knows to replace only 8 bits (per 64) in code flash OR 7 bits (per 32) in work flash, therefore this option is valid only for pgm64 command (Code) or pgm32 command (Work)
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------------|---------------------------|--------------|----|----|----|----|----|
| Name | ECC_OVERRIDE_SYNDROME [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ECC_OVERRIDE_CODE [31:31] | ECC_OVERRIDE_WORK [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------------|----|----|-----------------|---|
| 0:7 | ECC_OVERRIDE_SYNDROME | W | R | 0 | The override syndrome itself to be used in case one of the enables are set. It will take [7:0] in the case of Code flash and [6:0] in the case of work flash, to bypass the internal generated syndrome |
| 30 | ECC_OVERRIDE_WORK | W | R | 0 | 0: no override. Using internal ECC engine to calculate the ECC of the Work Flash |
| 31 | ECC_OVERRIDE_CODE | W | R | 0 | 0: no override. Using internal ECC engine to calculate the ECC of the Code Flash |

14.2.27.9 FLASHC_FM_DATA

Description: Flash macro data_in[31 to 0] both Code and Work Flash
Address: 0x4024F040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment: These registers support aligned 32-bit accesses. The usage of this register should follow the PGM sequence defined (and implemented by API). It has restrictions on the FM_ADDR and # of writes that can be done per pgm command (64,256,page for Code or 32 to work flash) and therefore the sequence must be correct. These register are related to C interface functionality.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | FM_DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | FM_DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | FM_DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | FM_DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:31 | FM_DATA | W | RW | 0 | Pgm command data in going to the internal write buffer (WBUF). |

14.2.27.10 FLASHC_BOOKMARK

Description: Bookmark register - keeps the current FW HV seq
Address: 0x4024F064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | BOOKMARK [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | BOOKMARK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | BOOKMARK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | BOOKMARK [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:31 | BOOKMARK | RW | R | 0 | Used by FW. Keeps the Current HV cycle sequence |

14.2.27.11 FLASHC_MAIN_FLASH_SAFETY

Description: Main (Code) Flash Security enable
Address: 0x4024F400
Offset: 0x400
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------------------------------|
| Name | None [7:1] | | | | | | | MAINFLASH WRITEENABL E [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------------|----|----|-----------------|--|
| 0 | MAINFLASH WRITEENABLE | RW | R | 0 | '0': Main Flash embedded operations are blocked '1': Main Flash embedded operations are enabled |

14.2.27.12 FLASHC_STATUS

Description: Status read from Flash Macro
Address: 0x4024F404
Offset: 0x404
Retention: Not Retained
IsDeepSleep: No
Comment: Read out by the CPUSS to understand the Flash Macro status
Default: 0x80000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------------------|------------------------|-------------------|------------------|------------------|----------------|----------------|
| Name | None [7:7] | BLANK_CHCEK_PASS [6:6] | BLANK_CHECK_WORK [5:5] | ERS_SUSPEND [4:4] | ERASE_WORK [3:3] | ERASE_CODE [2:2] | PGM_WORK [1:1] | PGM_CODE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------|--------------------|--------------------------|------------------------------|--------------|----|----|
| Name | BUSY [31:31] | HANG [30:30] | NATIVE_POR [29:29] | POR_2B_ECC_ERROR [28:28] | POR_1B_ECC_CORRECTED [27:27] | None [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0 | PGM_CODE | R | W | 0 | Indicates if active PGM operation to the Code flash is taking place 0: not running 1: running |
| 1 | PGM_WORK | R | W | 0 | Indicates if active PGM operation to the Work flash is taking place 0: not running 1: running |
| 2 | ERASE_CODE | R | W | 0 | Indicates if active Erase operation to the Code flash is taking place 0: not running 1: running |
| 3 | ERASE_WORK | R | W | 0 | Indicates if active Erase operation to the Work flash is taking place 0: not running 1: running |
| 4 | ERS_SUSPEND | R | W | 0 | Indicates if Erase operation (Code/Work) is currently being suspended 0: not suspended 1: suspended |
| 5 | BLANK_CHECK_WORK | R | W | 0 | Indicates if Blank Check mode is currently running on the work flash 0: not running 1: running |
| 6 | BLANK_CHCEK_PASS | R | W | 0 | Indicates the Blank check command result is PASS (Blank) 0: Not Blank 1: Blank (PASS) |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|--|
| 27 | POR_1B_ECC_CORRECTED | R | W | 0 | Indicates internal ECC found 1b error while downloading info in POR from NVM to VM and fixed it. Valid after 2nd, 3rd and 4th POR phases (FUR, IREM & MMR, SW DOWNLOAD). If Set it is not cleaned till additional POR (rst_hf_ac_t) 0: No error 1: 1b ECC Error corrected in POR |
| 28 | POR_2B_ECC_ERROR | R | W | 0 | Indicates an internal ECC error of 2b while downloading info in POR from NVM to VM. Valid after 2nd, 3rd and 4th POR phases (FUR, IREM & MMR, SW DOWNLOAD). If Set it is not cleaned till additional POR (rst_hf_ac_t) 0: No error 1: ECC 2b Error in POR |
| 29 | NATIVE_POR | R | W | 0 | Indicates a Native Flash state (UV) or sorted one. Valid only after 2nd phase of POR (FUR DOWNLOAD). Comment: not a retained flop, therefore reset (rst_hf_act_n) puts it back to 0. If Set it is not cleaned till additional POR (rst_hf_ac_t) 0: SORTED DEVICE (Non - Native) 1: NATIVE |
| 30 | HANG | R | W | 0 | After embedded operation (pgm/erase) this flag will tell if it was successful or failed 0: PASS 1: FAIL |
| 31 | BUSY | R | W | 1 | Whenever the device is in embedded mode the RDY goes low. Should be the same as c_interrupt pin of the IP (but inverted) 1: busy in embedded 0: rdy (high also in erase suspend) |

14.2.27.13 FLASHC_WORK_FLASH_SAFETY

Description: Work Flash Security enable
Address: 0x4024F500
Offset: 0x500
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------------------------------|
| Name | None [7:1] | | | | | | | WORKFLASH WRITEENABL E [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------------|----|----|-----------------|--|
| 0 | WORKFLASH WRITEENABLE | RW | R | 0 | 0: Work Flash embedded operations are blocked 1: Work Flash embedded operations are enabled |

15 GPIO

| | |
|---------------------|---------------------------------|
| Description | GPIO port control/configuration |
| Base Address | 0x40310000 |
| Size | 0x10000 |
| Slave Num | MMIO3 - 1 |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|--|
| GPIO_INTR_CAUSE0 | 0x40314000 | FULL | Interrupt port cause register 0 |
| GPIO_VDD_ACTIVE | 0x40314010 | FULL | Extern power supply detection register |
| GPIO_VDD_INTR | 0x40314014 | FULL | Supply detection interrupt register |
| GPIO_VDD_INTR_MASK | 0x40314018 | FULL | Supply detection interrupt mask register |
| GPIO_VDD_INTR_MASKED | 0x4031401C | FULL | Supply detection interrupt masked register |
| GPIO_VDD_INTR_SET | 0x40314020 | FULL | Supply detection interrupt set register |

15.1 PRT 0

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT0_OUT | 0x40310000 | FULL | Port output data register Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT0_OUT_CLR | 0x40310004 | FULL | Port output data clear register |
| GPIO_PRT0_OUT_SET | 0x40310008 | FULL | Port output data set register |
| GPIO_PRT0_OUT_INV | 0x4031000C | FULL | Port output data invert register |
| GPIO_PRT0_IN | 0x40310010 | FULL | Port input state register Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT0_INTR | 0x40310014 | FULL | Port interrupt status register Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT0_INTR_MASK | 0x40310018 | FULL | Port interrupt mask register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT0_INTR_MASKED | 0x4031001C | FULL | Port interrupt masked status register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT0_INTR_SET | 0x40310020 | FULL | Port interrupt set register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT0_INTR_CFG | 0x40310040 | FULL | Port interrupt configuration register Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT0_CFG | 0x40310044 | FULL | Port configuration register Note:DRIVE_MODE4 IN_EN4 DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT0_CFG_IN | 0x40310048 | FULL | Port input buffer configuration register Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT0_CFG_OUT | 0x4031004C | FULL | Port output buffer configuration register Note:SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT0_CFG_IN_AUTOLVL | 0x40310058 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.2 PRT 1

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|---|
| GPIO_PRT1_OUT | 0x40310080 | FULL | Port output data register Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT1_OUT_CLR | 0x40310084 | FULL | Port output data clear register |
| GPIO_PRT1_OUT_SET | 0x40310088 | FULL | Port output data set register |
| GPIO_PRT1_OUT_INV | 0x4031008C | FULL | Port output data invert register |
| GPIO_PRT1_IN | 0x40310090 | FULL | Port input state register Note:IN4 IN5 IN6 IN7 are not available for this register |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT1_INTR | 0x40310094 | FULL | Port interrupt status register Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT1_INTR_MASK | 0x40310098 | FULL | Port interrupt mask register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT1_INTR_MASKED | 0x4031009C | FULL | Port interrupt masked status register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT1_INTR_SET | 0x403100A0 | FULL | Port interrupt set register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT1_INTR_CFG | 0x403100C0 | FULL | Port interrupt configuration register Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT1_CFG | 0x403100C4 | FULL | Port configuration register Note:DRIVE_MODE4 IN_EN4 DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT1_CFG_IN | 0x403100C8 | FULL | Port input buffer configuration register Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT1_CFG_OUT | 0x403100CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT1_CFG_IN_AUTOLVL | 0x403100D8 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.3 PRT 2

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT2_OUT | 0x40310100 | FULL | Port output data register Note:OUT6 OUT7 are not available for this register |
| GPIO_PRT2_OUT_CLR | 0x40310104 | FULL | Port output data clear register |
| GPIO_PRT2_OUT_SET | 0x40310108 | FULL | Port output data set register |
| GPIO_PRT2_OUT_INV | 0x4031010C | FULL | Port output data invert register |
| GPIO_PRT2_IN | 0x40310110 | FULL | Port input state register Note:IN6 IN7 are not available for this register |
| GPIO_PRT2_INTR | 0x40310114 | FULL | Port interrupt status register Note:EDGE6 EDGE7 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT2_INTR_MASK | 0x40310118 | FULL | Port interrupt mask register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT2_INTR_MASKED | 0x4031011C | FULL | Port interrupt masked status register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT2_INTR_SET | 0x40310120 | FULL | Port interrupt set register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT2_INTR_CFG | 0x40310140 | FULL | Port interrupt configuration register Note:EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT2_CFG | 0x40310144 | FULL | Port configuration register Note:DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT2_CFG_IN | 0x40310148 | FULL | Port input buffer configuration register Note:VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT2_CFG_OUT | 0x4031014C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT2_CFG_IN_AUTOLVL | 0x40310158 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.4 PRT 3

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT3_OUT | 0x40310180 | FULL | Port output data register Note:OUT6 OUT7 are not available for this register |
| GPIO_PRT3_OUT_CLR | 0x40310184 | FULL | Port output data clear register |
| GPIO_PRT3_OUT_SET | 0x40310188 | FULL | Port output data set register |
| GPIO_PRT3_OUT_INV | 0x4031018C | FULL | Port output data invert register |
| GPIO_PRT3_IN | 0x40310190 | FULL | Port input state register Note:IN6 IN7 are not available for this register |
| GPIO_PRT3_INTR | 0x40310194 | FULL | Port interrupt status register Note:EDGE6 EDGE7 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT3_INTR_MASK | 0x40310198 | FULL | Port interrupt mask register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT3_INTR_MASKED | 0x4031019C | FULL | Port interrupt masked status register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT3_INTR_SET | 0x403101A0 | FULL | Port interrupt set register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT3_INTR_CFG | 0x403101C0 | FULL | Port interrupt configuration register Note:EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT3_CFG | 0x403101C4 | FULL | Port configuration register Note:DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT3_CFG_IN | 0x403101C8 | FULL | Port input buffer configuration register Note:VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT3_CFG_OUT | 0x403101CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT3_CFG_IN_AUTOLVL | 0x403101D8 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.5 PRT 4

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|--|
| GPIO_PRT4_OUT | 0x40310200 | FULL | Port output data register Note:OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT4_OUT_CLR | 0x40310204 | FULL | Port output data clear register |
| GPIO_PRT4_OUT_SET | 0x40310208 | FULL | Port output data set register |
| GPIO_PRT4_OUT_INV | 0x4031020C | FULL | Port output data invert register |
| GPIO_PRT4_IN | 0x40310210 | FULL | Port input state register Note:IN5 IN6 IN7 are not available for this register |
| GPIO_PRT4_INTR | 0x40310214 | FULL | Port interrupt status register Note:EDGE5 EDGE6 EDGE7 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT4_INTR_MASK | 0x40310218 | FULL | Port interrupt mask register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT4_INTR_MASKED | 0x4031021C | FULL | Port interrupt masked status register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT4_INTR_SET | 0x40310220 | FULL | Port interrupt set register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT4_INTR_CFG | 0x40310240 | FULL | Port interrupt configuration register Note:EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT4_CFG | 0x40310244 | FULL | Port configuration register Note:DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT4_CFG_IN | 0x40310248 | FULL | Port input buffer configuration register Note:VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT4_CFG_OUT | 0x4031024C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT4_CFG_IN_AUTOLVL | 0x40310258 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.6 PRT 5

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT5_OUT | 0x40310280 | FULL | Port output data register Note:OUT6 OUT7 are not available for this register |
| GPIO_PRT5_OUT_CLR | 0x40310284 | FULL | Port output data clear register |
| GPIO_PRT5_OUT_SET | 0x40310288 | FULL | Port output data set register |
| GPIO_PRT5_OUT_INV | 0x4031028C | FULL | Port output data invert register |
| GPIO_PRT5_IN | 0x40310290 | FULL | Port input state register Note:IN6 IN7 are not available for this register |
| GPIO_PRT5_INTR | 0x40310294 | FULL | Port interrupt status register Note:EDGE6 EDGE7 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT5_INTR_MASK | 0x40310298 | FULL | Port interrupt mask register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT5_INTR_MASKED | 0x4031029C | FULL | Port interrupt masked status register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT5_INTR_SET | 0x403102A0 | FULL | Port interrupt set register Note:EDGE6 EDGE7 are not available for this register |
| GPIO_PRT5_INTR_CFG | 0x403102C0 | FULL | Port interrupt configuration register Note:EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT5_CFG | 0x403102C4 | FULL | Port configuration register Note:DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT5_CFG_IN | 0x403102C8 | FULL | Port input buffer configuration register Note:VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT5_CFG_OUT | 0x403102CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT5_CFG_IN_AUTOLVL | 0x403102D8 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.7 PRT 6

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT6_OUT | 0x40310300 | FULL | Port output data register |
| GPIO_PRT6_OUT_CLR | 0x40310304 | FULL | Port output data clear register |
| GPIO_PRT6_OUT_SET | 0x40310308 | FULL | Port output data set register |
| GPIO_PRT6_OUT_INV | 0x4031030C | FULL | Port output data invert register |
| GPIO_PRT6_IN | 0x40310310 | FULL | Port input state register |
| GPIO_PRT6_INTR | 0x40310314 | FULL | Port interrupt status register |
| GPIO_PRT6_INTR_MASK | 0x40310318 | FULL | Port interrupt mask register |
| GPIO_PRT6_INTR_MASKED | 0x4031031C | FULL | Port interrupt masked status register |
| GPIO_PRT6_INTR_SET | 0x40310320 | FULL | Port interrupt set register |
| GPIO_PRT6_INTR_CFG | 0x40310340 | FULL | Port interrupt configuration register |
| GPIO_PRT6_CFG | 0x40310344 | FULL | Port configuration register |
| GPIO_PRT6_CFG_IN | 0x40310348 | FULL | Port input buffer configuration register |
| GPIO_PRT6_CFG_OUT | 0x4031034C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT6_CFG_IN_AUTOLVL | 0x40310358 | FULL | Port input buffer AUTOLVL configuration register |

15.8 PRT 7

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|----------------------------------|
| GPIO_PRT7_OUT | 0x40310380 | FULL | Port output data register |
| GPIO_PRT7_OUT_CLR | 0x40310384 | FULL | Port output data clear register |
| GPIO_PRT7_OUT_SET | 0x40310388 | FULL | Port output data set register |
| GPIO_PRT7_OUT_INV | 0x4031038C | FULL | Port output data invert register |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT7_IN | 0x40310390 | FULL | Port input state register |
| GPIO_PRT7_INTR | 0x40310394 | FULL | Port interrupt status register |
| GPIO_PRT7_INTR_MASK | 0x40310398 | FULL | Port interrupt mask register |
| GPIO_PRT7_INTR_MASKED | 0x4031039C | FULL | Port interrupt masked status register |
| GPIO_PRT7_INTR_SET | 0x403103A0 | FULL | Port interrupt set register |
| GPIO_PRT7_INTR_CFG | 0x403103C0 | FULL | Port interrupt configuration register |
| GPIO_PRT7_CFG | 0x403103C4 | FULL | Port configuration register |
| GPIO_PRT7_CFG_IN | 0x403103C8 | FULL | Port input buffer configuration register |
| GPIO_PRT7_CFG_OUT | 0x403103CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT7_CFG_IN_AUTOLVL | 0x403103D8 | FULL | Port input buffer AUTOLVL configuration register |

15.9 PRT 8

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|--|
| GPIO_PRT8_OUT | 0x40310400 | FULL | Port output data register Note:OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT8_OUT_CLR | 0x40310404 | FULL | Port output data clear register |
| GPIO_PRT8_OUT_SET | 0x40310408 | FULL | Port output data set register |
| GPIO_PRT8_OUT_INV | 0x4031040C | FULL | Port output data invert register |
| GPIO_PRT8_IN | 0x40310410 | FULL | Port input state register Note:IN5 IN6 IN7 are not available for this register |
| GPIO_PRT8_INTR | 0x40310414 | FULL | Port interrupt status register Note:EDGE5 EDGE6 EDGE7 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT8_INTR_MASK | 0x40310418 | FULL | Port interrupt mask register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT8_INTR_MASKED | 0x4031041C | FULL | Port interrupt masked status register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT8_INTR_SET | 0x40310420 | FULL | Port interrupt set register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT8_INTR_CFG | 0x40310440 | FULL | Port interrupt configuration register Note:EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT8_CFG | 0x40310444 | FULL | Port configuration register Note:DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT8_CFG_IN | 0x40310448 | FULL | Port input buffer configuration register Note:VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT8_CFG_OUT | 0x4031044C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT8_CFG_IN_AUTOLVL | 0x40310458 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.10 PRT 9

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|--|
| GPIO_PRT9_OUT | 0x40310480 | FULL | Port output data register Note:OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT9_OUT_CLR | 0x40310484 | FULL | Port output data clear register |
| GPIO_PRT9_OUT_SET | 0x40310488 | FULL | Port output data set register |
| GPIO_PRT9_OUT_INV | 0x4031048C | FULL | Port output data invert register |
| GPIO_PRT9_IN | 0x40310490 | FULL | Port input state register Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT9_INTR | 0x40310494 | FULL | Port interrupt status register Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---|
| GPIO_PRT9_INTR_MASK | 0x40310498 | FULL | Port interrupt mask register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT9_INTR_MASKED | 0x4031049C | FULL | Port interrupt masked status register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT9_INTR_SET | 0x403104A0 | FULL | Port interrupt set register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT9_INTR_CFG | 0x403104C0 | FULL | Port interrupt configuration register Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT9_CFG | 0x403104C4 | FULL | Port configuration register Note:DRIVE_MODE4 IN_EN4 DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT9_CFG_IN | 0x403104C8 | FULL | Port input buffer configuration register Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT9_CFG_OUT | 0x403104CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT9_CFG_IN_AUTOLVL | 0x403104D8 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.11 PRT 10

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT10_OUT | 0x40310500 | FULL | Port output data register |
| GPIO_PRT10_OUT_CLR | 0x40310504 | FULL | Port output data clear register |
| GPIO_PRT10_OUT_SET | 0x40310508 | FULL | Port output data set register |
| GPIO_PRT10_OUT_INV | 0x4031050C | FULL | Port output data invert register |
| GPIO_PRT10_IN | 0x40310510 | FULL | Port input state register |
| GPIO_PRT10_INTR | 0x40310514 | FULL | Port interrupt status register |
| GPIO_PRT10_INTR_MASK | 0x40310518 | FULL | Port interrupt mask register |
| GPIO_PRT10_INTR_MASKED | 0x4031051C | FULL | Port interrupt masked status register |
| GPIO_PRT10_INTR_SET | 0x40310520 | FULL | Port interrupt set register |
| GPIO_PRT10_INTR_CFG | 0x40310540 | FULL | Port interrupt configuration register |
| GPIO_PRT10_CFG | 0x40310544 | FULL | Port configuration register |
| GPIO_PRT10_CFG_IN | 0x40310548 | FULL | Port input buffer configuration register |
| GPIO_PRT10_CFG_OUT | 0x4031054C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT10_CFG_IN_AUTOLVL | 0x40310558 | FULL | Port input buffer AUTOLVL configuration register |

15.12 PRT 11

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| GPIO_PRT11_OUT | 0x40310580 | FULL | Port output data register Note:OUT3 OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT11_OUT_CLR | 0x40310584 | FULL | Port output data clear register |
| GPIO_PRT11_OUT_SET | 0x40310588 | FULL | Port output data set register |
| GPIO_PRT11_OUT_INV | 0x4031058C | FULL | Port output data invert register |
| GPIO_PRT11_IN | 0x40310590 | FULL | Port input state register Note:IN3 IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT11_INTR | 0x40310594 | FULL | Port interrupt status register Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 IN_IN3 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT11_INTR_MASK | 0x40310598 | FULL | Port interrupt mask register Note:EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |

| Register Name | Address | Permission | Description |
|---|------------|------------|--|
| GPIO_PRT11_INTR_MASKED | 0x4031059C | FULL | Port interrupt masked status register Note: EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT11_INTR_SET | 0x403105A0 | FULL | Port interrupt set register Note: EDGE3 EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT11_INTR_CFG | 0x403105C0 | FULL | Port interrupt configuration register Note: EDGE3_SEL EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT11_CFG | 0x403105C4 | FULL | Port configuration register Note: DRIVE_MODE3 IN_EN3 DRIVE_MODE4 IN_EN4 DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT11_CFG_IN | 0x403105C8 | FULL | Port input buffer configuration register Note: VTRIP_SEL3_0 VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT11_CFG_OUT | 0x403105CC | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL3 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT11_CFG_IN_AUTOLVL | 0x403105D8 | FULL | Port input buffer AUTOLVL configuration register Note: VTRIP_SEL3_1 VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.13 PRT 12

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| GPIO_PRT12_OUT | 0x40310600 | FULL | Port output data register |
| GPIO_PRT12_OUT_CLR | 0x40310604 | FULL | Port output data clear register |
| GPIO_PRT12_OUT_SET | 0x40310608 | FULL | Port output data set register |
| GPIO_PRT12_OUT_INV | 0x4031060C | FULL | Port output data invert register |
| GPIO_PRT12_IN | 0x40310610 | FULL | Port input state register |
| GPIO_PRT12_INTR | 0x40310614 | FULL | Port interrupt status register |
| GPIO_PRT12_INTR_MASK | 0x40310618 | FULL | Port interrupt mask register |
| GPIO_PRT12_INTR_MASKED | 0x4031061C | FULL | Port interrupt masked status register |
| GPIO_PRT12_INTR_SET | 0x40310620 | FULL | Port interrupt set register |
| GPIO_PRT12_INTR_CFG | 0x40310640 | FULL | Port interrupt configuration register |
| GPIO_PRT12_CFG | 0x40310644 | FULL | Port configuration register |
| GPIO_PRT12_CFG_IN | 0x40310648 | FULL | Port input buffer configuration register |
| GPIO_PRT12_CFG_OUT | 0x4031064C | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT12_CFG_IN_AUTOLVL | 0x40310658 | FULL | Port input buffer AUTOLVL configuration register |

15.14 PRT 13

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| GPIO_PRT13_OUT | 0x40310680 | FULL | Port output data register |
| GPIO_PRT13_OUT_CLR | 0x40310684 | FULL | Port output data clear register |
| GPIO_PRT13_OUT_SET | 0x40310688 | FULL | Port output data set register |
| GPIO_PRT13_OUT_INV | 0x4031068C | FULL | Port output data invert register |
| GPIO_PRT13_IN | 0x40310690 | FULL | Port input state register |
| GPIO_PRT13_INTR | 0x40310694 | FULL | Port interrupt status register |
| GPIO_PRT13_INTR_MASK | 0x40310698 | FULL | Port interrupt mask register |
| GPIO_PRT13_INTR_MASKED | 0x4031069C | FULL | Port interrupt masked status register |
| GPIO_PRT13_INTR_SET | 0x403106A0 | FULL | Port interrupt set register |
| GPIO_PRT13_INTR_CFG | 0x403106C0 | FULL | Port interrupt configuration register |
| GPIO_PRT13_CFG | 0x403106C4 | FULL | Port configuration register |
| GPIO_PRT13_CFG_IN | 0x403106C8 | FULL | Port input buffer configuration register |
| GPIO_PRT13_CFG_OUT | 0x403106CC | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT13_CFG_IN_AUTOLVL | 0x403106D8 | FULL | Port input buffer AUTOLVL configuration register |

15.15 PRT 14

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--|
| GPIO_PRT14_OUT | 0x40310700 | FULL | Port output data register |
| GPIO_PRT14_OUT_CLR | 0x40310704 | FULL | Port output data clear register |
| GPIO_PRT14_OUT_SET | 0x40310708 | FULL | Port output data set register |
| GPIO_PRT14_OUT_INV | 0x4031070C | FULL | Port output data invert register |
| GPIO_PRT14_IN | 0x40310710 | FULL | Port input state register |
| GPIO_PRT14_INTR | 0x40310714 | FULL | Port interrupt status register |
| GPIO_PRT14_INTR_MASK | 0x40310718 | FULL | Port interrupt mask register |
| GPIO_PRT14_INTR_MASKED | 0x4031071C | FULL | Port interrupt masked status register |
| GPIO_PRT14_INTR_SET | 0x40310720 | FULL | Port interrupt set register |
| GPIO_PRT14_INTR_CFG | 0x40310740 | FULL | Port interrupt configuration register |
| GPIO_PRT14_CFG | 0x40310744 | FULL | Port configuration register |
| GPIO_PRT14_CFG_IN | 0x40310748 | FULL | Port input buffer configuration register |
| GPIO_PRT14_CFG_OUT | 0x4031074C | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT14_CFG_IN_AUTOLVL | 0x40310758 | FULL | Port input buffer AUTOLVL configuration register |

15.16 PRT 15

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--|
| GPIO_PRT15_OUT | 0x40310780 | FULL | Port output data register Note: OUT4 OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT15_OUT_CLR | 0x40310784 | FULL | Port output data clear register |
| GPIO_PRT15_OUT_SET | 0x40310788 | FULL | Port output data set register |
| GPIO_PRT15_OUT_INV | 0x4031078C | FULL | Port output data invert register |
| GPIO_PRT15_IN | 0x40310790 | FULL | Port input state register Note: IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT15_INTR | 0x40310794 | FULL | Port interrupt status register Note: EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT15_INTR_MASK | 0x40310798 | FULL | Port interrupt mask register Note: EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT15_INTR_MASKED | 0x4031079C | FULL | Port interrupt masked status register Note: EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT15_INTR_SET | 0x403107A0 | FULL | Port interrupt set register Note: EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT15_INTR_CFG | 0x403107C0 | FULL | Port interrupt configuration register Note: EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT15_CFG | 0x403107C4 | FULL | Port configuration register Note: DRIVE_MODE4 IN_EN4 DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT15_CFG_IN | 0x403107C8 | FULL | Port input buffer configuration register Note: VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT15_CFG_OUT | 0x403107CC | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT15_CFG_IN_AUTOLVL | 0x403107D8 | FULL | Port input buffer AUTOLVL configuration register Note: VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.17 PRT 16

| Register Name | Address | Permission | Description |
|----------------|------------|------------|--|
| GPIO_PRT16_OUT | 0x40310800 | FULL | Port output data register Note: OUT4 OUT5 OUT6 OUT7 are not available for this register |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT16_OUT_CLR | 0x40310804 | FULL | Port output data clear register |
| GPIO_PRT16_OUT_SET | 0x40310808 | FULL | Port output data set register |
| GPIO_PRT16_OUT_INV | 0x4031080C | FULL | Port output data invert register |
| GPIO_PRT16_IN | 0x40310810 | FULL | Port input state register Note:IN4 IN5 IN6 IN7 are not available for this register |
| GPIO_PRT16_INTR | 0x40310814 | FULL | Port interrupt status register Note:EDGE4 EDGE5 EDGE6 EDGE7 IN_IN4 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT16_INTR_MASK | 0x40310818 | FULL | Port interrupt mask register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT16_INTR_MASKED | 0x4031081C | FULL | Port interrupt masked status register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT16_INTR_SET | 0x40310820 | FULL | Port interrupt set register Note:EDGE4 EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT16_INTR_CFG | 0x40310840 | FULL | Port interrupt configuration register Note:EDGE4_SEL EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT16_CFG | 0x40310844 | FULL | Port configuration register Note:DRIVE_MODE4 IN_EN4 DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT16_CFG_IN | 0x40310848 | FULL | Port input buffer configuration register Note:VTRIP_SEL4_0 VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT16_CFG_OUT | 0x4031084C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL4 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT16_CFG_IN_AUTOLVL | 0x40310858 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL4_1 VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.18 PRT 17

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT17_OUT | 0x40310880 | FULL | Port output data register |
| GPIO_PRT17_OUT_CLR | 0x40310884 | FULL | Port output data clear register |
| GPIO_PRT17_OUT_SET | 0x40310888 | FULL | Port output data set register |
| GPIO_PRT17_OUT_INV | 0x4031088C | FULL | Port output data invert register |
| GPIO_PRT17_IN | 0x40310890 | FULL | Port input state register |
| GPIO_PRT17_INTR | 0x40310894 | FULL | Port interrupt status register |
| GPIO_PRT17_INTR_MASK | 0x40310898 | FULL | Port interrupt mask register |
| GPIO_PRT17_INTR_MASKED | 0x4031089C | FULL | Port interrupt masked status register |
| GPIO_PRT17_INTR_SET | 0x403108A0 | FULL | Port interrupt set register |
| GPIO_PRT17_INTR_CFG | 0x403108C0 | FULL | Port interrupt configuration register |
| GPIO_PRT17_CFG | 0x403108C4 | FULL | Port configuration register |
| GPIO_PRT17_CFG_IN | 0x403108C8 | FULL | Port input buffer configuration register |
| GPIO_PRT17_CFG_OUT | 0x403108CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT17_CFG_IN_AUTOLVL | 0x403108D8 | FULL | Port input buffer AUTOLVL configuration register |

15.19 PRT 18

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|---------------------------------------|
| GPIO_PRT18_OUT | 0x40310900 | FULL | Port output data register |
| GPIO_PRT18_OUT_CLR | 0x40310904 | FULL | Port output data clear register |
| GPIO_PRT18_OUT_SET | 0x40310908 | FULL | Port output data set register |
| GPIO_PRT18_OUT_INV | 0x4031090C | FULL | Port output data invert register |
| GPIO_PRT18_IN | 0x40310910 | FULL | Port input state register |
| GPIO_PRT18_INTR | 0x40310914 | FULL | Port interrupt status register |
| GPIO_PRT18_INTR_MASK | 0x40310918 | FULL | Port interrupt mask register |
| GPIO_PRT18_INTR_MASKED | 0x4031091C | FULL | Port interrupt masked status register |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT18_INTR_SET | 0x40310920 | FULL | Port interrupt set register |
| GPIO_PRT18_INTR_CFG | 0x40310940 | FULL | Port interrupt configuration register |
| GPIO_PRT18_CFG | 0x40310944 | FULL | Port configuration register |
| GPIO_PRT18_CFG_IN | 0x40310948 | FULL | Port input buffer configuration register |
| GPIO_PRT18_CFG_OUT | 0x4031094C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT18_CFG_IN_AUTOLVL | 0x40310958 | FULL | Port input buffer AUTOLVL configuration register |

15.20 PRT 19

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--|
| GPIO_PRT19_OUT | 0x40310980 | FULL | Port output data register Note:OUT5 OUT6 OUT7 are not available for this register |
| GPIO_PRT19_OUT_CLR | 0x40310984 | FULL | Port output data clear register |
| GPIO_PRT19_OUT_SET | 0x40310988 | FULL | Port output data set register |
| GPIO_PRT19_OUT_INV | 0x4031098C | FULL | Port output data invert register |
| GPIO_PRT19_IN | 0x40310990 | FULL | Port input state register Note:IN5 IN6 IN7 are not available for this register |
| GPIO_PRT19_INTR | 0x40310994 | FULL | Port interrupt status register Note:EDGE5 EDGE6 EDGE7 IN_IN5 IN_IN6 IN_IN7 are not available for this register |
| GPIO_PRT19_INTR_MASK | 0x40310998 | FULL | Port interrupt mask register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT19_INTR_MASKED | 0x4031099C | FULL | Port interrupt masked status register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT19_INTR_SET | 0x403109A0 | FULL | Port interrupt set register Note:EDGE5 EDGE6 EDGE7 are not available for this register |
| GPIO_PRT19_INTR_CFG | 0x403109C0 | FULL | Port interrupt configuration register Note:EDGE5_SEL EDGE6_SEL EDGE7_SEL are not available for this register |
| GPIO_PRT19_CFG | 0x403109C4 | FULL | Port configuration register Note:DRIVE_MODE5 IN_EN5 DRIVE_MODE6 IN_EN6 DRIVE_MODE7 IN_EN7 are not available for this register |
| GPIO_PRT19_CFG_IN | 0x403109C8 | FULL | Port input buffer configuration register Note:VTRIP_SEL5_0 VTRIP_SEL6_0 VTRIP_SEL7_0 are not available for this register |
| GPIO_PRT19_CFG_OUT | 0x403109CC | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 DRIVE_SEL5 DRIVE_SEL6 DRIVE_SEL7 are not available for this register |
| GPIO_PRT19_CFG_IN_AUTOLVL | 0x403109D8 | FULL | Port input buffer AUTOLVL configuration register Note:VTRIP_SEL5_1 VTRIP_SEL6_1 VTRIP_SEL7_1 are not available for this register |

15.21 PRT 20

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT20_OUT | 0x40310A00 | FULL | Port output data register |
| GPIO_PRT20_OUT_CLR | 0x40310A04 | FULL | Port output data clear register |
| GPIO_PRT20_OUT_SET | 0x40310A08 | FULL | Port output data set register |
| GPIO_PRT20_OUT_INV | 0x40310A0C | FULL | Port output data invert register |
| GPIO_PRT20_IN | 0x40310A10 | FULL | Port input state register |
| GPIO_PRT20_INTR | 0x40310A14 | FULL | Port interrupt status register |
| GPIO_PRT20_INTR_MASK | 0x40310A18 | FULL | Port interrupt mask register |
| GPIO_PRT20_INTR_MASKED | 0x40310A1C | FULL | Port interrupt masked status register |
| GPIO_PRT20_INTR_SET | 0x40310A20 | FULL | Port interrupt set register |
| GPIO_PRT20_INTR_CFG | 0x40310A40 | FULL | Port interrupt configuration register |
| GPIO_PRT20_CFG | 0x40310A44 | FULL | Port configuration register |
| GPIO_PRT20_CFG_IN | 0x40310A48 | FULL | Port input buffer configuration register |
| GPIO_PRT20_CFG_OUT | 0x40310A4C | FULL | Port output buffer configuration register Note:SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT20_CFG_IN_AUTOLVL | 0x40310A58 | FULL | Port input buffer AUTOLVL configuration register |

15.22 PRT 21

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT21_OUT | 0x40310A80 | FULL | Port output data register |
| GPIO_PRT21_OUT_CLR | 0x40310A84 | FULL | Port output data clear register |
| GPIO_PRT21_OUT_SET | 0x40310A88 | FULL | Port output data set register |
| GPIO_PRT21_OUT_INV | 0x40310A8C | FULL | Port output data invert register |
| GPIO_PRT21_IN | 0x40310A90 | FULL | Port input state register |
| GPIO_PRT21_INTR | 0x40310A94 | FULL | Port interrupt status register |
| GPIO_PRT21_INTR_MASK | 0x40310A98 | FULL | Port interrupt mask register |
| GPIO_PRT21_INTR_MASKED | 0x40310A9C | FULL | Port interrupt masked status register |
| GPIO_PRT21_INTR_SET | 0x40310AA0 | FULL | Port interrupt set register |
| GPIO_PRT21_INTR_CFG | 0x40310AC0 | FULL | Port interrupt configuration register |
| GPIO_PRT21_CFG | 0x40310AC4 | FULL | Port configuration register |
| GPIO_PRT21_CFG_IN | 0x40310AC8 | FULL | Port input buffer configuration register |
| GPIO_PRT21_CFG_OUT | 0x40310ACC | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT21_CFG_IN_AUTOLVL | 0x40310AD8 | FULL | Port input buffer AUTOLVL configuration register |

15.23 PRT 22

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT22_OUT | 0x40310B00 | FULL | Port output data register |
| GPIO_PRT22_OUT_CLR | 0x40310B04 | FULL | Port output data clear register |
| GPIO_PRT22_OUT_SET | 0x40310B08 | FULL | Port output data set register |
| GPIO_PRT22_OUT_INV | 0x40310B0C | FULL | Port output data invert register |
| GPIO_PRT22_IN | 0x40310B10 | FULL | Port input state register |
| GPIO_PRT22_INTR | 0x40310B14 | FULL | Port interrupt status register |
| GPIO_PRT22_INTR_MASK | 0x40310B18 | FULL | Port interrupt mask register |
| GPIO_PRT22_INTR_MASKED | 0x40310B1C | FULL | Port interrupt masked status register |
| GPIO_PRT22_INTR_SET | 0x40310B20 | FULL | Port interrupt set register |
| GPIO_PRT22_INTR_CFG | 0x40310B40 | FULL | Port interrupt configuration register |
| GPIO_PRT22_CFG | 0x40310B44 | FULL | Port configuration register |
| GPIO_PRT22_CFG_IN | 0x40310B48 | FULL | Port input buffer configuration register |
| GPIO_PRT22_CFG_OUT | 0x40310B4C | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT22_CFG_IN_AUTOLVL | 0x40310B58 | FULL | Port input buffer AUTOLVL configuration register |

15.24 PRT 23

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| GPIO_PRT23_OUT | 0x40310B80 | FULL | Port output data register |
| GPIO_PRT23_OUT_CLR | 0x40310B84 | FULL | Port output data clear register |
| GPIO_PRT23_OUT_SET | 0x40310B88 | FULL | Port output data set register |
| GPIO_PRT23_OUT_INV | 0x40310B8C | FULL | Port output data invert register |
| GPIO_PRT23_IN | 0x40310B90 | FULL | Port input state register |
| GPIO_PRT23_INTR | 0x40310B94 | FULL | Port interrupt status register |
| GPIO_PRT23_INTR_MASK | 0x40310B98 | FULL | Port interrupt mask register |
| GPIO_PRT23_INTR_MASKED | 0x40310B9C | FULL | Port interrupt masked status register |
| GPIO_PRT23_INTR_SET | 0x40310BA0 | FULL | Port interrupt set register |
| GPIO_PRT23_INTR_CFG | 0x40310BC0 | FULL | Port interrupt configuration register |
| GPIO_PRT23_CFG | 0x40310BC4 | FULL | Port configuration register |
| GPIO_PRT23_CFG_IN | 0x40310BC8 | FULL | Port input buffer configuration register |
| GPIO_PRT23_CFG_OUT | 0x40310BCC | FULL | Port output buffer configuration register Note: SLOW0 SLOW1 SLOW2 SLOW3 SLOW4 SLOW5 SLOW6 SLOW7 are not available for this register |
| GPIO_PRT23_CFG_IN_AUTOLVL | 0x40310BD8 | FULL | Port input buffer AUTOLVL configuration register |

15.25 Register Details

15.25.1 GPIO_INTR_CAUSE0

Description: Interrupt port cause register 0
Address: 0x40314000
Offset: 0x4000
Retention: Retained
IsDeepSleep: No
Comment: This register provides interrupt status corresponding to ports 0 to 31
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|----|----|----|----|----|----|----|
| Name | PORT_INT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PORT_INT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PORT_INT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PORT_INT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:31 | PORT_INT | R | W | 0 | Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects 'gpio_interrupts[i]' for IO port i). The register is used when the system uses a combined interrupt line 'gpio_interrupt'. The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt |

15.25.2 GPIO_VDD_ACTIVE

Description: Extern power supply detection register
Address: 0x40314010
Offset: 0x4010
Retention: Retained
IsDeepSleep: No
Comment: This register provides external power supply status
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---------------------|--------------|----|----|----|----|----|
| Name | VDDIO_ACTIVE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VDDIO_ACTIVE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:15 | VDDIO_ACTIVE | R | W | 0 | <p>Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result.</p> <p>'0': Supply is not present '1': Supply is present</p> <p>When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation. For example 'vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1' are present then they will be assigned to these bits as below: 0: vbackup, 1: vddio_0, 2: vddio_1, 3: vddio_a, 4: vddio_r, 5: vddusb'</p> |
| 30 | VDDA_ACTIVE | R | W | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | R | W | 0 | This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) |

15.25.3 GPIO_VDD_INTR

Description: Supply detection interrupt register

Address: 0x40314014

Offset: 0x4014

Retention: Retained

IsDeepSleep: No

Comment: An interrupt cause is cleared (set to '0') by writing a '1' to the corresponding bit field. It is not recommended to write 0xFF to clear all interrupt causes, as a new interrupt cause may have occurred between reading the register and clearing. Note that the interrupt cause fields and the associated interrupt provide DeepSleep functionality (interrupt causes can be set to '1' and cause the system to wake up from DeepSleep power mode). This register is set whenever a supply ramp up or ramp down is detected. Some bits may be set after system power-up, depending on power supply sequencing.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---------------------|--------------|----|----|----|----|----|
| Name | VDDIO_ACTIVE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VDDIO_ACTIVE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|------|----|-----------------|--|
| 0:15 | VDDIO_ACTIVE | RW1C | A | 0 | Supply state change detected. '0': No change to supply detected '1': Change to supply detected |
| 30 | VDDA_ACTIVE | RW1C | A | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | RW1C | A | 0 | The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. |

15.25.4 GPIO_VDD_INTR_MASK

Description: Supply detection interrupt mask register
Address: 0x40314018
Offset: 0x4018
Retention: Retained
IsDeepSleep: No
Comment: This register configures the supply detection interrupts for all supplies. This register only masks the forwarding of interrupts to the CPU(s), it does not enable/disable the logging of interrupts into the VDD_INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---------------------|--------------|----|----|----|----|----|
| Name | VDDIO_ACTIVE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VDDIO_ACTIVE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:15 | VDDIO_ACTIVE | RW | R | 0 | Masks supply interrupt on VDDIO. '0': VDDIO interrupt forwarding disabled '1': VDDIO interrupt forwarding enabled |
| 30 | VDDA_ACTIVE | RW | R | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | RW | R | 0 | Same as VDDIO_ACTIVE for the digital supply VDDD. |

15.25.5 GPIO_VDD_INTR_MASKED

Description: Supply detection interrupt masked register
Address: 0x4031401C
Offset: 0x401C
Retention: Retained
IsDeepSleep: No
Comment: This register contains the AND-ed values of VDD_INTR and VDD_INTR_MASK registers
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---------------------|--------------|----|----|----|----|----|
| Name | VDDIO_ACTIVE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VDDIO_ACTIVE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:15 | VDDIO_ACTIVE | R | W | 0 | Supply transition detected AND masked '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU |
| 30 | VDDA_ACTIVE | R | W | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | R | W | 0 | Same as VDDIO_ACTIVE for the digital supply VDDD. |

15.25.6 GPIO_VDD_INTR_SET

Description: Supply detection interrupt set register
Address: 0x40314020
Offset: 0x4020
Retention: Retained
IsDeepSleep: No
Comment: Allows firmware or debugger to set interrupt bits in the VDD_INTR register by writing a '1' to the corresponding bit field. When read, returns the same value as the VDD_INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---------------------|--------------|----|----|----|----|----|
| Name | VDDIO_ACTIVE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | VDDIO_ACTIVE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VDDD_ACTIVE [31:31] | VDDA_ACTIVE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|------|----|-----------------|---|
| 0:15 | VDDIO_ACTIVE | RW1S | A | 0 | Sets supply interrupt. '0': Interrupt state not affected '1': Interrupt set |
| 30 | VDDA_ACTIVE | RW1S | A | 0 | Same as VDDIO_ACTIVE for the analog supply VDDA. |
| 31 | VDDD_ACTIVE | RW1S | A | 0 | Same as VDDIO_ACTIVE for the digital supply VDDD. |

15.25.7 PRT

15.25.7.1 GPIO_PRT_OUT

Description: Port output data register

Address: 0x40310000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: Used to read and write the output data for the IO pins in the port. A register write changes the output data to the written value. A register read reflects the output data (and not the current state of the input data for the IO pins). Using this register, Read-Modify-Write sequences are safely performed on a port with some IO pins configured as inputs.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | OUT0 | RW | RW | 0 | IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' |
| 1 | OUT1 | RW | RW | 0 | IO output data for pin 1 |
| 2 | OUT2 | RW | RW | 0 | IO output data for pin 2 |
| 3 | OUT3 | RW | RW | 0 | IO output data for pin 3 |
| 4 | OUT4 | RW | RW | 0 | IO output data for pin 4 |
| 5 | OUT5 | RW | RW | 0 | IO output data for pin 5 |
| 6 | OUT6 | RW | RW | 0 | IO output data for pin 6 |
| 7 | OUT7 | RW | RW | 0 | IO output data for pin 7 |

15.25.7.2 GPIO_PRT_OUT_CLR

Description: Port output data clear register

Address: 0x40310004

Offset: 0x4

Retention: Retained

IsDeepSleep: No

Comment: Used to clear output data of specific IO pins in the corresponding port to '0', without affecting the output data of the other IO pads in the port. A register read returns the same value as an OUT register read.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | OUT0 | RW | A | 0 | IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. |
| 1 | OUT1 | RW | A | 0 | IO clear output for pin 1 |
| 2 | OUT2 | RW | A | 0 | IO clear output for pin 2 |
| 3 | OUT3 | RW | A | 0 | IO clear output for pin 3 |
| 4 | OUT4 | RW | A | 0 | IO clear output for pin 4 |
| 5 | OUT5 | RW | A | 0 | IO clear output for pin 5 |
| 6 | OUT6 | RW | A | 0 | IO clear output for pin 6 |
| 7 | OUT7 | RW | A | 0 | IO clear output for pin 7 |

15.25.7.3 GPIO_PRT_OUT_SET

Description: Port output data set register

Address: 0x40310008

Offset: 0x8

Retention: Retained

IsDeepSleep: No

Comment: Used to set output data of specific IO pins in the corresponding port to '1', without affecting the output data of the other IO pads in the port. A register read returns the same value as an OUT register read.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | OUT0 | RW | A | 0 | IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. |
| 1 | OUT1 | RW | A | 0 | IO set output for pin 1 |
| 2 | OUT2 | RW | A | 0 | IO set output for pin 2 |
| 3 | OUT3 | RW | A | 0 | IO set output for pin 3 |
| 4 | OUT4 | RW | A | 0 | IO set output for pin 4 |
| 5 | OUT5 | RW | A | 0 | IO set output for pin 5 |
| 6 | OUT6 | RW | A | 0 | IO set output for pin 6 |
| 7 | OUT7 | RW | A | 0 | IO set output for pin 7 |

15.25.7.4 GPIO_PRT_OUT_INV

Description: Port output data invert register

Address: 0x4031000C

Offset: 0xC

Retention: Retained

IsDeepSleep: No

Comment: Used to invert output data of specific IO pins in the corresponding port, without affecting the output data of the other IO pads in the port. A register read returns the same value as an OUT register read.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | OUT7 [7:7] | OUT6 [6:6] | OUT5 [5:5] | OUT4 [4:4] | OUT3 [3:3] | OUT2 [2:2] | OUT1 [1:1] | OUT0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | OUT0 | RW | A | 0 | IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). |
| 1 | OUT1 | RW | A | 0 | IO invert output for pin 1 |
| 2 | OUT2 | RW | A | 0 | IO invert output for pin 2 |
| 3 | OUT3 | RW | A | 0 | IO invert output for pin 3 |
| 4 | OUT4 | RW | A | 0 | IO invert output for pin 4 |
| 5 | OUT5 | RW | A | 0 | IO invert output for pin 5 |
| 6 | OUT6 | RW | A | 0 | IO invert output for pin 6 |
| 7 | OUT7 | RW | A | 0 | IO invert output for pin 7 |

15.25.7.5 GPIO_PRT_IN

Description: Port input state register
Address: 0x40310010
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment: Used to read current pin status for IO pins that have their input buffer enabled (see CFG_IN).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Name | IN7 [7:7] | IN6 [6:6] | IN5 [5:5] | IN4 [4:4] | IN3 [3:3] | IN2 [2:2] | IN1 [1:1] | IN0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|--------------|
| Name | None [15:9] | | | | | | | FLT_IN [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0 | IN0 | R | W | 0 | IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. |
| 1 | IN1 | R | W | 0 | IO pin state for pin 1 |
| 2 | IN2 | R | W | 0 | IO pin state for pin 2 |
| 3 | IN3 | R | W | 0 | IO pin state for pin 3 |
| 4 | IN4 | R | W | 0 | IO pin state for pin 4 |
| 5 | IN5 | R | W | 0 | IO pin state for pin 5 |
| 6 | IN6 | R | W | 0 | IO pin state for pin 6 |
| 7 | IN7 | R | W | 0 | IO pin state for pin 7 |
| 8 | FLT_IN | R | W | 0 | Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. |

15.25.7.6 GPIO_PRT_INTR

Description: Port interrupt status register

Address: 0x40310014

Offset: 0x14

Retention: Retained

IsDeepSleep: No

Comment: An interrupt cause is cleared (set to '0') by writing a '1' to the corresponding bit field. It is not recommended to write 0xFF to clear all interrupt causes, as a new interrupt cause may have occurred between reading the register and clearing. Note that the pin interrupt provide DeepSleep functionality (interrupt causes can be set to '1' and cause the system to wake up from DeepSleep power mode). The IN.IN fields reflect the logical IO pin states at the time of reading this register (same as the IN register).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-------------------|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | IN_IN7 [23:23] | IN_IN6 [22:22] | IN_IN5 [21:21] | IN_IN4 [20:20] | IN_IN3 [19:19] | IN_IN2 [18:18] | IN_IN1 [17:17] | IN_IN0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----------------------|
| Name | None [31:25] | | | | | | | FLT_IN_IN [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|------|----|-----------------|--|
| 0 | EDGE0 | RW1C | A | 0 | Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. |
| 1 | EDGE1 | RW1C | A | 0 | Edge detect for IO pin 1 |
| 2 | EDGE2 | RW1C | A | 0 | Edge detect for IO pin 2 |
| 3 | EDGE3 | RW1C | A | 0 | Edge detect for IO pin 3 |
| 4 | EDGE4 | RW1C | A | 0 | Edge detect for IO pin 4 |
| 5 | EDGE5 | RW1C | A | 0 | Edge detect for IO pin 5 |
| 6 | EDGE6 | RW1C | A | 0 | Edge detect for IO pin 6 |
| 7 | EDGE7 | RW1C | A | 0 | Edge detect for IO pin 7 |
| 8 | FLT_EDGE | RW1C | A | 0 | Edge detected on filtered pin selected by INTR_CFG.FLT_SEL |
| 16 | IN_IN0 | R | W | 0 | IO pin state for pin 0 |
| 17 | IN_IN1 | R | W | 0 | IO pin state for pin 1 |
| 18 | IN_IN2 | R | W | 0 | IO pin state for pin 2 |
| 19 | IN_IN3 | R | W | 0 | IO pin state for pin 3 |
| 20 | IN_IN4 | R | W | 0 | IO pin state for pin 4 |
| 21 | IN_IN5 | R | W | 0 | IO pin state for pin 5 |
| 22 | IN_IN6 | R | W | 0 | IO pin state for pin 6 |
| 23 | IN_IN7 | R | W | 0 | IO pin state for pin 7 |
| 24 | FLT_IN_IN | R | W | 0 | Filtered pin state for pin selected by INTR_CFG.FLT_SEL |

15.25.7.7 GPIO_PRT_INTR_MASK

Description: Port interrupt mask register

Address: 0x40310018

Offset: 0x18

Retention: Retained

IsDeepSleep: No

Comment: This register configures the edge detection interrupts for all pins in a port. This register only masks the forwarding of interrupts to the CPU(s) interrupt controller, it does not enable/disable the logging of interrupts into the INTR register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-------------------|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0 | EDGE0 | RW | R | 0 | Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled |
| 1 | EDGE1 | RW | R | 0 | Masks edge interrupt on IO pin 1 |
| 2 | EDGE2 | RW | R | 0 | Masks edge interrupt on IO pin 2 |
| 3 | EDGE3 | RW | R | 0 | Masks edge interrupt on IO pin 3 |
| 4 | EDGE4 | RW | R | 0 | Masks edge interrupt on IO pin 4 |
| 5 | EDGE5 | RW | R | 0 | Masks edge interrupt on IO pin 5 |
| 6 | EDGE6 | RW | R | 0 | Masks edge interrupt on IO pin 6 |
| 7 | EDGE7 | RW | R | 0 | Masks edge interrupt on IO pin 7 |
| 8 | FLT_EDGE | RW | R | 0 | Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL |

15.25.7.8 GPIO_PRT_INTR_MASKED

Description: Port interrupt masked status register
Address: 0x4031001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment: This register contains the AND-ed values of INTR and INTR_MASK registers forwarded to the CPU interrupt controller.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-------------------|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0 | EDGE0 | R | W | 0 | Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU |
| 1 | EDGE1 | R | W | 0 | Edge detected and masked on IO pin 1 |
| 2 | EDGE2 | R | W | 0 | Edge detected and masked on IO pin 2 |
| 3 | EDGE3 | R | W | 0 | Edge detected and masked on IO pin 3 |
| 4 | EDGE4 | R | W | 0 | Edge detected and masked on IO pin 4 |
| 5 | EDGE5 | R | W | 0 | Edge detected and masked on IO pin 5 |
| 6 | EDGE6 | R | W | 0 | Edge detected and masked on IO pin 6 |
| 7 | EDGE7 | R | W | 0 | Edge detected and masked on IO pin 7 |
| 8 | FLT_EDGE | R | W | 0 | Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL |

15.25.7.9 GPIO_PRT_INTR_SET

Description: Port interrupt set register
Address: 0x40310020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: Allows firmware or debugger to set interrupt bits in the INTR register by writing a '1' to the corresponding bit field. When read, returns the same value as the INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Name | EDGE7 [7:7] | EDGE6 [6:6] | EDGE5 [5:5] | EDGE4 [4:4] | EDGE3 [3:3] | EDGE2 [2:2] | EDGE1 [1:1] | EDGE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-------------------|
| Name | None [15:9] | | | | | | | FLT_EDGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|----|-----------------|--|
| 0 | EDGE0 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set |
| 1 | EDGE1 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 1 |
| 2 | EDGE2 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 2 |
| 3 | EDGE3 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 3 |
| 4 | EDGE4 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 4 |
| 5 | EDGE5 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 5 |
| 6 | EDGE6 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 6 |
| 7 | EDGE7 | RW1S | A | 0 | Sets edge detect interrupt for IO pin 7 |
| 8 | FLT_EDGE | RW1S | A | 0 | Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL |

15.25.7.10 GPIO_PRT_INTR_CFG

Description: Port interrupt configuration register
Address: 0x40310040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: This register selects the edge detection type for each pin interrupt.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|-------------------|-----------------|-------------------|----|----------------------|----|
| Name | EDGE3_SEL [7:6] | | EDGE2_SEL [5:4] | | EDGE1_SEL [3:2] | | EDGE0_SEL [1:0] | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | EDGE7_SEL [15:14] | | EDGE6_SEL [13:12] | | EDGE5_SEL [11:10] | | EDGE4_SEL [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:21] | | | FLT_SEL [20:18] | | | FLT_EDGE_SEL [17:16] | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0:1 | EDGE0_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 0 |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 2:3 | EDGE1_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 1 |
| 4:5 | EDGE2_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 2 |
| 6:7 | EDGE3_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 3 |
| 8:9 | EDGE4_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 4 |
| 10:11 | EDGE5_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 5 |
| 12:13 | EDGE6_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 6 |
| 14:15 | EDGE7_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for IO pin 7 |
| 16:17 | FLT_EDGE_SEL | RW | R | 0 | Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL) |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 18:20 | FLT_SEL | RW | R | 0 | Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. |

15.25.7.11 GPIO_PRT_CFG

Description: Port configuration register
Address: 0x40310044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Configuration of drive mode and input buffer enable for each pin.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|-------------------|---|---|-----------------|-------------------|---|---|
| Name | IN_EN1 [7:7] | DRIVE_MODE1 [6:4] | | | IN_EN0 [3:3] | DRIVE_MODE0 [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------------|---------------------|----|----|-------------------|--------------------|---|---|
| Name | IN_EN3 [15:15] | DRIVE_MODE3 [14:12] | | | IN_EN2 [11:11] | DRIVE_MODE2 [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|---------------------|----|----|-------------------|---------------------|----|----|
| Name | IN_EN5 [23:23] | DRIVE_MODE5 [22:20] | | | IN_EN4 [19:19] | DRIVE_MODE4 [18:16] | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|---------------------|----|----|-------------------|---------------------|----|----|
| Name | IN_EN7 [31:31] | DRIVE_MODE7 [30:28] | | | IN_EN6 [27:27] | DRIVE_MODE6 [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:2 | DRIVE_MODE0 | RW | R | 0 | The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. |
| | HIGHZ | | | 0 | Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance |
| | RESERVED | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| | PULLUP | | | 2 | Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up |
| | PULLDOWN | | | 3 | Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down |
| | OD_DRIVESLOW | | | 4 | Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|---|
| | OD_DRIVESHIGH | | | 5 | <p>Open drain, drives high</p> <p>For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance</p> <p>For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance</p> |
| | STRONG | | | 6 | <p>Strong D_OUTput buffer</p> <p>For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance</p> <p>For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance</p> |
| | PULLUP_DOWN | | | 7 | <p>Pull up or pull down</p> <p>For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where 'GPIO_DSI_OUT' is a function of PORT_SEL, OUT & DSI_DATA_OUT.</p> <p>For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull up</p> |
| 3 | IN_EN0 | RW | R | 0 | <p>Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue.</p> <p>'0': Input buffer disabled '1': Input buffer enabled</p> |
| 4:6 | DRIVE_MODE1 | RW | R | 0 | The GPIO drive mode for IO pin 1 |
| 7 | IN_EN1 | RW | R | 0 | Enables the input buffer for IO pin 1 |
| 8:10 | DRIVE_MODE2 | RW | R | 0 | The GPIO drive mode for IO pin 2 |
| 11 | IN_EN2 | RW | R | 0 | Enables the input buffer for IO pin 2 |
| 12:14 | DRIVE_MODE3 | RW | R | 0 | The GPIO drive mode for IO pin 3 |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---------------------------------------|
| 15 | IN_EN3 | RW | R | 0 | Enables the input buffer for IO pin 3 |
| 16:18 | DRIVE_MODE4 | RW | R | 0 | The GPIO drive mode for IO pin4 |
| 19 | IN_EN4 | RW | R | 0 | Enables the input buffer for IO pin 4 |
| 20:22 | DRIVE_MODE5 | RW | R | 0 | The GPIO drive mode for IO pin 5 |
| 23 | IN_EN5 | RW | R | 0 | Enables the input buffer for IO pin 5 |
| 24:26 | DRIVE_MODE6 | RW | R | 0 | The GPIO drive mode for IO pin 6 |
| 27 | IN_EN6 | RW | R | 0 | Enables the input buffer for IO pin 6 |
| 28:30 | DRIVE_MODE7 | RW | R | 0 | The GPIO drive mode for IO pin 7 |
| 31 | IN_EN7 | RW | R | 0 | Enables the input buffer for IO pin 7 |

15.25.7.12 GPIO_PRT_CFG_IN

Description: Port input buffer configuration register
Address: 0x40310048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Configures the input buffer for each pin and this register is common for PSoC 6: & Traveo II: GPIO pins. This register control the lower bit i.e. VTRIP_SEL[0].
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| Name | VTRIP_SEL_7_0 [7:7] | VTRIP_SEL_6_0 [6:6] | VTRIP_SEL_5_0 [5:5] | VTRIP_SEL_4_0 [4:4] | VTRIP_SEL_3_0 [3:3] | VTRIP_SEL_2_0 [2:2] | VTRIP_SEL_1_0 [1:1] | VTRIP_SEL_0_0 [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0 | VTRIP_SEL0_0 | RW | R | 0 | Configures the pin 0 input buffer mode (trip points and hysteresis) |
| | CMOS | | | 0 | PSoC 6:: Input buffer compatible with CMOS and I2C interfaces Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 |
| | TTL | | | 1 | PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 |
| 1 | VTRIP_SEL1_0 | RW | R | 0 | Configures the pin 1 input buffer mode (trip points and hysteresis) |
| 2 | VTRIP_SEL2_0 | RW | R | 0 | Configures the pin 2 input buffer mode (trip points and hysteresis) |
| 3 | VTRIP_SEL3_0 | RW | R | 0 | Configures the pin 3 input buffer mode (trip points and hysteresis) |
| 4 | VTRIP_SEL4_0 | RW | R | 0 | Configures the pin 4 input buffer mode (trip points and hysteresis) |
| 5 | VTRIP_SEL5_0 | RW | R | 0 | Configures the pin 5 input buffer mode (trip points and hysteresis) |
| 6 | VTRIP_SEL6_0 | RW | R | 0 | Configures the pin 6 input buffer mode (trip points and hysteresis) |
| 7 | VTRIP_SEL7_0 | RW | R | 0 | Configures the pin 7 input buffer mode (trip points and hysteresis) |

15.25.7.13 GPIO_PRT_CFG_OUT

Description: Port output buffer configuration register

Address: 0x4031004C

Offset: 0x4C

Retention: Retained

IsDeepSleep: No

Comment: Configures the output driver for each pin.

Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before setting the IO drive mode to avoid producing glitches on the bus.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Name | SLOW7 [7:7] | SLOW6 [6:6] | SLOW5 [5:5] | SLOW4 [4:4] | SLOW3 [3:3] | SLOW2 [2:2] | SLOW1 [1:1] | SLOW0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| Name | DRIVE_SEL3 [23:22] | | DRIVE_SEL2 [21:20] | | DRIVE_SEL1 [19:18] | | DRIVE_SEL0 [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| Name | DRIVE_SEL7 [31:30] | | DRIVE_SEL6 [29:28] | | DRIVE_SEL5 [27:26] | | DRIVE_SEL4 [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------|----|----|-----------------|--|
| 0 | SLOW0 | RW | R | 0 | Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate |
| 1 | SLOW1 | RW | R | 0 | Enables slow slew rate for IO pin 1 |
| 2 | SLOW2 | RW | R | 0 | Enables slow slew rate for IO pin 2 |
| 3 | SLOW3 | RW | R | 0 | Enables slow slew rate for IO pin 3 |
| 4 | SLOW4 | RW | R | 0 | Enables slow slew rate for IO pin 4 |
| 5 | SLOW5 | RW | R | 0 | Enables slow slew rate for IO pin 5 |
| 6 | SLOW6 | RW | R | 0 | Enables slow slew rate for IO pin 6 |
| 7 | SLOW7 | RW | R | 0 | Enables slow slew rate for IO pin 7 |
| 16:17 | DRIVE_SEL0 | RW | R | 0 | Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table |
| | DRIVE_SEL_ZERO | | | 0 | Traveo II: GPIO_STD/GPIO_ENH: Full drive strength: GPIO drives current at its max rated spec. Traveo II: _GPIO_SMC: GPIO_SMC default mode. Traveo II: _HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec. |
| | DRIVE_SEL_ONE | | | 1 | Traveo II: GPIO_STD/GPIO_ENH: Full drive strength: GPIO drives current at its max rated spec. Traveo II: _GPIO_SMC: GPIO full drive strength. Traveo II: _HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| | DRIVE_SEL_TWO | | | 2 | Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. Traveo II: _GPIO_SMC: GPIO 1/2 drive strength. Traveo II: _HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec. |
| | DRIVE_SEL_THREE | | | 3 | Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. Traveo II: _GPIO_SMC: GPIO 1/4 drive strength. Traveo II: _HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec. |
| 18:19 | DRIVE_SEL1 | RW | R | 0 | Sets the GPIO drive strength for IO pin 1 |
| 20:21 | DRIVE_SEL2 | RW | R | 0 | Sets the GPIO drive strength for IO pin 2 |
| 22:23 | DRIVE_SEL3 | RW | R | 0 | Sets the GPIO drive strength for IO pin 3 |
| 24:25 | DRIVE_SEL4 | RW | R | 0 | Sets the GPIO drive strength for IO pin 4 |
| 26:27 | DRIVE_SEL5 | RW | R | 0 | Sets the GPIO drive strength for IO pin 5 |
| 28:29 | DRIVE_SEL6 | RW | R | 0 | Sets the GPIO drive strength for IO pin 6 |
| 30:31 | DRIVE_SEL7 | RW | R | 0 | Sets the GPIO drive strength for IO pin 7 |

15.25.7.14 GPIO_PRT_CFG_IN_AUTOLVL

Description: Port input buffer AUTOLVL configuration register
Address: 0x40310058
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment: Configures the GPIO input buffer upper bit i.e. VTRIP_SEL[1] for each pin.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| Name | VTRIP_SEL 7_1 [7:7] | VTRIP_SEL 6_1 [6:6] | VTRIP_SEL 5_1 [5:5] | VTRIP_SEL 4_1 [4:4] | VTRIP_SEL 3_1 [3:3] | VTRIP_SEL 2_1 [2:2] | VTRIP_SEL 1_1 [1:1] | VTRIP_SEL 0_1 [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0 | VTRIP_SELO_1 | RW | R | 0 | Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SELO_0 field. This field is used along with CFG_IN.VTRIP_SELO_0 field as below: {CFG_IN_AUTOLVL.VTRIP_SELO_1,CFG_IN.VTRIP_SELO_0}: |
| | CMOS_OR_TTL | | | 0 | 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotive |
| | AUTO | | | 1 | Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SELO_0. |
| 1 | VTRIP_SEL1_1 | RW | R | 0 | Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SELO_0. |
| 2 | VTRIP_SEL2_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 3 | VTRIP_SEL3_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 4 | VTRIP_SEL4_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 5 | VTRIP_SEL5_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 6 | VTRIP_SEL6_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |
| 7 | VTRIP_SEL7_1 | RW | R | 0 | Input buffer compatible with automotive (elevated Vil) interfaces. |

16 HSIOM

| | |
|---------------------|------------------------------|
| Description | High Speed IO Matrix (HSIOM) |
| Base Address | 0x40300000 |
| Size | 0x4000 |
| Slave Num | MMIO3 - 0 |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|--------------------------------------|
| HSIOM_AMUX_SPLIT_CTL0 | 0x40302000 | FULL | AMUX splitter cell control |
| HSIOM_AMUX_SPLIT_CTL1 | 0x40302004 | FULL | AMUX splitter cell control |
| HSIOM_AMUX_SPLIT_CTL2 | 0x40302008 | FULL | AMUX splitter cell control |
| HSIOM_MONITOR_CTL_0 | 0x40302200 | FULL | Power/Ground Monitor cell control 0 |
| HSIOM_ALT_JTAG_EN | 0x40302240 | FULL | Alternate JTAG IF selection register |

16.1 PRT 0

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|------------------|
| HSIOM_PRT0_PORT_SEL0 | 0x40300000 | FULL | Port selection 0 |

16.2 PRT 1

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|------------------|
| HSIOM_PRT1_PORT_SEL0 | 0x40300010 | FULL | Port selection 0 |

16.3 PRT 2

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|--|
| HSIOM_PRT2_PORT_SEL0 | 0x40300020 | FULL | Port selection 0 |
| HSIOM_PRT2_PORT_SEL1 | 0x40300024 | FULL | Port selection 1 Note:IO6_SEL IO7_SEL are not available for this register |

16.4 PRT 3

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|--|
| HSIOM_PRT3_PORT_SEL0 | 0x40300030 | FULL | Port selection 0 |
| HSIOM_PRT3_PORT_SEL1 | 0x40300034 | FULL | Port selection 1 Note:IO6_SEL IO7_SEL are not available for this register |

16.5 PRT 4

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|--|
| HSIOM_PRT4_PORT_SEL0 | 0x40300040 | FULL | Port selection 0 |
| HSIOM_PRT4_PORT_SEL1 | 0x40300044 | FULL | Port selection 1 Note:IO5_SEL IO6_SEL IO7_SEL are not available for this register |

16.6 PRT 5

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|--|
| HSIOM_PRT5_PORT_SEL0 | 0x40300050 | FULL | Port selection 0 |
| HSIOM_PRT5_PORT_SEL1 | 0x40300054 | FULL | Port selection 1 Note:IO6_SEL IO7_SEL are not available for this register |

16.7 PRT 6

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|------------------|
| HSIOM_PRT6_PORT_SEL0 | 0x40300060 | FULL | Port selection 0 |
| HSIOM_PRT6_PORT_SEL1 | 0x40300064 | FULL | Port selection 1 |

16.8 PRT 7

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|------------------|
| HSIOM_PRT7_PORT_SEL0 | 0x40300070 | FULL | Port selection 0 |
| HSIOM_PRT7_PORT_SEL1 | 0x40300074 | FULL | Port selection 1 |

16.9 PRT 8

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| HSIOM_PRT8_PORT_SEL0 | 0x40300080 | FULL | Port selection 0 |
| HSIOM_PRT8_PORT_SEL1 | 0x40300084 | FULL | Port selection 1 <i>Note:IO5_SEL IO6_SEL IO7_SEL are not available for this register</i> |

16.10 PRT 9

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|------------------|
| HSIOM_PRT9_PORT_SEL0 | 0x40300090 | FULL | Port selection 0 |

16.11 PRT 10

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT10_PORT_SEL0 | 0x403000A0 | FULL | Port selection 0 |
| HSIOM_PRT10_PORT_SEL1 | 0x403000A4 | FULL | Port selection 1 |

16.12 PRT 11

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|--|
| HSIOM_PRT11_PORT_SEL0 | 0x403000B0 | FULL | Port selection 0 <i>Note:IO3_SEL is not available for this register</i> |

16.13 PRT 12

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT12_PORT_SEL0 | 0x403000C0 | FULL | Port selection 0 |
| HSIOM_PRT12_PORT_SEL1 | 0x403000C4 | FULL | Port selection 1 |

16.14 PRT 13

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT13_PORT_SEL0 | 0x403000D0 | FULL | Port selection 0 |
| HSIOM_PRT13_PORT_SEL1 | 0x403000D4 | FULL | Port selection 1 |

16.15 PRT 14

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT14_PORT_SEL0 | 0x403000E0 | FULL | Port selection 0 |
| HSIOM_PRT14_PORT_SEL1 | 0x403000E4 | FULL | Port selection 1 |

16.16 PRT 15

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT15_PORT_SEL0 | 0x403000F0 | FULL | Port selection 0 |

16.17 PRT 16

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT16_PORT_SEL0 | 0x40300100 | FULL | Port selection 0 |

16.18 PRT 17

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT17_PORT_SEL0 | 0x40300110 | FULL | Port selection 0 |
| HSIOM_PRT17_PORT_SEL1 | 0x40300114 | FULL | Port selection 1 |

16.19 PRT 18

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|------------------|
| HSIOM_PRT18_PORT_SEL0 | 0x40300120 | FULL | Port selection 0 |
| HSIOM_PRT18_PORT_SEL1 | 0x40300124 | FULL | Port selection 1 |

16.20 PRT 19

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| HSIOM_PRT19_PORT_SEL0 | 0x40300130 | FULL | Port selection 0 |
| HSIOM_PRT19_PORT_SEL1 | 0x40300134 | FULL | Port selection 1 <i>Note:IO5_SEL IO6_SEL IO7_SEL are not available for this register</i> |

16.21 PRT 20

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| HSIOM_PRT20_PORT_SEL0 | 0x40300140 | FULL | Port selection 0 |
| HSIOM_PRT20_PORT_SEL1 | 0x40300144 | FULL | Port selection 1 |

16.22 PRT 21

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| HSIOM_PRT21_PORT_SEL0 | 0x40300150 | FULL | Port selection 0 |
| HSIOM_PRT21_PORT_SEL1 | 0x40300154 | FULL | Port selection 1 |

16.23 PRT 22

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| HSIOM_PRT22_PORT_SEL0 | 0x40300160 | FULL | Port selection 0 |
| HSIOM_PRT22_PORT_SEL1 | 0x40300164 | FULL | Port selection 1 |

16.24 PRT 23

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| HSIOM_PRT23_PORT_SEL0 | 0x40300170 | FULL | Port selection 0 |
| HSIOM_PRT23_PORT_SEL1 | 0x40300174 | FULL | Port selection 1 |

16.25 Register Details

16.25.1 HSIOM_AMUX_SPLIT_CTL

Description: AMUX splitter cell control

Address: 0x40302000

Offset: 0x2000

Retention: Retained

IsDeepSleep: No

Comment: This register controls the breaking of AMUX buses A and B into multiple segments. It allows for grounding, disconnecting and feeding through. Feeding through is be done straight (from Left segment AMUXBUSA/AMUXBUSB to Right segment AMUXBUSA/AMUXBUSB).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|--------------------|--------------------|--------------------|------------|--------------------|--------------------|--------------------|
| Name | None [7:7] | SWITCH_BB_S0 [6:6] | SWITCH_BB_SR [5:5] | SWITCH_BB_SL [4:4] | None [3:3] | SWITCH_AA_S0 [2:2] | SWITCH_AA_SR [1:1] | SWITCH_AA_SL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0 | SWITCH_AA_SL | RW | R | 0 | T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. |
| 1 | SWITCH_AA_SR | RW | R | 0 | T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. |
| 2 | SWITCH_AA_S0 | RW | R | 0 | T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. |
| 4 | SWITCH_BB_SL | RW | R | 0 | T-switch control for Left AMUXBUSB switch. |
| 5 | SWITCH_BB_SR | RW | R | 0 | T-switch control for Right AMUXBUSB switch. |
| 6 | SWITCH_BB_S0 | RW | R | 0 | T-switch control for AMUXBUSB vssa/ground switch. |

16.25.2 HSIOM_MONITOR_CTL_0

Description: Power/Ground Monitor cell control 0
Address: 0x40302200
Offset: 0x2200
Retention: Retained
IsDeepSleep: No
Comment: This register controls the connectivity of PWR/GND monitor cells to either AMUX bus A or B respectively.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | MONITOR_EN [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | MONITOR_EN [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | MONITOR_EN [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | MONITOR_EN [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:31 | MONITOR_EN | RW | R | 0 | control for switch, which connects the power/ground supply to AMUXBUS_A/B respectively when switch is closed: '0': switch open. '1': switch closed. |

16.25.3 HSIOM_ALT_JTAG_EN

Description: Alternate JTAG IF selection register
Address: 0x40302240
Offset: 0x2240
Retention: Retained
IsDeepSleep: No
Comment: This register provides the alternate JTAG interface selection
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 31 | ENABLE | RW | R | 0 | Provides the selection for alternate JTAG IF connectivity. 0: Primary JTAG interface is selected 1: Secondary (alternate) JTAG interface is selected. This connectivity works ONLY in ACTIVE mode. |

16.25.4 PRT

16.25.4.1 HSIOM_PRT_PORT_SEL0

Description: Port selection 0

Address: 0x40300000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: The High Speed IO Mux (HSIOM) selects the hardware peripheral connection to an IO pin. The default setting of 'GPIO' leaves the pin under CPU control through firmware. Pin specific connections for the 'DS_x' and 'ACT_x' settings are listed in the pinout section of the device datasheet.

Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on (GPIO_PRT_CFG.DRIVE_MODEx) to avoid producing glitches on the bus.

Note: peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0').

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---------------|---|---|---|---|
| Name | None [7:5] | | | IO0_SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----------------|----|----|---|---|
| Name | None [15:13] | | | IO1_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-----------------|----|----|----|----|
| Name | None [23:21] | | | IO2_SEL [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-----------------|----|----|----|----|
| Name | None [31:29] | | | IO3_SEL [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:4 | IO0_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. |
| | GPIO | | | 0 | GPIO controls 'out' |
| | GPIO_DSI | | | 1 | GPIO controls 'out', DSI controls 'output enable' |
| | DSI_DSI | | | 2 | DSI controls 'out' and 'output enable' |
| | DSI_GPIO | | | 3 | DSI controls 'out', GPIO controls 'output enable' |
| | AMUXA | | | 4 | AMUXBUS A |
| | AMUXB | | | 5 | AMUXBUS B |
| | AMUXA_DSI | | | 6 | Analog mux bus A, DSI control |
| | AMUXB_DSI | | | 7 | Analog mux bus B, DSI control |
| | ACT_0 | | | 8 | Active peripheral 0 |
| | ACT_1 | | | 9 | Active peripheral 1 |
| | ACT_2 | | | 10 | Active peripheral 2 |
| | ACT_3 | | | 11 | Active peripheral 3 |
| | DS_0 | | | 12 | Deep Sleep peripheral 0 |
| | DS_1 | | | 13 | Deep Sleep peripheral 1 |
| | DS_2 | | | 14 | Deep Sleep peripheral 2 |
| | DS_3 | | | 15 | Deep Sleep peripheral 3 |
| | ACT_4 | | | 16 | Active peripheral 4 |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|--|
| | ACT_5 | | | 17 | Active peripheral 5 |
| | ACT_6 | | | 18 | Active peripheral 6 |
| | ACT_7 | | | 19 | Active peripheral 7 |
| | ACT_8 | | | 20 | Active peripheral 8 |
| | ACT_9 | | | 21 | Active peripheral 9 |
| | ACT_10 | | | 22 | Active peripheral 10 |
| | ACT_11 | | | 23 | Active peripheral 11 |
| | ACT_12 | | | 24 | Active peripheral 12 |
| | ACT_13 | | | 25 | Active peripheral 13 |
| | ACT_14 | | | 26 | Active peripheral 14 |
| | ACT_15 | | | 27 | Active peripheral 15 |
| | DS_4 | | | 28 | Deep Sleep peripheral 4 |
| | DS_5 | | | 29 | Deep Sleep peripheral 5 |
| | DS_6 | | | 30 | Deep Sleep peripheral 6 |
| | DS_7 | | | 31 | Deep Sleep peripheral 7 |
| 8:12 | IO1_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 1. |
| 16:20 | IO2_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 2. |
| 24:28 | IO3_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 3. |

16.25.4.2 HSIOM_PRT_PORT_SEL1

Description: Port selection 1
Address: 0x40300004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: See PORT_SEL0 for details
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---------------|---|---|---|---|
| Name | None [7:5] | | | IO4_SEL [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----------------|----|----|---|---|
| Name | None [15:13] | | | IO5_SEL [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-----------------|----|----|----|----|
| Name | None [23:21] | | | IO6_SEL [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-----------------|----|----|----|----|
| Name | None [31:29] | | | IO7_SEL [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|--|
| 0:4 | IO4_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. |
| 8:12 | IO5_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 4. |
| 16:20 | IO6_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 5. |
| 24:28 | IO7_SEL | RW | RW | 0 | Selects the peripheral connections of Pin 6. |

17 IPC

Description IPC
Base Address 0x40220000
Size 0x10000
Slave Num MMIO2 - 2

17.1 STRUCT 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|------------------|
| IPC_STRUCT0_ACQUIRE | 0x40220000 | FULL | IPC acquire |
| IPC_STRUCT0_RELEASE | 0x40220004 | FULL | IPC release |
| IPC_STRUCT0_NOTIFY | 0x40220008 | FULL | IPC notification |
| IPC_STRUCT0_DATA0 | 0x4022000C | FULL | IPC data 0 |
| IPC_STRUCT0_DATA1 | 0x40220010 | FULL | IPC data 1 |
| IPC_STRUCT0_LOCK_STATUS | 0x4022001C | FULL | IPC lock status |

17.2 STRUCT 1

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|------------------|
| IPC_STRUCT1_ACQUIRE | 0x40220020 | FULL | IPC acquire |
| IPC_STRUCT1_RELEASE | 0x40220024 | FULL | IPC release |
| IPC_STRUCT1_NOTIFY | 0x40220028 | FULL | IPC notification |
| IPC_STRUCT1_DATA0 | 0x4022002C | FULL | IPC data 0 |
| IPC_STRUCT1_DATA1 | 0x40220030 | FULL | IPC data 1 |
| IPC_STRUCT1_LOCK_STATUS | 0x4022003C | FULL | IPC lock status |

17.3 STRUCT 2

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|------------------|
| IPC_STRUCT2_ACQUIRE | 0x40220040 | FULL | IPC acquire |
| IPC_STRUCT2_RELEASE | 0x40220044 | FULL | IPC release |
| IPC_STRUCT2_NOTIFY | 0x40220048 | FULL | IPC notification |
| IPC_STRUCT2_DATA0 | 0x4022004C | FULL | IPC data 0 |
| IPC_STRUCT2_DATA1 | 0x40220050 | FULL | IPC data 1 |
| IPC_STRUCT2_LOCK_STATUS | 0x4022005C | FULL | IPC lock status |

17.4 STRUCT 3

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|------------------|
| IPC_STRUCT3_ACQUIRE | 0x40220060 | FULL | IPC acquire |
| IPC_STRUCT3_RELEASE | 0x40220064 | FULL | IPC release |
| IPC_STRUCT3_NOTIFY | 0x40220068 | FULL | IPC notification |
| IPC_STRUCT3_DATA0 | 0x4022006C | FULL | IPC data 0 |
| IPC_STRUCT3_DATA1 | 0x40220070 | FULL | IPC data 1 |
| IPC_STRUCT3_LOCK_STATUS | 0x4022007C | FULL | IPC lock status |

17.5 STRUCT 4

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|------------------|
| IPC_STRUCT4_ACQUIRE | 0x40220080 | FULL | IPC acquire |
| IPC_STRUCT4_RELEASE | 0x40220084 | FULL | IPC release |
| IPC_STRUCT4_NOTIFY | 0x40220088 | FULL | IPC notification |
| IPC_STRUCT4_DATA0 | 0x4022008C | FULL | IPC data 0 |
| IPC_STRUCT4_DATA1 | 0x40220090 | FULL | IPC data 1 |
| IPC_STRUCT4_LOCK_STATUS | 0x4022009C | FULL | IPC lock status |

17.6 STRUCT 5

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|------------------|
| IPC_STRUCT5_ACQUIRE | 0x402200A0 | FULL | IPC acquire |
| IPC_STRUCT5_RELEASE | 0x402200A4 | FULL | IPC release |
| IPC_STRUCT5_NOTIFY | 0x402200A8 | FULL | IPC notification |
| IPC_STRUCT5_DATA0 | 0x402200AC | FULL | IPC data 0 |
| IPC_STRUCT5_DATA1 | 0x402200B0 | FULL | IPC data 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------|
| IPC_STRUCT5_LOCK_STATUS | 0x402200BC | FULL | IPC lock status |

17.7 STRUCT 6

| Register Name | Address | Permission | Description |
|---|------------|------------|------------------|
| IPC_STRUCT6_ACQUIRE | 0x402200C0 | FULL | IPC acquire |
| IPC_STRUCT6_RELEASE | 0x402200C4 | FULL | IPC release |
| IPC_STRUCT6_NOTIFY | 0x402200C8 | FULL | IPC notification |
| IPC_STRUCT6_DATA0 | 0x402200CC | FULL | IPC data 0 |
| IPC_STRUCT6_DATA1 | 0x402200D0 | FULL | IPC data 1 |
| IPC_STRUCT6_LOCK_STATUS | 0x402200DC | FULL | IPC lock status |

17.8 STRUCT 7

| Register Name | Address | Permission | Description |
|---|------------|------------|------------------|
| IPC_STRUCT7_ACQUIRE | 0x402200E0 | FULL | IPC acquire |
| IPC_STRUCT7_RELEASE | 0x402200E4 | FULL | IPC release |
| IPC_STRUCT7_NOTIFY | 0x402200E8 | FULL | IPC notification |
| IPC_STRUCT7_DATA0 | 0x402200EC | FULL | IPC data 0 |
| IPC_STRUCT7_DATA1 | 0x402200F0 | FULL | IPC data 1 |
| IPC_STRUCT7_LOCK_STATUS | 0x402200FC | FULL | IPC lock status |

17.9 INTR_STRUCT 0

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT0_INTR | 0x40221000 | FULL | Interrupt |
| IPC_INTR_STRUCT0_INTR_SET | 0x40221004 | FULL | Interrupt set |
| IPC_INTR_STRUCT0_INTR_MASK | 0x40221008 | FULL | Interrupt mask |
| IPC_INTR_STRUCT0_INTR_MASKED | 0x4022100C | FULL | Interrupt masked |

17.10 INTR_STRUCT 1

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT1_INTR | 0x40221020 | FULL | Interrupt |
| IPC_INTR_STRUCT1_INTR_SET | 0x40221024 | FULL | Interrupt set |
| IPC_INTR_STRUCT1_INTR_MASK | 0x40221028 | FULL | Interrupt mask |
| IPC_INTR_STRUCT1_INTR_MASKED | 0x4022102C | FULL | Interrupt masked |

17.11 INTR_STRUCT 2

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT2_INTR | 0x40221040 | FULL | Interrupt |
| IPC_INTR_STRUCT2_INTR_SET | 0x40221044 | FULL | Interrupt set |
| IPC_INTR_STRUCT2_INTR_MASK | 0x40221048 | FULL | Interrupt mask |
| IPC_INTR_STRUCT2_INTR_MASKED | 0x4022104C | FULL | Interrupt masked |

17.12 INTR_STRUCT 3

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT3_INTR | 0x40221060 | FULL | Interrupt |
| IPC_INTR_STRUCT3_INTR_SET | 0x40221064 | FULL | Interrupt set |
| IPC_INTR_STRUCT3_INTR_MASK | 0x40221068 | FULL | Interrupt mask |
| IPC_INTR_STRUCT3_INTR_MASKED | 0x4022106C | FULL | Interrupt masked |

17.13 INTR_STRUCT 4

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT4_INTR | 0x40221080 | FULL | Interrupt |
| IPC_INTR_STRUCT4_INTR_SET | 0x40221084 | FULL | Interrupt set |
| IPC_INTR_STRUCT4_INTR_MASK | 0x40221088 | FULL | Interrupt mask |
| IPC_INTR_STRUCT4_INTR_MASKED | 0x4022108C | FULL | Interrupt masked |

17.14 INTR_STRUCT 5

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------|
| IPC_INTR_STRUCT5_INTR | 0x402210A0 | FULL | Interrupt |
| IPC_INTR_STRUCT5_INTR_SET | 0x402210A4 | FULL | Interrupt set |

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT5_INTR_MASK | 0x402210A8 | FULL | Interrupt mask |
| IPC_INTR_STRUCT5_INTR_MASKED | 0x402210AC | FULL | Interrupt masked |

17.15 INTR_STRUCT 6

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT6_INTR | 0x402210C0 | FULL | Interrupt |
| IPC_INTR_STRUCT6_INTR_SET | 0x402210C4 | FULL | Interrupt set |
| IPC_INTR_STRUCT6_INTR_MASK | 0x402210C8 | FULL | Interrupt mask |
| IPC_INTR_STRUCT6_INTR_MASKED | 0x402210CC | FULL | Interrupt masked |

17.16 INTR_STRUCT 7

| Register Name | Address | Permission | Description |
|--|------------|------------|------------------|
| IPC_INTR_STRUCT7_INTR | 0x402210E0 | FULL | Interrupt |
| IPC_INTR_STRUCT7_INTR_SET | 0x402210E4 | FULL | Interrupt set |
| IPC_INTR_STRUCT7_INTR_MASK | 0x402210E8 | FULL | Interrupt mask |
| IPC_INTR_STRUCT7_INTR_MASKED | 0x402210EC | FULL | Interrupt masked |

17.17 Register Details

17.17.1 STRUCT

17.17.1.1 IPC_STRUCT_ACQUIRE

Description: IPC acquire
Address: 0x40220000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register is used to acquire a lock.

A non test controller (the master identifier of the access is NOT '15') read access attempts to acquire a lock. This read access will return the result of the attempt as well as parameters of the master which successfully acquired the lock.

A test controller (the master identifier of the access is '15') read access returns value of LOCK_STATUS. A test controller write access attempts to acquire a lock (the write data value is ignored and does not matter). A separate LOCK_STATUS read access is required to return the result of the attempt.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|----|------------|----|----------|---------|
| Name | PC [7:4] | | | | None [3:2] | | NS [1:1] | P [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | MS [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SUCCESS [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | P | R | W | Undefined | User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the access that successfully acquired the lock. |
| 1 | NS | R | W | Undefined | Secure/non-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the access that successfully acquired the lock. |
| 4:7 | PC | R | W | Undefined | This field specifies the protection context that successfully acquired the lock. |
| 8:11 | MS | R | W | Undefined | This field specifies the bus master identifier that successfully acquired the lock. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 31 | SUCCESS | R | RW | 0 | <p>Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED):</p> <p>'0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuiRED the lock; the fields are NOT affected by the current access.</p> <p>'1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access.</p> <p>Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value).</p> |

17.17.1.2 IPC_STRUCT_RELEASE

Description: IPC release
Address: 0x40220004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register is used to release a lock.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | INTR_RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | INTR_RELEASE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:15 | INTR_RELEASE | W | | 0 | <p>Writing this field releases a lock and allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'.</p> <p>SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field.</p> |

17.17.1.3 IPC_STRUCT_NOTIFY

Description: IPC notification
Address: 0x40220008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | INTR_NOTIFY [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|----|----|----|----|----|---|---|
| Name | INTR_NOTIFY [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:15 | INTR_NOTIFY | W | | 0 | <p>This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'.</p> <p>SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field.</p> |

17.17.1.4 IPC_STRUCT_DATA0

Description: IPC data 0
Address: 0x4022000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | DATA | RW | | Undefined | This field holds a 32-bit data element that is associated with the IPC structure. |

17.17.1.5 IPC_STRUCT_DATA1

Description: IPC data 1
Address: 0x40220010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | DATA [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | DATA | RW | | Undefined | This field holds a 32-bit data element that is associated with the IPC structure. |

17.17.1.6 IPC_STRUCT_LOCK_STATUS

Description: IPC lock status
Address: 0x4022001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------|----|----|------------|----|----------|---------|
| Name | PC [7:4] | | | | None [3:2] | | NS [1:1] | P [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | MS [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ACQUIRED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0 | P | R | W | Undefined | This field specifies the user/privileged access control: '0': user mode. '1': privileged mode. |
| 1 | NS | R | W | Undefined | This field specifies the secure/non-secure access control: '0': secure. '1': non-secure. |
| 4:7 | PC | R | W | Undefined | This field specifies the protection context that successfully acquired the lock. |
| 8:11 | MS | R | W | Undefined | This field specifies the bus master identifier that successfully acquired the lock. |
| 31 | ACQUIRED | R | R | 0 | Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). If zero, P, NS, PC, and MS are not valid. |

17.17.2 INTR_STRUCT

17.17.2.1 IPC_INTR_STRUCT_INTR

Description: Interrupt
Address: 0x40221000
Offset: 0x0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | RELEASE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | RELEASE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | NOTIFY [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | NOTIFY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|------|------|-----------------|--|
| 0:15 | RELEASE | RW1C | RW1S | 0 | These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. |
| 16:31 | NOTIFY | RW1C | RW1S | 0 | These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. |

17.17.2.2 IPC_INTR_STRUCT_INTR_SET

Description: Interrupt set
Address: 0x40221004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register. For debug purposes, SW can write a '1' to activate a specific interrupt cause (this allows for debug of the SW ISR, without relying on HW to activate the interrupt cause).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | RELEASE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | RELEASE [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | NOTIFY [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | NOTIFY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|------|----|-----------------|--|
| 0:15 | RELEASE | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |
| 16:31 | NOTIFY | RW1S | A | 0 | SW writes a '1' to this field to set the corresponding field in the INTR register. |

17.17.2.3 IPC_INTR_STRUCT_INTR_MASK

Description: Interrupt mask
Address: 0x40221008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | RELEASE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | NOTIFY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | NOTIFY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|--|
| 0:15 | RELEASE | RW | R | 0 | Mask bit for corresponding field in the INTR register. |
| 16:31 | NOTIFY | RW | R | 0 | Mask bit for corresponding field in the INTR register. |

17.17.2.4 IPC_INTR_STRUCT_INTR_MASKED

Description: Interrupt masked
Address: 0x4022100C
Offset: 0xC
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects 'a bitwise AND' between the INTR and INTR_MASK registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | RELEASE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | RELEASE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | NOTIFY [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | NOTIFY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|---|
| 0:15 | RELEASE | R | W | 0 | Logical and of corresponding request and mask bits. |
| 16:31 | NOTIFY | R | W | 0 | Logical and of corresponding INTR and INTR_MASK fields. |

18 LIN

Description LIN
Base Address 0x40500000
Size 0x10000
Slave Num MMIO5 - 0

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| LIN0_ERROR_CTL | 0x40500000 | FULL | Error control |
| LIN0_TEST_CTL | 0x40500004 | FULL | Test control |

18.1 CH 0

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LIN0_CH0_CTL0 | 0x40508000 | FULL | Control 0 |
| LIN0_CH0_CTL1 | 0x40508004 | FULL | Control 1 |
| LIN0_CH0_STATUS | 0x40508008 | FULL | Status |
| LIN0_CH0_CMD | 0x40508010 | FULL | Command |
| LIN0_CH0_TX_RX_STATUS | 0x40508060 | FULL | TX/RX status |
| LIN0_CH0_PID_CHECKSUM | 0x40508080 | FULL | PID and checksum |
| LIN0_CH0_DATA0 | 0x40508084 | FULL | Response data 0 |
| LIN0_CH0_DATA1 | 0x40508088 | FULL | Response data 1 |
| LIN0_CH0_INTR | 0x405080C0 | FULL | Interrupt |
| LIN0_CH0_INTR_SET | 0x405080C4 | FULL | Interrupt set |
| LIN0_CH0_INTR_MASK | 0x405080C8 | FULL | Interrupt mask |
| LIN0_CH0_INTR_MASKED | 0x405080CC | FULL | Interrupt masked |

18.2 CH 1

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LIN0_CH1_CTL0 | 0x40508100 | FULL | Control 0 |
| LIN0_CH1_CTL1 | 0x40508104 | FULL | Control 1 |
| LIN0_CH1_STATUS | 0x40508108 | FULL | Status |
| LIN0_CH1_CMD | 0x40508110 | FULL | Command |
| LIN0_CH1_TX_RX_STATUS | 0x40508160 | FULL | TX/RX status |
| LIN0_CH1_PID_CHECKSUM | 0x40508180 | FULL | PID and checksum |
| LIN0_CH1_DATA0 | 0x40508184 | FULL | Response data 0 |
| LIN0_CH1_DATA1 | 0x40508188 | FULL | Response data 1 |
| LIN0_CH1_INTR | 0x405081C0 | FULL | Interrupt |
| LIN0_CH1_INTR_SET | 0x405081C4 | FULL | Interrupt set |
| LIN0_CH1_INTR_MASK | 0x405081C8 | FULL | Interrupt mask |
| LIN0_CH1_INTR_MASKED | 0x405081CC | FULL | Interrupt masked |

18.3 CH 2

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LIN0_CH2_CTL0 | 0x40508200 | FULL | Control 0 |
| LIN0_CH2_CTL1 | 0x40508204 | FULL | Control 1 |
| LIN0_CH2_STATUS | 0x40508208 | FULL | Status |
| LIN0_CH2_CMD | 0x40508210 | FULL | Command |
| LIN0_CH2_TX_RX_STATUS | 0x40508260 | FULL | TX/RX status |
| LIN0_CH2_PID_CHECKSUM | 0x40508280 | FULL | PID and checksum |
| LIN0_CH2_DATA0 | 0x40508284 | FULL | Response data 0 |
| LIN0_CH2_DATA1 | 0x40508288 | FULL | Response data 1 |
| LIN0_CH2_INTR | 0x405082C0 | FULL | Interrupt |
| LIN0_CH2_INTR_SET | 0x405082C4 | FULL | Interrupt set |
| LIN0_CH2_INTR_MASK | 0x405082C8 | FULL | Interrupt mask |
| LIN0_CH2_INTR_MASKED | 0x405082CC | FULL | Interrupt masked |

18.4 CH 3

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|-------------|
| LIN0_CH3_CTL0 | 0x40508300 | FULL | Control 0 |
| LIN0_CH3_CTL1 | 0x40508304 | FULL | Control 1 |
| LIN0_CH3_STATUS | 0x40508308 | FULL | Status |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH3_CMD | 0x40508310 | FULL | Command |
| LINO_CH3_TX_RX_STATUS | 0x40508360 | FULL | TX/RX status |
| LINO_CH3_PID_CHECKSUM | 0x40508380 | FULL | PID and checksum |
| LINO_CH3_DATA0 | 0x40508384 | FULL | Response data 0 |
| LINO_CH3_DATA1 | 0x40508388 | FULL | Response data 1 |
| LINO_CH3_INTR | 0x405083C0 | FULL | Interrupt |
| LINO_CH3_INTR_SET | 0x405083C4 | FULL | Interrupt set |
| LINO_CH3_INTR_MASK | 0x405083C8 | FULL | Interrupt mask |
| LINO_CH3_INTR_MASKED | 0x405083CC | FULL | Interrupt masked |

18.5 CH 4

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH4_CTL0 | 0x40508400 | FULL | Control 0 |
| LINO_CH4_CTL1 | 0x40508404 | FULL | Control 1 |
| LINO_CH4_STATUS | 0x40508408 | FULL | Status |
| LINO_CH4_CMD | 0x40508410 | FULL | Command |
| LINO_CH4_TX_RX_STATUS | 0x40508460 | FULL | TX/RX status |
| LINO_CH4_PID_CHECKSUM | 0x40508480 | FULL | PID and checksum |
| LINO_CH4_DATA0 | 0x40508484 | FULL | Response data 0 |
| LINO_CH4_DATA1 | 0x40508488 | FULL | Response data 1 |
| LINO_CH4_INTR | 0x405084C0 | FULL | Interrupt |
| LINO_CH4_INTR_SET | 0x405084C4 | FULL | Interrupt set |
| LINO_CH4_INTR_MASK | 0x405084C8 | FULL | Interrupt mask |
| LINO_CH4_INTR_MASKED | 0x405084CC | FULL | Interrupt masked |

18.6 CH 5

This instance is not available in the following part numbers:

CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE, CYT2BL4BAS, CYT2BL4BAE, CYT2BL4CAS, CYT2BL4CAE, CYT2BL5BAS, CYT2BL5BAE, CYT2BL5CAS, CYT2BL5CAE.

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH5_CTL0 | 0x40508500 | FULL | Control 0 |
| LINO_CH5_CTL1 | 0x40508504 | FULL | Control 1 |
| LINO_CH5_STATUS | 0x40508508 | FULL | Status |
| LINO_CH5_CMD | 0x40508510 | FULL | Command |
| LINO_CH5_TX_RX_STATUS | 0x40508560 | FULL | TX/RX status |
| LINO_CH5_PID_CHECKSUM | 0x40508580 | FULL | PID and checksum |
| LINO_CH5_DATA0 | 0x40508584 | FULL | Response data 0 |
| LINO_CH5_DATA1 | 0x40508588 | FULL | Response data 1 |
| LINO_CH5_INTR | 0x405085C0 | FULL | Interrupt |
| LINO_CH5_INTR_SET | 0x405085C4 | FULL | Interrupt set |
| LINO_CH5_INTR_MASK | 0x405085C8 | FULL | Interrupt mask |
| LINO_CH5_INTR_MASKED | 0x405085CC | FULL | Interrupt masked |

18.7 CH 6

This instance is not available in the following part numbers:

CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE.

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH6_CTL0 | 0x40508600 | FULL | Control 0 |
| LINO_CH6_CTL1 | 0x40508604 | FULL | Control 1 |
| LINO_CH6_STATUS | 0x40508608 | FULL | Status |
| LINO_CH6_CMD | 0x40508610 | FULL | Command |
| LINO_CH6_TX_RX_STATUS | 0x40508660 | FULL | TX/RX status |
| LINO_CH6_PID_CHECKSUM | 0x40508680 | FULL | PID and checksum |
| LINO_CH6_DATA0 | 0x40508684 | FULL | Response data 0 |
| LINO_CH6_DATA1 | 0x40508688 | FULL | Response data 1 |
| LINO_CH6_INTR | 0x405086C0 | FULL | Interrupt |
| LINO_CH6_INTR_SET | 0x405086C4 | FULL | Interrupt set |
| LINO_CH6_INTR_MASK | 0x405086C8 | FULL | Interrupt mask |
| LINO_CH6_INTR_MASKED | 0x405086CC | FULL | Interrupt masked |

18.8 CH 7

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH7_CTL0 | 0x40508700 | FULL | Control 0 |
| LINO_CH7_CTL1 | 0x40508704 | FULL | Control 1 |
| LINO_CH7_STATUS | 0x40508708 | FULL | Status |
| LINO_CH7_CMD | 0x40508710 | FULL | Command |
| LINO_CH7_TX_RX_STATUS | 0x40508760 | FULL | TX/RX status |
| LINO_CH7_PID_CHECKSUM | 0x40508780 | FULL | PID and checksum |
| LINO_CH7_DATA0 | 0x40508784 | FULL | Response data 0 |
| LINO_CH7_DATA1 | 0x40508788 | FULL | Response data 1 |
| LINO_CH7_INTR | 0x405087C0 | FULL | Interrupt |
| LINO_CH7_INTR_SET | 0x405087C4 | FULL | Interrupt set |
| LINO_CH7_INTR_MASK | 0x405087C8 | FULL | Interrupt mask |
| LINO_CH7_INTR_MASKED | 0x405087CC | FULL | Interrupt masked |

18.9 CH 8

This instance is not available in the following part numbers:
CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE.

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH8_CTL0 | 0x40508800 | FULL | Control 0 |
| LINO_CH8_CTL1 | 0x40508804 | FULL | Control 1 |
| LINO_CH8_STATUS | 0x40508808 | FULL | Status |
| LINO_CH8_CMD | 0x40508810 | FULL | Command |
| LINO_CH8_TX_RX_STATUS | 0x40508860 | FULL | TX/RX status |
| LINO_CH8_PID_CHECKSUM | 0x40508880 | FULL | PID and checksum |
| LINO_CH8_DATA0 | 0x40508884 | FULL | Response data 0 |
| LINO_CH8_DATA1 | 0x40508888 | FULL | Response data 1 |
| LINO_CH8_INTR | 0x405088C0 | FULL | Interrupt |
| LINO_CH8_INTR_SET | 0x405088C4 | FULL | Interrupt set |
| LINO_CH8_INTR_MASK | 0x405088C8 | FULL | Interrupt mask |
| LINO_CH8_INTR_MASKED | 0x405088CC | FULL | Interrupt masked |

18.10 CH 9

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|------------------|
| LINO_CH9_CTL0 | 0x40508900 | FULL | Control 0 |
| LINO_CH9_CTL1 | 0x40508904 | FULL | Control 1 |
| LINO_CH9_STATUS | 0x40508908 | FULL | Status |
| LINO_CH9_CMD | 0x40508910 | FULL | Command |
| LINO_CH9_TX_RX_STATUS | 0x40508960 | FULL | TX/RX status |
| LINO_CH9_PID_CHECKSUM | 0x40508980 | FULL | PID and checksum |
| LINO_CH9_DATA0 | 0x40508984 | FULL | Response data 0 |
| LINO_CH9_DATA1 | 0x40508988 | FULL | Response data 1 |
| LINO_CH9_INTR | 0x405089C0 | FULL | Interrupt |
| LINO_CH9_INTR_SET | 0x405089C4 | FULL | Interrupt set |
| LINO_CH9_INTR_MASK | 0x405089C8 | FULL | Interrupt mask |
| LINO_CH9_INTR_MASKED | 0x405089CC | FULL | Interrupt masked |

18.11 CH 10

This instance is not available in the following part numbers:
CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE, CYT2BL4BAS, CYT2BL4BAE, CYT2BL4CAS, CYT2BL4CAE, CYT2BL5BAS, CYT2BL5BAE, CYT2BL5CAS, CYT2BL5CAE.

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|------------------|
| LINO_CH10_CTL0 | 0x40508A00 | FULL | Control 0 |
| LINO_CH10_CTL1 | 0x40508A04 | FULL | Control 1 |
| LINO_CH10_STATUS | 0x40508A08 | FULL | Status |
| LINO_CH10_CMD | 0x40508A10 | FULL | Command |
| LINO_CH10_TX_RX_STATUS | 0x40508A60 | FULL | TX/RX status |
| LINO_CH10_PID_CHECKSUM | 0x40508A80 | FULL | PID and checksum |
| LINO_CH10_DATA0 | 0x40508A84 | FULL | Response data 0 |
| LINO_CH10_DATA1 | 0x40508A88 | FULL | Response data 1 |
| LINO_CH10_INTR | 0x40508AC0 | FULL | Interrupt |
| LINO_CH10_INTR_SET | 0x40508AC4 | FULL | Interrupt set |
| LINO_CH10_INTR_MASK | 0x40508AC8 | FULL | Interrupt mask |
| LINO_CH10_INTR_MASKED | 0x40508ACC | FULL | Interrupt masked |

18.12 CH 11

This instance is not available in the following part numbers:

CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE, CYT2BL4BAS, CYT2BL4BAE, CYT2BL4CAS, CYT2BL4CAE, CYT2BL5BAS, CYT2BL5BAE, CYT2BL5CAS, CYT2BL5CAE.

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|------------------|
| LINO_CH11_CTL0 | 0x40508B00 | FULL | Control 0 |
| LINO_CH11_CTL1 | 0x40508B04 | FULL | Control 1 |
| LINO_CH11_STATUS | 0x40508B08 | FULL | Status |
| LINO_CH11_CMD | 0x40508B10 | FULL | Command |
| LINO_CH11_TX_RX_STATUS | 0x40508B60 | FULL | TX/RX status |
| LINO_CH11_PID_CHECKSUM | 0x40508B80 | FULL | PID and checksum |
| LINO_CH11_DATA0 | 0x40508B84 | FULL | Response data 0 |
| LINO_CH11_DATA1 | 0x40508B88 | FULL | Response data 1 |
| LINO_CH11_INTR | 0x40508BC0 | FULL | Interrupt |
| LINO_CH11_INTR_SET | 0x40508BC4 | FULL | Interrupt set |
| LINO_CH11_INTR_MASK | 0x40508BC8 | FULL | Interrupt mask |
| LINO_CH11_INTR_MASKED | 0x40508BCC | FULL | Interrupt masked |

18.13 Register Details

18.13.1 LIN_ERROR_CTL

Description: Error control

Address: 0x40500000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: This register supports error functionality: it enables HW injected channel transmitter errors. The receiver should detect these errors and report these errors through activation of corresponding interrupt causes.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------|---|---|---|---|
| Name | None [7:5] | | | CH_IDX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---|----------------------------------|--------------------------------------|-----------------|--------------------------------------|--------------------------------|--------------------------------------|------------------------------|
| Name | TX_CHECKS UM_STOP _ERROR [23:23] | TX_CHECKS UM_ERROR [22:22] | TX_DATA STOP _ERROR [21:21] | None [20:20] | TX_PID_ST OP _ERROR [19:19] | TX_PARITY _ERROR [18:18] | TX_SYNC STOP _ERROR [17:17] | TX_SYNC _ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|--------------|----|----|----|----|----|----|
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|----|----|-----------------|---|
| 0:4 | CH_IDX | RW | R | 0 | Specifies the channel index of the channel to which HW injected channel transmitter errors applies. |
| 16 | TX_SYNC_ERROR | RW | R | 0 | The synchronization field is changed from 0x55 to 0x00. At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR activation. |
| 17 | TX_SYNC_STOP_ERROR | RW | R | 0 | The synchronization field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_HEADER_SYNC_ERROR or INTR.RX_HEADER_FRAME_ERROR activation. |
| 18 | TX_PARITY_ERROR | RW | R | 0 | In LIN mode, the PID parity bit P[1] is inverted from $!(ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[1])$ to $(ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[1])$. At the receiver, this should result in INTR.RX_HEADER_PARITY_ERROR activation. In UART mode, a data field's parity bit is inverted. |
| 19 | TX_PID_STOP_ERROR | RW | R | 0 | The PID field STOP bits are inverted to '0'. At the receiver, this should result in INTR.RX_HEADER_FRAME_ERROR activation. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|----|----|-----------------|---|
| 21 | TX_DATA_STOP_ERROR | RW | R | 0 | <p>The data field STOP bits are inverted to '0'.</p> <p>At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation.</p> <p>Note: Used in UART mode.</p> |
| 22 | TX_CHECKSUM_ERROR | RW | R | 0 | <p>The checksum field is inverted.</p> <p>At the receiver, this should result in INTR.RX_RESPONSE_CHECKSUM_ERROR activation.</p> |
| 23 | TX_CHECKSUM_STOP_ERROR | RW | R | 0 | <p>The checksum field STOP bits are inverted to '0'.</p> <p>At the receiver, this should result in INTR.RX_RESPONSE_FRAME_ERROR activation.</p> |
| 31 | ENABLED | RW | R | 0 | <p>Error injection enable:</p> <p>'0': Disabled.</p> <p>'1': Enabled.</p> |

18.13.2 LIN_TEST_CTL

Description: Test control
Address: 0x40500004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register support test functionality.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|--------------|----|----|----|--------------|
| Name | None [7:5] | | | CH_IDX [4:0] | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:17] | | | | | | | MODE [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:4 | CH_IDX | RW | R | 0 | <p>Specifies the channel index of the channel to which test applies. The channel IO signals of channel indices CH_IDX and CH_NR-1 are connected as specified by MODE. CH_IDX should be in the range [0, CH_NR-2], as channel index CH_NR-1 is always involved in test and cannot be connected to itself. The test mode allows BOTH of the two connected channels to be tested.</p> <p>Note: this testing functionality simplifies SW development, but may also be used in the field to verify correct channel functionality.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 16 | MODE | RW | R | 0 | <p>Test mode:</p> <p>'0': Partial disconnect from IOSS. This mode's isolation allows for device test without relying on an external LIN transceiver. The IOSS 'tx' IO cell can be used to observe messages outside of the device.</p> <ul style="list-style-type: none"> - tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX]. - rx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS lin_tx_in[CH_IDX]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. <p>'1': Full disconnect from IOSS (the IOSS/HSIOM should disconnect 'tx_out' from the 'tx' IO cell). This mode's isolation allows for device test without effecting an operational LIN cluster.</p> <ul style="list-style-type: none"> - tx_in[CH_IDX] = lin_tx_out[CH_IDX]. - tx_in[CH_NR-1] = lin_tx_out[CH_IDX]. - rx_in[CH_IDX] = lin_tx_out[CH_IDX]. - rx_in[CH_NR-1] = lin_tx_out[CH_IDX]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX] & tx_out[CH_NR-1]. - lin_tx_out[CH_NR-1] = tx_out[CH_IDX] & tx_out[CH_NR-1]. |
| 31 | ENABLED | RW | R | 0 | <p>Test enable:</p> <p>'0': Disabled. Functional mode.</p> <ul style="list-style-type: none"> - tx_in[CH_IDX] = IOSS lin_tx_in[CH_IDX]. - tx_in[CH_NR-1] = IOSS lin_tx_in[CH_NR-1]. - rx_in[CH_IDX] = IOSS lin_rx_in[CH_IDX]. - rx_in[CH_NR-1] = IOSS lin_rx_in[CH_NR-1]. - lin_tx_out[CH_IDX] = tx_out[CH_IDX]. - lin_tx_out[CH_NR-1] = tx_out[CH_NR-1]. <p>'1': Enabled. Test mode, specific test mode is specified by MODE.</p> |

18.13.3 CH

18.13.3.1 LIN_CH_CTL0

Description: Control 0
Address: 0x40508000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x400C0101

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---------------|------------|---|-----------------|---|
| Name | None [7:5] | | | AUTO_EN [4:4] | None [3:2] | | STOP_BITS [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|-------------------------------|---|
| Name | None [15:10] | | | | | | BREAK_DELIMITER_LEN GTH [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-----------------------------|----|----|----|----|
| Name | None [23:21] | | | BREAK_WAKEUP_LENGTH [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|-------------------|-------------------|----------------|--------------------------|--------------|----|--------------|
| Name | ENABLED [31:31] | FILTER_EN [30:30] | PARITY_EN [29:29] | PARITY [28:28] | BIT_ERROR_IGNORE [27:27] | None [26:25] | | MODE [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:1 | STOP_BITS | RW | R | 1 | <p>STOP bit periods: '0': 1/2 bit period. '1': 1 bit period. '2': 1 1/2 bit period. '3': 2 bit periods.</p> <p>In LIN mode, this field should be set to '1' (the default value) .</p> <p>In UART mode, this field can be programmed as desired.</p> <p>Note: receiver STOP bit frame errors can only be detected if the number of STOP bit periods is 1 or more bit period.</p> |
| 4 | AUTO_EN | RW | R | 0 | <p>LIN transceiver auto enable: '0': Disabled. '1': Enabled. The TX_RX_STATUS.EN_OUT field is controlled by HW.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------------------|----|----|-----------------|---|
| 8:9 | BREAK_DELIMITER_LEN GTH | RW | R | 1 | <p>In LIN mode, this field specifies the break delimiter length: (used in header transmission, not used in header reception). '0': 1 bit period. '1': 2 bit periods (default value). '2': 3 bit periods. '3': 4 bit periods.</p> <p>In UART mode, this field specifies the data field size: '0': 5 bit data field. '1': 6 bit data field. '2': 7 bit data field. '3': 8 bit data field. When the data field size is less than 8 bits, the most significant (unused) bits of the DATAx.DATAy[7:0] fields should be set to '0' for the transmitter.</p> |
| 16:20 | BREAK_WAKEUP _LENGTH | RW | R | 12 | <p>Break/wakeup length (minus 1) in bit periods: '0': 1 bit period. ... '10': 11 bit periods (break length for slave nodes) ... '12': 13 bit periods (break length for master nodes) ... '30': 31 bit periods. '31': Illegal (should NOT be used!!!)</p> <p>This field is used for transmission/reception of BOTH break and wakeup signals. Note that these functions are mutually exclusive: - When CMD.TX_HEADER is '1', the field specifies the transmitted break field. - When CMD.TX_WAKEUP is '1', the field specifies the transmitted wakeup field. - When CMD.RX_HEADER is '1', the field specifies the to be received break field. - Otherwise, the field specifies the to be received wakeup field.</p> <p>Per the standard, the master wakeup duration is between 250 us and 5 ms. To support uncalibrated slaves, a slave has a detection threshold of 150 us (3 bit periods at 20 kbps). After transmission of a break or wakeup signal, the INTR.TX_BREAK_WAKEUP_DONE interrupt cause is activated. After reception of a wakeup signal, the INTR.RX_BREAK_WAKEUP_DONE interrupt cause is activated.</p> <p>To specify longer wakeup signals in terms of absolute time (us/ms rather than bit periods), the associated PERI clock divider value can be (temporarily) increased to make the LIN bit period longer.</p> <p>Note: entering bus sleep mode is achieved with the 'go-to-sleep' command.</p> |
| 24 | MODE | RW | R | 0 | <p>Mode of operation: '0': LIN mode. '1': UART mode.</p> |
| | LIN | | | 0 | LIN mode. |
| | UART | | | 1 | UART mode. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 27 | BIT_ERROR_IGNORE | RW | R | 0 | <p>Specifies behavior on a detected bit error during header or response transmission:</p> <p>'0': Message transfer is aborted.</p> <p>'1': Message transfer is NOT aborted.</p> <p>Note: this field does NOT effect the reporting of the bit error through INTR/STATUS.TX_HEADER/RESPONSE_BIT_ERROR; i.e. bit errors are always reported.</p> |
| 28 | PARITY | RW | R | 0 | <p>Parity mode:</p> <p>'0': Even parity: even number of '1' bits (including parity).</p> <p>'1': Odd parity.</p> <p>Note: Used in UART mode only.</p> |
| 29 | PARITY_EN | RW | R | 0 | <p>Parity generation enable:</p> <p>'0': Disabled. No parity bit is transferred.</p> <p>'1': Enabled. The parity bit is transferred after the last (most significant) data field bit.</p> <p>Note: Used in UART mode only.</p> |
| 30 | FILTER_EN | RW | R | 1 | <p>RX filter (for 'lin_rx_in'):</p> <p>'0': No filter.</p> <p>'1': Median 3 (default value) operates on the last three 'lin_rx_in' values. The sequences '000', '001', '010' and '100' result in a filtered value '0'. The sequences '111', '110', '101' and '011' result in a filtered value '1'.</p> |
| 31 | ENABLED | RW | R | 0 | <p>Channel enable:</p> <p>'0': Disabled. If a channel is disabled, all non-retained MMIO registers (e.g. the TX_RX_STATUS, and INTR registers) have their fields reset to their default value.</p> <p>'1': Enabled.</p> |

18.13.3.2 LIN_CH_CTL1

Description: Control 1
Address: 0x40508004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: A master node is aware of a message's checksum mode and number of data fields. Therefore, a master node can set the CHECKSUM_ENHANCED and DATA_NR fields accordingly, BEFORE the message header transmission.

A slave node needs to derive a message's checksum mode and number of data fields from the received PID field, AFTER the message header reception. The INTR.RX_HEADER_DONE interrupt cause indicates that the message header is received and PID_CHECKSUM.PID contains the received PID field. Slave node SW can use this PID field information to set CHECKSUM_ENHANCED and DATA_NR fields accordingly. A minimum message response consists of at least 1 data field, and the CHECKSUM_ENHANCED and DATA_NR fields need to be set BEFORE the receipt of the STOP bit(s) of the first data field; i.e. SW effectively has a data field transfer duration to set the fields.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---------------|---|---|
| Name | None [7:3] | | | | | DATA_NR [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-------------------------------|
| Name | None [15:9] | | | | | | | CHECKSUM ENHANCED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------------|----|----|----|----|----|----|----|
| Name | FRAME_TIMEOUT [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|------------------------------|----|
| Name | None [31:26] | | | | | | FRAME_TIMEOUT_SEL [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:2 | DATA_NR | RW | R | Undefined | <p>Number of data fields (minus 1) in the response (not including the checksum):</p> <p>'0': 1 data field.</p> <p>'1': 2 data fields.</p> <p>...</p> <p>'7': 8 data fields.</p> <p>Note: master and slave nodes need to agree upon the number of data fields before message transfer. In RX_RESPONSE case, When PID (header) is received, firmware has the time of one response data byte, to modify CTL1.DATA_NR.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|---|
| 8 | CHECKSUM_ENHANCED | RW | R | Undefined | <p>Checksum mode:</p> <p>'0': Classic mode. PID field is NOT included in the checksum calculation.</p> <p>'1': Enhanced mode. PID field is included in the checksum calculation. This mode requires special attention when the master node transmits the header and a (different) slave node transmits the response: the slave node will use the calculated partial checksum over the received PID field as a starting point for the calculation over the to be transmitted data fields.</p> <p>Note: If the frame identifier ID[5:0] is 0x3c or 0x3d, the classic mode will ALWAYS be used for transmission and assumed for reception, independent of the CHECKSUM_ENHANCED value.</p> |
| 16:23 | FRAME_TIMEOUT | RW | R | Undefined | <p>Specifies the maximum allowed length (timeout value) for a frame, frame header or frame response in bit periods. The LIN specification prescribes to set the maximum length to 1.4x the nominal length (Theader_max = 1.4 x Theader_nom and Tresponse_max = 1.4 x Tresponse_nom). The nominal header length Theader_nom is 34 bit periods and the nominal response length Tresponse_nom is 10 * (data_nr + 1) bit periods (data_nr is the number of data fields)</p> <p>Note: the LIN specification specifies the following: 'Tools and tests shall check the Tframe_max (= Theader_max + Tresponse_max). Nodes shall not check this time. The receiving node of the frame shall accept the frame up to the next frame slot (i.e. next break field), even if it is longer then Tframe_max).'</p> |
| 24:25 | FRAME_TIMEOUT_SEL | RW | R | 0 | <p>Specifies the frame timeout mode:</p> <p>'0': No timeout functionality (default value).</p> <p>'1': Frame mode: detects timeout from the start of break field to checksum field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34+20 bit periods (header and a response with 1 data field).</p> <p>'2': Frame header mode: detects timeout from the start of break field to PID field STOP bits (inclusive). The minimum FRAME_TIMEOUT value is 34 bit periods (header).</p> <p>'3': Frame response mode: detects timeout from the PID field STOP bits (exclusive) to checksum field STOP bits (the response space is included in the frame response). The minimum FRAME_TIMEOUT value is 20 bit periods (response with 1 data field).</p> |

18.13.3.3 LIN_CH_STATUS

Description: Status
Address: 0x40508008
Offset: 0x8
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

Default: This is a non-retained register; setting CTL.ENABLED to '0' clears all status fields to '0'.
0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|----------------------------|-----------------------|----------------|---|---|---|
| Name | None [7:6] | | RX_DATA0_FRAME_ERROR [5:5] | HEADER_RESPONSE [4:4] | DATA_IDX [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|-----------------|-----------------|--------------|----|---------------|---------------|
| Name | None [15:14] | | RX_DONE [13:13] | TX_DONE [12:12] | None [11:10] | | RX_BUSY [9:9] | TX_BUSY [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------------------------|-----------------------------|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|------------------------------------|---------------------------------|--------------------------------|------------------------------|-------------------------------|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| 0:3 | DATA_IDX | R | W | 0 | Number of transferred data and checksum fields in the response (also acts as an index/address into response data field and checksum field registers (DATA0, DATA1, PID_CHECKSUM)) : '0': No data fields transferred. '1': Data field 1 transferred. ... '7': Data fields 1, 2, 3, ... and 7 transferred. '8': Data fields 1, 2, 3, ... and 8 transferred. '9': Data fields 1, 2, 3, ..., 8 and checksum field transferred. '10'-'15': Unused. Set to '0' on the start of a TX_HEADER or RX_HEADER command. |
| 4 | HEADER_RESPONSE | R | W | 0 | Frame header / response identifier (only valid when TX_BUSY or RX_BUSY is '1'): '0': Frame header being transferred. '1': Frame response being transferred. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------------|----|----|-----------------|---|
| 5 | RX_DATA0_FRAME_ERROR | R | W | 0 | <p>Frame response, first data field frame error. HW sets this field to '1' when the received STOP bits of the first response data field have an unexpected value (only after a RX_HEADER command), and this data byte is 0x00. HW clears this field to '0' at the falling edge of SYNC start bit (after INTR.RX_HEADER_BREAK_WAKEUP_DONE). This field is used together with INTR.RX_RESPONSE_FRAME_ERROR to distinguish 'no response', 'error response' and 'correct response' scenarios.</p> <p>Note: The ongoing message transfer is NOT aborted.</p> |
| 8 | TX_BUSY | R | W | 0 | <p>Transmitter busy.</p> <ul style="list-style-type: none"> - Set to '1' on the start of the following commands: TX_HEADER, TX_RESPONSE, TX_WAKEUP. - Set to '0' on successful completion of previous commands or when an error is detected. <p>In 'TX_HEADER, RX_RESPONSE' case, set to '0' at the start bit falling edge in the first response data byte, after header transmission</p> |
| 9 | RX_BUSY | R | W | 0 | <p>Receiver busy.</p> <ul style="list-style-type: none"> - Set to '1' on the start of the following commands: RX_HEADER, RX_RESPONSE. <p>in RX_HEADER case, set at Break filed rising edge. in RX_RESPONSE case, set at the start bit falling edge in the first response data byte.</p> <ul style="list-style-type: none"> - Set to '0' on successful completion of previous commands or when an error is detected. |
| 12 | TX_DONE | R | W | 0 | <p>Transmitter done:</p> <ul style="list-style-type: none"> - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble): <ul style="list-style-type: none"> - TX_HEADER. - TX_HEADER, TX_RESPONSE. - RX_HEADER, TX_RESPONSE. - TX_WAKEUP. |
| 13 | RX_DONE | R | W | 0 | <p>Receiver done:</p> <ul style="list-style-type: none"> - Set to '0' on the start of a new command. - Set to '1' on successful completion of the following command sequences (if CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble): <ul style="list-style-type: none"> - RX_HEADER, RX_RESPONSE. - TX_HEADER, RX_RESPONSE. |
| 16 | TX_HEADER_BIT_ERROR | R | W | 0 | Copy of INTR.TX_HEADER_BIT_ERROR. |
| 17 | TX_RESPONSE_BIT_ERROR | R | W | 0 | Copy of INTR.TX_RESPONSE_BIT_ERROR. |
| 24 | RX_HEADER_FRAME_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_FRAME_ERROR. |
| 25 | RX_HEADER_SYNC_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_SYNC_ERROR. |
| 26 | RX_HEADER_PARITY_ERROR | R | W | 0 | Copy of INTR.RX_HEADER_PARITY_ERROR. |
| 27 | RX_RESPONSE_FRAME_ERROR | R | W | 0 | Copy of INTR.RX_RESPONSE_FRAME_ERROR. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------------|----|----|-----------------|--|
| 28 | RX_RESPONSE_CHECKSUM_ERROR | R | W | 0 | Copy of INTR.RX_RESPONSE_CHECKSUM_ERROR. |

18.13.3.4 LIN_CH_CMD

Description: Command
Address: 0x40508010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The register fields are retained. When a LIN channel is disabled (CTL.ENABLED is set to '0'), HW sets all the register fields to '0'.

The following restrictions apply when programming the commands:

- TX_HEADER and RX_HEADER are mutually exclusive; i.e. cannot both be set to '1'.
- TX_WAKEUP is mutually exclusive with all other commands.
- TX_RESPONSE and RX_RESPONSE are NOT mutually exclusive, but are evaluated in the following order (of decreasing priority): TX_RESPONSE, RX_RESPONSE.

The CMD.TX_HEADER register field description provides all legal command sequences.
The break or wakeup detection is always enabled, regardless of CMD register setting.

Note: LIN mode supports all commands, UART mode supports the TX_HEADER and RX_HEADER commands only.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|-------------------|-----------------|
| Name | None [7:3] | | | | | TX_WAKEUP [2:2] | TX_RESPONSE [1:1] | TX_HEADER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|-------------------|-----------------|
| Name | None [15:10] | | | | | | RX_RESPONSE [9:9] | RX_HEADER [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|------|------|-----------------|---|
| 0 | TX_HEADER | RW1S | RW | 0 | <p>SW sets this field to '1' to transmit a header. HW sets this field to '0' on successful completion of ANY of the following legal command sequences (also set to '0' when an error is detected):</p> <ul style="list-style-type: none"> - TX_HEADER - TX_HEADER, TX_RESPONSE. - TX_HEADER, RX_RESPONSE. - RX_HEADER, TX_RESPONSE. - RX_HEADER, RX_RESPONSE. - TX_WAKEUP. <p>The header is transmitted when the PID field STOP bits are transmitted (INTR.TX_HEADER_DONE).</p> <p>HW sets this field to '1', when the 'tr_cmd_tx_header' input trigger is activated. This allows for time triggered LIN message transfer. HW driven time triggered transfer eliminates the jitter that is typically associated with SW driven transfer.</p> <p>In UART mode, a single data field (DATA0.DATA1) is transmitted.</p> |
| 1 | TX_RESPONSE | RW1S | RW1C | 0 | <p>SW sets this field to '1' to transmit a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected).</p> <p>The response is transmitted when the checksum field STOP bits are transmitted (INTR.TX_RESPONSE_DONE).</p> |
| 2 | TX_WAKEUP | RW1S | RW1C | 0 | <p>SW sets this field to '1' to transmit a wakeup signal. HW sets this field to '0' on successful completion of ANY of the legal command sequences (also set to '0' when an error is detected).</p> <p>The command generates CTL.BREAK_WAKEUP_LENGTH bit periods in the dominant state (low/'0') and transitions to the recessive state (high/'1') (INTR.TX_WAKEUP_DONE).</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|------|------|-----------------|---|
| 8 | RX_HEADER | RW1S | RW1C | 0 | <p>SW sets this field to '1' to receive a header. HW sets this field to '0' on successful completion of the ANY of the legal command sequences (NOT set to '0' when an error is detected in LIN mode).</p> <p>The header is received when the PID field STOP bits are received (INTR.RX_HEADER_DONE).</p> <p>Typically, a slave node SW sets both RX_HEADER and RX_RESPONSE to '1', anticipating a transfer of a response from the master node to this slave node. After receipt of the header PID field (INTR.RX_HEADER_PID_DONE is activated), the slave node may decide to set TX_RESPONSE to '1' (which has a higher priority than RX_RESPONSE) to transmit a response.</p> <p>the Break detection is performed regardless of CMD.RX_HEADER. INTR.RX_BREAK_WAKEUP_DONE will trigger at LIN_RX rising edge, when the low pulse meet CTL0.BREAK_WAKEUP_LENGTH. when Break is detected, HW check CMD.RX_HEADER before entering SYNC byte processing state. when RX_HEADER is cleared, SW has at least 11 bit times to set RX_HEADER again, before next Break is detected (RX_BREAK_WAKEUP_DONE). in this case, there is no gap, Break will never be missed.</p> <p>In UART mode, a single data field is received (in DATA0.DATA1). HW set this field to '0' when the data field is received, or when an error is detected.</p> |
| 9 | RX_RESPONSE | RW1S | RW1C | 0 | <p>SW sets this field to '1' to receive a response. HW sets this field to '0' on successful completion of ANY of the legal command sequences (NOT set to '0' when an error is detected).</p> <p>The response is received when the checksum field STOP bits are received (INTR.RX_RESPONSE_DONE).</p> |

18.13.3.5 LIN_CH_TX_RX_STATUS

Description: TX/RX status
Address: 0x40508060
Offset: 0x60
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x5000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----------------|---------------|----------------|
| Name | SYNC_COUNTER [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:18] | | | | | | RX_IN [17:17] | TX_IN [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:27] | | | | | EN_OUT [26:26] | None [25:25] | TX_OUT [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:7 | SYNC_COUNTER | R | W | Undefined | <p>Synchronization counter in LIN channel clock periods. After the receipt of a synchronization field, this fields reflects the duration of the synchronization field. Ideally, SYNC_COUNTER = 8*16 = 128 (the synchronization fields consists of eight bit period of 16 LIN channel clock periods each).</p> <ul style="list-style-type: none"> - If SYNC_COUNTER is less than 128, the LIN channel clock is too slow and the PERI/PCLK divider value should be decreased. - If SYNC_COUNTER is greater than 128, the LIN channel clock is too fast and the PERI/PCLK divider value should be increased. <p>The biggest master-slave clock discrepancy occurs when the master is slow and the slave is fast or vice versa. At a 0.5 percent master inaccuracy and a 14 percent slave inaccuracy, this results in the extreme synchronization values of $(.86 * 128) / 1.005 = 109.5$ and $(1.14 * 128) / 0.995 = 146.6$. We add a little margin for a valid range of [106, 152].</p> <p>Note: Only slave nodes with imprecise clocks require clock resynchronization. Master and slave nodes with precise clocks do NOT require clock resynchronization.</p> |
| 16 | TX_IN | R | W | Undefined | LIN transmitter input ('tx_in', 'lin_tx_in' in functional mode). TX_IN and RX_IN can be used to determine a wakeup source. Note that wakeup source detection relies on the external transceiver functionality. |
| 17 | RX_IN | R | W | Undefined | LIN receiver input ('rx_in', 'lin_rx_in' in functional mode). |
| 24 | TX_OUT | R | W | 1 | LIN transmitter output ('tx_out', 'lin_tx_out'). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 26 | EN_OUT | RW | RW | 1 | <p>LIN transceiver enable ('en_out', 'lin_en_out'). This field controls the enable (or low active sleep enable) of the external transceiver: '0': Disabled. '1': Enabled.</p> <p>If CTL.AUTO_EN is '0', SW controls this field to enable the external transceiver. If CTL.AUTO_EN is '1', HW controls this field to enable the external transceiver: - Before a legal command sequence, HW sets this field to '1', if it is '0'. The start of the command sequence is effectively postponed by a 4-bit period preamble. - After a legal command sequence, HW clears this field to '0'. The end of the command sequence is effectively postponed by a 4-bit period postamble.</p> <p>Note: external transceivers require a 'power up' or 'power down' period of 1 or 2 bit periods, so a 4-bit period suffices for all known transceivers.</p> |

18.13.3.6 LIN_CH_PID_CHECKSUM

Description: PID and checksum
Address: 0x40508080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses.

A LIN header has a single PID field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

A LIN response has a single checksum field. This field is SW accessible through this register. The field is used in BOTH transmit and receive modes.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | PID [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CHECKSUM [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:7 | PID | RW | RW | Undefined | Header protected identifier (PID). - Bits 5 down to 0: frame identifier ID[5:0]. Frame identifier 0x3c is for a 'master request' frame, 0x3d is for a 'slave response' frame, 0x3e and 0x3f are for future LIN enhancements. Frame identifier ID[5:4] is optionally used for length control; i.e. specifies the number of response data fields. - Bits 1 down to 0: parity bits P[1] and P[0]. - $P[1] = \neg (ID[5] \wedge ID[4] \wedge ID[3] \wedge ID[1])$ - $P[0] = (ID[4] \wedge ID[2] \wedge ID[1] \wedge ID[0])$ Transmission: To be transmitted PID field. SW needs to calculate the PID field parity bits P[1] and P[0]. Reception: Received PID field. Slave node SW uses the PID field to determine how to handle the response for a received frame header: TX_RESPONSE or RX_RESPONSE. |
| 8:15 | CHECKSUM | R | RW | Undefined | Checksum. Transmission: HW calculated checksum (SW does not need to calculate the checksum) over the transmitted PID field (optional per CTL.CHECKSUM_ENHANCED) and data fields. Reception: Received checksum. Note that in case of a RX_CHECKSUM_ERROR, SW can use the received PID field and the received data fields to calculate the correct checksum value. |

18.13.3.7 LIN_CH_DATA0

Description: Response data 0

Address: 0x40508084

Offset: 0x84

Retention: Retained

IsDeepSleep: No

Comment: This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.

A LIN response has a maximum of eight data fields. These data fields are SW accessible through the DATA0 and DATA1 registers. These register are used in BOTH transmit and receive modes. If the LIN response is both transmitted and received, the to be transmitted data fields (provided by SW) in this register are overwritten by the received data fields (provided by HW).

Data field DATA1 is the first response data field (first to be transmitted/received). The number of transmitted/received data fields is specified by CTL.DATA_NR.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | DATA1 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | DATA2 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA3 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA4 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---|
| 0:7 | DATA1 | RW | RW | Undefined | Data field 1. Transmission: To be transmitted data field. SW provides data field. Reception: Received data field. SW uses the data field. |
| 8:15 | DATA2 | RW | RW | Undefined | Data field 2. |
| 16:23 | DATA3 | RW | RW | Undefined | Data field 3. |
| 24:31 | DATA4 | RW | RW | Undefined | Data field 4. |

18.13.3.8 LIN_CH_DATA1

Description: Response data 1
Address: 0x40508088
Offset: 0x88
Retention: Retained
IsDeepSleep: No
Comment: This register supports 8-bit, 16-bit and 32-bit accesses. This allows for a single 32-bit access to write or read four data fields.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA5 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA6 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA7 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA8 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|---------------|
| 0:7 | DATA5 | RW | RW | Undefined | Data field 5. |
| 8:15 | DATA6 | RW | RW | Undefined | Data field 6. |
| 16:23 | DATA7 | RW | RW | Undefined | Data field 7. |
| 24:31 | DATA8 | RW | RW | Undefined | Data field 8. |

18.13.3.9 LIN_CH_INTR

Description: Interrupt
Address: 0x405080C0
Offset: 0xC0
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

This is a non-retained register; setting CTL.ENABLED to '0' clears all command fields to '0'.

An activated error interrupt cause aborts an ongoing frame transfer (except for bit errors when CTL.BIT_ERROR_IGNORE is '1').

Note: LIN mode supports all interrupt causes. UART mode supports the RX_NOISE_DETECT, TX_HEADER_BIT_ERROR, RX_HEADER_FRAME_ERROR and RX_HEADER_PARITY_ERROR interrupt causes only.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------------|------------------------|----------------------|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-----------------|-------------------------|--------------|-----------------------------|------------------------------|------------------------|----------------------|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------------------------|-----------------------------|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|------------------------------------|---------------------------------|--------------------------------|------------------------------|-------------------------------|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|------|------|-----------------|---|
| 0 | TX_HEADER_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is transmitted (the CMD.TX_HEADER is completed). Specifically:</p> <ul style="list-style-type: none"> - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer. - When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. <p>Note: used in UART mode.</p> |
| 1 | TX_RESPONSE_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a frame response (data fields and checksum field) is transmitted (the CMD.TX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.</p> |
| 2 | TX_WAKEUP_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a wakeup signal is transmitted (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal.</p> |
| 8 | RX_HEADER_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a frame header (break field, synchronization field and PID field) is received (the CMD.RX_HEADER is completed). Specifically:</p> <ul style="list-style-type: none"> - When followed by CMD.TX_RESPONSE or CMD.RX_RESPONSE, this field is set to '1' after completion of the frame header transfer. - When not followed by a response command, this field is set to '1' after completion of the frame header transfer. If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble. <p>Note: used in UART mode.</p> |
| 9 | RX_RESPONSE_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a frame response (data fields and checksum field) is received (the CMD.RX_RESPONSE is completed). If CTL.AUTO_EN is '1', this includes the 4-bit period external transceiver disable post-amble.</p> <p>Note: activation implies that RX_RESPONSE_FRAME_ERROR and RX_RESPONSE_CHECKSUM_ERROR are not activated during response reception</p> |
| 10 | RX_BREAK_WAKEUP_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a break or wakeup signal is received (per CTL.BREAK_WAKEUP_LENGTH). This cause is activated on a transition from dominant/'0' state to recessive/'1' state; i.e. at the end of the wakeup signal.</p> <p>The break or wakeup detection is always enabled, regardless of CMD register setting.</p> |
| 11 | RX_HEADER_SYNC_DONE | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a synchronization field is received (including trailing STOP bits).</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------------|------|------|-----------------|---|
| 13 | RX_NOISE_DETECT | RW1C | RW1S | 0 | <p>HW sets this field to '1', when isolated '0' or '1' 'in_rx_in' values are observed or when during sampling the last three 'in_rx_in' values do NOT all have the same value. This mismatch is an indication of noise on the LIN line.</p> <p>Note: The ongoing frame transfer is NOT aborted.</p> <p>Note: Used in UART mode.</p> |
| 14 | TIMEOUT | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a frame, frame header or frame response timeout is detected (per CTL.FRAME_TIMEOUT_SEL).</p> <p>Note: The ongoing frame transfer is NOT aborted.</p> |
| 16 | TX_HEADER_BIT_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during header transmission). This specific test allows for delay through the external transceiver. This mismatch is an indication of bus collisions on the LIN line.</p> <p>The match is performed for the Wakeup, Break, SYNC and the PID fields (for the START bit, data Byte and STOP bit).</p> <p>Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> <p>Note: Used in UART mode.</p> |
| 17 | TX_RESPONSE_BIT_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when a transmitted 'lin_tx_out' value does NOT match a received 'lin_rx_in' value (during response transmission).</p> <p>The match is performed for the data fields and the checksum field (for the START bit, data Byte and STOP bit).</p> <p>Note: When CTL.BIT_ERROR_IGNORE is '0', the ongoing message transfer is aborted (INTR.TX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> |
| 24 | RX_HEADER_FRAME_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the received START or STOP bits have an unexpected value (during header reception).</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_HEADER_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> <p>Note: Used in UART mode.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------------|------|------|-----------------|--|
| 25 | RX_HEADER_SYNC_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the received synchronization field is not received within the synchronization counter range [106, 152] (see TX_RX_STATUS.SYNC_COUNTER).</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_HEADER_SYNC_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> |
| 26 | RX_HEADER_PARITY_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the received PID field has a parity error.</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_PID_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> <p>+G119 HW sets this field to '1', when the received data field has a parity error (when CTL0.PARITY_EN is '1').</p> |
| 27 | RX_RESPONSE_FRAME_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the received START or STOP bits have an unexpected value (during response reception). HW does NOT use this field for the STOP bits of the first data field after a RX_HEADER command, if the received data byte is 0x00. (STATUS.RX_DATA0_FRAME_ERROR is used instead).</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> |
| 28 | RX_RESPONSE_CHECKSUM_ERROR | RW1C | RW1S | 0 | <p>HW sets this field to '1', when the calculated checksum over the received PID and data fields is not the same as the received checksum.</p> <p>Note: The ongoing message transfer is aborted (INTR.RX_RESPONSE_DONE is NOT activated) and the TX_HEADER, TX_RESPONSE and TX_WAKEUP commands are set to '0'.</p> |

18.13.3.10 LIN_CH_INTR_SET

Description: Interrupt set
Address: 0x405080C4
Offset: 0xC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the INTR register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------------|------------------------|----------------------|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-----------------|-------------------------|--------------|-----------------------------|------------------------------|------------------------|----------------------|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------------------------|-----------------------------|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|------------------------------------|---------------------------------|--------------------------------|------------------------------|-------------------------------|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|------|----|-----------------|---|
| 0 | TX_HEADER_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 1 | TX_RESPONSE_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 2 | TX_WAKEUP_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 8 | RX_HEADER_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 9 | RX_RESPONSE_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 10 | RX_BREAK_WAKEUP_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 11 | RX_HEADER_SYNC_DONE | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 13 | RX_NOISE_DETECT | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 14 | TIMEOUT | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------------|------|----|-----------------|---|
| 16 | TX_HEADER_BIT_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 17 | TX_RESPONSE_BIT_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 24 | RX_HEADER_FRAME_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 25 | RX_HEADER_SYNC_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 26 | RX_HEADER_PARITY_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 27 | RX_RESPONSE_FRAME_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |
| 28 | RX_RESPONSE_CHECKSUM_ERROR | RW1S | A | 0 | Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). |

18.13.3.11 LIN_CH_INTR_MASK

Description: Interrupt mask
Address: 0x405080C8
Offset: 0xC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------------|------------------------|----------------------|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-----------------|-------------------------|--------------|-----------------------------|------------------------------|------------------------|----------------------|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------------------------|-----------------------------|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|------------------------------------|---------------------------------|--------------------------------|------------------------------|-------------------------------|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------------|----|----|-----------------|--|
| 0 | TX_HEADER_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 1 | TX_RESPONSE_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 2 | TX_WAKEUP_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 8 | RX_HEADER_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 9 | RX_RESPONSE_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 10 | RX_BREAK_WAKEUP_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 11 | RX_HEADER_SYNC_DONE | RW | R | 0 | Mask for corresponding field in INTR register. |
| 13 | RX_NOISE_DETECT | RW | R | 0 | Mask for corresponding field in INTR register. |
| 14 | TIMEOUT | RW | R | 0 | Mask for corresponding field in INTR register. |
| 16 | TX_HEADER_BIT_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 17 | TX_RESPONSE_BIT_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 24 | RX_HEADER_FRAME_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------------|----|----|-----------------|--|
| 25 | RX_HEADER_SYNC_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 26 | RX_HEADER_PARITY_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 27 | RX_RESPONSE_FRAME_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |
| 28 | RX_RESPONSE_CHECKSUM_ERROR | RW | R | 0 | Mask for corresponding field in INTR register. |

18.13.3.12 LIN_CH_INTR_MASKED

Description: Interrupt masked

Address: 0x405080CC

Offset: 0xCC

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise AND between the INTR and INTR_MASK registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for INTR and one for INTR_MASK. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------------|------------------------|----------------------|
| Name | None [7:3] | | | | | TX_WAKEUP_DONE [2:2] | TX_RESPONSE_DONE [1:1] | TX_HEADER_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-----------------|-------------------------|--------------|-----------------------------|------------------------------|------------------------|----------------------|
| Name | None [15:15] | TIMEOUT [14:14] | RX_NOISE_DETECT [13:13] | None [12:12] | RX_HEADER_SYNC_DONE [11:11] | RX_BREAK_WAKEUP_DONE [10:10] | RX_RESPONSE_DONE [9:9] | RX_HEADER_DONE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|-------------------------------|-----------------------------|
| Name | None [23:18] | | | | | | TX_RESPONSE_BIT_ERROR [17:17] | TX_HEADER_BIT_ERROR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|------------------------------------|---------------------------------|--------------------------------|------------------------------|-------------------------------|
| Name | None [31:29] | | | RX_RESPONSE_CHECKSUM_ERROR [28:28] | RX_RESPONSE_FRAME_ERROR [27:27] | RX_HEADER_PARITY_ERROR [26:26] | RX_HEADER_SYNC_ERROR [25:25] | RX_HEADER_FRAME_ERROR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|---|
| 0 | TX_HEADER_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 1 | TX_RESPONSE_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 2 | TX_WAKEUP_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 8 | RX_HEADER_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 9 | RX_RESPONSE_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 10 | RX_BREAK_WAKEUP_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 11 | RX_HEADER_SYNC_DONE | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------------|----|----|-----------------|---|
| 13 | RX_NOISE_DETECT | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 14 | TIMEOUT | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 16 | TX_HEADER_BIT_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 17 | TX_RESPONSE_BIT_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 24 | RX_HEADER_FRAME_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 25 | RX_HEADER_SYNC_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 26 | RX_HEADER_PARITY_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 27 | RX_RESPONSE_FRAME_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |
| 28 | RX_RESPONSE_CHECKSUM_ERROR | R | W | 0 | Logical AND of corresponding INTR and INTR_MASK fields. |

19 PASS

| | |
|---------------------|--|
| Description | Programmable Analog Subsystem for S40E |
| Base Address | 0x40900000 |
| Size | 0x100000 |
| Slave Num | MMIO9 - 0 |

19.1 SAR 0

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|---|
| PASS0_SAR0_CTL | 0x40900000 | FULL | Analog control register. |
| PASS0_SAR0_DIAG_CTL | 0x40900004 | FULL | Diagnostic Reference control register. |
| PASS0_SAR0_PRECOND_CTL | 0x40900010 | FULL | Preconditioning control register. |
| PASS0_SAR0_ANA_CAL | 0x40900080 | FULL | Current analog calibration values |
| PASS0_SAR0_DIG_CAL | 0x40900084 | FULL | Current digital calibration values |
| PASS0_SAR0_ANA_CAL_ALT | 0x40900090 | FULL | Alternate analog calibration values |
| PASS0_SAR0_DIG_CAL_ALT | 0x40900094 | FULL | Alternate digital calibration values |
| PASS0_SAR0_CAL_UPD_CMD | 0x40900098 | FULL | Calibration update command |
| PASS0_SAR0_TR_PEND | 0x40900100 | FULL | Trigger pending status |
| PASS0_SAR0_WORK_VALID | 0x40900180 | FULL | Channel working data register 'valid' bits |
| PASS0_SAR0_WORK_RANGE | 0x40900184 | FULL | Range detected |
| PASS0_SAR0_WORK_RANGE_HI | 0x40900188 | FULL | Range detect above Hi flag |
| PASS0_SAR0_WORK_PULSE | 0x4090018C | FULL | Pulse detected |
| PASS0_SAR0_RESULT_VALID | 0x409001A0 | FULL | Channel result data register 'valid' bits |
| PASS0_SAR0_RESULT_RANGE_HI | 0x409001A4 | FULL | Channel Range above Hi flags |
| PASS0_SAR0_STATUS | 0x40900200 | FULL | Current status of internal SAR registers (mostly for debug) |
| PASS0_SAR0_AVG_STAT | 0x40900204 | FULL | Current averaging status (for debug) |

19.1.1 CH 0

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH0_TR_CTL | 0x40900800 | FULL | Trigger control. |
| PASS0_SAR0_CH0_SAMPLE_CTL | 0x40900804 | FULL | Sample control. |
| PASS0_SAR0_CH0_POST_CTL | 0x40900808 | FULL | Post processing control |
| PASS0_SAR0_CH0_RANGE_CTL | 0x4090080C | FULL | Range thresholds |
| PASS0_SAR0_CH0_INTR | 0x40900810 | FULL | Interrupt request register. |
| PASS0_SAR0_CH0_INTR_SET | 0x40900814 | FULL | Interrupt set request register |
| PASS0_SAR0_CH0_INTR_MASK | 0x40900818 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH0_INTR_MASKED | 0x4090081C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH0_WORK | 0x40900820 | FULL | Working data register |
| PASS0_SAR0_CH0_RESULT | 0x40900824 | FULL | Result data register |
| PASS0_SAR0_CH0_GRP_STAT | 0x40900828 | FULL | Group status register |
| PASS0_SAR0_CH0_ENABLE | 0x40900838 | FULL | Enable register |
| PASS0_SAR0_CH0_TR_CMD | 0x4090083C | FULL | Software triggers |

19.1.2 CH 1

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH1_TR_CTL | 0x40900840 | FULL | Trigger control. |
| PASS0_SAR0_CH1_SAMPLE_CTL | 0x40900844 | FULL | Sample control. |
| PASS0_SAR0_CH1_POST_CTL | 0x40900848 | FULL | Post processing control |
| PASS0_SAR0_CH1_RANGE_CTL | 0x4090084C | FULL | Range thresholds |
| PASS0_SAR0_CH1_INTR | 0x40900850 | FULL | Interrupt request register. |
| PASS0_SAR0_CH1_INTR_SET | 0x40900854 | FULL | Interrupt set request register |
| PASS0_SAR0_CH1_INTR_MASK | 0x40900858 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH1_INTR_MASKED | 0x4090085C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH1_WORK | 0x40900860 | FULL | Working data register |
| PASS0_SAR0_CH1_RESULT | 0x40900864 | FULL | Result data register |
| PASS0_SAR0_CH1_GRP_STAT | 0x40900868 | FULL | Group status register |
| PASS0_SAR0_CH1_ENABLE | 0x40900878 | FULL | Enable register |
| PASS0_SAR0_CH1_TR_CMD | 0x4090087C | FULL | Software triggers |

19.1.3 CH 2

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH2_TR_CTL | 0x40900880 | FULL | Trigger control. |
| PASS0_SAR0_CH2_SAMPLE_CTL | 0x40900884 | FULL | Sample control. |
| PASS0_SAR0_CH2_POST_CTL | 0x40900888 | FULL | Post processing control |
| PASS0_SAR0_CH2_RANGE_CTL | 0x4090088C | FULL | Range thresholds |
| PASS0_SAR0_CH2_INTR | 0x40900890 | FULL | Interrupt request register. |
| PASS0_SAR0_CH2_INTR_SET | 0x40900894 | FULL | Interrupt set request register |
| PASS0_SAR0_CH2_INTR_MASK | 0x40900898 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH2_INTR_MASKED | 0x4090089C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH2_WORK | 0x409008A0 | FULL | Working data register |
| PASS0_SAR0_CH2_RESULT | 0x409008A4 | FULL | Result data register |
| PASS0_SAR0_CH2_GRP_STAT | 0x409008A8 | FULL | Group status register |
| PASS0_SAR0_CH2_ENABLE | 0x409008B8 | FULL | Enable register |
| PASS0_SAR0_CH2_TR_CMD | 0x409008BC | FULL | Software triggers |

19.1.4 CH 3

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH3_TR_CTL | 0x409008C0 | FULL | Trigger control. |
| PASS0_SAR0_CH3_SAMPLE_CTL | 0x409008C4 | FULL | Sample control. |
| PASS0_SAR0_CH3_POST_CTL | 0x409008C8 | FULL | Post processing control |
| PASS0_SAR0_CH3_RANGE_CTL | 0x409008CC | FULL | Range thresholds |
| PASS0_SAR0_CH3_INTR | 0x409008D0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH3_INTR_SET | 0x409008D4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH3_INTR_MASK | 0x409008D8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH3_INTR_MASKED | 0x409008DC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH3_WORK | 0x409008E0 | FULL | Working data register |
| PASS0_SAR0_CH3_RESULT | 0x409008E4 | FULL | Result data register |
| PASS0_SAR0_CH3_GRP_STAT | 0x409008E8 | FULL | Group status register |
| PASS0_SAR0_CH3_ENABLE | 0x409008F8 | FULL | Enable register |
| PASS0_SAR0_CH3_TR_CMD | 0x409008FC | FULL | Software triggers |

19.1.5 CH 4

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH4_TR_CTL | 0x40900900 | FULL | Trigger control. |
| PASS0_SAR0_CH4_SAMPLE_CTL | 0x40900904 | FULL | Sample control. |
| PASS0_SAR0_CH4_POST_CTL | 0x40900908 | FULL | Post processing control |
| PASS0_SAR0_CH4_RANGE_CTL | 0x4090090C | FULL | Range thresholds |
| PASS0_SAR0_CH4_INTR | 0x40900910 | FULL | Interrupt request register. |
| PASS0_SAR0_CH4_INTR_SET | 0x40900914 | FULL | Interrupt set request register |
| PASS0_SAR0_CH4_INTR_MASK | 0x40900918 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH4_INTR_MASKED | 0x4090091C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH4_WORK | 0x40900920 | FULL | Working data register |
| PASS0_SAR0_CH4_RESULT | 0x40900924 | FULL | Result data register |
| PASS0_SAR0_CH4_GRP_STAT | 0x40900928 | FULL | Group status register |
| PASS0_SAR0_CH4_ENABLE | 0x40900938 | FULL | Enable register |
| PASS0_SAR0_CH4_TR_CMD | 0x4090093C | FULL | Software triggers |

19.1.6 CH 5

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH5_TR_CTL | 0x40900940 | FULL | Trigger control. |
| PASS0_SAR0_CH5_SAMPLE_CTL | 0x40900944 | FULL | Sample control. |
| PASS0_SAR0_CH5_POST_CTL | 0x40900948 | FULL | Post processing control |
| PASS0_SAR0_CH5_RANGE_CTL | 0x4090094C | FULL | Range thresholds |
| PASS0_SAR0_CH5_INTR | 0x40900950 | FULL | Interrupt request register. |
| PASS0_SAR0_CH5_INTR_SET | 0x40900954 | FULL | Interrupt set request register |
| PASS0_SAR0_CH5_INTR_MASK | 0x40900958 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH5_INTR_MASKED | 0x4090095C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH5_WORK | 0x40900960 | FULL | Working data register |
| PASS0_SAR0_CH5_RESULT | 0x40900964 | FULL | Result data register |
| PASS0_SAR0_CH5_GRP_STAT | 0x40900968 | FULL | Group status register |
| PASS0_SAR0_CH5_ENABLE | 0x40900978 | FULL | Enable register |
| PASS0_SAR0_CH5_TR_CMD | 0x4090097C | FULL | Software triggers |

19.1.7 CH 6

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH6_TR_CTL | 0x40900980 | FULL | Trigger control. |
| PASS0_SAR0_CH6_SAMPLE_CTL | 0x40900984 | FULL | Sample control. |
| PASS0_SAR0_CH6_POST_CTL | 0x40900988 | FULL | Post processing control |
| PASS0_SAR0_CH6_RANGE_CTL | 0x4090098C | FULL | Range thresholds |
| PASS0_SAR0_CH6_INTR | 0x40900990 | FULL | Interrupt request register. |
| PASS0_SAR0_CH6_INTR_SET | 0x40900994 | FULL | Interrupt set request register |
| PASS0_SAR0_CH6_INTR_MASK | 0x40900998 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH6_INTR_MASKED | 0x4090099C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH6_WORK | 0x409009A0 | FULL | Working data register |
| PASS0_SAR0_CH6_RESULT | 0x409009A4 | FULL | Result data register |
| PASS0_SAR0_CH6_GRP_STAT | 0x409009A8 | FULL | Group status register |
| PASS0_SAR0_CH6_ENABLE | 0x409009B8 | FULL | Enable register |
| PASS0_SAR0_CH6_TR_CMD | 0x409009BC | FULL | Software triggers |

19.1.8 CH 7

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH7_TR_CTL | 0x409009C0 | FULL | Trigger control. |
| PASS0_SAR0_CH7_SAMPLE_CTL | 0x409009C4 | FULL | Sample control. |
| PASS0_SAR0_CH7_POST_CTL | 0x409009C8 | FULL | Post processing control |
| PASS0_SAR0_CH7_RANGE_CTL | 0x409009CC | FULL | Range thresholds |
| PASS0_SAR0_CH7_INTR | 0x409009D0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH7_INTR_SET | 0x409009D4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH7_INTR_MASK | 0x409009D8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH7_INTR_MASKED | 0x409009DC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH7_WORK | 0x409009E0 | FULL | Working data register |
| PASS0_SAR0_CH7_RESULT | 0x409009E4 | FULL | Result data register |
| PASS0_SAR0_CH7_GRP_STAT | 0x409009E8 | FULL | Group status register |
| PASS0_SAR0_CH7_ENABLE | 0x409009F8 | FULL | Enable register |
| PASS0_SAR0_CH7_TR_CMD | 0x409009FC | FULL | Software triggers |

19.1.9 CH 8

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH8_TR_CTL | 0x40900A00 | FULL | Trigger control. |
| PASS0_SAR0_CH8_SAMPLE_CTL | 0x40900A04 | FULL | Sample control. |
| PASS0_SAR0_CH8_POST_CTL | 0x40900A08 | FULL | Post processing control |
| PASS0_SAR0_CH8_RANGE_CTL | 0x40900A0C | FULL | Range thresholds |
| PASS0_SAR0_CH8_INTR | 0x40900A10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH8_INTR_SET | 0x40900A14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH8_INTR_MASK | 0x40900A18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH8_INTR_MASKED | 0x40900A1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH8_WORK | 0x40900A20 | FULL | Working data register |
| PASS0_SAR0_CH8_RESULT | 0x40900A24 | FULL | Result data register |
| PASS0_SAR0_CH8_GRP_STAT | 0x40900A28 | FULL | Group status register |
| PASS0_SAR0_CH8_ENABLE | 0x40900A38 | FULL | Enable register |
| PASS0_SAR0_CH8_TR_CMD | 0x40900A3C | FULL | Software triggers |

19.1.10 CH 9

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH9_TR_CTL | 0x40900A40 | FULL | Trigger control. |
| PASS0_SAR0_CH9_SAMPLE_CTL | 0x40900A44 | FULL | Sample control. |
| PASS0_SAR0_CH9_POST_CTL | 0x40900A48 | FULL | Post processing control |
| PASS0_SAR0_CH9_RANGE_CTL | 0x40900A4C | FULL | Range thresholds |
| PASS0_SAR0_CH9_INTR | 0x40900A50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH9_INTR_SET | 0x40900A54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH9_INTR_MASK | 0x40900A58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH9_INTR_MASKED | 0x40900A5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH9_WORK | 0x40900A60 | FULL | Working data register |
| PASS0_SAR0_CH9_RESULT | 0x40900A64 | FULL | Result data register |
| PASS0_SAR0_CH9_GRP_STAT | 0x40900A68 | FULL | Group status register |
| PASS0_SAR0_CH9_ENABLE | 0x40900A78 | FULL | Enable register |
| PASS0_SAR0_CH9_TR_CMD | 0x40900A7C | FULL | Software triggers |

19.1.11 CH 10

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH10_TR_CTL | 0x40900A80 | FULL | Trigger control. |
| PASS0_SAR0_CH10_SAMPLE_CTL | 0x40900A84 | FULL | Sample control. |
| PASS0_SAR0_CH10_POST_CTL | 0x40900A88 | FULL | Post processing control |
| PASS0_SAR0_CH10_RANGE_CTL | 0x40900A8C | FULL | Range thresholds |
| PASS0_SAR0_CH10_INTR | 0x40900A90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH10_INTR_SET | 0x40900A94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH10_INTR_MASK | 0x40900A98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH10_INTR_MASKED | 0x40900A9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH10_WORK | 0x40900AA0 | FULL | Working data register |
| PASS0_SAR0_CH10_RESULT | 0x40900AA4 | FULL | Result data register |
| PASS0_SAR0_CH10_GRP_STAT | 0x40900AA8 | FULL | Group status register |
| PASS0_SAR0_CH10_ENABLE | 0x40900AB8 | FULL | Enable register |
| PASS0_SAR0_CH10_TR_CMD | 0x40900ABC | FULL | Software triggers |

19.1.12 CH 11

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH11_TR_CTL | 0x40900AC0 | FULL | Trigger control. |
| PASS0_SAR0_CH11_SAMPLE_CTL | 0x40900AC4 | FULL | Sample control. |
| PASS0_SAR0_CH11_POST_CTL | 0x40900AC8 | FULL | Post processing control |
| PASS0_SAR0_CH11_RANGE_CTL | 0x40900ACC | FULL | Range thresholds |
| PASS0_SAR0_CH11_INTR | 0x40900AD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH11_INTR_SET | 0x40900AD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH11_INTR_MASK | 0x40900AD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH11_INTR_MASKED | 0x40900ADC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH11_WORK | 0x40900AE0 | FULL | Working data register |
| PASS0_SAR0_CH11_RESULT | 0x40900AE4 | FULL | Result data register |
| PASS0_SAR0_CH11_GRP_STAT | 0x40900AE8 | FULL | Group status register |
| PASS0_SAR0_CH11_ENABLE | 0x40900AF8 | FULL | Enable register |
| PASS0_SAR0_CH11_TR_CMD | 0x40900AFC | FULL | Software triggers |

19.1.13 CH 12

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH12_TR_CTL | 0x40900B00 | FULL | Trigger control. |
| PASS0_SAR0_CH12_SAMPLE_CTL | 0x40900B04 | FULL | Sample control. |
| PASS0_SAR0_CH12_POST_CTL | 0x40900B08 | FULL | Post processing control |
| PASS0_SAR0_CH12_RANGE_CTL | 0x40900B0C | FULL | Range thresholds |
| PASS0_SAR0_CH12_INTR | 0x40900B10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH12_INTR_SET | 0x40900B14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH12_INTR_MASK | 0x40900B18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH12_INTR_MASKED | 0x40900B1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH12_WORK | 0x40900B20 | FULL | Working data register |
| PASS0_SAR0_CH12_RESULT | 0x40900B24 | FULL | Result data register |
| PASS0_SAR0_CH12_GRP_STAT | 0x40900B28 | FULL | Group status register |
| PASS0_SAR0_CH12_ENABLE | 0x40900B38 | FULL | Enable register |
| PASS0_SAR0_CH12_TR_CMD | 0x40900B3C | FULL | Software triggers |

19.1.14 CH 13

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH13_TR_CTL | 0x40900B40 | FULL | Trigger control. |
| PASS0_SAR0_CH13_SAMPLE_CTL | 0x40900B44 | FULL | Sample control. |
| PASS0_SAR0_CH13_POST_CTL | 0x40900B48 | FULL | Post processing control |
| PASS0_SAR0_CH13_RANGE_CTL | 0x40900B4C | FULL | Range thresholds |
| PASS0_SAR0_CH13_INTR | 0x40900B50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH13_INTR_SET | 0x40900B54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH13_INTR_MASK | 0x40900B58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH13_INTR_MASKED | 0x40900B5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH13_WORK | 0x40900B60 | FULL | Working data register |
| PASS0_SAR0_CH13_RESULT | 0x40900B64 | FULL | Result data register |
| PASS0_SAR0_CH13_GRP_STAT | 0x40900B68 | FULL | Group status register |
| PASS0_SAR0_CH13_ENABLE | 0x40900B78 | FULL | Enable register |
| PASS0_SAR0_CH13_TR_CMD | 0x40900B7C | FULL | Software triggers |

19.1.15 CH 14

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH14_TR_CTL | 0x40900B80 | FULL | Trigger control. |
| PASS0_SAR0_CH14_SAMPLE_CTL | 0x40900B84 | FULL | Sample control. |
| PASS0_SAR0_CH14_POST_CTL | 0x40900B88 | FULL | Post processing control |
| PASS0_SAR0_CH14_RANGE_CTL | 0x40900B8C | FULL | Range thresholds |
| PASS0_SAR0_CH14_INTR | 0x40900B90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH14_INTR_SET | 0x40900B94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH14_INTR_MASK | 0x40900B98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH14_INTR_MASKED | 0x40900B9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH14_WORK | 0x40900BA0 | FULL | Working data register |
| PASS0_SAR0_CH14_RESULT | 0x40900BA4 | FULL | Result data register |
| PASS0_SAR0_CH14_GRP_STAT | 0x40900BA8 | FULL | Group status register |
| PASS0_SAR0_CH14_ENABLE | 0x40900BB8 | FULL | Enable register |
| PASS0_SAR0_CH14_TR_CMD | 0x40900BBC | FULL | Software triggers |

19.1.16 CH 15

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH15_TR_CTL | 0x40900BC0 | FULL | Trigger control. |
| PASS0_SAR0_CH15_SAMPLE_CTL | 0x40900BC4 | FULL | Sample control. |
| PASS0_SAR0_CH15_POST_CTL | 0x40900BC8 | FULL | Post processing control |
| PASS0_SAR0_CH15_RANGE_CTL | 0x40900BCC | FULL | Range thresholds |
| PASS0_SAR0_CH15_INTR | 0x40900BD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH15_INTR_SET | 0x40900BD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH15_INTR_MASK | 0x40900BD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH15_INTR_MASKED | 0x40900BDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH15_WORK | 0x40900BE0 | FULL | Working data register |
| PASS0_SAR0_CH15_RESULT | 0x40900BE4 | FULL | Result data register |
| PASS0_SAR0_CH15_GRP_STAT | 0x40900BE8 | FULL | Group status register |
| PASS0_SAR0_CH15_ENABLE | 0x40900BF8 | FULL | Enable register |
| PASS0_SAR0_CH15_TR_CMD | 0x40900BFC | FULL | Software triggers |

19.1.17 CH 16

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH16_TR_CTL | 0x40900C00 | FULL | Trigger control. |
| PASS0_SAR0_CH16_SAMPLE_CTL | 0x40900C04 | FULL | Sample control. |
| PASS0_SAR0_CH16_POST_CTL | 0x40900C08 | FULL | Post processing control |
| PASS0_SAR0_CH16_RANGE_CTL | 0x40900C0C | FULL | Range thresholds |
| PASS0_SAR0_CH16_INTR | 0x40900C10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH16_INTR_SET | 0x40900C14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH16_INTR_MASK | 0x40900C18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH16_INTR_MASKED | 0x40900C1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH16_WORK | 0x40900C20 | FULL | Working data register |
| PASS0_SAR0_CH16_RESULT | 0x40900C24 | FULL | Result data register |
| PASS0_SAR0_CH16_GRP_STAT | 0x40900C28 | FULL | Group status register |
| PASS0_SAR0_CH16_ENABLE | 0x40900C38 | FULL | Enable register |
| PASS0_SAR0_CH16_TR_CMD | 0x40900C3C | FULL | Software triggers |

19.1.18 CH 17

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH17_TR_CTL | 0x40900C40 | FULL | Trigger control. |
| PASS0_SAR0_CH17_SAMPLE_CTL | 0x40900C44 | FULL | Sample control. |
| PASS0_SAR0_CH17_POST_CTL | 0x40900C48 | FULL | Post processing control |
| PASS0_SAR0_CH17_RANGE_CTL | 0x40900C4C | FULL | Range thresholds |
| PASS0_SAR0_CH17_INTR | 0x40900C50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH17_INTR_SET | 0x40900C54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH17_INTR_MASK | 0x40900C58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH17_INTR_MASKED | 0x40900C5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH17_WORK | 0x40900C60 | FULL | Working data register |
| PASS0_SAR0_CH17_RESULT | 0x40900C64 | FULL | Result data register |
| PASS0_SAR0_CH17_GRP_STAT | 0x40900C68 | FULL | Group status register |
| PASS0_SAR0_CH17_ENABLE | 0x40900C78 | FULL | Enable register |
| PASS0_SAR0_CH17_TR_CMD | 0x40900C7C | FULL | Software triggers |

19.1.19 CH 18

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH18_TR_CTL | 0x40900C80 | FULL | Trigger control. |
| PASS0_SAR0_CH18_SAMPLE_CTL | 0x40900C84 | FULL | Sample control. |
| PASS0_SAR0_CH18_POST_CTL | 0x40900C88 | FULL | Post processing control |
| PASS0_SAR0_CH18_RANGE_CTL | 0x40900C8C | FULL | Range thresholds |
| PASS0_SAR0_CH18_INTR | 0x40900C90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH18_INTR_SET | 0x40900C94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH18_INTR_MASK | 0x40900C98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH18_INTR_MASKED | 0x40900C9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH18_WORK | 0x40900CA0 | FULL | Working data register |
| PASS0_SAR0_CH18_RESULT | 0x40900CA4 | FULL | Result data register |
| PASS0_SAR0_CH18_GRP_STAT | 0x40900CA8 | FULL | Group status register |
| PASS0_SAR0_CH18_ENABLE | 0x40900CB8 | FULL | Enable register |
| PASS0_SAR0_CH18_TR_CMD | 0x40900CBC | FULL | Software triggers |

19.1.20 CH 19

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH19_TR_CTL | 0x40900CC0 | FULL | Trigger control. |
| PASS0_SAR0_CH19_SAMPLE_CTL | 0x40900CC4 | FULL | Sample control. |
| PASS0_SAR0_CH19_POST_CTL | 0x40900CC8 | FULL | Post processing control |
| PASS0_SAR0_CH19_RANGE_CTL | 0x40900CCC | FULL | Range thresholds |
| PASS0_SAR0_CH19_INTR | 0x40900CD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH19_INTR_SET | 0x40900CD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH19_INTR_MASK | 0x40900CD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH19_INTR_MASKED | 0x40900CDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH19_WORK | 0x40900CE0 | FULL | Working data register |
| PASS0_SAR0_CH19_RESULT | 0x40900CE4 | FULL | Result data register |
| PASS0_SAR0_CH19_GRP_STAT | 0x40900CE8 | FULL | Group status register |
| PASS0_SAR0_CH19_ENABLE | 0x40900CF8 | FULL | Enable register |
| PASS0_SAR0_CH19_TR_CMD | 0x40900CFC | FULL | Software triggers |

19.1.21 CH 20

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH20_TR_CTL | 0x40900D00 | FULL | Trigger control. |
| PASS0_SAR0_CH20_SAMPLE_CTL | 0x40900D04 | FULL | Sample control. |
| PASS0_SAR0_CH20_POST_CTL | 0x40900D08 | FULL | Post processing control |
| PASS0_SAR0_CH20_RANGE_CTL | 0x40900D0C | FULL | Range thresholds |
| PASS0_SAR0_CH20_INTR | 0x40900D10 | FULL | Interrupt request register. |
| PASS0_SAR0_CH20_INTR_SET | 0x40900D14 | FULL | Interrupt set request register |
| PASS0_SAR0_CH20_INTR_MASK | 0x40900D18 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH20_INTR_MASKED | 0x40900D1C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH20_WORK | 0x40900D20 | FULL | Working data register |
| PASS0_SAR0_CH20_RESULT | 0x40900D24 | FULL | Result data register |
| PASS0_SAR0_CH20_GRP_STAT | 0x40900D28 | FULL | Group status register |
| PASS0_SAR0_CH20_ENABLE | 0x40900D38 | FULL | Enable register |
| PASS0_SAR0_CH20_TR_CMD | 0x40900D3C | FULL | Software triggers |

19.1.22 CH 21

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH21_TR_CTL | 0x40900D40 | FULL | Trigger control. |
| PASS0_SAR0_CH21_SAMPLE_CTL | 0x40900D44 | FULL | Sample control. |
| PASS0_SAR0_CH21_POST_CTL | 0x40900D48 | FULL | Post processing control |
| PASS0_SAR0_CH21_RANGE_CTL | 0x40900D4C | FULL | Range thresholds |
| PASS0_SAR0_CH21_INTR | 0x40900D50 | FULL | Interrupt request register. |
| PASS0_SAR0_CH21_INTR_SET | 0x40900D54 | FULL | Interrupt set request register |
| PASS0_SAR0_CH21_INTR_MASK | 0x40900D58 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH21_INTR_MASKED | 0x40900D5C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH21_WORK | 0x40900D60 | FULL | Working data register |
| PASS0_SAR0_CH21_RESULT | 0x40900D64 | FULL | Result data register |
| PASS0_SAR0_CH21_GRP_STAT | 0x40900D68 | FULL | Group status register |
| PASS0_SAR0_CH21_ENABLE | 0x40900D78 | FULL | Enable register |
| PASS0_SAR0_CH21_TR_CMD | 0x40900D7C | FULL | Software triggers |

19.1.23 CH 22

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH22_TR_CTL | 0x40900D80 | FULL | Trigger control. |
| PASS0_SAR0_CH22_SAMPLE_CTL | 0x40900D84 | FULL | Sample control. |
| PASS0_SAR0_CH22_POST_CTL | 0x40900D88 | FULL | Post processing control |
| PASS0_SAR0_CH22_RANGE_CTL | 0x40900D8C | FULL | Range thresholds |
| PASS0_SAR0_CH22_INTR | 0x40900D90 | FULL | Interrupt request register. |
| PASS0_SAR0_CH22_INTR_SET | 0x40900D94 | FULL | Interrupt set request register |
| PASS0_SAR0_CH22_INTR_MASK | 0x40900D98 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH22_INTR_MASKED | 0x40900D9C | FULL | Interrupt masked request register |
| PASS0_SAR0_CH22_WORK | 0x40900DA0 | FULL | Working data register |
| PASS0_SAR0_CH22_RESULT | 0x40900DA4 | FULL | Result data register |
| PASS0_SAR0_CH22_GRP_STAT | 0x40900DA8 | FULL | Group status register |
| PASS0_SAR0_CH22_ENABLE | 0x40900DB8 | FULL | Enable register |
| PASS0_SAR0_CH22_TR_CMD | 0x40900DBC | FULL | Software triggers |

19.1.24 CH 23

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR0_CH23_TR_CTL | 0x40900DC0 | FULL | Trigger control. |
| PASS0_SAR0_CH23_SAMPLE_CTL | 0x40900DC4 | FULL | Sample control. |
| PASS0_SAR0_CH23_POST_CTL | 0x40900DC8 | FULL | Post processing control |
| PASS0_SAR0_CH23_RANGE_CTL | 0x40900DCC | FULL | Range thresholds |
| PASS0_SAR0_CH23_INTR | 0x40900DD0 | FULL | Interrupt request register. |
| PASS0_SAR0_CH23_INTR_SET | 0x40900DD4 | FULL | Interrupt set request register |
| PASS0_SAR0_CH23_INTR_MASK | 0x40900DD8 | FULL | Interrupt mask register. |
| PASS0_SAR0_CH23_INTR_MASKED | 0x40900DDC | FULL | Interrupt masked request register |
| PASS0_SAR0_CH23_WORK | 0x40900DE0 | FULL | Working data register |
| PASS0_SAR0_CH23_RESULT | 0x40900DE4 | FULL | Result data register |
| PASS0_SAR0_CH23_GRP_STAT | 0x40900DE8 | FULL | Group status register |
| PASS0_SAR0_CH23_ENABLE | 0x40900DF8 | FULL | Enable register |
| PASS0_SAR0_CH23_TR_CMD | 0x40900DFC | FULL | Software triggers |

19.2 SAR 1

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|---|
| PASS0_SAR1_CTL | 0x40901000 | FULL | Analog control register. |
| PASS0_SAR1_DIAG_CTL | 0x40901004 | FULL | Diagnostic Reference control register. |
| PASS0_SAR1_PRECOND_CTL | 0x40901010 | FULL | Preconditioning control register. |
| PASS0_SAR1_ANA_CAL | 0x40901080 | FULL | Current analog calibration values |
| PASS0_SAR1_DIG_CAL | 0x40901084 | FULL | Current digital calibration values |
| PASS0_SAR1_ANA_CAL_ALT | 0x40901090 | FULL | Alternate analog calibration values |
| PASS0_SAR1_DIG_CAL_ALT | 0x40901094 | FULL | Alternate digital calibration values |
| PASS0_SAR1_CAL_UPD_CMD | 0x40901098 | FULL | Calibration update command |
| PASS0_SAR1_TR_PEND | 0x40901100 | FULL | Trigger pending status |
| PASS0_SAR1_WORK_VALID | 0x40901180 | FULL | Channel working data register 'valid' bits |
| PASS0_SAR1_WORK_RANGE | 0x40901184 | FULL | Range detected |
| PASS0_SAR1_WORK_RANGE_HI | 0x40901188 | FULL | Range detect above Hi flag |
| PASS0_SAR1_WORK_PULSE | 0x4090118C | FULL | Pulse detected |
| PASS0_SAR1_RESULT_VALID | 0x409011A0 | FULL | Channel result data register 'valid' bits |
| PASS0_SAR1_RESULT_RANGE_HI | 0x409011A4 | FULL | Channel Range above Hi flags |
| PASS0_SAR1_STATUS | 0x40901200 | FULL | Current status of internal SAR registers (mostly for debug) |
| PASS0_SAR1_AVG_STAT | 0x40901204 | FULL | Current averaging status (for debug) |

19.2.1 CH 0

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH0_TR_CTL | 0x40901800 | FULL | Trigger control. |
| PASS0_SAR1_CH0_SAMPLE_CTL | 0x40901804 | FULL | Sample control. |
| PASS0_SAR1_CH0_POST_CTL | 0x40901808 | FULL | Post processing control |
| PASS0_SAR1_CH0_RANGE_CTL | 0x4090180C | FULL | Range thresholds |
| PASS0_SAR1_CH0_INTR | 0x40901810 | FULL | Interrupt request register. |
| PASS0_SAR1_CH0_INTR_SET | 0x40901814 | FULL | Interrupt set request register |
| PASS0_SAR1_CH0_INTR_MASK | 0x40901818 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH0_INTR_MASKED | 0x4090181C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH0_WORK | 0x40901820 | FULL | Working data register |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------|
| PASS0_SAR1_CH0_RESULT | 0x40901824 | FULL | Result data register |
| PASS0_SAR1_CH0_GRP_STAT | 0x40901828 | FULL | Group status register |
| PASS0_SAR1_CH0_ENABLE | 0x40901838 | FULL | Enable register |
| PASS0_SAR1_CH0_TR_CMD | 0x4090183C | FULL | Software triggers |

19.2.2 CH 1

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH1_TR_CTL | 0x40901840 | FULL | Trigger control. |
| PASS0_SAR1_CH1_SAMPLE_CTL | 0x40901844 | FULL | Sample control. |
| PASS0_SAR1_CH1_POST_CTL | 0x40901848 | FULL | Post processing control |
| PASS0_SAR1_CH1_RANGE_CTL | 0x4090184C | FULL | Range thresholds |
| PASS0_SAR1_CH1_INTR | 0x40901850 | FULL | Interrupt request register. |
| PASS0_SAR1_CH1_INTR_SET | 0x40901854 | FULL | Interrupt set request register |
| PASS0_SAR1_CH1_INTR_MASK | 0x40901858 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH1_INTR_MASKED | 0x4090185C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH1_WORK | 0x40901860 | FULL | Working data register |
| PASS0_SAR1_CH1_RESULT | 0x40901864 | FULL | Result data register |
| PASS0_SAR1_CH1_GRP_STAT | 0x40901868 | FULL | Group status register |
| PASS0_SAR1_CH1_ENABLE | 0x40901878 | FULL | Enable register |
| PASS0_SAR1_CH1_TR_CMD | 0x4090187C | FULL | Software triggers |

19.2.3 CH 2

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH2_TR_CTL | 0x40901880 | FULL | Trigger control. |
| PASS0_SAR1_CH2_SAMPLE_CTL | 0x40901884 | FULL | Sample control. |
| PASS0_SAR1_CH2_POST_CTL | 0x40901888 | FULL | Post processing control |
| PASS0_SAR1_CH2_RANGE_CTL | 0x4090188C | FULL | Range thresholds |
| PASS0_SAR1_CH2_INTR | 0x40901890 | FULL | Interrupt request register. |
| PASS0_SAR1_CH2_INTR_SET | 0x40901894 | FULL | Interrupt set request register |
| PASS0_SAR1_CH2_INTR_MASK | 0x40901898 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH2_INTR_MASKED | 0x4090189C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH2_WORK | 0x409018A0 | FULL | Working data register |
| PASS0_SAR1_CH2_RESULT | 0x409018A4 | FULL | Result data register |
| PASS0_SAR1_CH2_GRP_STAT | 0x409018A8 | FULL | Group status register |
| PASS0_SAR1_CH2_ENABLE | 0x409018B8 | FULL | Enable register |
| PASS0_SAR1_CH2_TR_CMD | 0x409018BC | FULL | Software triggers |

19.2.4 CH 3

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH3_TR_CTL | 0x409018C0 | FULL | Trigger control. |
| PASS0_SAR1_CH3_SAMPLE_CTL | 0x409018C4 | FULL | Sample control. |
| PASS0_SAR1_CH3_POST_CTL | 0x409018C8 | FULL | Post processing control |
| PASS0_SAR1_CH3_RANGE_CTL | 0x409018CC | FULL | Range thresholds |
| PASS0_SAR1_CH3_INTR | 0x409018D0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH3_INTR_SET | 0x409018D4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH3_INTR_MASK | 0x409018D8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH3_INTR_MASKED | 0x409018DC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH3_WORK | 0x409018E0 | FULL | Working data register |
| PASS0_SAR1_CH3_RESULT | 0x409018E4 | FULL | Result data register |
| PASS0_SAR1_CH3_GRP_STAT | 0x409018E8 | FULL | Group status register |
| PASS0_SAR1_CH3_ENABLE | 0x409018F8 | FULL | Enable register |
| PASS0_SAR1_CH3_TR_CMD | 0x409018FC | FULL | Software triggers |

19.2.5 CH 4

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH4_TR_CTL | 0x40901900 | FULL | Trigger control. |
| PASS0_SAR1_CH4_SAMPLE_CTL | 0x40901904 | FULL | Sample control. |
| PASS0_SAR1_CH4_POST_CTL | 0x40901908 | FULL | Post processing control |
| PASS0_SAR1_CH4_RANGE_CTL | 0x4090190C | FULL | Range thresholds |
| PASS0_SAR1_CH4_INTR | 0x40901910 | FULL | Interrupt request register. |
| PASS0_SAR1_CH4_INTR_SET | 0x40901914 | FULL | Interrupt set request register |
| PASS0_SAR1_CH4_INTR_MASK | 0x40901918 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH4_INTR_MASKED | 0x4090191C | FULL | Interrupt masked request register |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------|
| PASS0_SAR1_CH4_WORK | 0x40901920 | FULL | Working data register |
| PASS0_SAR1_CH4_RESULT | 0x40901924 | FULL | Result data register |
| PASS0_SAR1_CH4_GRP_STAT | 0x40901928 | FULL | Group status register |
| PASS0_SAR1_CH4_ENABLE | 0x40901938 | FULL | Enable register |
| PASS0_SAR1_CH4_TR_CMD | 0x4090193C | FULL | Software triggers |

19.2.6 CH 5

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH5_TR_CTL | 0x40901940 | FULL | Trigger control. |
| PASS0_SAR1_CH5_SAMPLE_CTL | 0x40901944 | FULL | Sample control. |
| PASS0_SAR1_CH5_POST_CTL | 0x40901948 | FULL | Post processing control |
| PASS0_SAR1_CH5_RANGE_CTL | 0x4090194C | FULL | Range thresholds |
| PASS0_SAR1_CH5_INTR | 0x40901950 | FULL | Interrupt request register. |
| PASS0_SAR1_CH5_INTR_SET | 0x40901954 | FULL | Interrupt set request register |
| PASS0_SAR1_CH5_INTR_MASK | 0x40901958 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH5_INTR_MASKED | 0x4090195C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH5_WORK | 0x40901960 | FULL | Working data register |
| PASS0_SAR1_CH5_RESULT | 0x40901964 | FULL | Result data register |
| PASS0_SAR1_CH5_GRP_STAT | 0x40901968 | FULL | Group status register |
| PASS0_SAR1_CH5_ENABLE | 0x40901978 | FULL | Enable register |
| PASS0_SAR1_CH5_TR_CMD | 0x4090197C | FULL | Software triggers |

19.2.7 CH 6

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH6_TR_CTL | 0x40901980 | FULL | Trigger control. |
| PASS0_SAR1_CH6_SAMPLE_CTL | 0x40901984 | FULL | Sample control. |
| PASS0_SAR1_CH6_POST_CTL | 0x40901988 | FULL | Post processing control |
| PASS0_SAR1_CH6_RANGE_CTL | 0x4090198C | FULL | Range thresholds |
| PASS0_SAR1_CH6_INTR | 0x40901990 | FULL | Interrupt request register. |
| PASS0_SAR1_CH6_INTR_SET | 0x40901994 | FULL | Interrupt set request register |
| PASS0_SAR1_CH6_INTR_MASK | 0x40901998 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH6_INTR_MASKED | 0x4090199C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH6_WORK | 0x409019A0 | FULL | Working data register |
| PASS0_SAR1_CH6_RESULT | 0x409019A4 | FULL | Result data register |
| PASS0_SAR1_CH6_GRP_STAT | 0x409019A8 | FULL | Group status register |
| PASS0_SAR1_CH6_ENABLE | 0x409019B8 | FULL | Enable register |
| PASS0_SAR1_CH6_TR_CMD | 0x409019BC | FULL | Software triggers |

19.2.8 CH 7

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH7_TR_CTL | 0x409019C0 | FULL | Trigger control. |
| PASS0_SAR1_CH7_SAMPLE_CTL | 0x409019C4 | FULL | Sample control. |
| PASS0_SAR1_CH7_POST_CTL | 0x409019C8 | FULL | Post processing control |
| PASS0_SAR1_CH7_RANGE_CTL | 0x409019CC | FULL | Range thresholds |
| PASS0_SAR1_CH7_INTR | 0x409019D0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH7_INTR_SET | 0x409019D4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH7_INTR_MASK | 0x409019D8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH7_INTR_MASKED | 0x409019DC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH7_WORK | 0x409019E0 | FULL | Working data register |
| PASS0_SAR1_CH7_RESULT | 0x409019E4 | FULL | Result data register |
| PASS0_SAR1_CH7_GRP_STAT | 0x409019E8 | FULL | Group status register |
| PASS0_SAR1_CH7_ENABLE | 0x409019F8 | FULL | Enable register |
| PASS0_SAR1_CH7_TR_CMD | 0x409019FC | FULL | Software triggers |

19.2.9 CH 8

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--------------------------------|
| PASS0_SAR1_CH8_TR_CTL | 0x40901A00 | FULL | Trigger control. |
| PASS0_SAR1_CH8_SAMPLE_CTL | 0x40901A04 | FULL | Sample control. |
| PASS0_SAR1_CH8_POST_CTL | 0x40901A08 | FULL | Post processing control |
| PASS0_SAR1_CH8_RANGE_CTL | 0x40901A0C | FULL | Range thresholds |
| PASS0_SAR1_CH8_INTR | 0x40901A10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH8_INTR_SET | 0x40901A14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH8_INTR_MASK | 0x40901A18 | FULL | Interrupt mask register. |

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH8_INTR_MASKED | 0x40901A1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH8_WORK | 0x40901A20 | FULL | Working data register |
| PASS0_SAR1_CH8_RESULT | 0x40901A24 | FULL | Result data register |
| PASS0_SAR1_CH8_GRP_STAT | 0x40901A28 | FULL | Group status register |
| PASS0_SAR1_CH8_ENABLE | 0x40901A38 | FULL | Enable register |
| PASS0_SAR1_CH8_TR_CMD | 0x40901A3C | FULL | Software triggers |

19.2.10 CH 9

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH9_TR_CTL | 0x40901A40 | FULL | Trigger control. |
| PASS0_SAR1_CH9_SAMPLE_CTL | 0x40901A44 | FULL | Sample control. |
| PASS0_SAR1_CH9_POST_CTL | 0x40901A48 | FULL | Post processing control |
| PASS0_SAR1_CH9_RANGE_CTL | 0x40901A4C | FULL | Range thresholds |
| PASS0_SAR1_CH9_INTR | 0x40901A50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH9_INTR_SET | 0x40901A54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH9_INTR_MASK | 0x40901A58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH9_INTR_MASKED | 0x40901A5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH9_WORK | 0x40901A60 | FULL | Working data register |
| PASS0_SAR1_CH9_RESULT | 0x40901A64 | FULL | Result data register |
| PASS0_SAR1_CH9_GRP_STAT | 0x40901A68 | FULL | Group status register |
| PASS0_SAR1_CH9_ENABLE | 0x40901A78 | FULL | Enable register |
| PASS0_SAR1_CH9_TR_CMD | 0x40901A7C | FULL | Software triggers |

19.2.11 CH 10

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH10_TR_CTL | 0x40901A80 | FULL | Trigger control. |
| PASS0_SAR1_CH10_SAMPLE_CTL | 0x40901A84 | FULL | Sample control. |
| PASS0_SAR1_CH10_POST_CTL | 0x40901A88 | FULL | Post processing control |
| PASS0_SAR1_CH10_RANGE_CTL | 0x40901A8C | FULL | Range thresholds |
| PASS0_SAR1_CH10_INTR | 0x40901A90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH10_INTR_SET | 0x40901A94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH10_INTR_MASK | 0x40901A98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH10_INTR_MASKED | 0x40901A9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH10_WORK | 0x40901AA0 | FULL | Working data register |
| PASS0_SAR1_CH10_RESULT | 0x40901AA4 | FULL | Result data register |
| PASS0_SAR1_CH10_GRP_STAT | 0x40901AA8 | FULL | Group status register |
| PASS0_SAR1_CH10_ENABLE | 0x40901AB8 | FULL | Enable register |
| PASS0_SAR1_CH10_TR_CMD | 0x40901ABC | FULL | Software triggers |

19.2.12 CH 11

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH11_TR_CTL | 0x40901AC0 | FULL | Trigger control. |
| PASS0_SAR1_CH11_SAMPLE_CTL | 0x40901AC4 | FULL | Sample control. |
| PASS0_SAR1_CH11_POST_CTL | 0x40901AC8 | FULL | Post processing control |
| PASS0_SAR1_CH11_RANGE_CTL | 0x40901ACC | FULL | Range thresholds |
| PASS0_SAR1_CH11_INTR | 0x40901AD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH11_INTR_SET | 0x40901AD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH11_INTR_MASK | 0x40901AD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH11_INTR_MASKED | 0x40901ADC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH11_WORK | 0x40901AE0 | FULL | Working data register |
| PASS0_SAR1_CH11_RESULT | 0x40901AE4 | FULL | Result data register |
| PASS0_SAR1_CH11_GRP_STAT | 0x40901AE8 | FULL | Group status register |
| PASS0_SAR1_CH11_ENABLE | 0x40901AF8 | FULL | Enable register |
| PASS0_SAR1_CH11_TR_CMD | 0x40901AFC | FULL | Software triggers |

19.2.13 CH 12

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--------------------------------|
| PASS0_SAR1_CH12_TR_CTL | 0x40901B00 | FULL | Trigger control. |
| PASS0_SAR1_CH12_SAMPLE_CTL | 0x40901B04 | FULL | Sample control. |
| PASS0_SAR1_CH12_POST_CTL | 0x40901B08 | FULL | Post processing control |
| PASS0_SAR1_CH12_RANGE_CTL | 0x40901B0C | FULL | Range thresholds |
| PASS0_SAR1_CH12_INTR | 0x40901B10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH12_INTR_SET | 0x40901B14 | FULL | Interrupt set request register |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH12_INTR_MASK | 0x40901B18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH12_INTR_MASKED | 0x40901B1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH12_WORK | 0x40901B20 | FULL | Working data register |
| PASS0_SAR1_CH12_RESULT | 0x40901B24 | FULL | Result data register |
| PASS0_SAR1_CH12_GRP_STAT | 0x40901B28 | FULL | Group status register |
| PASS0_SAR1_CH12_ENABLE | 0x40901B38 | FULL | Enable register |
| PASS0_SAR1_CH12_TR_CMD | 0x40901B3C | FULL | Software triggers |

19.2.14 CH 13

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH13_TR_CTL | 0x40901B40 | FULL | Trigger control. |
| PASS0_SAR1_CH13_SAMPLE_CTL | 0x40901B44 | FULL | Sample control. |
| PASS0_SAR1_CH13_POST_CTL | 0x40901B48 | FULL | Post processing control |
| PASS0_SAR1_CH13_RANGE_CTL | 0x40901B4C | FULL | Range thresholds |
| PASS0_SAR1_CH13_INTR | 0x40901B50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH13_INTR_SET | 0x40901B54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH13_INTR_MASK | 0x40901B58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH13_INTR_MASKED | 0x40901B5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH13_WORK | 0x40901B60 | FULL | Working data register |
| PASS0_SAR1_CH13_RESULT | 0x40901B64 | FULL | Result data register |
| PASS0_SAR1_CH13_GRP_STAT | 0x40901B68 | FULL | Group status register |
| PASS0_SAR1_CH13_ENABLE | 0x40901B78 | FULL | Enable register |
| PASS0_SAR1_CH13_TR_CMD | 0x40901B7C | FULL | Software triggers |

19.2.15 CH 14

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH14_TR_CTL | 0x40901B80 | FULL | Trigger control. |
| PASS0_SAR1_CH14_SAMPLE_CTL | 0x40901B84 | FULL | Sample control. |
| PASS0_SAR1_CH14_POST_CTL | 0x40901B88 | FULL | Post processing control |
| PASS0_SAR1_CH14_RANGE_CTL | 0x40901B8C | FULL | Range thresholds |
| PASS0_SAR1_CH14_INTR | 0x40901B90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH14_INTR_SET | 0x40901B94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH14_INTR_MASK | 0x40901B98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH14_INTR_MASKED | 0x40901B9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH14_WORK | 0x40901BA0 | FULL | Working data register |
| PASS0_SAR1_CH14_RESULT | 0x40901BA4 | FULL | Result data register |
| PASS0_SAR1_CH14_GRP_STAT | 0x40901BA8 | FULL | Group status register |
| PASS0_SAR1_CH14_ENABLE | 0x40901BB8 | FULL | Enable register |
| PASS0_SAR1_CH14_TR_CMD | 0x40901BBC | FULL | Software triggers |

19.2.16 CH 15

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH15_TR_CTL | 0x40901BC0 | FULL | Trigger control. |
| PASS0_SAR1_CH15_SAMPLE_CTL | 0x40901BC4 | FULL | Sample control. |
| PASS0_SAR1_CH15_POST_CTL | 0x40901BC8 | FULL | Post processing control |
| PASS0_SAR1_CH15_RANGE_CTL | 0x40901BCC | FULL | Range thresholds |
| PASS0_SAR1_CH15_INTR | 0x40901BD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH15_INTR_SET | 0x40901BD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH15_INTR_MASK | 0x40901BD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH15_INTR_MASKED | 0x40901BDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH15_WORK | 0x40901BE0 | FULL | Working data register |
| PASS0_SAR1_CH15_RESULT | 0x40901BE4 | FULL | Result data register |
| PASS0_SAR1_CH15_GRP_STAT | 0x40901BE8 | FULL | Group status register |
| PASS0_SAR1_CH15_ENABLE | 0x40901BF8 | FULL | Enable register |
| PASS0_SAR1_CH15_TR_CMD | 0x40901BFC | FULL | Software triggers |

19.2.17 CH 16

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------|
| PASS0_SAR1_CH16_TR_CTL | 0x40901C00 | FULL | Trigger control. |
| PASS0_SAR1_CH16_SAMPLE_CTL | 0x40901C04 | FULL | Sample control. |
| PASS0_SAR1_CH16_POST_CTL | 0x40901C08 | FULL | Post processing control |
| PASS0_SAR1_CH16_RANGE_CTL | 0x40901C0C | FULL | Range thresholds |
| PASS0_SAR1_CH16_INTR | 0x40901C10 | FULL | Interrupt request register. |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH16_INTR_SET | 0x40901C14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH16_INTR_MASK | 0x40901C18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH16_INTR_MASKED | 0x40901C1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH16_WORK | 0x40901C20 | FULL | Working data register |
| PASS0_SAR1_CH16_RESULT | 0x40901C24 | FULL | Result data register |
| PASS0_SAR1_CH16_GRP_STAT | 0x40901C28 | FULL | Group status register |
| PASS0_SAR1_CH16_ENABLE | 0x40901C38 | FULL | Enable register |
| PASS0_SAR1_CH16_TR_CMD | 0x40901C3C | FULL | Software triggers |

19.2.18 CH 17

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH17_TR_CTL | 0x40901C40 | FULL | Trigger control. |
| PASS0_SAR1_CH17_SAMPLE_CTL | 0x40901C44 | FULL | Sample control. |
| PASS0_SAR1_CH17_POST_CTL | 0x40901C48 | FULL | Post processing control |
| PASS0_SAR1_CH17_RANGE_CTL | 0x40901C4C | FULL | Range thresholds |
| PASS0_SAR1_CH17_INTR | 0x40901C50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH17_INTR_SET | 0x40901C54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH17_INTR_MASK | 0x40901C58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH17_INTR_MASKED | 0x40901C5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH17_WORK | 0x40901C60 | FULL | Working data register |
| PASS0_SAR1_CH17_RESULT | 0x40901C64 | FULL | Result data register |
| PASS0_SAR1_CH17_GRP_STAT | 0x40901C68 | FULL | Group status register |
| PASS0_SAR1_CH17_ENABLE | 0x40901C78 | FULL | Enable register |
| PASS0_SAR1_CH17_TR_CMD | 0x40901C7C | FULL | Software triggers |

19.2.19 CH 18

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH18_TR_CTL | 0x40901C80 | FULL | Trigger control. |
| PASS0_SAR1_CH18_SAMPLE_CTL | 0x40901C84 | FULL | Sample control. |
| PASS0_SAR1_CH18_POST_CTL | 0x40901C88 | FULL | Post processing control |
| PASS0_SAR1_CH18_RANGE_CTL | 0x40901C8C | FULL | Range thresholds |
| PASS0_SAR1_CH18_INTR | 0x40901C90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH18_INTR_SET | 0x40901C94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH18_INTR_MASK | 0x40901C98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH18_INTR_MASKED | 0x40901C9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH18_WORK | 0x40901CA0 | FULL | Working data register |
| PASS0_SAR1_CH18_RESULT | 0x40901CA4 | FULL | Result data register |
| PASS0_SAR1_CH18_GRP_STAT | 0x40901CA8 | FULL | Group status register |
| PASS0_SAR1_CH18_ENABLE | 0x40901CB8 | FULL | Enable register |
| PASS0_SAR1_CH18_TR_CMD | 0x40901CBC | FULL | Software triggers |

19.2.20 CH 19

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH19_TR_CTL | 0x40901CC0 | FULL | Trigger control. |
| PASS0_SAR1_CH19_SAMPLE_CTL | 0x40901CC4 | FULL | Sample control. |
| PASS0_SAR1_CH19_POST_CTL | 0x40901CC8 | FULL | Post processing control |
| PASS0_SAR1_CH19_RANGE_CTL | 0x40901CCC | FULL | Range thresholds |
| PASS0_SAR1_CH19_INTR | 0x40901CD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH19_INTR_SET | 0x40901CD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH19_INTR_MASK | 0x40901CD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH19_INTR_MASKED | 0x40901CDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH19_WORK | 0x40901CE0 | FULL | Working data register |
| PASS0_SAR1_CH19_RESULT | 0x40901CE4 | FULL | Result data register |
| PASS0_SAR1_CH19_GRP_STAT | 0x40901CE8 | FULL | Group status register |
| PASS0_SAR1_CH19_ENABLE | 0x40901CF8 | FULL | Enable register |
| PASS0_SAR1_CH19_TR_CMD | 0x40901CFC | FULL | Software triggers |

19.2.21 CH 20

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-------------------------|
| PASS0_SAR1_CH20_TR_CTL | 0x40901D00 | FULL | Trigger control. |
| PASS0_SAR1_CH20_SAMPLE_CTL | 0x40901D04 | FULL | Sample control. |
| PASS0_SAR1_CH20_POST_CTL | 0x40901D08 | FULL | Post processing control |
| PASS0_SAR1_CH20_RANGE_CTL | 0x40901D0C | FULL | Range thresholds |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH20_INTR | 0x40901D10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH20_INTR_SET | 0x40901D14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH20_INTR_MASK | 0x40901D18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH20_INTR_MASKED | 0x40901D1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH20_WORK | 0x40901D20 | FULL | Working data register |
| PASS0_SAR1_CH20_RESULT | 0x40901D24 | FULL | Result data register |
| PASS0_SAR1_CH20_GRP_STAT | 0x40901D28 | FULL | Group status register |
| PASS0_SAR1_CH20_ENABLE | 0x40901D38 | FULL | Enable register |
| PASS0_SAR1_CH20_TR_CMD | 0x40901D3C | FULL | Software triggers |

19.2.22 CH 21

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH21_TR_CTL | 0x40901D40 | FULL | Trigger control. |
| PASS0_SAR1_CH21_SAMPLE_CTL | 0x40901D44 | FULL | Sample control. |
| PASS0_SAR1_CH21_POST_CTL | 0x40901D48 | FULL | Post processing control |
| PASS0_SAR1_CH21_RANGE_CTL | 0x40901D4C | FULL | Range thresholds |
| PASS0_SAR1_CH21_INTR | 0x40901D50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH21_INTR_SET | 0x40901D54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH21_INTR_MASK | 0x40901D58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH21_INTR_MASKED | 0x40901D5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH21_WORK | 0x40901D60 | FULL | Working data register |
| PASS0_SAR1_CH21_RESULT | 0x40901D64 | FULL | Result data register |
| PASS0_SAR1_CH21_GRP_STAT | 0x40901D68 | FULL | Group status register |
| PASS0_SAR1_CH21_ENABLE | 0x40901D78 | FULL | Enable register |
| PASS0_SAR1_CH21_TR_CMD | 0x40901D7C | FULL | Software triggers |

19.2.23 CH 22

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH22_TR_CTL | 0x40901D80 | FULL | Trigger control. |
| PASS0_SAR1_CH22_SAMPLE_CTL | 0x40901D84 | FULL | Sample control. |
| PASS0_SAR1_CH22_POST_CTL | 0x40901D88 | FULL | Post processing control |
| PASS0_SAR1_CH22_RANGE_CTL | 0x40901D8C | FULL | Range thresholds |
| PASS0_SAR1_CH22_INTR | 0x40901D90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH22_INTR_SET | 0x40901D94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH22_INTR_MASK | 0x40901D98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH22_INTR_MASKED | 0x40901D9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH22_WORK | 0x40901DA0 | FULL | Working data register |
| PASS0_SAR1_CH22_RESULT | 0x40901DA4 | FULL | Result data register |
| PASS0_SAR1_CH22_GRP_STAT | 0x40901DA8 | FULL | Group status register |
| PASS0_SAR1_CH22_ENABLE | 0x40901DB8 | FULL | Enable register |
| PASS0_SAR1_CH22_TR_CMD | 0x40901DBC | FULL | Software triggers |

19.2.24 CH 23

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH23_TR_CTL | 0x40901DC0 | FULL | Trigger control. |
| PASS0_SAR1_CH23_SAMPLE_CTL | 0x40901DC4 | FULL | Sample control. |
| PASS0_SAR1_CH23_POST_CTL | 0x40901DC8 | FULL | Post processing control |
| PASS0_SAR1_CH23_RANGE_CTL | 0x40901DCC | FULL | Range thresholds |
| PASS0_SAR1_CH23_INTR | 0x40901DD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH23_INTR_SET | 0x40901DD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH23_INTR_MASK | 0x40901DD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH23_INTR_MASKED | 0x40901DDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH23_WORK | 0x40901DE0 | FULL | Working data register |
| PASS0_SAR1_CH23_RESULT | 0x40901DE4 | FULL | Result data register |
| PASS0_SAR1_CH23_GRP_STAT | 0x40901DE8 | FULL | Group status register |
| PASS0_SAR1_CH23_ENABLE | 0x40901DF8 | FULL | Enable register |
| PASS0_SAR1_CH23_TR_CMD | 0x40901DFC | FULL | Software triggers |

19.2.25 CH 24

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-------------------------|
| PASS0_SAR1_CH24_TR_CTL | 0x40901E00 | FULL | Trigger control. |
| PASS0_SAR1_CH24_SAMPLE_CTL | 0x40901E04 | FULL | Sample control. |
| PASS0_SAR1_CH24_POST_CTL | 0x40901E08 | FULL | Post processing control |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH24_RANGE_CTL | 0x40901E0C | FULL | Range thresholds |
| PASS0_SAR1_CH24_INTR | 0x40901E10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH24_INTR_SET | 0x40901E14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH24_INTR_MASK | 0x40901E18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH24_INTR_MASKED | 0x40901E1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH24_WORK | 0x40901E20 | FULL | Working data register |
| PASS0_SAR1_CH24_RESULT | 0x40901E24 | FULL | Result data register |
| PASS0_SAR1_CH24_GRP_STAT | 0x40901E28 | FULL | Group status register |
| PASS0_SAR1_CH24_ENABLE | 0x40901E38 | FULL | Enable register |
| PASS0_SAR1_CH24_TR_CMD | 0x40901E3C | FULL | Software triggers |

19.2.26 CH 25

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH25_TR_CTL | 0x40901E40 | FULL | Trigger control. |
| PASS0_SAR1_CH25_SAMPLE_CTL | 0x40901E44 | FULL | Sample control. |
| PASS0_SAR1_CH25_POST_CTL | 0x40901E48 | FULL | Post processing control |
| PASS0_SAR1_CH25_RANGE_CTL | 0x40901E4C | FULL | Range thresholds |
| PASS0_SAR1_CH25_INTR | 0x40901E50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH25_INTR_SET | 0x40901E54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH25_INTR_MASK | 0x40901E58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH25_INTR_MASKED | 0x40901E5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH25_WORK | 0x40901E60 | FULL | Working data register |
| PASS0_SAR1_CH25_RESULT | 0x40901E64 | FULL | Result data register |
| PASS0_SAR1_CH25_GRP_STAT | 0x40901E68 | FULL | Group status register |
| PASS0_SAR1_CH25_ENABLE | 0x40901E78 | FULL | Enable register |
| PASS0_SAR1_CH25_TR_CMD | 0x40901E7C | FULL | Software triggers |

19.2.27 CH 26

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH26_TR_CTL | 0x40901E80 | FULL | Trigger control. |
| PASS0_SAR1_CH26_SAMPLE_CTL | 0x40901E84 | FULL | Sample control. |
| PASS0_SAR1_CH26_POST_CTL | 0x40901E88 | FULL | Post processing control |
| PASS0_SAR1_CH26_RANGE_CTL | 0x40901E8C | FULL | Range thresholds |
| PASS0_SAR1_CH26_INTR | 0x40901E90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH26_INTR_SET | 0x40901E94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH26_INTR_MASK | 0x40901E98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH26_INTR_MASKED | 0x40901E9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH26_WORK | 0x40901EA0 | FULL | Working data register |
| PASS0_SAR1_CH26_RESULT | 0x40901EA4 | FULL | Result data register |
| PASS0_SAR1_CH26_GRP_STAT | 0x40901EA8 | FULL | Group status register |
| PASS0_SAR1_CH26_ENABLE | 0x40901EB8 | FULL | Enable register |
| PASS0_SAR1_CH26_TR_CMD | 0x40901EBC | FULL | Software triggers |

19.2.28 CH 27

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH27_TR_CTL | 0x40901EC0 | FULL | Trigger control. |
| PASS0_SAR1_CH27_SAMPLE_CTL | 0x40901EC4 | FULL | Sample control. |
| PASS0_SAR1_CH27_POST_CTL | 0x40901EC8 | FULL | Post processing control |
| PASS0_SAR1_CH27_RANGE_CTL | 0x40901ECC | FULL | Range thresholds |
| PASS0_SAR1_CH27_INTR | 0x40901ED0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH27_INTR_SET | 0x40901ED4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH27_INTR_MASK | 0x40901ED8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH27_INTR_MASKED | 0x40901EDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH27_WORK | 0x40901EE0 | FULL | Working data register |
| PASS0_SAR1_CH27_RESULT | 0x40901EE4 | FULL | Result data register |
| PASS0_SAR1_CH27_GRP_STAT | 0x40901EE8 | FULL | Group status register |
| PASS0_SAR1_CH27_ENABLE | 0x40901EF8 | FULL | Enable register |
| PASS0_SAR1_CH27_TR_CMD | 0x40901EFC | FULL | Software triggers |

19.2.29 CH 28

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|------------------|
| PASS0_SAR1_CH28_TR_CTL | 0x40901F00 | FULL | Trigger control. |
| PASS0_SAR1_CH28_SAMPLE_CTL | 0x40901F04 | FULL | Sample control. |

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH28_POST_CTL | 0x40901F08 | FULL | Post processing control |
| PASS0_SAR1_CH28_RANGE_CTL | 0x40901F0C | FULL | Range thresholds |
| PASS0_SAR1_CH28_INTR | 0x40901F10 | FULL | Interrupt request register. |
| PASS0_SAR1_CH28_INTR_SET | 0x40901F14 | FULL | Interrupt set request register |
| PASS0_SAR1_CH28_INTR_MASK | 0x40901F18 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH28_INTR_MASKED | 0x40901F1C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH28_WORK | 0x40901F20 | FULL | Working data register |
| PASS0_SAR1_CH28_RESULT | 0x40901F24 | FULL | Result data register |
| PASS0_SAR1_CH28_GRP_STAT | 0x40901F28 | FULL | Group status register |
| PASS0_SAR1_CH28_ENABLE | 0x40901F38 | FULL | Enable register |
| PASS0_SAR1_CH28_TR_CMD | 0x40901F3C | FULL | Software triggers |

19.2.30 CH 29

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH29_TR_CTL | 0x40901F40 | FULL | Trigger control. |
| PASS0_SAR1_CH29_SAMPLE_CTL | 0x40901F44 | FULL | Sample control. |
| PASS0_SAR1_CH29_POST_CTL | 0x40901F48 | FULL | Post processing control |
| PASS0_SAR1_CH29_RANGE_CTL | 0x40901F4C | FULL | Range thresholds |
| PASS0_SAR1_CH29_INTR | 0x40901F50 | FULL | Interrupt request register. |
| PASS0_SAR1_CH29_INTR_SET | 0x40901F54 | FULL | Interrupt set request register |
| PASS0_SAR1_CH29_INTR_MASK | 0x40901F58 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH29_INTR_MASKED | 0x40901F5C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH29_WORK | 0x40901F60 | FULL | Working data register |
| PASS0_SAR1_CH29_RESULT | 0x40901F64 | FULL | Result data register |
| PASS0_SAR1_CH29_GRP_STAT | 0x40901F68 | FULL | Group status register |
| PASS0_SAR1_CH29_ENABLE | 0x40901F78 | FULL | Enable register |
| PASS0_SAR1_CH29_TR_CMD | 0x40901F7C | FULL | Software triggers |

19.2.31 CH 30

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH30_TR_CTL | 0x40901F80 | FULL | Trigger control. |
| PASS0_SAR1_CH30_SAMPLE_CTL | 0x40901F84 | FULL | Sample control. |
| PASS0_SAR1_CH30_POST_CTL | 0x40901F88 | FULL | Post processing control |
| PASS0_SAR1_CH30_RANGE_CTL | 0x40901F8C | FULL | Range thresholds |
| PASS0_SAR1_CH30_INTR | 0x40901F90 | FULL | Interrupt request register. |
| PASS0_SAR1_CH30_INTR_SET | 0x40901F94 | FULL | Interrupt set request register |
| PASS0_SAR1_CH30_INTR_MASK | 0x40901F98 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH30_INTR_MASKED | 0x40901F9C | FULL | Interrupt masked request register |
| PASS0_SAR1_CH30_WORK | 0x40901FA0 | FULL | Working data register |
| PASS0_SAR1_CH30_RESULT | 0x40901FA4 | FULL | Result data register |
| PASS0_SAR1_CH30_GRP_STAT | 0x40901FA8 | FULL | Group status register |
| PASS0_SAR1_CH30_ENABLE | 0x40901FB8 | FULL | Enable register |
| PASS0_SAR1_CH30_TR_CMD | 0x40901FBC | FULL | Software triggers |

19.2.32 CH 31

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR1_CH31_TR_CTL | 0x40901FC0 | FULL | Trigger control. |
| PASS0_SAR1_CH31_SAMPLE_CTL | 0x40901FC4 | FULL | Sample control. |
| PASS0_SAR1_CH31_POST_CTL | 0x40901FC8 | FULL | Post processing control |
| PASS0_SAR1_CH31_RANGE_CTL | 0x40901FCC | FULL | Range thresholds |
| PASS0_SAR1_CH31_INTR | 0x40901FD0 | FULL | Interrupt request register. |
| PASS0_SAR1_CH31_INTR_SET | 0x40901FD4 | FULL | Interrupt set request register |
| PASS0_SAR1_CH31_INTR_MASK | 0x40901FD8 | FULL | Interrupt mask register. |
| PASS0_SAR1_CH31_INTR_MASKED | 0x40901FDC | FULL | Interrupt masked request register |
| PASS0_SAR1_CH31_WORK | 0x40901FE0 | FULL | Working data register |
| PASS0_SAR1_CH31_RESULT | 0x40901FE4 | FULL | Result data register |
| PASS0_SAR1_CH31_GRP_STAT | 0x40901FE8 | FULL | Group status register |
| PASS0_SAR1_CH31_ENABLE | 0x40901FF8 | FULL | Enable register |
| PASS0_SAR1_CH31_TR_CMD | 0x40901FFC | FULL | Software triggers |

19.3 SAR 2

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|---|
| PASS0_SAR2_CTL | 0x40902000 | FULL | Analog control register. |
| PASS0_SAR2_DIAG_CTL | 0x40902004 | FULL | Diagnostic Reference control register. |
| PASS0_SAR2_PRECOND_CTL | 0x40902010 | FULL | Preconditioning control register. |
| PASS0_SAR2_ANA_CAL | 0x40902080 | FULL | Current analog calibration values |
| PASS0_SAR2_DIG_CAL | 0x40902084 | FULL | Current digital calibration values |
| PASS0_SAR2_ANA_CAL_ALT | 0x40902090 | FULL | Alternate analog calibration values |
| PASS0_SAR2_DIG_CAL_ALT | 0x40902094 | FULL | Alternate digital calibration values |
| PASS0_SAR2_CAL_UPD_CMD | 0x40902098 | FULL | Calibration update command |
| PASS0_SAR2_TR_PEND | 0x40902100 | FULL | Trigger pending status |
| PASS0_SAR2_WORK_VALID | 0x40902180 | FULL | Channel working data register 'valid' bits |
| PASS0_SAR2_WORK_RANGE | 0x40902184 | FULL | Range detected |
| PASS0_SAR2_WORK_RANGE_HI | 0x40902188 | FULL | Range detect above Hi flag |
| PASS0_SAR2_WORK_PULSE | 0x4090218C | FULL | Pulse detected |
| PASS0_SAR2_RESULT_VALID | 0x409021A0 | FULL | Channel result data register 'valid' bits |
| PASS0_SAR2_RESULT_RANGE_HI | 0x409021A4 | FULL | Channel Range above Hi flags |
| PASS0_SAR2_STATUS | 0x40902200 | FULL | Current status of internal SAR registers (mostly for debug) |
| PASS0_SAR2_AVG_STAT | 0x40902204 | FULL | Current averaging status (for debug) |

19.3.1 CH 0

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH0_TR_CTL | 0x40902800 | FULL | Trigger control. |
| PASS0_SAR2_CH0_SAMPLE_CTL | 0x40902804 | FULL | Sample control. |
| PASS0_SAR2_CH0_POST_CTL | 0x40902808 | FULL | Post processing control |
| PASS0_SAR2_CH0_RANGE_CTL | 0x4090280C | FULL | Range thresholds |
| PASS0_SAR2_CH0_INTR | 0x40902810 | FULL | Interrupt request register. |
| PASS0_SAR2_CH0_INTR_SET | 0x40902814 | FULL | Interrupt set request register |
| PASS0_SAR2_CH0_INTR_MASK | 0x40902818 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH0_INTR_MASKED | 0x4090281C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH0_WORK | 0x40902820 | FULL | Working data register |
| PASS0_SAR2_CH0_RESULT | 0x40902824 | FULL | Result data register |
| PASS0_SAR2_CH0_GRP_STAT | 0x40902828 | FULL | Group status register |
| PASS0_SAR2_CH0_ENABLE | 0x40902838 | FULL | Enable register |
| PASS0_SAR2_CH0_TR_CMD | 0x4090283C | FULL | Software triggers |

19.3.2 CH 1

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH1_TR_CTL | 0x40902840 | FULL | Trigger control. |
| PASS0_SAR2_CH1_SAMPLE_CTL | 0x40902844 | FULL | Sample control. |
| PASS0_SAR2_CH1_POST_CTL | 0x40902848 | FULL | Post processing control |
| PASS0_SAR2_CH1_RANGE_CTL | 0x4090284C | FULL | Range thresholds |
| PASS0_SAR2_CH1_INTR | 0x40902850 | FULL | Interrupt request register. |
| PASS0_SAR2_CH1_INTR_SET | 0x40902854 | FULL | Interrupt set request register |
| PASS0_SAR2_CH1_INTR_MASK | 0x40902858 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH1_INTR_MASKED | 0x4090285C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH1_WORK | 0x40902860 | FULL | Working data register |
| PASS0_SAR2_CH1_RESULT | 0x40902864 | FULL | Result data register |
| PASS0_SAR2_CH1_GRP_STAT | 0x40902868 | FULL | Group status register |
| PASS0_SAR2_CH1_ENABLE | 0x40902878 | FULL | Enable register |
| PASS0_SAR2_CH1_TR_CMD | 0x4090287C | FULL | Software triggers |

19.3.3 CH 2

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH2_TR_CTL | 0x40902880 | FULL | Trigger control. |
| PASS0_SAR2_CH2_SAMPLE_CTL | 0x40902884 | FULL | Sample control. |
| PASS0_SAR2_CH2_POST_CTL | 0x40902888 | FULL | Post processing control |
| PASS0_SAR2_CH2_RANGE_CTL | 0x4090288C | FULL | Range thresholds |
| PASS0_SAR2_CH2_INTR | 0x40902890 | FULL | Interrupt request register. |
| PASS0_SAR2_CH2_INTR_SET | 0x40902894 | FULL | Interrupt set request register |
| PASS0_SAR2_CH2_INTR_MASK | 0x40902898 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH2_INTR_MASKED | 0x4090289C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH2_WORK | 0x409028A0 | FULL | Working data register |
| PASS0_SAR2_CH2_RESULT | 0x409028A4 | FULL | Result data register |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------|
| PASS0_SAR2_CH2_GRP_STAT | 0x409028A8 | FULL | Group status register |
| PASS0_SAR2_CH2_ENABLE | 0x409028B8 | FULL | Enable register |
| PASS0_SAR2_CH2_TR_CMD | 0x409028BC | FULL | Software triggers |

19.3.4 CH 3

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH3_TR_CTL | 0x409028C0 | FULL | Trigger control. |
| PASS0_SAR2_CH3_SAMPLE_CTL | 0x409028C4 | FULL | Sample control. |
| PASS0_SAR2_CH3_POST_CTL | 0x409028C8 | FULL | Post processing control |
| PASS0_SAR2_CH3_RANGE_CTL | 0x409028CC | FULL | Range thresholds |
| PASS0_SAR2_CH3_INTR | 0x409028D0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH3_INTR_SET | 0x409028D4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH3_INTR_MASK | 0x409028D8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH3_INTR_MASKED | 0x409028DC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH3_WORK | 0x409028E0 | FULL | Working data register |
| PASS0_SAR2_CH3_RESULT | 0x409028E4 | FULL | Result data register |
| PASS0_SAR2_CH3_GRP_STAT | 0x409028E8 | FULL | Group status register |
| PASS0_SAR2_CH3_ENABLE | 0x409028F8 | FULL | Enable register |
| PASS0_SAR2_CH3_TR_CMD | 0x409028FC | FULL | Software triggers |

19.3.5 CH 4

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH4_TR_CTL | 0x40902900 | FULL | Trigger control. |
| PASS0_SAR2_CH4_SAMPLE_CTL | 0x40902904 | FULL | Sample control. |
| PASS0_SAR2_CH4_POST_CTL | 0x40902908 | FULL | Post processing control |
| PASS0_SAR2_CH4_RANGE_CTL | 0x4090290C | FULL | Range thresholds |
| PASS0_SAR2_CH4_INTR | 0x40902910 | FULL | Interrupt request register. |
| PASS0_SAR2_CH4_INTR_SET | 0x40902914 | FULL | Interrupt set request register |
| PASS0_SAR2_CH4_INTR_MASK | 0x40902918 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH4_INTR_MASKED | 0x4090291C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH4_WORK | 0x40902920 | FULL | Working data register |
| PASS0_SAR2_CH4_RESULT | 0x40902924 | FULL | Result data register |
| PASS0_SAR2_CH4_GRP_STAT | 0x40902928 | FULL | Group status register |
| PASS0_SAR2_CH4_ENABLE | 0x40902938 | FULL | Enable register |
| PASS0_SAR2_CH4_TR_CMD | 0x4090293C | FULL | Software triggers |

19.3.6 CH 5

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH5_TR_CTL | 0x40902940 | FULL | Trigger control. |
| PASS0_SAR2_CH5_SAMPLE_CTL | 0x40902944 | FULL | Sample control. |
| PASS0_SAR2_CH5_POST_CTL | 0x40902948 | FULL | Post processing control |
| PASS0_SAR2_CH5_RANGE_CTL | 0x4090294C | FULL | Range thresholds |
| PASS0_SAR2_CH5_INTR | 0x40902950 | FULL | Interrupt request register. |
| PASS0_SAR2_CH5_INTR_SET | 0x40902954 | FULL | Interrupt set request register |
| PASS0_SAR2_CH5_INTR_MASK | 0x40902958 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH5_INTR_MASKED | 0x4090295C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH5_WORK | 0x40902960 | FULL | Working data register |
| PASS0_SAR2_CH5_RESULT | 0x40902964 | FULL | Result data register |
| PASS0_SAR2_CH5_GRP_STAT | 0x40902968 | FULL | Group status register |
| PASS0_SAR2_CH5_ENABLE | 0x40902978 | FULL | Enable register |
| PASS0_SAR2_CH5_TR_CMD | 0x4090297C | FULL | Software triggers |

19.3.7 CH 6

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH6_TR_CTL | 0x40902980 | FULL | Trigger control. |
| PASS0_SAR2_CH6_SAMPLE_CTL | 0x40902984 | FULL | Sample control. |
| PASS0_SAR2_CH6_POST_CTL | 0x40902988 | FULL | Post processing control |
| PASS0_SAR2_CH6_RANGE_CTL | 0x4090298C | FULL | Range thresholds |
| PASS0_SAR2_CH6_INTR | 0x40902990 | FULL | Interrupt request register. |
| PASS0_SAR2_CH6_INTR_SET | 0x40902994 | FULL | Interrupt set request register |
| PASS0_SAR2_CH6_INTR_MASK | 0x40902998 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH6_INTR_MASKED | 0x4090299C | FULL | Interrupt masked request register |
| PASS0_SAR2_CH6_WORK | 0x409029A0 | FULL | Working data register |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------|
| PASS0_SAR2_CH6_RESULT | 0x409029A4 | FULL | Result data register |
| PASS0_SAR2_CH6_GRP_STAT | 0x409029A8 | FULL | Group status register |
| PASS0_SAR2_CH6_ENABLE | 0x409029B8 | FULL | Enable register |
| PASS0_SAR2_CH6_TR_CMD | 0x409029BC | FULL | Software triggers |

19.3.8 CH 7

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|-----------------------------------|
| PASS0_SAR2_CH7_TR_CTL | 0x409029C0 | FULL | Trigger control. |
| PASS0_SAR2_CH7_SAMPLE_CTL | 0x409029C4 | FULL | Sample control. |
| PASS0_SAR2_CH7_POST_CTL | 0x409029C8 | FULL | Post processing control |
| PASS0_SAR2_CH7_RANGE_CTL | 0x409029CC | FULL | Range thresholds |
| PASS0_SAR2_CH7_INTR | 0x409029D0 | FULL | Interrupt request register. |
| PASS0_SAR2_CH7_INTR_SET | 0x409029D4 | FULL | Interrupt set request register |
| PASS0_SAR2_CH7_INTR_MASK | 0x409029D8 | FULL | Interrupt mask register. |
| PASS0_SAR2_CH7_INTR_MASKED | 0x409029DC | FULL | Interrupt masked request register |
| PASS0_SAR2_CH7_WORK | 0x409029E0 | FULL | Working data register |
| PASS0_SAR2_CH7_RESULT | 0x409029E4 | FULL | Result data register |
| PASS0_SAR2_CH7_GRP_STAT | 0x409029E8 | FULL | Group status register |
| PASS0_SAR2_CH7_ENABLE | 0x409029F8 | FULL | Enable register |
| PASS0_SAR2_CH7_TR_CMD | 0x409029FC | FULL | Software triggers |

19.4 EPASS_MMIO

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---------------------------------------|
| PASS0_PASS_CTL | 0x409F0000 | FULL | PASS control register |
| PASS0_SAR_TR_IN_SEL0 | 0x409F0020 | FULL | per SAR generic input trigger select |
| PASS0_SAR_TR_IN_SEL1 | 0x409F0024 | FULL | per SAR generic input trigger select |
| PASS0_SAR_TR_IN_SEL2 | 0x409F0028 | FULL | per SAR generic input trigger select |
| PASS0_SAR_TR_OUT_SEL0 | 0x409F0040 | FULL | per SAR generic output trigger select |
| PASS0_SAR_TR_OUT_SEL1 | 0x409F0044 | FULL | per SAR generic output trigger select |
| PASS0_SAR_TR_OUT_SEL2 | 0x409F0048 | FULL | per SAR generic output trigger select |
| PASS0_TEST_CTL | 0x409F0080 | FULL | Test control bits |

19.5 Register Details

19.5.1 SAR

19.5.1.1 PASS_SAR_CTL

Description: Analog control register.
Address: 0x40900000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|---|---|---|---|---|---|
| Name | PWRUP_TIME [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|------------------|-------------------|-------------------|
| Name | None [15:11] | | | | | HALF_LSB [10:10] | MSB_STRETCH [9:9] | IDLE_PWRDWN [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----------------|-------------------|--------------|----|----|----|----|
| Name | ENABLED [31:31] | ADC_EN [30:30] | SARMUX_EN [29:29] | None [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:7 | PWRUP_TIME | RW | R | 0 | Number cycles to wait to power up after IDLE_PWRDWN. Check the STATUS.PWRUP_BUSY flag to see if the delay is still in progress. The power up delay is 1 us. |
| 8 | IDLE_PWRDWN | RW | R | 0 | When idle automatically power down the analog. After an automatic power down a new trigger will power up the analog, however it will take PWRUP_TIME cycles before the first acquisition can be started. Note that re-arbitration happens at that time, i.e. the trigger that caused the power up may not get handled first. |
| 9 | MSB_STRETCH | RW | R | 0 | When set use 2 cycles for the Most Significant Bit (MSB) - 0: Use 1 clock cycle for MSB - 1: Use 2 clock cycles for MSB |
| 10 | HALF_LSB | RW | R | 0 | When set take an extra cycle to convert the half LSB and add it to 12-bit result for Missing Code Recovery. This bit should always be set to '1' - 0: disable half LSB conversion (not recommended) - 1: enable half LSB conversion |
| 29 | SARMUX_EN | RW | R | 0 | Enable the SARMUX (only valid if ENABLED=1) - 0: SARMUX disabled (put analog in power down) - 1: SARMUX enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 30 | ADC_EN | RW | R | 0 | Enable the SAR ADC and SAR sequencer (only valid if ENABLED=1) - 0: SARADC and SARSEQ are disabled (put SARADC analog in power down and stop clocks), also clears all pending triggers. - 1: SAR ADC and SARSEQ are enabled. To enable ADC0 to borrow SARMUX1-3 the corresponding ADC_EN must be set to 0. |
| 31 | ENABLED | RW | R | 0 | - 0: SAR IP disabled (put analog in power down and stop clocks), also clears all pending triggers. - 1: SAR IP enabled. |

19.5.1.2 PASS_SAR_DIAG_CTL

Description: Diagnostic Reference control register.
Address: 0x40900004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------------|---|---|---|
| Name | None [7:4] | | | | DIAG_SEL [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|----|----|----|----|
| Name | DIAG_EN [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:3 | DIAG_SEL | RW | R | 0 | Select Diagnostic Reference function |
| | VREFL | | | 0 | DiagOut = VrefL |
| | VREFH_1DIV8 | | | 1 | DiagOut = VrefH * 1/8 |
| | VREFH_2DIV8 | | | 2 | DiagOut = VrefH * 2/8 |
| | VREFH_3DIV8 | | | 3 | DiagOut = VrefH * 3/8 |
| | VREFH_4DIV8 | | | 4 | DiagOut = VrefH * 4/8 |
| | VREFH_5DIV8 | | | 5 | DiagOut = VrefH * 5/8 |
| | VREFH_6DIV8 | | | 6 | DiagOut = VrefH * 6/8 |
| | VREFH_7DIV8 | | | 7 | DiagOut = VrefH * 7/8 |
| | VREFH | | | 8 | DiagOut = VrefH |
| | VREFX | | | 9 | DiagOut = VrefX = VrefH * 199/200 |
| | VBG | | | 10 | DiagOut = Vbg from SRSS |
| | VIN1 | | | 11 | DiagOut = Vin1 |
| | VIN2 | | | 12 | DiagOut = Vin2 |
| | VIN3 | | | 13 | DiagOut = Vin3 |
| | I_SOURCE | | | 14 | DiagOut = Isource (10uA) |
| | I_SINK | | | 15 | DiagOut = Isink (10uA) |
| 31 | DIAG_EN | RW | R | 0 | Diagnostic Reference enable (only valid if ENABLED=1) - 0: Diagnostic Reference disabled (powered down resistor ladder and current mirrors, DiagOut = Vssa). - 1: Diagnostic Reference enabled, output signal select according to DIAG_SEL (note also EPASS_MMIO.PASS_CTL.REFBUF_EN must be set). |

19.5.1.3 PASS_SAR_PRECOND_CTL

Description: Preconditioning control register.
Address: 0x40900010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Precondition time value used when a channel enables preconditioning (PRECOND_MODE)
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------------|---|---|---|
| Name | None [7:4] | | | | PRECOND_TIME [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:3 | PRECOND_TIME | RW | R | 0 | Number ADC clock cycles that Preconditioning is done before the sample window starts. If OVERLAP_EN=0 there will be 1 additional break before make cycle between preconditioning and sampling. Note that the minimum value is 1 (0 gives the same result as 1). |

19.5.1.4 PASS_SAR_ANA_CAL

Description: Current analog calibration values
Address: 0x40900080
Offset: 0x80
Retention: Retained
IsDeepSleep: No
Comment: Hardware can update this register if software sets the CAL_UPD_CMD.UPDATE
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | AOFFSET [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|---------------|----|----|----|
| Name | None [23:21] | | | | AGAIN [20:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|--------------------------|
| 0:7 | AOFFSET | RW | RW | 0 | Analog offset correction |
| 16:20 | AGAIN | RW | RW | 0 | Analog gain correction |

19.5.1.5 PASS_SAR_DIG_CAL

Description: Current digital calibration values
Address: 0x40900084
Offset: 0x84
Retention: Retained
IsDeepSleep: No
Comment: Hardware can update this register if software sets the CAL_UPD_CMD.UPDATE
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|---------------|----|----------------|----|----|----|
| Name | DOFFSET [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | DOFFSET [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:22] | | DGAIN [21:16] | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|---|
| 0:11 | DOFFSET | RW | RW | 0 | Digital offset correction Subtract DOFFSET from ADC output. |
| 16:21 | DGAIN | RW | RW | 0 | Digital gain correction. Signed value to correct +/- 30 codes for the maximum input voltage. Corrected = (D - DOFFSET) + ((D - DOFFSET) * DGAIN + 0x800) / 0x1000 |

19.5.1.6 PASS_SAR_ANA_CAL_ALT

Description: Alternate analog calibration values
Address: 0x40900090
Offset: 0x90
Retention: Retained
IsDeepSleep: No
Comment: Also known as 'shadow' calibration registers to enable background calibration
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | AOFFSET [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|---------------|----|----|----|----|
| Name | None [23:21] | | | AGAIN [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|---------------------------------|
| 0:7 | AOFFSET | RW | R | 0 | See corresponding ANA_CAL field |
| 16:20 | AGAIN | RW | R | 0 | See corresponding ANA_CAL field |

19.5.1.7 PASS_SAR_DIG_CAL_ALT

Description: Alternate digital calibration values
Address: 0x40900094
Offset: 0x94
Retention: Retained
IsDeepSleep: No
Comment: First use analog calibration to avoid saturation for the required input voltage range. Then use this digital calibration to map codes on full 12-bit range.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|---------------|----|----------------|----|----|----|
| Name | DOFFSET [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | DOFFSET [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:22] | | DGAIN [21:16] | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|---------------------------------|
| 0:11 | DOFFSET | RW | R | 0 | See corresponding DIG_CAL field |
| 16:21 | DGAIN | RW | R | 0 | See corresponding DIG_CAL field |

19.5.1.8 PASS_SAR_CAL_UPD_CMD

Description: Calibration update command
Address: 0x40900098
Offset: 0x98
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|--------------|
| Name | None [7:1] | | | | | | | UPDATE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|------|-----------------|---|
| 0 | UPDATE | RW | RW1C | 0 | <p>Calibration update command: coherently copy values from alternate calibration regs to current calibration regs.</p> <p>Software sets this bit when the alternate calibration values have been set with the new values. Hardware will do the calibration update as soon as the ADC is idle or a 'continuous' triggered group completes. This ensures that all acquisitions within a group scan (even if preempted) are done with the same calibration values.</p> <p>This bit is cleared at the same time the calibration update is done. By clearing this bit software can cancel a requested update.</p> <p>Note: if the ADC is always busy with acquisitions for non continuously triggered groups/channels then the calibration update will remain pending forever. In such a case the software can either do a non coherent update by writing directly to the current calibration registers, or software can force the ADC to idle by disabling some or all channels.</p> <p>Software can check/poll this bit to see if the calibration update has taken effect.</p> |

19.5.1.9 PASS_SAR_TR_PEND

Description: Trigger pending status
Address: 0x40900100
Offset: 0x100
Retention: Not Retained
IsDeepSleep: No
Comment: Status
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | TR_PEND [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | TR_PEND [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | TR_PEND [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | TR_PEND [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:31 | TR_PEND | R | W | 0 | Trigger Pending. Hardware will set this bit if a hardware trigger is received. |

19.5.1.10 PASS_SAR_WORK_VALID

Description: Channel working data register 'valid' bits
Address: 0x40900180
Offset: 0x180
Retention: Not Retained
IsDeepSleep: No
Comment: bits of disabled channels will be reset
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|---|---|---|---|---|---|
| Name | WORK_VALID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------------|----|----|----|----|----|---|---|
| Name | WORK_VALID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | WORK_VALID [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | WORK_VALID [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:31 | WORK_VALID | R | RW | 0 | If set the corresponding WORK register is valid, i.e. was already acquired during the current group scan. If this bit is low then either the channel is not enabled, not yet acquired or it is used as a pulse detect channel. |

19.5.1.11 PASS_SAR_WORK_RANGE

Description: Range detected
Address: 0x40900184
Offset: 0x184
Retention: Not Retained
IsDeepSleep: No
Comment: bits of disabled channels will be reset
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | RANGE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | RANGE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | RANGE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | RANGE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | RANGE | R | RW | 0 | N/A |

19.5.1.12 PASS_SAR_WORK_RANGE_HI

Description: Range detect above Hi flag
Address: 0x40900188
Offset: 0x188
Retention: Not Retained
IsDeepSleep: No
Comment: bits of disabled channels will be reset
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | ABOVE_HI [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | ABOVE_HI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | ABOVE_HI [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | ABOVE_HI [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:31 | ABOVE_HI | R | RW | 0 | Out of range was detected and the value was above the Hi threshold |

19.5.1.13 PASS_SAR_WORK_PULSE

Description: Pulse detected
Address: 0x4090018C
Offset: 0x18C
Retention: Not Retained
IsDeepSleep: No
Comment: bits of disabled channels will be reset
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | PULSE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | PULSE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | PULSE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | PULSE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | PULSE | R | RW | 0 | N/A |

19.5.1.14 PASS_SAR_RESULT_VALID

Description: Channel result data register 'valid' bits
Address: 0x409001A0
Offset: 0x1A0
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | RESULT_VALID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | RESULT_VALID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | RESULT_VALID [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | RESULT_VALID [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:31 | RESULT_VALID | R | RW | 0 | If set the corresponding RESULT register is valid, i.e. was acquired during the preceding group scan. If this bit is low, after a group scan completed, then either the channel is not enabled or is used as a pulse detect channel. |

19.5.1.15 PASS_SAR_RESULT_RANGE_HI

Description: Channel Range above Hi flags
Address: 0x409001A4
Offset: 0x1A4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | ABOVE_HI [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | ABOVE_HI [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | ABOVE_HI [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | ABOVE_HI [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:31 | ABOVE_HI | R | RW | 0 | Out of range was detected and the value was above the Hi threshold |

19.5.1.16 PASS_SAR_STATUS

Description: Current status of internal SAR registers (mostly for debug)
Address: 0x40900200
Offset: 0x200
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|---|---|---|---|
| Name | None [7:5] | | | CUR_CHAN [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|--------------------------|----|--------------|-----------------|---|---|
| Name | None [15:14] | | CUR_PREEMPT_TYPE [13:12] | | None [11:11] | CUR_PRIO [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------------|--------------------|--------------|----|----|----|----|
| Name | BUSY [31:31] | PWRUP_BUSY [30:30] | DBG_FREEZE [29:29] | None [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------------|----|----|-----------------|---|
| 0:4 | CUR_CHAN | R | W | 0 | current channel being acquired, only valid if BUSY. |
| 8:10 | CUR_PRIO | R | W | 0 | priority of current group/channel, only valid if BUSY. |
| 12:13 | CUR_PREEMPT_TYPE | R | W | 0 | Preempting type of current group/channel, only valid if BUSY. |
| 29 | DBG_FREEZE | R | W | 0 | If high then the SAR is prevented from starting a new acquisition, see DBG_FREEZE_EN. |
| 30 | PWRUP_BUSY | R | W | 0 | If high then the SAR is waiting for PWRUP_TIME due to IDLE_PWRDWN |
| 31 | BUSY | R | W | 0 | If high then the SAR is busy with a conversion. |

19.5.1.17 PASS_SAR_AVG_STAT

Description: Current averaging status (for debug)
Address: 0x40900204
Offset: 0x204
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----------------------|----|----|----|
| Name | CUR_AVG_ACCU [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CUR_AVG_ACCU [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | CUR_AVG_ACCU [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CUR_AVG_CNT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0:19 | CUR_AVG_ACCU | R | W | 0 | the current value of the averaging accumulator |
| 24:31 | CUR_AVG_CNT | R | W | 0 | the current value of the averaging counter. Note that the value shown is updated after the sample window and therefore runs ahead of the accumulator update. |

19.5.1.18 CH

19.5.1.18.1 PASS_SAR_CH_TR_CTL

Description: Trigger control.
Address: 0x40900800
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Make sure the channel or the IP is disabled before changing this register
Default: 0x800

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|---|---|------------|-----------|---|---|
| Name | None [7:7] | PRIO [6:4] | | | None [3:3] | SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-------------------|--------------|--------------------|---|
| Name | None [15:12] | | | | GROUP_END [11:11] | None [10:10] | PREEMPT_TYPE [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------|--------------|----|----|----|----|----|----|
| Name | DONE_LEVEL [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:2 | SEL | RW | R | 0 | Trigger select |
| | OFF | | | 0 | Use for channels in group, except the first channel |
| | TCPWM | | | 1 | Trigger from corresponding TCPWM channel |
| | GENERIC0 | | | 2 | Generic trigger input 0 |
| | GENERIC1 | | | 3 | N/A |
| | GENERIC2 | | | 4 | N/A |
| | GENERIC3 | | | 5 | N/A |
| | GENERIC4 | | | 6 | N/A |
| 4:6 | CONTINUOUS | | | 7 | Always triggered (also called idle), can only be used for at most 1 channel |
| | PRIO | RW | R | 0 | Channel priority: '0': highest priority. '1' ... '6' '7': lowest priority. Channels with the same priority constitute a priority level. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority level with pending channels is identified. Second, within this priority level, round robin arbitration is applied. Round robin arbitration (within a priority level) gives the highest priority to the lower channel indices (within the priority level). |
| 8:9 | PREEMPT_TYPE | RW | R | 0 | Preemption type allow for this group |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| | ABORT_CANCEL | | | 0 | <p>Abort ongoing acquisition, do not return Clear pending trigger for aborted group and set Cancelled interrupt.</p> <p>Also 'Abort' whenever this group (do not pend the trigger) is not immediately scheduled for acquisition after a new trigger arrives.</p> <p>For this preemption type only, only a positive edge on the trigger can trigger the channel, i.e. CONTINUOUS or level high operation is not supported (to avoid continuous Cancelled interrupts).</p> <p>In case CTL.IDLE_PWRDWN is used and the analog is powered down, the group cannot be immediately scheduled for acquisition and therefore a trigger for a group with this preemption type will power up the analog, but the group will ABORT and set the Cancelled interrupt</p> |
| | ABORT_RESTART | | | 1 | Abort ongoing acquisition, up on return Restart group from first channel. |
| | ABORT_RESUME | | | 2 | <p>Abort ongoing acquisition, up on return Resume group from aborted channel</p> <p>If averaging, discard averaging results so far and restart averaging.</p> |
| | FINISH_RESUME | | | 3 | Complete ongoing acquisition (including averaging), up on return Resume group from next channel |
| 11 | GROUP_END | RW | R | 1 | <p>0: continue group with next channel 1: last channel of a group.</p> <p>Note that for the channel with the highest index (SAR_CH_NR) this always needs to be set</p> |
| 31 | DONE_LEVEL | RW | R | 0 | <p>select level or pulse for 'tr_ch_done' trigger output Also see POST_CTL.TR_DONE_GRP_VIO</p> |
| | PULSE | | | 0 | tr_ch_done generates a 2 cycle pulse (clk_sys), no need to read the result to clear (also no ch_overflow detection) |
| | LEVEL | | | 1 | tr_ch_done is a level output until the result register is read (typical for DW usage, this also enables ch_overflow detection when DW is too slow) |

19.5.1.18.2 PASS_SAR_CH_SAMPLE_CTL

Description: Sample control.
Address: 0x40900804
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: Make sure the channel or the IP is disabled before changing this register
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|----------------|---|---|---|---|---|
| Name | PORT_ADDR [7:6] | | PIN_ADDR [5:0] | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------------|----|----------------------|----|--------------------|--------------------|---|---|
| Name | OVERLAP_DIAG [15:14] | | PRECOND_MODE [13:12] | | EXT_MUX_EN [11:11] | EXT_MUX_SEL [10:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | SAMPLE_TIME [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|----|---------------------|----|----|----|
| Name | ALT_CAL [31:31] | None [30:28] | | | SAMPLE_TIME [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:5 | PIN_ADDR | RW | R | Undefined | <p>Address of the analog signal (pin) to be sampled by this channel</p> <ul style="list-style-type: none"> - 0..31 : Vout = AN0..31, select corresponding analog input - 32: Vout = Vmotor, select motor input - 33: Vout = Vaux, select auxiliary input - 34: Vout = AmuxbusA - 35: Vout = AmuxbusB - 36: Vout = Vccd - 37: Vout = Vdda - 38: Vout = Vbg, Bandgap voltage from SRSS - 39: Vout = Vtemp, select temperature sensor. Make sure that only 1 ADC is allowed to use this. - 40..61: Vout = undefined, reserved for future products - 62: Vout = VrefL (VrefL actually bypasses the SARMUX (XSL)) - 63: Vout = VrefH (VrefH actually bypasses the SARMUX (XSH)) <p>Note: When PORT_ADDR is not set to SARMUX0, pin addresses from 32-63 are not available. Only addresses 0-31 can be accessed from SARMUX1-3</p> |
| 6:7 | PORT_ADDR | RW | R | Undefined | <p>Select the physical port. This field is only valid for ADC0.</p> <p>ADC0 can control and connect to the SARMUX of the neighboring ADC1-3. This requires the corresponding ADC to be off while the SARMUX is left on.</p> <p>When ADC0 controls another SARMUX it uses the PIN_ADDR, EXT_MUX_EN/SEL of this channel to control the other SARMUX.</p> |
| | SARMUX0 | | | 0 | ADC uses it's own SARMUX |
| | SARMUX1 | | | 1 | ADC0 uses SARMUX1 (only valid for ADC0, undefined result if used for ADC1-3) |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| | SARMUX2 | | | 2 | ADC0 uses SARMUX2 (only valid for ADC0, undefined result if used for ADC1-3) |
| | SARMUX3 | | | 3 | ADC0 uses SARMUX3 (only valid for ADC0, undefined result if used for ADC1-3) |
| 8:10 | EXT_MUX_SEL | RW | R | Undefined | External analog mux select. This bit setting is related to EXT_MUX[x]_y on pin assignment. 0x0: Select EXT_MUX[x]_0 pin 0x1: Select EXT_MUX[x]_1 pin |
| 11 | EXT_MUX_EN | RW | R | Undefined | External analog mux enable. This enable can be used as enable (chip select) for the external analog mux (this enable is not used as enable for the GPIO output driver). This enable also prevents unnecessary toggle activity on the select signals of the external analog mux. When this enable is low EXT_MUX_SEL value will be ignored and the previous value will be maintained. Note that an external analog mux can only be used in combination with a pin input, i.e. PIN_ADDR<32 or Vmotor. If an internal signal is selected this enable should be 0. |
| 12:13 | PRECOND_MODE | RW | R | Undefined | Select preconditioning mode. Preconditioning (dis)charges the SAR sample capacitor to the selected reference voltage for PRECOND_TIME (global) cycles, a break before make cycle will be inserted before sampling starts (SAMPLE_TIME). |
| | OFF | | | 0 | No preconditioning |
| | VREFL | | | 1 | Discharge to VREFL |
| | VREFH | | | 2 | Charge to VREFH |
| | DIAG | | | 3 | Connect the Diagnostic reference output during preconditioning. The Diagnostic reference should be configured to output a reference voltage. Note: this selection is mutual exclusive with using the Diagnostic reference to supply an ibias current for OVERLAP. |
| 14:15 | OVERLAP_DIAG | RW | R | Undefined | Select Overlap mode or SARMUX Diagnostics, in both cases the Diagnostic reference is used. With Overlap the Diagnostic reference typically sources or sinks a small current which is connected at the same time as the analog signal being sampled. For SARMUX Diagnostics the Diagnostic reference should provide a reference voltage which is selected at the SARMUX input instead of the normal analog signal being sampled. |
| | OFF | | | 0 | No overlap or SARMUX Diagnostics |
| | HALF | | | 1 | Sample the selected analog input for 2 SAMPLE_TIME periods. During the first period use overlap sampling, i.e. connect both the analog input and Diagnostic reference. During second period only connect the analog input. |
| | FULL | | | 2 | Like normal sample the selected analog input for a single SAMPLE_TIME period but use overlap sampling, i.e. connect both the analog input and Diagnostic reference. |
| | MUX_DIAG | | | 3 | Select Diagnostic reference instead of analog signal at the input of the SARMUX. This enables a functional safety check of the SARMUX analog connections. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 16:27 | SAMPLE_TIME | RW | R | Undefined | Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 300ns, i.e. 6 clock cycles at the max frequency of 20MHz. |
| 31 | ALT_CAL | RW | R | Undefined | Use alternate calibration values instead of the current calibration values. This allows the firmware to allocate one or more channels to quietly re-calibrate the ADC in the background of regular processing. 0 = use regular calibration values (ANA/DIG_CAL) 1 = use alternate calibration values (ANA/DIG_CAL_ALT) Note: typically calibration measurements select VrefL (PIN_ADDR=62) or VrefH (PIN_ADDR=63) |

19.5.1.18.3 PASS_SAR_CH_POST_CTL

Description: Post processing control
Address: 0x40900808
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Make sure the channel or the IP is disabled before changing this register
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|------------------|------------|---|---|-----------------|---|---|
| Name | SIGN_EXT [7:7] | LEFT_ALIGN [6:6] | None [5:3] | | | POST_PROC [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | AVG_CNT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------------|----|--------------|-----------------|----|----|----|----|
| Name | RANGE_MODE [23:22] | | None [21:21] | SHIFT_R [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|-------------------------|--------------|
| Name | None [31:26] | | | | | | TR_DONE_GRP_VIO [25:25] | None [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:2 | POST_PROC | RW | R | Undefined | Post processing |
| | NONE | | | 0 | No postprocessing |
| | AVG | | | 1 | Averaging |
| | AVG_RANGE | | | 2 | Averaging followed by Range detect |
| | RANGE | | | 3 | Range detect |
| | RANGE_PULSE | | | 4 | Range detect followed by pulse detect |
| | RESERVED0 | | | 5 | N/A |
| | RESERVED1 | | | 6 | N/A |
| 6 | LEFT_ALIGN | RW | R | Undefined | Left or right align data in result[15:0]. 0: the data is right aligned in result[11:0], with sign extension to 16 bits if enabled 1: the data is left aligned in result[15:4] with the lower nibble 0. Caveat if the result was more than 12 bits (e.g. after averaging) then the bits above 12 will be discarded. |
| | SIGN_EXT | RW | R | Undefined | Output data is sign extended |
| | UNSIGNED | | | 0 | Default: result data is unsigned (zero extended if needed) |
| | SIGNED | | | 1 | Result data is signed (sign extended if needed) |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 8:15 | AVG_CNT | RW | R | Undefined | <p>Either averaging count (minus 1) or Pulse positive reload value</p> <p>Averaging Count for channels that have averaging enabled. A channel will be sampled (AVG_CNT+1) = [1..256] times. The signal will be acquired back to back (1st order accumulate and dump filter), the average result is calculated and stored and then the next enabled channel is sampled. If more than 16 sample are taken (AVG_CNT>=16) then AVG_SHIFT must be set so that the result after shifting fits in 16 bits</p> <p>Pulse detect positive reload value PULSE_POS_RL[7:0]</p> |
| 16:20 | SHIFT_R | RW | R | Undefined | <p>Either Shift Right (no pulse detection) or Pulse negative reload value (if pulse detection is enabled)</p> <p>Shift right SHIFT_R[3:0] = [0..12]: the result (typically after averaging) is shifted right as specified here. Software has to make sure that the result fits in less than 16 bits. Any value >12 will be treated as 12, bit [4] is always ignored. This can also be used to fit the 12-bit result in 8 bits.</p> <p>Pulse detect negative reload value PULSE_NEG_RL[4:0]</p> |
| 22:23 | RANGE_MODE | RW | R | Undefined | Range detect mode |
| | BELOW_LO | | | 0 | Below Low threshold (result < Lo) |
| | INSIDE_RANGE | | | 1 | Inside range (Lo <= result < Hi) |
| | ABOVE_HI | | | 2 | Above high threshold (Hi <= result) |
| | OUTSIDE_RANGE | | | 3 | Outside range (result < Lo Hi <= result) |
| 25 | TR_DONE_GRP_VIO | RW | R | Undefined | <p>Select tr_sar_ch_done mode for last channel of a group, ignored for all other channels Also see TR_CTL.DONE_LEVEL</p> |
| | DONE | | | 0 | Default: tr_sar_ch_done is set when the group is done |
| | GRP_RANGE_VIO | | | 1 | <p>tr_sar_ch_done is only set if any of the channels in the group has a Range Violation. This mode is ignored if this is not the last channel in the group.</p> <p>Note that if none of the channels in the group have Range detection enabled then the trigger will never get set.</p> |

19.5.1.18.4 PASS_SAR_CH_RANGE_CTL

Description: Range thresholds
Address: 0x4090080C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Make sure the channel or the IP is disabled before changing this register
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | RANGE_LO [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | RANGE_LO [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | RANGE_HI [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | RANGE_HI [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|----------------------------------|
| 0:15 | RANGE_LO | RW | R | Undefined | Range detect low threshold (Lo) |
| 16:31 | RANGE_HI | RW | R | Undefined | Range detect high threshold (Hi) |

19.5.1.18.5 PASS_SAR_CH_INTR

Description: Interrupt request register.
Address: 0x40900810
Offset: 0x10
Retention: Not Retained
IsDeepSleep: No
Comment: interrupts for one channel
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--------------------|---------------------|----------------|
| Name | None [7:3] | | | | | GRP_OVERFLOW [2:2] | GRP_CANCELLED [1:1] | GRP_DONE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|---------------------|----------------|----------------|
| Name | None [15:11] | | | | | CH_OVERFLOW [10:10] | CH_PULSE [9:9] | CH_RANGE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|------|-----------------|--|
| 0 | GRP_DONE | RW1C | RW1S | 0 | Done Interrupt: hardware sets this interrupt for the last channel of a group if the group scan is done. Write with '1' to clear bit. |
| 1 | GRP_CANCELLED | RW1C | RW1S | 0 | Cancelled Interrupt: hardware sets this interrupt for the last channel of a group if the group scan was preempted and CANCELLED. Note that it is possible that also the GRP_DONE interrupt is set. If that is the case one or more new triggers were detected while the group was already busy, i.e. triggers are too fast. Write with '1' to clear bit. |
| 2 | GRP_OVERFLOW | RW1C | RW1S | 0 | Overflow Interrupt: hardware sets this interrupt for the last channel of a group if the group scan is done and the Done interrupt is already (still) pending. Write with '1' to clear bit. |
| 8 | CH_RANGE | RW1C | RW1S | 0 | Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. This interrupt is mutual exclusive with Pulse detect interrupt. Write with '1' to clear bit. |
| 9 | CH_PULSE | RW1C | RW1S | 0 | Pulse detect Interrupt: hardware sets this interrupt for each channel if the positive pulse counter reaches zero. This interrupt is mutual exclusive with Range detect interrupt. Write with '1' to clear bit. |
| 10 | CH_OVERFLOW | RW1C | RW1S | 0 | Channel overflow Interrupt: hardware sets this interrupt for each channel if a new Pulse or Range interrupt is detected while the interrupt is still pending or when DW did not acknowledge data pickup. Write with '1' to clear bit. |

19.5.1.18.6 PASS_SAR_CH_INTR_SET

Description: Interrupt set request register
Address: 0x40900814
Offset: 0x14
Retention: Not Retained
IsDeepSleep: No
Comment: Not really a register, intended for verification/debug. When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|------------------------|-------------------------|--------------------|
| Name | None [7:3] | | | | | GRP_OVERFLOW_SET [2:2] | GRP_CANCELLED_SET [1:1] | GRP_DONE_SET [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|-------------------------|--------------------|--------------------|
| Name | None [15:11] | | | | | CH_OVERFLOW_SET [10:10] | CH_PULSE_SET [9:9] | CH_RANGE_SET [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|----|-----------------|--|
| 0 | GRP_DONE_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | GRP_CANCELLED_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | GRP_OVERFLOW_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | CH_RANGE_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | CH_PULSE_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 10 | CH_OVERFLOW_SET | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

19.5.1.18.7 PASS_SAR_CH_INTR_MASK

Description: Interrupt mask register.
Address: 0x40900818
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--|-----------------------------|
| Name | None [7:3] | | | | | GRP _OVERF _LOW _MASK [2:2] | GRP _CANCE _LLED _MASK [1:1] | GRP _DONE_ MASK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|-------------------------------------|----------------------------|-----------------------------|
| Name | None [15:11] | | | | | CH _OVERFL OW_MASK [10:10] | CH_PULSE _MASK [9:9] | CH _RANGE_ MASK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------------|----|----|-----------------|---|
| 0 | GRP_DONE_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | GRP_CANCELLED_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | GRP_OVERFLOW_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | CH_RANGE_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | CH_PULSE_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | CH_OVERFLOW_MASK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

19.5.1.18.8 PASS_SAR_CH_INTR_MASKED

Description: Interrupt masked request register
Address: 0x4090081C
Offset: 0x1C
Retention: Not Retained
IsDeepSleep: No
Comment: If the value is not zero then the SAR interrupt signal to the NVIC is high. When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--|---|---------------------------------|
| Name | None [7:3] | | | | | GRP _OVERF LOW _MASKED [2:2] | GRP _CANCE LLED _MASKED [1:1] | GRP DONE _MASKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|---|------------------------------|----------------------------------|
| Name | None [15:11] | | | | | CH _OVERFL OW _MASKED [10:10] | CH_PULSE _MASKED [9:9] | CH _RANGE _MASKED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|---|
| 0 | GRP_DONE_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | GRP_CANCELLED_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | GRP_OVERFLOW_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | CH_RANGE_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | CH_PULSE_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | CH_OVERFLOW_MASKED | R | W | 0 | Logical and of corresponding request and mask bits. |

19.5.1.18.9 PASS_SAR_CH_WORK

Description: Working data register
Address: 0x40900820
Offset: 0x20
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|----------------------|----------------------|-------------------------|--------------|----|----|----|
| Name | WORK [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | WORK [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID_MIR [31:31] | PULSE_MIR [30:30] | RANGE_MIR [29:29] | ABOVE_HI_MIR [28:28] | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:15 | WORK | R | RW | Undefined | SAR conversion working data of the channel. The data is written here right after sampling this channel. |
| 28 | ABOVE_HI_MIR | R | W | 0 | mirror bit of the corresponding ABOVE_HI bit |
| 29 | RANGE_MIR | R | W | 0 | mirror bit of corresponding bit in WORK_RANGE register |
| 30 | PULSE_MIR | R | W | 0 | mirror bit of corresponding bit in WORK_PULSE register |
| 31 | VALID_MIR | R | W | 0 | mirror bit of corresponding bit in WORK_VALID register |

19.5.1.18.10 PASS_SAR_CH_RESULT

Description: Result data register
Address: 0x40900824
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|------------------------|------------------------|----------------------|--------------|----|----|----|
| Name | RESULT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | RESULT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID_MIR [31:31] | PULSE_INTR_MIR [30:30] | RANGE_INTR_MIR [29:29] | ABOVE_HI_MIR [28:28] | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0:15 | RESULT | R | W | Undefined | SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. |
| 28 | ABOVE_HI_MIR | R | W | 0 | mirror bit of the corresponding ABOVE_HI bit |
| 29 | RANGE_INTR_MIR | R | W | 0 | mirror bit of INTR.CH_RANGE bit |
| 30 | PULSE_INTR_MIR | R | W | 0 | mirror bit of INTR.CH_PULSE bit |
| 31 | VALID_MIR | R | W | 0 | mirror bit of the corresponding bit in RESULT_VALID register |

19.5.1.18.11 PASS_SAR_CH_GRP_STAT

Description: Group status register
Address: 0x40900828
Offset: 0x28
Retention: Not Retained
IsDeepSleep: No
Comment: This register contains the status information required for a coherent read for the AutoSAR 'ADC Channel Group Status Service'
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|--------------------|---------------------|--------------------|
| Name | None [7:3] | | | | | GRP_OVERFLOW [2:2] | GRP_CANCELLED [1:1] | GRP_COMPLETE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|---------------------|-------------------------|-------------------------|
| Name | None [15:11] | | | | | CH_OVERFLOW [10:10] | CH_PULSE_COMPLETE [9:9] | CH_RANGE_COMPLETE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|------------------|
| Name | None [23:17] | | | | | | | GRP_BUSY [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|--|
| 0 | GRP_COMPLETE | R | W | 0 | Group acquisition complete. This is a copy of the INTR.GRP_DONE bit. |
| 1 | GRP_CANCELLED | R | W | 0 | Group Cancelled. This is a copy of the INTR.GRP_CANCELLED bit. |
| 2 | GRP_OVERFLOW | R | W | 0 | Group Overflow. This is a copy of the INTR.GRP_OVERFLOW bit. |
| 8 | CH_RANGE_COMPLETE | R | W | 0 | Channel Range complete. This is a copy of the INTR.CH_RANGE bit. |
| 9 | CH_PULSE_COMPLETE | R | W | 0 | Channel Pulse complete. This is a copy of the INTR.CH_PULSE bit. |
| 10 | CH_OVERFLOW | R | W | 0 | Channel Overflow. This is a copy of the INTR.CH_OVERFLOW bit. |
| 16 | GRP_BUSY | R | W | 0 | Group acquisition busy. This is a copy of the TR_PENDING bit of the first channel of the group. |

19.5.1.18.12 PASS_SAR_CH_ENABLE

Description: Enable register
Address: 0x40900838
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------|
| Name | None [7:1] | | | | | | | CHAN_EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0 | CHAN_EN | RW | R | 0 | Channel enable. - 0: the corresponding channel is disabled. Corresponding trigger will be reset immediately. - 1: the corresponding channel is enabled. Note: To disable a group either stop the trigger first or begin with disabling the lowest channel first. To enable a group either start with enabling the last channel first and the first channel last, or start the trigger after all channels are enabled. If these rules are not followed the result is undefined. |

19.5.1.18.13 PASS_SAR_CH_TR_CMD

Description: Software triggers
Address: 0x4090083C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-------------|
| Name | None [7:1] | | | | | | | START [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|------|----|-----------------|---|
| 0 | START | RW1S | A | 0 | Software start trigger. When written with '1', a start trigger is generated which sets the corresponding TR_PEND bit (only if the channel is enabled). A read always returns a 0. |

19.5.2 EPASS_MMIO

19.5.2.1 PASS_PASS_CTL

Description: PASS control register
Address: 0x409F0000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------------------|-----------------------|------------|---|------------------------|-----------------------|
| Name | None [7:6] | | SUPPLY_MON_LVL_B [5:5] | SUPPLY_MON_EN_B [4:4] | None [3:2] | | SUPPLY_MON_LVL_A [1:1] | SUPPLY_MON_EN_A [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|---------------------|----|--------------|----|----|----|----|
| Name | None [23:23] | REFBUF_MODE [22:21] | | None [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------------|----|----|----|--------------|----|----|----|
| Name | DBG_FREEZE_EN [31:28] | | | | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------------|----|----|-----------------|---|
| 0 | SUPPLY_MON_EN_A | RW | R | 0 | Supply monitor enable for AMUXBUS_A (amuxbus_a_mon) |
| 1 | SUPPLY_MON_LVL_A | RW | R | 0 | Supply monitor level select for AMUXBUS_A |
| | VRL | | | 0 | amuxbus_a_mon = VRL |
| | VRH | | | 1 | amuxbus_a_mon = VRH |
| 4 | SUPPLY_MON_EN_B | RW | R | 0 | Supply monitor enable for AMUXBUS_B (amuxbus_b_mon) |
| 5 | SUPPLY_MON_LVL_B | RW | R | 0 | Supply monitor level select for AMUXBUS_B |
| | VRL | | | 0 | amuxbus_b_mon = VRL |
| | VRH | | | 1 | amuxbus_b_mon = VRH |
| 21:22 | REFBUF_MODE | RW | R | 0 | Reference mode. The reference needs to be present when using TEMP sensor or diagnostic reference (in addition to SAR.DIAG_CTL.DIAG_EN). Note that setting this mode is not required for the ADC operation itself. |
| | OFF | | | 0 | No reference |
| | ON | | | 1 | Reference = buffered Vbg from SRSS |
| | RESERVED | | | 2 | undefined |
| | BYPASS | | | 3 | Reference = unbuffered Vbg from SRSS |
| 28:31 | DBG_FREEZE_EN | RW | R | 0 | Debug pause enable, 1 per ADC. When set a high tr_debug_freeze trigger will prevent the scheduler from starting acquisitions on a new channel. Note that averaging for an already started channel will be completed. |

19.5.2.2 PASS_SAR_TR_IN_SEL

Description: per SAR generic input trigger select
Address: 0x409F0020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: forward 5 out of max 16 generic input triggers to one SAR instance (there are 5 generic input triggers per SAR)
Default: 0x43210

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|-----------------|----|----|----|
| Name | IN1_SEL [7:4] | | | | IN0_SEL [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | IN3_SEL [15:12] | | | | IN2_SEL [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | IN4_SEL [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------|----|----|-----------------|--|
| 0:3 | IN0_SEL | RW | R | 0 | Select generic trigger for SAR generic trigger input 0 |
| 4:7 | IN1_SEL | RW | R | 1 | Select generic trigger for SAR generic trigger input 1 |
| 8:11 | IN2_SEL | RW | R | 2 | Select generic trigger for SAR generic trigger input 2 |
| 12:15 | IN3_SEL | RW | R | 3 | Select generic trigger for SAR generic trigger input 3 |
| 16:19 | IN4_SEL | RW | R | 4 | Select generic trigger for SAR generic trigger input 4 |

19.5.2.3 PASS_SAR_TR_OUT_SEL

Description: per SAR generic output trigger select
Address: 0x409F0040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: forward 2 of the up to 64 SAR triggers (tr_sar_ch_done + tr_sar_ch_rangevio) to a generic output trigger
Default: 0x100

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|-----------------|----|----|----|----|----|
| Name | None [7:6] | | OUT0_SEL [5:0] | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:14] | | OUT1_SEL [13:8] | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:5 | OUT0_SEL | RW | R | 0 | Select SAR output trigger for generic trigger output 0 0-31: selects a tr_sar_ch_done trigger 32-63: selects a tr_sar_ch_rangvio trigger |
| 8:13 | OUT1_SEL | RW | R | 1 | Select SAR output trigger for generic trigger output 1 |

19.5.2.4 PASS_TEST_CTL

Description: Test control bits
Address: 0x409F0080
Offset: 0x80
Retention: Not Retained
IsDeepSleep: No
Comment: Note: All bits besides 6, 8, 9 are reserved, and should not be modified by the user
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---------------------|---------------------------|-----------------------|---------------------|---------------------|------------|---------------------|
| Name | None [7:7] | TS_CAL_VI_SEL [6:6] | TS_CAL_DIODE_PNP_EN [5:5] | TS_CAL_DIODE_EN [4:4] | TS_CAL_VE_OUT [3:3] | TS_CAL_VB_OUT [2:2] | None [1:1] | TS_CAL_CUR_IN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----------------------|--------------|----|----------------------|---|
| Name | None [15:13] | | | TS_CAL_SPARE [12:12] | None [11:10] | | TS_CAL_CUR_SEL [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------------|----|----|-----------------|---|
| 0 | TS_CAL_CUR_IN | RW | R | 0 | External current input switch control, for Temperature Sensor Calibration |
| 2 | TS_CAL_VB_OUT | RW | R | 0 | Voltage Base switch control, for Temperature Sensor Calibration |
| 3 | TS_CAL_VE_OUT | RW | R | 0 | Voltage Emitter switch control, for Temperature Sensor Calibration |
| 4 | TS_CAL_DIODE_EN | RW | R | 0 | Diode Enable, disconnect or connect the base and collector terminal of the BJT |
| 5 | TS_CAL_DIODE_PNP_EN | RW | R | 0 | Enable signal for PNP transistor. This transistor will be used only during calibration for accurate estimation of chip temp. 0 = Turn PNP off 1 = Configure PNP as a diode (short base and collector) |
| 6 | TS_CAL_VI_SEL | RW | R | 0 | Select current or voltage output on 'v_temp' pin, for Temperature Sensor Calibration |
| | CURRENT | | | 0 | Current is selected |
| | VOLTAGE | | | 1 | Voltage is selected |
| 8:9 | TS_CAL_CUR_SEL | RW | R | 0 | Select the current going into the BJT, for Temperature Sensor Calibration |
| | I_1U | | | 0 | Select 1 uA |
| | I_2U | | | 1 | Select 2 uA |
| | I_5U | | | 2 | Select 5 uA |
| | I_10U | | | 3 | Select 10 uA |
| 12 | TS_CAL_SPARE | RW | R | 0 | Spare |

20 PERI

Description Peripheral interconnect
Base Address 0x40000000
Size 0x10000
Slave Num MMIO0 - 0

| Register Name | Address | Permission | Description |
|------------------|------------|------------|-----------------|
| PERI_TIMEOUT_CTL | 0x40000200 | FULL | Timeout control |
| PERI_TR_CMD | 0x40000220 | FULL | Trigger command |
| PERI_DIV_CMD | 0x40000400 | FULL | Divider command |
| PERI_CLOCK_CTL0 | 0x40000C00 | FULL | Clock control |
| PERI_CLOCK_CTL1 | 0x40000C04 | FULL | Clock control |
| PERI_CLOCK_CTL2 | 0x40000C08 | FULL | Clock control |
| PERI_CLOCK_CTL3 | 0x40000C0C | FULL | Clock control |
| PERI_CLOCK_CTL4 | 0x40000C10 | FULL | Clock control |
| PERI_CLOCK_CTL5 | 0x40000C14 | FULL | Clock control |
| PERI_CLOCK_CTL6 | 0x40000C18 | FULL | Clock control |
| PERI_CLOCK_CTL7 | 0x40000C1C | FULL | Clock control |
| PERI_CLOCK_CTL8 | 0x40000C20 | FULL | Clock control |
| PERI_CLOCK_CTL9 | 0x40000C24 | FULL | Clock control |
| PERI_CLOCK_CTL10 | 0x40000C28 | FULL | Clock control |
| PERI_CLOCK_CTL11 | 0x40000C2C | FULL | Clock control |
| PERI_CLOCK_CTL12 | 0x40000C30 | FULL | Clock control |
| PERI_CLOCK_CTL13 | 0x40000C34 | FULL | Clock control |
| PERI_CLOCK_CTL14 | 0x40000C38 | FULL | Clock control |
| PERI_CLOCK_CTL15 | 0x40000C3C | FULL | Clock control |
| PERI_CLOCK_CTL16 | 0x40000C40 | FULL | Clock control |
| PERI_CLOCK_CTL17 | 0x40000C44 | FULL | Clock control |
| PERI_CLOCK_CTL18 | 0x40000C48 | FULL | Clock control |
| PERI_CLOCK_CTL19 | 0x40000C4C | FULL | Clock control |
| PERI_CLOCK_CTL20 | 0x40000C50 | FULL | Clock control |
| PERI_CLOCK_CTL21 | 0x40000C54 | FULL | Clock control |
| PERI_CLOCK_CTL22 | 0x40000C58 | FULL | Clock control |
| PERI_CLOCK_CTL23 | 0x40000C5C | FULL | Clock control |
| PERI_CLOCK_CTL24 | 0x40000C60 | FULL | Clock control |
| PERI_CLOCK_CTL25 | 0x40000C64 | FULL | Clock control |
| PERI_CLOCK_CTL26 | 0x40000C68 | FULL | Clock control |
| PERI_CLOCK_CTL27 | 0x40000C6C | FULL | Clock control |
| PERI_CLOCK_CTL28 | 0x40000C70 | FULL | Clock control |
| PERI_CLOCK_CTL29 | 0x40000C74 | FULL | Clock control |
| PERI_CLOCK_CTL30 | 0x40000C78 | FULL | Clock control |
| PERI_CLOCK_CTL31 | 0x40000C7C | FULL | Clock control |
| PERI_CLOCK_CTL32 | 0x40000C80 | FULL | Clock control |
| PERI_CLOCK_CTL33 | 0x40000C84 | FULL | Clock control |
| PERI_CLOCK_CTL34 | 0x40000C88 | FULL | Clock control |
| PERI_CLOCK_CTL35 | 0x40000C8C | FULL | Clock control |
| PERI_CLOCK_CTL36 | 0x40000C90 | FULL | Clock control |
| PERI_CLOCK_CTL37 | 0x40000C94 | FULL | Clock control |
| PERI_CLOCK_CTL38 | 0x40000C98 | FULL | Clock control |
| PERI_CLOCK_CTL39 | 0x40000C9C | FULL | Clock control |
| PERI_CLOCK_CTL40 | 0x40000CA0 | FULL | Clock control |
| PERI_CLOCK_CTL41 | 0x40000CA4 | FULL | Clock control |
| PERI_CLOCK_CTL42 | 0x40000CA8 | FULL | Clock control |
| PERI_CLOCK_CTL43 | 0x40000CAC | FULL | Clock control |
| PERI_CLOCK_CTL44 | 0x40000CB0 | FULL | Clock control |
| PERI_CLOCK_CTL45 | 0x40000CB4 | FULL | Clock control |
| PERI_CLOCK_CTL46 | 0x40000CB8 | FULL | Clock control |
| PERI_CLOCK_CTL47 | 0x40000CBC | FULL | Clock control |
| PERI_CLOCK_CTL48 | 0x40000CC0 | FULL | Clock control |
| PERI_CLOCK_CTL49 | 0x40000CC4 | FULL | Clock control |
| PERI_CLOCK_CTL50 | 0x40000CC8 | FULL | Clock control |
| PERI_CLOCK_CTL51 | 0x40000CCC | FULL | Clock control |

| Register Name | Address | Permission | Description |
|-------------------|------------|------------|---------------|
| PERI_CLOCK_CTL52 | 0x40000CD0 | FULL | Clock control |
| PERI_CLOCK_CTL53 | 0x40000CD4 | FULL | Clock control |
| PERI_CLOCK_CTL54 | 0x40000CD8 | FULL | Clock control |
| PERI_CLOCK_CTL55 | 0x40000CDC | FULL | Clock control |
| PERI_CLOCK_CTL56 | 0x40000CE0 | FULL | Clock control |
| PERI_CLOCK_CTL57 | 0x40000CE4 | FULL | Clock control |
| PERI_CLOCK_CTL58 | 0x40000CE8 | FULL | Clock control |
| PERI_CLOCK_CTL59 | 0x40000CEC | FULL | Clock control |
| PERI_CLOCK_CTL60 | 0x40000CF0 | FULL | Clock control |
| PERI_CLOCK_CTL61 | 0x40000CF4 | FULL | Clock control |
| PERI_CLOCK_CTL62 | 0x40000CF8 | FULL | Clock control |
| PERI_CLOCK_CTL63 | 0x40000CFC | FULL | Clock control |
| PERI_CLOCK_CTL64 | 0x40000D00 | FULL | Clock control |
| PERI_CLOCK_CTL65 | 0x40000D04 | FULL | Clock control |
| PERI_CLOCK_CTL66 | 0x40000D08 | FULL | Clock control |
| PERI_CLOCK_CTL67 | 0x40000D0C | FULL | Clock control |
| PERI_CLOCK_CTL68 | 0x40000D10 | FULL | Clock control |
| PERI_CLOCK_CTL69 | 0x40000D14 | FULL | Clock control |
| PERI_CLOCK_CTL70 | 0x40000D18 | FULL | Clock control |
| PERI_CLOCK_CTL71 | 0x40000D1C | FULL | Clock control |
| PERI_CLOCK_CTL72 | 0x40000D20 | FULL | Clock control |
| PERI_CLOCK_CTL73 | 0x40000D24 | FULL | Clock control |
| PERI_CLOCK_CTL74 | 0x40000D28 | FULL | Clock control |
| PERI_CLOCK_CTL75 | 0x40000D2C | FULL | Clock control |
| PERI_CLOCK_CTL76 | 0x40000D30 | FULL | Clock control |
| PERI_CLOCK_CTL77 | 0x40000D34 | FULL | Clock control |
| PERI_CLOCK_CTL78 | 0x40000D38 | FULL | Clock control |
| PERI_CLOCK_CTL79 | 0x40000D3C | FULL | Clock control |
| PERI_CLOCK_CTL80 | 0x40000D40 | FULL | Clock control |
| PERI_CLOCK_CTL81 | 0x40000D44 | FULL | Clock control |
| PERI_CLOCK_CTL82 | 0x40000D48 | FULL | Clock control |
| PERI_CLOCK_CTL83 | 0x40000D4C | FULL | Clock control |
| PERI_CLOCK_CTL84 | 0x40000D50 | FULL | Clock control |
| PERI_CLOCK_CTL85 | 0x40000D54 | FULL | Clock control |
| PERI_CLOCK_CTL86 | 0x40000D58 | FULL | Clock control |
| PERI_CLOCK_CTL87 | 0x40000D5C | FULL | Clock control |
| PERI_CLOCK_CTL88 | 0x40000D60 | FULL | Clock control |
| PERI_CLOCK_CTL89 | 0x40000D64 | FULL | Clock control |
| PERI_CLOCK_CTL90 | 0x40000D68 | FULL | Clock control |
| PERI_CLOCK_CTL91 | 0x40000D6C | FULL | Clock control |
| PERI_CLOCK_CTL92 | 0x40000D70 | FULL | Clock control |
| PERI_CLOCK_CTL93 | 0x40000D74 | FULL | Clock control |
| PERI_CLOCK_CTL94 | 0x40000D78 | FULL | Clock control |
| PERI_CLOCK_CTL95 | 0x40000D7C | FULL | Clock control |
| PERI_CLOCK_CTL96 | 0x40000D80 | FULL | Clock control |
| PERI_CLOCK_CTL97 | 0x40000D84 | FULL | Clock control |
| PERI_CLOCK_CTL98 | 0x40000D88 | FULL | Clock control |
| PERI_CLOCK_CTL99 | 0x40000D8C | FULL | Clock control |
| PERI_CLOCK_CTL100 | 0x40000D90 | FULL | Clock control |
| PERI_CLOCK_CTL101 | 0x40000D94 | FULL | Clock control |
| PERI_CLOCK_CTL102 | 0x40000D98 | FULL | Clock control |
| PERI_CLOCK_CTL103 | 0x40000D9C | FULL | Clock control |
| PERI_CLOCK_CTL104 | 0x40000DA0 | FULL | Clock control |
| PERI_CLOCK_CTL105 | 0x40000DA4 | FULL | Clock control |
| PERI_CLOCK_CTL106 | 0x40000DA8 | FULL | Clock control |
| PERI_CLOCK_CTL107 | 0x40000DAC | FULL | Clock control |
| PERI_CLOCK_CTL108 | 0x40000DB0 | FULL | Clock control |
| PERI_CLOCK_CTL109 | 0x40000DB4 | FULL | Clock control |
| PERI_CLOCK_CTL110 | 0x40000DB8 | FULL | Clock control |
| PERI_CLOCK_CTL111 | 0x40000DBC | FULL | Clock control |
| PERI_CLOCK_CTL112 | 0x40000DC0 | FULL | Clock control |
| PERI_CLOCK_CTL113 | 0x40000DC4 | FULL | Clock control |
| PERI_CLOCK_CTL114 | 0x40000DC8 | FULL | Clock control |

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|------------------------------------|
| PERI_CLOCK_CTL115 | 0x40000DCC | FULL | Clock control |
| PERI_CLOCK_CTL116 | 0x40000DD0 | FULL | Clock control |
| PERI_CLOCK_CTL117 | 0x40000DD4 | FULL | Clock control |
| PERI_CLOCK_CTL118 | 0x40000DD8 | FULL | Clock control |
| PERI_CLOCK_CTL119 | 0x40000DDC | FULL | Clock control |
| PERI_CLOCK_CTL120 | 0x40000DE0 | FULL | Clock control |
| PERI_CLOCK_CTL121 | 0x40000DE4 | FULL | Clock control |
| PERI_CLOCK_CTL122 | 0x40000DE8 | FULL | Clock control |
| PERI_CLOCK_CTL123 | 0x40000DEC | FULL | Clock control |
| PERI_DIV_8_CTL0 | 0x40001000 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL1 | 0x40001004 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL2 | 0x40001008 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL3 | 0x4000100C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL4 | 0x40001010 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL5 | 0x40001014 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL6 | 0x40001018 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL7 | 0x4000101C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL8 | 0x40001020 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL9 | 0x40001024 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL10 | 0x40001028 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL11 | 0x4000102C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL12 | 0x40001030 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL13 | 0x40001034 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL14 | 0x40001038 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL15 | 0x4000103C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL16 | 0x40001040 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL17 | 0x40001044 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL18 | 0x40001048 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL19 | 0x4000104C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL20 | 0x40001050 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL21 | 0x40001054 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL22 | 0x40001058 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL23 | 0x4000105C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL24 | 0x40001060 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL25 | 0x40001064 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL26 | 0x40001068 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL27 | 0x4000106C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL28 | 0x40001070 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL29 | 0x40001074 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL30 | 0x40001078 | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_8_CTL31 | 0x4000107C | FULL | Divider control (for 8.0 divider) |
| PERI_DIV_16_CTL0 | 0x40001400 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL1 | 0x40001404 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL2 | 0x40001408 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL3 | 0x4000140C | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL4 | 0x40001410 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL5 | 0x40001414 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL6 | 0x40001418 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL7 | 0x4000141C | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL8 | 0x40001420 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL9 | 0x40001424 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL10 | 0x40001428 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL11 | 0x4000142C | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL12 | 0x40001430 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL13 | 0x40001434 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL14 | 0x40001438 | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_16_CTL15 | 0x4000143C | FULL | Divider control (for 16.0 divider) |
| PERI_DIV_24_5_CTL0 | 0x40001C00 | FULL | Divider control (for 24.5 divider) |
| PERI_DIV_24_5_CTL1 | 0x40001C04 | FULL | Divider control (for 24.5 divider) |
| PERI_DIV_24_5_CTL2 | 0x40001C08 | FULL | Divider control (for 24.5 divider) |
| PERI_DIV_24_5_CTL3 | 0x40001C0C | FULL | Divider control (for 24.5 divider) |
| PERI_DIV_24_5_CTL4 | 0x40001C10 | FULL | Divider control (for 24.5 divider) |
| PERI_DIV_24_5_CTL5 | 0x40001C14 | FULL | Divider control (for 24.5 divider) |

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|------------------------------------|
| PERI_DIV_24_5_CTL6 | 0x40001C18 | FULL | Divider control (for 24.5 divider) |
| PERI_DIV_24_5_CTL7 | 0x40001C1C | FULL | Divider control (for 24.5 divider) |
| PERI_ECC_CTL | 0x40002000 | FULL | ECC control |

20.1 GR 0

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| PERI_GR0_SL_CTL | 0x40004010 | FULL | Slave control Note:ENABLED_2 ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_2 DISABLED_3 DISABLED_4 DISABLED_5 DISABLED_6 DISABLED_7 DISABLED_8 DISABLED_9 DISABLED_10 DISABLED_11 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.2 GR 1

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| PERI_GR1_SL_CTL | 0x40004030 | FULL | Slave control Note:ENABLED_1 ENABLED_2 ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_1 DISABLED_2 DISABLED_3 DISABLED_4 DISABLED_5 DISABLED_6 DISABLED_7 DISABLED_8 DISABLED_9 DISABLED_10 DISABLED_11 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.3 GR 2

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| PERI_GR2_SL_CTL | 0x40004050 | FULL | Slave control Note:ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.4 GR 3

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|---|
| PERI_GR3_CLOCK_CTL | 0x40004060 | FULL | Clock control |
| PERI_GR3_SL_CTL | 0x40004070 | FULL | Slave control Note:ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_5 DISABLED_6 DISABLED_7 DISABLED_8 DISABLED_9 DISABLED_10 DISABLED_11 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.5 GR 5

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|--|
| PERI_GR5_CLOCK_CTL | 0x400040A0 | FULL | Clock control |
| PERI_GR5_SL_CTL | 0x400040B0 | FULL | Slave control Note:ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_4 DISABLED_5 DISABLED_6 DISABLED_7 DISABLED_8 DISABLED_9 DISABLED_10 DISABLED_11 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.6 GR 6

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|--|
| PERI_GR6_CLOCK_CTL | 0x400040C0 | FULL | Clock control |
| PERI_GR6_SL_CTL | 0x400040D0 | FULL | Slave control Note:ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_8 DISABLED_9 DISABLED_10 DISABLED_11 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.7 GR 9

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|---|
| PERI_GR9_CLOCK_CTL | 0x40004120 | FULL | Clock control |
| PERI_GR9_SL_CTL | 0x40004130 | FULL | Slave control Note:ENABLED_1 ENABLED_2 ENABLED_3 ENABLED_4 ENABLED_5 ENABLED_6 ENABLED_7 ENABLED_8 ENABLED_9 ENABLED_10 ENABLED_11 ENABLED_12 ENABLED_13 ENABLED_14 ENABLED_15 DISABLED_1 DISABLED_2 DISABLED_3 DISABLED_4 DISABLED_5 DISABLED_6 DISABLED_7 DISABLED_8 DISABLED_9 DISABLED_10 DISABLED_11 DISABLED_12 DISABLED_13 DISABLED_14 DISABLED_15 are not available for this register |

20.8 TR_GR 0

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR0_TR_CTL0 | 0x40008000 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL1 | 0x40008004 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL2 | 0x40008008 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL3 | 0x4000800C | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL4 | 0x40008010 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL5 | 0x40008014 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL6 | 0x40008018 | FULL | Trigger control register |
| PERI_TR_GR0_TR_CTL7 | 0x4000801C | FULL | Trigger control register |

20.9 TR_GR 1

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR1_TR_CTL0 | 0x40008400 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL1 | 0x40008404 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL2 | 0x40008408 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL3 | 0x4000840C | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL4 | 0x40008410 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL5 | 0x40008414 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL6 | 0x40008418 | FULL | Trigger control register |
| PERI_TR_GR1_TR_CTL7 | 0x4000841C | FULL | Trigger control register |

20.10 TR_GR 2

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR2_TR_CTL0 | 0x40008800 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL1 | 0x40008804 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL2 | 0x40008808 | FULL | Trigger control register |
| PERI_TR_GR2_TR_CTL3 | 0x4000880C | FULL | Trigger control register |

20.11 TR_GR 3

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR3_TR_CTL0 | 0x40008C00 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL1 | 0x40008C04 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL2 | 0x40008C08 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL3 | 0x40008C0C | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL4 | 0x40008C10 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL5 | 0x40008C14 | FULL | Trigger control register |
| PERI_TR_GR3_TR_CTL6 | 0x40008C18 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR3_TR_CTL7 | 0x40008C1C | FULL | Trigger control register |

20.12 TR_GR 4

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR4_TR_CTL0 | 0x40009000 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL1 | 0x40009004 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL2 | 0x40009008 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL3 | 0x4000900C | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL4 | 0x40009010 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL5 | 0x40009014 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL6 | 0x40009018 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL7 | 0x4000901C | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL8 | 0x40009020 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL9 | 0x40009024 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL10 | 0x40009028 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL11 | 0x4000902C | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL12 | 0x40009030 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL13 | 0x40009034 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL14 | 0x40009038 | FULL | Trigger control register |
| PERI_TR_GR4_TR_CTL15 | 0x4000903C | FULL | Trigger control register |

20.13 TR_GR 5

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR5_TR_CTL0 | 0x40009400 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL1 | 0x40009404 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL2 | 0x40009408 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL3 | 0x4000940C | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL4 | 0x40009410 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL5 | 0x40009414 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL6 | 0x40009418 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL7 | 0x4000941C | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL8 | 0x40009420 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL9 | 0x40009424 | FULL | Trigger control register |
| PERI_TR_GR5_TR_CTL10 | 0x40009428 | FULL | Trigger control register |

20.14 TR_GR 6

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR6_TR_CTL0 | 0x40009800 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL1 | 0x40009804 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL2 | 0x40009808 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL3 | 0x4000980C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL4 | 0x40009810 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL5 | 0x40009814 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL6 | 0x40009818 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL7 | 0x4000981C | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL8 | 0x40009820 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL9 | 0x40009824 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL10 | 0x40009828 | FULL | Trigger control register |
| PERI_TR_GR6_TR_CTL11 | 0x4000982C | FULL | Trigger control register |

20.15 TR_GR 7

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|--------------------------|
| PERI_TR_GR7_TR_CTL0 | 0x40009C00 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL1 | 0x40009C04 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL2 | 0x40009C08 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL3 | 0x40009C0C | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL4 | 0x40009C10 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL5 | 0x40009C14 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL6 | 0x40009C18 | FULL | Trigger control register |
| PERI_TR_GR7_TR_CTL7 | 0x40009C1C | FULL | Trigger control register |

20.16 TR_GR 8

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|--------------------------|
| PERI_TR_GR8_TR_CTL0 | 0x4000A000 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL1 | 0x4000A004 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL2 | 0x4000A008 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL3 | 0x4000A00C | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL4 | 0x4000A010 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL5 | 0x4000A014 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL6 | 0x4000A018 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL7 | 0x4000A01C | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL8 | 0x4000A020 | FULL | Trigger control register |
| PERI_TR_GR8_TR_CTL9 | 0x4000A024 | FULL | Trigger control register |

20.17 TR_GR 9

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|---|
| PERI_TR_GR9_TR_CTL0 | 0x4000A400 | FULL | Trigger control register Note: TR_INV TR_EDGE are not available for this register |
| PERI_TR_GR9_TR_CTL1 | 0x4000A404 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL2 | 0x4000A408 | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL3 | 0x4000A40C | FULL | Trigger control register |
| PERI_TR_GR9_TR_CTL4 | 0x4000A410 | FULL | Trigger control register |

20.18 TR_GR 10

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| PERI_TR_GR10_TR_CTL0 | 0x4000A800 | FULL | Trigger control register Note: TR_INV TR_EDGE are not available for this register |
| PERI_TR_GR10_TR_CTL1 | 0x4000A804 | FULL | Trigger control register |
| PERI_TR_GR10_TR_CTL2 | 0x4000A808 | FULL | Trigger control register |
| PERI_TR_GR10_TR_CTL3 | 0x4000A80C | FULL | Trigger control register |
| PERI_TR_GR10_TR_CTL4 | 0x4000A810 | FULL | Trigger control register |

20.19 TR_1TO1_GR 0

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR0_TR_CTL0 | 0x4000C000 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL1 | 0x4000C004 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL2 | 0x4000C008 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL3 | 0x4000C00C | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL4 | 0x4000C010 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL5 | 0x4000C014 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL6 | 0x4000C018 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL7 | 0x4000C01C | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL8 | 0x4000C020 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL9 | 0x4000C024 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL10 | 0x4000C028 | FULL | Trigger control register |
| PERI_TR_1TO1_GR0_TR_CTL11 | 0x4000C02C | FULL | Trigger control register |

20.20 TR_1TO1_GR 1

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR1_TR_CTL0 | 0x4000C400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL1 | 0x4000C404 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL2 | 0x4000C408 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL3 | 0x4000C40C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL4 | 0x4000C410 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL5 | 0x4000C414 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL6 | 0x4000C418 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL7 | 0x4000C41C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL8 | 0x4000C420 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL9 | 0x4000C424 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL10 | 0x4000C428 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL11 | 0x4000C42C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL12 | 0x4000C430 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR1_TR_CTL13 | 0x4000C434 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL14 | 0x4000C438 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL15 | 0x4000C43C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL16 | 0x4000C440 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL17 | 0x4000C444 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL18 | 0x4000C448 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL19 | 0x4000C44C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL20 | 0x4000C450 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL21 | 0x4000C454 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL22 | 0x4000C458 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL23 | 0x4000C45C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL24 | 0x4000C460 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL25 | 0x4000C464 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL26 | 0x4000C468 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL27 | 0x4000C46C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL28 | 0x4000C470 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL29 | 0x4000C474 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL30 | 0x4000C478 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL31 | 0x4000C47C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL32 | 0x4000C480 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL33 | 0x4000C484 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL34 | 0x4000C488 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL35 | 0x4000C48C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL36 | 0x4000C490 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL37 | 0x4000C494 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL38 | 0x4000C498 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL39 | 0x4000C49C | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL40 | 0x4000C4A0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL41 | 0x4000C4A4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL42 | 0x4000C4A8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL43 | 0x4000C4AC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL44 | 0x4000C4B0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL45 | 0x4000C4B4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL46 | 0x4000C4B8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL47 | 0x4000C4BC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL48 | 0x4000C4C0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL49 | 0x4000C4C4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL50 | 0x4000C4C8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL51 | 0x4000C4CC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL52 | 0x4000C4D0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL53 | 0x4000C4D4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL54 | 0x4000C4D8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL55 | 0x4000C4DC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL56 | 0x4000C4E0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL57 | 0x4000C4E4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL58 | 0x4000C4E8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL59 | 0x4000C4EC | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL60 | 0x4000C4F0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL61 | 0x4000C4F4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL62 | 0x4000C4F8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR1_TR_CTL63 | 0x4000C4FC | FULL | Trigger control register |

20.21 TR_1TO1_GR 2

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR2_TR_CTL0 | 0x4000C800 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL1 | 0x4000C804 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL2 | 0x4000C808 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL3 | 0x4000C80C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL4 | 0x4000C810 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL5 | 0x4000C814 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL6 | 0x4000C818 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL7 | 0x4000C81C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL8 | 0x4000C820 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR2_TR_CTL9 | 0x4000C824 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL10 | 0x4000C828 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL11 | 0x4000C82C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL12 | 0x4000C830 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL13 | 0x4000C834 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL14 | 0x4000C838 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL15 | 0x4000C83C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL16 | 0x4000C840 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL17 | 0x4000C844 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL18 | 0x4000C848 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL19 | 0x4000C84C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL20 | 0x4000C850 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL21 | 0x4000C854 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL22 | 0x4000C858 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL23 | 0x4000C85C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL24 | 0x4000C860 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL25 | 0x4000C864 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL26 | 0x4000C868 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL27 | 0x4000C86C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL28 | 0x4000C870 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL29 | 0x4000C874 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL30 | 0x4000C878 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL31 | 0x4000C87C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL32 | 0x4000C880 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL33 | 0x4000C884 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL34 | 0x4000C888 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL35 | 0x4000C88C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL36 | 0x4000C890 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL37 | 0x4000C894 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL38 | 0x4000C898 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL39 | 0x4000C89C | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL40 | 0x4000C8A0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL41 | 0x4000C8A4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL42 | 0x4000C8A8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL43 | 0x4000C8AC | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL44 | 0x4000C8B0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL45 | 0x4000C8B4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL46 | 0x4000C8B8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL47 | 0x4000C8BC | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL48 | 0x4000C8C0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL49 | 0x4000C8C4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL50 | 0x4000C8C8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL51 | 0x4000C8CC | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL52 | 0x4000C8D0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL53 | 0x4000C8D4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL54 | 0x4000C8D8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL55 | 0x4000C8DC | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL56 | 0x4000C8E0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL57 | 0x4000C8E4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL58 | 0x4000C8E8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL59 | 0x4000C8EC | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL60 | 0x4000C8F0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL61 | 0x4000C8F4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL62 | 0x4000C8F8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR2_TR_CTL63 | 0x4000C8FC | FULL | Trigger control register |

20.22 TR_1TO1_GR 3

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR3_TR_CTL0 | 0x4000CC00 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL1 | 0x4000CC04 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL2 | 0x4000CC08 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL3 | 0x4000CC0C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL4 | 0x4000CC10 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR3_TR_CTL5 | 0x4000CC14 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL6 | 0x4000CC18 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL7 | 0x4000CC1C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL8 | 0x4000CC20 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL9 | 0x4000CC24 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL10 | 0x4000CC28 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL11 | 0x4000CC2C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL12 | 0x4000CC30 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL13 | 0x4000CC34 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL14 | 0x4000CC38 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL15 | 0x4000CC3C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL16 | 0x4000CC40 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL17 | 0x4000CC44 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL18 | 0x4000CC48 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL19 | 0x4000CC4C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL20 | 0x4000CC50 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL21 | 0x4000CC54 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL22 | 0x4000CC58 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL23 | 0x4000CC5C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL24 | 0x4000CC60 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL25 | 0x4000CC64 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL26 | 0x4000CC68 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL27 | 0x4000CC6C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL28 | 0x4000CC70 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL29 | 0x4000CC74 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL30 | 0x4000CC78 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL31 | 0x4000CC7C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL32 | 0x4000CC80 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL33 | 0x4000CC84 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL34 | 0x4000CC88 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL35 | 0x4000CC8C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL36 | 0x4000CC90 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL37 | 0x4000CC94 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL38 | 0x4000CC98 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL39 | 0x4000CC9C | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL40 | 0x4000CCA0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL41 | 0x4000CCA4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL42 | 0x4000CCA8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL43 | 0x4000CCAC | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL44 | 0x4000CCB0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL45 | 0x4000CCB4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL46 | 0x4000CCB8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL47 | 0x4000CCBC | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL48 | 0x4000CCC0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL49 | 0x4000CCC4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL50 | 0x4000CCC8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL51 | 0x4000CCC0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL52 | 0x4000CCD0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL53 | 0x4000CCD4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL54 | 0x4000CCD8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL55 | 0x4000CCDC | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL56 | 0x4000CCE0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL57 | 0x4000CCE4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL58 | 0x4000CCE8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL59 | 0x4000CCEC | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL60 | 0x4000CCF0 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL61 | 0x4000CCF4 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL62 | 0x4000CCF8 | FULL | Trigger control register |
| PERI_TR_1TO1_GR3_TR_CTL63 | 0x4000CCFC | FULL | Trigger control register |

20.23 TR_1TO1_GR 4

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|--------------------------|
| PERI_TR_1TO1_GR4_TR_CTL0 | 0x4000D000 | FULL | Trigger control register |

| Register Name | Address | Permission | Description |
|---|------------|------------|--------------------------|
| PERI_TR_1TO1_GR4_TR_CTL1 | 0x4000D004 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL2 | 0x4000D008 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL3 | 0x4000D00C | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL4 | 0x4000D010 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL5 | 0x4000D014 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL6 | 0x4000D018 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL7 | 0x4000D01C | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL8 | 0x4000D020 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL9 | 0x4000D024 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL10 | 0x4000D028 | FULL | Trigger control register |
| PERI_TR_1TO1_GR4_TR_CTL11 | 0x4000D02C | FULL | Trigger control register |

20.24 TR_1TO1_GR 5

| Register Name | Address | Permission | Description |
|---|------------|------------|--------------------------|
| PERI_TR_1TO1_GR5_TR_CTL0 | 0x4000D400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL1 | 0x4000D404 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL2 | 0x4000D408 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL3 | 0x4000D40C | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL4 | 0x4000D410 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL5 | 0x4000D414 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL6 | 0x4000D418 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL7 | 0x4000D41C | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL8 | 0x4000D420 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL9 | 0x4000D424 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL10 | 0x4000D428 | FULL | Trigger control register |
| PERI_TR_1TO1_GR5_TR_CTL11 | 0x4000D42C | FULL | Trigger control register |

20.25 TR_1TO1_GR 6

| Register Name | Address | Permission | Description |
|--|------------|------------|--------------------------|
| PERI_TR_1TO1_GR6_TR_CTL0 | 0x4000D800 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL1 | 0x4000D804 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL2 | 0x4000D808 | FULL | Trigger control register |
| PERI_TR_1TO1_GR6_TR_CTL3 | 0x4000D80C | FULL | Trigger control register |

20.26 TR_1TO1_GR 7

| Register Name | Address | Permission | Description |
|--|------------|------------|--------------------------|
| PERI_TR_1TO1_GR7_TR_CTL0 | 0x4000DC00 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL1 | 0x4000DC04 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL2 | 0x4000DC08 | FULL | Trigger control register |
| PERI_TR_1TO1_GR7_TR_CTL3 | 0x4000DC0C | FULL | Trigger control register |

20.27 TR_1TO1_GR 8

| Register Name | Address | Permission | Description |
|---|------------|------------|--------------------------|
| PERI_TR_1TO1_GR8_TR_CTL0 | 0x4000E000 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL1 | 0x4000E004 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL2 | 0x4000E008 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL3 | 0x4000E00C | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL4 | 0x4000E010 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL5 | 0x4000E014 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL6 | 0x4000E018 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL7 | 0x4000E01C | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL8 | 0x4000E020 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL9 | 0x4000E024 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL10 | 0x4000E028 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL11 | 0x4000E02C | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL12 | 0x4000E030 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL13 | 0x4000E034 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL14 | 0x4000E038 | FULL | Trigger control register |
| PERI_TR_1TO1_GR8_TR_CTL15 | 0x4000E03C | FULL | Trigger control register |

20.28 TR_1TO1_GR 9

| Register Name | Address | Permission | Description |
|--|------------|------------|--------------------------|
| PERI_TR_1TO1_GR9_TR_CTL0 | 0x4000E400 | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL1 | 0x4000E404 | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL2 | 0x4000E408 | FULL | Trigger control register |
| PERI_TR_1TO1_GR9_TR_CTL3 | 0x4000E40C | FULL | Trigger control register |

20.29 TR_1TO1_GR 10

| Register Name | Address | Permission | Description |
|---|------------|------------|--------------------------|
| PERI_TR_1TO1_GR10_TR_CTL0 | 0x4000E800 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL1 | 0x4000E804 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL2 | 0x4000E808 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL3 | 0x4000E80C | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL4 | 0x4000E810 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL5 | 0x4000E814 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL6 | 0x4000E818 | FULL | Trigger control register |
| PERI_TR_1TO1_GR10_TR_CTL7 | 0x4000E81C | FULL | Trigger control register |

20.30 Register Details

20.30.1 PERI_TIMEOUT_CTL

Description: Timeout control

Address: 0x40000200

Offset: 0x200

Retention: Retained

IsDeepSleep: No

Comment: The presence of the TIMEOUT_CTL register is dependent on the TIMEOUT_PRESENT parameter.

The presence of TIMEOUT_CTL requires slave 0 of the peripheral group to be present (SL0_PRESENT must be '1').

Default: 0xFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | TIMEOUT [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | TIMEOUT [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:15 | TIMEOUT | RW | R | 65535 | This field specifies a number of clock cycles (clk_slow). If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB-Lite bus error and a fault is generated (and possibly recorded in the fault report structure(s)). '0x0000'-'0xfffe': Number of clock cycles. '0xffff': This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated and a fault will never be generated. |

20.30.2 PERI_TR_CMD

Description: Trigger command

Address: 0x40000220

Offset: 0x220

Retention: Not Retained

IsDeepSleep: No

Comment: This register provides SW control over trigger activation. This is useful for SW initiated triggers (e.g. DW/DMA transfers) or for debugging purposes. The control enables SW activation of one specific input trigger or output trigger of the trigger multiplexer structure.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|-----------------|-----------------|------------------|----|----|----|----|
| Name | TR_SEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | GROUP_SEL [12:8] | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ACTIVATE [31:31] | OUT_SEL [30:30] | TR_EDGE [29:29] | None [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:7 | TR_SEL | RW | R | 0 | Specifies the activated trigger when ACTIVATE is '1'. If the specified trigger is not present, the trigger activation has no effect. |
| 8:12 | GROUP_SEL | RW | R | 0 | Specifies the trigger group: '0'-'15': trigger multiplexer groups. '16'-'31': trigger 1-to-1 groups. |
| 29 | TR_EDGE | RW | R | 0 | Specifies if the activated trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. The trigger reflects TR_CMD.ACTIVATE. '1': edge sensitive trigger. The trigger is activated for two clk_peri cycles. |
| 30 | OUT_SEL | RW | R | 0 | Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Note: this field is not used for trigger 1-to-1 groups. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|------|-----------------|---|
| 31 | ACTIVATE | RW | RW1C | 0 | <p>SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL, TR_EDGE and OUT_SEL. HW sets this field to '0' for edge sensitive triggers AFTER the selected trigger is activated for two clk_peri cycles.</p> <p>Note: when ACTIVATE is '1', SW should not modify the other register fields. SW MUST NOT set ACTIVATE bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set ACTIVATE to '1' with a new register write.</p> |

20.30.3 PERI_DIV_CMD

Description: Divider command

Address: 0x40000400

Offset: 0x400

Retention: Not Retained

IsDeepSleep: No

Comment: The (PA_TYPE_SEL, PA_DIV_SEL) field pair allows a divider to be phase aligned with another divider. E.g., consider a 48 MHz 'clk_peri', and a need for a 12 MHz divided clock A and a 8 MHz divided clock B. Clock A uses 8.0 integer divider 0 and is created by aligning it to 'clk_peri' ((PA_TYPE_SEL, PA_DIV_SEL) is (3, 63)) and DIV_8_CTL0.INT8_DIV is '4-1'. Clock B uses 8.0 integer divider 1 and is created by aligning it to clock A ((PA_TYPE_SEL, PA_DIV_SEL) is (0, 0)) and DIV_8_CTL1.INT8_DIV is '6-1'. This guarantees that clock B is phase aligned with clock A: as the smallest common multiple of the two clock periods is 12 'clk_peri' cycles, the clocks A and B will be aligned every 12 'clk_peri' cycles. Note: clock B is phase aligned to clock A, but still uses 'clk_peri' as a reference clock for its divider value.

Default: 0x3FF03FF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|-----------------|--------------|----|----|----|---------------------|----|
| Name | DIV_SEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | TYPE_SEL [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PA_DIV_SEL [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLE [31:31] | DISABLE [30:30] | None [29:26] | | | | PA_TYPE_SEL [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|---|
| 0:7 | DIV_SEL | RW | R | 255 | (TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed. If DIV_SEL is '255' and TYPE_SEL is '3' (default/reset value), no divider is specified and no clock signal(s) are generated. |
| 8:9 | TYPE_SEL | RW | R | 3 | Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. |
| 16:23 | PA_DIV_SEL | RW | R | 255 | (PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_DIV_SEL is '255' and PA_TYPE_SEL is '3', 'clk_peri' is used as reference. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|------|-----------------|--|
| 24:25 | PA_TYPE_SEL | RW | R | 3 | Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. |
| 30 | DISABLE | RW | RW1C | 0 | Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. |
| 31 | ENABLE | RW | RW1C | 0 | Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to '0'. If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either 'clk_peri' (typical usage) or to ANY enabled divider. The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of 'clk_peri'/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to 'clk_peri' takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. |

20.30.4 PERI_CLOCK_CTL

Description: Clock control
Address: 0x40000C00
Offset: 0xC00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3FF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----------------|----|
| Name | DIV_SEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | TYPE_SEL [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0:7 | DIV_SEL | RW | R | 255 | <p>Specifies one of the dividers of the divider type specified by TYPE_SEL.</p> <p>If DIV_SEL is '255' and TYPE_SEL is '3' (default/reset value), no divider is specified and no clock control signal(s) are generated.</p> <p>When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one 'clk_peri' cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is '255' and TYPE_SEL is '3') for a transition time that is larger than the smaller of the two divider periods.</p> |
| 8:9 | TYPE_SEL | RW | R | 3 | <p>Specifies divider type:</p> <p>0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers.</p> |

20.30.5 PERI_DIV_8_CTL

Description: Divider control (for 8.0 divider)
Address: 0x40001000
Offset: 0x1000
Retention: Retained
IsDeepSleep: No
Comment: Smallest of the divider types.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------|
| Name | None [7:1] | | | | | | | EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | INT8_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0 | EN | R | RW | 0 | <p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.</p> |
| 8:15 | INT8_DIV | RW | R | 0 | <p>Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 256].</p> <p>For the generation of a 50/50 percent duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 percent duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> |

20.30.6 PERI_DIV_16_CTL

Description: Divider control (for 16.0 divider)
Address: 0x40001400
Offset: 0x1400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|----------|
| Name | None [7:1] | | | | | | | EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | INT16_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | INT16_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | EN | R | RW | 0 | <p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.</p> |
| 8:23 | INT16_DIV | RW | R | 0 | <p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50 percent duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 percent duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> |

20.30.7 PERI_DIV_24_5_CTL

Description: Divider control (for 24.5 divider)
Address: 0x40001C00
Offset: 0x1C00
Retention: Retained
IsDeepSleep: No
Comment: Largest of the divider types.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|------------|---|----------|
| Name | FRAC5_DIV [7:3] | | | | | None [2:1] | | EN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | INT24_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | INT24_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | INT24_DIV [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0 | EN | R | RW | 0 | <p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.</p> |
| 3:7 | FRAC5_DIV | RW | R | 0 | <p>Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 'clk_peri' cycle longer than other clock periods.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> |
| 8:31 | INT24_DIV | RW | R | 0 | <p>Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32].</p> <p>For the generation of a 50/50 percent duty cycle divided clock, the division range is restricted to [2, 16,777,216].</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode.</p> |

20.30.8 PERI_ECC_CTL

Description: ECC control
Address: 0x40002000
Offset: 0x2000
Retention: Retained
IsDeepSleep: No
Comment: This register provides ECC support for the protection structures SRAM in the master interfaces peripheral (peripheral group 0, peripheral 1).
Default: 0x10000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|----|--------------------|--------------|----------------|
| Name | WORD_ADDR [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:11] | | | | | WORD_ADDR [10:8] | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:19] | | | | | ECC_INJ_EN [18:18] | None [17:17] | ECC_EN [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PARITY [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|--|
| 0:10 | WORD_ADDR | RW | R | 0 | Specifies the word address where the parity is injected. - On a 32-bit write access to this SRAM address and when ECC_INJ_EN bit is '1', the parity (PARITY) is injected. |
| 16 | ECC_EN | RW | R | 1 | Enable ECC checking: '0': Disabled. '1': Enabled. |
| 18 | ECC_INJ_EN | RW | R | 0 | Enable error injection for PERI protection structure SRAM. When '1', the parity (PARITY) is used when a write is done to the WORD_ADDR word address of the SRAM. |
| 24:31 | PARITY | RW | R | 0 | ECC parity to use for ECC error injection at address WORD_ADDR. |

20.30.9 GR

20.30.9.1 PERI_GR_CLOCK_CTL

Description: Clock control
Address: 0x40004000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: The peripheral interconnect supports up to sixteen groups: group 0, group 1, ..., group 15. Peripheral groups 0, 1 and 2 use clk_slow (clk_group[0] = clk_group[1] = clk_group[2] = clk_slow) and do NOT have a CLOCK_GROUP_DIV_CTL register. Peripheral groups 3, 4, ..., 15 have a dedicated CLOCK_GROUP_DIV_CTL register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|----|----|----|----|----|---|---|
| Name | INT8_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 8:15 | INT8_DIV | RW | R | 0 | Specifies a group clock divider (from the peripheral clock 'clk_peri' to the group clock 'clk_group[3/4/5/...15]'). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to '0' when transitioning from DeepSleep to Active power mode. |

20.30.9.2 PERI_GR_SL_CTL

Description: Slave control
Address: 0x40004010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | ENABLED_7 [7:7] | ENABLED_6 [6:6] | ENABLED_5 [5:5] | ENABLED_4 [4:4] | ENABLED_3 [3:3] | ENABLED_2 [2:2] | ENABLED_1 [1:1] | ENABLED_0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-----------------|-----------------|
| Name | ENABLED_15 [15:15] | ENABLED_14 [14:14] | ENABLED_13 [13:13] | ENABLED_12 [12:12] | ENABLED_11 [11:11] | ENABLED_10 [10:10] | ENABLED_9 [9:9] | ENABLED_8 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | DISABLED_7 [23:23] | DISABLED_6 [22:22] | DISABLED_5 [21:21] | DISABLED_4 [20:20] | DISABLED_3 [19:19] | DISABLED_2 [18:18] | DISABLED_1 [17:17] | DISABLED_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|--------------------|
| Name | DISABLED_15 [31:31] | DISABLED_14 [30:30] | DISABLED_13 [29:29] | DISABLED_12 [28:28] | DISABLED_11 [27:27] | DISABLED_10 [26:26] | DISABLED_9 [25:25] | DISABLED_8 [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | ENABLED_0 | RW | R | 1 | Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant '0') and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. |
| 1 | ENABLED_1 | RW | R | 1 | Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant '0') and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. |
| 2 | ENABLED_2 | RW | R | 1 | N/A |
| 3 | ENABLED_3 | RW | R | 1 | N/A |
| 4 | ENABLED_4 | RW | R | 1 | N/A |
| 5 | ENABLED_5 | RW | R | 1 | N/A |
| 6 | ENABLED_6 | RW | R | 1 | N/A |
| 7 | ENABLED_7 | RW | R | 1 | N/A |
| 8 | ENABLED_8 | RW | R | 1 | N/A |
| 9 | ENABLED_9 | RW | R | 1 | N/A |
| 10 | ENABLED_10 | RW | R | 1 | N/A |
| 11 | ENABLED_11 | RW | R | 1 | N/A |
| 12 | ENABLED_12 | RW | R | 1 | N/A |
| 13 | ENABLED_13 | RW | R | 1 | N/A |
| 14 | ENABLED_14 | RW | R | 1 | N/A |
| 15 | ENABLED_15 | RW | R | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|------|----|-----------------|---|
| 16 | DISABLED_0 | RW1S | R | 0 | Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. |
| 17 | DISABLED_1 | RW1S | R | 0 | N/A |
| 18 | DISABLED_2 | RW1S | R | 0 | N/A |
| 19 | DISABLED_3 | RW1S | R | 0 | N/A |
| 20 | DISABLED_4 | RW1S | R | 0 | N/A |
| 21 | DISABLED_5 | RW1S | R | 0 | N/A |
| 22 | DISABLED_6 | RW1S | R | 0 | N/A |
| 23 | DISABLED_7 | RW1S | R | 0 | N/A |
| 24 | DISABLED_8 | RW1S | R | 0 | N/A |
| 25 | DISABLED_9 | RW1S | R | 0 | N/A |
| 26 | DISABLED_10 | RW1S | R | 0 | N/A |
| 27 | DISABLED_11 | RW1S | R | 0 | N/A |
| 28 | DISABLED_12 | RW1S | R | 0 | N/A |
| 29 | DISABLED_13 | RW1S | R | 0 | N/A |
| 30 | DISABLED_14 | RW1S | R | 0 | N/A |
| 31 | DISABLED_15 | RW1S | R | 0 | N/A |

20.30.10 TR_GR

20.30.10.1 PERI_TR_GR_TR_CTL

Description: Trigger control register

Address: 0x40008000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: This register specifies the input trigger for a specific output trigger in trigger group 0. Note that for SW initiated triggers, SW is responsible for activating the output trigger, rather than relying on a specific HW input trigger. For this reason, input trigger 0 is typically connected to a constant signal level of '0' at chip integration (design decision) and SW initiated output triggers are all connected to input trigger 0 (SW responsibility: TR_OUT_CTL.TR_SEL should be set to '0' to select the constant signal level '0' from chip level). As a result, SW initiated triggers can never be activated by a HW input trigger to the trigger multiplexer.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|-----------------------|--------------|----|---------------|--------------|
| Name | TR_SEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | DBG_FREEZE_EN [12:12] | None [11:10] | | TR_EDGE [9:9] | TR_INV [8:8] |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:7 | TR_SEL | RW | R | 0 | Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. |
| 8 | TR_INV | RW | R | 0 | Specifies if the output trigger is inverted. |
| 9 | TR_EDGE | RW | R | 0 | Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. |
| 12 | DBG_FREEZE_EN | RW | R | 0 | Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. |

20.30.11 TR_1TO1_GR

20.30.11.1 PERI_TR_1TO1_GR_TR_CTL

Description: Trigger control register
Address: 0x4000C000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|--------------|
| Name | None [7:1] | | | | | | | TR_SEL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-----------------------|--------------|----|---------------|--------------|
| Name | None [15:13] | | | DBG_FREEZE_EN [12:12] | None [11:10] | | TR_EDGE [9:9] | TR_INV [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | TR_SEL | RW | R | 0 | Specifies input trigger: '0': constant signal level '0'. '1': input trigger. |
| 8 | TR_INV | RW | R | 0 | Specifies if the output trigger is inverted. |
| 9 | TR_EDGE | RW | R | 0 | Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. |
| 12 | DBG_FREEZE_EN | RW | R | 0 | Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. |

21 PERI_MS

| | |
|---------------------|---|
| Description | Peripheral interconnect, master interface |
| Base Address | 0x40010000 |
| Size | 0x10000 |
| Slave Num | MMIO0 - 1 |

21.1 PPU_PR 0

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR0_SL_ADDR | 0x40010000 | FULL | Slave region, base address |
| PERI_MS_PPU_PR0_SL_SIZE | 0x40010004 | FULL | Slave region, size |
| PERI_MS_PPU_PR0_SL_ATT0 | 0x40010010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR0_SL_ATT1 | 0x40010014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR0_SL_ATT2 | 0x40010018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR0_SL_ATT3 | 0x4001001C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR0_MS_ADDR | 0x40010020 | FULL | Master region, base address |
| PERI_MS_PPU_PR0_MS_SIZE | 0x40010024 | FULL | Master region, size |
| PERI_MS_PPU_PR0_MS_ATT0 | 0x40010030 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR0_MS_ATT1 | 0x40010034 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR0_MS_ATT2 | 0x40010038 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR0_MS_ATT3 | 0x4001003C | FULL | Master attributes 3 |

21.2 PPU_PR 1

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR1_SL_ADDR | 0x40010040 | FULL | Slave region, base address |
| PERI_MS_PPU_PR1_SL_SIZE | 0x40010044 | FULL | Slave region, size |
| PERI_MS_PPU_PR1_SL_ATT0 | 0x40010050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR1_SL_ATT1 | 0x40010054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR1_SL_ATT2 | 0x40010058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR1_SL_ATT3 | 0x4001005C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR1_MS_ADDR | 0x40010060 | FULL | Master region, base address |
| PERI_MS_PPU_PR1_MS_SIZE | 0x40010064 | FULL | Master region, size |
| PERI_MS_PPU_PR1_MS_ATT0 | 0x40010070 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR1_MS_ATT1 | 0x40010074 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR1_MS_ATT2 | 0x40010078 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR1_MS_ATT3 | 0x4001007C | FULL | Master attributes 3 |

21.3 PPU_PR 2

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR2_SL_ADDR | 0x40010080 | FULL | Slave region, base address |
| PERI_MS_PPU_PR2_SL_SIZE | 0x40010084 | FULL | Slave region, size |
| PERI_MS_PPU_PR2_SL_ATT0 | 0x40010090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR2_SL_ATT1 | 0x40010094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR2_SL_ATT2 | 0x40010098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR2_SL_ATT3 | 0x4001009C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR2_MS_ADDR | 0x400100A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR2_MS_SIZE | 0x400100A4 | FULL | Master region, size |
| PERI_MS_PPU_PR2_MS_ATT0 | 0x400100B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR2_MS_ATT1 | 0x400100B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR2_MS_ATT2 | 0x400100B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR2_MS_ATT3 | 0x400100BC | FULL | Master attributes 3 |

21.4 PPU_PR 3

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_PR3_SL_ADDR | 0x400100C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR3_SL_SIZE | 0x400100C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR3_SL_ATT0 | 0x400100D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR3_SL_ATT1 | 0x400100D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR3_SL_ATT2 | 0x400100D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR3_SL_ATT3 | 0x400100DC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR3_MS_ADDR | 0x400100E0 | FULL | Master region, base address |
| PERI_MS_PPU_PR3_MS_SIZE | 0x400100E4 | FULL | Master region, size |
| PERI_MS_PPU_PR3_MS_ATT0 | 0x400100F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR3_MS_ATT1 | 0x400100F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR3_MS_ATT2 | 0x400100F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR3_MS_ATT3 | 0x400100FC | FULL | Master attributes 3 |

21.5 PPU_PR 4

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR4_SL_ADDR | 0x40010100 | FULL | Slave region, base address |
| PERI_MS_PPU_PR4_SL_SIZE | 0x40010104 | FULL | Slave region, size |
| PERI_MS_PPU_PR4_SL_ATT0 | 0x40010110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR4_SL_ATT1 | 0x40010114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR4_SL_ATT2 | 0x40010118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR4_SL_ATT3 | 0x4001011C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR4_MS_ADDR | 0x40010120 | FULL | Master region, base address |
| PERI_MS_PPU_PR4_MS_SIZE | 0x40010124 | FULL | Master region, size |
| PERI_MS_PPU_PR4_MS_ATT0 | 0x40010130 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR4_MS_ATT1 | 0x40010134 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR4_MS_ATT2 | 0x40010138 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR4_MS_ATT3 | 0x4001013C | FULL | Master attributes 3 |

21.6 PPU_PR 5

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR5_SL_ADDR | 0x40010140 | FULL | Slave region, base address |
| PERI_MS_PPU_PR5_SL_SIZE | 0x40010144 | FULL | Slave region, size |
| PERI_MS_PPU_PR5_SL_ATT0 | 0x40010150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR5_SL_ATT1 | 0x40010154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR5_SL_ATT2 | 0x40010158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR5_SL_ATT3 | 0x4001015C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR5_MS_ADDR | 0x40010160 | FULL | Master region, base address |
| PERI_MS_PPU_PR5_MS_SIZE | 0x40010164 | FULL | Master region, size |
| PERI_MS_PPU_PR5_MS_ATT0 | 0x40010170 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR5_MS_ATT1 | 0x40010174 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR5_MS_ATT2 | 0x40010178 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR5_MS_ATT3 | 0x4001017C | FULL | Master attributes 3 |

21.7 PPU_PR 6

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR6_SL_ADDR | 0x40010180 | FULL | Slave region, base address |
| PERI_MS_PPU_PR6_SL_SIZE | 0x40010184 | FULL | Slave region, size |
| PERI_MS_PPU_PR6_SL_ATT0 | 0x40010190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR6_SL_ATT1 | 0x40010194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR6_SL_ATT2 | 0x40010198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR6_SL_ATT3 | 0x4001019C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR6_MS_ADDR | 0x400101A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR6_MS_SIZE | 0x400101A4 | FULL | Master region, size |
| PERI_MS_PPU_PR6_MS_ATT0 | 0x400101B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR6_MS_ATT1 | 0x400101B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR6_MS_ATT2 | 0x400101B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR6_MS_ATT3 | 0x400101BC | FULL | Master attributes 3 |

21.8 PPU_PR 7

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR7_SL_ADDR | 0x400101C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR7_SL_SIZE | 0x400101C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR7_SL_ATT0 | 0x400101D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR7_SL_ATT1 | 0x400101D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR7_SL_ATT2 | 0x400101D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR7_SL_ATT3 | 0x400101DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR7_MS_ADDR | 0x400101E0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_PR7_MS_SIZE | 0x400101E4 | FULL | Master region, size |
| PERI_MS_PPU_PR7_MS_ATT0 | 0x400101F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR7_MS_ATT1 | 0x400101F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR7_MS_ATT2 | 0x400101F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR7_MS_ATT3 | 0x400101FC | FULL | Master attributes 3 |

21.9 PPU_PR 8

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR8_SL_ADDR | 0x40010200 | FULL | Slave region, base address |
| PERI_MS_PPU_PR8_SL_SIZE | 0x40010204 | FULL | Slave region, size |
| PERI_MS_PPU_PR8_SL_ATT0 | 0x40010210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR8_SL_ATT1 | 0x40010214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR8_SL_ATT2 | 0x40010218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR8_SL_ATT3 | 0x4001021C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR8_MS_ADDR | 0x40010220 | FULL | Master region, base address |
| PERI_MS_PPU_PR8_MS_SIZE | 0x40010224 | FULL | Master region, size |
| PERI_MS_PPU_PR8_MS_ATT0 | 0x40010230 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR8_MS_ATT1 | 0x40010234 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR8_MS_ATT2 | 0x40010238 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR8_MS_ATT3 | 0x4001023C | FULL | Master attributes 3 |

21.10 PPU_PR 9

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_PR9_SL_ADDR | 0x40010240 | FULL | Slave region, base address |
| PERI_MS_PPU_PR9_SL_SIZE | 0x40010244 | FULL | Slave region, size |
| PERI_MS_PPU_PR9_SL_ATT0 | 0x40010250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR9_SL_ATT1 | 0x40010254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR9_SL_ATT2 | 0x40010258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR9_SL_ATT3 | 0x4001025C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR9_MS_ADDR | 0x40010260 | FULL | Master region, base address |
| PERI_MS_PPU_PR9_MS_SIZE | 0x40010264 | FULL | Master region, size |
| PERI_MS_PPU_PR9_MS_ATT0 | 0x40010270 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR9_MS_ATT1 | 0x40010274 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR9_MS_ATT2 | 0x40010278 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR9_MS_ATT3 | 0x4001027C | FULL | Master attributes 3 |

21.11 PPU_PR 10

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_PR10_SL_ADDR | 0x40010280 | FULL | Slave region, base address |
| PERI_MS_PPU_PR10_SL_SIZE | 0x40010284 | FULL | Slave region, size |
| PERI_MS_PPU_PR10_SL_ATT0 | 0x40010290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR10_SL_ATT1 | 0x40010294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR10_SL_ATT2 | 0x40010298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR10_SL_ATT3 | 0x4001029C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR10_MS_ADDR | 0x400102A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR10_MS_SIZE | 0x400102A4 | FULL | Master region, size |
| PERI_MS_PPU_PR10_MS_ATT0 | 0x400102B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR10_MS_ATT1 | 0x400102B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR10_MS_ATT2 | 0x400102B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR10_MS_ATT3 | 0x400102BC | FULL | Master attributes 3 |

21.12 PPU_PR 11

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_PR11_SL_ADDR | 0x400102C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR11_SL_SIZE | 0x400102C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR11_SL_ATT0 | 0x400102D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR11_SL_ATT1 | 0x400102D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR11_SL_ATT2 | 0x400102D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR11_SL_ATT3 | 0x400102DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR11_MS_ADDR | 0x400102E0 | FULL | Master region, base address |
| PERI_MS_PPU_PR11_MS_SIZE | 0x400102E4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|--|------------|------------|---------------------|
| PERI_MS_PPU_PR11_MS_ATT0 | 0x400102F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR11_MS_ATT1 | 0x400102F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR11_MS_ATT2 | 0x400102F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR11_MS_ATT3 | 0x400102FC | FULL | Master attributes 3 |

21.13 PPU_PR 12

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_PR12_SL_ADDR | 0x40010300 | FULL | Slave region, base address |
| PERI_MS_PPU_PR12_SL_SIZE | 0x40010304 | FULL | Slave region, size |
| PERI_MS_PPU_PR12_SL_ATT0 | 0x40010310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR12_SL_ATT1 | 0x40010314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR12_SL_ATT2 | 0x40010318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR12_SL_ATT3 | 0x4001031C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR12_MS_ADDR | 0x40010320 | FULL | Master region, base address |
| PERI_MS_PPU_PR12_MS_SIZE | 0x40010324 | FULL | Master region, size |
| PERI_MS_PPU_PR12_MS_ATT0 | 0x40010330 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR12_MS_ATT1 | 0x40010334 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR12_MS_ATT2 | 0x40010338 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR12_MS_ATT3 | 0x4001033C | FULL | Master attributes 3 |

21.14 PPU_PR 13

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_PR13_SL_ADDR | 0x40010340 | FULL | Slave region, base address |
| PERI_MS_PPU_PR13_SL_SIZE | 0x40010344 | FULL | Slave region, size |
| PERI_MS_PPU_PR13_SL_ATT0 | 0x40010350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR13_SL_ATT1 | 0x40010354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR13_SL_ATT2 | 0x40010358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR13_SL_ATT3 | 0x4001035C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR13_MS_ADDR | 0x40010360 | FULL | Master region, base address |
| PERI_MS_PPU_PR13_MS_SIZE | 0x40010364 | FULL | Master region, size |
| PERI_MS_PPU_PR13_MS_ATT0 | 0x40010370 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR13_MS_ATT1 | 0x40010374 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR13_MS_ATT2 | 0x40010378 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR13_MS_ATT3 | 0x4001037C | FULL | Master attributes 3 |

21.15 PPU_PR 14

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_PR14_SL_ADDR | 0x40010380 | FULL | Slave region, base address |
| PERI_MS_PPU_PR14_SL_SIZE | 0x40010384 | FULL | Slave region, size |
| PERI_MS_PPU_PR14_SL_ATT0 | 0x40010390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR14_SL_ATT1 | 0x40010394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR14_SL_ATT2 | 0x40010398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR14_SL_ATT3 | 0x4001039C | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR14_MS_ADDR | 0x400103A0 | FULL | Master region, base address |
| PERI_MS_PPU_PR14_MS_SIZE | 0x400103A4 | FULL | Master region, size |
| PERI_MS_PPU_PR14_MS_ATT0 | 0x400103B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_PR14_MS_ATT1 | 0x400103B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR14_MS_ATT2 | 0x400103B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR14_MS_ATT3 | 0x400103BC | FULL | Master attributes 3 |

21.16 PPU_PR 15

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_PR15_SL_ADDR | 0x400103C0 | FULL | Slave region, base address |
| PERI_MS_PPU_PR15_SL_SIZE | 0x400103C4 | FULL | Slave region, size |
| PERI_MS_PPU_PR15_SL_ATT0 | 0x400103D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_PR15_SL_ATT1 | 0x400103D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_PR15_SL_ATT2 | 0x400103D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_PR15_SL_ATT3 | 0x400103DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_PR15_MS_ADDR | 0x400103E0 | FULL | Master region, base address |
| PERI_MS_PPU_PR15_MS_SIZE | 0x400103E4 | FULL | Master region, size |
| PERI_MS_PPU_PR15_MS_ATT0 | 0x400103F0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---------------------|
| PERI_MS_PPU_PR15_MS_ATT1 | 0x400103F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_PR15_MS_ATT2 | 0x400103F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_PR15_MS_ATT3 | 0x400103FC | FULL | Master attributes 3 |

21.17 PPU_FX 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX0_SL_ADDR | 0x40010800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX0_SL_SIZE | 0x40010804 | FULL | Slave region, size |
| PERI_MS_PPU_FX0_SL_ATT0 | 0x40010810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX0_SL_ATT1 | 0x40010814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX0_SL_ATT2 | 0x40010818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX0_SL_ATT3 | 0x4001081C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX0_MS_ADDR | 0x40010820 | FULL | Master region, base address |
| PERI_MS_PPU_FX0_MS_SIZE | 0x40010824 | FULL | Master region, size |
| PERI_MS_PPU_FX0_MS_ATT0 | 0x40010830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX0_MS_ATT1 | 0x40010834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX0_MS_ATT2 | 0x40010838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX0_MS_ATT3 | 0x4001083C | FULL | Master attributes 3 |

21.18 PPU_FX 1

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX1_SL_ADDR | 0x40010840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX1_SL_SIZE | 0x40010844 | FULL | Slave region, size |
| PERI_MS_PPU_FX1_SL_ATT0 | 0x40010850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX1_SL_ATT1 | 0x40010854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX1_SL_ATT2 | 0x40010858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX1_SL_ATT3 | 0x4001085C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX1_MS_ADDR | 0x40010860 | FULL | Master region, base address |
| PERI_MS_PPU_FX1_MS_SIZE | 0x40010864 | FULL | Master region, size |
| PERI_MS_PPU_FX1_MS_ATT0 | 0x40010870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX1_MS_ATT1 | 0x40010874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX1_MS_ATT2 | 0x40010878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX1_MS_ATT3 | 0x4001087C | FULL | Master attributes 3 |

21.19 PPU_FX 2

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX2_SL_ADDR | 0x40010880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX2_SL_SIZE | 0x40010884 | FULL | Slave region, size |
| PERI_MS_PPU_FX2_SL_ATT0 | 0x40010890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX2_SL_ATT1 | 0x40010894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX2_SL_ATT2 | 0x40010898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX2_SL_ATT3 | 0x4001089C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX2_MS_ADDR | 0x400108A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX2_MS_SIZE | 0x400108A4 | FULL | Master region, size |
| PERI_MS_PPU_FX2_MS_ATT0 | 0x400108B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX2_MS_ATT1 | 0x400108B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX2_MS_ATT2 | 0x400108B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX2_MS_ATT3 | 0x400108BC | FULL | Master attributes 3 |

21.20 PPU_FX 3

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX3_SL_ADDR | 0x400108C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX3_SL_SIZE | 0x400108C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX3_SL_ATT0 | 0x400108D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX3_SL_ATT1 | 0x400108D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX3_SL_ATT2 | 0x400108D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX3_SL_ATT3 | 0x400108DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX3_MS_ADDR | 0x400108E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX3_MS_SIZE | 0x400108E4 | FULL | Master region, size |
| PERI_MS_PPU_FX3_MS_ATT0 | 0x400108F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX3_MS_ATT1 | 0x400108F4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX3_MS_ATT2 | 0x400108F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX3_MS_ATT3 | 0x400108FC | FULL | Master attributes 3 |

21.21 PPU_FX 4

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX4_SL_ADDR | 0x40010900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX4_SL_SIZE | 0x40010904 | FULL | Slave region, size |
| PERI_MS_PPU_FX4_SL_ATT0 | 0x40010910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX4_SL_ATT1 | 0x40010914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX4_SL_ATT2 | 0x40010918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX4_SL_ATT3 | 0x4001091C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX4_MS_ADDR | 0x40010920 | FULL | Master region, base address |
| PERI_MS_PPU_FX4_MS_SIZE | 0x40010924 | FULL | Master region, size |
| PERI_MS_PPU_FX4_MS_ATT0 | 0x40010930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX4_MS_ATT1 | 0x40010934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX4_MS_ATT2 | 0x40010938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX4_MS_ATT3 | 0x4001093C | FULL | Master attributes 3 |

21.22 PPU_FX 5

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX5_SL_ADDR | 0x40010940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX5_SL_SIZE | 0x40010944 | FULL | Slave region, size |
| PERI_MS_PPU_FX5_SL_ATT0 | 0x40010950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX5_SL_ATT1 | 0x40010954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX5_SL_ATT2 | 0x40010958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX5_SL_ATT3 | 0x4001095C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX5_MS_ADDR | 0x40010960 | FULL | Master region, base address |
| PERI_MS_PPU_FX5_MS_SIZE | 0x40010964 | FULL | Master region, size |
| PERI_MS_PPU_FX5_MS_ATT0 | 0x40010970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX5_MS_ATT1 | 0x40010974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX5_MS_ATT2 | 0x40010978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX5_MS_ATT3 | 0x4001097C | FULL | Master attributes 3 |

21.23 PPU_FX 6

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX6_SL_ADDR | 0x40010980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX6_SL_SIZE | 0x40010984 | FULL | Slave region, size |
| PERI_MS_PPU_FX6_SL_ATT0 | 0x40010990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX6_SL_ATT1 | 0x40010994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX6_SL_ATT2 | 0x40010998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX6_SL_ATT3 | 0x4001099C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX6_MS_ADDR | 0x400109A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX6_MS_SIZE | 0x400109A4 | FULL | Master region, size |
| PERI_MS_PPU_FX6_MS_ATT0 | 0x400109B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX6_MS_ATT1 | 0x400109B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX6_MS_ATT2 | 0x400109B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX6_MS_ATT3 | 0x400109BC | FULL | Master attributes 3 |

21.24 PPU_FX 7

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX7_SL_ADDR | 0x400109C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX7_SL_SIZE | 0x400109C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX7_SL_ATT0 | 0x400109D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX7_SL_ATT1 | 0x400109D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX7_SL_ATT2 | 0x400109D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX7_SL_ATT3 | 0x400109DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX7_MS_ADDR | 0x400109E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX7_MS_SIZE | 0x400109E4 | FULL | Master region, size |
| PERI_MS_PPU_FX7_MS_ATT0 | 0x400109F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX7_MS_ATT1 | 0x400109F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX7_MS_ATT2 | 0x400109F8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX7_MS_ATT3 | 0x400109FC | FULL | Master attributes 3 |

21.25 PPU_FX 8

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX8_SL_ADDR | 0x40010A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX8_SL_SIZE | 0x40010A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX8_SL_ATT0 | 0x40010A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX8_SL_ATT1 | 0x40010A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX8_SL_ATT2 | 0x40010A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX8_SL_ATT3 | 0x40010A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX8_MS_ADDR | 0x40010A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX8_MS_SIZE | 0x40010A24 | FULL | Master region, size |
| PERI_MS_PPU_FX8_MS_ATT0 | 0x40010A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX8_MS_ATT1 | 0x40010A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX8_MS_ATT2 | 0x40010A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX8_MS_ATT3 | 0x40010A3C | FULL | Master attributes 3 |

21.26 PPU_FX 9

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX9_SL_ADDR | 0x40010A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX9_SL_SIZE | 0x40010A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX9_SL_ATT0 | 0x40010A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX9_SL_ATT1 | 0x40010A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX9_SL_ATT2 | 0x40010A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX9_SL_ATT3 | 0x40010A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX9_MS_ADDR | 0x40010A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX9_MS_SIZE | 0x40010A64 | FULL | Master region, size |
| PERI_MS_PPU_FX9_MS_ATT0 | 0x40010A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX9_MS_ATT1 | 0x40010A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX9_MS_ATT2 | 0x40010A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX9_MS_ATT3 | 0x40010A7C | FULL | Master attributes 3 |

21.27 PPU_FX 10

| Register Name | Address | Permission | Description |
|--|------------|----------------------|-----------------------------|
| PERI_MS_PPU_FX10_SL_ADDR | 0x40010A80 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX10_SL_SIZE | 0x40010A84 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX10_SL_ATT0 | 0x40010A90 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX10_SL_ATT1 | 0x40010A94 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX10_SL_ATT2 | 0x40010A98 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX10_SL_ATT3 | 0x40010A9C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX10_MS_ADDR | 0x40010AA0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX10_MS_SIZE | 0x40010AA4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX10_MS_ATT0 | 0x40010AB0 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX10_MS_ATT1 | 0x40010AB4 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX10_MS_ATT2 | 0x40010AB8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX10_MS_ATT3 | 0x40010ABC | PRIVILEGE - WRITE | Master attributes 3 |

21.28 PPU_FX 11

| Register Name | Address | Permission | Description |
|--|------------|----------------------|-----------------------------|
| PERI_MS_PPU_FX11_SL_ADDR | 0x40010AC0 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX11_SL_SIZE | 0x40010AC4 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX11_SL_ATT0 | 0x40010AD0 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX11_SL_ATT1 | 0x40010AD4 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX11_SL_ATT2 | 0x40010AD8 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX11_SL_ATT3 | 0x40010ADC | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX11_MS_ADDR | 0x40010AE0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX11_MS_SIZE | 0x40010AE4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX11_MS_ATT0 | 0x40010AF0 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX11_MS_ATT1 | 0x40010AF4 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX11_MS_ATT2 | 0x40010AF8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX11_MS_ATT3 | 0x40010AFC | PRIVILEGE - WRITE | Master attributes 3 |

21.29 PPU_FX 12

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX12_SL_ADDR | 0x40010B00 | READ | Slave region, base address |
| PERI_MS_PPU_FX12_SL_SIZE | 0x40010B04 | READ | Slave region, size |
| PERI_MS_PPU_FX12_SL_ATT0 | 0x40010B10 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX12_SL_ATT1 | 0x40010B14 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX12_SL_ATT2 | 0x40010B18 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX12_SL_ATT3 | 0x40010B1C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX12_MS_ADDR | 0x40010B20 | READ | Master region, base address |
| PERI_MS_PPU_FX12_MS_SIZE | 0x40010B24 | READ | Master region, size |
| PERI_MS_PPU_FX12_MS_ATT0 | 0x40010B30 | READ | Master attributes 0 |
| PERI_MS_PPU_FX12_MS_ATT1 | 0x40010B34 | READ | Master attributes 1 |
| PERI_MS_PPU_FX12_MS_ATT2 | 0x40010B38 | READ | Master attributes 2 |
| PERI_MS_PPU_FX12_MS_ATT3 | 0x40010B3C | READ | Master attributes 3 |

21.30 PPU_FX 13

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX13_SL_ADDR | 0x40010B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX13_SL_SIZE | 0x40010B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX13_SL_ATT0 | 0x40010B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX13_SL_ATT1 | 0x40010B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX13_SL_ATT2 | 0x40010B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX13_SL_ATT3 | 0x40010B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX13_MS_ADDR | 0x40010B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX13_MS_SIZE | 0x40010B64 | FULL | Master region, size |
| PERI_MS_PPU_FX13_MS_ATT0 | 0x40010B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX13_MS_ATT1 | 0x40010B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX13_MS_ATT2 | 0x40010B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX13_MS_ATT3 | 0x40010B7C | FULL | Master attributes 3 |

21.31 PPU_FX 14

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PERI_MS_PPU_FX14_SL_ADDR | 0x40010B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX14_SL_SIZE | 0x40010B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX14_SL_ATT0 | 0x40010B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX14_SL_ATT1 | 0x40010B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX14_SL_ATT2 | 0x40010B98 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX14_SL_ATT3 | 0x40010B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX14_MS_ADDR | 0x40010BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX14_MS_SIZE | 0x40010BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX14_MS_ATT0 | 0x40010BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX14_MS_ATT1 | 0x40010BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX14_MS_ATT2 | 0x40010BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX14_MS_ATT3 | 0x40010BBC | FULL | Master attributes 3 |

21.32 PPU_FX 15

| Register Name | Address | Permission | Description |
|--|------------|----------------------|-----------------------------|
| PERI_MS_PPU_FX15_SL_ADDR | 0x40010BC0 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX15_SL_SIZE | 0x40010BC4 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX15_SL_ATT0 | 0x40010BD0 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX15_SL_ATT1 | 0x40010BD4 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX15_SL_ATT2 | 0x40010BD8 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX15_SL_ATT3 | 0x40010BDC | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX15_MS_ADDR | 0x40010BE0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX15_MS_SIZE | 0x40010BE4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX15_MS_ATT0 | 0x40010BF0 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX15_MS_ATT1 | 0x40010BF4 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX15_MS_ATT2 | 0x40010BF8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX15_MS_ATT3 | 0x40010BFC | PRIVILEGE - WRITE | Master attributes 3 |

21.33 PPU_FX 16

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX16_SL_ADDR | 0x40010C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX16_SL_SIZE | 0x40010C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX16_SL_ATT0 | 0x40010C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX16_SL_ATT1 | 0x40010C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX16_SL_ATT2 | 0x40010C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX16_SL_ATT3 | 0x40010C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX16_MS_ADDR | 0x40010C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX16_MS_SIZE | 0x40010C24 | FULL | Master region, size |
| PERI_MS_PPU_FX16_MS_ATT0 | 0x40010C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX16_MS_ATT1 | 0x40010C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX16_MS_ATT2 | 0x40010C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX16_MS_ATT3 | 0x40010C3C | FULL | Master attributes 3 |

21.34 PPU_FX 17

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX17_SL_ADDR | 0x40010C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX17_SL_SIZE | 0x40010C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX17_SL_ATT0 | 0x40010C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX17_SL_ATT1 | 0x40010C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX17_SL_ATT2 | 0x40010C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX17_SL_ATT3 | 0x40010C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX17_MS_ADDR | 0x40010C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX17_MS_SIZE | 0x40010C64 | FULL | Master region, size |
| PERI_MS_PPU_FX17_MS_ATT0 | 0x40010C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX17_MS_ATT1 | 0x40010C74 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|--|------------|------------|---------------------|
| PERI_MS_PPU_FX17_MS_ATT2 | 0x40010C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX17_MS_ATT3 | 0x40010C7C | FULL | Master attributes 3 |

21.35 PPU_FX 18

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX18_SL_ADDR | 0x40010C80 | READ | Slave region, base address |
| PERI_MS_PPU_FX18_SL_SIZE | 0x40010C84 | READ | Slave region, size |
| PERI_MS_PPU_FX18_SL_ATT0 | 0x40010C90 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX18_SL_ATT1 | 0x40010C94 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX18_SL_ATT2 | 0x40010C98 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX18_SL_ATT3 | 0x40010C9C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX18_MS_ADDR | 0x40010CA0 | READ | Master region, base address |
| PERI_MS_PPU_FX18_MS_SIZE | 0x40010CA4 | READ | Master region, size |
| PERI_MS_PPU_FX18_MS_ATT0 | 0x40010CB0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX18_MS_ATT1 | 0x40010CB4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX18_MS_ATT2 | 0x40010CB8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX18_MS_ATT3 | 0x40010CBC | READ | Master attributes 3 |

21.36 PPU_FX 19

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX19_SL_ADDR | 0x40010CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX19_SL_SIZE | 0x40010CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX19_SL_ATT0 | 0x40010CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX19_SL_ATT1 | 0x40010CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX19_SL_ATT2 | 0x40010CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX19_SL_ATT3 | 0x40010CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX19_MS_ADDR | 0x40010CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX19_MS_SIZE | 0x40010CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX19_MS_ATT0 | 0x40010CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX19_MS_ATT1 | 0x40010CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX19_MS_ATT2 | 0x40010CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX19_MS_ATT3 | 0x40010CFC | FULL | Master attributes 3 |

21.37 PPU_FX 20

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX20_SL_ADDR | 0x40010D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX20_SL_SIZE | 0x40010D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX20_SL_ATT0 | 0x40010D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX20_SL_ATT1 | 0x40010D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX20_SL_ATT2 | 0x40010D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX20_SL_ATT3 | 0x40010D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX20_MS_ADDR | 0x40010D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX20_MS_SIZE | 0x40010D24 | FULL | Master region, size |
| PERI_MS_PPU_FX20_MS_ATT0 | 0x40010D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX20_MS_ATT1 | 0x40010D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX20_MS_ATT2 | 0x40010D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX20_MS_ATT3 | 0x40010D3C | FULL | Master attributes 3 |

21.38 PPU_FX 21

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX21_SL_ADDR | 0x40010D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX21_SL_SIZE | 0x40010D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX21_SL_ATT0 | 0x40010D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX21_SL_ATT1 | 0x40010D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX21_SL_ATT2 | 0x40010D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX21_SL_ATT3 | 0x40010D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX21_MS_ADDR | 0x40010D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX21_MS_SIZE | 0x40010D64 | FULL | Master region, size |
| PERI_MS_PPU_FX21_MS_ATT0 | 0x40010D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX21_MS_ATT1 | 0x40010D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX21_MS_ATT2 | 0x40010D78 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX21_MS_ATT3 | 0x40010D7C | FULL | Master attributes 3 |

21.39 PPU_FX 22

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX22_SL_ADDR | 0x40010D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX22_SL_SIZE | 0x40010D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX22_SL_ATT0 | 0x40010D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX22_SL_ATT1 | 0x40010D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX22_SL_ATT2 | 0x40010D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX22_SL_ATT3 | 0x40010D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX22_MS_ADDR | 0x40010DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX22_MS_SIZE | 0x40010DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX22_MS_ATT0 | 0x40010DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX22_MS_ATT1 | 0x40010DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX22_MS_ATT2 | 0x40010DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX22_MS_ATT3 | 0x40010DBC | FULL | Master attributes 3 |

21.40 PPU_FX 23

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX23_SL_ADDR | 0x40010DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX23_SL_SIZE | 0x40010DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX23_SL_ATT0 | 0x40010DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX23_SL_ATT1 | 0x40010DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX23_SL_ATT2 | 0x40010DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX23_SL_ATT3 | 0x40010DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX23_MS_ADDR | 0x40010DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX23_MS_SIZE | 0x40010DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX23_MS_ATT0 | 0x40010DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX23_MS_ATT1 | 0x40010DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX23_MS_ATT2 | 0x40010DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX23_MS_ATT3 | 0x40010DFC | FULL | Master attributes 3 |

21.41 PPU_FX 24

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX24_SL_ADDR | 0x40010E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX24_SL_SIZE | 0x40010E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX24_SL_ATT0 | 0x40010E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX24_SL_ATT1 | 0x40010E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX24_SL_ATT2 | 0x40010E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX24_SL_ATT3 | 0x40010E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX24_MS_ADDR | 0x40010E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX24_MS_SIZE | 0x40010E24 | FULL | Master region, size |
| PERI_MS_PPU_FX24_MS_ATT0 | 0x40010E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX24_MS_ATT1 | 0x40010E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX24_MS_ATT2 | 0x40010E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX24_MS_ATT3 | 0x40010E3C | FULL | Master attributes 3 |

21.42 PPU_FX 25

| Register Name | Address | Permission | Description |
|--------------------------|------------|----------------------|----------------------------|
| PERI_MS_PPU_FX25_SL_ADDR | 0x40010E40 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX25_SL_SIZE | 0x40010E44 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX25_SL_ATT0 | 0x40010E50 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX25_SL_ATT1 | 0x40010E54 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX25_SL_ATT2 | 0x40010E58 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX25_SL_ATT3 | 0x40010E5C | PRIVILEGE - WRITE | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|--|------------|----------------------|-----------------------------|
| PERI_MS_PPU_FX25_MS_ADDR | 0x40010E60 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX25_MS_SIZE | 0x40010E64 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX25_MS_ATT0 | 0x40010E70 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX25_MS_ATT1 | 0x40010E74 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX25_MS_ATT2 | 0x40010E78 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX25_MS_ATT3 | 0x40010E7C | PRIVILEGE - WRITE | Master attributes 3 |

21.43 PPU_FX 26

| Register Name | Address | Permission | Description |
|--|------------|----------------------|-----------------------------|
| PERI_MS_PPU_FX26_SL_ADDR | 0x40010E80 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX26_SL_SIZE | 0x40010E84 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX26_SL_ATT0 | 0x40010E90 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX26_SL_ATT1 | 0x40010E94 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX26_SL_ATT2 | 0x40010E98 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX26_SL_ATT3 | 0x40010E9C | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX26_MS_ADDR | 0x40010EA0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX26_MS_SIZE | 0x40010EA4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX26_MS_ATT0 | 0x40010EB0 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX26_MS_ATT1 | 0x40010EB4 | PRIVILEGE - WRITE | Master attributes 1 |
| PERI_MS_PPU_FX26_MS_ATT2 | 0x40010EB8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX26_MS_ATT3 | 0x40010EBC | PRIVILEGE - WRITE | Master attributes 3 |

21.44 PPU_FX 27

| Register Name | Address | Permission | Description |
|--|------------|----------------------|-----------------------------|
| PERI_MS_PPU_FX27_SL_ADDR | 0x40010EC0 | PRIVILEGE - WRITE | Slave region, base address |
| PERI_MS_PPU_FX27_SL_SIZE | 0x40010EC4 | PRIVILEGE - WRITE | Slave region, size |
| PERI_MS_PPU_FX27_SL_ATT0 | 0x40010ED0 | PRIVILEGE - WRITE | Slave attributes 0 |
| PERI_MS_PPU_FX27_SL_ATT1 | 0x40010ED4 | PRIVILEGE - WRITE | Slave attributes 1 |
| PERI_MS_PPU_FX27_SL_ATT2 | 0x40010ED8 | PRIVILEGE - WRITE | Slave attributes 2 |
| PERI_MS_PPU_FX27_SL_ATT3 | 0x40010EDC | PRIVILEGE - WRITE | Slave attributes 3 |
| PERI_MS_PPU_FX27_MS_ADDR | 0x40010EE0 | PRIVILEGE - WRITE | Master region, base address |
| PERI_MS_PPU_FX27_MS_SIZE | 0x40010EE4 | PRIVILEGE - WRITE | Master region, size |
| PERI_MS_PPU_FX27_MS_ATT0 | 0x40010EF0 | PRIVILEGE - WRITE | Master attributes 0 |
| PERI_MS_PPU_FX27_MS_ATT1 | 0x40010EF4 | PRIVILEGE - WRITE | Master attributes 1 |

| Register Name | Address | Permission | Description |
|--|------------|----------------------|---------------------|
| PERI_MS_PPU_FX27_MS_ATT2 | 0x40010EF8 | PRIVILEGE - WRITE | Master attributes 2 |
| PERI_MS_PPU_FX27_MS_ATT3 | 0x40010EFC | PRIVILEGE - WRITE | Master attributes 3 |

21.45 PPU_FX 28

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX28_SL_ADDR | 0x40010F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX28_SL_SIZE | 0x40010F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX28_SL_ATT0 | 0x40010F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX28_SL_ATT1 | 0x40010F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX28_SL_ATT2 | 0x40010F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX28_SL_ATT3 | 0x40010F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX28_MS_ADDR | 0x40010F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX28_MS_SIZE | 0x40010F24 | FULL | Master region, size |
| PERI_MS_PPU_FX28_MS_ATT0 | 0x40010F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX28_MS_ATT1 | 0x40010F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX28_MS_ATT2 | 0x40010F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX28_MS_ATT3 | 0x40010F3C | FULL | Master attributes 3 |

21.46 PPU_FX 29

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX29_SL_ADDR | 0x40010F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX29_SL_SIZE | 0x40010F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX29_SL_ATT0 | 0x40010F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX29_SL_ATT1 | 0x40010F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX29_SL_ATT2 | 0x40010F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX29_SL_ATT3 | 0x40010F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX29_MS_ADDR | 0x40010F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX29_MS_SIZE | 0x40010F64 | FULL | Master region, size |
| PERI_MS_PPU_FX29_MS_ATT0 | 0x40010F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX29_MS_ATT1 | 0x40010F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX29_MS_ATT2 | 0x40010F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX29_MS_ATT3 | 0x40010F7C | FULL | Master attributes 3 |

21.47 PPU_FX 30

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX30_SL_ADDR | 0x40010F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX30_SL_SIZE | 0x40010F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX30_SL_ATT0 | 0x40010F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX30_SL_ATT1 | 0x40010F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX30_SL_ATT2 | 0x40010F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX30_SL_ATT3 | 0x40010F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX30_MS_ADDR | 0x40010FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX30_MS_SIZE | 0x40010FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX30_MS_ATT0 | 0x40010FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX30_MS_ATT1 | 0x40010FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX30_MS_ATT2 | 0x40010FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX30_MS_ATT3 | 0x40010FBC | FULL | Master attributes 3 |

21.48 PPU_FX 31

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX31_SL_ADDR | 0x40010FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX31_SL_SIZE | 0x40010FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX31_SL_ATT0 | 0x40010FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX31_SL_ATT1 | 0x40010FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX31_SL_ATT2 | 0x40010FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX31_SL_ATT3 | 0x40010FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX31_MS_ADDR | 0x40010FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX31_MS_SIZE | 0x40010FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX31_MS_ATT0 | 0x40010FF0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|--|------------|------------|---------------------|
| PERI_MS_PPU_FX31_MS_ATT1 | 0x40010FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX31_MS_ATT2 | 0x40010FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX31_MS_ATT3 | 0x40010FFC | FULL | Master attributes 3 |

21.49 PPU_FX 32

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX32_SL_ADDR | 0x40011000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX32_SL_SIZE | 0x40011004 | FULL | Slave region, size |
| PERI_MS_PPU_FX32_SL_ATT0 | 0x40011010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX32_SL_ATT1 | 0x40011014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX32_SL_ATT2 | 0x40011018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX32_SL_ATT3 | 0x4001101C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX32_MS_ADDR | 0x40011020 | FULL | Master region, base address |
| PERI_MS_PPU_FX32_MS_SIZE | 0x40011024 | FULL | Master region, size |
| PERI_MS_PPU_FX32_MS_ATT0 | 0x40011030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX32_MS_ATT1 | 0x40011034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX32_MS_ATT2 | 0x40011038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX32_MS_ATT3 | 0x4001103C | FULL | Master attributes 3 |

21.50 PPU_FX 33

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX33_SL_ADDR | 0x40011040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX33_SL_SIZE | 0x40011044 | FULL | Slave region, size |
| PERI_MS_PPU_FX33_SL_ATT0 | 0x40011050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX33_SL_ATT1 | 0x40011054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX33_SL_ATT2 | 0x40011058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX33_SL_ATT3 | 0x4001105C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX33_MS_ADDR | 0x40011060 | FULL | Master region, base address |
| PERI_MS_PPU_FX33_MS_SIZE | 0x40011064 | FULL | Master region, size |
| PERI_MS_PPU_FX33_MS_ATT0 | 0x40011070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX33_MS_ATT1 | 0x40011074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX33_MS_ATT2 | 0x40011078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX33_MS_ATT3 | 0x4001107C | FULL | Master attributes 3 |

21.51 PPU_FX 34

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX34_SL_ADDR | 0x40011080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX34_SL_SIZE | 0x40011084 | FULL | Slave region, size |
| PERI_MS_PPU_FX34_SL_ATT0 | 0x40011090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX34_SL_ATT1 | 0x40011094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX34_SL_ATT2 | 0x40011098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX34_SL_ATT3 | 0x4001109C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX34_MS_ADDR | 0x400110A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX34_MS_SIZE | 0x400110A4 | FULL | Master region, size |
| PERI_MS_PPU_FX34_MS_ATT0 | 0x400110B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX34_MS_ATT1 | 0x400110B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX34_MS_ATT2 | 0x400110B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX34_MS_ATT3 | 0x400110BC | FULL | Master attributes 3 |

21.52 PPU_FX 35

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX35_SL_ADDR | 0x400110C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX35_SL_SIZE | 0x400110C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX35_SL_ATT0 | 0x400110D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX35_SL_ATT1 | 0x400110D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX35_SL_ATT2 | 0x400110D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX35_SL_ATT3 | 0x400110DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX35_MS_ADDR | 0x400110E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX35_MS_SIZE | 0x400110E4 | FULL | Master region, size |
| PERI_MS_PPU_FX35_MS_ATT0 | 0x400110F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX35_MS_ATT1 | 0x400110F4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|--|------------|------------|---------------------|
| PERI_MS_PPU_FX35_MS_ATT2 | 0x400110F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX35_MS_ATT3 | 0x400110FC | FULL | Master attributes 3 |

21.53 PPU_FX 36

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX36_SL_ADDR | 0x40011100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX36_SL_SIZE | 0x40011104 | FULL | Slave region, size |
| PERI_MS_PPU_FX36_SL_ATT0 | 0x40011110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX36_SL_ATT1 | 0x40011114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX36_SL_ATT2 | 0x40011118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX36_SL_ATT3 | 0x4001111C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX36_MS_ADDR | 0x40011120 | FULL | Master region, base address |
| PERI_MS_PPU_FX36_MS_SIZE | 0x40011124 | FULL | Master region, size |
| PERI_MS_PPU_FX36_MS_ATT0 | 0x40011130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX36_MS_ATT1 | 0x40011134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX36_MS_ATT2 | 0x40011138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX36_MS_ATT3 | 0x4001113C | FULL | Master attributes 3 |

21.54 PPU_FX 37

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX37_SL_ADDR | 0x40011140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX37_SL_SIZE | 0x40011144 | FULL | Slave region, size |
| PERI_MS_PPU_FX37_SL_ATT0 | 0x40011150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX37_SL_ATT1 | 0x40011154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX37_SL_ATT2 | 0x40011158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX37_SL_ATT3 | 0x4001115C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX37_MS_ADDR | 0x40011160 | FULL | Master region, base address |
| PERI_MS_PPU_FX37_MS_SIZE | 0x40011164 | FULL | Master region, size |
| PERI_MS_PPU_FX37_MS_ATT0 | 0x40011170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX37_MS_ATT1 | 0x40011174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX37_MS_ATT2 | 0x40011178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX37_MS_ATT3 | 0x4001117C | FULL | Master attributes 3 |

21.55 PPU_FX 38

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX38_SL_ADDR | 0x40011180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX38_SL_SIZE | 0x40011184 | FULL | Slave region, size |
| PERI_MS_PPU_FX38_SL_ATT0 | 0x40011190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX38_SL_ATT1 | 0x40011194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX38_SL_ATT2 | 0x40011198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX38_SL_ATT3 | 0x4001119C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX38_MS_ADDR | 0x400111A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX38_MS_SIZE | 0x400111A4 | FULL | Master region, size |
| PERI_MS_PPU_FX38_MS_ATT0 | 0x400111B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX38_MS_ATT1 | 0x400111B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX38_MS_ATT2 | 0x400111B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX38_MS_ATT3 | 0x400111BC | FULL | Master attributes 3 |

21.56 PPU_FX 39

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX39_SL_ADDR | 0x400111C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX39_SL_SIZE | 0x400111C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX39_SL_ATT0 | 0x400111D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX39_SL_ATT1 | 0x400111D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX39_SL_ATT2 | 0x400111D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX39_SL_ATT3 | 0x400111DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX39_MS_ADDR | 0x400111E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX39_MS_SIZE | 0x400111E4 | FULL | Master region, size |
| PERI_MS_PPU_FX39_MS_ATT0 | 0x400111F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX39_MS_ATT1 | 0x400111F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX39_MS_ATT2 | 0x400111F8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX39_MS_ATT3 | 0x400111FC | FULL | Master attributes 3 |

21.57 PPU_FX 40

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX40_SL_ADDR | 0x40011200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX40_SL_SIZE | 0x40011204 | FULL | Slave region, size |
| PERI_MS_PPU_FX40_SL_ATT0 | 0x40011210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX40_SL_ATT1 | 0x40011214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX40_SL_ATT2 | 0x40011218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX40_SL_ATT3 | 0x4001121C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX40_MS_ADDR | 0x40011220 | FULL | Master region, base address |
| PERI_MS_PPU_FX40_MS_SIZE | 0x40011224 | FULL | Master region, size |
| PERI_MS_PPU_FX40_MS_ATT0 | 0x40011230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX40_MS_ATT1 | 0x40011234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX40_MS_ATT2 | 0x40011238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX40_MS_ATT3 | 0x4001123C | FULL | Master attributes 3 |

21.58 PPU_FX 41

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX41_SL_ADDR | 0x40011240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX41_SL_SIZE | 0x40011244 | FULL | Slave region, size |
| PERI_MS_PPU_FX41_SL_ATT0 | 0x40011250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX41_SL_ATT1 | 0x40011254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX41_SL_ATT2 | 0x40011258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX41_SL_ATT3 | 0x4001125C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX41_MS_ADDR | 0x40011260 | FULL | Master region, base address |
| PERI_MS_PPU_FX41_MS_SIZE | 0x40011264 | FULL | Master region, size |
| PERI_MS_PPU_FX41_MS_ATT0 | 0x40011270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX41_MS_ATT1 | 0x40011274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX41_MS_ATT2 | 0x40011278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX41_MS_ATT3 | 0x4001127C | FULL | Master attributes 3 |

21.59 PPU_FX 42

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX42_SL_ADDR | 0x40011280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX42_SL_SIZE | 0x40011284 | FULL | Slave region, size |
| PERI_MS_PPU_FX42_SL_ATT0 | 0x40011290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX42_SL_ATT1 | 0x40011294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX42_SL_ATT2 | 0x40011298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX42_SL_ATT3 | 0x4001129C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX42_MS_ADDR | 0x400112A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX42_MS_SIZE | 0x400112A4 | FULL | Master region, size |
| PERI_MS_PPU_FX42_MS_ATT0 | 0x400112B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX42_MS_ATT1 | 0x400112B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX42_MS_ATT2 | 0x400112B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX42_MS_ATT3 | 0x400112BC | FULL | Master attributes 3 |

21.60 PPU_FX 43

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX43_SL_ADDR | 0x400112C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX43_SL_SIZE | 0x400112C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX43_SL_ATT0 | 0x400112D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX43_SL_ATT1 | 0x400112D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX43_SL_ATT2 | 0x400112D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX43_SL_ATT3 | 0x400112DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX43_MS_ADDR | 0x400112E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX43_MS_SIZE | 0x400112E4 | FULL | Master region, size |
| PERI_MS_PPU_FX43_MS_ATT0 | 0x400112F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX43_MS_ATT1 | 0x400112F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX43_MS_ATT2 | 0x400112F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX43_MS_ATT3 | 0x400112FC | FULL | Master attributes 3 |

21.61 PPU_FX 44

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX44_SL_ADDR | 0x40011300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX44_SL_SIZE | 0x40011304 | FULL | Slave region, size |
| PERI_MS_PPU_FX44_SL_ATT0 | 0x40011310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX44_SL_ATT1 | 0x40011314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX44_SL_ATT2 | 0x40011318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX44_SL_ATT3 | 0x4001131C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX44_MS_ADDR | 0x40011320 | FULL | Master region, base address |
| PERI_MS_PPU_FX44_MS_SIZE | 0x40011324 | FULL | Master region, size |
| PERI_MS_PPU_FX44_MS_ATT0 | 0x40011330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX44_MS_ATT1 | 0x40011334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX44_MS_ATT2 | 0x40011338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX44_MS_ATT3 | 0x4001133C | FULL | Master attributes 3 |

21.62 PPU_FX 45

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX45_SL_ADDR | 0x40011340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX45_SL_SIZE | 0x40011344 | FULL | Slave region, size |
| PERI_MS_PPU_FX45_SL_ATT0 | 0x40011350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX45_SL_ATT1 | 0x40011354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX45_SL_ATT2 | 0x40011358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX45_SL_ATT3 | 0x4001135C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX45_MS_ADDR | 0x40011360 | FULL | Master region, base address |
| PERI_MS_PPU_FX45_MS_SIZE | 0x40011364 | FULL | Master region, size |
| PERI_MS_PPU_FX45_MS_ATT0 | 0x40011370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX45_MS_ATT1 | 0x40011374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX45_MS_ATT2 | 0x40011378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX45_MS_ATT3 | 0x4001137C | FULL | Master attributes 3 |

21.63 PPU_FX 46

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX46_SL_ADDR | 0x40011380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX46_SL_SIZE | 0x40011384 | FULL | Slave region, size |
| PERI_MS_PPU_FX46_SL_ATT0 | 0x40011390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX46_SL_ATT1 | 0x40011394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX46_SL_ATT2 | 0x40011398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX46_SL_ATT3 | 0x4001139C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX46_MS_ADDR | 0x400113A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX46_MS_SIZE | 0x400113A4 | FULL | Master region, size |
| PERI_MS_PPU_FX46_MS_ATT0 | 0x400113B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX46_MS_ATT1 | 0x400113B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX46_MS_ATT2 | 0x400113B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX46_MS_ATT3 | 0x400113BC | FULL | Master attributes 3 |

21.64 PPU_FX 47

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX47_SL_ADDR | 0x400113C0 | READ | Slave region, base address |
| PERI_MS_PPU_FX47_SL_SIZE | 0x400113C4 | READ | Slave region, size |
| PERI_MS_PPU_FX47_SL_ATT0 | 0x400113D0 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX47_SL_ATT1 | 0x400113D4 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX47_SL_ATT2 | 0x400113D8 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX47_SL_ATT3 | 0x400113DC | READ | Slave attributes 3 |
| PERI_MS_PPU_FX47_MS_ADDR | 0x400113E0 | READ | Master region, base address |
| PERI_MS_PPU_FX47_MS_SIZE | 0x400113E4 | READ | Master region, size |
| PERI_MS_PPU_FX47_MS_ATT0 | 0x400113F0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX47_MS_ATT1 | 0x400113F4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX47_MS_ATT2 | 0x400113F8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX47_MS_ATT3 | 0x400113FC | READ | Master attributes 3 |

21.65 PPU_FX 48

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX48_SL_ADDR | 0x40011400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX48_SL_SIZE | 0x40011404 | FULL | Slave region, size |
| PERI_MS_PPU_FX48_SL_ATT0 | 0x40011410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX48_SL_ATT1 | 0x40011414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX48_SL_ATT2 | 0x40011418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX48_SL_ATT3 | 0x4001141C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX48_MS_ADDR | 0x40011420 | FULL | Master region, base address |
| PERI_MS_PPU_FX48_MS_SIZE | 0x40011424 | FULL | Master region, size |
| PERI_MS_PPU_FX48_MS_ATT0 | 0x40011430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX48_MS_ATT1 | 0x40011434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX48_MS_ATT2 | 0x40011438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX48_MS_ATT3 | 0x4001143C | FULL | Master attributes 3 |

21.66 PPU_FX 49

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX49_SL_ADDR | 0x40011440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX49_SL_SIZE | 0x40011444 | FULL | Slave region, size |
| PERI_MS_PPU_FX49_SL_ATT0 | 0x40011450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX49_SL_ATT1 | 0x40011454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX49_SL_ATT2 | 0x40011458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX49_SL_ATT3 | 0x4001145C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX49_MS_ADDR | 0x40011460 | FULL | Master region, base address |
| PERI_MS_PPU_FX49_MS_SIZE | 0x40011464 | FULL | Master region, size |
| PERI_MS_PPU_FX49_MS_ATT0 | 0x40011470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX49_MS_ATT1 | 0x40011474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX49_MS_ATT2 | 0x40011478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX49_MS_ATT3 | 0x4001147C | FULL | Master attributes 3 |

21.67 PPU_FX 50

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX50_SL_ADDR | 0x40011480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX50_SL_SIZE | 0x40011484 | FULL | Slave region, size |
| PERI_MS_PPU_FX50_SL_ATT0 | 0x40011490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX50_SL_ATT1 | 0x40011494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX50_SL_ATT2 | 0x40011498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX50_SL_ATT3 | 0x4001149C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX50_MS_ADDR | 0x400114A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX50_MS_SIZE | 0x400114A4 | FULL | Master region, size |
| PERI_MS_PPU_FX50_MS_ATT0 | 0x400114B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX50_MS_ATT1 | 0x400114B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX50_MS_ATT2 | 0x400114B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX50_MS_ATT3 | 0x400114BC | FULL | Master attributes 3 |

21.68 PPU_FX 51

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX51_SL_ADDR | 0x400114C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX51_SL_SIZE | 0x400114C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX51_SL_ATT0 | 0x400114D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX51_SL_ATT1 | 0x400114D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX51_SL_ATT2 | 0x400114D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX51_SL_ATT3 | 0x400114DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX51_MS_ADDR | 0x400114E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX51_MS_SIZE | 0x400114E4 | FULL | Master region, size |
| PERI_MS_PPU_FX51_MS_ATT0 | 0x400114F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX51_MS_ATT1 | 0x400114F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX51_MS_ATT2 | 0x400114F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX51_MS_ATT3 | 0x400114FC | FULL | Master attributes 3 |

21.69 PPU_FX 52

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PERI_MS_PPU_FX52_SL_ADDR | 0x40011500 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX52_SL_SIZE | 0x40011504 | FULL | Slave region, size |
| PERI_MS_PPU_FX52_SL_ATT0 | 0x40011510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX52_SL_ATT1 | 0x40011514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX52_SL_ATT2 | 0x40011518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX52_SL_ATT3 | 0x4001151C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX52_MS_ADDR | 0x40011520 | FULL | Master region, base address |
| PERI_MS_PPU_FX52_MS_SIZE | 0x40011524 | FULL | Master region, size |
| PERI_MS_PPU_FX52_MS_ATT0 | 0x40011530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX52_MS_ATT1 | 0x40011534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX52_MS_ATT2 | 0x40011538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX52_MS_ATT3 | 0x4001153C | FULL | Master attributes 3 |

21.70 PPU_FX 53

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX53_SL_ADDR | 0x40011540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX53_SL_SIZE | 0x40011544 | FULL | Slave region, size |
| PERI_MS_PPU_FX53_SL_ATT0 | 0x40011550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX53_SL_ATT1 | 0x40011554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX53_SL_ATT2 | 0x40011558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX53_SL_ATT3 | 0x4001155C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX53_MS_ADDR | 0x40011560 | FULL | Master region, base address |
| PERI_MS_PPU_FX53_MS_SIZE | 0x40011564 | FULL | Master region, size |
| PERI_MS_PPU_FX53_MS_ATT0 | 0x40011570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX53_MS_ATT1 | 0x40011574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX53_MS_ATT2 | 0x40011578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX53_MS_ATT3 | 0x4001157C | FULL | Master attributes 3 |

21.71 PPU_FX 54

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX54_SL_ADDR | 0x40011580 | READ | Slave region, base address |
| PERI_MS_PPU_FX54_SL_SIZE | 0x40011584 | READ | Slave region, size |
| PERI_MS_PPU_FX54_SL_ATT0 | 0x40011590 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX54_SL_ATT1 | 0x40011594 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX54_SL_ATT2 | 0x40011598 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX54_SL_ATT3 | 0x4001159C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX54_MS_ADDR | 0x400115A0 | READ | Master region, base address |
| PERI_MS_PPU_FX54_MS_SIZE | 0x400115A4 | READ | Master region, size |
| PERI_MS_PPU_FX54_MS_ATT0 | 0x400115B0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX54_MS_ATT1 | 0x400115B4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX54_MS_ATT2 | 0x400115B8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX54_MS_ATT3 | 0x400115BC | READ | Master attributes 3 |

21.72 PPU_FX 55

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX55_SL_ADDR | 0x400115C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX55_SL_SIZE | 0x400115C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX55_SL_ATT0 | 0x400115D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX55_SL_ATT1 | 0x400115D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX55_SL_ATT2 | 0x400115D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX55_SL_ATT3 | 0x400115DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX55_MS_ADDR | 0x400115E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX55_MS_SIZE | 0x400115E4 | FULL | Master region, size |
| PERI_MS_PPU_FX55_MS_ATT0 | 0x400115F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX55_MS_ATT1 | 0x400115F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX55_MS_ATT2 | 0x400115F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX55_MS_ATT3 | 0x400115FC | FULL | Master attributes 3 |

21.73 PPU_FX 56

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PERI_MS_PPU_FX56_SL_ADDR | 0x40011600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX56_SL_SIZE | 0x40011604 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX56_SL_ATT0 | 0x40011610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX56_SL_ATT1 | 0x40011614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX56_SL_ATT2 | 0x40011618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX56_SL_ATT3 | 0x4001161C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX56_MS_ADDR | 0x40011620 | FULL | Master region, base address |
| PERI_MS_PPU_FX56_MS_SIZE | 0x40011624 | FULL | Master region, size |
| PERI_MS_PPU_FX56_MS_ATT0 | 0x40011630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX56_MS_ATT1 | 0x40011634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX56_MS_ATT2 | 0x40011638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX56_MS_ATT3 | 0x4001163C | FULL | Master attributes 3 |

21.74 PPU_FX 57

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX57_SL_ADDR | 0x40011640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX57_SL_SIZE | 0x40011644 | FULL | Slave region, size |
| PERI_MS_PPU_FX57_SL_ATT0 | 0x40011650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX57_SL_ATT1 | 0x40011654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX57_SL_ATT2 | 0x40011658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX57_SL_ATT3 | 0x4001165C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX57_MS_ADDR | 0x40011660 | FULL | Master region, base address |
| PERI_MS_PPU_FX57_MS_SIZE | 0x40011664 | FULL | Master region, size |
| PERI_MS_PPU_FX57_MS_ATT0 | 0x40011670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX57_MS_ATT1 | 0x40011674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX57_MS_ATT2 | 0x40011678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX57_MS_ATT3 | 0x4001167C | FULL | Master attributes 3 |

21.75 PPU_FX 58

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX58_SL_ADDR | 0x40011680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX58_SL_SIZE | 0x40011684 | FULL | Slave region, size |
| PERI_MS_PPU_FX58_SL_ATT0 | 0x40011690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX58_SL_ATT1 | 0x40011694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX58_SL_ATT2 | 0x40011698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX58_SL_ATT3 | 0x4001169C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX58_MS_ADDR | 0x400116A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX58_MS_SIZE | 0x400116A4 | FULL | Master region, size |
| PERI_MS_PPU_FX58_MS_ATT0 | 0x400116B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX58_MS_ATT1 | 0x400116B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX58_MS_ATT2 | 0x400116B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX58_MS_ATT3 | 0x400116BC | FULL | Master attributes 3 |

21.76 PPU_FX 59

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX59_SL_ADDR | 0x400116C0 | READ | Slave region, base address |
| PERI_MS_PPU_FX59_SL_SIZE | 0x400116C4 | READ | Slave region, size |
| PERI_MS_PPU_FX59_SL_ATT0 | 0x400116D0 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX59_SL_ATT1 | 0x400116D4 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX59_SL_ATT2 | 0x400116D8 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX59_SL_ATT3 | 0x400116DC | READ | Slave attributes 3 |
| PERI_MS_PPU_FX59_MS_ADDR | 0x400116E0 | READ | Master region, base address |
| PERI_MS_PPU_FX59_MS_SIZE | 0x400116E4 | READ | Master region, size |
| PERI_MS_PPU_FX59_MS_ATT0 | 0x400116F0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX59_MS_ATT1 | 0x400116F4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX59_MS_ATT2 | 0x400116F8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX59_MS_ATT3 | 0x400116FC | READ | Master attributes 3 |

21.77 PPU_FX 60

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PERI_MS_PPU_FX60_SL_ADDR | 0x40011700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX60_SL_SIZE | 0x40011704 | FULL | Slave region, size |
| PERI_MS_PPU_FX60_SL_ATT0 | 0x40011710 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX60_SL_ATT1 | 0x40011714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX60_SL_ATT2 | 0x40011718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX60_SL_ATT3 | 0x4001171C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX60_MS_ADDR | 0x40011720 | FULL | Master region, base address |
| PERI_MS_PPU_FX60_MS_SIZE | 0x40011724 | FULL | Master region, size |
| PERI_MS_PPU_FX60_MS_ATT0 | 0x40011730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX60_MS_ATT1 | 0x40011734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX60_MS_ATT2 | 0x40011738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX60_MS_ATT3 | 0x4001173C | FULL | Master attributes 3 |

21.78 PPU_FX 61

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX61_SL_ADDR | 0x40011740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX61_SL_SIZE | 0x40011744 | FULL | Slave region, size |
| PERI_MS_PPU_FX61_SL_ATT0 | 0x40011750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX61_SL_ATT1 | 0x40011754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX61_SL_ATT2 | 0x40011758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX61_SL_ATT3 | 0x4001175C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX61_MS_ADDR | 0x40011760 | FULL | Master region, base address |
| PERI_MS_PPU_FX61_MS_SIZE | 0x40011764 | FULL | Master region, size |
| PERI_MS_PPU_FX61_MS_ATT0 | 0x40011770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX61_MS_ATT1 | 0x40011774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX61_MS_ATT2 | 0x40011778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX61_MS_ATT3 | 0x4001177C | FULL | Master attributes 3 |

21.79 PPU_FX 62

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX62_SL_ADDR | 0x40011780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX62_SL_SIZE | 0x40011784 | FULL | Slave region, size |
| PERI_MS_PPU_FX62_SL_ATT0 | 0x40011790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX62_SL_ATT1 | 0x40011794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX62_SL_ATT2 | 0x40011798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX62_SL_ATT3 | 0x4001179C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX62_MS_ADDR | 0x400117A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX62_MS_SIZE | 0x400117A4 | FULL | Master region, size |
| PERI_MS_PPU_FX62_MS_ATT0 | 0x400117B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX62_MS_ATT1 | 0x400117B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX62_MS_ATT2 | 0x400117B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX62_MS_ATT3 | 0x400117BC | FULL | Master attributes 3 |

21.80 PPU_FX 63

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX63_SL_ADDR | 0x400117C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX63_SL_SIZE | 0x400117C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX63_SL_ATT0 | 0x400117D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX63_SL_ATT1 | 0x400117D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX63_SL_ATT2 | 0x400117D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX63_SL_ATT3 | 0x400117DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX63_MS_ADDR | 0x400117E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX63_MS_SIZE | 0x400117E4 | FULL | Master region, size |
| PERI_MS_PPU_FX63_MS_ATT0 | 0x400117F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX63_MS_ATT1 | 0x400117F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX63_MS_ATT2 | 0x400117F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX63_MS_ATT3 | 0x400117FC | FULL | Master attributes 3 |

21.81 PPU_FX 64

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX64_SL_ADDR | 0x40011800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX64_SL_SIZE | 0x40011804 | FULL | Slave region, size |
| PERI_MS_PPU_FX64_SL_ATT0 | 0x40011810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX64_SL_ATT1 | 0x40011814 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX64_SL_ATT2 | 0x40011818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX64_SL_ATT3 | 0x4001181C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX64_MS_ADDR | 0x40011820 | FULL | Master region, base address |
| PERI_MS_PPU_FX64_MS_SIZE | 0x40011824 | FULL | Master region, size |
| PERI_MS_PPU_FX64_MS_ATT0 | 0x40011830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX64_MS_ATT1 | 0x40011834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX64_MS_ATT2 | 0x40011838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX64_MS_ATT3 | 0x4001183C | FULL | Master attributes 3 |

21.82 PPU_FX 65

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX65_SL_ADDR | 0x40011840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX65_SL_SIZE | 0x40011844 | FULL | Slave region, size |
| PERI_MS_PPU_FX65_SL_ATT0 | 0x40011850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX65_SL_ATT1 | 0x40011854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX65_SL_ATT2 | 0x40011858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX65_SL_ATT3 | 0x4001185C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX65_MS_ADDR | 0x40011860 | FULL | Master region, base address |
| PERI_MS_PPU_FX65_MS_SIZE | 0x40011864 | FULL | Master region, size |
| PERI_MS_PPU_FX65_MS_ATT0 | 0x40011870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX65_MS_ATT1 | 0x40011874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX65_MS_ATT2 | 0x40011878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX65_MS_ATT3 | 0x4001187C | FULL | Master attributes 3 |

21.83 PPU_FX 66

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX66_SL_ADDR | 0x40011880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX66_SL_SIZE | 0x40011884 | FULL | Slave region, size |
| PERI_MS_PPU_FX66_SL_ATT0 | 0x40011890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX66_SL_ATT1 | 0x40011894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX66_SL_ATT2 | 0x40011898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX66_SL_ATT3 | 0x4001189C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX66_MS_ADDR | 0x400118A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX66_MS_SIZE | 0x400118A4 | FULL | Master region, size |
| PERI_MS_PPU_FX66_MS_ATT0 | 0x400118B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX66_MS_ATT1 | 0x400118B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX66_MS_ATT2 | 0x400118B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX66_MS_ATT3 | 0x400118BC | FULL | Master attributes 3 |

21.84 PPU_FX 67

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX67_SL_ADDR | 0x400118C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX67_SL_SIZE | 0x400118C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX67_SL_ATT0 | 0x400118D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX67_SL_ATT1 | 0x400118D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX67_SL_ATT2 | 0x400118D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX67_SL_ATT3 | 0x400118DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX67_MS_ADDR | 0x400118E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX67_MS_SIZE | 0x400118E4 | FULL | Master region, size |
| PERI_MS_PPU_FX67_MS_ATT0 | 0x400118F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX67_MS_ATT1 | 0x400118F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX67_MS_ATT2 | 0x400118F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX67_MS_ATT3 | 0x400118FC | FULL | Master attributes 3 |

21.85 PPU_FX 68

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PERI_MS_PPU_FX68_SL_ADDR | 0x40011900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX68_SL_SIZE | 0x40011904 | FULL | Slave region, size |
| PERI_MS_PPU_FX68_SL_ATT0 | 0x40011910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX68_SL_ATT1 | 0x40011914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX68_SL_ATT2 | 0x40011918 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX68_SL_ATT3 | 0x4001191C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX68_MS_ADDR | 0x40011920 | FULL | Master region, base address |
| PERI_MS_PPU_FX68_MS_SIZE | 0x40011924 | FULL | Master region, size |
| PERI_MS_PPU_FX68_MS_ATT0 | 0x40011930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX68_MS_ATT1 | 0x40011934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX68_MS_ATT2 | 0x40011938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX68_MS_ATT3 | 0x4001193C | FULL | Master attributes 3 |

21.86 PPU_FX 69

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX69_SL_ADDR | 0x40011940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX69_SL_SIZE | 0x40011944 | FULL | Slave region, size |
| PERI_MS_PPU_FX69_SL_ATT0 | 0x40011950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX69_SL_ATT1 | 0x40011954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX69_SL_ATT2 | 0x40011958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX69_SL_ATT3 | 0x4001195C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX69_MS_ADDR | 0x40011960 | FULL | Master region, base address |
| PERI_MS_PPU_FX69_MS_SIZE | 0x40011964 | FULL | Master region, size |
| PERI_MS_PPU_FX69_MS_ATT0 | 0x40011970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX69_MS_ATT1 | 0x40011974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX69_MS_ATT2 | 0x40011978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX69_MS_ATT3 | 0x4001197C | FULL | Master attributes 3 |

21.87 PPU_FX 70

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX70_SL_ADDR | 0x40011980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX70_SL_SIZE | 0x40011984 | FULL | Slave region, size |
| PERI_MS_PPU_FX70_SL_ATT0 | 0x40011990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX70_SL_ATT1 | 0x40011994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX70_SL_ATT2 | 0x40011998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX70_SL_ATT3 | 0x4001199C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX70_MS_ADDR | 0x400119A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX70_MS_SIZE | 0x400119A4 | FULL | Master region, size |
| PERI_MS_PPU_FX70_MS_ATT0 | 0x400119B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX70_MS_ATT1 | 0x400119B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX70_MS_ATT2 | 0x400119B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX70_MS_ATT3 | 0x400119BC | FULL | Master attributes 3 |

21.88 PPU_FX 71

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX71_SL_ADDR | 0x400119C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX71_SL_SIZE | 0x400119C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX71_SL_ATT0 | 0x400119D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX71_SL_ATT1 | 0x400119D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX71_SL_ATT2 | 0x400119D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX71_SL_ATT3 | 0x400119DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX71_MS_ADDR | 0x400119E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX71_MS_SIZE | 0x400119E4 | FULL | Master region, size |
| PERI_MS_PPU_FX71_MS_ATT0 | 0x400119F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX71_MS_ATT1 | 0x400119F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX71_MS_ATT2 | 0x400119F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX71_MS_ATT3 | 0x400119FC | FULL | Master attributes 3 |

21.89 PPU_FX 72

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PERI_MS_PPU_FX72_SL_ADDR | 0x40011A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX72_SL_SIZE | 0x40011A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX72_SL_ATT0 | 0x40011A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX72_SL_ATT1 | 0x40011A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX72_SL_ATT2 | 0x40011A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX72_SL_ATT3 | 0x40011A1C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX72_MS_ADDR | 0x40011A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX72_MS_SIZE | 0x40011A24 | FULL | Master region, size |
| PERI_MS_PPU_FX72_MS_ATT0 | 0x40011A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX72_MS_ATT1 | 0x40011A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX72_MS_ATT2 | 0x40011A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX72_MS_ATT3 | 0x40011A3C | FULL | Master attributes 3 |

21.90 PPU_FX 73

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX73_SL_ADDR | 0x40011A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX73_SL_SIZE | 0x40011A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX73_SL_ATT0 | 0x40011A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX73_SL_ATT1 | 0x40011A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX73_SL_ATT2 | 0x40011A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX73_SL_ATT3 | 0x40011A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX73_MS_ADDR | 0x40011A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX73_MS_SIZE | 0x40011A64 | FULL | Master region, size |
| PERI_MS_PPU_FX73_MS_ATT0 | 0x40011A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX73_MS_ATT1 | 0x40011A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX73_MS_ATT2 | 0x40011A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX73_MS_ATT3 | 0x40011A7C | FULL | Master attributes 3 |

21.91 PPU_FX 74

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX74_SL_ADDR | 0x40011A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX74_SL_SIZE | 0x40011A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX74_SL_ATT0 | 0x40011A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX74_SL_ATT1 | 0x40011A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX74_SL_ATT2 | 0x40011A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX74_SL_ATT3 | 0x40011A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX74_MS_ADDR | 0x40011AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX74_MS_SIZE | 0x40011AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX74_MS_ATT0 | 0x40011AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX74_MS_ATT1 | 0x40011AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX74_MS_ATT2 | 0x40011AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX74_MS_ATT3 | 0x40011ABC | FULL | Master attributes 3 |

21.92 PPU_FX 75

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX75_SL_ADDR | 0x40011AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX75_SL_SIZE | 0x40011AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX75_SL_ATT0 | 0x40011AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX75_SL_ATT1 | 0x40011AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX75_SL_ATT2 | 0x40011AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX75_SL_ATT3 | 0x40011ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX75_MS_ADDR | 0x40011AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX75_MS_SIZE | 0x40011AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX75_MS_ATT0 | 0x40011AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX75_MS_ATT1 | 0x40011AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX75_MS_ATT2 | 0x40011AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX75_MS_ATT3 | 0x40011AFC | FULL | Master attributes 3 |

21.93 PPU_FX 76

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX76_SL_ADDR | 0x40011B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX76_SL_SIZE | 0x40011B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX76_SL_ATT0 | 0x40011B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX76_SL_ATT1 | 0x40011B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX76_SL_ATT2 | 0x40011B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX76_SL_ATT3 | 0x40011B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX76_MS_ADDR | 0x40011B20 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX76_MS_SIZE | 0x40011B24 | FULL | Master region, size |
| PERI_MS_PPU_FX76_MS_ATT0 | 0x40011B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX76_MS_ATT1 | 0x40011B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX76_MS_ATT2 | 0x40011B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX76_MS_ATT3 | 0x40011B3C | FULL | Master attributes 3 |

21.94 PPU_FX 77

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX77_SL_ADDR | 0x40011B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX77_SL_SIZE | 0x40011B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX77_SL_ATT0 | 0x40011B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX77_SL_ATT1 | 0x40011B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX77_SL_ATT2 | 0x40011B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX77_SL_ATT3 | 0x40011B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX77_MS_ADDR | 0x40011B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX77_MS_SIZE | 0x40011B64 | FULL | Master region, size |
| PERI_MS_PPU_FX77_MS_ATT0 | 0x40011B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX77_MS_ATT1 | 0x40011B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX77_MS_ATT2 | 0x40011B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX77_MS_ATT3 | 0x40011B7C | FULL | Master attributes 3 |

21.95 PPU_FX 78

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX78_SL_ADDR | 0x40011B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX78_SL_SIZE | 0x40011B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX78_SL_ATT0 | 0x40011B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX78_SL_ATT1 | 0x40011B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX78_SL_ATT2 | 0x40011B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX78_SL_ATT3 | 0x40011B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX78_MS_ADDR | 0x40011BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX78_MS_SIZE | 0x40011BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX78_MS_ATT0 | 0x40011BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX78_MS_ATT1 | 0x40011BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX78_MS_ATT2 | 0x40011BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX78_MS_ATT3 | 0x40011BBC | FULL | Master attributes 3 |

21.96 PPU_FX 79

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX79_SL_ADDR | 0x40011BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX79_SL_SIZE | 0x40011BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX79_SL_ATT0 | 0x40011BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX79_SL_ATT1 | 0x40011BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX79_SL_ATT2 | 0x40011BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX79_SL_ATT3 | 0x40011BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX79_MS_ADDR | 0x40011BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX79_MS_SIZE | 0x40011BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX79_MS_ATT0 | 0x40011BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX79_MS_ATT1 | 0x40011BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX79_MS_ATT2 | 0x40011BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX79_MS_ATT3 | 0x40011BFC | FULL | Master attributes 3 |

21.97 PPU_FX 80

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX80_SL_ADDR | 0x40011C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX80_SL_SIZE | 0x40011C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX80_SL_ATT0 | 0x40011C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX80_SL_ATT1 | 0x40011C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX80_SL_ATT2 | 0x40011C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX80_SL_ATT3 | 0x40011C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX80_MS_ADDR | 0x40011C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX80_MS_SIZE | 0x40011C24 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX80_MS_ATT0 | 0x40011C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX80_MS_ATT1 | 0x40011C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX80_MS_ATT2 | 0x40011C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX80_MS_ATT3 | 0x40011C3C | FULL | Master attributes 3 |

21.98 PPU_FX 81

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX81_SL_ADDR | 0x40011C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX81_SL_SIZE | 0x40011C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX81_SL_ATT0 | 0x40011C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX81_SL_ATT1 | 0x40011C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX81_SL_ATT2 | 0x40011C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX81_SL_ATT3 | 0x40011C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX81_MS_ADDR | 0x40011C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX81_MS_SIZE | 0x40011C64 | FULL | Master region, size |
| PERI_MS_PPU_FX81_MS_ATT0 | 0x40011C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX81_MS_ATT1 | 0x40011C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX81_MS_ATT2 | 0x40011C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX81_MS_ATT3 | 0x40011C7C | FULL | Master attributes 3 |

21.99 PPU_FX 82

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX82_SL_ADDR | 0x40011C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX82_SL_SIZE | 0x40011C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX82_SL_ATT0 | 0x40011C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX82_SL_ATT1 | 0x40011C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX82_SL_ATT2 | 0x40011C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX82_SL_ATT3 | 0x40011C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX82_MS_ADDR | 0x40011CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX82_MS_SIZE | 0x40011CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX82_MS_ATT0 | 0x40011CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX82_MS_ATT1 | 0x40011CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX82_MS_ATT2 | 0x40011CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX82_MS_ATT3 | 0x40011CBC | FULL | Master attributes 3 |

21.100 PPU_FX 83

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX83_SL_ADDR | 0x40011CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX83_SL_SIZE | 0x40011CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX83_SL_ATT0 | 0x40011CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX83_SL_ATT1 | 0x40011CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX83_SL_ATT2 | 0x40011CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX83_SL_ATT3 | 0x40011CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX83_MS_ADDR | 0x40011CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX83_MS_SIZE | 0x40011CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX83_MS_ATT0 | 0x40011CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX83_MS_ATT1 | 0x40011CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX83_MS_ATT2 | 0x40011CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX83_MS_ATT3 | 0x40011CFC | FULL | Master attributes 3 |

21.101 PPU_FX 84

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX84_SL_ADDR | 0x40011D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX84_SL_SIZE | 0x40011D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX84_SL_ATT0 | 0x40011D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX84_SL_ATT1 | 0x40011D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX84_SL_ATT2 | 0x40011D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX84_SL_ATT3 | 0x40011D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX84_MS_ADDR | 0x40011D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX84_MS_SIZE | 0x40011D24 | FULL | Master region, size |
| PERI_MS_PPU_FX84_MS_ATT0 | 0x40011D30 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|--|------------|------------|---------------------|
| PERI_MS_PPU_FX84_MS_ATT1 | 0x40011D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX84_MS_ATT2 | 0x40011D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX84_MS_ATT3 | 0x40011D3C | FULL | Master attributes 3 |

21.102 PPU_FX 85

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX85_SL_ADDR | 0x40011D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX85_SL_SIZE | 0x40011D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX85_SL_ATT0 | 0x40011D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX85_SL_ATT1 | 0x40011D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX85_SL_ATT2 | 0x40011D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX85_SL_ATT3 | 0x40011D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX85_MS_ADDR | 0x40011D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX85_MS_SIZE | 0x40011D64 | FULL | Master region, size |
| PERI_MS_PPU_FX85_MS_ATT0 | 0x40011D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX85_MS_ATT1 | 0x40011D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX85_MS_ATT2 | 0x40011D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX85_MS_ATT3 | 0x40011D7C | FULL | Master attributes 3 |

21.103 PPU_FX 86

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX86_SL_ADDR | 0x40011D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX86_SL_SIZE | 0x40011D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX86_SL_ATT0 | 0x40011D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX86_SL_ATT1 | 0x40011D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX86_SL_ATT2 | 0x40011D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX86_SL_ATT3 | 0x40011D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX86_MS_ADDR | 0x40011DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX86_MS_SIZE | 0x40011DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX86_MS_ATT0 | 0x40011DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX86_MS_ATT1 | 0x40011DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX86_MS_ATT2 | 0x40011DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX86_MS_ATT3 | 0x40011DBC | FULL | Master attributes 3 |

21.104 PPU_FX 87

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX87_SL_ADDR | 0x40011DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX87_SL_SIZE | 0x40011DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX87_SL_ATT0 | 0x40011DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX87_SL_ATT1 | 0x40011DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX87_SL_ATT2 | 0x40011DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX87_SL_ATT3 | 0x40011DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX87_MS_ADDR | 0x40011DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX87_MS_SIZE | 0x40011DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX87_MS_ATT0 | 0x40011DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX87_MS_ATT1 | 0x40011DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX87_MS_ATT2 | 0x40011DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX87_MS_ATT3 | 0x40011DFC | FULL | Master attributes 3 |

21.105 PPU_FX 88

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX88_SL_ADDR | 0x40011E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX88_SL_SIZE | 0x40011E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX88_SL_ATT0 | 0x40011E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX88_SL_ATT1 | 0x40011E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX88_SL_ATT2 | 0x40011E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX88_SL_ATT3 | 0x40011E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX88_MS_ADDR | 0x40011E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX88_MS_SIZE | 0x40011E24 | FULL | Master region, size |
| PERI_MS_PPU_FX88_MS_ATT0 | 0x40011E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX88_MS_ATT1 | 0x40011E34 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|--|------------|------------|---------------------|
| PERI_MS_PPU_FX88_MS_ATT2 | 0x40011E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX88_MS_ATT3 | 0x40011E3C | FULL | Master attributes 3 |

21.106 PPU_FX 89

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX89_SL_ADDR | 0x40011E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX89_SL_SIZE | 0x40011E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX89_SL_ATT0 | 0x40011E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX89_SL_ATT1 | 0x40011E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX89_SL_ATT2 | 0x40011E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX89_SL_ATT3 | 0x40011E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX89_MS_ADDR | 0x40011E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX89_MS_SIZE | 0x40011E64 | FULL | Master region, size |
| PERI_MS_PPU_FX89_MS_ATT0 | 0x40011E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX89_MS_ATT1 | 0x40011E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX89_MS_ATT2 | 0x40011E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX89_MS_ATT3 | 0x40011E7C | FULL | Master attributes 3 |

21.107 PPU_FX 90

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX90_SL_ADDR | 0x40011E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX90_SL_SIZE | 0x40011E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX90_SL_ATT0 | 0x40011E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX90_SL_ATT1 | 0x40011E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX90_SL_ATT2 | 0x40011E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX90_SL_ATT3 | 0x40011E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX90_MS_ADDR | 0x40011EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX90_MS_SIZE | 0x40011EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX90_MS_ATT0 | 0x40011EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX90_MS_ATT1 | 0x40011EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX90_MS_ATT2 | 0x40011EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX90_MS_ATT3 | 0x40011EBC | FULL | Master attributes 3 |

21.108 PPU_FX 91

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX91_SL_ADDR | 0x40011EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX91_SL_SIZE | 0x40011EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX91_SL_ATT0 | 0x40011ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX91_SL_ATT1 | 0x40011ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX91_SL_ATT2 | 0x40011ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX91_SL_ATT3 | 0x40011EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX91_MS_ADDR | 0x40011EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX91_MS_SIZE | 0x40011EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX91_MS_ATT0 | 0x40011EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX91_MS_ATT1 | 0x40011EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX91_MS_ATT2 | 0x40011EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX91_MS_ATT3 | 0x40011EFC | FULL | Master attributes 3 |

21.109 PPU_FX 92

| Register Name | Address | Permission | Description |
|--|------------|------------|-----------------------------|
| PERI_MS_PPU_FX92_SL_ADDR | 0x40011F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX92_SL_SIZE | 0x40011F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX92_SL_ATT0 | 0x40011F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX92_SL_ATT1 | 0x40011F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX92_SL_ATT2 | 0x40011F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX92_SL_ATT3 | 0x40011F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX92_MS_ADDR | 0x40011F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX92_MS_SIZE | 0x40011F24 | FULL | Master region, size |
| PERI_MS_PPU_FX92_MS_ATT0 | 0x40011F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX92_MS_ATT1 | 0x40011F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX92_MS_ATT2 | 0x40011F38 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX92_MS_ATT3 | 0x40011F3C | FULL | Master attributes 3 |

21.110 PPU_FX 93

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX93_SL_ADDR | 0x40011F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX93_SL_SIZE | 0x40011F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX93_SL_ATT0 | 0x40011F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX93_SL_ATT1 | 0x40011F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX93_SL_ATT2 | 0x40011F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX93_SL_ATT3 | 0x40011F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX93_MS_ADDR | 0x40011F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX93_MS_SIZE | 0x40011F64 | FULL | Master region, size |
| PERI_MS_PPU_FX93_MS_ATT0 | 0x40011F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX93_MS_ATT1 | 0x40011F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX93_MS_ATT2 | 0x40011F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX93_MS_ATT3 | 0x40011F7C | FULL | Master attributes 3 |

21.111 PPU_FX 94

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX94_SL_ADDR | 0x40011F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX94_SL_SIZE | 0x40011F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX94_SL_ATT0 | 0x40011F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX94_SL_ATT1 | 0x40011F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX94_SL_ATT2 | 0x40011F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX94_SL_ATT3 | 0x40011F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX94_MS_ADDR | 0x40011FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX94_MS_SIZE | 0x40011FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX94_MS_ATT0 | 0x40011FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX94_MS_ATT1 | 0x40011FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX94_MS_ATT2 | 0x40011FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX94_MS_ATT3 | 0x40011FBC | FULL | Master attributes 3 |

21.112 PPU_FX 95

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX95_SL_ADDR | 0x40011FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX95_SL_SIZE | 0x40011FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX95_SL_ATT0 | 0x40011FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX95_SL_ATT1 | 0x40011FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX95_SL_ATT2 | 0x40011FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX95_SL_ATT3 | 0x40011FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX95_MS_ADDR | 0x40011FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX95_MS_SIZE | 0x40011FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX95_MS_ATT0 | 0x40011FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX95_MS_ATT1 | 0x40011FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX95_MS_ATT2 | 0x40011FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX95_MS_ATT3 | 0x40011FFC | FULL | Master attributes 3 |

21.113 PPU_FX 96

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX96_SL_ADDR | 0x40012000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX96_SL_SIZE | 0x40012004 | FULL | Slave region, size |
| PERI_MS_PPU_FX96_SL_ATT0 | 0x40012010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX96_SL_ATT1 | 0x40012014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX96_SL_ATT2 | 0x40012018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX96_SL_ATT3 | 0x4001201C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX96_MS_ADDR | 0x40012020 | FULL | Master region, base address |
| PERI_MS_PPU_FX96_MS_SIZE | 0x40012024 | FULL | Master region, size |
| PERI_MS_PPU_FX96_MS_ATT0 | 0x40012030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX96_MS_ATT1 | 0x40012034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX96_MS_ATT2 | 0x40012038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX96_MS_ATT3 | 0x4001203C | FULL | Master attributes 3 |

21.114 PPU_FX 97

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX97_SL_ADDR | 0x40012040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX97_SL_SIZE | 0x40012044 | FULL | Slave region, size |
| PERI_MS_PPU_FX97_SL_ATT0 | 0x40012050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX97_SL_ATT1 | 0x40012054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX97_SL_ATT2 | 0x40012058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX97_SL_ATT3 | 0x4001205C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX97_MS_ADDR | 0x40012060 | FULL | Master region, base address |
| PERI_MS_PPU_FX97_MS_SIZE | 0x40012064 | FULL | Master region, size |
| PERI_MS_PPU_FX97_MS_ATT0 | 0x40012070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX97_MS_ATT1 | 0x40012074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX97_MS_ATT2 | 0x40012078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX97_MS_ATT3 | 0x4001207C | FULL | Master attributes 3 |

21.115 PPU_FX 98

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX98_SL_ADDR | 0x40012080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX98_SL_SIZE | 0x40012084 | FULL | Slave region, size |
| PERI_MS_PPU_FX98_SL_ATT0 | 0x40012090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX98_SL_ATT1 | 0x40012094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX98_SL_ATT2 | 0x40012098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX98_SL_ATT3 | 0x4001209C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX98_MS_ADDR | 0x400120A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX98_MS_SIZE | 0x400120A4 | FULL | Master region, size |
| PERI_MS_PPU_FX98_MS_ATT0 | 0x400120B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX98_MS_ATT1 | 0x400120B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX98_MS_ATT2 | 0x400120B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX98_MS_ATT3 | 0x400120BC | FULL | Master attributes 3 |

21.116 PPU_FX 99

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX99_SL_ADDR | 0x400120C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX99_SL_SIZE | 0x400120C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX99_SL_ATT0 | 0x400120D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX99_SL_ATT1 | 0x400120D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX99_SL_ATT2 | 0x400120D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX99_SL_ATT3 | 0x400120DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX99_MS_ADDR | 0x400120E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX99_MS_SIZE | 0x400120E4 | FULL | Master region, size |
| PERI_MS_PPU_FX99_MS_ATT0 | 0x400120F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX99_MS_ATT1 | 0x400120F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX99_MS_ATT2 | 0x400120F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX99_MS_ATT3 | 0x400120FC | FULL | Master attributes 3 |

21.117 PPU_FX 100

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX100_SL_ADDR | 0x40012100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX100_SL_SIZE | 0x40012104 | FULL | Slave region, size |
| PERI_MS_PPU_FX100_SL_ATT0 | 0x40012110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX100_SL_ATT1 | 0x40012114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX100_SL_ATT2 | 0x40012118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX100_SL_ATT3 | 0x4001211C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX100_MS_ADDR | 0x40012120 | FULL | Master region, base address |
| PERI_MS_PPU_FX100_MS_SIZE | 0x40012124 | FULL | Master region, size |
| PERI_MS_PPU_FX100_MS_ATT0 | 0x40012130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX100_MS_ATT1 | 0x40012134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX100_MS_ATT2 | 0x40012138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX100_MS_ATT3 | 0x4001213C | FULL | Master attributes 3 |

21.118 PPU_FX 101

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX101_SL_ADDR | 0x40012140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX101_SL_SIZE | 0x40012144 | FULL | Slave region, size |
| PERI_MS_PPU_FX101_SL_ATT0 | 0x40012150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX101_SL_ATT1 | 0x40012154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX101_SL_ATT2 | 0x40012158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX101_SL_ATT3 | 0x4001215C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX101_MS_ADDR | 0x40012160 | FULL | Master region, base address |
| PERI_MS_PPU_FX101_MS_SIZE | 0x40012164 | FULL | Master region, size |
| PERI_MS_PPU_FX101_MS_ATT0 | 0x40012170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX101_MS_ATT1 | 0x40012174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX101_MS_ATT2 | 0x40012178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX101_MS_ATT3 | 0x4001217C | FULL | Master attributes 3 |

21.119 PPU_FX 102

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX102_SL_ADDR | 0x40012180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX102_SL_SIZE | 0x40012184 | FULL | Slave region, size |
| PERI_MS_PPU_FX102_SL_ATT0 | 0x40012190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX102_SL_ATT1 | 0x40012194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX102_SL_ATT2 | 0x40012198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX102_SL_ATT3 | 0x4001219C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX102_MS_ADDR | 0x400121A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX102_MS_SIZE | 0x400121A4 | FULL | Master region, size |
| PERI_MS_PPU_FX102_MS_ATT0 | 0x400121B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX102_MS_ATT1 | 0x400121B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX102_MS_ATT2 | 0x400121B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX102_MS_ATT3 | 0x400121BC | FULL | Master attributes 3 |

21.120 PPU_FX 103

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX103_SL_ADDR | 0x400121C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX103_SL_SIZE | 0x400121C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX103_SL_ATT0 | 0x400121D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX103_SL_ATT1 | 0x400121D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX103_SL_ATT2 | 0x400121D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX103_SL_ATT3 | 0x400121DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX103_MS_ADDR | 0x400121E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX103_MS_SIZE | 0x400121E4 | FULL | Master region, size |
| PERI_MS_PPU_FX103_MS_ATT0 | 0x400121F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX103_MS_ATT1 | 0x400121F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX103_MS_ATT2 | 0x400121F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX103_MS_ATT3 | 0x400121FC | FULL | Master attributes 3 |

21.121 PPU_FX 104

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX104_SL_ADDR | 0x40012200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX104_SL_SIZE | 0x40012204 | FULL | Slave region, size |
| PERI_MS_PPU_FX104_SL_ATT0 | 0x40012210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX104_SL_ATT1 | 0x40012214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX104_SL_ATT2 | 0x40012218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX104_SL_ATT3 | 0x4001221C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX104_MS_ADDR | 0x40012220 | FULL | Master region, base address |
| PERI_MS_PPU_FX104_MS_SIZE | 0x40012224 | FULL | Master region, size |
| PERI_MS_PPU_FX104_MS_ATT0 | 0x40012230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX104_MS_ATT1 | 0x40012234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX104_MS_ATT2 | 0x40012238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX104_MS_ATT3 | 0x4001223C | FULL | Master attributes 3 |

21.122 PPU_FX 105

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX105_SL_ADDR | 0x40012240 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX105_SL_SIZE | 0x40012244 | FULL | Slave region, size |
| PERI_MS_PPU_FX105_SL_ATT0 | 0x40012250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX105_SL_ATT1 | 0x40012254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX105_SL_ATT2 | 0x40012258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX105_SL_ATT3 | 0x4001225C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX105_MS_ADDR | 0x40012260 | FULL | Master region, base address |
| PERI_MS_PPU_FX105_MS_SIZE | 0x40012264 | FULL | Master region, size |
| PERI_MS_PPU_FX105_MS_ATT0 | 0x40012270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX105_MS_ATT1 | 0x40012274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX105_MS_ATT2 | 0x40012278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX105_MS_ATT3 | 0x4001227C | FULL | Master attributes 3 |

21.123 PPU_FX 106

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX106_SL_ADDR | 0x40012280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX106_SL_SIZE | 0x40012284 | FULL | Slave region, size |
| PERI_MS_PPU_FX106_SL_ATT0 | 0x40012290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX106_SL_ATT1 | 0x40012294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX106_SL_ATT2 | 0x40012298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX106_SL_ATT3 | 0x4001229C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX106_MS_ADDR | 0x400122A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX106_MS_SIZE | 0x400122A4 | FULL | Master region, size |
| PERI_MS_PPU_FX106_MS_ATT0 | 0x400122B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX106_MS_ATT1 | 0x400122B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX106_MS_ATT2 | 0x400122B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX106_MS_ATT3 | 0x400122BC | FULL | Master attributes 3 |

21.124 PPU_FX 107

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX107_SL_ADDR | 0x400122C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX107_SL_SIZE | 0x400122C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX107_SL_ATT0 | 0x400122D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX107_SL_ATT1 | 0x400122D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX107_SL_ATT2 | 0x400122D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX107_SL_ATT3 | 0x400122DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX107_MS_ADDR | 0x400122E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX107_MS_SIZE | 0x400122E4 | FULL | Master region, size |
| PERI_MS_PPU_FX107_MS_ATT0 | 0x400122F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX107_MS_ATT1 | 0x400122F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX107_MS_ATT2 | 0x400122F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX107_MS_ATT3 | 0x400122FC | FULL | Master attributes 3 |

21.125 PPU_FX 108

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX108_SL_ADDR | 0x40012300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX108_SL_SIZE | 0x40012304 | FULL | Slave region, size |
| PERI_MS_PPU_FX108_SL_ATT0 | 0x40012310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX108_SL_ATT1 | 0x40012314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX108_SL_ATT2 | 0x40012318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX108_SL_ATT3 | 0x4001231C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX108_MS_ADDR | 0x40012320 | FULL | Master region, base address |
| PERI_MS_PPU_FX108_MS_SIZE | 0x40012324 | FULL | Master region, size |
| PERI_MS_PPU_FX108_MS_ATT0 | 0x40012330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX108_MS_ATT1 | 0x40012334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX108_MS_ATT2 | 0x40012338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX108_MS_ATT3 | 0x4001233C | FULL | Master attributes 3 |

21.126 PPU_FX 109

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX109_SL_ADDR | 0x40012340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX109_SL_SIZE | 0x40012344 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX109_SL_ATT0 | 0x40012350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX109_SL_ATT1 | 0x40012354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX109_SL_ATT2 | 0x40012358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX109_SL_ATT3 | 0x4001235C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX109_MS_ADDR | 0x40012360 | FULL | Master region, base address |
| PERI_MS_PPU_FX109_MS_SIZE | 0x40012364 | FULL | Master region, size |
| PERI_MS_PPU_FX109_MS_ATT0 | 0x40012370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX109_MS_ATT1 | 0x40012374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX109_MS_ATT2 | 0x40012378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX109_MS_ATT3 | 0x4001237C | FULL | Master attributes 3 |

21.127 PPU_FX 110

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX110_SL_ADDR | 0x40012380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX110_SL_SIZE | 0x40012384 | FULL | Slave region, size |
| PERI_MS_PPU_FX110_SL_ATT0 | 0x40012390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX110_SL_ATT1 | 0x40012394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX110_SL_ATT2 | 0x40012398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX110_SL_ATT3 | 0x4001239C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX110_MS_ADDR | 0x400123A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX110_MS_SIZE | 0x400123A4 | FULL | Master region, size |
| PERI_MS_PPU_FX110_MS_ATT0 | 0x400123B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX110_MS_ATT1 | 0x400123B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX110_MS_ATT2 | 0x400123B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX110_MS_ATT3 | 0x400123BC | FULL | Master attributes 3 |

21.128 PPU_FX 111

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX111_SL_ADDR | 0x400123C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX111_SL_SIZE | 0x400123C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX111_SL_ATT0 | 0x400123D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX111_SL_ATT1 | 0x400123D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX111_SL_ATT2 | 0x400123D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX111_SL_ATT3 | 0x400123DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX111_MS_ADDR | 0x400123E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX111_MS_SIZE | 0x400123E4 | FULL | Master region, size |
| PERI_MS_PPU_FX111_MS_ATT0 | 0x400123F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX111_MS_ATT1 | 0x400123F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX111_MS_ATT2 | 0x400123F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX111_MS_ATT3 | 0x400123FC | FULL | Master attributes 3 |

21.129 PPU_FX 112

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX112_SL_ADDR | 0x40012400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX112_SL_SIZE | 0x40012404 | FULL | Slave region, size |
| PERI_MS_PPU_FX112_SL_ATT0 | 0x40012410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX112_SL_ATT1 | 0x40012414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX112_SL_ATT2 | 0x40012418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX112_SL_ATT3 | 0x4001241C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX112_MS_ADDR | 0x40012420 | FULL | Master region, base address |
| PERI_MS_PPU_FX112_MS_SIZE | 0x40012424 | FULL | Master region, size |
| PERI_MS_PPU_FX112_MS_ATT0 | 0x40012430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX112_MS_ATT1 | 0x40012434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX112_MS_ATT2 | 0x40012438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX112_MS_ATT3 | 0x4001243C | FULL | Master attributes 3 |

21.130 PPU_FX 113

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX113_SL_ADDR | 0x40012440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX113_SL_SIZE | 0x40012444 | FULL | Slave region, size |
| PERI_MS_PPU_FX113_SL_ATT0 | 0x40012450 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX113_SL_ATT1 | 0x40012454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX113_SL_ATT2 | 0x40012458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX113_SL_ATT3 | 0x4001245C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX113_MS_ADDR | 0x40012460 | FULL | Master region, base address |
| PERI_MS_PPU_FX113_MS_SIZE | 0x40012464 | FULL | Master region, size |
| PERI_MS_PPU_FX113_MS_ATT0 | 0x40012470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX113_MS_ATT1 | 0x40012474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX113_MS_ATT2 | 0x40012478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX113_MS_ATT3 | 0x4001247C | FULL | Master attributes 3 |

21.131 PPU_FX 114

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX114_SL_ADDR | 0x40012480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX114_SL_SIZE | 0x40012484 | FULL | Slave region, size |
| PERI_MS_PPU_FX114_SL_ATT0 | 0x40012490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX114_SL_ATT1 | 0x40012494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX114_SL_ATT2 | 0x40012498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX114_SL_ATT3 | 0x4001249C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX114_MS_ADDR | 0x400124A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX114_MS_SIZE | 0x400124A4 | FULL | Master region, size |
| PERI_MS_PPU_FX114_MS_ATT0 | 0x400124B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX114_MS_ATT1 | 0x400124B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX114_MS_ATT2 | 0x400124B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX114_MS_ATT3 | 0x400124BC | FULL | Master attributes 3 |

21.132 PPU_FX 115

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX115_SL_ADDR | 0x400124C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX115_SL_SIZE | 0x400124C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX115_SL_ATT0 | 0x400124D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX115_SL_ATT1 | 0x400124D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX115_SL_ATT2 | 0x400124D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX115_SL_ATT3 | 0x400124DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX115_MS_ADDR | 0x400124E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX115_MS_SIZE | 0x400124E4 | FULL | Master region, size |
| PERI_MS_PPU_FX115_MS_ATT0 | 0x400124F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX115_MS_ATT1 | 0x400124F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX115_MS_ATT2 | 0x400124F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX115_MS_ATT3 | 0x400124FC | FULL | Master attributes 3 |

21.133 PPU_FX 116

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX116_SL_ADDR | 0x40012500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX116_SL_SIZE | 0x40012504 | FULL | Slave region, size |
| PERI_MS_PPU_FX116_SL_ATT0 | 0x40012510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX116_SL_ATT1 | 0x40012514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX116_SL_ATT2 | 0x40012518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX116_SL_ATT3 | 0x4001251C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX116_MS_ADDR | 0x40012520 | FULL | Master region, base address |
| PERI_MS_PPU_FX116_MS_SIZE | 0x40012524 | FULL | Master region, size |
| PERI_MS_PPU_FX116_MS_ATT0 | 0x40012530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX116_MS_ATT1 | 0x40012534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX116_MS_ATT2 | 0x40012538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX116_MS_ATT3 | 0x4001253C | FULL | Master attributes 3 |

21.134 PPU_FX 117

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX117_SL_ADDR | 0x40012540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX117_SL_SIZE | 0x40012544 | FULL | Slave region, size |
| PERI_MS_PPU_FX117_SL_ATT0 | 0x40012550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX117_SL_ATT1 | 0x40012554 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX117_SL_ATT2 | 0x40012558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX117_SL_ATT3 | 0x4001255C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX117_MS_ADDR | 0x40012560 | FULL | Master region, base address |
| PERI_MS_PPU_FX117_MS_SIZE | 0x40012564 | FULL | Master region, size |
| PERI_MS_PPU_FX117_MS_ATT0 | 0x40012570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX117_MS_ATT1 | 0x40012574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX117_MS_ATT2 | 0x40012578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX117_MS_ATT3 | 0x4001257C | FULL | Master attributes 3 |

21.135 PPU_FX 118

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX118_SL_ADDR | 0x40012580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX118_SL_SIZE | 0x40012584 | FULL | Slave region, size |
| PERI_MS_PPU_FX118_SL_ATT0 | 0x40012590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX118_SL_ATT1 | 0x40012594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX118_SL_ATT2 | 0x40012598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX118_SL_ATT3 | 0x4001259C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX118_MS_ADDR | 0x400125A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX118_MS_SIZE | 0x400125A4 | FULL | Master region, size |
| PERI_MS_PPU_FX118_MS_ATT0 | 0x400125B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX118_MS_ATT1 | 0x400125B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX118_MS_ATT2 | 0x400125B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX118_MS_ATT3 | 0x400125BC | FULL | Master attributes 3 |

21.136 PPU_FX 119

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX119_SL_ADDR | 0x400125C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX119_SL_SIZE | 0x400125C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX119_SL_ATT0 | 0x400125D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX119_SL_ATT1 | 0x400125D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX119_SL_ATT2 | 0x400125D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX119_SL_ATT3 | 0x400125DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX119_MS_ADDR | 0x400125E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX119_MS_SIZE | 0x400125E4 | FULL | Master region, size |
| PERI_MS_PPU_FX119_MS_ATT0 | 0x400125F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX119_MS_ATT1 | 0x400125F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX119_MS_ATT2 | 0x400125F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX119_MS_ATT3 | 0x400125FC | FULL | Master attributes 3 |

21.137 PPU_FX 120

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX120_SL_ADDR | 0x40012600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX120_SL_SIZE | 0x40012604 | FULL | Slave region, size |
| PERI_MS_PPU_FX120_SL_ATT0 | 0x40012610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX120_SL_ATT1 | 0x40012614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX120_SL_ATT2 | 0x40012618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX120_SL_ATT3 | 0x4001261C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX120_MS_ADDR | 0x40012620 | FULL | Master region, base address |
| PERI_MS_PPU_FX120_MS_SIZE | 0x40012624 | FULL | Master region, size |
| PERI_MS_PPU_FX120_MS_ATT0 | 0x40012630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX120_MS_ATT1 | 0x40012634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX120_MS_ATT2 | 0x40012638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX120_MS_ATT3 | 0x4001263C | FULL | Master attributes 3 |

21.138 PPU_FX 121

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX121_SL_ADDR | 0x40012640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX121_SL_SIZE | 0x40012644 | FULL | Slave region, size |
| PERI_MS_PPU_FX121_SL_ATT0 | 0x40012650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX121_SL_ATT1 | 0x40012654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX121_SL_ATT2 | 0x40012658 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX121_SL_ATT3 | 0x4001265C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX121_MS_ADDR | 0x40012660 | FULL | Master region, base address |
| PERI_MS_PPU_FX121_MS_SIZE | 0x40012664 | FULL | Master region, size |
| PERI_MS_PPU_FX121_MS_ATT0 | 0x40012670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX121_MS_ATT1 | 0x40012674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX121_MS_ATT2 | 0x40012678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX121_MS_ATT3 | 0x4001267C | FULL | Master attributes 3 |

21.139 PPU_FX 122

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX122_SL_ADDR | 0x40012680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX122_SL_SIZE | 0x40012684 | FULL | Slave region, size |
| PERI_MS_PPU_FX122_SL_ATT0 | 0x40012690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX122_SL_ATT1 | 0x40012694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX122_SL_ATT2 | 0x40012698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX122_SL_ATT3 | 0x4001269C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX122_MS_ADDR | 0x400126A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX122_MS_SIZE | 0x400126A4 | FULL | Master region, size |
| PERI_MS_PPU_FX122_MS_ATT0 | 0x400126B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX122_MS_ATT1 | 0x400126B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX122_MS_ATT2 | 0x400126B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX122_MS_ATT3 | 0x400126BC | FULL | Master attributes 3 |

21.140 PPU_FX 123

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX123_SL_ADDR | 0x400126C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX123_SL_SIZE | 0x400126C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX123_SL_ATT0 | 0x400126D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX123_SL_ATT1 | 0x400126D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX123_SL_ATT2 | 0x400126D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX123_SL_ATT3 | 0x400126DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX123_MS_ADDR | 0x400126E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX123_MS_SIZE | 0x400126E4 | FULL | Master region, size |
| PERI_MS_PPU_FX123_MS_ATT0 | 0x400126F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX123_MS_ATT1 | 0x400126F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX123_MS_ATT2 | 0x400126F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX123_MS_ATT3 | 0x400126FC | FULL | Master attributes 3 |

21.141 PPU_FX 124

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX124_SL_ADDR | 0x40012700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX124_SL_SIZE | 0x40012704 | FULL | Slave region, size |
| PERI_MS_PPU_FX124_SL_ATT0 | 0x40012710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX124_SL_ATT1 | 0x40012714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX124_SL_ATT2 | 0x40012718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX124_SL_ATT3 | 0x4001271C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX124_MS_ADDR | 0x40012720 | FULL | Master region, base address |
| PERI_MS_PPU_FX124_MS_SIZE | 0x40012724 | FULL | Master region, size |
| PERI_MS_PPU_FX124_MS_ATT0 | 0x40012730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX124_MS_ATT1 | 0x40012734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX124_MS_ATT2 | 0x40012738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX124_MS_ATT3 | 0x4001273C | FULL | Master attributes 3 |

21.142 PPU_FX 125

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX125_SL_ADDR | 0x40012740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX125_SL_SIZE | 0x40012744 | FULL | Slave region, size |
| PERI_MS_PPU_FX125_SL_ATT0 | 0x40012750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX125_SL_ATT1 | 0x40012754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX125_SL_ATT2 | 0x40012758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX125_SL_ATT3 | 0x4001275C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX125_MS_ADDR | 0x40012760 | FULL | Master region, base address |
| PERI_MS_PPU_FX125_MS_SIZE | 0x40012764 | FULL | Master region, size |
| PERI_MS_PPU_FX125_MS_ATT0 | 0x40012770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX125_MS_ATT1 | 0x40012774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX125_MS_ATT2 | 0x40012778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX125_MS_ATT3 | 0x4001277C | FULL | Master attributes 3 |

21.143 PPU_FX 126

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX126_SL_ADDR | 0x40012780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX126_SL_SIZE | 0x40012784 | FULL | Slave region, size |
| PERI_MS_PPU_FX126_SL_ATT0 | 0x40012790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX126_SL_ATT1 | 0x40012794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX126_SL_ATT2 | 0x40012798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX126_SL_ATT3 | 0x4001279C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX126_MS_ADDR | 0x400127A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX126_MS_SIZE | 0x400127A4 | FULL | Master region, size |
| PERI_MS_PPU_FX126_MS_ATT0 | 0x400127B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX126_MS_ATT1 | 0x400127B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX126_MS_ATT2 | 0x400127B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX126_MS_ATT3 | 0x400127BC | FULL | Master attributes 3 |

21.144 PPU_FX 127

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX127_SL_ADDR | 0x400127C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX127_SL_SIZE | 0x400127C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX127_SL_ATT0 | 0x400127D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX127_SL_ATT1 | 0x400127D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX127_SL_ATT2 | 0x400127D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX127_SL_ATT3 | 0x400127DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX127_MS_ADDR | 0x400127E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX127_MS_SIZE | 0x400127E4 | FULL | Master region, size |
| PERI_MS_PPU_FX127_MS_ATT0 | 0x400127F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX127_MS_ATT1 | 0x400127F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX127_MS_ATT2 | 0x400127F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX127_MS_ATT3 | 0x400127FC | FULL | Master attributes 3 |

21.145 PPU_FX 128

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX128_SL_ADDR | 0x40012800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX128_SL_SIZE | 0x40012804 | FULL | Slave region, size |
| PERI_MS_PPU_FX128_SL_ATT0 | 0x40012810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX128_SL_ATT1 | 0x40012814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX128_SL_ATT2 | 0x40012818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX128_SL_ATT3 | 0x4001281C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX128_MS_ADDR | 0x40012820 | FULL | Master region, base address |
| PERI_MS_PPU_FX128_MS_SIZE | 0x40012824 | FULL | Master region, size |
| PERI_MS_PPU_FX128_MS_ATT0 | 0x40012830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX128_MS_ATT1 | 0x40012834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX128_MS_ATT2 | 0x40012838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX128_MS_ATT3 | 0x4001283C | FULL | Master attributes 3 |

21.146 PPU_FX 129

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX129_SL_ADDR | 0x40012840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX129_SL_SIZE | 0x40012844 | FULL | Slave region, size |
| PERI_MS_PPU_FX129_SL_ATT0 | 0x40012850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX129_SL_ATT1 | 0x40012854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX129_SL_ATT2 | 0x40012858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX129_SL_ATT3 | 0x4001285C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX129_MS_ADDR | 0x40012860 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX129_MS_SIZE | 0x40012864 | FULL | Master region, size |
| PERI_MS_PPU_FX129_MS_ATT0 | 0x40012870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX129_MS_ATT1 | 0x40012874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX129_MS_ATT2 | 0x40012878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX129_MS_ATT3 | 0x4001287C | FULL | Master attributes 3 |

21.147 PPU_FX 130

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX130_SL_ADDR | 0x40012880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX130_SL_SIZE | 0x40012884 | FULL | Slave region, size |
| PERI_MS_PPU_FX130_SL_ATT0 | 0x40012890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX130_SL_ATT1 | 0x40012894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX130_SL_ATT2 | 0x40012898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX130_SL_ATT3 | 0x4001289C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX130_MS_ADDR | 0x400128A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX130_MS_SIZE | 0x400128A4 | FULL | Master region, size |
| PERI_MS_PPU_FX130_MS_ATT0 | 0x400128B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX130_MS_ATT1 | 0x400128B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX130_MS_ATT2 | 0x400128B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX130_MS_ATT3 | 0x400128BC | FULL | Master attributes 3 |

21.148 PPU_FX 131

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX131_SL_ADDR | 0x400128C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX131_SL_SIZE | 0x400128C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX131_SL_ATT0 | 0x400128D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX131_SL_ATT1 | 0x400128D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX131_SL_ATT2 | 0x400128D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX131_SL_ATT3 | 0x400128DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX131_MS_ADDR | 0x400128E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX131_MS_SIZE | 0x400128E4 | FULL | Master region, size |
| PERI_MS_PPU_FX131_MS_ATT0 | 0x400128F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX131_MS_ATT1 | 0x400128F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX131_MS_ATT2 | 0x400128F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX131_MS_ATT3 | 0x400128FC | FULL | Master attributes 3 |

21.149 PPU_FX 132

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX132_SL_ADDR | 0x40012900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX132_SL_SIZE | 0x40012904 | FULL | Slave region, size |
| PERI_MS_PPU_FX132_SL_ATT0 | 0x40012910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX132_SL_ATT1 | 0x40012914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX132_SL_ATT2 | 0x40012918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX132_SL_ATT3 | 0x4001291C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX132_MS_ADDR | 0x40012920 | FULL | Master region, base address |
| PERI_MS_PPU_FX132_MS_SIZE | 0x40012924 | FULL | Master region, size |
| PERI_MS_PPU_FX132_MS_ATT0 | 0x40012930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX132_MS_ATT1 | 0x40012934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX132_MS_ATT2 | 0x40012938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX132_MS_ATT3 | 0x4001293C | FULL | Master attributes 3 |

21.150 PPU_FX 133

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX133_SL_ADDR | 0x40012940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX133_SL_SIZE | 0x40012944 | FULL | Slave region, size |
| PERI_MS_PPU_FX133_SL_ATT0 | 0x40012950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX133_SL_ATT1 | 0x40012954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX133_SL_ATT2 | 0x40012958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX133_SL_ATT3 | 0x4001295C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX133_MS_ADDR | 0x40012960 | FULL | Master region, base address |
| PERI_MS_PPU_FX133_MS_SIZE | 0x40012964 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX133_MS_ATT0 | 0x40012970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX133_MS_ATT1 | 0x40012974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX133_MS_ATT2 | 0x40012978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX133_MS_ATT3 | 0x4001297C | FULL | Master attributes 3 |

21.151 PPU_FX 134

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX134_SL_ADDR | 0x40012980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX134_SL_SIZE | 0x40012984 | FULL | Slave region, size |
| PERI_MS_PPU_FX134_SL_ATT0 | 0x40012990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX134_SL_ATT1 | 0x40012994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX134_SL_ATT2 | 0x40012998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX134_SL_ATT3 | 0x4001299C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX134_MS_ADDR | 0x400129A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX134_MS_SIZE | 0x400129A4 | FULL | Master region, size |
| PERI_MS_PPU_FX134_MS_ATT0 | 0x400129B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX134_MS_ATT1 | 0x400129B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX134_MS_ATT2 | 0x400129B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX134_MS_ATT3 | 0x400129BC | FULL | Master attributes 3 |

21.152 PPU_FX 135

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX135_SL_ADDR | 0x400129C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX135_SL_SIZE | 0x400129C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX135_SL_ATT0 | 0x400129D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX135_SL_ATT1 | 0x400129D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX135_SL_ATT2 | 0x400129D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX135_SL_ATT3 | 0x400129DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX135_MS_ADDR | 0x400129E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX135_MS_SIZE | 0x400129E4 | FULL | Master region, size |
| PERI_MS_PPU_FX135_MS_ATT0 | 0x400129F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX135_MS_ATT1 | 0x400129F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX135_MS_ATT2 | 0x400129F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX135_MS_ATT3 | 0x400129FC | FULL | Master attributes 3 |

21.153 PPU_FX 136

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX136_SL_ADDR | 0x40012A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX136_SL_SIZE | 0x40012A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX136_SL_ATT0 | 0x40012A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX136_SL_ATT1 | 0x40012A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX136_SL_ATT2 | 0x40012A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX136_SL_ATT3 | 0x40012A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX136_MS_ADDR | 0x40012A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX136_MS_SIZE | 0x40012A24 | FULL | Master region, size |
| PERI_MS_PPU_FX136_MS_ATT0 | 0x40012A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX136_MS_ATT1 | 0x40012A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX136_MS_ATT2 | 0x40012A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX136_MS_ATT3 | 0x40012A3C | FULL | Master attributes 3 |

21.154 PPU_FX 137

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX137_SL_ADDR | 0x40012A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX137_SL_SIZE | 0x40012A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX137_SL_ATT0 | 0x40012A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX137_SL_ATT1 | 0x40012A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX137_SL_ATT2 | 0x40012A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX137_SL_ATT3 | 0x40012A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX137_MS_ADDR | 0x40012A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX137_MS_SIZE | 0x40012A64 | FULL | Master region, size |
| PERI_MS_PPU_FX137_MS_ATT0 | 0x40012A70 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX137_MS_ATT1 | 0x40012A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX137_MS_ATT2 | 0x40012A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX137_MS_ATT3 | 0x40012A7C | FULL | Master attributes 3 |

21.155 PPU_FX 138

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX138_SL_ADDR | 0x40012A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX138_SL_SIZE | 0x40012A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX138_SL_ATT0 | 0x40012A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX138_SL_ATT1 | 0x40012A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX138_SL_ATT2 | 0x40012A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX138_SL_ATT3 | 0x40012A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX138_MS_ADDR | 0x40012AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX138_MS_SIZE | 0x40012AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX138_MS_ATT0 | 0x40012AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX138_MS_ATT1 | 0x40012AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX138_MS_ATT2 | 0x40012AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX138_MS_ATT3 | 0x40012ABC | FULL | Master attributes 3 |

21.156 PPU_FX 139

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX139_SL_ADDR | 0x40012AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX139_SL_SIZE | 0x40012AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX139_SL_ATT0 | 0x40012AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX139_SL_ATT1 | 0x40012AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX139_SL_ATT2 | 0x40012AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX139_SL_ATT3 | 0x40012ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX139_MS_ADDR | 0x40012AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX139_MS_SIZE | 0x40012AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX139_MS_ATT0 | 0x40012AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX139_MS_ATT1 | 0x40012AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX139_MS_ATT2 | 0x40012AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX139_MS_ATT3 | 0x40012AFC | FULL | Master attributes 3 |

21.157 PPU_FX 140

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX140_SL_ADDR | 0x40012B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX140_SL_SIZE | 0x40012B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX140_SL_ATT0 | 0x40012B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX140_SL_ATT1 | 0x40012B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX140_SL_ATT2 | 0x40012B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX140_SL_ATT3 | 0x40012B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX140_MS_ADDR | 0x40012B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX140_MS_SIZE | 0x40012B24 | FULL | Master region, size |
| PERI_MS_PPU_FX140_MS_ATT0 | 0x40012B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX140_MS_ATT1 | 0x40012B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX140_MS_ATT2 | 0x40012B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX140_MS_ATT3 | 0x40012B3C | FULL | Master attributes 3 |

21.158 PPU_FX 141

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX141_SL_ADDR | 0x40012B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX141_SL_SIZE | 0x40012B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX141_SL_ATT0 | 0x40012B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX141_SL_ATT1 | 0x40012B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX141_SL_ATT2 | 0x40012B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX141_SL_ATT3 | 0x40012B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX141_MS_ADDR | 0x40012B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX141_MS_SIZE | 0x40012B64 | FULL | Master region, size |
| PERI_MS_PPU_FX141_MS_ATT0 | 0x40012B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX141_MS_ATT1 | 0x40012B74 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX141_MS_ATT2 | 0x40012B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX141_MS_ATT3 | 0x40012B7C | FULL | Master attributes 3 |

21.159 PPU_FX 142

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX142_SL_ADDR | 0x40012B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX142_SL_SIZE | 0x40012B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX142_SL_ATT0 | 0x40012B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX142_SL_ATT1 | 0x40012B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX142_SL_ATT2 | 0x40012B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX142_SL_ATT3 | 0x40012B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX142_MS_ADDR | 0x40012BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX142_MS_SIZE | 0x40012BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX142_MS_ATT0 | 0x40012BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX142_MS_ATT1 | 0x40012BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX142_MS_ATT2 | 0x40012BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX142_MS_ATT3 | 0x40012BBC | FULL | Master attributes 3 |

21.160 PPU_FX 143

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX143_SL_ADDR | 0x40012BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX143_SL_SIZE | 0x40012BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX143_SL_ATT0 | 0x40012BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX143_SL_ATT1 | 0x40012BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX143_SL_ATT2 | 0x40012BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX143_SL_ATT3 | 0x40012BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX143_MS_ADDR | 0x40012BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX143_MS_SIZE | 0x40012BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX143_MS_ATT0 | 0x40012BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX143_MS_ATT1 | 0x40012BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX143_MS_ATT2 | 0x40012BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX143_MS_ATT3 | 0x40012BFC | FULL | Master attributes 3 |

21.161 PPU_FX 144

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX144_SL_ADDR | 0x40012C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX144_SL_SIZE | 0x40012C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX144_SL_ATT0 | 0x40012C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX144_SL_ATT1 | 0x40012C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX144_SL_ATT2 | 0x40012C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX144_SL_ATT3 | 0x40012C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX144_MS_ADDR | 0x40012C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX144_MS_SIZE | 0x40012C24 | FULL | Master region, size |
| PERI_MS_PPU_FX144_MS_ATT0 | 0x40012C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX144_MS_ATT1 | 0x40012C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX144_MS_ATT2 | 0x40012C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX144_MS_ATT3 | 0x40012C3C | FULL | Master attributes 3 |

21.162 PPU_FX 145

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX145_SL_ADDR | 0x40012C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX145_SL_SIZE | 0x40012C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX145_SL_ATT0 | 0x40012C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX145_SL_ATT1 | 0x40012C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX145_SL_ATT2 | 0x40012C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX145_SL_ATT3 | 0x40012C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX145_MS_ADDR | 0x40012C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX145_MS_SIZE | 0x40012C64 | FULL | Master region, size |
| PERI_MS_PPU_FX145_MS_ATT0 | 0x40012C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX145_MS_ATT1 | 0x40012C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX145_MS_ATT2 | 0x40012C78 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX145_MS_ATT3 | 0x40012C7C | FULL | Master attributes 3 |

21.163 PPU_FX 146

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX146_SL_ADDR | 0x40012C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX146_SL_SIZE | 0x40012C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX146_SL_ATT0 | 0x40012C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX146_SL_ATT1 | 0x40012C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX146_SL_ATT2 | 0x40012C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX146_SL_ATT3 | 0x40012C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX146_MS_ADDR | 0x40012CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX146_MS_SIZE | 0x40012CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX146_MS_ATT0 | 0x40012CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX146_MS_ATT1 | 0x40012CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX146_MS_ATT2 | 0x40012CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX146_MS_ATT3 | 0x40012CBC | FULL | Master attributes 3 |

21.164 PPU_FX 147

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX147_SL_ADDR | 0x40012CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX147_SL_SIZE | 0x40012CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX147_SL_ATT0 | 0x40012CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX147_SL_ATT1 | 0x40012CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX147_SL_ATT2 | 0x40012CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX147_SL_ATT3 | 0x40012CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX147_MS_ADDR | 0x40012CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX147_MS_SIZE | 0x40012CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX147_MS_ATT0 | 0x40012CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX147_MS_ATT1 | 0x40012CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX147_MS_ATT2 | 0x40012CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX147_MS_ATT3 | 0x40012CFC | FULL | Master attributes 3 |

21.165 PPU_FX 148

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX148_SL_ADDR | 0x40012D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX148_SL_SIZE | 0x40012D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX148_SL_ATT0 | 0x40012D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX148_SL_ATT1 | 0x40012D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX148_SL_ATT2 | 0x40012D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX148_SL_ATT3 | 0x40012D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX148_MS_ADDR | 0x40012D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX148_MS_SIZE | 0x40012D24 | FULL | Master region, size |
| PERI_MS_PPU_FX148_MS_ATT0 | 0x40012D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX148_MS_ATT1 | 0x40012D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX148_MS_ATT2 | 0x40012D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX148_MS_ATT3 | 0x40012D3C | FULL | Master attributes 3 |

21.166 PPU_FX 149

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX149_SL_ADDR | 0x40012D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX149_SL_SIZE | 0x40012D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX149_SL_ATT0 | 0x40012D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX149_SL_ATT1 | 0x40012D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX149_SL_ATT2 | 0x40012D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX149_SL_ATT3 | 0x40012D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX149_MS_ADDR | 0x40012D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX149_MS_SIZE | 0x40012D64 | FULL | Master region, size |
| PERI_MS_PPU_FX149_MS_ATT0 | 0x40012D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX149_MS_ATT1 | 0x40012D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX149_MS_ATT2 | 0x40012D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX149_MS_ATT3 | 0x40012D7C | FULL | Master attributes 3 |

21.167 PPU_FX 150

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX150_SL_ADDR | 0x40012D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX150_SL_SIZE | 0x40012D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX150_SL_ATT0 | 0x40012D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX150_SL_ATT1 | 0x40012D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX150_SL_ATT2 | 0x40012D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX150_SL_ATT3 | 0x40012D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX150_MS_ADDR | 0x40012DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX150_MS_SIZE | 0x40012DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX150_MS_ATT0 | 0x40012DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX150_MS_ATT1 | 0x40012DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX150_MS_ATT2 | 0x40012DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX150_MS_ATT3 | 0x40012DBC | FULL | Master attributes 3 |

21.168 PPU_FX 151

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX151_SL_ADDR | 0x40012DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX151_SL_SIZE | 0x40012DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX151_SL_ATT0 | 0x40012DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX151_SL_ATT1 | 0x40012DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX151_SL_ATT2 | 0x40012DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX151_SL_ATT3 | 0x40012DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX151_MS_ADDR | 0x40012DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX151_MS_SIZE | 0x40012DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX151_MS_ATT0 | 0x40012DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX151_MS_ATT1 | 0x40012DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX151_MS_ATT2 | 0x40012DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX151_MS_ATT3 | 0x40012DFC | FULL | Master attributes 3 |

21.169 PPU_FX 152

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX152_SL_ADDR | 0x40012E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX152_SL_SIZE | 0x40012E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX152_SL_ATT0 | 0x40012E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX152_SL_ATT1 | 0x40012E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX152_SL_ATT2 | 0x40012E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX152_SL_ATT3 | 0x40012E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX152_MS_ADDR | 0x40012E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX152_MS_SIZE | 0x40012E24 | FULL | Master region, size |
| PERI_MS_PPU_FX152_MS_ATT0 | 0x40012E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX152_MS_ATT1 | 0x40012E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX152_MS_ATT2 | 0x40012E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX152_MS_ATT3 | 0x40012E3C | FULL | Master attributes 3 |

21.170 PPU_FX 153

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX153_SL_ADDR | 0x40012E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX153_SL_SIZE | 0x40012E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX153_SL_ATT0 | 0x40012E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX153_SL_ATT1 | 0x40012E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX153_SL_ATT2 | 0x40012E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX153_SL_ATT3 | 0x40012E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX153_MS_ADDR | 0x40012E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX153_MS_SIZE | 0x40012E64 | FULL | Master region, size |
| PERI_MS_PPU_FX153_MS_ATT0 | 0x40012E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX153_MS_ATT1 | 0x40012E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX153_MS_ATT2 | 0x40012E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX153_MS_ATT3 | 0x40012E7C | FULL | Master attributes 3 |

21.171 PPU_FX 154

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX154_SL_ADDR | 0x40012E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX154_SL_SIZE | 0x40012E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX154_SL_ATT0 | 0x40012E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX154_SL_ATT1 | 0x40012E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX154_SL_ATT2 | 0x40012E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX154_SL_ATT3 | 0x40012E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX154_MS_ADDR | 0x40012EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX154_MS_SIZE | 0x40012EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX154_MS_ATT0 | 0x40012EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX154_MS_ATT1 | 0x40012EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX154_MS_ATT2 | 0x40012EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX154_MS_ATT3 | 0x40012EBC | FULL | Master attributes 3 |

21.172 PPU_FX 155

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX155_SL_ADDR | 0x40012EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX155_SL_SIZE | 0x40012EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX155_SL_ATT0 | 0x40012ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX155_SL_ATT1 | 0x40012ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX155_SL_ATT2 | 0x40012ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX155_SL_ATT3 | 0x40012EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX155_MS_ADDR | 0x40012EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX155_MS_SIZE | 0x40012EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX155_MS_ATT0 | 0x40012EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX155_MS_ATT1 | 0x40012EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX155_MS_ATT2 | 0x40012EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX155_MS_ATT3 | 0x40012EFC | FULL | Master attributes 3 |

21.173 PPU_FX 156

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX156_SL_ADDR | 0x40012F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX156_SL_SIZE | 0x40012F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX156_SL_ATT0 | 0x40012F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX156_SL_ATT1 | 0x40012F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX156_SL_ATT2 | 0x40012F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX156_SL_ATT3 | 0x40012F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX156_MS_ADDR | 0x40012F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX156_MS_SIZE | 0x40012F24 | FULL | Master region, size |
| PERI_MS_PPU_FX156_MS_ATT0 | 0x40012F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX156_MS_ATT1 | 0x40012F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX156_MS_ATT2 | 0x40012F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX156_MS_ATT3 | 0x40012F3C | FULL | Master attributes 3 |

21.174 PPU_FX 157

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX157_SL_ADDR | 0x40012F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX157_SL_SIZE | 0x40012F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX157_SL_ATT0 | 0x40012F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX157_SL_ATT1 | 0x40012F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX157_SL_ATT2 | 0x40012F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX157_SL_ATT3 | 0x40012F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX157_MS_ADDR | 0x40012F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX157_MS_SIZE | 0x40012F64 | FULL | Master region, size |
| PERI_MS_PPU_FX157_MS_ATT0 | 0x40012F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX157_MS_ATT1 | 0x40012F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX157_MS_ATT2 | 0x40012F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX157_MS_ATT3 | 0x40012F7C | FULL | Master attributes 3 |

21.175 PPU_FX 158

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX158_SL_ADDR | 0x40012F80 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX158_SL_SIZE | 0x40012F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX158_SL_ATT0 | 0x40012F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX158_SL_ATT1 | 0x40012F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX158_SL_ATT2 | 0x40012F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX158_SL_ATT3 | 0x40012F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX158_MS_ADDR | 0x40012FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX158_MS_SIZE | 0x40012FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX158_MS_ATT0 | 0x40012FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX158_MS_ATT1 | 0x40012FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX158_MS_ATT2 | 0x40012FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX158_MS_ATT3 | 0x40012FBC | FULL | Master attributes 3 |

21.176 PPU_FX 159

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX159_SL_ADDR | 0x40012FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX159_SL_SIZE | 0x40012FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX159_SL_ATT0 | 0x40012FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX159_SL_ATT1 | 0x40012FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX159_SL_ATT2 | 0x40012FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX159_SL_ATT3 | 0x40012FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX159_MS_ADDR | 0x40012FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX159_MS_SIZE | 0x40012FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX159_MS_ATT0 | 0x40012FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX159_MS_ATT1 | 0x40012FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX159_MS_ATT2 | 0x40012FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX159_MS_ATT3 | 0x40012FFC | FULL | Master attributes 3 |

21.177 PPU_FX 160

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX160_SL_ADDR | 0x40013000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX160_SL_SIZE | 0x40013004 | FULL | Slave region, size |
| PERI_MS_PPU_FX160_SL_ATT0 | 0x40013010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX160_SL_ATT1 | 0x40013014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX160_SL_ATT2 | 0x40013018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX160_SL_ATT3 | 0x4001301C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX160_MS_ADDR | 0x40013020 | FULL | Master region, base address |
| PERI_MS_PPU_FX160_MS_SIZE | 0x40013024 | FULL | Master region, size |
| PERI_MS_PPU_FX160_MS_ATT0 | 0x40013030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX160_MS_ATT1 | 0x40013034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX160_MS_ATT2 | 0x40013038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX160_MS_ATT3 | 0x4001303C | FULL | Master attributes 3 |

21.178 PPU_FX 161

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX161_SL_ADDR | 0x40013040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX161_SL_SIZE | 0x40013044 | FULL | Slave region, size |
| PERI_MS_PPU_FX161_SL_ATT0 | 0x40013050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX161_SL_ATT1 | 0x40013054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX161_SL_ATT2 | 0x40013058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX161_SL_ATT3 | 0x4001305C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX161_MS_ADDR | 0x40013060 | FULL | Master region, base address |
| PERI_MS_PPU_FX161_MS_SIZE | 0x40013064 | FULL | Master region, size |
| PERI_MS_PPU_FX161_MS_ATT0 | 0x40013070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX161_MS_ATT1 | 0x40013074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX161_MS_ATT2 | 0x40013078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX161_MS_ATT3 | 0x4001307C | FULL | Master attributes 3 |

21.179 PPU_FX 162

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX162_SL_ADDR | 0x40013080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX162_SL_SIZE | 0x40013084 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX162_SL_ATT0 | 0x40013090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX162_SL_ATT1 | 0x40013094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX162_SL_ATT2 | 0x40013098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX162_SL_ATT3 | 0x4001309C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX162_MS_ADDR | 0x400130A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX162_MS_SIZE | 0x400130A4 | FULL | Master region, size |
| PERI_MS_PPU_FX162_MS_ATT0 | 0x400130B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX162_MS_ATT1 | 0x400130B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX162_MS_ATT2 | 0x400130B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX162_MS_ATT3 | 0x400130BC | FULL | Master attributes 3 |

21.180 PPU_FX 163

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX163_SL_ADDR | 0x400130C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX163_SL_SIZE | 0x400130C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX163_SL_ATT0 | 0x400130D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX163_SL_ATT1 | 0x400130D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX163_SL_ATT2 | 0x400130D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX163_SL_ATT3 | 0x400130DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX163_MS_ADDR | 0x400130E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX163_MS_SIZE | 0x400130E4 | FULL | Master region, size |
| PERI_MS_PPU_FX163_MS_ATT0 | 0x400130F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX163_MS_ATT1 | 0x400130F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX163_MS_ATT2 | 0x400130F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX163_MS_ATT3 | 0x400130FC | FULL | Master attributes 3 |

21.181 PPU_FX 164

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX164_SL_ADDR | 0x40013100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX164_SL_SIZE | 0x40013104 | FULL | Slave region, size |
| PERI_MS_PPU_FX164_SL_ATT0 | 0x40013110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX164_SL_ATT1 | 0x40013114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX164_SL_ATT2 | 0x40013118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX164_SL_ATT3 | 0x4001311C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX164_MS_ADDR | 0x40013120 | FULL | Master region, base address |
| PERI_MS_PPU_FX164_MS_SIZE | 0x40013124 | FULL | Master region, size |
| PERI_MS_PPU_FX164_MS_ATT0 | 0x40013130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX164_MS_ATT1 | 0x40013134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX164_MS_ATT2 | 0x40013138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX164_MS_ATT3 | 0x4001313C | FULL | Master attributes 3 |

21.182 PPU_FX 165

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX165_SL_ADDR | 0x40013140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX165_SL_SIZE | 0x40013144 | FULL | Slave region, size |
| PERI_MS_PPU_FX165_SL_ATT0 | 0x40013150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX165_SL_ATT1 | 0x40013154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX165_SL_ATT2 | 0x40013158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX165_SL_ATT3 | 0x4001315C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX165_MS_ADDR | 0x40013160 | FULL | Master region, base address |
| PERI_MS_PPU_FX165_MS_SIZE | 0x40013164 | FULL | Master region, size |
| PERI_MS_PPU_FX165_MS_ATT0 | 0x40013170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX165_MS_ATT1 | 0x40013174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX165_MS_ATT2 | 0x40013178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX165_MS_ATT3 | 0x4001317C | FULL | Master attributes 3 |

21.183 PPU_FX 166

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX166_SL_ADDR | 0x40013180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX166_SL_SIZE | 0x40013184 | FULL | Slave region, size |
| PERI_MS_PPU_FX166_SL_ATT0 | 0x40013190 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX166_SL_ATT1 | 0x40013194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX166_SL_ATT2 | 0x40013198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX166_SL_ATT3 | 0x4001319C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX166_MS_ADDR | 0x400131A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX166_MS_SIZE | 0x400131A4 | FULL | Master region, size |
| PERI_MS_PPU_FX166_MS_ATT0 | 0x400131B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX166_MS_ATT1 | 0x400131B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX166_MS_ATT2 | 0x400131B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX166_MS_ATT3 | 0x400131BC | FULL | Master attributes 3 |

21.184 PPU_FX 167

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX167_SL_ADDR | 0x400131C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX167_SL_SIZE | 0x400131C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX167_SL_ATT0 | 0x400131D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX167_SL_ATT1 | 0x400131D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX167_SL_ATT2 | 0x400131D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX167_SL_ATT3 | 0x400131DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX167_MS_ADDR | 0x400131E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX167_MS_SIZE | 0x400131E4 | FULL | Master region, size |
| PERI_MS_PPU_FX167_MS_ATT0 | 0x400131F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX167_MS_ATT1 | 0x400131F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX167_MS_ATT2 | 0x400131F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX167_MS_ATT3 | 0x400131FC | FULL | Master attributes 3 |

21.185 PPU_FX 168

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX168_SL_ADDR | 0x40013200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX168_SL_SIZE | 0x40013204 | FULL | Slave region, size |
| PERI_MS_PPU_FX168_SL_ATT0 | 0x40013210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX168_SL_ATT1 | 0x40013214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX168_SL_ATT2 | 0x40013218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX168_SL_ATT3 | 0x4001321C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX168_MS_ADDR | 0x40013220 | FULL | Master region, base address |
| PERI_MS_PPU_FX168_MS_SIZE | 0x40013224 | FULL | Master region, size |
| PERI_MS_PPU_FX168_MS_ATT0 | 0x40013230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX168_MS_ATT1 | 0x40013234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX168_MS_ATT2 | 0x40013238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX168_MS_ATT3 | 0x4001323C | FULL | Master attributes 3 |

21.186 PPU_FX 169

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX169_SL_ADDR | 0x40013240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX169_SL_SIZE | 0x40013244 | FULL | Slave region, size |
| PERI_MS_PPU_FX169_SL_ATT0 | 0x40013250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX169_SL_ATT1 | 0x40013254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX169_SL_ATT2 | 0x40013258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX169_SL_ATT3 | 0x4001325C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX169_MS_ADDR | 0x40013260 | FULL | Master region, base address |
| PERI_MS_PPU_FX169_MS_SIZE | 0x40013264 | FULL | Master region, size |
| PERI_MS_PPU_FX169_MS_ATT0 | 0x40013270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX169_MS_ATT1 | 0x40013274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX169_MS_ATT2 | 0x40013278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX169_MS_ATT3 | 0x4001327C | FULL | Master attributes 3 |

21.187 PPU_FX 170

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX170_SL_ADDR | 0x40013280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX170_SL_SIZE | 0x40013284 | FULL | Slave region, size |
| PERI_MS_PPU_FX170_SL_ATT0 | 0x40013290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX170_SL_ATT1 | 0x40013294 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX170_SL_ATT2 | 0x40013298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX170_SL_ATT3 | 0x4001329C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX170_MS_ADDR | 0x400132A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX170_MS_SIZE | 0x400132A4 | FULL | Master region, size |
| PERI_MS_PPU_FX170_MS_ATT0 | 0x400132B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX170_MS_ATT1 | 0x400132B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX170_MS_ATT2 | 0x400132B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX170_MS_ATT3 | 0x400132BC | FULL | Master attributes 3 |

21.188 PPU_FX 171

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX171_SL_ADDR | 0x400132C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX171_SL_SIZE | 0x400132C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX171_SL_ATT0 | 0x400132D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX171_SL_ATT1 | 0x400132D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX171_SL_ATT2 | 0x400132D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX171_SL_ATT3 | 0x400132DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX171_MS_ADDR | 0x400132E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX171_MS_SIZE | 0x400132E4 | FULL | Master region, size |
| PERI_MS_PPU_FX171_MS_ATT0 | 0x400132F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX171_MS_ATT1 | 0x400132F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX171_MS_ATT2 | 0x400132F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX171_MS_ATT3 | 0x400132FC | FULL | Master attributes 3 |

21.189 PPU_FX 172

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX172_SL_ADDR | 0x40013300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX172_SL_SIZE | 0x40013304 | FULL | Slave region, size |
| PERI_MS_PPU_FX172_SL_ATT0 | 0x40013310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX172_SL_ATT1 | 0x40013314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX172_SL_ATT2 | 0x40013318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX172_SL_ATT3 | 0x4001331C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX172_MS_ADDR | 0x40013320 | FULL | Master region, base address |
| PERI_MS_PPU_FX172_MS_SIZE | 0x40013324 | FULL | Master region, size |
| PERI_MS_PPU_FX172_MS_ATT0 | 0x40013330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX172_MS_ATT1 | 0x40013334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX172_MS_ATT2 | 0x40013338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX172_MS_ATT3 | 0x4001333C | FULL | Master attributes 3 |

21.190 PPU_FX 173

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX173_SL_ADDR | 0x40013340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX173_SL_SIZE | 0x40013344 | FULL | Slave region, size |
| PERI_MS_PPU_FX173_SL_ATT0 | 0x40013350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX173_SL_ATT1 | 0x40013354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX173_SL_ATT2 | 0x40013358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX173_SL_ATT3 | 0x4001335C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX173_MS_ADDR | 0x40013360 | FULL | Master region, base address |
| PERI_MS_PPU_FX173_MS_SIZE | 0x40013364 | FULL | Master region, size |
| PERI_MS_PPU_FX173_MS_ATT0 | 0x40013370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX173_MS_ATT1 | 0x40013374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX173_MS_ATT2 | 0x40013378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX173_MS_ATT3 | 0x4001337C | FULL | Master attributes 3 |

21.191 PPU_FX 174

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX174_SL_ADDR | 0x40013380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX174_SL_SIZE | 0x40013384 | FULL | Slave region, size |
| PERI_MS_PPU_FX174_SL_ATT0 | 0x40013390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX174_SL_ATT1 | 0x40013394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX174_SL_ATT2 | 0x40013398 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX174_SL_ATT3 | 0x4001339C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX174_MS_ADDR | 0x400133A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX174_MS_SIZE | 0x400133A4 | FULL | Master region, size |
| PERI_MS_PPU_FX174_MS_ATT0 | 0x400133B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX174_MS_ATT1 | 0x400133B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX174_MS_ATT2 | 0x400133B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX174_MS_ATT3 | 0x400133BC | FULL | Master attributes 3 |

21.192 PPU_FX 175

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX175_SL_ADDR | 0x400133C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX175_SL_SIZE | 0x400133C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX175_SL_ATT0 | 0x400133D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX175_SL_ATT1 | 0x400133D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX175_SL_ATT2 | 0x400133D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX175_SL_ATT3 | 0x400133DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX175_MS_ADDR | 0x400133E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX175_MS_SIZE | 0x400133E4 | FULL | Master region, size |
| PERI_MS_PPU_FX175_MS_ATT0 | 0x400133F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX175_MS_ATT1 | 0x400133F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX175_MS_ATT2 | 0x400133F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX175_MS_ATT3 | 0x400133FC | FULL | Master attributes 3 |

21.193 PPU_FX 176

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX176_SL_ADDR | 0x40013400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX176_SL_SIZE | 0x40013404 | FULL | Slave region, size |
| PERI_MS_PPU_FX176_SL_ATT0 | 0x40013410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX176_SL_ATT1 | 0x40013414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX176_SL_ATT2 | 0x40013418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX176_SL_ATT3 | 0x4001341C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX176_MS_ADDR | 0x40013420 | FULL | Master region, base address |
| PERI_MS_PPU_FX176_MS_SIZE | 0x40013424 | FULL | Master region, size |
| PERI_MS_PPU_FX176_MS_ATT0 | 0x40013430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX176_MS_ATT1 | 0x40013434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX176_MS_ATT2 | 0x40013438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX176_MS_ATT3 | 0x4001343C | FULL | Master attributes 3 |

21.194 PPU_FX 177

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX177_SL_ADDR | 0x40013440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX177_SL_SIZE | 0x40013444 | FULL | Slave region, size |
| PERI_MS_PPU_FX177_SL_ATT0 | 0x40013450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX177_SL_ATT1 | 0x40013454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX177_SL_ATT2 | 0x40013458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX177_SL_ATT3 | 0x4001345C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX177_MS_ADDR | 0x40013460 | FULL | Master region, base address |
| PERI_MS_PPU_FX177_MS_SIZE | 0x40013464 | FULL | Master region, size |
| PERI_MS_PPU_FX177_MS_ATT0 | 0x40013470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX177_MS_ATT1 | 0x40013474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX177_MS_ATT2 | 0x40013478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX177_MS_ATT3 | 0x4001347C | FULL | Master attributes 3 |

21.195 PPU_FX 178

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX178_SL_ADDR | 0x40013480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX178_SL_SIZE | 0x40013484 | FULL | Slave region, size |
| PERI_MS_PPU_FX178_SL_ATT0 | 0x40013490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX178_SL_ATT1 | 0x40013494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX178_SL_ATT2 | 0x40013498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX178_SL_ATT3 | 0x4001349C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX178_MS_ADDR | 0x400134A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX178_MS_SIZE | 0x400134A4 | FULL | Master region, size |
| PERI_MS_PPU_FX178_MS_ATT0 | 0x400134B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX178_MS_ATT1 | 0x400134B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX178_MS_ATT2 | 0x400134B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX178_MS_ATT3 | 0x400134BC | FULL | Master attributes 3 |

21.196 PPU_FX 179

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX179_SL_ADDR | 0x400134C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX179_SL_SIZE | 0x400134C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX179_SL_ATT0 | 0x400134D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX179_SL_ATT1 | 0x400134D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX179_SL_ATT2 | 0x400134D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX179_SL_ATT3 | 0x400134DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX179_MS_ADDR | 0x400134E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX179_MS_SIZE | 0x400134E4 | FULL | Master region, size |
| PERI_MS_PPU_FX179_MS_ATT0 | 0x400134F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX179_MS_ATT1 | 0x400134F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX179_MS_ATT2 | 0x400134F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX179_MS_ATT3 | 0x400134FC | FULL | Master attributes 3 |

21.197 PPU_FX 180

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX180_SL_ADDR | 0x40013500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX180_SL_SIZE | 0x40013504 | FULL | Slave region, size |
| PERI_MS_PPU_FX180_SL_ATT0 | 0x40013510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX180_SL_ATT1 | 0x40013514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX180_SL_ATT2 | 0x40013518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX180_SL_ATT3 | 0x4001351C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX180_MS_ADDR | 0x40013520 | FULL | Master region, base address |
| PERI_MS_PPU_FX180_MS_SIZE | 0x40013524 | FULL | Master region, size |
| PERI_MS_PPU_FX180_MS_ATT0 | 0x40013530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX180_MS_ATT1 | 0x40013534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX180_MS_ATT2 | 0x40013538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX180_MS_ATT3 | 0x4001353C | FULL | Master attributes 3 |

21.198 PPU_FX 181

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX181_SL_ADDR | 0x40013540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX181_SL_SIZE | 0x40013544 | FULL | Slave region, size |
| PERI_MS_PPU_FX181_SL_ATT0 | 0x40013550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX181_SL_ATT1 | 0x40013554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX181_SL_ATT2 | 0x40013558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX181_SL_ATT3 | 0x4001355C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX181_MS_ADDR | 0x40013560 | FULL | Master region, base address |
| PERI_MS_PPU_FX181_MS_SIZE | 0x40013564 | FULL | Master region, size |
| PERI_MS_PPU_FX181_MS_ATT0 | 0x40013570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX181_MS_ATT1 | 0x40013574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX181_MS_ATT2 | 0x40013578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX181_MS_ATT3 | 0x4001357C | FULL | Master attributes 3 |

21.199 PPU_FX 182

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX182_SL_ADDR | 0x40013580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX182_SL_SIZE | 0x40013584 | FULL | Slave region, size |
| PERI_MS_PPU_FX182_SL_ATT0 | 0x40013590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX182_SL_ATT1 | 0x40013594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX182_SL_ATT2 | 0x40013598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX182_SL_ATT3 | 0x4001359C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX182_MS_ADDR | 0x400135A0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX182_MS_SIZE | 0x400135A4 | FULL | Master region, size |
| PERI_MS_PPU_FX182_MS_ATT0 | 0x400135B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX182_MS_ATT1 | 0x400135B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX182_MS_ATT2 | 0x400135B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX182_MS_ATT3 | 0x400135BC | FULL | Master attributes 3 |

21.200 PPU_FX 183

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX183_SL_ADDR | 0x400135C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX183_SL_SIZE | 0x400135C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX183_SL_ATT0 | 0x400135D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX183_SL_ATT1 | 0x400135D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX183_SL_ATT2 | 0x400135D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX183_SL_ATT3 | 0x400135DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX183_MS_ADDR | 0x400135E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX183_MS_SIZE | 0x400135E4 | FULL | Master region, size |
| PERI_MS_PPU_FX183_MS_ATT0 | 0x400135F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX183_MS_ATT1 | 0x400135F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX183_MS_ATT2 | 0x400135F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX183_MS_ATT3 | 0x400135FC | FULL | Master attributes 3 |

21.201 PPU_FX 184

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX184_SL_ADDR | 0x40013600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX184_SL_SIZE | 0x40013604 | FULL | Slave region, size |
| PERI_MS_PPU_FX184_SL_ATT0 | 0x40013610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX184_SL_ATT1 | 0x40013614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX184_SL_ATT2 | 0x40013618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX184_SL_ATT3 | 0x4001361C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX184_MS_ADDR | 0x40013620 | FULL | Master region, base address |
| PERI_MS_PPU_FX184_MS_SIZE | 0x40013624 | FULL | Master region, size |
| PERI_MS_PPU_FX184_MS_ATT0 | 0x40013630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX184_MS_ATT1 | 0x40013634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX184_MS_ATT2 | 0x40013638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX184_MS_ATT3 | 0x4001363C | FULL | Master attributes 3 |

21.202 PPU_FX 185

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX185_SL_ADDR | 0x40013640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX185_SL_SIZE | 0x40013644 | FULL | Slave region, size |
| PERI_MS_PPU_FX185_SL_ATT0 | 0x40013650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX185_SL_ATT1 | 0x40013654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX185_SL_ATT2 | 0x40013658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX185_SL_ATT3 | 0x4001365C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX185_MS_ADDR | 0x40013660 | FULL | Master region, base address |
| PERI_MS_PPU_FX185_MS_SIZE | 0x40013664 | FULL | Master region, size |
| PERI_MS_PPU_FX185_MS_ATT0 | 0x40013670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX185_MS_ATT1 | 0x40013674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX185_MS_ATT2 | 0x40013678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX185_MS_ATT3 | 0x4001367C | FULL | Master attributes 3 |

21.203 PPU_FX 186

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX186_SL_ADDR | 0x40013680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX186_SL_SIZE | 0x40013684 | FULL | Slave region, size |
| PERI_MS_PPU_FX186_SL_ATT0 | 0x40013690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX186_SL_ATT1 | 0x40013694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX186_SL_ATT2 | 0x40013698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX186_SL_ATT3 | 0x4001369C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX186_MS_ADDR | 0x400136A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX186_MS_SIZE | 0x400136A4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX186_MS_ATT0 | 0x400136B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX186_MS_ATT1 | 0x400136B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX186_MS_ATT2 | 0x400136B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX186_MS_ATT3 | 0x400136BC | FULL | Master attributes 3 |

21.204 PPU_FX 187

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX187_SL_ADDR | 0x400136C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX187_SL_SIZE | 0x400136C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX187_SL_ATT0 | 0x400136D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX187_SL_ATT1 | 0x400136D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX187_SL_ATT2 | 0x400136D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX187_SL_ATT3 | 0x400136DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX187_MS_ADDR | 0x400136E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX187_MS_SIZE | 0x400136E4 | FULL | Master region, size |
| PERI_MS_PPU_FX187_MS_ATT0 | 0x400136F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX187_MS_ATT1 | 0x400136F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX187_MS_ATT2 | 0x400136F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX187_MS_ATT3 | 0x400136FC | FULL | Master attributes 3 |

21.205 PPU_FX 188

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX188_SL_ADDR | 0x40013700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX188_SL_SIZE | 0x40013704 | FULL | Slave region, size |
| PERI_MS_PPU_FX188_SL_ATT0 | 0x40013710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX188_SL_ATT1 | 0x40013714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX188_SL_ATT2 | 0x40013718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX188_SL_ATT3 | 0x4001371C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX188_MS_ADDR | 0x40013720 | FULL | Master region, base address |
| PERI_MS_PPU_FX188_MS_SIZE | 0x40013724 | FULL | Master region, size |
| PERI_MS_PPU_FX188_MS_ATT0 | 0x40013730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX188_MS_ATT1 | 0x40013734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX188_MS_ATT2 | 0x40013738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX188_MS_ATT3 | 0x4001373C | FULL | Master attributes 3 |

21.206 PPU_FX 189

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX189_SL_ADDR | 0x40013740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX189_SL_SIZE | 0x40013744 | FULL | Slave region, size |
| PERI_MS_PPU_FX189_SL_ATT0 | 0x40013750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX189_SL_ATT1 | 0x40013754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX189_SL_ATT2 | 0x40013758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX189_SL_ATT3 | 0x4001375C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX189_MS_ADDR | 0x40013760 | FULL | Master region, base address |
| PERI_MS_PPU_FX189_MS_SIZE | 0x40013764 | FULL | Master region, size |
| PERI_MS_PPU_FX189_MS_ATT0 | 0x40013770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX189_MS_ATT1 | 0x40013774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX189_MS_ATT2 | 0x40013778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX189_MS_ATT3 | 0x4001377C | FULL | Master attributes 3 |

21.207 PPU_FX 190

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX190_SL_ADDR | 0x40013780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX190_SL_SIZE | 0x40013784 | FULL | Slave region, size |
| PERI_MS_PPU_FX190_SL_ATT0 | 0x40013790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX190_SL_ATT1 | 0x40013794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX190_SL_ATT2 | 0x40013798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX190_SL_ATT3 | 0x4001379C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX190_MS_ADDR | 0x400137A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX190_MS_SIZE | 0x400137A4 | FULL | Master region, size |
| PERI_MS_PPU_FX190_MS_ATT0 | 0x400137B0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX190_MS_ATT1 | 0x400137B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX190_MS_ATT2 | 0x400137B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX190_MS_ATT3 | 0x400137BC | FULL | Master attributes 3 |

21.208 PPU_FX 191

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX191_SL_ADDR | 0x400137C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX191_SL_SIZE | 0x400137C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX191_SL_ATT0 | 0x400137D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX191_SL_ATT1 | 0x400137D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX191_SL_ATT2 | 0x400137D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX191_SL_ATT3 | 0x400137DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX191_MS_ADDR | 0x400137E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX191_MS_SIZE | 0x400137E4 | FULL | Master region, size |
| PERI_MS_PPU_FX191_MS_ATT0 | 0x400137F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX191_MS_ATT1 | 0x400137F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX191_MS_ATT2 | 0x400137F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX191_MS_ATT3 | 0x400137FC | FULL | Master attributes 3 |

21.209 PPU_FX 192

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX192_SL_ADDR | 0x40013800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX192_SL_SIZE | 0x40013804 | FULL | Slave region, size |
| PERI_MS_PPU_FX192_SL_ATT0 | 0x40013810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX192_SL_ATT1 | 0x40013814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX192_SL_ATT2 | 0x40013818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX192_SL_ATT3 | 0x4001381C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX192_MS_ADDR | 0x40013820 | FULL | Master region, base address |
| PERI_MS_PPU_FX192_MS_SIZE | 0x40013824 | FULL | Master region, size |
| PERI_MS_PPU_FX192_MS_ATT0 | 0x40013830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX192_MS_ATT1 | 0x40013834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX192_MS_ATT2 | 0x40013838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX192_MS_ATT3 | 0x4001383C | FULL | Master attributes 3 |

21.210 PPU_FX 193

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX193_SL_ADDR | 0x40013840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX193_SL_SIZE | 0x40013844 | FULL | Slave region, size |
| PERI_MS_PPU_FX193_SL_ATT0 | 0x40013850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX193_SL_ATT1 | 0x40013854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX193_SL_ATT2 | 0x40013858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX193_SL_ATT3 | 0x4001385C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX193_MS_ADDR | 0x40013860 | FULL | Master region, base address |
| PERI_MS_PPU_FX193_MS_SIZE | 0x40013864 | FULL | Master region, size |
| PERI_MS_PPU_FX193_MS_ATT0 | 0x40013870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX193_MS_ATT1 | 0x40013874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX193_MS_ATT2 | 0x40013878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX193_MS_ATT3 | 0x4001387C | FULL | Master attributes 3 |

21.211 PPU_FX 194

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX194_SL_ADDR | 0x40013880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX194_SL_SIZE | 0x40013884 | FULL | Slave region, size |
| PERI_MS_PPU_FX194_SL_ATT0 | 0x40013890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX194_SL_ATT1 | 0x40013894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX194_SL_ATT2 | 0x40013898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX194_SL_ATT3 | 0x4001389C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX194_MS_ADDR | 0x400138A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX194_MS_SIZE | 0x400138A4 | FULL | Master region, size |
| PERI_MS_PPU_FX194_MS_ATT0 | 0x400138B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX194_MS_ATT1 | 0x400138B4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX194_MS_ATT2 | 0x400138B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX194_MS_ATT3 | 0x400138BC | FULL | Master attributes 3 |

21.212 PPU_FX 195

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX195_SL_ADDR | 0x400138C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX195_SL_SIZE | 0x400138C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX195_SL_ATT0 | 0x400138D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX195_SL_ATT1 | 0x400138D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX195_SL_ATT2 | 0x400138D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX195_SL_ATT3 | 0x400138DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX195_MS_ADDR | 0x400138E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX195_MS_SIZE | 0x400138E4 | FULL | Master region, size |
| PERI_MS_PPU_FX195_MS_ATT0 | 0x400138F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX195_MS_ATT1 | 0x400138F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX195_MS_ATT2 | 0x400138F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX195_MS_ATT3 | 0x400138FC | FULL | Master attributes 3 |

21.213 PPU_FX 196

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX196_SL_ADDR | 0x40013900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX196_SL_SIZE | 0x40013904 | FULL | Slave region, size |
| PERI_MS_PPU_FX196_SL_ATT0 | 0x40013910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX196_SL_ATT1 | 0x40013914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX196_SL_ATT2 | 0x40013918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX196_SL_ATT3 | 0x4001391C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX196_MS_ADDR | 0x40013920 | FULL | Master region, base address |
| PERI_MS_PPU_FX196_MS_SIZE | 0x40013924 | FULL | Master region, size |
| PERI_MS_PPU_FX196_MS_ATT0 | 0x40013930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX196_MS_ATT1 | 0x40013934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX196_MS_ATT2 | 0x40013938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX196_MS_ATT3 | 0x4001393C | FULL | Master attributes 3 |

21.214 PPU_FX 197

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX197_SL_ADDR | 0x40013940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX197_SL_SIZE | 0x40013944 | FULL | Slave region, size |
| PERI_MS_PPU_FX197_SL_ATT0 | 0x40013950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX197_SL_ATT1 | 0x40013954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX197_SL_ATT2 | 0x40013958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX197_SL_ATT3 | 0x4001395C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX197_MS_ADDR | 0x40013960 | FULL | Master region, base address |
| PERI_MS_PPU_FX197_MS_SIZE | 0x40013964 | FULL | Master region, size |
| PERI_MS_PPU_FX197_MS_ATT0 | 0x40013970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX197_MS_ATT1 | 0x40013974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX197_MS_ATT2 | 0x40013978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX197_MS_ATT3 | 0x4001397C | FULL | Master attributes 3 |

21.215 PPU_FX 198

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX198_SL_ADDR | 0x40013980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX198_SL_SIZE | 0x40013984 | FULL | Slave region, size |
| PERI_MS_PPU_FX198_SL_ATT0 | 0x40013990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX198_SL_ATT1 | 0x40013994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX198_SL_ATT2 | 0x40013998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX198_SL_ATT3 | 0x4001399C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX198_MS_ADDR | 0x400139A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX198_MS_SIZE | 0x400139A4 | FULL | Master region, size |
| PERI_MS_PPU_FX198_MS_ATT0 | 0x400139B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX198_MS_ATT1 | 0x400139B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX198_MS_ATT2 | 0x400139B8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX198_MS_ATT3 | 0x400139BC | FULL | Master attributes 3 |

21.216 PPU_FX 199

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX199_SL_ADDR | 0x400139C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX199_SL_SIZE | 0x400139C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX199_SL_ATT0 | 0x400139D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX199_SL_ATT1 | 0x400139D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX199_SL_ATT2 | 0x400139D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX199_SL_ATT3 | 0x400139DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX199_MS_ADDR | 0x400139E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX199_MS_SIZE | 0x400139E4 | FULL | Master region, size |
| PERI_MS_PPU_FX199_MS_ATT0 | 0x400139F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX199_MS_ATT1 | 0x400139F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX199_MS_ATT2 | 0x400139F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX199_MS_ATT3 | 0x400139FC | FULL | Master attributes 3 |

21.217 PPU_FX 200

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX200_SL_ADDR | 0x40013A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX200_SL_SIZE | 0x40013A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX200_SL_ATT0 | 0x40013A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX200_SL_ATT1 | 0x40013A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX200_SL_ATT2 | 0x40013A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX200_SL_ATT3 | 0x40013A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX200_MS_ADDR | 0x40013A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX200_MS_SIZE | 0x40013A24 | FULL | Master region, size |
| PERI_MS_PPU_FX200_MS_ATT0 | 0x40013A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX200_MS_ATT1 | 0x40013A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX200_MS_ATT2 | 0x40013A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX200_MS_ATT3 | 0x40013A3C | FULL | Master attributes 3 |

21.218 PPU_FX 201

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX201_SL_ADDR | 0x40013A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX201_SL_SIZE | 0x40013A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX201_SL_ATT0 | 0x40013A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX201_SL_ATT1 | 0x40013A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX201_SL_ATT2 | 0x40013A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX201_SL_ATT3 | 0x40013A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX201_MS_ADDR | 0x40013A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX201_MS_SIZE | 0x40013A64 | FULL | Master region, size |
| PERI_MS_PPU_FX201_MS_ATT0 | 0x40013A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX201_MS_ATT1 | 0x40013A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX201_MS_ATT2 | 0x40013A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX201_MS_ATT3 | 0x40013A7C | FULL | Master attributes 3 |

21.219 PPU_FX 202

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX202_SL_ADDR | 0x40013A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX202_SL_SIZE | 0x40013A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX202_SL_ATT0 | 0x40013A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX202_SL_ATT1 | 0x40013A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX202_SL_ATT2 | 0x40013A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX202_SL_ATT3 | 0x40013A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX202_MS_ADDR | 0x40013AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX202_MS_SIZE | 0x40013AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX202_MS_ATT0 | 0x40013AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX202_MS_ATT1 | 0x40013AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX202_MS_ATT2 | 0x40013AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX202_MS_ATT3 | 0x40013ABC | FULL | Master attributes 3 |

21.220 PPU_FX 203

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX203_SL_ADDR | 0x40013AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX203_SL_SIZE | 0x40013AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX203_SL_ATT0 | 0x40013AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX203_SL_ATT1 | 0x40013AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX203_SL_ATT2 | 0x40013AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX203_SL_ATT3 | 0x40013ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX203_MS_ADDR | 0x40013AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX203_MS_SIZE | 0x40013AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX203_MS_ATT0 | 0x40013AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX203_MS_ATT1 | 0x40013AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX203_MS_ATT2 | 0x40013AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX203_MS_ATT3 | 0x40013AFC | FULL | Master attributes 3 |

21.221 PPU_FX 204

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX204_SL_ADDR | 0x40013B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX204_SL_SIZE | 0x40013B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX204_SL_ATT0 | 0x40013B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX204_SL_ATT1 | 0x40013B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX204_SL_ATT2 | 0x40013B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX204_SL_ATT3 | 0x40013B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX204_MS_ADDR | 0x40013B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX204_MS_SIZE | 0x40013B24 | FULL | Master region, size |
| PERI_MS_PPU_FX204_MS_ATT0 | 0x40013B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX204_MS_ATT1 | 0x40013B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX204_MS_ATT2 | 0x40013B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX204_MS_ATT3 | 0x40013B3C | FULL | Master attributes 3 |

21.222 PPU_FX 205

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX205_SL_ADDR | 0x40013B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX205_SL_SIZE | 0x40013B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX205_SL_ATT0 | 0x40013B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX205_SL_ATT1 | 0x40013B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX205_SL_ATT2 | 0x40013B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX205_SL_ATT3 | 0x40013B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX205_MS_ADDR | 0x40013B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX205_MS_SIZE | 0x40013B64 | FULL | Master region, size |
| PERI_MS_PPU_FX205_MS_ATT0 | 0x40013B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX205_MS_ATT1 | 0x40013B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX205_MS_ATT2 | 0x40013B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX205_MS_ATT3 | 0x40013B7C | FULL | Master attributes 3 |

21.223 PPU_FX 206

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX206_SL_ADDR | 0x40013B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX206_SL_SIZE | 0x40013B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX206_SL_ATT0 | 0x40013B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX206_SL_ATT1 | 0x40013B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX206_SL_ATT2 | 0x40013B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX206_SL_ATT3 | 0x40013B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX206_MS_ADDR | 0x40013BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX206_MS_SIZE | 0x40013BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX206_MS_ATT0 | 0x40013BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX206_MS_ATT1 | 0x40013BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX206_MS_ATT2 | 0x40013BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX206_MS_ATT3 | 0x40013BBC | FULL | Master attributes 3 |

21.224 PPU_FX 207

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX207_SL_ADDR | 0x40013BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX207_SL_SIZE | 0x40013BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX207_SL_ATT0 | 0x40013BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX207_SL_ATT1 | 0x40013BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX207_SL_ATT2 | 0x40013BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX207_SL_ATT3 | 0x40013BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX207_MS_ADDR | 0x40013BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX207_MS_SIZE | 0x40013BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX207_MS_ATT0 | 0x40013BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX207_MS_ATT1 | 0x40013BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX207_MS_ATT2 | 0x40013BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX207_MS_ATT3 | 0x40013BFC | FULL | Master attributes 3 |

21.225 PPU_FX 208

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX208_SL_ADDR | 0x40013C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX208_SL_SIZE | 0x40013C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX208_SL_ATT0 | 0x40013C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX208_SL_ATT1 | 0x40013C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX208_SL_ATT2 | 0x40013C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX208_SL_ATT3 | 0x40013C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX208_MS_ADDR | 0x40013C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX208_MS_SIZE | 0x40013C24 | FULL | Master region, size |
| PERI_MS_PPU_FX208_MS_ATT0 | 0x40013C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX208_MS_ATT1 | 0x40013C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX208_MS_ATT2 | 0x40013C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX208_MS_ATT3 | 0x40013C3C | FULL | Master attributes 3 |

21.226 PPU_FX 209

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX209_SL_ADDR | 0x40013C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX209_SL_SIZE | 0x40013C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX209_SL_ATT0 | 0x40013C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX209_SL_ATT1 | 0x40013C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX209_SL_ATT2 | 0x40013C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX209_SL_ATT3 | 0x40013C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX209_MS_ADDR | 0x40013C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX209_MS_SIZE | 0x40013C64 | FULL | Master region, size |
| PERI_MS_PPU_FX209_MS_ATT0 | 0x40013C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX209_MS_ATT1 | 0x40013C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX209_MS_ATT2 | 0x40013C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX209_MS_ATT3 | 0x40013C7C | FULL | Master attributes 3 |

21.227 PPU_FX 210

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX210_SL_ADDR | 0x40013C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX210_SL_SIZE | 0x40013C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX210_SL_ATT0 | 0x40013C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX210_SL_ATT1 | 0x40013C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX210_SL_ATT2 | 0x40013C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX210_SL_ATT3 | 0x40013C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX210_MS_ADDR | 0x40013CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX210_MS_SIZE | 0x40013CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX210_MS_ATT0 | 0x40013CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX210_MS_ATT1 | 0x40013CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX210_MS_ATT2 | 0x40013CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX210_MS_ATT3 | 0x40013CBC | FULL | Master attributes 3 |

21.228 PPU_FX 211

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX211_SL_ADDR | 0x40013CC0 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX211_SL_SIZE | 0x40013CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX211_SL_ATT0 | 0x40013CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX211_SL_ATT1 | 0x40013CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX211_SL_ATT2 | 0x40013CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX211_SL_ATT3 | 0x40013CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX211_MS_ADDR | 0x40013CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX211_MS_SIZE | 0x40013CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX211_MS_ATT0 | 0x40013CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX211_MS_ATT1 | 0x40013CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX211_MS_ATT2 | 0x40013CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX211_MS_ATT3 | 0x40013CFC | FULL | Master attributes 3 |

21.229 PPU_FX 212

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX212_SL_ADDR | 0x40013D00 | READ | Slave region, base address |
| PERI_MS_PPU_FX212_SL_SIZE | 0x40013D04 | READ | Slave region, size |
| PERI_MS_PPU_FX212_SL_ATT0 | 0x40013D10 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX212_SL_ATT1 | 0x40013D14 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX212_SL_ATT2 | 0x40013D18 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX212_SL_ATT3 | 0x40013D1C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX212_MS_ADDR | 0x40013D20 | READ | Master region, base address |
| PERI_MS_PPU_FX212_MS_SIZE | 0x40013D24 | READ | Master region, size |
| PERI_MS_PPU_FX212_MS_ATT0 | 0x40013D30 | READ | Master attributes 0 |
| PERI_MS_PPU_FX212_MS_ATT1 | 0x40013D34 | READ | Master attributes 1 |
| PERI_MS_PPU_FX212_MS_ATT2 | 0x40013D38 | READ | Master attributes 2 |
| PERI_MS_PPU_FX212_MS_ATT3 | 0x40013D3C | READ | Master attributes 3 |

21.230 PPU_FX 213

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX213_SL_ADDR | 0x40013D40 | READ | Slave region, base address |
| PERI_MS_PPU_FX213_SL_SIZE | 0x40013D44 | READ | Slave region, size |
| PERI_MS_PPU_FX213_SL_ATT0 | 0x40013D50 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX213_SL_ATT1 | 0x40013D54 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX213_SL_ATT2 | 0x40013D58 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX213_SL_ATT3 | 0x40013D5C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX213_MS_ADDR | 0x40013D60 | READ | Master region, base address |
| PERI_MS_PPU_FX213_MS_SIZE | 0x40013D64 | READ | Master region, size |
| PERI_MS_PPU_FX213_MS_ATT0 | 0x40013D70 | READ | Master attributes 0 |
| PERI_MS_PPU_FX213_MS_ATT1 | 0x40013D74 | READ | Master attributes 1 |
| PERI_MS_PPU_FX213_MS_ATT2 | 0x40013D78 | READ | Master attributes 2 |
| PERI_MS_PPU_FX213_MS_ATT3 | 0x40013D7C | READ | Master attributes 3 |

21.231 PPU_FX 214

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX214_SL_ADDR | 0x40013D80 | READ | Slave region, base address |
| PERI_MS_PPU_FX214_SL_SIZE | 0x40013D84 | READ | Slave region, size |
| PERI_MS_PPU_FX214_SL_ATT0 | 0x40013D90 | READ | Slave attributes 0 |
| PERI_MS_PPU_FX214_SL_ATT1 | 0x40013D94 | READ | Slave attributes 1 |
| PERI_MS_PPU_FX214_SL_ATT2 | 0x40013D98 | READ | Slave attributes 2 |
| PERI_MS_PPU_FX214_SL_ATT3 | 0x40013D9C | READ | Slave attributes 3 |
| PERI_MS_PPU_FX214_MS_ADDR | 0x40013DA0 | READ | Master region, base address |
| PERI_MS_PPU_FX214_MS_SIZE | 0x40013DA4 | READ | Master region, size |
| PERI_MS_PPU_FX214_MS_ATT0 | 0x40013DB0 | READ | Master attributes 0 |
| PERI_MS_PPU_FX214_MS_ATT1 | 0x40013DB4 | READ | Master attributes 1 |
| PERI_MS_PPU_FX214_MS_ATT2 | 0x40013DB8 | READ | Master attributes 2 |
| PERI_MS_PPU_FX214_MS_ATT3 | 0x40013DBC | READ | Master attributes 3 |

21.232 PPU_FX 215

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX215_SL_ADDR | 0x40013DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX215_SL_SIZE | 0x40013DC4 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX215_SL_ATT0 | 0x40013DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX215_SL_ATT1 | 0x40013DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX215_SL_ATT2 | 0x40013DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX215_SL_ATT3 | 0x40013DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX215_MS_ADDR | 0x40013DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX215_MS_SIZE | 0x40013DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX215_MS_ATT0 | 0x40013DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX215_MS_ATT1 | 0x40013DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX215_MS_ATT2 | 0x40013DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX215_MS_ATT3 | 0x40013DFC | FULL | Master attributes 3 |

21.233 PPU_FX 216

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX216_SL_ADDR | 0x40013E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX216_SL_SIZE | 0x40013E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX216_SL_ATT0 | 0x40013E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX216_SL_ATT1 | 0x40013E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX216_SL_ATT2 | 0x40013E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX216_SL_ATT3 | 0x40013E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX216_MS_ADDR | 0x40013E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX216_MS_SIZE | 0x40013E24 | FULL | Master region, size |
| PERI_MS_PPU_FX216_MS_ATT0 | 0x40013E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX216_MS_ATT1 | 0x40013E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX216_MS_ATT2 | 0x40013E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX216_MS_ATT3 | 0x40013E3C | FULL | Master attributes 3 |

21.234 PPU_FX 217

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX217_SL_ADDR | 0x40013E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX217_SL_SIZE | 0x40013E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX217_SL_ATT0 | 0x40013E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX217_SL_ATT1 | 0x40013E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX217_SL_ATT2 | 0x40013E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX217_SL_ATT3 | 0x40013E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX217_MS_ADDR | 0x40013E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX217_MS_SIZE | 0x40013E64 | FULL | Master region, size |
| PERI_MS_PPU_FX217_MS_ATT0 | 0x40013E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX217_MS_ATT1 | 0x40013E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX217_MS_ATT2 | 0x40013E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX217_MS_ATT3 | 0x40013E7C | FULL | Master attributes 3 |

21.235 PPU_FX 218

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX218_SL_ADDR | 0x40013E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX218_SL_SIZE | 0x40013E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX218_SL_ATT0 | 0x40013E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX218_SL_ATT1 | 0x40013E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX218_SL_ATT2 | 0x40013E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX218_SL_ATT3 | 0x40013E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX218_MS_ADDR | 0x40013EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX218_MS_SIZE | 0x40013EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX218_MS_ATT0 | 0x40013EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX218_MS_ATT1 | 0x40013EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX218_MS_ATT2 | 0x40013EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX218_MS_ATT3 | 0x40013EBC | FULL | Master attributes 3 |

21.236 PPU_FX 219

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX219_SL_ADDR | 0x40013EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX219_SL_SIZE | 0x40013EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX219_SL_ATT0 | 0x40013ED0 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX219_SL_ATT1 | 0x40013ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX219_SL_ATT2 | 0x40013ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX219_SL_ATT3 | 0x40013EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX219_MS_ADDR | 0x40013EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX219_MS_SIZE | 0x40013EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX219_MS_ATT0 | 0x40013EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX219_MS_ATT1 | 0x40013EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX219_MS_ATT2 | 0x40013EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX219_MS_ATT3 | 0x40013EFC | FULL | Master attributes 3 |

21.237 PPU_FX 220

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX220_SL_ADDR | 0x40013F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX220_SL_SIZE | 0x40013F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX220_SL_ATT0 | 0x40013F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX220_SL_ATT1 | 0x40013F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX220_SL_ATT2 | 0x40013F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX220_SL_ATT3 | 0x40013F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX220_MS_ADDR | 0x40013F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX220_MS_SIZE | 0x40013F24 | FULL | Master region, size |
| PERI_MS_PPU_FX220_MS_ATT0 | 0x40013F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX220_MS_ATT1 | 0x40013F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX220_MS_ATT2 | 0x40013F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX220_MS_ATT3 | 0x40013F3C | FULL | Master attributes 3 |

21.238 PPU_FX 221

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX221_SL_ADDR | 0x40013F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX221_SL_SIZE | 0x40013F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX221_SL_ATT0 | 0x40013F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX221_SL_ATT1 | 0x40013F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX221_SL_ATT2 | 0x40013F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX221_SL_ATT3 | 0x40013F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX221_MS_ADDR | 0x40013F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX221_MS_SIZE | 0x40013F64 | FULL | Master region, size |
| PERI_MS_PPU_FX221_MS_ATT0 | 0x40013F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX221_MS_ATT1 | 0x40013F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX221_MS_ATT2 | 0x40013F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX221_MS_ATT3 | 0x40013F7C | FULL | Master attributes 3 |

21.239 PPU_FX 222

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX222_SL_ADDR | 0x40013F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX222_SL_SIZE | 0x40013F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX222_SL_ATT0 | 0x40013F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX222_SL_ATT1 | 0x40013F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX222_SL_ATT2 | 0x40013F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX222_SL_ATT3 | 0x40013F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX222_MS_ADDR | 0x40013FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX222_MS_SIZE | 0x40013FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX222_MS_ATT0 | 0x40013FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX222_MS_ATT1 | 0x40013FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX222_MS_ATT2 | 0x40013FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX222_MS_ATT3 | 0x40013FBC | FULL | Master attributes 3 |

21.240 PPU_FX 223

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX223_SL_ADDR | 0x40013FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX223_SL_SIZE | 0x40013FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX223_SL_ATT0 | 0x40013FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX223_SL_ATT1 | 0x40013FD4 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX223_SL_ATT2 | 0x40013FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX223_SL_ATT3 | 0x40013FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX223_MS_ADDR | 0x40013FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX223_MS_SIZE | 0x40013FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX223_MS_ATT0 | 0x40013FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX223_MS_ATT1 | 0x40013FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX223_MS_ATT2 | 0x40013FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX223_MS_ATT3 | 0x40013FFC | FULL | Master attributes 3 |

21.241 PPU_FX 224

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX224_SL_ADDR | 0x40014000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX224_SL_SIZE | 0x40014004 | FULL | Slave region, size |
| PERI_MS_PPU_FX224_SL_ATT0 | 0x40014010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX224_SL_ATT1 | 0x40014014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX224_SL_ATT2 | 0x40014018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX224_SL_ATT3 | 0x4001401C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX224_MS_ADDR | 0x40014020 | FULL | Master region, base address |
| PERI_MS_PPU_FX224_MS_SIZE | 0x40014024 | FULL | Master region, size |
| PERI_MS_PPU_FX224_MS_ATT0 | 0x40014030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX224_MS_ATT1 | 0x40014034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX224_MS_ATT2 | 0x40014038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX224_MS_ATT3 | 0x4001403C | FULL | Master attributes 3 |

21.242 PPU_FX 225

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX225_SL_ADDR | 0x40014040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX225_SL_SIZE | 0x40014044 | FULL | Slave region, size |
| PERI_MS_PPU_FX225_SL_ATT0 | 0x40014050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX225_SL_ATT1 | 0x40014054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX225_SL_ATT2 | 0x40014058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX225_SL_ATT3 | 0x4001405C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX225_MS_ADDR | 0x40014060 | FULL | Master region, base address |
| PERI_MS_PPU_FX225_MS_SIZE | 0x40014064 | FULL | Master region, size |
| PERI_MS_PPU_FX225_MS_ATT0 | 0x40014070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX225_MS_ATT1 | 0x40014074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX225_MS_ATT2 | 0x40014078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX225_MS_ATT3 | 0x4001407C | FULL | Master attributes 3 |

21.243 PPU_FX 226

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX226_SL_ADDR | 0x40014080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX226_SL_SIZE | 0x40014084 | FULL | Slave region, size |
| PERI_MS_PPU_FX226_SL_ATT0 | 0x40014090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX226_SL_ATT1 | 0x40014094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX226_SL_ATT2 | 0x40014098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX226_SL_ATT3 | 0x4001409C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX226_MS_ADDR | 0x400140A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX226_MS_SIZE | 0x400140A4 | FULL | Master region, size |
| PERI_MS_PPU_FX226_MS_ATT0 | 0x400140B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX226_MS_ATT1 | 0x400140B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX226_MS_ATT2 | 0x400140B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX226_MS_ATT3 | 0x400140BC | FULL | Master attributes 3 |

21.244 PPU_FX 227

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX227_SL_ADDR | 0x400140C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX227_SL_SIZE | 0x400140C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX227_SL_ATT0 | 0x400140D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX227_SL_ATT1 | 0x400140D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX227_SL_ATT2 | 0x400140D8 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX227_SL_ATT3 | 0x400140DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX227_MS_ADDR | 0x400140E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX227_MS_SIZE | 0x400140E4 | FULL | Master region, size |
| PERI_MS_PPU_FX227_MS_ATT0 | 0x400140F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX227_MS_ATT1 | 0x400140F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX227_MS_ATT2 | 0x400140F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX227_MS_ATT3 | 0x400140FC | FULL | Master attributes 3 |

21.245 PPU_FX 228

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX228_SL_ADDR | 0x40014100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX228_SL_SIZE | 0x40014104 | FULL | Slave region, size |
| PERI_MS_PPU_FX228_SL_ATT0 | 0x40014110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX228_SL_ATT1 | 0x40014114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX228_SL_ATT2 | 0x40014118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX228_SL_ATT3 | 0x4001411C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX228_MS_ADDR | 0x40014120 | FULL | Master region, base address |
| PERI_MS_PPU_FX228_MS_SIZE | 0x40014124 | FULL | Master region, size |
| PERI_MS_PPU_FX228_MS_ATT0 | 0x40014130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX228_MS_ATT1 | 0x40014134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX228_MS_ATT2 | 0x40014138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX228_MS_ATT3 | 0x4001413C | FULL | Master attributes 3 |

21.246 PPU_FX 229

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX229_SL_ADDR | 0x40014140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX229_SL_SIZE | 0x40014144 | FULL | Slave region, size |
| PERI_MS_PPU_FX229_SL_ATT0 | 0x40014150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX229_SL_ATT1 | 0x40014154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX229_SL_ATT2 | 0x40014158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX229_SL_ATT3 | 0x4001415C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX229_MS_ADDR | 0x40014160 | FULL | Master region, base address |
| PERI_MS_PPU_FX229_MS_SIZE | 0x40014164 | FULL | Master region, size |
| PERI_MS_PPU_FX229_MS_ATT0 | 0x40014170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX229_MS_ATT1 | 0x40014174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX229_MS_ATT2 | 0x40014178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX229_MS_ATT3 | 0x4001417C | FULL | Master attributes 3 |

21.247 PPU_FX 230

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX230_SL_ADDR | 0x40014180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX230_SL_SIZE | 0x40014184 | FULL | Slave region, size |
| PERI_MS_PPU_FX230_SL_ATT0 | 0x40014190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX230_SL_ATT1 | 0x40014194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX230_SL_ATT2 | 0x40014198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX230_SL_ATT3 | 0x4001419C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX230_MS_ADDR | 0x400141A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX230_MS_SIZE | 0x400141A4 | FULL | Master region, size |
| PERI_MS_PPU_FX230_MS_ATT0 | 0x400141B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX230_MS_ATT1 | 0x400141B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX230_MS_ATT2 | 0x400141B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX230_MS_ATT3 | 0x400141BC | FULL | Master attributes 3 |

21.248 PPU_FX 231

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX231_SL_ADDR | 0x400141C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX231_SL_SIZE | 0x400141C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX231_SL_ATT0 | 0x400141D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX231_SL_ATT1 | 0x400141D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX231_SL_ATT2 | 0x400141D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX231_SL_ATT3 | 0x400141DC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX231_MS_ADDR | 0x400141E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX231_MS_SIZE | 0x400141E4 | FULL | Master region, size |
| PERI_MS_PPU_FX231_MS_ATT0 | 0x400141F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX231_MS_ATT1 | 0x400141F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX231_MS_ATT2 | 0x400141F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX231_MS_ATT3 | 0x400141FC | FULL | Master attributes 3 |

21.249 PPU_FX 232

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX232_SL_ADDR | 0x40014200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX232_SL_SIZE | 0x40014204 | FULL | Slave region, size |
| PERI_MS_PPU_FX232_SL_ATT0 | 0x40014210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX232_SL_ATT1 | 0x40014214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX232_SL_ATT2 | 0x40014218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX232_SL_ATT3 | 0x4001421C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX232_MS_ADDR | 0x40014220 | FULL | Master region, base address |
| PERI_MS_PPU_FX232_MS_SIZE | 0x40014224 | FULL | Master region, size |
| PERI_MS_PPU_FX232_MS_ATT0 | 0x40014230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX232_MS_ATT1 | 0x40014234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX232_MS_ATT2 | 0x40014238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX232_MS_ATT3 | 0x4001423C | FULL | Master attributes 3 |

21.250 PPU_FX 233

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX233_SL_ADDR | 0x40014240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX233_SL_SIZE | 0x40014244 | FULL | Slave region, size |
| PERI_MS_PPU_FX233_SL_ATT0 | 0x40014250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX233_SL_ATT1 | 0x40014254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX233_SL_ATT2 | 0x40014258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX233_SL_ATT3 | 0x4001425C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX233_MS_ADDR | 0x40014260 | FULL | Master region, base address |
| PERI_MS_PPU_FX233_MS_SIZE | 0x40014264 | FULL | Master region, size |
| PERI_MS_PPU_FX233_MS_ATT0 | 0x40014270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX233_MS_ATT1 | 0x40014274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX233_MS_ATT2 | 0x40014278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX233_MS_ATT3 | 0x4001427C | FULL | Master attributes 3 |

21.251 PPU_FX 234

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX234_SL_ADDR | 0x40014280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX234_SL_SIZE | 0x40014284 | FULL | Slave region, size |
| PERI_MS_PPU_FX234_SL_ATT0 | 0x40014290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX234_SL_ATT1 | 0x40014294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX234_SL_ATT2 | 0x40014298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX234_SL_ATT3 | 0x4001429C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX234_MS_ADDR | 0x400142A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX234_MS_SIZE | 0x400142A4 | FULL | Master region, size |
| PERI_MS_PPU_FX234_MS_ATT0 | 0x400142B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX234_MS_ATT1 | 0x400142B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX234_MS_ATT2 | 0x400142B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX234_MS_ATT3 | 0x400142BC | FULL | Master attributes 3 |

21.252 PPU_FX 235

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX235_SL_ADDR | 0x400142C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX235_SL_SIZE | 0x400142C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX235_SL_ATT0 | 0x400142D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX235_SL_ATT1 | 0x400142D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX235_SL_ATT2 | 0x400142D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX235_SL_ATT3 | 0x400142DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX235_MS_ADDR | 0x400142E0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX235_MS_SIZE | 0x400142E4 | FULL | Master region, size |
| PERI_MS_PPU_FX235_MS_ATT0 | 0x400142F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX235_MS_ATT1 | 0x400142F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX235_MS_ATT2 | 0x400142F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX235_MS_ATT3 | 0x400142FC | FULL | Master attributes 3 |

21.253 PPU_FX 236

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX236_SL_ADDR | 0x40014300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX236_SL_SIZE | 0x40014304 | FULL | Slave region, size |
| PERI_MS_PPU_FX236_SL_ATT0 | 0x40014310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX236_SL_ATT1 | 0x40014314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX236_SL_ATT2 | 0x40014318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX236_SL_ATT3 | 0x4001431C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX236_MS_ADDR | 0x40014320 | FULL | Master region, base address |
| PERI_MS_PPU_FX236_MS_SIZE | 0x40014324 | FULL | Master region, size |
| PERI_MS_PPU_FX236_MS_ATT0 | 0x40014330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX236_MS_ATT1 | 0x40014334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX236_MS_ATT2 | 0x40014338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX236_MS_ATT3 | 0x4001433C | FULL | Master attributes 3 |

21.254 PPU_FX 237

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX237_SL_ADDR | 0x40014340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX237_SL_SIZE | 0x40014344 | FULL | Slave region, size |
| PERI_MS_PPU_FX237_SL_ATT0 | 0x40014350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX237_SL_ATT1 | 0x40014354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX237_SL_ATT2 | 0x40014358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX237_SL_ATT3 | 0x4001435C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX237_MS_ADDR | 0x40014360 | FULL | Master region, base address |
| PERI_MS_PPU_FX237_MS_SIZE | 0x40014364 | FULL | Master region, size |
| PERI_MS_PPU_FX237_MS_ATT0 | 0x40014370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX237_MS_ATT1 | 0x40014374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX237_MS_ATT2 | 0x40014378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX237_MS_ATT3 | 0x4001437C | FULL | Master attributes 3 |

21.255 PPU_FX 238

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX238_SL_ADDR | 0x40014380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX238_SL_SIZE | 0x40014384 | FULL | Slave region, size |
| PERI_MS_PPU_FX238_SL_ATT0 | 0x40014390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX238_SL_ATT1 | 0x40014394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX238_SL_ATT2 | 0x40014398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX238_SL_ATT3 | 0x4001439C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX238_MS_ADDR | 0x400143A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX238_MS_SIZE | 0x400143A4 | FULL | Master region, size |
| PERI_MS_PPU_FX238_MS_ATT0 | 0x400143B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX238_MS_ATT1 | 0x400143B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX238_MS_ATT2 | 0x400143B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX238_MS_ATT3 | 0x400143BC | FULL | Master attributes 3 |

21.256 PPU_FX 239

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX239_SL_ADDR | 0x400143C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX239_SL_SIZE | 0x400143C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX239_SL_ATT0 | 0x400143D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX239_SL_ATT1 | 0x400143D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX239_SL_ATT2 | 0x400143D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX239_SL_ATT3 | 0x400143DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX239_MS_ADDR | 0x400143E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX239_MS_SIZE | 0x400143E4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX239_MS_ATT0 | 0x400143F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX239_MS_ATT1 | 0x400143F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX239_MS_ATT2 | 0x400143F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX239_MS_ATT3 | 0x400143FC | FULL | Master attributes 3 |

21.257 PPU_FX 240

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX240_SL_ADDR | 0x40014400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX240_SL_SIZE | 0x40014404 | FULL | Slave region, size |
| PERI_MS_PPU_FX240_SL_ATT0 | 0x40014410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX240_SL_ATT1 | 0x40014414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX240_SL_ATT2 | 0x40014418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX240_SL_ATT3 | 0x4001441C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX240_MS_ADDR | 0x40014420 | FULL | Master region, base address |
| PERI_MS_PPU_FX240_MS_SIZE | 0x40014424 | FULL | Master region, size |
| PERI_MS_PPU_FX240_MS_ATT0 | 0x40014430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX240_MS_ATT1 | 0x40014434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX240_MS_ATT2 | 0x40014438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX240_MS_ATT3 | 0x4001443C | FULL | Master attributes 3 |

21.258 PPU_FX 241

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX241_SL_ADDR | 0x40014440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX241_SL_SIZE | 0x40014444 | FULL | Slave region, size |
| PERI_MS_PPU_FX241_SL_ATT0 | 0x40014450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX241_SL_ATT1 | 0x40014454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX241_SL_ATT2 | 0x40014458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX241_SL_ATT3 | 0x4001445C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX241_MS_ADDR | 0x40014460 | FULL | Master region, base address |
| PERI_MS_PPU_FX241_MS_SIZE | 0x40014464 | FULL | Master region, size |
| PERI_MS_PPU_FX241_MS_ATT0 | 0x40014470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX241_MS_ATT1 | 0x40014474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX241_MS_ATT2 | 0x40014478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX241_MS_ATT3 | 0x4001447C | FULL | Master attributes 3 |

21.259 PPU_FX 242

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX242_SL_ADDR | 0x40014480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX242_SL_SIZE | 0x40014484 | FULL | Slave region, size |
| PERI_MS_PPU_FX242_SL_ATT0 | 0x40014490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX242_SL_ATT1 | 0x40014494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX242_SL_ATT2 | 0x40014498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX242_SL_ATT3 | 0x4001449C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX242_MS_ADDR | 0x400144A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX242_MS_SIZE | 0x400144A4 | FULL | Master region, size |
| PERI_MS_PPU_FX242_MS_ATT0 | 0x400144B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX242_MS_ATT1 | 0x400144B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX242_MS_ATT2 | 0x400144B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX242_MS_ATT3 | 0x400144BC | FULL | Master attributes 3 |

21.260 PPU_FX 243

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX243_SL_ADDR | 0x400144C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX243_SL_SIZE | 0x400144C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX243_SL_ATT0 | 0x400144D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX243_SL_ATT1 | 0x400144D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX243_SL_ATT2 | 0x400144D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX243_SL_ATT3 | 0x400144DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX243_MS_ADDR | 0x400144E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX243_MS_SIZE | 0x400144E4 | FULL | Master region, size |
| PERI_MS_PPU_FX243_MS_ATT0 | 0x400144F0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX243_MS_ATT1 | 0x400144F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX243_MS_ATT2 | 0x400144F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX243_MS_ATT3 | 0x400144FC | FULL | Master attributes 3 |

21.261 PPU_FX 244

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX244_SL_ADDR | 0x40014500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX244_SL_SIZE | 0x40014504 | FULL | Slave region, size |
| PERI_MS_PPU_FX244_SL_ATT0 | 0x40014510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX244_SL_ATT1 | 0x40014514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX244_SL_ATT2 | 0x40014518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX244_SL_ATT3 | 0x4001451C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX244_MS_ADDR | 0x40014520 | FULL | Master region, base address |
| PERI_MS_PPU_FX244_MS_SIZE | 0x40014524 | FULL | Master region, size |
| PERI_MS_PPU_FX244_MS_ATT0 | 0x40014530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX244_MS_ATT1 | 0x40014534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX244_MS_ATT2 | 0x40014538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX244_MS_ATT3 | 0x4001453C | FULL | Master attributes 3 |

21.262 PPU_FX 245

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX245_SL_ADDR | 0x40014540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX245_SL_SIZE | 0x40014544 | FULL | Slave region, size |
| PERI_MS_PPU_FX245_SL_ATT0 | 0x40014550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX245_SL_ATT1 | 0x40014554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX245_SL_ATT2 | 0x40014558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX245_SL_ATT3 | 0x4001455C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX245_MS_ADDR | 0x40014560 | FULL | Master region, base address |
| PERI_MS_PPU_FX245_MS_SIZE | 0x40014564 | FULL | Master region, size |
| PERI_MS_PPU_FX245_MS_ATT0 | 0x40014570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX245_MS_ATT1 | 0x40014574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX245_MS_ATT2 | 0x40014578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX245_MS_ATT3 | 0x4001457C | FULL | Master attributes 3 |

21.263 PPU_FX 246

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX246_SL_ADDR | 0x40014580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX246_SL_SIZE | 0x40014584 | FULL | Slave region, size |
| PERI_MS_PPU_FX246_SL_ATT0 | 0x40014590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX246_SL_ATT1 | 0x40014594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX246_SL_ATT2 | 0x40014598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX246_SL_ATT3 | 0x4001459C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX246_MS_ADDR | 0x400145A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX246_MS_SIZE | 0x400145A4 | FULL | Master region, size |
| PERI_MS_PPU_FX246_MS_ATT0 | 0x400145B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX246_MS_ATT1 | 0x400145B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX246_MS_ATT2 | 0x400145B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX246_MS_ATT3 | 0x400145BC | FULL | Master attributes 3 |

21.264 PPU_FX 247

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX247_SL_ADDR | 0x400145C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX247_SL_SIZE | 0x400145C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX247_SL_ATT0 | 0x400145D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX247_SL_ATT1 | 0x400145D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX247_SL_ATT2 | 0x400145D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX247_SL_ATT3 | 0x400145DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX247_MS_ADDR | 0x400145E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX247_MS_SIZE | 0x400145E4 | FULL | Master region, size |
| PERI_MS_PPU_FX247_MS_ATT0 | 0x400145F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX247_MS_ATT1 | 0x400145F4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX247_MS_ATT2 | 0x400145F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX247_MS_ATT3 | 0x400145FC | FULL | Master attributes 3 |

21.265 PPU_FX 248

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX248_SL_ADDR | 0x40014600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX248_SL_SIZE | 0x40014604 | FULL | Slave region, size |
| PERI_MS_PPU_FX248_SL_ATT0 | 0x40014610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX248_SL_ATT1 | 0x40014614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX248_SL_ATT2 | 0x40014618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX248_SL_ATT3 | 0x4001461C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX248_MS_ADDR | 0x40014620 | FULL | Master region, base address |
| PERI_MS_PPU_FX248_MS_SIZE | 0x40014624 | FULL | Master region, size |
| PERI_MS_PPU_FX248_MS_ATT0 | 0x40014630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX248_MS_ATT1 | 0x40014634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX248_MS_ATT2 | 0x40014638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX248_MS_ATT3 | 0x4001463C | FULL | Master attributes 3 |

21.266 PPU_FX 249

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX249_SL_ADDR | 0x40014640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX249_SL_SIZE | 0x40014644 | FULL | Slave region, size |
| PERI_MS_PPU_FX249_SL_ATT0 | 0x40014650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX249_SL_ATT1 | 0x40014654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX249_SL_ATT2 | 0x40014658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX249_SL_ATT3 | 0x4001465C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX249_MS_ADDR | 0x40014660 | FULL | Master region, base address |
| PERI_MS_PPU_FX249_MS_SIZE | 0x40014664 | FULL | Master region, size |
| PERI_MS_PPU_FX249_MS_ATT0 | 0x40014670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX249_MS_ATT1 | 0x40014674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX249_MS_ATT2 | 0x40014678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX249_MS_ATT3 | 0x4001467C | FULL | Master attributes 3 |

21.267 PPU_FX 250

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX250_SL_ADDR | 0x40014680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX250_SL_SIZE | 0x40014684 | FULL | Slave region, size |
| PERI_MS_PPU_FX250_SL_ATT0 | 0x40014690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX250_SL_ATT1 | 0x40014694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX250_SL_ATT2 | 0x40014698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX250_SL_ATT3 | 0x4001469C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX250_MS_ADDR | 0x400146A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX250_MS_SIZE | 0x400146A4 | FULL | Master region, size |
| PERI_MS_PPU_FX250_MS_ATT0 | 0x400146B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX250_MS_ATT1 | 0x400146B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX250_MS_ATT2 | 0x400146B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX250_MS_ATT3 | 0x400146BC | FULL | Master attributes 3 |

21.268 PPU_FX 251

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX251_SL_ADDR | 0x400146C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX251_SL_SIZE | 0x400146C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX251_SL_ATT0 | 0x400146D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX251_SL_ATT1 | 0x400146D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX251_SL_ATT2 | 0x400146D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX251_SL_ATT3 | 0x400146DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX251_MS_ADDR | 0x400146E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX251_MS_SIZE | 0x400146E4 | FULL | Master region, size |
| PERI_MS_PPU_FX251_MS_ATT0 | 0x400146F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX251_MS_ATT1 | 0x400146F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX251_MS_ATT2 | 0x400146F8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX251_MS_ATT3 | 0x400146FC | FULL | Master attributes 3 |

21.269 PPU_FX 252

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX252_SL_ADDR | 0x40014700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX252_SL_SIZE | 0x40014704 | FULL | Slave region, size |
| PERI_MS_PPU_FX252_SL_ATT0 | 0x40014710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX252_SL_ATT1 | 0x40014714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX252_SL_ATT2 | 0x40014718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX252_SL_ATT3 | 0x4001471C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX252_MS_ADDR | 0x40014720 | FULL | Master region, base address |
| PERI_MS_PPU_FX252_MS_SIZE | 0x40014724 | FULL | Master region, size |
| PERI_MS_PPU_FX252_MS_ATT0 | 0x40014730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX252_MS_ATT1 | 0x40014734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX252_MS_ATT2 | 0x40014738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX252_MS_ATT3 | 0x4001473C | FULL | Master attributes 3 |

21.270 PPU_FX 253

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX253_SL_ADDR | 0x40014740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX253_SL_SIZE | 0x40014744 | FULL | Slave region, size |
| PERI_MS_PPU_FX253_SL_ATT0 | 0x40014750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX253_SL_ATT1 | 0x40014754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX253_SL_ATT2 | 0x40014758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX253_SL_ATT3 | 0x4001475C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX253_MS_ADDR | 0x40014760 | FULL | Master region, base address |
| PERI_MS_PPU_FX253_MS_SIZE | 0x40014764 | FULL | Master region, size |
| PERI_MS_PPU_FX253_MS_ATT0 | 0x40014770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX253_MS_ATT1 | 0x40014774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX253_MS_ATT2 | 0x40014778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX253_MS_ATT3 | 0x4001477C | FULL | Master attributes 3 |

21.271 PPU_FX 254

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX254_SL_ADDR | 0x40014780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX254_SL_SIZE | 0x40014784 | FULL | Slave region, size |
| PERI_MS_PPU_FX254_SL_ATT0 | 0x40014790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX254_SL_ATT1 | 0x40014794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX254_SL_ATT2 | 0x40014798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX254_SL_ATT3 | 0x4001479C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX254_MS_ADDR | 0x400147A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX254_MS_SIZE | 0x400147A4 | FULL | Master region, size |
| PERI_MS_PPU_FX254_MS_ATT0 | 0x400147B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX254_MS_ATT1 | 0x400147B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX254_MS_ATT2 | 0x400147B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX254_MS_ATT3 | 0x400147BC | FULL | Master attributes 3 |

21.272 PPU_FX 255

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX255_SL_ADDR | 0x400147C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX255_SL_SIZE | 0x400147C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX255_SL_ATT0 | 0x400147D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX255_SL_ATT1 | 0x400147D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX255_SL_ATT2 | 0x400147D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX255_SL_ATT3 | 0x400147DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX255_MS_ADDR | 0x400147E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX255_MS_SIZE | 0x400147E4 | FULL | Master region, size |
| PERI_MS_PPU_FX255_MS_ATT0 | 0x400147F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX255_MS_ATT1 | 0x400147F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX255_MS_ATT2 | 0x400147F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX255_MS_ATT3 | 0x400147FC | FULL | Master attributes 3 |

21.273 PPU_FX 256

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX256_SL_ADDR | 0x40014800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX256_SL_SIZE | 0x40014804 | FULL | Slave region, size |
| PERI_MS_PPU_FX256_SL_ATT0 | 0x40014810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX256_SL_ATT1 | 0x40014814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX256_SL_ATT2 | 0x40014818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX256_SL_ATT3 | 0x4001481C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX256_MS_ADDR | 0x40014820 | FULL | Master region, base address |
| PERI_MS_PPU_FX256_MS_SIZE | 0x40014824 | FULL | Master region, size |
| PERI_MS_PPU_FX256_MS_ATT0 | 0x40014830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX256_MS_ATT1 | 0x40014834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX256_MS_ATT2 | 0x40014838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX256_MS_ATT3 | 0x4001483C | FULL | Master attributes 3 |

21.274 PPU_FX 257

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX257_SL_ADDR | 0x40014840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX257_SL_SIZE | 0x40014844 | FULL | Slave region, size |
| PERI_MS_PPU_FX257_SL_ATT0 | 0x40014850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX257_SL_ATT1 | 0x40014854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX257_SL_ATT2 | 0x40014858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX257_SL_ATT3 | 0x4001485C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX257_MS_ADDR | 0x40014860 | FULL | Master region, base address |
| PERI_MS_PPU_FX257_MS_SIZE | 0x40014864 | FULL | Master region, size |
| PERI_MS_PPU_FX257_MS_ATT0 | 0x40014870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX257_MS_ATT1 | 0x40014874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX257_MS_ATT2 | 0x40014878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX257_MS_ATT3 | 0x4001487C | FULL | Master attributes 3 |

21.275 PPU_FX 258

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX258_SL_ADDR | 0x40014880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX258_SL_SIZE | 0x40014884 | FULL | Slave region, size |
| PERI_MS_PPU_FX258_SL_ATT0 | 0x40014890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX258_SL_ATT1 | 0x40014894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX258_SL_ATT2 | 0x40014898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX258_SL_ATT3 | 0x4001489C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX258_MS_ADDR | 0x400148A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX258_MS_SIZE | 0x400148A4 | FULL | Master region, size |
| PERI_MS_PPU_FX258_MS_ATT0 | 0x400148B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX258_MS_ATT1 | 0x400148B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX258_MS_ATT2 | 0x400148B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX258_MS_ATT3 | 0x400148BC | FULL | Master attributes 3 |

21.276 PPU_FX 259

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX259_SL_ADDR | 0x400148C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX259_SL_SIZE | 0x400148C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX259_SL_ATT0 | 0x400148D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX259_SL_ATT1 | 0x400148D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX259_SL_ATT2 | 0x400148D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX259_SL_ATT3 | 0x400148DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX259_MS_ADDR | 0x400148E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX259_MS_SIZE | 0x400148E4 | FULL | Master region, size |
| PERI_MS_PPU_FX259_MS_ATT0 | 0x400148F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX259_MS_ATT1 | 0x400148F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX259_MS_ATT2 | 0x400148F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX259_MS_ATT3 | 0x400148FC | FULL | Master attributes 3 |

21.277 PPU_FX 260

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX260_SL_ADDR | 0x40014900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX260_SL_SIZE | 0x40014904 | FULL | Slave region, size |
| PERI_MS_PPU_FX260_SL_ATT0 | 0x40014910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX260_SL_ATT1 | 0x40014914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX260_SL_ATT2 | 0x40014918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX260_SL_ATT3 | 0x4001491C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX260_MS_ADDR | 0x40014920 | FULL | Master region, base address |
| PERI_MS_PPU_FX260_MS_SIZE | 0x40014924 | FULL | Master region, size |
| PERI_MS_PPU_FX260_MS_ATT0 | 0x40014930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX260_MS_ATT1 | 0x40014934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX260_MS_ATT2 | 0x40014938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX260_MS_ATT3 | 0x4001493C | FULL | Master attributes 3 |

21.278 PPU_FX 261

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX261_SL_ADDR | 0x40014940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX261_SL_SIZE | 0x40014944 | FULL | Slave region, size |
| PERI_MS_PPU_FX261_SL_ATT0 | 0x40014950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX261_SL_ATT1 | 0x40014954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX261_SL_ATT2 | 0x40014958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX261_SL_ATT3 | 0x4001495C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX261_MS_ADDR | 0x40014960 | FULL | Master region, base address |
| PERI_MS_PPU_FX261_MS_SIZE | 0x40014964 | FULL | Master region, size |
| PERI_MS_PPU_FX261_MS_ATT0 | 0x40014970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX261_MS_ATT1 | 0x40014974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX261_MS_ATT2 | 0x40014978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX261_MS_ATT3 | 0x4001497C | FULL | Master attributes 3 |

21.279 PPU_FX 262

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX262_SL_ADDR | 0x40014980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX262_SL_SIZE | 0x40014984 | FULL | Slave region, size |
| PERI_MS_PPU_FX262_SL_ATT0 | 0x40014990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX262_SL_ATT1 | 0x40014994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX262_SL_ATT2 | 0x40014998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX262_SL_ATT3 | 0x4001499C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX262_MS_ADDR | 0x400149A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX262_MS_SIZE | 0x400149A4 | FULL | Master region, size |
| PERI_MS_PPU_FX262_MS_ATT0 | 0x400149B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX262_MS_ATT1 | 0x400149B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX262_MS_ATT2 | 0x400149B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX262_MS_ATT3 | 0x400149BC | FULL | Master attributes 3 |

21.280 PPU_FX 263

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX263_SL_ADDR | 0x400149C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX263_SL_SIZE | 0x400149C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX263_SL_ATT0 | 0x400149D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX263_SL_ATT1 | 0x400149D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX263_SL_ATT2 | 0x400149D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX263_SL_ATT3 | 0x400149DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX263_MS_ADDR | 0x400149E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX263_MS_SIZE | 0x400149E4 | FULL | Master region, size |
| PERI_MS_PPU_FX263_MS_ATT0 | 0x400149F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX263_MS_ATT1 | 0x400149F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX263_MS_ATT2 | 0x400149F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX263_MS_ATT3 | 0x400149FC | FULL | Master attributes 3 |

21.281 PPU_FX 264

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX264_SL_ADDR | 0x40014A00 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX264_SL_SIZE | 0x40014A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX264_SL_ATT0 | 0x40014A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX264_SL_ATT1 | 0x40014A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX264_SL_ATT2 | 0x40014A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX264_SL_ATT3 | 0x40014A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX264_MS_ADDR | 0x40014A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX264_MS_SIZE | 0x40014A24 | FULL | Master region, size |
| PERI_MS_PPU_FX264_MS_ATT0 | 0x40014A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX264_MS_ATT1 | 0x40014A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX264_MS_ATT2 | 0x40014A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX264_MS_ATT3 | 0x40014A3C | FULL | Master attributes 3 |

21.282 PPU_FX 265

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX265_SL_ADDR | 0x40014A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX265_SL_SIZE | 0x40014A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX265_SL_ATT0 | 0x40014A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX265_SL_ATT1 | 0x40014A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX265_SL_ATT2 | 0x40014A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX265_SL_ATT3 | 0x40014A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX265_MS_ADDR | 0x40014A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX265_MS_SIZE | 0x40014A64 | FULL | Master region, size |
| PERI_MS_PPU_FX265_MS_ATT0 | 0x40014A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX265_MS_ATT1 | 0x40014A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX265_MS_ATT2 | 0x40014A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX265_MS_ATT3 | 0x40014A7C | FULL | Master attributes 3 |

21.283 PPU_FX 266

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX266_SL_ADDR | 0x40014A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX266_SL_SIZE | 0x40014A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX266_SL_ATT0 | 0x40014A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX266_SL_ATT1 | 0x40014A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX266_SL_ATT2 | 0x40014A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX266_SL_ATT3 | 0x40014A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX266_MS_ADDR | 0x40014AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX266_MS_SIZE | 0x40014AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX266_MS_ATT0 | 0x40014AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX266_MS_ATT1 | 0x40014AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX266_MS_ATT2 | 0x40014AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX266_MS_ATT3 | 0x40014ABC | FULL | Master attributes 3 |

21.284 PPU_FX 267

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX267_SL_ADDR | 0x40014AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX267_SL_SIZE | 0x40014AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX267_SL_ATT0 | 0x40014AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX267_SL_ATT1 | 0x40014AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX267_SL_ATT2 | 0x40014AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX267_SL_ATT3 | 0x40014ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX267_MS_ADDR | 0x40014AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX267_MS_SIZE | 0x40014AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX267_MS_ATT0 | 0x40014AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX267_MS_ATT1 | 0x40014AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX267_MS_ATT2 | 0x40014AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX267_MS_ATT3 | 0x40014AFC | FULL | Master attributes 3 |

21.285 PPU_FX 268

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX268_SL_ADDR | 0x40014B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX268_SL_SIZE | 0x40014B04 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX268_SL_ATT0 | 0x40014B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX268_SL_ATT1 | 0x40014B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX268_SL_ATT2 | 0x40014B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX268_SL_ATT3 | 0x40014B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX268_MS_ADDR | 0x40014B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX268_MS_SIZE | 0x40014B24 | FULL | Master region, size |
| PERI_MS_PPU_FX268_MS_ATT0 | 0x40014B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX268_MS_ATT1 | 0x40014B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX268_MS_ATT2 | 0x40014B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX268_MS_ATT3 | 0x40014B3C | FULL | Master attributes 3 |

21.286 PPU_FX 269

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX269_SL_ADDR | 0x40014B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX269_SL_SIZE | 0x40014B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX269_SL_ATT0 | 0x40014B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX269_SL_ATT1 | 0x40014B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX269_SL_ATT2 | 0x40014B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX269_SL_ATT3 | 0x40014B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX269_MS_ADDR | 0x40014B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX269_MS_SIZE | 0x40014B64 | FULL | Master region, size |
| PERI_MS_PPU_FX269_MS_ATT0 | 0x40014B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX269_MS_ATT1 | 0x40014B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX269_MS_ATT2 | 0x40014B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX269_MS_ATT3 | 0x40014B7C | FULL | Master attributes 3 |

21.287 PPU_FX 270

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX270_SL_ADDR | 0x40014B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX270_SL_SIZE | 0x40014B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX270_SL_ATT0 | 0x40014B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX270_SL_ATT1 | 0x40014B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX270_SL_ATT2 | 0x40014B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX270_SL_ATT3 | 0x40014B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX270_MS_ADDR | 0x40014BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX270_MS_SIZE | 0x40014BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX270_MS_ATT0 | 0x40014BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX270_MS_ATT1 | 0x40014BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX270_MS_ATT2 | 0x40014BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX270_MS_ATT3 | 0x40014BBC | FULL | Master attributes 3 |

21.288 PPU_FX 271

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX271_SL_ADDR | 0x40014BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX271_SL_SIZE | 0x40014BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX271_SL_ATT0 | 0x40014BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX271_SL_ATT1 | 0x40014BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX271_SL_ATT2 | 0x40014BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX271_SL_ATT3 | 0x40014BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX271_MS_ADDR | 0x40014BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX271_MS_SIZE | 0x40014BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX271_MS_ATT0 | 0x40014BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX271_MS_ATT1 | 0x40014BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX271_MS_ATT2 | 0x40014BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX271_MS_ATT3 | 0x40014BFC | FULL | Master attributes 3 |

21.289 PPU_FX 272

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX272_SL_ADDR | 0x40014C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX272_SL_SIZE | 0x40014C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX272_SL_ATT0 | 0x40014C10 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX272_SL_ATT1 | 0x40014C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX272_SL_ATT2 | 0x40014C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX272_SL_ATT3 | 0x40014C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX272_MS_ADDR | 0x40014C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX272_MS_SIZE | 0x40014C24 | FULL | Master region, size |
| PERI_MS_PPU_FX272_MS_ATT0 | 0x40014C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX272_MS_ATT1 | 0x40014C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX272_MS_ATT2 | 0x40014C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX272_MS_ATT3 | 0x40014C3C | FULL | Master attributes 3 |

21.290 PPU_FX 273

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX273_SL_ADDR | 0x40014C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX273_SL_SIZE | 0x40014C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX273_SL_ATT0 | 0x40014C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX273_SL_ATT1 | 0x40014C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX273_SL_ATT2 | 0x40014C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX273_SL_ATT3 | 0x40014C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX273_MS_ADDR | 0x40014C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX273_MS_SIZE | 0x40014C64 | FULL | Master region, size |
| PERI_MS_PPU_FX273_MS_ATT0 | 0x40014C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX273_MS_ATT1 | 0x40014C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX273_MS_ATT2 | 0x40014C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX273_MS_ATT3 | 0x40014C7C | FULL | Master attributes 3 |

21.291 PPU_FX 274

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX274_SL_ADDR | 0x40014C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX274_SL_SIZE | 0x40014C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX274_SL_ATT0 | 0x40014C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX274_SL_ATT1 | 0x40014C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX274_SL_ATT2 | 0x40014C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX274_SL_ATT3 | 0x40014C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX274_MS_ADDR | 0x40014CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX274_MS_SIZE | 0x40014CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX274_MS_ATT0 | 0x40014CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX274_MS_ATT1 | 0x40014CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX274_MS_ATT2 | 0x40014CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX274_MS_ATT3 | 0x40014CBC | FULL | Master attributes 3 |

21.292 PPU_FX 275

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX275_SL_ADDR | 0x40014CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX275_SL_SIZE | 0x40014CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX275_SL_ATT0 | 0x40014CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX275_SL_ATT1 | 0x40014CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX275_SL_ATT2 | 0x40014CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX275_SL_ATT3 | 0x40014CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX275_MS_ADDR | 0x40014CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX275_MS_SIZE | 0x40014CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX275_MS_ATT0 | 0x40014CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX275_MS_ATT1 | 0x40014CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX275_MS_ATT2 | 0x40014CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX275_MS_ATT3 | 0x40014CFC | FULL | Master attributes 3 |

21.293 PPU_FX 276

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX276_SL_ADDR | 0x40014D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX276_SL_SIZE | 0x40014D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX276_SL_ATT0 | 0x40014D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX276_SL_ATT1 | 0x40014D14 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX276_SL_ATT2 | 0x40014D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX276_SL_ATT3 | 0x40014D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX276_MS_ADDR | 0x40014D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX276_MS_SIZE | 0x40014D24 | FULL | Master region, size |
| PERI_MS_PPU_FX276_MS_ATT0 | 0x40014D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX276_MS_ATT1 | 0x40014D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX276_MS_ATT2 | 0x40014D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX276_MS_ATT3 | 0x40014D3C | FULL | Master attributes 3 |

21.294 PPU_FX 277

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX277_SL_ADDR | 0x40014D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX277_SL_SIZE | 0x40014D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX277_SL_ATT0 | 0x40014D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX277_SL_ATT1 | 0x40014D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX277_SL_ATT2 | 0x40014D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX277_SL_ATT3 | 0x40014D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX277_MS_ADDR | 0x40014D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX277_MS_SIZE | 0x40014D64 | FULL | Master region, size |
| PERI_MS_PPU_FX277_MS_ATT0 | 0x40014D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX277_MS_ATT1 | 0x40014D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX277_MS_ATT2 | 0x40014D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX277_MS_ATT3 | 0x40014D7C | FULL | Master attributes 3 |

21.295 PPU_FX 278

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX278_SL_ADDR | 0x40014D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX278_SL_SIZE | 0x40014D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX278_SL_ATT0 | 0x40014D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX278_SL_ATT1 | 0x40014D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX278_SL_ATT2 | 0x40014D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX278_SL_ATT3 | 0x40014D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX278_MS_ADDR | 0x40014DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX278_MS_SIZE | 0x40014DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX278_MS_ATT0 | 0x40014DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX278_MS_ATT1 | 0x40014DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX278_MS_ATT2 | 0x40014DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX278_MS_ATT3 | 0x40014DBC | FULL | Master attributes 3 |

21.296 PPU_FX 279

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX279_SL_ADDR | 0x40014DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX279_SL_SIZE | 0x40014DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX279_SL_ATT0 | 0x40014DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX279_SL_ATT1 | 0x40014DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX279_SL_ATT2 | 0x40014DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX279_SL_ATT3 | 0x40014DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX279_MS_ADDR | 0x40014DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX279_MS_SIZE | 0x40014DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX279_MS_ATT0 | 0x40014DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX279_MS_ATT1 | 0x40014DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX279_MS_ATT2 | 0x40014DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX279_MS_ATT3 | 0x40014DFC | FULL | Master attributes 3 |

21.297 PPU_FX 280

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX280_SL_ADDR | 0x40014E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX280_SL_SIZE | 0x40014E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX280_SL_ATT0 | 0x40014E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX280_SL_ATT1 | 0x40014E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX280_SL_ATT2 | 0x40014E18 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX280_SL_ATT3 | 0x40014E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX280_MS_ADDR | 0x40014E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX280_MS_SIZE | 0x40014E24 | FULL | Master region, size |
| PERI_MS_PPU_FX280_MS_ATT0 | 0x40014E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX280_MS_ATT1 | 0x40014E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX280_MS_ATT2 | 0x40014E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX280_MS_ATT3 | 0x40014E3C | FULL | Master attributes 3 |

21.298 PPU_FX 281

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX281_SL_ADDR | 0x40014E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX281_SL_SIZE | 0x40014E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX281_SL_ATT0 | 0x40014E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX281_SL_ATT1 | 0x40014E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX281_SL_ATT2 | 0x40014E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX281_SL_ATT3 | 0x40014E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX281_MS_ADDR | 0x40014E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX281_MS_SIZE | 0x40014E64 | FULL | Master region, size |
| PERI_MS_PPU_FX281_MS_ATT0 | 0x40014E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX281_MS_ATT1 | 0x40014E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX281_MS_ATT2 | 0x40014E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX281_MS_ATT3 | 0x40014E7C | FULL | Master attributes 3 |

21.299 PPU_FX 282

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX282_SL_ADDR | 0x40014E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX282_SL_SIZE | 0x40014E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX282_SL_ATT0 | 0x40014E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX282_SL_ATT1 | 0x40014E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX282_SL_ATT2 | 0x40014E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX282_SL_ATT3 | 0x40014E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX282_MS_ADDR | 0x40014EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX282_MS_SIZE | 0x40014EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX282_MS_ATT0 | 0x40014EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX282_MS_ATT1 | 0x40014EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX282_MS_ATT2 | 0x40014EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX282_MS_ATT3 | 0x40014EBC | FULL | Master attributes 3 |

21.300 PPU_FX 283

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX283_SL_ADDR | 0x40014EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX283_SL_SIZE | 0x40014EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX283_SL_ATT0 | 0x40014ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX283_SL_ATT1 | 0x40014ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX283_SL_ATT2 | 0x40014ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX283_SL_ATT3 | 0x40014EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX283_MS_ADDR | 0x40014EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX283_MS_SIZE | 0x40014EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX283_MS_ATT0 | 0x40014EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX283_MS_ATT1 | 0x40014EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX283_MS_ATT2 | 0x40014EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX283_MS_ATT3 | 0x40014EFC | FULL | Master attributes 3 |

21.301 PPU_FX 284

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX284_SL_ADDR | 0x40014F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX284_SL_SIZE | 0x40014F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX284_SL_ATT0 | 0x40014F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX284_SL_ATT1 | 0x40014F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX284_SL_ATT2 | 0x40014F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX284_SL_ATT3 | 0x40014F1C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX284_MS_ADDR | 0x40014F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX284_MS_SIZE | 0x40014F24 | FULL | Master region, size |
| PERI_MS_PPU_FX284_MS_ATT0 | 0x40014F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX284_MS_ATT1 | 0x40014F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX284_MS_ATT2 | 0x40014F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX284_MS_ATT3 | 0x40014F3C | FULL | Master attributes 3 |

21.302 PPU_FX 285

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX285_SL_ADDR | 0x40014F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX285_SL_SIZE | 0x40014F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX285_SL_ATT0 | 0x40014F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX285_SL_ATT1 | 0x40014F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX285_SL_ATT2 | 0x40014F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX285_SL_ATT3 | 0x40014F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX285_MS_ADDR | 0x40014F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX285_MS_SIZE | 0x40014F64 | FULL | Master region, size |
| PERI_MS_PPU_FX285_MS_ATT0 | 0x40014F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX285_MS_ATT1 | 0x40014F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX285_MS_ATT2 | 0x40014F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX285_MS_ATT3 | 0x40014F7C | FULL | Master attributes 3 |

21.303 PPU_FX 286

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX286_SL_ADDR | 0x40014F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX286_SL_SIZE | 0x40014F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX286_SL_ATT0 | 0x40014F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX286_SL_ATT1 | 0x40014F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX286_SL_ATT2 | 0x40014F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX286_SL_ATT3 | 0x40014F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX286_MS_ADDR | 0x40014FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX286_MS_SIZE | 0x40014FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX286_MS_ATT0 | 0x40014FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX286_MS_ATT1 | 0x40014FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX286_MS_ATT2 | 0x40014FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX286_MS_ATT3 | 0x40014FBC | FULL | Master attributes 3 |

21.304 PPU_FX 287

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX287_SL_ADDR | 0x40014FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX287_SL_SIZE | 0x40014FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX287_SL_ATT0 | 0x40014FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX287_SL_ATT1 | 0x40014FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX287_SL_ATT2 | 0x40014FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX287_SL_ATT3 | 0x40014FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX287_MS_ADDR | 0x40014FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX287_MS_SIZE | 0x40014FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX287_MS_ATT0 | 0x40014FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX287_MS_ATT1 | 0x40014FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX287_MS_ATT2 | 0x40014FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX287_MS_ATT3 | 0x40014FFC | FULL | Master attributes 3 |

21.305 PPU_FX 288

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX288_SL_ADDR | 0x40015000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX288_SL_SIZE | 0x40015004 | FULL | Slave region, size |
| PERI_MS_PPU_FX288_SL_ATT0 | 0x40015010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX288_SL_ATT1 | 0x40015014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX288_SL_ATT2 | 0x40015018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX288_SL_ATT3 | 0x4001501C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX288_MS_ADDR | 0x40015020 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX288_MS_SIZE | 0x40015024 | FULL | Master region, size |
| PERI_MS_PPU_FX288_MS_ATT0 | 0x40015030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX288_MS_ATT1 | 0x40015034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX288_MS_ATT2 | 0x40015038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX288_MS_ATT3 | 0x4001503C | FULL | Master attributes 3 |

21.306 PPU_FX 289

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX289_SL_ADDR | 0x40015040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX289_SL_SIZE | 0x40015044 | FULL | Slave region, size |
| PERI_MS_PPU_FX289_SL_ATT0 | 0x40015050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX289_SL_ATT1 | 0x40015054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX289_SL_ATT2 | 0x40015058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX289_SL_ATT3 | 0x4001505C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX289_MS_ADDR | 0x40015060 | FULL | Master region, base address |
| PERI_MS_PPU_FX289_MS_SIZE | 0x40015064 | FULL | Master region, size |
| PERI_MS_PPU_FX289_MS_ATT0 | 0x40015070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX289_MS_ATT1 | 0x40015074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX289_MS_ATT2 | 0x40015078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX289_MS_ATT3 | 0x4001507C | FULL | Master attributes 3 |

21.307 PPU_FX 290

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX290_SL_ADDR | 0x40015080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX290_SL_SIZE | 0x40015084 | FULL | Slave region, size |
| PERI_MS_PPU_FX290_SL_ATT0 | 0x40015090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX290_SL_ATT1 | 0x40015094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX290_SL_ATT2 | 0x40015098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX290_SL_ATT3 | 0x4001509C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX290_MS_ADDR | 0x400150A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX290_MS_SIZE | 0x400150A4 | FULL | Master region, size |
| PERI_MS_PPU_FX290_MS_ATT0 | 0x400150B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX290_MS_ATT1 | 0x400150B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX290_MS_ATT2 | 0x400150B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX290_MS_ATT3 | 0x400150BC | FULL | Master attributes 3 |

21.308 PPU_FX 291

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX291_SL_ADDR | 0x400150C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX291_SL_SIZE | 0x400150C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX291_SL_ATT0 | 0x400150D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX291_SL_ATT1 | 0x400150D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX291_SL_ATT2 | 0x400150D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX291_SL_ATT3 | 0x400150DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX291_MS_ADDR | 0x400150E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX291_MS_SIZE | 0x400150E4 | FULL | Master region, size |
| PERI_MS_PPU_FX291_MS_ATT0 | 0x400150F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX291_MS_ATT1 | 0x400150F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX291_MS_ATT2 | 0x400150F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX291_MS_ATT3 | 0x400150FC | FULL | Master attributes 3 |

21.309 PPU_FX 292

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX292_SL_ADDR | 0x40015100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX292_SL_SIZE | 0x40015104 | FULL | Slave region, size |
| PERI_MS_PPU_FX292_SL_ATT0 | 0x40015110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX292_SL_ATT1 | 0x40015114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX292_SL_ATT2 | 0x40015118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX292_SL_ATT3 | 0x4001511C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX292_MS_ADDR | 0x40015120 | FULL | Master region, base address |
| PERI_MS_PPU_FX292_MS_SIZE | 0x40015124 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX292_MS_ATT0 | 0x40015130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX292_MS_ATT1 | 0x40015134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX292_MS_ATT2 | 0x40015138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX292_MS_ATT3 | 0x4001513C | FULL | Master attributes 3 |

21.310 PPU_FX 293

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX293_SL_ADDR | 0x40015140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX293_SL_SIZE | 0x40015144 | FULL | Slave region, size |
| PERI_MS_PPU_FX293_SL_ATT0 | 0x40015150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX293_SL_ATT1 | 0x40015154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX293_SL_ATT2 | 0x40015158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX293_SL_ATT3 | 0x4001515C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX293_MS_ADDR | 0x40015160 | FULL | Master region, base address |
| PERI_MS_PPU_FX293_MS_SIZE | 0x40015164 | FULL | Master region, size |
| PERI_MS_PPU_FX293_MS_ATT0 | 0x40015170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX293_MS_ATT1 | 0x40015174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX293_MS_ATT2 | 0x40015178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX293_MS_ATT3 | 0x4001517C | FULL | Master attributes 3 |

21.311 PPU_FX 294

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX294_SL_ADDR | 0x40015180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX294_SL_SIZE | 0x40015184 | FULL | Slave region, size |
| PERI_MS_PPU_FX294_SL_ATT0 | 0x40015190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX294_SL_ATT1 | 0x40015194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX294_SL_ATT2 | 0x40015198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX294_SL_ATT3 | 0x4001519C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX294_MS_ADDR | 0x400151A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX294_MS_SIZE | 0x400151A4 | FULL | Master region, size |
| PERI_MS_PPU_FX294_MS_ATT0 | 0x400151B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX294_MS_ATT1 | 0x400151B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX294_MS_ATT2 | 0x400151B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX294_MS_ATT3 | 0x400151BC | FULL | Master attributes 3 |

21.312 PPU_FX 295

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX295_SL_ADDR | 0x400151C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX295_SL_SIZE | 0x400151C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX295_SL_ATT0 | 0x400151D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX295_SL_ATT1 | 0x400151D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX295_SL_ATT2 | 0x400151D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX295_SL_ATT3 | 0x400151DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX295_MS_ADDR | 0x400151E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX295_MS_SIZE | 0x400151E4 | FULL | Master region, size |
| PERI_MS_PPU_FX295_MS_ATT0 | 0x400151F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX295_MS_ATT1 | 0x400151F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX295_MS_ATT2 | 0x400151F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX295_MS_ATT3 | 0x400151FC | FULL | Master attributes 3 |

21.313 PPU_FX 296

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX296_SL_ADDR | 0x40015200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX296_SL_SIZE | 0x40015204 | FULL | Slave region, size |
| PERI_MS_PPU_FX296_SL_ATT0 | 0x40015210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX296_SL_ATT1 | 0x40015214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX296_SL_ATT2 | 0x40015218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX296_SL_ATT3 | 0x4001521C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX296_MS_ADDR | 0x40015220 | FULL | Master region, base address |
| PERI_MS_PPU_FX296_MS_SIZE | 0x40015224 | FULL | Master region, size |
| PERI_MS_PPU_FX296_MS_ATT0 | 0x40015230 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX296_MS_ATT1 | 0x40015234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX296_MS_ATT2 | 0x40015238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX296_MS_ATT3 | 0x4001523C | FULL | Master attributes 3 |

21.314 PPU_FX 297

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX297_SL_ADDR | 0x40015240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX297_SL_SIZE | 0x40015244 | FULL | Slave region, size |
| PERI_MS_PPU_FX297_SL_ATT0 | 0x40015250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX297_SL_ATT1 | 0x40015254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX297_SL_ATT2 | 0x40015258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX297_SL_ATT3 | 0x4001525C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX297_MS_ADDR | 0x40015260 | FULL | Master region, base address |
| PERI_MS_PPU_FX297_MS_SIZE | 0x40015264 | FULL | Master region, size |
| PERI_MS_PPU_FX297_MS_ATT0 | 0x40015270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX297_MS_ATT1 | 0x40015274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX297_MS_ATT2 | 0x40015278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX297_MS_ATT3 | 0x4001527C | FULL | Master attributes 3 |

21.315 PPU_FX 298

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX298_SL_ADDR | 0x40015280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX298_SL_SIZE | 0x40015284 | FULL | Slave region, size |
| PERI_MS_PPU_FX298_SL_ATT0 | 0x40015290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX298_SL_ATT1 | 0x40015294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX298_SL_ATT2 | 0x40015298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX298_SL_ATT3 | 0x4001529C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX298_MS_ADDR | 0x400152A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX298_MS_SIZE | 0x400152A4 | FULL | Master region, size |
| PERI_MS_PPU_FX298_MS_ATT0 | 0x400152B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX298_MS_ATT1 | 0x400152B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX298_MS_ATT2 | 0x400152B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX298_MS_ATT3 | 0x400152BC | FULL | Master attributes 3 |

21.316 PPU_FX 299

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX299_SL_ADDR | 0x400152C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX299_SL_SIZE | 0x400152C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX299_SL_ATT0 | 0x400152D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX299_SL_ATT1 | 0x400152D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX299_SL_ATT2 | 0x400152D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX299_SL_ATT3 | 0x400152DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX299_MS_ADDR | 0x400152E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX299_MS_SIZE | 0x400152E4 | FULL | Master region, size |
| PERI_MS_PPU_FX299_MS_ATT0 | 0x400152F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX299_MS_ATT1 | 0x400152F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX299_MS_ATT2 | 0x400152F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX299_MS_ATT3 | 0x400152FC | FULL | Master attributes 3 |

21.317 PPU_FX 300

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX300_SL_ADDR | 0x40015300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX300_SL_SIZE | 0x40015304 | FULL | Slave region, size |
| PERI_MS_PPU_FX300_SL_ATT0 | 0x40015310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX300_SL_ATT1 | 0x40015314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX300_SL_ATT2 | 0x40015318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX300_SL_ATT3 | 0x4001531C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX300_MS_ADDR | 0x40015320 | FULL | Master region, base address |
| PERI_MS_PPU_FX300_MS_SIZE | 0x40015324 | FULL | Master region, size |
| PERI_MS_PPU_FX300_MS_ATT0 | 0x40015330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX300_MS_ATT1 | 0x40015334 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX300_MS_ATT2 | 0x40015338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX300_MS_ATT3 | 0x4001533C | FULL | Master attributes 3 |

21.318 PPU_FX 301

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX301_SL_ADDR | 0x40015340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX301_SL_SIZE | 0x40015344 | FULL | Slave region, size |
| PERI_MS_PPU_FX301_SL_ATT0 | 0x40015350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX301_SL_ATT1 | 0x40015354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX301_SL_ATT2 | 0x40015358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX301_SL_ATT3 | 0x4001535C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX301_MS_ADDR | 0x40015360 | FULL | Master region, base address |
| PERI_MS_PPU_FX301_MS_SIZE | 0x40015364 | FULL | Master region, size |
| PERI_MS_PPU_FX301_MS_ATT0 | 0x40015370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX301_MS_ATT1 | 0x40015374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX301_MS_ATT2 | 0x40015378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX301_MS_ATT3 | 0x4001537C | FULL | Master attributes 3 |

21.319 PPU_FX 302

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX302_SL_ADDR | 0x40015380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX302_SL_SIZE | 0x40015384 | FULL | Slave region, size |
| PERI_MS_PPU_FX302_SL_ATT0 | 0x40015390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX302_SL_ATT1 | 0x40015394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX302_SL_ATT2 | 0x40015398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX302_SL_ATT3 | 0x4001539C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX302_MS_ADDR | 0x400153A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX302_MS_SIZE | 0x400153A4 | FULL | Master region, size |
| PERI_MS_PPU_FX302_MS_ATT0 | 0x400153B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX302_MS_ATT1 | 0x400153B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX302_MS_ATT2 | 0x400153B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX302_MS_ATT3 | 0x400153BC | FULL | Master attributes 3 |

21.320 PPU_FX 303

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX303_SL_ADDR | 0x400153C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX303_SL_SIZE | 0x400153C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX303_SL_ATT0 | 0x400153D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX303_SL_ATT1 | 0x400153D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX303_SL_ATT2 | 0x400153D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX303_SL_ATT3 | 0x400153DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX303_MS_ADDR | 0x400153E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX303_MS_SIZE | 0x400153E4 | FULL | Master region, size |
| PERI_MS_PPU_FX303_MS_ATT0 | 0x400153F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX303_MS_ATT1 | 0x400153F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX303_MS_ATT2 | 0x400153F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX303_MS_ATT3 | 0x400153FC | FULL | Master attributes 3 |

21.321 PPU_FX 304

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX304_SL_ADDR | 0x40015400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX304_SL_SIZE | 0x40015404 | FULL | Slave region, size |
| PERI_MS_PPU_FX304_SL_ATT0 | 0x40015410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX304_SL_ATT1 | 0x40015414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX304_SL_ATT2 | 0x40015418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX304_SL_ATT3 | 0x4001541C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX304_MS_ADDR | 0x40015420 | FULL | Master region, base address |
| PERI_MS_PPU_FX304_MS_SIZE | 0x40015424 | FULL | Master region, size |
| PERI_MS_PPU_FX304_MS_ATT0 | 0x40015430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX304_MS_ATT1 | 0x40015434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX304_MS_ATT2 | 0x40015438 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX304_MS_ATT3 | 0x4001543C | FULL | Master attributes 3 |

21.322 PPU_FX 305

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX305_SL_ADDR | 0x40015440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX305_SL_SIZE | 0x40015444 | FULL | Slave region, size |
| PERI_MS_PPU_FX305_SL_ATT0 | 0x40015450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX305_SL_ATT1 | 0x40015454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX305_SL_ATT2 | 0x40015458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX305_SL_ATT3 | 0x4001545C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX305_MS_ADDR | 0x40015460 | FULL | Master region, base address |
| PERI_MS_PPU_FX305_MS_SIZE | 0x40015464 | FULL | Master region, size |
| PERI_MS_PPU_FX305_MS_ATT0 | 0x40015470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX305_MS_ATT1 | 0x40015474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX305_MS_ATT2 | 0x40015478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX305_MS_ATT3 | 0x4001547C | FULL | Master attributes 3 |

21.323 PPU_FX 306

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX306_SL_ADDR | 0x40015480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX306_SL_SIZE | 0x40015484 | FULL | Slave region, size |
| PERI_MS_PPU_FX306_SL_ATT0 | 0x40015490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX306_SL_ATT1 | 0x40015494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX306_SL_ATT2 | 0x40015498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX306_SL_ATT3 | 0x4001549C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX306_MS_ADDR | 0x400154A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX306_MS_SIZE | 0x400154A4 | FULL | Master region, size |
| PERI_MS_PPU_FX306_MS_ATT0 | 0x400154B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX306_MS_ATT1 | 0x400154B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX306_MS_ATT2 | 0x400154B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX306_MS_ATT3 | 0x400154BC | FULL | Master attributes 3 |

21.324 PPU_FX 307

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX307_SL_ADDR | 0x400154C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX307_SL_SIZE | 0x400154C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX307_SL_ATT0 | 0x400154D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX307_SL_ATT1 | 0x400154D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX307_SL_ATT2 | 0x400154D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX307_SL_ATT3 | 0x400154DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX307_MS_ADDR | 0x400154E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX307_MS_SIZE | 0x400154E4 | FULL | Master region, size |
| PERI_MS_PPU_FX307_MS_ATT0 | 0x400154F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX307_MS_ATT1 | 0x400154F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX307_MS_ATT2 | 0x400154F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX307_MS_ATT3 | 0x400154FC | FULL | Master attributes 3 |

21.325 PPU_FX 308

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX308_SL_ADDR | 0x40015500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX308_SL_SIZE | 0x40015504 | FULL | Slave region, size |
| PERI_MS_PPU_FX308_SL_ATT0 | 0x40015510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX308_SL_ATT1 | 0x40015514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX308_SL_ATT2 | 0x40015518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX308_SL_ATT3 | 0x4001551C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX308_MS_ADDR | 0x40015520 | FULL | Master region, base address |
| PERI_MS_PPU_FX308_MS_SIZE | 0x40015524 | FULL | Master region, size |
| PERI_MS_PPU_FX308_MS_ATT0 | 0x40015530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX308_MS_ATT1 | 0x40015534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX308_MS_ATT2 | 0x40015538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX308_MS_ATT3 | 0x4001553C | FULL | Master attributes 3 |

21.326 PPU_FX 309

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX309_SL_ADDR | 0x40015540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX309_SL_SIZE | 0x40015544 | FULL | Slave region, size |
| PERI_MS_PPU_FX309_SL_ATT0 | 0x40015550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX309_SL_ATT1 | 0x40015554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX309_SL_ATT2 | 0x40015558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX309_SL_ATT3 | 0x4001555C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX309_MS_ADDR | 0x40015560 | FULL | Master region, base address |
| PERI_MS_PPU_FX309_MS_SIZE | 0x40015564 | FULL | Master region, size |
| PERI_MS_PPU_FX309_MS_ATT0 | 0x40015570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX309_MS_ATT1 | 0x40015574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX309_MS_ATT2 | 0x40015578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX309_MS_ATT3 | 0x4001557C | FULL | Master attributes 3 |

21.327 PPU_FX 310

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX310_SL_ADDR | 0x40015580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX310_SL_SIZE | 0x40015584 | FULL | Slave region, size |
| PERI_MS_PPU_FX310_SL_ATT0 | 0x40015590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX310_SL_ATT1 | 0x40015594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX310_SL_ATT2 | 0x40015598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX310_SL_ATT3 | 0x4001559C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX310_MS_ADDR | 0x400155A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX310_MS_SIZE | 0x400155A4 | FULL | Master region, size |
| PERI_MS_PPU_FX310_MS_ATT0 | 0x400155B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX310_MS_ATT1 | 0x400155B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX310_MS_ATT2 | 0x400155B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX310_MS_ATT3 | 0x400155BC | FULL | Master attributes 3 |

21.328 PPU_FX 311

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX311_SL_ADDR | 0x400155C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX311_SL_SIZE | 0x400155C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX311_SL_ATT0 | 0x400155D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX311_SL_ATT1 | 0x400155D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX311_SL_ATT2 | 0x400155D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX311_SL_ATT3 | 0x400155DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX311_MS_ADDR | 0x400155E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX311_MS_SIZE | 0x400155E4 | FULL | Master region, size |
| PERI_MS_PPU_FX311_MS_ATT0 | 0x400155F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX311_MS_ATT1 | 0x400155F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX311_MS_ATT2 | 0x400155F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX311_MS_ATT3 | 0x400155FC | FULL | Master attributes 3 |

21.329 PPU_FX 312

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX312_SL_ADDR | 0x40015600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX312_SL_SIZE | 0x40015604 | FULL | Slave region, size |
| PERI_MS_PPU_FX312_SL_ATT0 | 0x40015610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX312_SL_ATT1 | 0x40015614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX312_SL_ATT2 | 0x40015618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX312_SL_ATT3 | 0x4001561C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX312_MS_ADDR | 0x40015620 | FULL | Master region, base address |
| PERI_MS_PPU_FX312_MS_SIZE | 0x40015624 | FULL | Master region, size |
| PERI_MS_PPU_FX312_MS_ATT0 | 0x40015630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX312_MS_ATT1 | 0x40015634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX312_MS_ATT2 | 0x40015638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX312_MS_ATT3 | 0x4001563C | FULL | Master attributes 3 |

21.330 PPU_FX 313

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX313_SL_ADDR | 0x40015640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX313_SL_SIZE | 0x40015644 | FULL | Slave region, size |
| PERI_MS_PPU_FX313_SL_ATT0 | 0x40015650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX313_SL_ATT1 | 0x40015654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX313_SL_ATT2 | 0x40015658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX313_SL_ATT3 | 0x4001565C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX313_MS_ADDR | 0x40015660 | FULL | Master region, base address |
| PERI_MS_PPU_FX313_MS_SIZE | 0x40015664 | FULL | Master region, size |
| PERI_MS_PPU_FX313_MS_ATT0 | 0x40015670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX313_MS_ATT1 | 0x40015674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX313_MS_ATT2 | 0x40015678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX313_MS_ATT3 | 0x4001567C | FULL | Master attributes 3 |

21.331 PPU_FX 314

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX314_SL_ADDR | 0x40015680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX314_SL_SIZE | 0x40015684 | FULL | Slave region, size |
| PERI_MS_PPU_FX314_SL_ATT0 | 0x40015690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX314_SL_ATT1 | 0x40015694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX314_SL_ATT2 | 0x40015698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX314_SL_ATT3 | 0x4001569C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX314_MS_ADDR | 0x400156A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX314_MS_SIZE | 0x400156A4 | FULL | Master region, size |
| PERI_MS_PPU_FX314_MS_ATT0 | 0x400156B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX314_MS_ATT1 | 0x400156B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX314_MS_ATT2 | 0x400156B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX314_MS_ATT3 | 0x400156BC | FULL | Master attributes 3 |

21.332 PPU_FX 315

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX315_SL_ADDR | 0x400156C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX315_SL_SIZE | 0x400156C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX315_SL_ATT0 | 0x400156D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX315_SL_ATT1 | 0x400156D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX315_SL_ATT2 | 0x400156D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX315_SL_ATT3 | 0x400156DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX315_MS_ADDR | 0x400156E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX315_MS_SIZE | 0x400156E4 | FULL | Master region, size |
| PERI_MS_PPU_FX315_MS_ATT0 | 0x400156F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX315_MS_ATT1 | 0x400156F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX315_MS_ATT2 | 0x400156F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX315_MS_ATT3 | 0x400156FC | FULL | Master attributes 3 |

21.333 PPU_FX 316

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX316_SL_ADDR | 0x40015700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX316_SL_SIZE | 0x40015704 | FULL | Slave region, size |
| PERI_MS_PPU_FX316_SL_ATT0 | 0x40015710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX316_SL_ATT1 | 0x40015714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX316_SL_ATT2 | 0x40015718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX316_SL_ATT3 | 0x4001571C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX316_MS_ADDR | 0x40015720 | FULL | Master region, base address |
| PERI_MS_PPU_FX316_MS_SIZE | 0x40015724 | FULL | Master region, size |
| PERI_MS_PPU_FX316_MS_ATT0 | 0x40015730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX316_MS_ATT1 | 0x40015734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX316_MS_ATT2 | 0x40015738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX316_MS_ATT3 | 0x4001573C | FULL | Master attributes 3 |

21.334 PPU_FX 317

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX317_SL_ADDR | 0x40015740 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX317_SL_SIZE | 0x40015744 | FULL | Slave region, size |
| PERI_MS_PPU_FX317_SL_ATT0 | 0x40015750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX317_SL_ATT1 | 0x40015754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX317_SL_ATT2 | 0x40015758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX317_SL_ATT3 | 0x4001575C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX317_MS_ADDR | 0x40015760 | FULL | Master region, base address |
| PERI_MS_PPU_FX317_MS_SIZE | 0x40015764 | FULL | Master region, size |
| PERI_MS_PPU_FX317_MS_ATT0 | 0x40015770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX317_MS_ATT1 | 0x40015774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX317_MS_ATT2 | 0x40015778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX317_MS_ATT3 | 0x4001577C | FULL | Master attributes 3 |

21.335 PPU_FX 318

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX318_SL_ADDR | 0x40015780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX318_SL_SIZE | 0x40015784 | FULL | Slave region, size |
| PERI_MS_PPU_FX318_SL_ATT0 | 0x40015790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX318_SL_ATT1 | 0x40015794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX318_SL_ATT2 | 0x40015798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX318_SL_ATT3 | 0x4001579C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX318_MS_ADDR | 0x400157A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX318_MS_SIZE | 0x400157A4 | FULL | Master region, size |
| PERI_MS_PPU_FX318_MS_ATT0 | 0x400157B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX318_MS_ATT1 | 0x400157B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX318_MS_ATT2 | 0x400157B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX318_MS_ATT3 | 0x400157BC | FULL | Master attributes 3 |

21.336 PPU_FX 319

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX319_SL_ADDR | 0x400157C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX319_SL_SIZE | 0x400157C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX319_SL_ATT0 | 0x400157D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX319_SL_ATT1 | 0x400157D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX319_SL_ATT2 | 0x400157D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX319_SL_ATT3 | 0x400157DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX319_MS_ADDR | 0x400157E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX319_MS_SIZE | 0x400157E4 | FULL | Master region, size |
| PERI_MS_PPU_FX319_MS_ATT0 | 0x400157F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX319_MS_ATT1 | 0x400157F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX319_MS_ATT2 | 0x400157F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX319_MS_ATT3 | 0x400157FC | FULL | Master attributes 3 |

21.337 PPU_FX 320

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX320_SL_ADDR | 0x40015800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX320_SL_SIZE | 0x40015804 | FULL | Slave region, size |
| PERI_MS_PPU_FX320_SL_ATT0 | 0x40015810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX320_SL_ATT1 | 0x40015814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX320_SL_ATT2 | 0x40015818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX320_SL_ATT3 | 0x4001581C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX320_MS_ADDR | 0x40015820 | FULL | Master region, base address |
| PERI_MS_PPU_FX320_MS_SIZE | 0x40015824 | FULL | Master region, size |
| PERI_MS_PPU_FX320_MS_ATT0 | 0x40015830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX320_MS_ATT1 | 0x40015834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX320_MS_ATT2 | 0x40015838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX320_MS_ATT3 | 0x4001583C | FULL | Master attributes 3 |

21.338 PPU_FX 321

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX321_SL_ADDR | 0x40015840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX321_SL_SIZE | 0x40015844 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX321_SL_ATT0 | 0x40015850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX321_SL_ATT1 | 0x40015854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX321_SL_ATT2 | 0x40015858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX321_SL_ATT3 | 0x4001585C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX321_MS_ADDR | 0x40015860 | FULL | Master region, base address |
| PERI_MS_PPU_FX321_MS_SIZE | 0x40015864 | FULL | Master region, size |
| PERI_MS_PPU_FX321_MS_ATT0 | 0x40015870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX321_MS_ATT1 | 0x40015874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX321_MS_ATT2 | 0x40015878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX321_MS_ATT3 | 0x4001587C | FULL | Master attributes 3 |

21.339 PPU_FX 322

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX322_SL_ADDR | 0x40015880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX322_SL_SIZE | 0x40015884 | FULL | Slave region, size |
| PERI_MS_PPU_FX322_SL_ATT0 | 0x40015890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX322_SL_ATT1 | 0x40015894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX322_SL_ATT2 | 0x40015898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX322_SL_ATT3 | 0x4001589C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX322_MS_ADDR | 0x400158A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX322_MS_SIZE | 0x400158A4 | FULL | Master region, size |
| PERI_MS_PPU_FX322_MS_ATT0 | 0x400158B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX322_MS_ATT1 | 0x400158B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX322_MS_ATT2 | 0x400158B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX322_MS_ATT3 | 0x400158BC | FULL | Master attributes 3 |

21.340 PPU_FX 323

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX323_SL_ADDR | 0x400158C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX323_SL_SIZE | 0x400158C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX323_SL_ATT0 | 0x400158D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX323_SL_ATT1 | 0x400158D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX323_SL_ATT2 | 0x400158D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX323_SL_ATT3 | 0x400158DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX323_MS_ADDR | 0x400158E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX323_MS_SIZE | 0x400158E4 | FULL | Master region, size |
| PERI_MS_PPU_FX323_MS_ATT0 | 0x400158F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX323_MS_ATT1 | 0x400158F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX323_MS_ATT2 | 0x400158F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX323_MS_ATT3 | 0x400158FC | FULL | Master attributes 3 |

21.341 PPU_FX 324

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX324_SL_ADDR | 0x40015900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX324_SL_SIZE | 0x40015904 | FULL | Slave region, size |
| PERI_MS_PPU_FX324_SL_ATT0 | 0x40015910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX324_SL_ATT1 | 0x40015914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX324_SL_ATT2 | 0x40015918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX324_SL_ATT3 | 0x4001591C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX324_MS_ADDR | 0x40015920 | FULL | Master region, base address |
| PERI_MS_PPU_FX324_MS_SIZE | 0x40015924 | FULL | Master region, size |
| PERI_MS_PPU_FX324_MS_ATT0 | 0x40015930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX324_MS_ATT1 | 0x40015934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX324_MS_ATT2 | 0x40015938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX324_MS_ATT3 | 0x4001593C | FULL | Master attributes 3 |

21.342 PPU_FX 325

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX325_SL_ADDR | 0x40015940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX325_SL_SIZE | 0x40015944 | FULL | Slave region, size |
| PERI_MS_PPU_FX325_SL_ATT0 | 0x40015950 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX325_SL_ATT1 | 0x40015954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX325_SL_ATT2 | 0x40015958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX325_SL_ATT3 | 0x4001595C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX325_MS_ADDR | 0x40015960 | FULL | Master region, base address |
| PERI_MS_PPU_FX325_MS_SIZE | 0x40015964 | FULL | Master region, size |
| PERI_MS_PPU_FX325_MS_ATT0 | 0x40015970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX325_MS_ATT1 | 0x40015974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX325_MS_ATT2 | 0x40015978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX325_MS_ATT3 | 0x4001597C | FULL | Master attributes 3 |

21.343 PPU_FX 326

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX326_SL_ADDR | 0x40015980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX326_SL_SIZE | 0x40015984 | FULL | Slave region, size |
| PERI_MS_PPU_FX326_SL_ATT0 | 0x40015990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX326_SL_ATT1 | 0x40015994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX326_SL_ATT2 | 0x40015998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX326_SL_ATT3 | 0x4001599C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX326_MS_ADDR | 0x400159A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX326_MS_SIZE | 0x400159A4 | FULL | Master region, size |
| PERI_MS_PPU_FX326_MS_ATT0 | 0x400159B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX326_MS_ATT1 | 0x400159B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX326_MS_ATT2 | 0x400159B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX326_MS_ATT3 | 0x400159BC | FULL | Master attributes 3 |

21.344 PPU_FX 327

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX327_SL_ADDR | 0x400159C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX327_SL_SIZE | 0x400159C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX327_SL_ATT0 | 0x400159D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX327_SL_ATT1 | 0x400159D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX327_SL_ATT2 | 0x400159D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX327_SL_ATT3 | 0x400159DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX327_MS_ADDR | 0x400159E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX327_MS_SIZE | 0x400159E4 | FULL | Master region, size |
| PERI_MS_PPU_FX327_MS_ATT0 | 0x400159F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX327_MS_ATT1 | 0x400159F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX327_MS_ATT2 | 0x400159F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX327_MS_ATT3 | 0x400159FC | FULL | Master attributes 3 |

21.345 PPU_FX 328

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX328_SL_ADDR | 0x40015A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX328_SL_SIZE | 0x40015A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX328_SL_ATT0 | 0x40015A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX328_SL_ATT1 | 0x40015A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX328_SL_ATT2 | 0x40015A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX328_SL_ATT3 | 0x40015A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX328_MS_ADDR | 0x40015A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX328_MS_SIZE | 0x40015A24 | FULL | Master region, size |
| PERI_MS_PPU_FX328_MS_ATT0 | 0x40015A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX328_MS_ATT1 | 0x40015A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX328_MS_ATT2 | 0x40015A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX328_MS_ATT3 | 0x40015A3C | FULL | Master attributes 3 |

21.346 PPU_FX 329

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX329_SL_ADDR | 0x40015A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX329_SL_SIZE | 0x40015A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX329_SL_ATT0 | 0x40015A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX329_SL_ATT1 | 0x40015A54 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX329_SL_ATT2 | 0x40015A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX329_SL_ATT3 | 0x40015A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX329_MS_ADDR | 0x40015A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX329_MS_SIZE | 0x40015A64 | FULL | Master region, size |
| PERI_MS_PPU_FX329_MS_ATT0 | 0x40015A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX329_MS_ATT1 | 0x40015A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX329_MS_ATT2 | 0x40015A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX329_MS_ATT3 | 0x40015A7C | FULL | Master attributes 3 |

21.347 PPU_FX 330

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX330_SL_ADDR | 0x40015A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX330_SL_SIZE | 0x40015A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX330_SL_ATT0 | 0x40015A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX330_SL_ATT1 | 0x40015A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX330_SL_ATT2 | 0x40015A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX330_SL_ATT3 | 0x40015A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX330_MS_ADDR | 0x40015AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX330_MS_SIZE | 0x40015AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX330_MS_ATT0 | 0x40015AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX330_MS_ATT1 | 0x40015AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX330_MS_ATT2 | 0x40015AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX330_MS_ATT3 | 0x40015ABC | FULL | Master attributes 3 |

21.348 PPU_FX 331

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX331_SL_ADDR | 0x40015AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX331_SL_SIZE | 0x40015AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX331_SL_ATT0 | 0x40015AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX331_SL_ATT1 | 0x40015AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX331_SL_ATT2 | 0x40015AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX331_SL_ATT3 | 0x40015ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX331_MS_ADDR | 0x40015AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX331_MS_SIZE | 0x40015AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX331_MS_ATT0 | 0x40015AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX331_MS_ATT1 | 0x40015AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX331_MS_ATT2 | 0x40015AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX331_MS_ATT3 | 0x40015AFC | FULL | Master attributes 3 |

21.349 PPU_FX 332

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX332_SL_ADDR | 0x40015B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX332_SL_SIZE | 0x40015B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX332_SL_ATT0 | 0x40015B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX332_SL_ATT1 | 0x40015B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX332_SL_ATT2 | 0x40015B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX332_SL_ATT3 | 0x40015B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX332_MS_ADDR | 0x40015B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX332_MS_SIZE | 0x40015B24 | FULL | Master region, size |
| PERI_MS_PPU_FX332_MS_ATT0 | 0x40015B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX332_MS_ATT1 | 0x40015B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX332_MS_ATT2 | 0x40015B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX332_MS_ATT3 | 0x40015B3C | FULL | Master attributes 3 |

21.350 PPU_FX 333

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX333_SL_ADDR | 0x40015B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX333_SL_SIZE | 0x40015B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX333_SL_ATT0 | 0x40015B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX333_SL_ATT1 | 0x40015B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX333_SL_ATT2 | 0x40015B58 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX333_SL_ATT3 | 0x40015B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX333_MS_ADDR | 0x40015B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX333_MS_SIZE | 0x40015B64 | FULL | Master region, size |
| PERI_MS_PPU_FX333_MS_ATT0 | 0x40015B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX333_MS_ATT1 | 0x40015B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX333_MS_ATT2 | 0x40015B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX333_MS_ATT3 | 0x40015B7C | FULL | Master attributes 3 |

21.351 PPU_FX 334

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX334_SL_ADDR | 0x40015B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX334_SL_SIZE | 0x40015B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX334_SL_ATT0 | 0x40015B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX334_SL_ATT1 | 0x40015B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX334_SL_ATT2 | 0x40015B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX334_SL_ATT3 | 0x40015B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX334_MS_ADDR | 0x40015BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX334_MS_SIZE | 0x40015BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX334_MS_ATT0 | 0x40015BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX334_MS_ATT1 | 0x40015BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX334_MS_ATT2 | 0x40015BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX334_MS_ATT3 | 0x40015BBC | FULL | Master attributes 3 |

21.352 PPU_FX 335

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX335_SL_ADDR | 0x40015BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX335_SL_SIZE | 0x40015BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX335_SL_ATT0 | 0x40015BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX335_SL_ATT1 | 0x40015BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX335_SL_ATT2 | 0x40015BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX335_SL_ATT3 | 0x40015BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX335_MS_ADDR | 0x40015BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX335_MS_SIZE | 0x40015BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX335_MS_ATT0 | 0x40015BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX335_MS_ATT1 | 0x40015BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX335_MS_ATT2 | 0x40015BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX335_MS_ATT3 | 0x40015BFC | FULL | Master attributes 3 |

21.353 PPU_FX 336

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX336_SL_ADDR | 0x40015C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX336_SL_SIZE | 0x40015C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX336_SL_ATT0 | 0x40015C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX336_SL_ATT1 | 0x40015C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX336_SL_ATT2 | 0x40015C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX336_SL_ATT3 | 0x40015C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX336_MS_ADDR | 0x40015C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX336_MS_SIZE | 0x40015C24 | FULL | Master region, size |
| PERI_MS_PPU_FX336_MS_ATT0 | 0x40015C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX336_MS_ATT1 | 0x40015C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX336_MS_ATT2 | 0x40015C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX336_MS_ATT3 | 0x40015C3C | FULL | Master attributes 3 |

21.354 PPU_FX 337

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX337_SL_ADDR | 0x40015C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX337_SL_SIZE | 0x40015C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX337_SL_ATT0 | 0x40015C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX337_SL_ATT1 | 0x40015C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX337_SL_ATT2 | 0x40015C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX337_SL_ATT3 | 0x40015C5C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX337_MS_ADDR | 0x40015C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX337_MS_SIZE | 0x40015C64 | FULL | Master region, size |
| PERI_MS_PPU_FX337_MS_ATT0 | 0x40015C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX337_MS_ATT1 | 0x40015C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX337_MS_ATT2 | 0x40015C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX337_MS_ATT3 | 0x40015C7C | FULL | Master attributes 3 |

21.355 PPU_FX 338

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX338_SL_ADDR | 0x40015C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX338_SL_SIZE | 0x40015C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX338_SL_ATT0 | 0x40015C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX338_SL_ATT1 | 0x40015C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX338_SL_ATT2 | 0x40015C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX338_SL_ATT3 | 0x40015C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX338_MS_ADDR | 0x40015CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX338_MS_SIZE | 0x40015CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX338_MS_ATT0 | 0x40015CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX338_MS_ATT1 | 0x40015CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX338_MS_ATT2 | 0x40015CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX338_MS_ATT3 | 0x40015CBC | FULL | Master attributes 3 |

21.356 PPU_FX 339

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX339_SL_ADDR | 0x40015CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX339_SL_SIZE | 0x40015CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX339_SL_ATT0 | 0x40015CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX339_SL_ATT1 | 0x40015CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX339_SL_ATT2 | 0x40015CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX339_SL_ATT3 | 0x40015CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX339_MS_ADDR | 0x40015CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX339_MS_SIZE | 0x40015CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX339_MS_ATT0 | 0x40015CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX339_MS_ATT1 | 0x40015CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX339_MS_ATT2 | 0x40015CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX339_MS_ATT3 | 0x40015CFC | FULL | Master attributes 3 |

21.357 PPU_FX 340

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX340_SL_ADDR | 0x40015D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX340_SL_SIZE | 0x40015D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX340_SL_ATT0 | 0x40015D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX340_SL_ATT1 | 0x40015D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX340_SL_ATT2 | 0x40015D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX340_SL_ATT3 | 0x40015D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX340_MS_ADDR | 0x40015D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX340_MS_SIZE | 0x40015D24 | FULL | Master region, size |
| PERI_MS_PPU_FX340_MS_ATT0 | 0x40015D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX340_MS_ATT1 | 0x40015D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX340_MS_ATT2 | 0x40015D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX340_MS_ATT3 | 0x40015D3C | FULL | Master attributes 3 |

21.358 PPU_FX 341

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX341_SL_ADDR | 0x40015D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX341_SL_SIZE | 0x40015D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX341_SL_ATT0 | 0x40015D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX341_SL_ATT1 | 0x40015D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX341_SL_ATT2 | 0x40015D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX341_SL_ATT3 | 0x40015D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX341_MS_ADDR | 0x40015D60 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX341_MS_SIZE | 0x40015D64 | FULL | Master region, size |
| PERI_MS_PPU_FX341_MS_ATT0 | 0x40015D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX341_MS_ATT1 | 0x40015D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX341_MS_ATT2 | 0x40015D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX341_MS_ATT3 | 0x40015D7C | FULL | Master attributes 3 |

21.359 PPU_FX 342

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX342_SL_ADDR | 0x40015D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX342_SL_SIZE | 0x40015D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX342_SL_ATT0 | 0x40015D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX342_SL_ATT1 | 0x40015D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX342_SL_ATT2 | 0x40015D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX342_SL_ATT3 | 0x40015D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX342_MS_ADDR | 0x40015DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX342_MS_SIZE | 0x40015DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX342_MS_ATT0 | 0x40015DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX342_MS_ATT1 | 0x40015DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX342_MS_ATT2 | 0x40015DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX342_MS_ATT3 | 0x40015DBC | FULL | Master attributes 3 |

21.360 PPU_FX 343

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX343_SL_ADDR | 0x40015DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX343_SL_SIZE | 0x40015DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX343_SL_ATT0 | 0x40015DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX343_SL_ATT1 | 0x40015DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX343_SL_ATT2 | 0x40015DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX343_SL_ATT3 | 0x40015DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX343_MS_ADDR | 0x40015DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX343_MS_SIZE | 0x40015DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX343_MS_ATT0 | 0x40015DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX343_MS_ATT1 | 0x40015DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX343_MS_ATT2 | 0x40015DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX343_MS_ATT3 | 0x40015DFC | FULL | Master attributes 3 |

21.361 PPU_FX 344

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX344_SL_ADDR | 0x40015E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX344_SL_SIZE | 0x40015E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX344_SL_ATT0 | 0x40015E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX344_SL_ATT1 | 0x40015E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX344_SL_ATT2 | 0x40015E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX344_SL_ATT3 | 0x40015E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX344_MS_ADDR | 0x40015E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX344_MS_SIZE | 0x40015E24 | FULL | Master region, size |
| PERI_MS_PPU_FX344_MS_ATT0 | 0x40015E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX344_MS_ATT1 | 0x40015E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX344_MS_ATT2 | 0x40015E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX344_MS_ATT3 | 0x40015E3C | FULL | Master attributes 3 |

21.362 PPU_FX 345

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX345_SL_ADDR | 0x40015E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX345_SL_SIZE | 0x40015E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX345_SL_ATT0 | 0x40015E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX345_SL_ATT1 | 0x40015E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX345_SL_ATT2 | 0x40015E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX345_SL_ATT3 | 0x40015E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX345_MS_ADDR | 0x40015E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX345_MS_SIZE | 0x40015E64 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX345_MS_ATT0 | 0x40015E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX345_MS_ATT1 | 0x40015E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX345_MS_ATT2 | 0x40015E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX345_MS_ATT3 | 0x40015E7C | FULL | Master attributes 3 |

21.363 PPU_FX 346

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX346_SL_ADDR | 0x40015E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX346_SL_SIZE | 0x40015E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX346_SL_ATT0 | 0x40015E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX346_SL_ATT1 | 0x40015E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX346_SL_ATT2 | 0x40015E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX346_SL_ATT3 | 0x40015E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX346_MS_ADDR | 0x40015EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX346_MS_SIZE | 0x40015EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX346_MS_ATT0 | 0x40015EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX346_MS_ATT1 | 0x40015EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX346_MS_ATT2 | 0x40015EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX346_MS_ATT3 | 0x40015EBC | FULL | Master attributes 3 |

21.364 PPU_FX 347

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX347_SL_ADDR | 0x40015EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX347_SL_SIZE | 0x40015EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX347_SL_ATT0 | 0x40015ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX347_SL_ATT1 | 0x40015ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX347_SL_ATT2 | 0x40015ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX347_SL_ATT3 | 0x40015EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX347_MS_ADDR | 0x40015EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX347_MS_SIZE | 0x40015EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX347_MS_ATT0 | 0x40015EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX347_MS_ATT1 | 0x40015EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX347_MS_ATT2 | 0x40015EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX347_MS_ATT3 | 0x40015EFC | FULL | Master attributes 3 |

21.365 PPU_FX 348

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX348_SL_ADDR | 0x40015F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX348_SL_SIZE | 0x40015F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX348_SL_ATT0 | 0x40015F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX348_SL_ATT1 | 0x40015F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX348_SL_ATT2 | 0x40015F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX348_SL_ATT3 | 0x40015F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX348_MS_ADDR | 0x40015F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX348_MS_SIZE | 0x40015F24 | FULL | Master region, size |
| PERI_MS_PPU_FX348_MS_ATT0 | 0x40015F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX348_MS_ATT1 | 0x40015F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX348_MS_ATT2 | 0x40015F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX348_MS_ATT3 | 0x40015F3C | FULL | Master attributes 3 |

21.366 PPU_FX 349

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX349_SL_ADDR | 0x40015F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX349_SL_SIZE | 0x40015F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX349_SL_ATT0 | 0x40015F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX349_SL_ATT1 | 0x40015F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX349_SL_ATT2 | 0x40015F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX349_SL_ATT3 | 0x40015F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX349_MS_ADDR | 0x40015F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX349_MS_SIZE | 0x40015F64 | FULL | Master region, size |
| PERI_MS_PPU_FX349_MS_ATT0 | 0x40015F70 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX349_MS_ATT1 | 0x40015F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX349_MS_ATT2 | 0x40015F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX349_MS_ATT3 | 0x40015F7C | FULL | Master attributes 3 |

21.367 PPU_FX 350

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX350_SL_ADDR | 0x40015F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX350_SL_SIZE | 0x40015F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX350_SL_ATT0 | 0x40015F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX350_SL_ATT1 | 0x40015F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX350_SL_ATT2 | 0x40015F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX350_SL_ATT3 | 0x40015F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX350_MS_ADDR | 0x40015FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX350_MS_SIZE | 0x40015FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX350_MS_ATT0 | 0x40015FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX350_MS_ATT1 | 0x40015FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX350_MS_ATT2 | 0x40015FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX350_MS_ATT3 | 0x40015FBC | FULL | Master attributes 3 |

21.368 PPU_FX 351

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX351_SL_ADDR | 0x40015FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX351_SL_SIZE | 0x40015FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX351_SL_ATT0 | 0x40015FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX351_SL_ATT1 | 0x40015FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX351_SL_ATT2 | 0x40015FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX351_SL_ATT3 | 0x40015FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX351_MS_ADDR | 0x40015FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX351_MS_SIZE | 0x40015FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX351_MS_ATT0 | 0x40015FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX351_MS_ATT1 | 0x40015FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX351_MS_ATT2 | 0x40015FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX351_MS_ATT3 | 0x40015FFC | FULL | Master attributes 3 |

21.369 PPU_FX 352

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX352_SL_ADDR | 0x40016000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX352_SL_SIZE | 0x40016004 | FULL | Slave region, size |
| PERI_MS_PPU_FX352_SL_ATT0 | 0x40016010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX352_SL_ATT1 | 0x40016014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX352_SL_ATT2 | 0x40016018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX352_SL_ATT3 | 0x4001601C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX352_MS_ADDR | 0x40016020 | FULL | Master region, base address |
| PERI_MS_PPU_FX352_MS_SIZE | 0x40016024 | FULL | Master region, size |
| PERI_MS_PPU_FX352_MS_ATT0 | 0x40016030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX352_MS_ATT1 | 0x40016034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX352_MS_ATT2 | 0x40016038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX352_MS_ATT3 | 0x4001603C | FULL | Master attributes 3 |

21.370 PPU_FX 353

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX353_SL_ADDR | 0x40016040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX353_SL_SIZE | 0x40016044 | FULL | Slave region, size |
| PERI_MS_PPU_FX353_SL_ATT0 | 0x40016050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX353_SL_ATT1 | 0x40016054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX353_SL_ATT2 | 0x40016058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX353_SL_ATT3 | 0x4001605C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX353_MS_ADDR | 0x40016060 | FULL | Master region, base address |
| PERI_MS_PPU_FX353_MS_SIZE | 0x40016064 | FULL | Master region, size |
| PERI_MS_PPU_FX353_MS_ATT0 | 0x40016070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX353_MS_ATT1 | 0x40016074 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX353_MS_ATT2 | 0x40016078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX353_MS_ATT3 | 0x4001607C | FULL | Master attributes 3 |

21.371 PPU_FX 354

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX354_SL_ADDR | 0x40016080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX354_SL_SIZE | 0x40016084 | FULL | Slave region, size |
| PERI_MS_PPU_FX354_SL_ATT0 | 0x40016090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX354_SL_ATT1 | 0x40016094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX354_SL_ATT2 | 0x40016098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX354_SL_ATT3 | 0x4001609C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX354_MS_ADDR | 0x400160A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX354_MS_SIZE | 0x400160A4 | FULL | Master region, size |
| PERI_MS_PPU_FX354_MS_ATT0 | 0x400160B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX354_MS_ATT1 | 0x400160B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX354_MS_ATT2 | 0x400160B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX354_MS_ATT3 | 0x400160BC | FULL | Master attributes 3 |

21.372 PPU_FX 355

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX355_SL_ADDR | 0x400160C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX355_SL_SIZE | 0x400160C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX355_SL_ATT0 | 0x400160D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX355_SL_ATT1 | 0x400160D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX355_SL_ATT2 | 0x400160D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX355_SL_ATT3 | 0x400160DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX355_MS_ADDR | 0x400160E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX355_MS_SIZE | 0x400160E4 | FULL | Master region, size |
| PERI_MS_PPU_FX355_MS_ATT0 | 0x400160F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX355_MS_ATT1 | 0x400160F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX355_MS_ATT2 | 0x400160F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX355_MS_ATT3 | 0x400160FC | FULL | Master attributes 3 |

21.373 PPU_FX 356

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX356_SL_ADDR | 0x40016100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX356_SL_SIZE | 0x40016104 | FULL | Slave region, size |
| PERI_MS_PPU_FX356_SL_ATT0 | 0x40016110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX356_SL_ATT1 | 0x40016114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX356_SL_ATT2 | 0x40016118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX356_SL_ATT3 | 0x4001611C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX356_MS_ADDR | 0x40016120 | FULL | Master region, base address |
| PERI_MS_PPU_FX356_MS_SIZE | 0x40016124 | FULL | Master region, size |
| PERI_MS_PPU_FX356_MS_ATT0 | 0x40016130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX356_MS_ATT1 | 0x40016134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX356_MS_ATT2 | 0x40016138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX356_MS_ATT3 | 0x4001613C | FULL | Master attributes 3 |

21.374 PPU_FX 357

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX357_SL_ADDR | 0x40016140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX357_SL_SIZE | 0x40016144 | FULL | Slave region, size |
| PERI_MS_PPU_FX357_SL_ATT0 | 0x40016150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX357_SL_ATT1 | 0x40016154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX357_SL_ATT2 | 0x40016158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX357_SL_ATT3 | 0x4001615C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX357_MS_ADDR | 0x40016160 | FULL | Master region, base address |
| PERI_MS_PPU_FX357_MS_SIZE | 0x40016164 | FULL | Master region, size |
| PERI_MS_PPU_FX357_MS_ATT0 | 0x40016170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX357_MS_ATT1 | 0x40016174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX357_MS_ATT2 | 0x40016178 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX357_MS_ATT3 | 0x4001617C | FULL | Master attributes 3 |

21.375 PPU_FX 358

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX358_SL_ADDR | 0x40016180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX358_SL_SIZE | 0x40016184 | FULL | Slave region, size |
| PERI_MS_PPU_FX358_SL_ATT0 | 0x40016190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX358_SL_ATT1 | 0x40016194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX358_SL_ATT2 | 0x40016198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX358_SL_ATT3 | 0x4001619C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX358_MS_ADDR | 0x400161A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX358_MS_SIZE | 0x400161A4 | FULL | Master region, size |
| PERI_MS_PPU_FX358_MS_ATT0 | 0x400161B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX358_MS_ATT1 | 0x400161B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX358_MS_ATT2 | 0x400161B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX358_MS_ATT3 | 0x400161BC | FULL | Master attributes 3 |

21.376 PPU_FX 359

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX359_SL_ADDR | 0x400161C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX359_SL_SIZE | 0x400161C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX359_SL_ATT0 | 0x400161D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX359_SL_ATT1 | 0x400161D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX359_SL_ATT2 | 0x400161D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX359_SL_ATT3 | 0x400161DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX359_MS_ADDR | 0x400161E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX359_MS_SIZE | 0x400161E4 | FULL | Master region, size |
| PERI_MS_PPU_FX359_MS_ATT0 | 0x400161F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX359_MS_ATT1 | 0x400161F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX359_MS_ATT2 | 0x400161F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX359_MS_ATT3 | 0x400161FC | FULL | Master attributes 3 |

21.377 PPU_FX 360

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX360_SL_ADDR | 0x40016200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX360_SL_SIZE | 0x40016204 | FULL | Slave region, size |
| PERI_MS_PPU_FX360_SL_ATT0 | 0x40016210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX360_SL_ATT1 | 0x40016214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX360_SL_ATT2 | 0x40016218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX360_SL_ATT3 | 0x4001621C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX360_MS_ADDR | 0x40016220 | FULL | Master region, base address |
| PERI_MS_PPU_FX360_MS_SIZE | 0x40016224 | FULL | Master region, size |
| PERI_MS_PPU_FX360_MS_ATT0 | 0x40016230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX360_MS_ATT1 | 0x40016234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX360_MS_ATT2 | 0x40016238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX360_MS_ATT3 | 0x4001623C | FULL | Master attributes 3 |

21.378 PPU_FX 361

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX361_SL_ADDR | 0x40016240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX361_SL_SIZE | 0x40016244 | FULL | Slave region, size |
| PERI_MS_PPU_FX361_SL_ATT0 | 0x40016250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX361_SL_ATT1 | 0x40016254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX361_SL_ATT2 | 0x40016258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX361_SL_ATT3 | 0x4001625C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX361_MS_ADDR | 0x40016260 | FULL | Master region, base address |
| PERI_MS_PPU_FX361_MS_SIZE | 0x40016264 | FULL | Master region, size |
| PERI_MS_PPU_FX361_MS_ATT0 | 0x40016270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX361_MS_ATT1 | 0x40016274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX361_MS_ATT2 | 0x40016278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX361_MS_ATT3 | 0x4001627C | FULL | Master attributes 3 |

21.379 PPU_FX 362

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX362_SL_ADDR | 0x40016280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX362_SL_SIZE | 0x40016284 | FULL | Slave region, size |
| PERI_MS_PPU_FX362_SL_ATT0 | 0x40016290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX362_SL_ATT1 | 0x40016294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX362_SL_ATT2 | 0x40016298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX362_SL_ATT3 | 0x4001629C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX362_MS_ADDR | 0x400162A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX362_MS_SIZE | 0x400162A4 | FULL | Master region, size |
| PERI_MS_PPU_FX362_MS_ATT0 | 0x400162B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX362_MS_ATT1 | 0x400162B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX362_MS_ATT2 | 0x400162B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX362_MS_ATT3 | 0x400162BC | FULL | Master attributes 3 |

21.380 PPU_FX 363

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX363_SL_ADDR | 0x400162C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX363_SL_SIZE | 0x400162C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX363_SL_ATT0 | 0x400162D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX363_SL_ATT1 | 0x400162D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX363_SL_ATT2 | 0x400162D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX363_SL_ATT3 | 0x400162DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX363_MS_ADDR | 0x400162E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX363_MS_SIZE | 0x400162E4 | FULL | Master region, size |
| PERI_MS_PPU_FX363_MS_ATT0 | 0x400162F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX363_MS_ATT1 | 0x400162F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX363_MS_ATT2 | 0x400162F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX363_MS_ATT3 | 0x400162FC | FULL | Master attributes 3 |

21.381 PPU_FX 364

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX364_SL_ADDR | 0x40016300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX364_SL_SIZE | 0x40016304 | FULL | Slave region, size |
| PERI_MS_PPU_FX364_SL_ATT0 | 0x40016310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX364_SL_ATT1 | 0x40016314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX364_SL_ATT2 | 0x40016318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX364_SL_ATT3 | 0x4001631C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX364_MS_ADDR | 0x40016320 | FULL | Master region, base address |
| PERI_MS_PPU_FX364_MS_SIZE | 0x40016324 | FULL | Master region, size |
| PERI_MS_PPU_FX364_MS_ATT0 | 0x40016330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX364_MS_ATT1 | 0x40016334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX364_MS_ATT2 | 0x40016338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX364_MS_ATT3 | 0x4001633C | FULL | Master attributes 3 |

21.382 PPU_FX 365

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX365_SL_ADDR | 0x40016340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX365_SL_SIZE | 0x40016344 | FULL | Slave region, size |
| PERI_MS_PPU_FX365_SL_ATT0 | 0x40016350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX365_SL_ATT1 | 0x40016354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX365_SL_ATT2 | 0x40016358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX365_SL_ATT3 | 0x4001635C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX365_MS_ADDR | 0x40016360 | FULL | Master region, base address |
| PERI_MS_PPU_FX365_MS_SIZE | 0x40016364 | FULL | Master region, size |
| PERI_MS_PPU_FX365_MS_ATT0 | 0x40016370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX365_MS_ATT1 | 0x40016374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX365_MS_ATT2 | 0x40016378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX365_MS_ATT3 | 0x4001637C | FULL | Master attributes 3 |

21.383 PPU_FX 366

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX366_SL_ADDR | 0x40016380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX366_SL_SIZE | 0x40016384 | FULL | Slave region, size |
| PERI_MS_PPU_FX366_SL_ATT0 | 0x40016390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX366_SL_ATT1 | 0x40016394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX366_SL_ATT2 | 0x40016398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX366_SL_ATT3 | 0x4001639C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX366_MS_ADDR | 0x400163A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX366_MS_SIZE | 0x400163A4 | FULL | Master region, size |
| PERI_MS_PPU_FX366_MS_ATT0 | 0x400163B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX366_MS_ATT1 | 0x400163B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX366_MS_ATT2 | 0x400163B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX366_MS_ATT3 | 0x400163BC | FULL | Master attributes 3 |

21.384 PPU_FX 367

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX367_SL_ADDR | 0x400163C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX367_SL_SIZE | 0x400163C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX367_SL_ATT0 | 0x400163D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX367_SL_ATT1 | 0x400163D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX367_SL_ATT2 | 0x400163D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX367_SL_ATT3 | 0x400163DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX367_MS_ADDR | 0x400163E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX367_MS_SIZE | 0x400163E4 | FULL | Master region, size |
| PERI_MS_PPU_FX367_MS_ATT0 | 0x400163F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX367_MS_ATT1 | 0x400163F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX367_MS_ATT2 | 0x400163F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX367_MS_ATT3 | 0x400163FC | FULL | Master attributes 3 |

21.385 PPU_FX 368

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX368_SL_ADDR | 0x40016400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX368_SL_SIZE | 0x40016404 | FULL | Slave region, size |
| PERI_MS_PPU_FX368_SL_ATT0 | 0x40016410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX368_SL_ATT1 | 0x40016414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX368_SL_ATT2 | 0x40016418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX368_SL_ATT3 | 0x4001641C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX368_MS_ADDR | 0x40016420 | FULL | Master region, base address |
| PERI_MS_PPU_FX368_MS_SIZE | 0x40016424 | FULL | Master region, size |
| PERI_MS_PPU_FX368_MS_ATT0 | 0x40016430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX368_MS_ATT1 | 0x40016434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX368_MS_ATT2 | 0x40016438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX368_MS_ATT3 | 0x4001643C | FULL | Master attributes 3 |

21.386 PPU_FX 369

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX369_SL_ADDR | 0x40016440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX369_SL_SIZE | 0x40016444 | FULL | Slave region, size |
| PERI_MS_PPU_FX369_SL_ATT0 | 0x40016450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX369_SL_ATT1 | 0x40016454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX369_SL_ATT2 | 0x40016458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX369_SL_ATT3 | 0x4001645C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX369_MS_ADDR | 0x40016460 | FULL | Master region, base address |
| PERI_MS_PPU_FX369_MS_SIZE | 0x40016464 | FULL | Master region, size |
| PERI_MS_PPU_FX369_MS_ATT0 | 0x40016470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX369_MS_ATT1 | 0x40016474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX369_MS_ATT2 | 0x40016478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX369_MS_ATT3 | 0x4001647C | FULL | Master attributes 3 |

21.387 PPU_FX 370

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX370_SL_ADDR | 0x40016480 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX370_SL_SIZE | 0x40016484 | FULL | Slave region, size |
| PERI_MS_PPU_FX370_SL_ATT0 | 0x40016490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX370_SL_ATT1 | 0x40016494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX370_SL_ATT2 | 0x40016498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX370_SL_ATT3 | 0x4001649C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX370_MS_ADDR | 0x400164A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX370_MS_SIZE | 0x400164A4 | FULL | Master region, size |
| PERI_MS_PPU_FX370_MS_ATT0 | 0x400164B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX370_MS_ATT1 | 0x400164B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX370_MS_ATT2 | 0x400164B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX370_MS_ATT3 | 0x400164BC | FULL | Master attributes 3 |

21.388 PPU_FX 371

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX371_SL_ADDR | 0x400164C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX371_SL_SIZE | 0x400164C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX371_SL_ATT0 | 0x400164D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX371_SL_ATT1 | 0x400164D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX371_SL_ATT2 | 0x400164D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX371_SL_ATT3 | 0x400164DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX371_MS_ADDR | 0x400164E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX371_MS_SIZE | 0x400164E4 | FULL | Master region, size |
| PERI_MS_PPU_FX371_MS_ATT0 | 0x400164F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX371_MS_ATT1 | 0x400164F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX371_MS_ATT2 | 0x400164F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX371_MS_ATT3 | 0x400164FC | FULL | Master attributes 3 |

21.389 PPU_FX 372

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX372_SL_ADDR | 0x40016500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX372_SL_SIZE | 0x40016504 | FULL | Slave region, size |
| PERI_MS_PPU_FX372_SL_ATT0 | 0x40016510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX372_SL_ATT1 | 0x40016514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX372_SL_ATT2 | 0x40016518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX372_SL_ATT3 | 0x4001651C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX372_MS_ADDR | 0x40016520 | FULL | Master region, base address |
| PERI_MS_PPU_FX372_MS_SIZE | 0x40016524 | FULL | Master region, size |
| PERI_MS_PPU_FX372_MS_ATT0 | 0x40016530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX372_MS_ATT1 | 0x40016534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX372_MS_ATT2 | 0x40016538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX372_MS_ATT3 | 0x4001653C | FULL | Master attributes 3 |

21.390 PPU_FX 373

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX373_SL_ADDR | 0x40016540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX373_SL_SIZE | 0x40016544 | FULL | Slave region, size |
| PERI_MS_PPU_FX373_SL_ATT0 | 0x40016550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX373_SL_ATT1 | 0x40016554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX373_SL_ATT2 | 0x40016558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX373_SL_ATT3 | 0x4001655C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX373_MS_ADDR | 0x40016560 | FULL | Master region, base address |
| PERI_MS_PPU_FX373_MS_SIZE | 0x40016564 | FULL | Master region, size |
| PERI_MS_PPU_FX373_MS_ATT0 | 0x40016570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX373_MS_ATT1 | 0x40016574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX373_MS_ATT2 | 0x40016578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX373_MS_ATT3 | 0x4001657C | FULL | Master attributes 3 |

21.391 PPU_FX 374

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX374_SL_ADDR | 0x40016580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX374_SL_SIZE | 0x40016584 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX374_SL_ATT0 | 0x40016590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX374_SL_ATT1 | 0x40016594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX374_SL_ATT2 | 0x40016598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX374_SL_ATT3 | 0x4001659C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX374_MS_ADDR | 0x400165A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX374_MS_SIZE | 0x400165A4 | FULL | Master region, size |
| PERI_MS_PPU_FX374_MS_ATT0 | 0x400165B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX374_MS_ATT1 | 0x400165B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX374_MS_ATT2 | 0x400165B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX374_MS_ATT3 | 0x400165BC | FULL | Master attributes 3 |

21.392 PPU_FX 375

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX375_SL_ADDR | 0x400165C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX375_SL_SIZE | 0x400165C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX375_SL_ATT0 | 0x400165D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX375_SL_ATT1 | 0x400165D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX375_SL_ATT2 | 0x400165D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX375_SL_ATT3 | 0x400165DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX375_MS_ADDR | 0x400165E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX375_MS_SIZE | 0x400165E4 | FULL | Master region, size |
| PERI_MS_PPU_FX375_MS_ATT0 | 0x400165F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX375_MS_ATT1 | 0x400165F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX375_MS_ATT2 | 0x400165F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX375_MS_ATT3 | 0x400165FC | FULL | Master attributes 3 |

21.393 PPU_FX 376

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX376_SL_ADDR | 0x40016600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX376_SL_SIZE | 0x40016604 | FULL | Slave region, size |
| PERI_MS_PPU_FX376_SL_ATT0 | 0x40016610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX376_SL_ATT1 | 0x40016614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX376_SL_ATT2 | 0x40016618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX376_SL_ATT3 | 0x4001661C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX376_MS_ADDR | 0x40016620 | FULL | Master region, base address |
| PERI_MS_PPU_FX376_MS_SIZE | 0x40016624 | FULL | Master region, size |
| PERI_MS_PPU_FX376_MS_ATT0 | 0x40016630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX376_MS_ATT1 | 0x40016634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX376_MS_ATT2 | 0x40016638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX376_MS_ATT3 | 0x4001663C | FULL | Master attributes 3 |

21.394 PPU_FX 377

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX377_SL_ADDR | 0x40016640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX377_SL_SIZE | 0x40016644 | FULL | Slave region, size |
| PERI_MS_PPU_FX377_SL_ATT0 | 0x40016650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX377_SL_ATT1 | 0x40016654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX377_SL_ATT2 | 0x40016658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX377_SL_ATT3 | 0x4001665C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX377_MS_ADDR | 0x40016660 | FULL | Master region, base address |
| PERI_MS_PPU_FX377_MS_SIZE | 0x40016664 | FULL | Master region, size |
| PERI_MS_PPU_FX377_MS_ATT0 | 0x40016670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX377_MS_ATT1 | 0x40016674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX377_MS_ATT2 | 0x40016678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX377_MS_ATT3 | 0x4001667C | FULL | Master attributes 3 |

21.395 PPU_FX 378

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX378_SL_ADDR | 0x40016680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX378_SL_SIZE | 0x40016684 | FULL | Slave region, size |
| PERI_MS_PPU_FX378_SL_ATT0 | 0x40016690 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX378_SL_ATT1 | 0x40016694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX378_SL_ATT2 | 0x40016698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX378_SL_ATT3 | 0x4001669C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX378_MS_ADDR | 0x400166A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX378_MS_SIZE | 0x400166A4 | FULL | Master region, size |
| PERI_MS_PPU_FX378_MS_ATT0 | 0x400166B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX378_MS_ATT1 | 0x400166B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX378_MS_ATT2 | 0x400166B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX378_MS_ATT3 | 0x400166BC | FULL | Master attributes 3 |

21.396 PPU_FX 379

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX379_SL_ADDR | 0x400166C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX379_SL_SIZE | 0x400166C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX379_SL_ATT0 | 0x400166D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX379_SL_ATT1 | 0x400166D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX379_SL_ATT2 | 0x400166D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX379_SL_ATT3 | 0x400166DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX379_MS_ADDR | 0x400166E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX379_MS_SIZE | 0x400166E4 | FULL | Master region, size |
| PERI_MS_PPU_FX379_MS_ATT0 | 0x400166F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX379_MS_ATT1 | 0x400166F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX379_MS_ATT2 | 0x400166F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX379_MS_ATT3 | 0x400166FC | FULL | Master attributes 3 |

21.397 PPU_FX 380

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX380_SL_ADDR | 0x40016700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX380_SL_SIZE | 0x40016704 | FULL | Slave region, size |
| PERI_MS_PPU_FX380_SL_ATT0 | 0x40016710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX380_SL_ATT1 | 0x40016714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX380_SL_ATT2 | 0x40016718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX380_SL_ATT3 | 0x4001671C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX380_MS_ADDR | 0x40016720 | FULL | Master region, base address |
| PERI_MS_PPU_FX380_MS_SIZE | 0x40016724 | FULL | Master region, size |
| PERI_MS_PPU_FX380_MS_ATT0 | 0x40016730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX380_MS_ATT1 | 0x40016734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX380_MS_ATT2 | 0x40016738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX380_MS_ATT3 | 0x4001673C | FULL | Master attributes 3 |

21.398 PPU_FX 381

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX381_SL_ADDR | 0x40016740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX381_SL_SIZE | 0x40016744 | FULL | Slave region, size |
| PERI_MS_PPU_FX381_SL_ATT0 | 0x40016750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX381_SL_ATT1 | 0x40016754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX381_SL_ATT2 | 0x40016758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX381_SL_ATT3 | 0x4001675C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX381_MS_ADDR | 0x40016760 | FULL | Master region, base address |
| PERI_MS_PPU_FX381_MS_SIZE | 0x40016764 | FULL | Master region, size |
| PERI_MS_PPU_FX381_MS_ATT0 | 0x40016770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX381_MS_ATT1 | 0x40016774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX381_MS_ATT2 | 0x40016778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX381_MS_ATT3 | 0x4001677C | FULL | Master attributes 3 |

21.399 PPU_FX 382

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX382_SL_ADDR | 0x40016780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX382_SL_SIZE | 0x40016784 | FULL | Slave region, size |
| PERI_MS_PPU_FX382_SL_ATT0 | 0x40016790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX382_SL_ATT1 | 0x40016794 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX382_SL_ATT2 | 0x40016798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX382_SL_ATT3 | 0x4001679C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX382_MS_ADDR | 0x400167A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX382_MS_SIZE | 0x400167A4 | FULL | Master region, size |
| PERI_MS_PPU_FX382_MS_ATT0 | 0x400167B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX382_MS_ATT1 | 0x400167B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX382_MS_ATT2 | 0x400167B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX382_MS_ATT3 | 0x400167BC | FULL | Master attributes 3 |

21.400 PPU_FX 383

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX383_SL_ADDR | 0x400167C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX383_SL_SIZE | 0x400167C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX383_SL_ATT0 | 0x400167D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX383_SL_ATT1 | 0x400167D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX383_SL_ATT2 | 0x400167D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX383_SL_ATT3 | 0x400167DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX383_MS_ADDR | 0x400167E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX383_MS_SIZE | 0x400167E4 | FULL | Master region, size |
| PERI_MS_PPU_FX383_MS_ATT0 | 0x400167F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX383_MS_ATT1 | 0x400167F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX383_MS_ATT2 | 0x400167F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX383_MS_ATT3 | 0x400167FC | FULL | Master attributes 3 |

21.401 PPU_FX 384

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX384_SL_ADDR | 0x40016800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX384_SL_SIZE | 0x40016804 | FULL | Slave region, size |
| PERI_MS_PPU_FX384_SL_ATT0 | 0x40016810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX384_SL_ATT1 | 0x40016814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX384_SL_ATT2 | 0x40016818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX384_SL_ATT3 | 0x4001681C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX384_MS_ADDR | 0x40016820 | FULL | Master region, base address |
| PERI_MS_PPU_FX384_MS_SIZE | 0x40016824 | FULL | Master region, size |
| PERI_MS_PPU_FX384_MS_ATT0 | 0x40016830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX384_MS_ATT1 | 0x40016834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX384_MS_ATT2 | 0x40016838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX384_MS_ATT3 | 0x4001683C | FULL | Master attributes 3 |

21.402 PPU_FX 385

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX385_SL_ADDR | 0x40016840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX385_SL_SIZE | 0x40016844 | FULL | Slave region, size |
| PERI_MS_PPU_FX385_SL_ATT0 | 0x40016850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX385_SL_ATT1 | 0x40016854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX385_SL_ATT2 | 0x40016858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX385_SL_ATT3 | 0x4001685C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX385_MS_ADDR | 0x40016860 | FULL | Master region, base address |
| PERI_MS_PPU_FX385_MS_SIZE | 0x40016864 | FULL | Master region, size |
| PERI_MS_PPU_FX385_MS_ATT0 | 0x40016870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX385_MS_ATT1 | 0x40016874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX385_MS_ATT2 | 0x40016878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX385_MS_ATT3 | 0x4001687C | FULL | Master attributes 3 |

21.403 PPU_FX 386

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX386_SL_ADDR | 0x40016880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX386_SL_SIZE | 0x40016884 | FULL | Slave region, size |
| PERI_MS_PPU_FX386_SL_ATT0 | 0x40016890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX386_SL_ATT1 | 0x40016894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX386_SL_ATT2 | 0x40016898 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX386_SL_ATT3 | 0x4001689C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX386_MS_ADDR | 0x400168A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX386_MS_SIZE | 0x400168A4 | FULL | Master region, size |
| PERI_MS_PPU_FX386_MS_ATT0 | 0x400168B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX386_MS_ATT1 | 0x400168B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX386_MS_ATT2 | 0x400168B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX386_MS_ATT3 | 0x400168BC | FULL | Master attributes 3 |

21.404 PPU_FX 387

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX387_SL_ADDR | 0x400168C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX387_SL_SIZE | 0x400168C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX387_SL_ATT0 | 0x400168D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX387_SL_ATT1 | 0x400168D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX387_SL_ATT2 | 0x400168D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX387_SL_ATT3 | 0x400168DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX387_MS_ADDR | 0x400168E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX387_MS_SIZE | 0x400168E4 | FULL | Master region, size |
| PERI_MS_PPU_FX387_MS_ATT0 | 0x400168F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX387_MS_ATT1 | 0x400168F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX387_MS_ATT2 | 0x400168F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX387_MS_ATT3 | 0x400168FC | FULL | Master attributes 3 |

21.405 PPU_FX 388

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX388_SL_ADDR | 0x40016900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX388_SL_SIZE | 0x40016904 | FULL | Slave region, size |
| PERI_MS_PPU_FX388_SL_ATT0 | 0x40016910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX388_SL_ATT1 | 0x40016914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX388_SL_ATT2 | 0x40016918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX388_SL_ATT3 | 0x4001691C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX388_MS_ADDR | 0x40016920 | FULL | Master region, base address |
| PERI_MS_PPU_FX388_MS_SIZE | 0x40016924 | FULL | Master region, size |
| PERI_MS_PPU_FX388_MS_ATT0 | 0x40016930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX388_MS_ATT1 | 0x40016934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX388_MS_ATT2 | 0x40016938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX388_MS_ATT3 | 0x4001693C | FULL | Master attributes 3 |

21.406 PPU_FX 389

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX389_SL_ADDR | 0x40016940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX389_SL_SIZE | 0x40016944 | FULL | Slave region, size |
| PERI_MS_PPU_FX389_SL_ATT0 | 0x40016950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX389_SL_ATT1 | 0x40016954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX389_SL_ATT2 | 0x40016958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX389_SL_ATT3 | 0x4001695C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX389_MS_ADDR | 0x40016960 | FULL | Master region, base address |
| PERI_MS_PPU_FX389_MS_SIZE | 0x40016964 | FULL | Master region, size |
| PERI_MS_PPU_FX389_MS_ATT0 | 0x40016970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX389_MS_ATT1 | 0x40016974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX389_MS_ATT2 | 0x40016978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX389_MS_ATT3 | 0x4001697C | FULL | Master attributes 3 |

21.407 PPU_FX 390

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX390_SL_ADDR | 0x40016980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX390_SL_SIZE | 0x40016984 | FULL | Slave region, size |
| PERI_MS_PPU_FX390_SL_ATT0 | 0x40016990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX390_SL_ATT1 | 0x40016994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX390_SL_ATT2 | 0x40016998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX390_SL_ATT3 | 0x4001699C | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX390_MS_ADDR | 0x400169A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX390_MS_SIZE | 0x400169A4 | FULL | Master region, size |
| PERI_MS_PPU_FX390_MS_ATT0 | 0x400169B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX390_MS_ATT1 | 0x400169B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX390_MS_ATT2 | 0x400169B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX390_MS_ATT3 | 0x400169BC | FULL | Master attributes 3 |

21.408 PPU_FX 391

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX391_SL_ADDR | 0x400169C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX391_SL_SIZE | 0x400169C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX391_SL_ATT0 | 0x400169D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX391_SL_ATT1 | 0x400169D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX391_SL_ATT2 | 0x400169D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX391_SL_ATT3 | 0x400169DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX391_MS_ADDR | 0x400169E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX391_MS_SIZE | 0x400169E4 | FULL | Master region, size |
| PERI_MS_PPU_FX391_MS_ATT0 | 0x400169F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX391_MS_ATT1 | 0x400169F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX391_MS_ATT2 | 0x400169F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX391_MS_ATT3 | 0x400169FC | FULL | Master attributes 3 |

21.409 PPU_FX 392

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX392_SL_ADDR | 0x40016A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX392_SL_SIZE | 0x40016A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX392_SL_ATT0 | 0x40016A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX392_SL_ATT1 | 0x40016A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX392_SL_ATT2 | 0x40016A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX392_SL_ATT3 | 0x40016A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX392_MS_ADDR | 0x40016A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX392_MS_SIZE | 0x40016A24 | FULL | Master region, size |
| PERI_MS_PPU_FX392_MS_ATT0 | 0x40016A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX392_MS_ATT1 | 0x40016A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX392_MS_ATT2 | 0x40016A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX392_MS_ATT3 | 0x40016A3C | FULL | Master attributes 3 |

21.410 PPU_FX 393

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX393_SL_ADDR | 0x40016A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX393_SL_SIZE | 0x40016A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX393_SL_ATT0 | 0x40016A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX393_SL_ATT1 | 0x40016A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX393_SL_ATT2 | 0x40016A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX393_SL_ATT3 | 0x40016A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX393_MS_ADDR | 0x40016A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX393_MS_SIZE | 0x40016A64 | FULL | Master region, size |
| PERI_MS_PPU_FX393_MS_ATT0 | 0x40016A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX393_MS_ATT1 | 0x40016A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX393_MS_ATT2 | 0x40016A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX393_MS_ATT3 | 0x40016A7C | FULL | Master attributes 3 |

21.411 PPU_FX 394

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX394_SL_ADDR | 0x40016A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX394_SL_SIZE | 0x40016A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX394_SL_ATT0 | 0x40016A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX394_SL_ATT1 | 0x40016A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX394_SL_ATT2 | 0x40016A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX394_SL_ATT3 | 0x40016A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX394_MS_ADDR | 0x40016AA0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX394_MS_SIZE | 0x40016AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX394_MS_ATT0 | 0x40016AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX394_MS_ATT1 | 0x40016AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX394_MS_ATT2 | 0x40016AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX394_MS_ATT3 | 0x40016ABC | FULL | Master attributes 3 |

21.412 PPU_FX 395

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX395_SL_ADDR | 0x40016AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX395_SL_SIZE | 0x40016AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX395_SL_ATT0 | 0x40016AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX395_SL_ATT1 | 0x40016AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX395_SL_ATT2 | 0x40016AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX395_SL_ATT3 | 0x40016ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX395_MS_ADDR | 0x40016AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX395_MS_SIZE | 0x40016AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX395_MS_ATT0 | 0x40016AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX395_MS_ATT1 | 0x40016AF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX395_MS_ATT2 | 0x40016AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX395_MS_ATT3 | 0x40016AFC | FULL | Master attributes 3 |

21.413 PPU_FX 396

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX396_SL_ADDR | 0x40016B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX396_SL_SIZE | 0x40016B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX396_SL_ATT0 | 0x40016B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX396_SL_ATT1 | 0x40016B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX396_SL_ATT2 | 0x40016B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX396_SL_ATT3 | 0x40016B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX396_MS_ADDR | 0x40016B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX396_MS_SIZE | 0x40016B24 | FULL | Master region, size |
| PERI_MS_PPU_FX396_MS_ATT0 | 0x40016B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX396_MS_ATT1 | 0x40016B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX396_MS_ATT2 | 0x40016B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX396_MS_ATT3 | 0x40016B3C | FULL | Master attributes 3 |

21.414 PPU_FX 397

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX397_SL_ADDR | 0x40016B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX397_SL_SIZE | 0x40016B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX397_SL_ATT0 | 0x40016B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX397_SL_ATT1 | 0x40016B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX397_SL_ATT2 | 0x40016B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX397_SL_ATT3 | 0x40016B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX397_MS_ADDR | 0x40016B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX397_MS_SIZE | 0x40016B64 | FULL | Master region, size |
| PERI_MS_PPU_FX397_MS_ATT0 | 0x40016B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX397_MS_ATT1 | 0x40016B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX397_MS_ATT2 | 0x40016B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX397_MS_ATT3 | 0x40016B7C | FULL | Master attributes 3 |

21.415 PPU_FX 398

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX398_SL_ADDR | 0x40016B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX398_SL_SIZE | 0x40016B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX398_SL_ATT0 | 0x40016B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX398_SL_ATT1 | 0x40016B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX398_SL_ATT2 | 0x40016B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX398_SL_ATT3 | 0x40016B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX398_MS_ADDR | 0x40016BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX398_MS_SIZE | 0x40016BA4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX398_MS_ATT0 | 0x40016BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX398_MS_ATT1 | 0x40016BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX398_MS_ATT2 | 0x40016BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX398_MS_ATT3 | 0x40016BBC | FULL | Master attributes 3 |

21.416 PPU_FX 399

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX399_SL_ADDR | 0x40016BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX399_SL_SIZE | 0x40016BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX399_SL_ATT0 | 0x40016BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX399_SL_ATT1 | 0x40016BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX399_SL_ATT2 | 0x40016BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX399_SL_ATT3 | 0x40016BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX399_MS_ADDR | 0x40016BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX399_MS_SIZE | 0x40016BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX399_MS_ATT0 | 0x40016BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX399_MS_ATT1 | 0x40016BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX399_MS_ATT2 | 0x40016BF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX399_MS_ATT3 | 0x40016BFC | FULL | Master attributes 3 |

21.417 PPU_FX 400

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX400_SL_ADDR | 0x40016C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX400_SL_SIZE | 0x40016C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX400_SL_ATT0 | 0x40016C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX400_SL_ATT1 | 0x40016C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX400_SL_ATT2 | 0x40016C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX400_SL_ATT3 | 0x40016C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX400_MS_ADDR | 0x40016C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX400_MS_SIZE | 0x40016C24 | FULL | Master region, size |
| PERI_MS_PPU_FX400_MS_ATT0 | 0x40016C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX400_MS_ATT1 | 0x40016C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX400_MS_ATT2 | 0x40016C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX400_MS_ATT3 | 0x40016C3C | FULL | Master attributes 3 |

21.418 PPU_FX 401

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX401_SL_ADDR | 0x40016C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX401_SL_SIZE | 0x40016C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX401_SL_ATT0 | 0x40016C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX401_SL_ATT1 | 0x40016C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX401_SL_ATT2 | 0x40016C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX401_SL_ATT3 | 0x40016C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX401_MS_ADDR | 0x40016C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX401_MS_SIZE | 0x40016C64 | FULL | Master region, size |
| PERI_MS_PPU_FX401_MS_ATT0 | 0x40016C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX401_MS_ATT1 | 0x40016C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX401_MS_ATT2 | 0x40016C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX401_MS_ATT3 | 0x40016C7C | FULL | Master attributes 3 |

21.419 PPU_FX 402

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX402_SL_ADDR | 0x40016C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX402_SL_SIZE | 0x40016C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX402_SL_ATT0 | 0x40016C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX402_SL_ATT1 | 0x40016C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX402_SL_ATT2 | 0x40016C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX402_SL_ATT3 | 0x40016C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX402_MS_ADDR | 0x40016CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX402_MS_SIZE | 0x40016CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX402_MS_ATT0 | 0x40016CB0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX402_MS_ATT1 | 0x40016CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX402_MS_ATT2 | 0x40016CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX402_MS_ATT3 | 0x40016CBC | FULL | Master attributes 3 |

21.420 PPU_FX 403

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX403_SL_ADDR | 0x40016CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX403_SL_SIZE | 0x40016CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX403_SL_ATT0 | 0x40016CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX403_SL_ATT1 | 0x40016CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX403_SL_ATT2 | 0x40016CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX403_SL_ATT3 | 0x40016CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX403_MS_ADDR | 0x40016CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX403_MS_SIZE | 0x40016CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX403_MS_ATT0 | 0x40016CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX403_MS_ATT1 | 0x40016CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX403_MS_ATT2 | 0x40016CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX403_MS_ATT3 | 0x40016CFC | FULL | Master attributes 3 |

21.421 PPU_FX 404

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX404_SL_ADDR | 0x40016D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX404_SL_SIZE | 0x40016D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX404_SL_ATT0 | 0x40016D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX404_SL_ATT1 | 0x40016D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX404_SL_ATT2 | 0x40016D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX404_SL_ATT3 | 0x40016D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX404_MS_ADDR | 0x40016D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX404_MS_SIZE | 0x40016D24 | FULL | Master region, size |
| PERI_MS_PPU_FX404_MS_ATT0 | 0x40016D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX404_MS_ATT1 | 0x40016D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX404_MS_ATT2 | 0x40016D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX404_MS_ATT3 | 0x40016D3C | FULL | Master attributes 3 |

21.422 PPU_FX 405

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX405_SL_ADDR | 0x40016D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX405_SL_SIZE | 0x40016D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX405_SL_ATT0 | 0x40016D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX405_SL_ATT1 | 0x40016D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX405_SL_ATT2 | 0x40016D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX405_SL_ATT3 | 0x40016D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX405_MS_ADDR | 0x40016D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX405_MS_SIZE | 0x40016D64 | FULL | Master region, size |
| PERI_MS_PPU_FX405_MS_ATT0 | 0x40016D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX405_MS_ATT1 | 0x40016D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX405_MS_ATT2 | 0x40016D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX405_MS_ATT3 | 0x40016D7C | FULL | Master attributes 3 |

21.423 PPU_FX 406

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX406_SL_ADDR | 0x40016D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX406_SL_SIZE | 0x40016D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX406_SL_ATT0 | 0x40016D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX406_SL_ATT1 | 0x40016D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX406_SL_ATT2 | 0x40016D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX406_SL_ATT3 | 0x40016D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX406_MS_ADDR | 0x40016DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX406_MS_SIZE | 0x40016DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX406_MS_ATT0 | 0x40016DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX406_MS_ATT1 | 0x40016DB4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX406_MS_ATT2 | 0x40016DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX406_MS_ATT3 | 0x40016DBC | FULL | Master attributes 3 |

21.424 PPU_FX 407

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX407_SL_ADDR | 0x40016DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX407_SL_SIZE | 0x40016DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX407_SL_ATT0 | 0x40016DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX407_SL_ATT1 | 0x40016DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX407_SL_ATT2 | 0x40016DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX407_SL_ATT3 | 0x40016DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX407_MS_ADDR | 0x40016DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX407_MS_SIZE | 0x40016DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX407_MS_ATT0 | 0x40016DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX407_MS_ATT1 | 0x40016DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX407_MS_ATT2 | 0x40016DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX407_MS_ATT3 | 0x40016DFC | FULL | Master attributes 3 |

21.425 PPU_FX 408

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX408_SL_ADDR | 0x40016E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX408_SL_SIZE | 0x40016E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX408_SL_ATT0 | 0x40016E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX408_SL_ATT1 | 0x40016E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX408_SL_ATT2 | 0x40016E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX408_SL_ATT3 | 0x40016E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX408_MS_ADDR | 0x40016E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX408_MS_SIZE | 0x40016E24 | FULL | Master region, size |
| PERI_MS_PPU_FX408_MS_ATT0 | 0x40016E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX408_MS_ATT1 | 0x40016E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX408_MS_ATT2 | 0x40016E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX408_MS_ATT3 | 0x40016E3C | FULL | Master attributes 3 |

21.426 PPU_FX 409

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX409_SL_ADDR | 0x40016E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX409_SL_SIZE | 0x40016E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX409_SL_ATT0 | 0x40016E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX409_SL_ATT1 | 0x40016E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX409_SL_ATT2 | 0x40016E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX409_SL_ATT3 | 0x40016E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX409_MS_ADDR | 0x40016E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX409_MS_SIZE | 0x40016E64 | FULL | Master region, size |
| PERI_MS_PPU_FX409_MS_ATT0 | 0x40016E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX409_MS_ATT1 | 0x40016E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX409_MS_ATT2 | 0x40016E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX409_MS_ATT3 | 0x40016E7C | FULL | Master attributes 3 |

21.427 PPU_FX 410

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX410_SL_ADDR | 0x40016E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX410_SL_SIZE | 0x40016E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX410_SL_ATT0 | 0x40016E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX410_SL_ATT1 | 0x40016E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX410_SL_ATT2 | 0x40016E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX410_SL_ATT3 | 0x40016E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX410_MS_ADDR | 0x40016EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX410_MS_SIZE | 0x40016EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX410_MS_ATT0 | 0x40016EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX410_MS_ATT1 | 0x40016EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX410_MS_ATT2 | 0x40016EB8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX410_MS_ATT3 | 0x40016EBC | FULL | Master attributes 3 |

21.428 PPU_FX 411

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX411_SL_ADDR | 0x40016EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX411_SL_SIZE | 0x40016EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX411_SL_ATT0 | 0x40016ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX411_SL_ATT1 | 0x40016ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX411_SL_ATT2 | 0x40016ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX411_SL_ATT3 | 0x40016EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX411_MS_ADDR | 0x40016EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX411_MS_SIZE | 0x40016EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX411_MS_ATT0 | 0x40016EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX411_MS_ATT1 | 0x40016EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX411_MS_ATT2 | 0x40016EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX411_MS_ATT3 | 0x40016EFC | FULL | Master attributes 3 |

21.429 PPU_FX 412

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX412_SL_ADDR | 0x40016F00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX412_SL_SIZE | 0x40016F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX412_SL_ATT0 | 0x40016F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX412_SL_ATT1 | 0x40016F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX412_SL_ATT2 | 0x40016F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX412_SL_ATT3 | 0x40016F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX412_MS_ADDR | 0x40016F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX412_MS_SIZE | 0x40016F24 | FULL | Master region, size |
| PERI_MS_PPU_FX412_MS_ATT0 | 0x40016F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX412_MS_ATT1 | 0x40016F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX412_MS_ATT2 | 0x40016F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX412_MS_ATT3 | 0x40016F3C | FULL | Master attributes 3 |

21.430 PPU_FX 413

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX413_SL_ADDR | 0x40016F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX413_SL_SIZE | 0x40016F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX413_SL_ATT0 | 0x40016F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX413_SL_ATT1 | 0x40016F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX413_SL_ATT2 | 0x40016F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX413_SL_ATT3 | 0x40016F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX413_MS_ADDR | 0x40016F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX413_MS_SIZE | 0x40016F64 | FULL | Master region, size |
| PERI_MS_PPU_FX413_MS_ATT0 | 0x40016F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX413_MS_ATT1 | 0x40016F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX413_MS_ATT2 | 0x40016F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX413_MS_ATT3 | 0x40016F7C | FULL | Master attributes 3 |

21.431 PPU_FX 414

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX414_SL_ADDR | 0x40016F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX414_SL_SIZE | 0x40016F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX414_SL_ATT0 | 0x40016F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX414_SL_ATT1 | 0x40016F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX414_SL_ATT2 | 0x40016F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX414_SL_ATT3 | 0x40016F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX414_MS_ADDR | 0x40016FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX414_MS_SIZE | 0x40016FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX414_MS_ATT0 | 0x40016FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX414_MS_ATT1 | 0x40016FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX414_MS_ATT2 | 0x40016FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX414_MS_ATT3 | 0x40016FBC | FULL | Master attributes 3 |

21.432 PPU_FX 415

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX415_SL_ADDR | 0x40016FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX415_SL_SIZE | 0x40016FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX415_SL_ATT0 | 0x40016FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX415_SL_ATT1 | 0x40016FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX415_SL_ATT2 | 0x40016FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX415_SL_ATT3 | 0x40016FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX415_MS_ADDR | 0x40016FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX415_MS_SIZE | 0x40016FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX415_MS_ATT0 | 0x40016FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX415_MS_ATT1 | 0x40016FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX415_MS_ATT2 | 0x40016FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX415_MS_ATT3 | 0x40016FFC | FULL | Master attributes 3 |

21.433 PPU_FX 416

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX416_SL_ADDR | 0x40017000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX416_SL_SIZE | 0x40017004 | FULL | Slave region, size |
| PERI_MS_PPU_FX416_SL_ATT0 | 0x40017010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX416_SL_ATT1 | 0x40017014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX416_SL_ATT2 | 0x40017018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX416_SL_ATT3 | 0x4001701C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX416_MS_ADDR | 0x40017020 | FULL | Master region, base address |
| PERI_MS_PPU_FX416_MS_SIZE | 0x40017024 | FULL | Master region, size |
| PERI_MS_PPU_FX416_MS_ATT0 | 0x40017030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX416_MS_ATT1 | 0x40017034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX416_MS_ATT2 | 0x40017038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX416_MS_ATT3 | 0x4001703C | FULL | Master attributes 3 |

21.434 PPU_FX 417

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX417_SL_ADDR | 0x40017040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX417_SL_SIZE | 0x40017044 | FULL | Slave region, size |
| PERI_MS_PPU_FX417_SL_ATT0 | 0x40017050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX417_SL_ATT1 | 0x40017054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX417_SL_ATT2 | 0x40017058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX417_SL_ATT3 | 0x4001705C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX417_MS_ADDR | 0x40017060 | FULL | Master region, base address |
| PERI_MS_PPU_FX417_MS_SIZE | 0x40017064 | FULL | Master region, size |
| PERI_MS_PPU_FX417_MS_ATT0 | 0x40017070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX417_MS_ATT1 | 0x40017074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX417_MS_ATT2 | 0x40017078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX417_MS_ATT3 | 0x4001707C | FULL | Master attributes 3 |

21.435 PPU_FX 418

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX418_SL_ADDR | 0x40017080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX418_SL_SIZE | 0x40017084 | FULL | Slave region, size |
| PERI_MS_PPU_FX418_SL_ATT0 | 0x40017090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX418_SL_ATT1 | 0x40017094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX418_SL_ATT2 | 0x40017098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX418_SL_ATT3 | 0x4001709C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX418_MS_ADDR | 0x400170A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX418_MS_SIZE | 0x400170A4 | FULL | Master region, size |
| PERI_MS_PPU_FX418_MS_ATT0 | 0x400170B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX418_MS_ATT1 | 0x400170B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX418_MS_ATT2 | 0x400170B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX418_MS_ATT3 | 0x400170BC | FULL | Master attributes 3 |

21.436 PPU_FX 419

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX419_SL_ADDR | 0x400170C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX419_SL_SIZE | 0x400170C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX419_SL_ATT0 | 0x400170D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX419_SL_ATT1 | 0x400170D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX419_SL_ATT2 | 0x400170D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX419_SL_ATT3 | 0x400170DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX419_MS_ADDR | 0x400170E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX419_MS_SIZE | 0x400170E4 | FULL | Master region, size |
| PERI_MS_PPU_FX419_MS_ATT0 | 0x400170F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX419_MS_ATT1 | 0x400170F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX419_MS_ATT2 | 0x400170F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX419_MS_ATT3 | 0x400170FC | FULL | Master attributes 3 |

21.437 PPU_FX 420

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX420_SL_ADDR | 0x40017100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX420_SL_SIZE | 0x40017104 | FULL | Slave region, size |
| PERI_MS_PPU_FX420_SL_ATT0 | 0x40017110 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX420_SL_ATT1 | 0x40017114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX420_SL_ATT2 | 0x40017118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX420_SL_ATT3 | 0x4001711C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX420_MS_ADDR | 0x40017120 | FULL | Master region, base address |
| PERI_MS_PPU_FX420_MS_SIZE | 0x40017124 | FULL | Master region, size |
| PERI_MS_PPU_FX420_MS_ATT0 | 0x40017130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX420_MS_ATT1 | 0x40017134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX420_MS_ATT2 | 0x40017138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX420_MS_ATT3 | 0x4001713C | FULL | Master attributes 3 |

21.438 PPU_FX 421

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX421_SL_ADDR | 0x40017140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX421_SL_SIZE | 0x40017144 | FULL | Slave region, size |
| PERI_MS_PPU_FX421_SL_ATT0 | 0x40017150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX421_SL_ATT1 | 0x40017154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX421_SL_ATT2 | 0x40017158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX421_SL_ATT3 | 0x4001715C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX421_MS_ADDR | 0x40017160 | FULL | Master region, base address |
| PERI_MS_PPU_FX421_MS_SIZE | 0x40017164 | FULL | Master region, size |
| PERI_MS_PPU_FX421_MS_ATT0 | 0x40017170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX421_MS_ATT1 | 0x40017174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX421_MS_ATT2 | 0x40017178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX421_MS_ATT3 | 0x4001717C | FULL | Master attributes 3 |

21.439 PPU_FX 422

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX422_SL_ADDR | 0x40017180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX422_SL_SIZE | 0x40017184 | FULL | Slave region, size |
| PERI_MS_PPU_FX422_SL_ATT0 | 0x40017190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX422_SL_ATT1 | 0x40017194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX422_SL_ATT2 | 0x40017198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX422_SL_ATT3 | 0x4001719C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX422_MS_ADDR | 0x400171A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX422_MS_SIZE | 0x400171A4 | FULL | Master region, size |
| PERI_MS_PPU_FX422_MS_ATT0 | 0x400171B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX422_MS_ATT1 | 0x400171B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX422_MS_ATT2 | 0x400171B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX422_MS_ATT3 | 0x400171BC | FULL | Master attributes 3 |

21.440 PPU_FX 423

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX423_SL_ADDR | 0x400171C0 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX423_SL_SIZE | 0x400171C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX423_SL_ATT0 | 0x400171D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX423_SL_ATT1 | 0x400171D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX423_SL_ATT2 | 0x400171D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX423_SL_ATT3 | 0x400171DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX423_MS_ADDR | 0x400171E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX423_MS_SIZE | 0x400171E4 | FULL | Master region, size |
| PERI_MS_PPU_FX423_MS_ATT0 | 0x400171F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX423_MS_ATT1 | 0x400171F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX423_MS_ATT2 | 0x400171F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX423_MS_ATT3 | 0x400171FC | FULL | Master attributes 3 |

21.441 PPU_FX 424

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX424_SL_ADDR | 0x40017200 | FULL | Slave region, base address |
| PERI_MS_PPU_FX424_SL_SIZE | 0x40017204 | FULL | Slave region, size |
| PERI_MS_PPU_FX424_SL_ATT0 | 0x40017210 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX424_SL_ATT1 | 0x40017214 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX424_SL_ATT2 | 0x40017218 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX424_SL_ATT3 | 0x4001721C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX424_MS_ADDR | 0x40017220 | FULL | Master region, base address |
| PERI_MS_PPU_FX424_MS_SIZE | 0x40017224 | FULL | Master region, size |
| PERI_MS_PPU_FX424_MS_ATT0 | 0x40017230 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX424_MS_ATT1 | 0x40017234 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX424_MS_ATT2 | 0x40017238 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX424_MS_ATT3 | 0x4001723C | FULL | Master attributes 3 |

21.442 PPU_FX 425

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX425_SL_ADDR | 0x40017240 | FULL | Slave region, base address |
| PERI_MS_PPU_FX425_SL_SIZE | 0x40017244 | FULL | Slave region, size |
| PERI_MS_PPU_FX425_SL_ATT0 | 0x40017250 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX425_SL_ATT1 | 0x40017254 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX425_SL_ATT2 | 0x40017258 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX425_SL_ATT3 | 0x4001725C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX425_MS_ADDR | 0x40017260 | FULL | Master region, base address |
| PERI_MS_PPU_FX425_MS_SIZE | 0x40017264 | FULL | Master region, size |
| PERI_MS_PPU_FX425_MS_ATT0 | 0x40017270 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX425_MS_ATT1 | 0x40017274 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX425_MS_ATT2 | 0x40017278 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX425_MS_ATT3 | 0x4001727C | FULL | Master attributes 3 |

21.443 PPU_FX 426

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX426_SL_ADDR | 0x40017280 | FULL | Slave region, base address |
| PERI_MS_PPU_FX426_SL_SIZE | 0x40017284 | FULL | Slave region, size |
| PERI_MS_PPU_FX426_SL_ATT0 | 0x40017290 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX426_SL_ATT1 | 0x40017294 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX426_SL_ATT2 | 0x40017298 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX426_SL_ATT3 | 0x4001729C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX426_MS_ADDR | 0x400172A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX426_MS_SIZE | 0x400172A4 | FULL | Master region, size |
| PERI_MS_PPU_FX426_MS_ATT0 | 0x400172B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX426_MS_ATT1 | 0x400172B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX426_MS_ATT2 | 0x400172B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX426_MS_ATT3 | 0x400172BC | FULL | Master attributes 3 |

21.444 PPU_FX 427

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX427_SL_ADDR | 0x400172C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX427_SL_SIZE | 0x400172C4 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX427_SL_ATT0 | 0x400172D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX427_SL_ATT1 | 0x400172D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX427_SL_ATT2 | 0x400172D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX427_SL_ATT3 | 0x400172DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX427_MS_ADDR | 0x400172E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX427_MS_SIZE | 0x400172E4 | FULL | Master region, size |
| PERI_MS_PPU_FX427_MS_ATT0 | 0x400172F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX427_MS_ATT1 | 0x400172F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX427_MS_ATT2 | 0x400172F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX427_MS_ATT3 | 0x400172FC | FULL | Master attributes 3 |

21.445 PPU_FX 428

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX428_SL_ADDR | 0x40017300 | FULL | Slave region, base address |
| PERI_MS_PPU_FX428_SL_SIZE | 0x40017304 | FULL | Slave region, size |
| PERI_MS_PPU_FX428_SL_ATT0 | 0x40017310 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX428_SL_ATT1 | 0x40017314 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX428_SL_ATT2 | 0x40017318 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX428_SL_ATT3 | 0x4001731C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX428_MS_ADDR | 0x40017320 | FULL | Master region, base address |
| PERI_MS_PPU_FX428_MS_SIZE | 0x40017324 | FULL | Master region, size |
| PERI_MS_PPU_FX428_MS_ATT0 | 0x40017330 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX428_MS_ATT1 | 0x40017334 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX428_MS_ATT2 | 0x40017338 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX428_MS_ATT3 | 0x4001733C | FULL | Master attributes 3 |

21.446 PPU_FX 429

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX429_SL_ADDR | 0x40017340 | FULL | Slave region, base address |
| PERI_MS_PPU_FX429_SL_SIZE | 0x40017344 | FULL | Slave region, size |
| PERI_MS_PPU_FX429_SL_ATT0 | 0x40017350 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX429_SL_ATT1 | 0x40017354 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX429_SL_ATT2 | 0x40017358 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX429_SL_ATT3 | 0x4001735C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX429_MS_ADDR | 0x40017360 | FULL | Master region, base address |
| PERI_MS_PPU_FX429_MS_SIZE | 0x40017364 | FULL | Master region, size |
| PERI_MS_PPU_FX429_MS_ATT0 | 0x40017370 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX429_MS_ATT1 | 0x40017374 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX429_MS_ATT2 | 0x40017378 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX429_MS_ATT3 | 0x4001737C | FULL | Master attributes 3 |

21.447 PPU_FX 430

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX430_SL_ADDR | 0x40017380 | FULL | Slave region, base address |
| PERI_MS_PPU_FX430_SL_SIZE | 0x40017384 | FULL | Slave region, size |
| PERI_MS_PPU_FX430_SL_ATT0 | 0x40017390 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX430_SL_ATT1 | 0x40017394 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX430_SL_ATT2 | 0x40017398 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX430_SL_ATT3 | 0x4001739C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX430_MS_ADDR | 0x400173A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX430_MS_SIZE | 0x400173A4 | FULL | Master region, size |
| PERI_MS_PPU_FX430_MS_ATT0 | 0x400173B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX430_MS_ATT1 | 0x400173B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX430_MS_ATT2 | 0x400173B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX430_MS_ATT3 | 0x400173BC | FULL | Master attributes 3 |

21.448 PPU_FX 431

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX431_SL_ADDR | 0x400173C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX431_SL_SIZE | 0x400173C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX431_SL_ATT0 | 0x400173D0 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX431_SL_ATT1 | 0x400173D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX431_SL_ATT2 | 0x400173D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX431_SL_ATT3 | 0x400173DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX431_MS_ADDR | 0x400173E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX431_MS_SIZE | 0x400173E4 | FULL | Master region, size |
| PERI_MS_PPU_FX431_MS_ATT0 | 0x400173F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX431_MS_ATT1 | 0x400173F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX431_MS_ATT2 | 0x400173F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX431_MS_ATT3 | 0x400173FC | FULL | Master attributes 3 |

21.449 PPU_FX 432

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX432_SL_ADDR | 0x40017400 | FULL | Slave region, base address |
| PERI_MS_PPU_FX432_SL_SIZE | 0x40017404 | FULL | Slave region, size |
| PERI_MS_PPU_FX432_SL_ATT0 | 0x40017410 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX432_SL_ATT1 | 0x40017414 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX432_SL_ATT2 | 0x40017418 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX432_SL_ATT3 | 0x4001741C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX432_MS_ADDR | 0x40017420 | FULL | Master region, base address |
| PERI_MS_PPU_FX432_MS_SIZE | 0x40017424 | FULL | Master region, size |
| PERI_MS_PPU_FX432_MS_ATT0 | 0x40017430 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX432_MS_ATT1 | 0x40017434 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX432_MS_ATT2 | 0x40017438 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX432_MS_ATT3 | 0x4001743C | FULL | Master attributes 3 |

21.450 PPU_FX 433

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX433_SL_ADDR | 0x40017440 | FULL | Slave region, base address |
| PERI_MS_PPU_FX433_SL_SIZE | 0x40017444 | FULL | Slave region, size |
| PERI_MS_PPU_FX433_SL_ATT0 | 0x40017450 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX433_SL_ATT1 | 0x40017454 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX433_SL_ATT2 | 0x40017458 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX433_SL_ATT3 | 0x4001745C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX433_MS_ADDR | 0x40017460 | FULL | Master region, base address |
| PERI_MS_PPU_FX433_MS_SIZE | 0x40017464 | FULL | Master region, size |
| PERI_MS_PPU_FX433_MS_ATT0 | 0x40017470 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX433_MS_ATT1 | 0x40017474 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX433_MS_ATT2 | 0x40017478 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX433_MS_ATT3 | 0x4001747C | FULL | Master attributes 3 |

21.451 PPU_FX 434

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX434_SL_ADDR | 0x40017480 | FULL | Slave region, base address |
| PERI_MS_PPU_FX434_SL_SIZE | 0x40017484 | FULL | Slave region, size |
| PERI_MS_PPU_FX434_SL_ATT0 | 0x40017490 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX434_SL_ATT1 | 0x40017494 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX434_SL_ATT2 | 0x40017498 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX434_SL_ATT3 | 0x4001749C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX434_MS_ADDR | 0x400174A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX434_MS_SIZE | 0x400174A4 | FULL | Master region, size |
| PERI_MS_PPU_FX434_MS_ATT0 | 0x400174B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX434_MS_ATT1 | 0x400174B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX434_MS_ATT2 | 0x400174B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX434_MS_ATT3 | 0x400174BC | FULL | Master attributes 3 |

21.452 PPU_FX 435

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX435_SL_ADDR | 0x400174C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX435_SL_SIZE | 0x400174C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX435_SL_ATT0 | 0x400174D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX435_SL_ATT1 | 0x400174D4 | FULL | Slave attributes 1 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX435_SL_ATT2 | 0x400174D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX435_SL_ATT3 | 0x400174DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX435_MS_ADDR | 0x400174E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX435_MS_SIZE | 0x400174E4 | FULL | Master region, size |
| PERI_MS_PPU_FX435_MS_ATT0 | 0x400174F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX435_MS_ATT1 | 0x400174F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX435_MS_ATT2 | 0x400174F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX435_MS_ATT3 | 0x400174FC | FULL | Master attributes 3 |

21.453 PPU_FX 436

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX436_SL_ADDR | 0x40017500 | FULL | Slave region, base address |
| PERI_MS_PPU_FX436_SL_SIZE | 0x40017504 | FULL | Slave region, size |
| PERI_MS_PPU_FX436_SL_ATT0 | 0x40017510 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX436_SL_ATT1 | 0x40017514 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX436_SL_ATT2 | 0x40017518 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX436_SL_ATT3 | 0x4001751C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX436_MS_ADDR | 0x40017520 | FULL | Master region, base address |
| PERI_MS_PPU_FX436_MS_SIZE | 0x40017524 | FULL | Master region, size |
| PERI_MS_PPU_FX436_MS_ATT0 | 0x40017530 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX436_MS_ATT1 | 0x40017534 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX436_MS_ATT2 | 0x40017538 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX436_MS_ATT3 | 0x4001753C | FULL | Master attributes 3 |

21.454 PPU_FX 437

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX437_SL_ADDR | 0x40017540 | FULL | Slave region, base address |
| PERI_MS_PPU_FX437_SL_SIZE | 0x40017544 | FULL | Slave region, size |
| PERI_MS_PPU_FX437_SL_ATT0 | 0x40017550 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX437_SL_ATT1 | 0x40017554 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX437_SL_ATT2 | 0x40017558 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX437_SL_ATT3 | 0x4001755C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX437_MS_ADDR | 0x40017560 | FULL | Master region, base address |
| PERI_MS_PPU_FX437_MS_SIZE | 0x40017564 | FULL | Master region, size |
| PERI_MS_PPU_FX437_MS_ATT0 | 0x40017570 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX437_MS_ATT1 | 0x40017574 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX437_MS_ATT2 | 0x40017578 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX437_MS_ATT3 | 0x4001757C | FULL | Master attributes 3 |

21.455 PPU_FX 438

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX438_SL_ADDR | 0x40017580 | FULL | Slave region, base address |
| PERI_MS_PPU_FX438_SL_SIZE | 0x40017584 | FULL | Slave region, size |
| PERI_MS_PPU_FX438_SL_ATT0 | 0x40017590 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX438_SL_ATT1 | 0x40017594 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX438_SL_ATT2 | 0x40017598 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX438_SL_ATT3 | 0x4001759C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX438_MS_ADDR | 0x400175A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX438_MS_SIZE | 0x400175A4 | FULL | Master region, size |
| PERI_MS_PPU_FX438_MS_ATT0 | 0x400175B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX438_MS_ATT1 | 0x400175B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX438_MS_ATT2 | 0x400175B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX438_MS_ATT3 | 0x400175BC | FULL | Master attributes 3 |

21.456 PPU_FX 439

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|----------------------------|
| PERI_MS_PPU_FX439_SL_ADDR | 0x400175C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX439_SL_SIZE | 0x400175C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX439_SL_ATT0 | 0x400175D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX439_SL_ATT1 | 0x400175D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX439_SL_ATT2 | 0x400175D8 | FULL | Slave attributes 2 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX439_SL_ATT3 | 0x400175DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX439_MS_ADDR | 0x400175E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX439_MS_SIZE | 0x400175E4 | FULL | Master region, size |
| PERI_MS_PPU_FX439_MS_ATT0 | 0x400175F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX439_MS_ATT1 | 0x400175F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX439_MS_ATT2 | 0x400175F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX439_MS_ATT3 | 0x400175FC | FULL | Master attributes 3 |

21.457 PPU_FX 440

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX440_SL_ADDR | 0x40017600 | FULL | Slave region, base address |
| PERI_MS_PPU_FX440_SL_SIZE | 0x40017604 | FULL | Slave region, size |
| PERI_MS_PPU_FX440_SL_ATT0 | 0x40017610 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX440_SL_ATT1 | 0x40017614 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX440_SL_ATT2 | 0x40017618 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX440_SL_ATT3 | 0x4001761C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX440_MS_ADDR | 0x40017620 | FULL | Master region, base address |
| PERI_MS_PPU_FX440_MS_SIZE | 0x40017624 | FULL | Master region, size |
| PERI_MS_PPU_FX440_MS_ATT0 | 0x40017630 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX440_MS_ATT1 | 0x40017634 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX440_MS_ATT2 | 0x40017638 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX440_MS_ATT3 | 0x4001763C | FULL | Master attributes 3 |

21.458 PPU_FX 441

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX441_SL_ADDR | 0x40017640 | FULL | Slave region, base address |
| PERI_MS_PPU_FX441_SL_SIZE | 0x40017644 | FULL | Slave region, size |
| PERI_MS_PPU_FX441_SL_ATT0 | 0x40017650 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX441_SL_ATT1 | 0x40017654 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX441_SL_ATT2 | 0x40017658 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX441_SL_ATT3 | 0x4001765C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX441_MS_ADDR | 0x40017660 | FULL | Master region, base address |
| PERI_MS_PPU_FX441_MS_SIZE | 0x40017664 | FULL | Master region, size |
| PERI_MS_PPU_FX441_MS_ATT0 | 0x40017670 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX441_MS_ATT1 | 0x40017674 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX441_MS_ATT2 | 0x40017678 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX441_MS_ATT3 | 0x4001767C | FULL | Master attributes 3 |

21.459 PPU_FX 442

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX442_SL_ADDR | 0x40017680 | FULL | Slave region, base address |
| PERI_MS_PPU_FX442_SL_SIZE | 0x40017684 | FULL | Slave region, size |
| PERI_MS_PPU_FX442_SL_ATT0 | 0x40017690 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX442_SL_ATT1 | 0x40017694 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX442_SL_ATT2 | 0x40017698 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX442_SL_ATT3 | 0x4001769C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX442_MS_ADDR | 0x400176A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX442_MS_SIZE | 0x400176A4 | FULL | Master region, size |
| PERI_MS_PPU_FX442_MS_ATT0 | 0x400176B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX442_MS_ATT1 | 0x400176B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX442_MS_ATT2 | 0x400176B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX442_MS_ATT3 | 0x400176BC | FULL | Master attributes 3 |

21.460 PPU_FX 443

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX443_SL_ADDR | 0x400176C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX443_SL_SIZE | 0x400176C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX443_SL_ATT0 | 0x400176D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX443_SL_ATT1 | 0x400176D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX443_SL_ATT2 | 0x400176D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX443_SL_ATT3 | 0x400176DC | FULL | Slave attributes 3 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX443_MS_ADDR | 0x400176E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX443_MS_SIZE | 0x400176E4 | FULL | Master region, size |
| PERI_MS_PPU_FX443_MS_ATT0 | 0x400176F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX443_MS_ATT1 | 0x400176F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX443_MS_ATT2 | 0x400176F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX443_MS_ATT3 | 0x400176FC | FULL | Master attributes 3 |

21.461 PPU_FX 444

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX444_SL_ADDR | 0x40017700 | FULL | Slave region, base address |
| PERI_MS_PPU_FX444_SL_SIZE | 0x40017704 | FULL | Slave region, size |
| PERI_MS_PPU_FX444_SL_ATT0 | 0x40017710 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX444_SL_ATT1 | 0x40017714 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX444_SL_ATT2 | 0x40017718 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX444_SL_ATT3 | 0x4001771C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX444_MS_ADDR | 0x40017720 | FULL | Master region, base address |
| PERI_MS_PPU_FX444_MS_SIZE | 0x40017724 | FULL | Master region, size |
| PERI_MS_PPU_FX444_MS_ATT0 | 0x40017730 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX444_MS_ATT1 | 0x40017734 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX444_MS_ATT2 | 0x40017738 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX444_MS_ATT3 | 0x4001773C | FULL | Master attributes 3 |

21.462 PPU_FX 445

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX445_SL_ADDR | 0x40017740 | FULL | Slave region, base address |
| PERI_MS_PPU_FX445_SL_SIZE | 0x40017744 | FULL | Slave region, size |
| PERI_MS_PPU_FX445_SL_ATT0 | 0x40017750 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX445_SL_ATT1 | 0x40017754 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX445_SL_ATT2 | 0x40017758 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX445_SL_ATT3 | 0x4001775C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX445_MS_ADDR | 0x40017760 | FULL | Master region, base address |
| PERI_MS_PPU_FX445_MS_SIZE | 0x40017764 | FULL | Master region, size |
| PERI_MS_PPU_FX445_MS_ATT0 | 0x40017770 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX445_MS_ATT1 | 0x40017774 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX445_MS_ATT2 | 0x40017778 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX445_MS_ATT3 | 0x4001777C | FULL | Master attributes 3 |

21.463 PPU_FX 446

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX446_SL_ADDR | 0x40017780 | FULL | Slave region, base address |
| PERI_MS_PPU_FX446_SL_SIZE | 0x40017784 | FULL | Slave region, size |
| PERI_MS_PPU_FX446_SL_ATT0 | 0x40017790 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX446_SL_ATT1 | 0x40017794 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX446_SL_ATT2 | 0x40017798 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX446_SL_ATT3 | 0x4001779C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX446_MS_ADDR | 0x400177A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX446_MS_SIZE | 0x400177A4 | FULL | Master region, size |
| PERI_MS_PPU_FX446_MS_ATT0 | 0x400177B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX446_MS_ATT1 | 0x400177B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX446_MS_ATT2 | 0x400177B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX446_MS_ATT3 | 0x400177BC | FULL | Master attributes 3 |

21.464 PPU_FX 447

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX447_SL_ADDR | 0x400177C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX447_SL_SIZE | 0x400177C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX447_SL_ATT0 | 0x400177D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX447_SL_ATT1 | 0x400177D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX447_SL_ATT2 | 0x400177D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX447_SL_ATT3 | 0x400177DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX447_MS_ADDR | 0x400177E0 | FULL | Master region, base address |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX447_MS_SIZE | 0x400177E4 | FULL | Master region, size |
| PERI_MS_PPU_FX447_MS_ATT0 | 0x400177F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX447_MS_ATT1 | 0x400177F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX447_MS_ATT2 | 0x400177F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX447_MS_ATT3 | 0x400177FC | FULL | Master attributes 3 |

21.465 PPU_FX 448

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX448_SL_ADDR | 0x40017800 | FULL | Slave region, base address |
| PERI_MS_PPU_FX448_SL_SIZE | 0x40017804 | FULL | Slave region, size |
| PERI_MS_PPU_FX448_SL_ATT0 | 0x40017810 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX448_SL_ATT1 | 0x40017814 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX448_SL_ATT2 | 0x40017818 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX448_SL_ATT3 | 0x4001781C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX448_MS_ADDR | 0x40017820 | FULL | Master region, base address |
| PERI_MS_PPU_FX448_MS_SIZE | 0x40017824 | FULL | Master region, size |
| PERI_MS_PPU_FX448_MS_ATT0 | 0x40017830 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX448_MS_ATT1 | 0x40017834 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX448_MS_ATT2 | 0x40017838 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX448_MS_ATT3 | 0x4001783C | FULL | Master attributes 3 |

21.466 PPU_FX 449

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX449_SL_ADDR | 0x40017840 | FULL | Slave region, base address |
| PERI_MS_PPU_FX449_SL_SIZE | 0x40017844 | FULL | Slave region, size |
| PERI_MS_PPU_FX449_SL_ATT0 | 0x40017850 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX449_SL_ATT1 | 0x40017854 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX449_SL_ATT2 | 0x40017858 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX449_SL_ATT3 | 0x4001785C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX449_MS_ADDR | 0x40017860 | FULL | Master region, base address |
| PERI_MS_PPU_FX449_MS_SIZE | 0x40017864 | FULL | Master region, size |
| PERI_MS_PPU_FX449_MS_ATT0 | 0x40017870 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX449_MS_ATT1 | 0x40017874 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX449_MS_ATT2 | 0x40017878 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX449_MS_ATT3 | 0x4001787C | FULL | Master attributes 3 |

21.467 PPU_FX 450

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX450_SL_ADDR | 0x40017880 | FULL | Slave region, base address |
| PERI_MS_PPU_FX450_SL_SIZE | 0x40017884 | FULL | Slave region, size |
| PERI_MS_PPU_FX450_SL_ATT0 | 0x40017890 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX450_SL_ATT1 | 0x40017894 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX450_SL_ATT2 | 0x40017898 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX450_SL_ATT3 | 0x4001789C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX450_MS_ADDR | 0x400178A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX450_MS_SIZE | 0x400178A4 | FULL | Master region, size |
| PERI_MS_PPU_FX450_MS_ATT0 | 0x400178B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX450_MS_ATT1 | 0x400178B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX450_MS_ATT2 | 0x400178B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX450_MS_ATT3 | 0x400178BC | FULL | Master attributes 3 |

21.468 PPU_FX 451

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX451_SL_ADDR | 0x400178C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX451_SL_SIZE | 0x400178C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX451_SL_ATT0 | 0x400178D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX451_SL_ATT1 | 0x400178D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX451_SL_ATT2 | 0x400178D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX451_SL_ATT3 | 0x400178DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX451_MS_ADDR | 0x400178E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX451_MS_SIZE | 0x400178E4 | FULL | Master region, size |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX451_MS_ATT0 | 0x400178F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX451_MS_ATT1 | 0x400178F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX451_MS_ATT2 | 0x400178F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX451_MS_ATT3 | 0x400178FC | FULL | Master attributes 3 |

21.469 PPU_FX 452

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX452_SL_ADDR | 0x40017900 | FULL | Slave region, base address |
| PERI_MS_PPU_FX452_SL_SIZE | 0x40017904 | FULL | Slave region, size |
| PERI_MS_PPU_FX452_SL_ATT0 | 0x40017910 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX452_SL_ATT1 | 0x40017914 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX452_SL_ATT2 | 0x40017918 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX452_SL_ATT3 | 0x4001791C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX452_MS_ADDR | 0x40017920 | FULL | Master region, base address |
| PERI_MS_PPU_FX452_MS_SIZE | 0x40017924 | FULL | Master region, size |
| PERI_MS_PPU_FX452_MS_ATT0 | 0x40017930 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX452_MS_ATT1 | 0x40017934 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX452_MS_ATT2 | 0x40017938 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX452_MS_ATT3 | 0x4001793C | FULL | Master attributes 3 |

21.470 PPU_FX 453

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX453_SL_ADDR | 0x40017940 | FULL | Slave region, base address |
| PERI_MS_PPU_FX453_SL_SIZE | 0x40017944 | FULL | Slave region, size |
| PERI_MS_PPU_FX453_SL_ATT0 | 0x40017950 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX453_SL_ATT1 | 0x40017954 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX453_SL_ATT2 | 0x40017958 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX453_SL_ATT3 | 0x4001795C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX453_MS_ADDR | 0x40017960 | FULL | Master region, base address |
| PERI_MS_PPU_FX453_MS_SIZE | 0x40017964 | FULL | Master region, size |
| PERI_MS_PPU_FX453_MS_ATT0 | 0x40017970 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX453_MS_ATT1 | 0x40017974 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX453_MS_ATT2 | 0x40017978 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX453_MS_ATT3 | 0x4001797C | FULL | Master attributes 3 |

21.471 PPU_FX 454

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX454_SL_ADDR | 0x40017980 | FULL | Slave region, base address |
| PERI_MS_PPU_FX454_SL_SIZE | 0x40017984 | FULL | Slave region, size |
| PERI_MS_PPU_FX454_SL_ATT0 | 0x40017990 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX454_SL_ATT1 | 0x40017994 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX454_SL_ATT2 | 0x40017998 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX454_SL_ATT3 | 0x4001799C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX454_MS_ADDR | 0x400179A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX454_MS_SIZE | 0x400179A4 | FULL | Master region, size |
| PERI_MS_PPU_FX454_MS_ATT0 | 0x400179B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX454_MS_ATT1 | 0x400179B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX454_MS_ATT2 | 0x400179B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX454_MS_ATT3 | 0x400179BC | FULL | Master attributes 3 |

21.472 PPU_FX 455

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX455_SL_ADDR | 0x400179C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX455_SL_SIZE | 0x400179C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX455_SL_ATT0 | 0x400179D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX455_SL_ATT1 | 0x400179D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX455_SL_ATT2 | 0x400179D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX455_SL_ATT3 | 0x400179DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX455_MS_ADDR | 0x400179E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX455_MS_SIZE | 0x400179E4 | FULL | Master region, size |
| PERI_MS_PPU_FX455_MS_ATT0 | 0x400179F0 | FULL | Master attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX455_MS_ATT1 | 0x400179F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX455_MS_ATT2 | 0x400179F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX455_MS_ATT3 | 0x400179FC | FULL | Master attributes 3 |

21.473 PPU_FX 456

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX456_SL_ADDR | 0x40017A00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX456_SL_SIZE | 0x40017A04 | FULL | Slave region, size |
| PERI_MS_PPU_FX456_SL_ATT0 | 0x40017A10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX456_SL_ATT1 | 0x40017A14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX456_SL_ATT2 | 0x40017A18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX456_SL_ATT3 | 0x40017A1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX456_MS_ADDR | 0x40017A20 | FULL | Master region, base address |
| PERI_MS_PPU_FX456_MS_SIZE | 0x40017A24 | FULL | Master region, size |
| PERI_MS_PPU_FX456_MS_ATT0 | 0x40017A30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX456_MS_ATT1 | 0x40017A34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX456_MS_ATT2 | 0x40017A38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX456_MS_ATT3 | 0x40017A3C | FULL | Master attributes 3 |

21.474 PPU_FX 457

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX457_SL_ADDR | 0x40017A40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX457_SL_SIZE | 0x40017A44 | FULL | Slave region, size |
| PERI_MS_PPU_FX457_SL_ATT0 | 0x40017A50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX457_SL_ATT1 | 0x40017A54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX457_SL_ATT2 | 0x40017A58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX457_SL_ATT3 | 0x40017A5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX457_MS_ADDR | 0x40017A60 | FULL | Master region, base address |
| PERI_MS_PPU_FX457_MS_SIZE | 0x40017A64 | FULL | Master region, size |
| PERI_MS_PPU_FX457_MS_ATT0 | 0x40017A70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX457_MS_ATT1 | 0x40017A74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX457_MS_ATT2 | 0x40017A78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX457_MS_ATT3 | 0x40017A7C | FULL | Master attributes 3 |

21.475 PPU_FX 458

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX458_SL_ADDR | 0x40017A80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX458_SL_SIZE | 0x40017A84 | FULL | Slave region, size |
| PERI_MS_PPU_FX458_SL_ATT0 | 0x40017A90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX458_SL_ATT1 | 0x40017A94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX458_SL_ATT2 | 0x40017A98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX458_SL_ATT3 | 0x40017A9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX458_MS_ADDR | 0x40017AA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX458_MS_SIZE | 0x40017AA4 | FULL | Master region, size |
| PERI_MS_PPU_FX458_MS_ATT0 | 0x40017AB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX458_MS_ATT1 | 0x40017AB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX458_MS_ATT2 | 0x40017AB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX458_MS_ATT3 | 0x40017ABC | FULL | Master attributes 3 |

21.476 PPU_FX 459

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX459_SL_ADDR | 0x40017AC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX459_SL_SIZE | 0x40017AC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX459_SL_ATT0 | 0x40017AD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX459_SL_ATT1 | 0x40017AD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX459_SL_ATT2 | 0x40017AD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX459_SL_ATT3 | 0x40017ADC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX459_MS_ADDR | 0x40017AE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX459_MS_SIZE | 0x40017AE4 | FULL | Master region, size |
| PERI_MS_PPU_FX459_MS_ATT0 | 0x40017AF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX459_MS_ATT1 | 0x40017AF4 | FULL | Master attributes 1 |

| Register Name | Address | Permission | Description |
|---|------------|------------|---------------------|
| PERI_MS_PPU_FX459_MS_ATT2 | 0x40017AF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX459_MS_ATT3 | 0x40017AFC | FULL | Master attributes 3 |

21.477 PPU_FX 460

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX460_SL_ADDR | 0x40017B00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX460_SL_SIZE | 0x40017B04 | FULL | Slave region, size |
| PERI_MS_PPU_FX460_SL_ATT0 | 0x40017B10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX460_SL_ATT1 | 0x40017B14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX460_SL_ATT2 | 0x40017B18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX460_SL_ATT3 | 0x40017B1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX460_MS_ADDR | 0x40017B20 | FULL | Master region, base address |
| PERI_MS_PPU_FX460_MS_SIZE | 0x40017B24 | FULL | Master region, size |
| PERI_MS_PPU_FX460_MS_ATT0 | 0x40017B30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX460_MS_ATT1 | 0x40017B34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX460_MS_ATT2 | 0x40017B38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX460_MS_ATT3 | 0x40017B3C | FULL | Master attributes 3 |

21.478 PPU_FX 461

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX461_SL_ADDR | 0x40017B40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX461_SL_SIZE | 0x40017B44 | FULL | Slave region, size |
| PERI_MS_PPU_FX461_SL_ATT0 | 0x40017B50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX461_SL_ATT1 | 0x40017B54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX461_SL_ATT2 | 0x40017B58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX461_SL_ATT3 | 0x40017B5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX461_MS_ADDR | 0x40017B60 | FULL | Master region, base address |
| PERI_MS_PPU_FX461_MS_SIZE | 0x40017B64 | FULL | Master region, size |
| PERI_MS_PPU_FX461_MS_ATT0 | 0x40017B70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX461_MS_ATT1 | 0x40017B74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX461_MS_ATT2 | 0x40017B78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX461_MS_ATT3 | 0x40017B7C | FULL | Master attributes 3 |

21.479 PPU_FX 462

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX462_SL_ADDR | 0x40017B80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX462_SL_SIZE | 0x40017B84 | FULL | Slave region, size |
| PERI_MS_PPU_FX462_SL_ATT0 | 0x40017B90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX462_SL_ATT1 | 0x40017B94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX462_SL_ATT2 | 0x40017B98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX462_SL_ATT3 | 0x40017B9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX462_MS_ADDR | 0x40017BA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX462_MS_SIZE | 0x40017BA4 | FULL | Master region, size |
| PERI_MS_PPU_FX462_MS_ATT0 | 0x40017BB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX462_MS_ATT1 | 0x40017BB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX462_MS_ATT2 | 0x40017BB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX462_MS_ATT3 | 0x40017BBC | FULL | Master attributes 3 |

21.480 PPU_FX 463

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX463_SL_ADDR | 0x40017BC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX463_SL_SIZE | 0x40017BC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX463_SL_ATT0 | 0x40017BD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX463_SL_ATT1 | 0x40017BD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX463_SL_ATT2 | 0x40017BD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX463_SL_ATT3 | 0x40017BDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX463_MS_ADDR | 0x40017BE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX463_MS_SIZE | 0x40017BE4 | FULL | Master region, size |
| PERI_MS_PPU_FX463_MS_ATT0 | 0x40017BF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX463_MS_ATT1 | 0x40017BF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX463_MS_ATT2 | 0x40017BF8 | FULL | Master attributes 2 |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---------------------|
| PERI_MS_PPU_FX463_MS_ATT3 | 0x40017BFC | FULL | Master attributes 3 |

21.481 PPU_FX 464

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX464_SL_ADDR | 0x40017C00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX464_SL_SIZE | 0x40017C04 | FULL | Slave region, size |
| PERI_MS_PPU_FX464_SL_ATT0 | 0x40017C10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX464_SL_ATT1 | 0x40017C14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX464_SL_ATT2 | 0x40017C18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX464_SL_ATT3 | 0x40017C1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX464_MS_ADDR | 0x40017C20 | FULL | Master region, base address |
| PERI_MS_PPU_FX464_MS_SIZE | 0x40017C24 | FULL | Master region, size |
| PERI_MS_PPU_FX464_MS_ATT0 | 0x40017C30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX464_MS_ATT1 | 0x40017C34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX464_MS_ATT2 | 0x40017C38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX464_MS_ATT3 | 0x40017C3C | FULL | Master attributes 3 |

21.482 PPU_FX 465

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX465_SL_ADDR | 0x40017C40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX465_SL_SIZE | 0x40017C44 | FULL | Slave region, size |
| PERI_MS_PPU_FX465_SL_ATT0 | 0x40017C50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX465_SL_ATT1 | 0x40017C54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX465_SL_ATT2 | 0x40017C58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX465_SL_ATT3 | 0x40017C5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX465_MS_ADDR | 0x40017C60 | FULL | Master region, base address |
| PERI_MS_PPU_FX465_MS_SIZE | 0x40017C64 | FULL | Master region, size |
| PERI_MS_PPU_FX465_MS_ATT0 | 0x40017C70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX465_MS_ATT1 | 0x40017C74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX465_MS_ATT2 | 0x40017C78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX465_MS_ATT3 | 0x40017C7C | FULL | Master attributes 3 |

21.483 PPU_FX 466

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX466_SL_ADDR | 0x40017C80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX466_SL_SIZE | 0x40017C84 | FULL | Slave region, size |
| PERI_MS_PPU_FX466_SL_ATT0 | 0x40017C90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX466_SL_ATT1 | 0x40017C94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX466_SL_ATT2 | 0x40017C98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX466_SL_ATT3 | 0x40017C9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX466_MS_ADDR | 0x40017CA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX466_MS_SIZE | 0x40017CA4 | FULL | Master region, size |
| PERI_MS_PPU_FX466_MS_ATT0 | 0x40017CB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX466_MS_ATT1 | 0x40017CB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX466_MS_ATT2 | 0x40017CB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX466_MS_ATT3 | 0x40017CBC | FULL | Master attributes 3 |

21.484 PPU_FX 467

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|-----------------------------|
| PERI_MS_PPU_FX467_SL_ADDR | 0x40017CC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX467_SL_SIZE | 0x40017CC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX467_SL_ATT0 | 0x40017CD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX467_SL_ATT1 | 0x40017CD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX467_SL_ATT2 | 0x40017CD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX467_SL_ATT3 | 0x40017CDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX467_MS_ADDR | 0x40017CE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX467_MS_SIZE | 0x40017CE4 | FULL | Master region, size |
| PERI_MS_PPU_FX467_MS_ATT0 | 0x40017CF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX467_MS_ATT1 | 0x40017CF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX467_MS_ATT2 | 0x40017CF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX467_MS_ATT3 | 0x40017CFC | FULL | Master attributes 3 |

21.485 PPU_FX 468

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX468_SL_ADDR | 0x40017D00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX468_SL_SIZE | 0x40017D04 | FULL | Slave region, size |
| PERI_MS_PPU_FX468_SL_ATT0 | 0x40017D10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX468_SL_ATT1 | 0x40017D14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX468_SL_ATT2 | 0x40017D18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX468_SL_ATT3 | 0x40017D1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX468_MS_ADDR | 0x40017D20 | FULL | Master region, base address |
| PERI_MS_PPU_FX468_MS_SIZE | 0x40017D24 | FULL | Master region, size |
| PERI_MS_PPU_FX468_MS_ATT0 | 0x40017D30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX468_MS_ATT1 | 0x40017D34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX468_MS_ATT2 | 0x40017D38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX468_MS_ATT3 | 0x40017D3C | FULL | Master attributes 3 |

21.486 PPU_FX 469

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX469_SL_ADDR | 0x40017D40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX469_SL_SIZE | 0x40017D44 | FULL | Slave region, size |
| PERI_MS_PPU_FX469_SL_ATT0 | 0x40017D50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX469_SL_ATT1 | 0x40017D54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX469_SL_ATT2 | 0x40017D58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX469_SL_ATT3 | 0x40017D5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX469_MS_ADDR | 0x40017D60 | FULL | Master region, base address |
| PERI_MS_PPU_FX469_MS_SIZE | 0x40017D64 | FULL | Master region, size |
| PERI_MS_PPU_FX469_MS_ATT0 | 0x40017D70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX469_MS_ATT1 | 0x40017D74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX469_MS_ATT2 | 0x40017D78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX469_MS_ATT3 | 0x40017D7C | FULL | Master attributes 3 |

21.487 PPU_FX 470

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX470_SL_ADDR | 0x40017D80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX470_SL_SIZE | 0x40017D84 | FULL | Slave region, size |
| PERI_MS_PPU_FX470_SL_ATT0 | 0x40017D90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX470_SL_ATT1 | 0x40017D94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX470_SL_ATT2 | 0x40017D98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX470_SL_ATT3 | 0x40017D9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX470_MS_ADDR | 0x40017DA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX470_MS_SIZE | 0x40017DA4 | FULL | Master region, size |
| PERI_MS_PPU_FX470_MS_ATT0 | 0x40017DB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX470_MS_ATT1 | 0x40017DB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX470_MS_ATT2 | 0x40017DB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX470_MS_ATT3 | 0x40017DBC | FULL | Master attributes 3 |

21.488 PPU_FX 471

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX471_SL_ADDR | 0x40017DC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX471_SL_SIZE | 0x40017DC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX471_SL_ATT0 | 0x40017DD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX471_SL_ATT1 | 0x40017DD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX471_SL_ATT2 | 0x40017DD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX471_SL_ATT3 | 0x40017DDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX471_MS_ADDR | 0x40017DE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX471_MS_SIZE | 0x40017DE4 | FULL | Master region, size |
| PERI_MS_PPU_FX471_MS_ATT0 | 0x40017DF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX471_MS_ATT1 | 0x40017DF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX471_MS_ATT2 | 0x40017DF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX471_MS_ATT3 | 0x40017DFC | FULL | Master attributes 3 |

21.489 PPU_FX 472

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX472_SL_ADDR | 0x40017E00 | FULL | Slave region, base address |
| PERI_MS_PPU_FX472_SL_SIZE | 0x40017E04 | FULL | Slave region, size |
| PERI_MS_PPU_FX472_SL_ATT0 | 0x40017E10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX472_SL_ATT1 | 0x40017E14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX472_SL_ATT2 | 0x40017E18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX472_SL_ATT3 | 0x40017E1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX472_MS_ADDR | 0x40017E20 | FULL | Master region, base address |
| PERI_MS_PPU_FX472_MS_SIZE | 0x40017E24 | FULL | Master region, size |
| PERI_MS_PPU_FX472_MS_ATT0 | 0x40017E30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX472_MS_ATT1 | 0x40017E34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX472_MS_ATT2 | 0x40017E38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX472_MS_ATT3 | 0x40017E3C | FULL | Master attributes 3 |

21.490 PPU_FX 473

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX473_SL_ADDR | 0x40017E40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX473_SL_SIZE | 0x40017E44 | FULL | Slave region, size |
| PERI_MS_PPU_FX473_SL_ATT0 | 0x40017E50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX473_SL_ATT1 | 0x40017E54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX473_SL_ATT2 | 0x40017E58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX473_SL_ATT3 | 0x40017E5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX473_MS_ADDR | 0x40017E60 | FULL | Master region, base address |
| PERI_MS_PPU_FX473_MS_SIZE | 0x40017E64 | FULL | Master region, size |
| PERI_MS_PPU_FX473_MS_ATT0 | 0x40017E70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX473_MS_ATT1 | 0x40017E74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX473_MS_ATT2 | 0x40017E78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX473_MS_ATT3 | 0x40017E7C | FULL | Master attributes 3 |

21.491 PPU_FX 474

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX474_SL_ADDR | 0x40017E80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX474_SL_SIZE | 0x40017E84 | FULL | Slave region, size |
| PERI_MS_PPU_FX474_SL_ATT0 | 0x40017E90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX474_SL_ATT1 | 0x40017E94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX474_SL_ATT2 | 0x40017E98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX474_SL_ATT3 | 0x40017E9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX474_MS_ADDR | 0x40017EA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX474_MS_SIZE | 0x40017EA4 | FULL | Master region, size |
| PERI_MS_PPU_FX474_MS_ATT0 | 0x40017EB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX474_MS_ATT1 | 0x40017EB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX474_MS_ATT2 | 0x40017EB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX474_MS_ATT3 | 0x40017EBC | FULL | Master attributes 3 |

21.492 PPU_FX 475

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX475_SL_ADDR | 0x40017EC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX475_SL_SIZE | 0x40017EC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX475_SL_ATT0 | 0x40017ED0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX475_SL_ATT1 | 0x40017ED4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX475_SL_ATT2 | 0x40017ED8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX475_SL_ATT3 | 0x40017EDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX475_MS_ADDR | 0x40017EE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX475_MS_SIZE | 0x40017EE4 | FULL | Master region, size |
| PERI_MS_PPU_FX475_MS_ATT0 | 0x40017EF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX475_MS_ATT1 | 0x40017EF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX475_MS_ATT2 | 0x40017EF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX475_MS_ATT3 | 0x40017EFC | FULL | Master attributes 3 |

21.493 PPU_FX 476

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX476_SL_ADDR | 0x40017F00 | FULL | Slave region, base address |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX476_SL_SIZE | 0x40017F04 | FULL | Slave region, size |
| PERI_MS_PPU_FX476_SL_ATT0 | 0x40017F10 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX476_SL_ATT1 | 0x40017F14 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX476_SL_ATT2 | 0x40017F18 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX476_SL_ATT3 | 0x40017F1C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX476_MS_ADDR | 0x40017F20 | FULL | Master region, base address |
| PERI_MS_PPU_FX476_MS_SIZE | 0x40017F24 | FULL | Master region, size |
| PERI_MS_PPU_FX476_MS_ATT0 | 0x40017F30 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX476_MS_ATT1 | 0x40017F34 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX476_MS_ATT2 | 0x40017F38 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX476_MS_ATT3 | 0x40017F3C | FULL | Master attributes 3 |

21.494 PPU_FX 477

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX477_SL_ADDR | 0x40017F40 | FULL | Slave region, base address |
| PERI_MS_PPU_FX477_SL_SIZE | 0x40017F44 | FULL | Slave region, size |
| PERI_MS_PPU_FX477_SL_ATT0 | 0x40017F50 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX477_SL_ATT1 | 0x40017F54 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX477_SL_ATT2 | 0x40017F58 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX477_SL_ATT3 | 0x40017F5C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX477_MS_ADDR | 0x40017F60 | FULL | Master region, base address |
| PERI_MS_PPU_FX477_MS_SIZE | 0x40017F64 | FULL | Master region, size |
| PERI_MS_PPU_FX477_MS_ATT0 | 0x40017F70 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX477_MS_ATT1 | 0x40017F74 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX477_MS_ATT2 | 0x40017F78 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX477_MS_ATT3 | 0x40017F7C | FULL | Master attributes 3 |

21.495 PPU_FX 478

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX478_SL_ADDR | 0x40017F80 | FULL | Slave region, base address |
| PERI_MS_PPU_FX478_SL_SIZE | 0x40017F84 | FULL | Slave region, size |
| PERI_MS_PPU_FX478_SL_ATT0 | 0x40017F90 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX478_SL_ATT1 | 0x40017F94 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX478_SL_ATT2 | 0x40017F98 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX478_SL_ATT3 | 0x40017F9C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX478_MS_ADDR | 0x40017FA0 | FULL | Master region, base address |
| PERI_MS_PPU_FX478_MS_SIZE | 0x40017FA4 | FULL | Master region, size |
| PERI_MS_PPU_FX478_MS_ATT0 | 0x40017FB0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX478_MS_ATT1 | 0x40017FB4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX478_MS_ATT2 | 0x40017FB8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX478_MS_ATT3 | 0x40017FBC | FULL | Master attributes 3 |

21.496 PPU_FX 479

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX479_SL_ADDR | 0x40017FC0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX479_SL_SIZE | 0x40017FC4 | FULL | Slave region, size |
| PERI_MS_PPU_FX479_SL_ATT0 | 0x40017FD0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX479_SL_ATT1 | 0x40017FD4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX479_SL_ATT2 | 0x40017FD8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX479_SL_ATT3 | 0x40017FDC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX479_MS_ADDR | 0x40017FE0 | FULL | Master region, base address |
| PERI_MS_PPU_FX479_MS_SIZE | 0x40017FE4 | FULL | Master region, size |
| PERI_MS_PPU_FX479_MS_ATT0 | 0x40017FF0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX479_MS_ATT1 | 0x40017FF4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX479_MS_ATT2 | 0x40017FF8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX479_MS_ATT3 | 0x40017FFC | FULL | Master attributes 3 |

21.497 PPU_FX 480

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX480_SL_ADDR | 0x40018000 | FULL | Slave region, base address |
| PERI_MS_PPU_FX480_SL_SIZE | 0x40018004 | FULL | Slave region, size |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX480_SL_ATT0 | 0x40018010 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX480_SL_ATT1 | 0x40018014 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX480_SL_ATT2 | 0x40018018 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX480_SL_ATT3 | 0x4001801C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX480_MS_ADDR | 0x40018020 | FULL | Master region, base address |
| PERI_MS_PPU_FX480_MS_SIZE | 0x40018024 | FULL | Master region, size |
| PERI_MS_PPU_FX480_MS_ATT0 | 0x40018030 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX480_MS_ATT1 | 0x40018034 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX480_MS_ATT2 | 0x40018038 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX480_MS_ATT3 | 0x4001803C | FULL | Master attributes 3 |

21.498 PPU_FX 481

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX481_SL_ADDR | 0x40018040 | FULL | Slave region, base address |
| PERI_MS_PPU_FX481_SL_SIZE | 0x40018044 | FULL | Slave region, size |
| PERI_MS_PPU_FX481_SL_ATT0 | 0x40018050 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX481_SL_ATT1 | 0x40018054 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX481_SL_ATT2 | 0x40018058 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX481_SL_ATT3 | 0x4001805C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX481_MS_ADDR | 0x40018060 | FULL | Master region, base address |
| PERI_MS_PPU_FX481_MS_SIZE | 0x40018064 | FULL | Master region, size |
| PERI_MS_PPU_FX481_MS_ATT0 | 0x40018070 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX481_MS_ATT1 | 0x40018074 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX481_MS_ATT2 | 0x40018078 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX481_MS_ATT3 | 0x4001807C | FULL | Master attributes 3 |

21.499 PPU_FX 482

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX482_SL_ADDR | 0x40018080 | FULL | Slave region, base address |
| PERI_MS_PPU_FX482_SL_SIZE | 0x40018084 | FULL | Slave region, size |
| PERI_MS_PPU_FX482_SL_ATT0 | 0x40018090 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX482_SL_ATT1 | 0x40018094 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX482_SL_ATT2 | 0x40018098 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX482_SL_ATT3 | 0x4001809C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX482_MS_ADDR | 0x400180A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX482_MS_SIZE | 0x400180A4 | FULL | Master region, size |
| PERI_MS_PPU_FX482_MS_ATT0 | 0x400180B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX482_MS_ATT1 | 0x400180B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX482_MS_ATT2 | 0x400180B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX482_MS_ATT3 | 0x400180BC | FULL | Master attributes 3 |

21.500 PPU_FX 483

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX483_SL_ADDR | 0x400180C0 | FULL | Slave region, base address |
| PERI_MS_PPU_FX483_SL_SIZE | 0x400180C4 | FULL | Slave region, size |
| PERI_MS_PPU_FX483_SL_ATT0 | 0x400180D0 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX483_SL_ATT1 | 0x400180D4 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX483_SL_ATT2 | 0x400180D8 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX483_SL_ATT3 | 0x400180DC | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX483_MS_ADDR | 0x400180E0 | FULL | Master region, base address |
| PERI_MS_PPU_FX483_MS_SIZE | 0x400180E4 | FULL | Master region, size |
| PERI_MS_PPU_FX483_MS_ATT0 | 0x400180F0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX483_MS_ATT1 | 0x400180F4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX483_MS_ATT2 | 0x400180F8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX483_MS_ATT3 | 0x400180FC | FULL | Master attributes 3 |

21.501 PPU_FX 484

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PERI_MS_PPU_FX484_SL_ADDR | 0x40018100 | FULL | Slave region, base address |
| PERI_MS_PPU_FX484_SL_SIZE | 0x40018104 | FULL | Slave region, size |
| PERI_MS_PPU_FX484_SL_ATT0 | 0x40018110 | FULL | Slave attributes 0 |

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX484_SL_ATT1 | 0x40018114 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX484_SL_ATT2 | 0x40018118 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX484_SL_ATT3 | 0x4001811C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX484_MS_ADDR | 0x40018120 | FULL | Master region, base address |
| PERI_MS_PPU_FX484_MS_SIZE | 0x40018124 | FULL | Master region, size |
| PERI_MS_PPU_FX484_MS_ATT0 | 0x40018130 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX484_MS_ATT1 | 0x40018134 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX484_MS_ATT2 | 0x40018138 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX484_MS_ATT3 | 0x4001813C | FULL | Master attributes 3 |

21.502 PPU_FX 485

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX485_SL_ADDR | 0x40018140 | FULL | Slave region, base address |
| PERI_MS_PPU_FX485_SL_SIZE | 0x40018144 | FULL | Slave region, size |
| PERI_MS_PPU_FX485_SL_ATT0 | 0x40018150 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX485_SL_ATT1 | 0x40018154 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX485_SL_ATT2 | 0x40018158 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX485_SL_ATT3 | 0x4001815C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX485_MS_ADDR | 0x40018160 | FULL | Master region, base address |
| PERI_MS_PPU_FX485_MS_SIZE | 0x40018164 | FULL | Master region, size |
| PERI_MS_PPU_FX485_MS_ATT0 | 0x40018170 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX485_MS_ATT1 | 0x40018174 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX485_MS_ATT2 | 0x40018178 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX485_MS_ATT3 | 0x4001817C | FULL | Master attributes 3 |

21.503 PPU_FX 486

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------------|
| PERI_MS_PPU_FX486_SL_ADDR | 0x40018180 | FULL | Slave region, base address |
| PERI_MS_PPU_FX486_SL_SIZE | 0x40018184 | FULL | Slave region, size |
| PERI_MS_PPU_FX486_SL_ATT0 | 0x40018190 | FULL | Slave attributes 0 |
| PERI_MS_PPU_FX486_SL_ATT1 | 0x40018194 | FULL | Slave attributes 1 |
| PERI_MS_PPU_FX486_SL_ATT2 | 0x40018198 | FULL | Slave attributes 2 |
| PERI_MS_PPU_FX486_SL_ATT3 | 0x4001819C | FULL | Slave attributes 3 |
| PERI_MS_PPU_FX486_MS_ADDR | 0x400181A0 | FULL | Master region, base address |
| PERI_MS_PPU_FX486_MS_SIZE | 0x400181A4 | FULL | Master region, size |
| PERI_MS_PPU_FX486_MS_ATT0 | 0x400181B0 | FULL | Master attributes 0 |
| PERI_MS_PPU_FX486_MS_ATT1 | 0x400181B4 | FULL | Master attributes 1 |
| PERI_MS_PPU_FX486_MS_ATT2 | 0x400181B8 | FULL | Master attributes 2 |
| PERI_MS_PPU_FX486_MS_ATT3 | 0x400181BC | FULL | Master attributes 3 |

21.504 Register Details

21.504.1 PPU_PR

21.504.1.1 PERI_MS_PPU_PR_SL_ADDR

Description: Slave region, base address

Address: 0x40010000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: SL_ADDR can only be written by protection context '0' (protection context '0' has unrestricted access). The access privileges for other protection contexts are determined by MS_ATT0, ..., MS_ATT3, with the additional restriction that SL_ADDR can NOT be written.

Typically, the SL_ADDR and SL_SIZE registers are programmed by the boot process with protection context '0'.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | ADDR30 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR30 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR30 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 2:31 | ADDR30 | RW | R | Undefined | This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is '15') must be 64 KByte aligned, and ADDR30[13:0] must be '0's. |

21.504.1.2 PERI_MS_PPU_PR_SL_SIZE

Description: Slave region, size
Address: 0x40010004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: SL_SIZE can only be written by protection context '0' (protection context '0' has unrestricted access). The access privileges for other protection contexts are determined by MS_ATT0, ..., MS_ATT3, with the additional restriction that SL_SIZE can NOT be written.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|---------------------|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 24:28 | REGION_SIZE | RW | R | Undefined | This field specifies the size of the slave region: '0': Undefined. '1': 4 B region (this is the smallest region size). '2': 8 B region '3': 16 B region '4': 32 B region '5': 64 B region '6': 128 B region '7': 256 B region '8': 512 B region '9': 1 KB region '10': 2 KB region '11': 4 KB region '12': 8 KB region '13': 16 KB region '14': 32 KB region '15': 64 KB region '16': 128 KB region '17': 256 KB region '18': 512 KB region '19': 1 MB region '20': 2 MB region '21': 4 MB region '22': 8 MB region '23': 16 MB region '24': 32 MB region '25': 64 MB region '26': 128 MB region '27': 256 MB region '28': 512 MB region '29': 1 GB region '30': 2 GB region '31': 4 GB region |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 31 | VALID | RW | R | 0 | Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. |

21.504.1.3 PERI_MS_PPU_PR_SL_ATT0

Description: Slave attributes 0
Address: 0x40010010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The access privileges for SL_ATT0, ..., SL_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the SL_ATT0, ..., SL_ATT3 registers are initialized by the boot process with protection context '0'.

For 4 or less protection contexts (PC_NR ≤ 4), only SL_ATT0 is present. For 5 through 8 protection contexts, only SL_ATT0 and SL_ATT1 are present. For 9 through 12 or less protection contexts, only SL_ATT0, SL_ATT1 and SL_ATT2 are present. For 13 through 16 protection contexts, SL_ATT0, SL_ATT1, SL_ATT2 and SL_ATT3 are all present. If the number of protection contexts is not a multiple of 4, the 'missing' protection contexts in a register have no associated access fields (and the field positions read as '0').

Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | RW | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | RW | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | RW | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | RW | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | RW | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | RW | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

21.504.1.4 PERI_MS_PPU_PR_SL_ATT1

Description: Slave attributes 1
Address: 0x40010014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | PC4_UR | RW | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | RW | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | RW | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | RW | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | RW | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | RW | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | RW | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | RW | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

21.504.1.5 PERI_MS_PPU_PR_SL_ATT2

Description: Slave attributes 2
Address: 0x40010018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC8_UR | RW | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | RW | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | RW | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | RW | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | RW | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | RW | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | RW | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | RW | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

21.504.1.6 PERI_MS_PPU_PR_SL_ATT3

Description: Slave attributes 3
Address: 0x4001001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|------------------|------------------|------------------|------------------|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|--------------------|--------------------|--------------------|------------------|------------------|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC12_UR | RW | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | RW | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | RW | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | RW | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | RW | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | RW | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | RW | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | RW | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

21.504.1.7 PERI_MS_PPU_PR_MS_ADDR

Description: Master region, base address
Address: 0x40010020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: MS_ADDR is fixed (non-programmable).

Default: The access privileges for MS_ADDR are determined by MS_ATT0, ..., MS_ATT3.
 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|------------|
| Name | | | | | | | | None [5:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----|----|----|----|----|----|---|---------------|
| Name | | | | | | | | ADDR26 [15:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|----------------|
| Name | | | | | | | | ADDR26 [23:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----|----|----|----|----|----|----|----------------|
| Name | | | | | | | | ADDR26 [31:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 6:31 | ADDR26 | R | R | ADDR1_DEF | This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. |

21.504.1.8 PERI_MS_PPU_PR_MS_SIZE

Description: Master region, size
Address: 0x40010024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: MS_SIZE is fixed (non-programmable).

Default: The access privileges for MS_SIZE are determined by MS_ATT0, ..., MS_ATT3.
 0x85000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|---------------------|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 24:28 | REGION_SIZE | R | R | 5 | This field specifies the size of the master region: '5': 64 B region The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. |
| 31 | VALID | R | R | 1 | Master region enable: '1': Enabled. |

21.504.1.9 PERI_MS_PPU_PR_MS_ATT0

Description: Master attributes 0
Address: 0x40010030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: The access privileges for MS_ATT0, ..., MS_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the MS_ATT0, ..., MS_ATT3 registers are programmed by the boot process with protection context '0'.

Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | R | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | R | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | R | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | R | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | R | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | R | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

21.504.1.10 PERI_MS_PPU_PR_MS_ATT1

Description: Master attributes 1
Address: 0x40010034
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | PC4_UR | R | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | R | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | R | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | R | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | R | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | R | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | R | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | R | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

21.504.1.11 PERI_MS_PPU_PR_MS_ATT2

Description: Master attributes 2
Address: 0x40010038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC8_UR | R | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | R | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | R | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | R | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | R | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | R | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | R | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | R | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

21.504.1.12 PERI_MS_PPU_PR_MS_ATT3

Description: Master attributes 3
Address: 0x4001003C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|------------------|------------------|------------------|------------------|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|--------------------|--------------------|--------------------|------------------|------------------|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC12_UR | R | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | R | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | R | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | R | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | R | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | R | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | R | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | R | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

21.504.2 PPU_FX

21.504.2.1 PERI_MS_PPU_FX_SL_ADDR

Description: Slave region, base address
Address: 0x40010800
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: SL_ADDR is fixed (non-programmable).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|------------|---|
| Name | | | | | | | None [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | ADDR30 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR30 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR30 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 2:31 | ADDR30 | R | R | ADDR0_DEF | This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is '15') must be 64 KByte aligned, and ADDR30[13:0] must be '0's. |

21.504.2.2 PERI_MS_PPU_FX_SL_SIZE

Description: Slave region, size
Address: 0x40010804
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: SL_SIZE is fixed (non-programmable).
Default: 0x80000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|--------------|----|---------------------|----|----|----|----|
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|------------------|--|
| 24:28 | REGION_SIZE | R | R | REGION_SIZE0_DEF | This field specifies the size of the slave region: '0': Undefined. '1': 4 B region (this is the smallest region size). '2': 8 B region '3': 16 B region '4': 32 B region '5': 64 B region '6': 128 B region '7': 256 B region '8': 512 B region '9': 1 KB region '10': 2 KB region '11': 4 KB region '12': 8 KB region '13': 16 KB region '14': 32 KB region '15': 64 KB region '16': 128 KB region '17': 256 KB region '18': 512 KB region '19': 1 MB region '20': 2 MB region '21': 4 MB region '22': 8 MB region '23': 16 MB region '24': 32 MB region '25': 64 MB region '26': 128 MB region '27': 256 MB region '28': 512 MB region '29': 1 GB region '30': 2 GB region '31': 4 GB region |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 31 | VALID | R | R | 1 | Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. |

21.504.2.3 PERI_MS_PPU_FX_SL_ATT0

Description: Slave attributes 0
Address: 0x40010810
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: The access privileges for SL_ATT0, ..., SL_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the SL_ATT0, ..., SL_ATT3 registers are initialized by the boot process with protection context '0'.

For 4 or less protection contexts (PC_NR ≤ 4), only SL_ATT0 is present. For 5 through 8 protection contexts, only SL_ATT0 and SL_ATT1 are present. For 9 through 12 or less protection contexts, only SL_ATT0, SL_ATT1 and SL_ATT2 are present. For 13 through 16 protection contexts, SL_ATT0, SL_ATT1, SL_ATT2 and SL_ATT3 are all present. If the number of protection contexts is not a multiple of 4, the 'missing' protection contexts in a register have no associated access fields (and the field positions read as '0').

Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | RW | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | RW | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | RW | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | RW | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | RW | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | RW | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

21.504.2.4 PERI_MS_PPU_FX_SL_ATT1

Description: Slave attributes 1
Address: 0x40010814
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | PC4_UR | RW | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | RW | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | RW | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | RW | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | RW | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | RW | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | RW | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | RW | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

21.504.2.5 PERI_MS_PPU_FX_SL_ATT2

Description: Slave attributes 2
Address: 0x40010818
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC8_UR | RW | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | RW | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | RW | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | RW | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | RW | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | RW | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | RW | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | RW | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

21.504.2.6 PERI_MS_PPU_FX_SL_ATT3

Description: Slave attributes 3
Address: 0x4001081C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|------------------|------------------|------------------|------------------|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|--------------------|--------------------|--------------------|------------------|------------------|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC12_UR | RW | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | RW | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | RW | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | RW | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | RW | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | RW | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | RW | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | RW | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

21.504.2.7 PERI_MS_PPU_FX_MS_ADDR

Description: Master region, base address
Address: 0x40010820
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: MS_ADDR is fixed (non-programmable).

Default: The access privileges for MS_ADDR are determined by MS_ATT0, ..., MS_ATT3.
 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|------------|
| Name | | | | | | | | None [5:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----|----|----|----|----|----|---|---------------|
| Name | | | | | | | | ADDR26 [15:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|----------------|
| Name | | | | | | | | ADDR26 [23:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----|----|----|----|----|----|----|----------------|
| Name | | | | | | | | ADDR26 [31:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 6:31 | ADDR26 | R | R | ADDR1_DEF | This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. |

21.504.2.8 PERI_MS_PPU_FX_MS_SIZE

Description: Master region, size
Address: 0x40010824
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: MS_SIZE is fixed (non-programmable).

Default: The access privileges for MS_SIZE are determined by MS_ATT0, ..., MS_ATT3.
 0x85000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|--------------|----|---------------------|----|----|----|----|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | VALID [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 24:28 | REGION_SIZE | R | R | 5 | This field specifies the size of the master region: '5': 64 B region The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. |
| 31 | VALID | R | R | 1 | Master region enable: '1': Enabled. |

21.504.2.9 PERI_MS_PPU_FX_MS_ATT0

Description: Master attributes 0
Address: 0x40010830
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment: The access privileges for MS_ATT0, ..., MS_ATT3 are determined by MS_ATT0, ..., MS_ATT3.

Note that protection context '0' has unrestricted access: PC0_UR, ..., PC0_NS fields are fixed to '1's. The other protection contexts have SW programmable fields.

Typically, the MS_ATT0, ..., MS_ATT3 registers are programmed by the boot process with protection context '0'.

Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC0_NS [4:4] | PC0_PW [3:3] | PC0_PR [2:2] | PC0_UW [1:1] | PC0_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC1_NS [12:12] | PC1_PW [11:11] | PC1_PR [10:10] | PC1_UW [9:9] | PC1_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC2_NS [20:20] | PC2_PW [19:19] | PC2_PR [18:18] | PC2_UW [17:17] | PC2_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC3_NS [28:28] | PC3_PW [27:27] | PC3_PR [26:26] | PC3_UW [25:25] | PC3_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | PC0_UR | R | R | 1 | Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). |
| 1 | PC0_UW | R | R | 1 | Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | PC0_PR | R | R | 1 | Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). |
| 3 | PC0_PW | R | R | 1 | Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |
| 4 | PC0_NS | R | R | 1 | Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC1_UR | R | R | 1 | Protection context 1, user read enable. |
| 9 | PC1_UW | RW | R | 1 | Protection context 1, user write enable. |
| 10 | PC1_PR | R | R | 1 | Protection context 1, privileged read enable. |
| 11 | PC1_PW | RW | R | 1 | Protection context 1, privileged write enable. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 12 | PC1_NS | RW | R | 1 | Protection context 1, non-secure. |
| 16 | PC2_UR | R | R | 1 | Protection context 2, user read enable. |
| 17 | PC2_UW | RW | R | 1 | Protection context 2, user write enable. |
| 18 | PC2_PR | R | R | 1 | Protection context 2, privileged read enable. |
| 19 | PC2_PW | RW | R | 1 | Protection context 2, privileged write enable. |
| 20 | PC2_NS | RW | R | 1 | Protection context 2, non-secure. |
| 24 | PC3_UR | R | R | 1 | Protection context 3, user read enable. |
| 25 | PC3_UW | RW | R | 1 | Protection context 3, user write enable. |
| 26 | PC3_PR | R | R | 1 | Protection context 3, privileged read enable. |
| 27 | PC3_PW | RW | R | 1 | Protection context 3, privileged write enable. |
| 28 | PC3_NS | RW | R | 1 | Protection context 3, non-secure. |

21.504.2.10 PERI_MS_PPU_FX_MS_ATT1

Description: Master attributes 1
Address: 0x40010834
Offset: 0x34
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC4_NS [4:4] | PC4_PW [3:3] | PC4_PR [2:2] | PC4_UW [1:1] | PC4_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC5_NS [12:12] | PC5_PW [11:11] | PC5_PR [10:10] | PC5_UW [9:9] | PC5_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [23:21] | | | PC6_NS [20:20] | PC6_PW [19:19] | PC6_PR [18:18] | PC6_UW [17:17] | PC6_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|
| Name | None [31:29] | | | PC7_NS [28:28] | PC7_PW [27:27] | PC7_PR [26:26] | PC7_UW [25:25] | PC7_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | PC4_UR | R | R | 1 | Protection context 4, user read enable. |
| 1 | PC4_UW | RW | R | 1 | Protection context 4, user write enable. |
| 2 | PC4_PR | R | R | 1 | Protection context 4, privileged read enable. |
| 3 | PC4_PW | RW | R | 1 | Protection context 4, privileged write enable. |
| 4 | PC4_NS | RW | R | 1 | Protection context 4, non-secure. |
| 8 | PC5_UR | R | R | 1 | Protection context 5, user read enable. |
| 9 | PC5_UW | RW | R | 1 | Protection context 5, user write enable. |
| 10 | PC5_PR | R | R | 1 | Protection context 5, privileged read enable. |
| 11 | PC5_PW | RW | R | 1 | Protection context 5, privileged write enable. |
| 12 | PC5_NS | RW | R | 1 | Protection context 5, non-secure. |
| 16 | PC6_UR | R | R | 1 | Protection context 6, user read enable. |
| 17 | PC6_UW | RW | R | 1 | Protection context 6, user write enable. |
| 18 | PC6_PR | R | R | 1 | Protection context 6, privileged read enable. |
| 19 | PC6_PW | RW | R | 1 | Protection context 6, privileged write enable. |
| 20 | PC6_NS | RW | R | 1 | Protection context 6, non-secure. |
| 24 | PC7_UR | R | R | 1 | Protection context 7, user read enable. |
| 25 | PC7_UW | RW | R | 1 | Protection context 7, user write enable. |
| 26 | PC7_PR | R | R | 1 | Protection context 7, privileged read enable. |
| 27 | PC7_PW | RW | R | 1 | Protection context 7, privileged write enable. |
| 28 | PC7_NS | RW | R | 1 | Protection context 7, non-secure. |

21.504.2.11 PERI_MS_PPU_FX_MS_ATT2

Description: Master attributes 2
Address: 0x40010838
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name | None [7:5] | | | PC8_NS [4:4] | PC8_PW [3:3] | PC8_PR [2:2] | PC8_UW [1:1] | PC8_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------|-------------------|-------------------|-----------------|-----------------|
| Name | None [15:13] | | | PC9_NS [12:12] | PC9_PW [11:11] | PC9_PR [10:10] | PC9_UW [9:9] | PC9_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC10_NS [20:20] | PC10_PW [19:19] | PC10_PR [18:18] | PC10_UW [17:17] | PC10_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC11_NS [28:28] | PC11_PW [27:27] | PC11_PR [26:26] | PC11_UW [25:25] | PC11_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC8_UR | R | R | 1 | Protection context 8, user read enable. |
| 1 | PC8_UW | RW | R | 1 | Protection context 8, user write enable. |
| 2 | PC8_PR | R | R | 1 | Protection context 8, privileged read enable. |
| 3 | PC8_PW | RW | R | 1 | Protection context 8, privileged write enable. |
| 4 | PC8_NS | RW | R | 1 | Protection context 8, non-secure. |
| 8 | PC9_UR | R | R | 1 | Protection context 9, user read enable. |
| 9 | PC9_UW | RW | R | 1 | Protection context 9, user write enable. |
| 10 | PC9_PR | R | R | 1 | Protection context 9, privileged read enable. |
| 11 | PC9_PW | RW | R | 1 | Protection context 9, privileged write enable. |
| 12 | PC9_NS | RW | R | 1 | Protection context 9, non-secure. |
| 16 | PC10_UR | R | R | 1 | Protection context 10, user read enable. |
| 17 | PC10_UW | RW | R | 1 | Protection context 10, user write enable. |
| 18 | PC10_PR | R | R | 1 | Protection context 10, privileged read enable. |
| 19 | PC10_PW | RW | R | 1 | Protection context 10, privileged write enable. |
| 20 | PC10_NS | RW | R | 1 | Protection context 10, non-secure. |
| 24 | PC11_UR | R | R | 1 | Protection context 11, user read enable. |
| 25 | PC11_UW | RW | R | 1 | Protection context 11, user write enable. |
| 26 | PC11_PR | R | R | 1 | Protection context 11, privileged read enable. |
| 27 | PC11_PW | RW | R | 1 | Protection context 11, privileged write enable. |
| 28 | PC11_NS | RW | R | 1 | Protection context 11, non-secure. |

21.504.2.12 PERI_MS_PPU_FX_MS_ATT3

Description: Master attributes 3
Address: 0x4001083C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1F1F1F1F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|------------------|------------------|------------------|------------------|
| Name | None [7:5] | | | PC12_NS [4:4] | PC12_PW [3:3] | PC12_PR [2:2] | PC12_UW [1:1] | PC12_UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|--------------------|--------------------|--------------------|------------------|------------------|
| Name | None [15:13] | | | PC13_NS [12:12] | PC13_PW [11:11] | PC13_PR [10:10] | PC13_UW [9:9] | PC13_UR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [23:21] | | | PC14_NS [20:20] | PC14_PW [19:19] | PC14_PR [18:18] | PC14_UW [17:17] | PC14_UR [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name | None [31:29] | | | PC15_NS [28:28] | PC15_PW [27:27] | PC15_PR [26:26] | PC15_UW [25:25] | PC15_UR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | PC12_UR | R | R | 1 | Protection context 12, user read enable. |
| 1 | PC12_UW | RW | R | 1 | Protection context 12, user write enable. |
| 2 | PC12_PR | R | R | 1 | Protection context 12, privileged read enable. |
| 3 | PC12_PW | RW | R | 1 | Protection context 12, privileged write enable. |
| 4 | PC12_NS | RW | R | 1 | Protection context 12, non-secure. |
| 8 | PC13_UR | R | R | 1 | Protection context 13, user read enable. |
| 9 | PC13_UW | RW | R | 1 | Protection context 13, user write enable. |
| 10 | PC13_PR | R | R | 1 | Protection context 13, privileged read enable. |
| 11 | PC13_PW | RW | R | 1 | Protection context 13, privileged write enable. |
| 12 | PC13_NS | RW | R | 1 | Protection context 13, non-secure. |
| 16 | PC14_UR | R | R | 1 | Protection context 14, user read enable. |
| 17 | PC14_UW | RW | R | 1 | Protection context 14, user write enable. |
| 18 | PC14_PR | R | R | 1 | Protection context 14, privileged read enable. |
| 19 | PC14_PW | RW | R | 1 | Protection context 14, privileged write enable. |
| 20 | PC14_NS | RW | R | 1 | Protection context 14, non-secure. |
| 24 | PC15_UR | R | R | 1 | Protection context 15, user read enable. |
| 25 | PC15_UW | RW | R | 1 | Protection context 15, user write enable. |
| 26 | PC15_PR | R | R | 1 | Protection context 15, privileged read enable. |
| 27 | PC15_PW | RW | R | 1 | Protection context 15, privileged write enable. |
| 28 | PC15_NS | RW | R | 1 | Protection context 15, non-secure. |

22 PROT

| | |
|--------------|------------|
| Description | Protection |
| Base Address | 0x40230000 |
| Size | 0x10000 |
| Slave Num | MMIO2 - 3 |

22.1 SMPU

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|--|
| PROT_SMPU_MS0_CTL | 0x40230000 | FULL | Master 0 protection context control |
| PROT_SMPU_MS1_CTL | 0x40230004 | FULL | Master 1 protection context control <i>Note: P NS PC_MASK_15_TO_1 are not available for this register</i> |
| PROT_SMPU_MS2_CTL | 0x40230008 | FULL | Master 2 protection context control <i>Note: P NS PC_MASK_15_TO_1 are not available for this register</i> |
| PROT_SMPU_MS3_CTL | 0x4023000C | FULL | Master 3 protection context control <i>Note: P NS PC_MASK_15_TO_1 are not available for this register</i> |
| PROT_SMPU_MS4_CTL | 0x40230010 | FULL | Master 4 protection context control <i>Note: P NS PC_MASK_15_TO_1 are not available for this register</i> |
| PROT_SMPU_MS14_CTL | 0x40230038 | FULL | Master 14 protection context control |
| PROT_SMPU_MS15_CTL | 0x4023003C | FULL | Master 15 protection context control |

22.1.1 SMPU_STRUCT 0

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT0_ADDR0 | 0x40232000 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT0_ATT0 | 0x40232004 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT0_ADDR1 | 0x40232020 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT0_ATT1 | 0x40232024 | FULL | SMPU region attributes 1 (master structure) |

22.1.2 SMPU_STRUCT 1

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT1_ADDR0 | 0x40232040 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT1_ATT0 | 0x40232044 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT1_ADDR1 | 0x40232060 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT1_ATT1 | 0x40232064 | FULL | SMPU region attributes 1 (master structure) |

22.1.3 SMPU_STRUCT 2

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT2_ADDR0 | 0x40232080 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT2_ATT0 | 0x40232084 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT2_ADDR1 | 0x402320A0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT2_ATT1 | 0x402320A4 | FULL | SMPU region attributes 1 (master structure) |

22.1.4 SMPU_STRUCT 3

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT3_ADDR0 | 0x402320C0 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT3_ATT0 | 0x402320C4 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT3_ADDR1 | 0x402320E0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT3_ATT1 | 0x402320E4 | FULL | SMPU region attributes 1 (master structure) |

22.1.5 SMPU_STRUCT 4

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT4_ADDR0 | 0x40232100 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT4_ATT0 | 0x40232104 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT4_ADDR1 | 0x40232120 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT4_ATT1 | 0x40232124 | FULL | SMPU region attributes 1 (master structure) |

22.1.6 SMPU_STRUCT 5

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT5_ADDR0 | 0x40232140 | FULL | SMPU region address 0 (slave structure) |

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT5_ATT0 | 0x40232144 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT5_ADDR1 | 0x40232160 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT5_ATT1 | 0x40232164 | FULL | SMPU region attributes 1 (master structure) |

22.1.7 SMPU_STRUCT 6

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT6_ADDR0 | 0x40232180 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT6_ATT0 | 0x40232184 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT6_ADDR1 | 0x402321A0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT6_ATT1 | 0x402321A4 | FULL | SMPU region attributes 1 (master structure) |

22.1.8 SMPU_STRUCT 7

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT7_ADDR0 | 0x402321C0 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT7_ATT0 | 0x402321C4 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT7_ADDR1 | 0x402321E0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT7_ATT1 | 0x402321E4 | FULL | SMPU region attributes 1 (master structure) |

22.1.9 SMPU_STRUCT 8

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT8_ADDR0 | 0x40232200 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT8_ATT0 | 0x40232204 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT8_ADDR1 | 0x40232220 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT8_ATT1 | 0x40232224 | FULL | SMPU region attributes 1 (master structure) |

22.1.10 SMPU_STRUCT 9

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT9_ADDR0 | 0x40232240 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT9_ATT0 | 0x40232244 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT9_ADDR1 | 0x40232260 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT9_ATT1 | 0x40232264 | FULL | SMPU region attributes 1 (master structure) |

22.1.11 SMPU_STRUCT 10

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT10_ADDR0 | 0x40232280 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT10_ATT0 | 0x40232284 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT10_ADDR1 | 0x402322A0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT10_ATT1 | 0x402322A4 | FULL | SMPU region attributes 1 (master structure) |

22.1.12 SMPU_STRUCT 11

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT11_ADDR0 | 0x402322C0 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT11_ATT0 | 0x402322C4 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT11_ADDR1 | 0x402322E0 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT11_ATT1 | 0x402322E4 | FULL | SMPU region attributes 1 (master structure) |

22.1.13 SMPU_STRUCT 12

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT12_ADDR0 | 0x40232300 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT12_ATT0 | 0x40232304 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT12_ADDR1 | 0x40232320 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT12_ATT1 | 0x40232324 | FULL | SMPU region attributes 1 (master structure) |

22.1.14 SMPU_STRUCT 13

| Register Name | Address | Permission | Description |
|---|------------|------------|---|
| PROT_SMPU_SMPU_STRUCT13_ADDR0 | 0x40232340 | FULL | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT13_ATT0 | 0x40232344 | FULL | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT13_ADDR1 | 0x40232360 | FULL | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT13_ATT1 | 0x40232364 | FULL | SMPU region attributes 1 (master structure) |

22.1.15 SMPU_STRUCT 14

| Register Name | Address | Permission | Description |
|---|------------|------------------|---|
| PROT_SMPU_SMPU_STRUCT14_ADDR0 | 0x40232380 | SECURE - READ | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT14_ATT0 | 0x40232384 | SECURE - READ | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT14_ADDR1 | 0x402323A0 | SECURE - READ | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT14_ATT1 | 0x402323A4 | SECURE - READ | SMPU region attributes 1 (master structure) |

22.1.16 SMPU_STRUCT 15

| Register Name | Address | Permission | Description |
|---|------------|------------------|---|
| PROT_SMPU_SMPU_STRUCT15_ADDR0 | 0x402323C0 | SECURE - READ | SMPU region address 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT15_ATT0 | 0x402323C4 | SECURE - READ | SMPU region attributes 0 (slave structure) |
| PROT_SMPU_SMPU_STRUCT15_ADDR1 | 0x402323E0 | SECURE - READ | SMPU region address 1 (master structure) |
| PROT_SMPU_SMPU_STRUCT15_ATT1 | 0x402323E4 | SECURE - READ | SMPU region attributes 1 (master structure) |

22.2 MPU 0

| Register Name | Address | Permission | Description |
|---|------------|------------|----------------------------|
| PROT_MPU0_MS_CTL | 0x40234000 | FULL | Master control |
| PROT_MPU0_MS_CTL_READ_MIR0 | 0x40234004 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR1 | 0x40234008 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR2 | 0x4023400C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR3 | 0x40234010 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR4 | 0x40234014 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR5 | 0x40234018 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR6 | 0x4023401C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR7 | 0x40234020 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR8 | 0x40234024 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR9 | 0x40234028 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR10 | 0x4023402C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR11 | 0x40234030 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR12 | 0x40234034 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR13 | 0x40234038 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR14 | 0x4023403C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR15 | 0x40234040 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR16 | 0x40234044 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR17 | 0x40234048 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR18 | 0x4023404C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR19 | 0x40234050 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR20 | 0x40234054 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR21 | 0x40234058 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR22 | 0x4023405C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR23 | 0x40234060 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR24 | 0x40234064 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR25 | 0x40234068 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR26 | 0x4023406C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR27 | 0x40234070 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR28 | 0x40234074 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR29 | 0x40234078 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR30 | 0x4023407C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR31 | 0x40234080 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR32 | 0x40234084 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR33 | 0x40234088 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR34 | 0x4023408C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR35 | 0x40234090 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR36 | 0x40234094 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR37 | 0x40234098 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR38 | 0x4023409C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR39 | 0x402340A0 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PROT_MPU0_MS_CTL_READ_MIR40 | 0x402340A4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR41 | 0x402340A8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR42 | 0x402340AC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR43 | 0x402340B0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR44 | 0x402340B4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR45 | 0x402340B8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR46 | 0x402340BC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR47 | 0x402340C0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR48 | 0x402340C4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR49 | 0x402340C8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR50 | 0x402340CC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR51 | 0x402340D0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR52 | 0x402340D4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR53 | 0x402340D8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR54 | 0x402340DC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR55 | 0x402340E0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR56 | 0x402340E4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR57 | 0x402340E8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR58 | 0x402340EC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR59 | 0x402340F0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR60 | 0x402340F4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR61 | 0x402340F8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR62 | 0x402340FC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR63 | 0x40234100 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR64 | 0x40234104 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR65 | 0x40234108 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR66 | 0x4023410C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR67 | 0x40234110 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR68 | 0x40234114 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR69 | 0x40234118 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR70 | 0x4023411C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR71 | 0x40234120 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR72 | 0x40234124 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR73 | 0x40234128 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR74 | 0x4023412C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR75 | 0x40234130 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR76 | 0x40234134 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR77 | 0x40234138 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR78 | 0x4023413C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR79 | 0x40234140 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR80 | 0x40234144 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR81 | 0x40234148 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR82 | 0x4023414C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR83 | 0x40234150 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR84 | 0x40234154 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR85 | 0x40234158 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR86 | 0x4023415C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR87 | 0x40234160 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR88 | 0x40234164 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR89 | 0x40234168 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR90 | 0x4023416C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR91 | 0x40234170 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR92 | 0x40234174 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR93 | 0x40234178 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR94 | 0x4023417C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR95 | 0x40234180 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR96 | 0x40234184 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR97 | 0x40234188 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR98 | 0x4023418C | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR99 | 0x40234190 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR100 | 0x40234194 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR101 | 0x40234198 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR102 | 0x4023419C | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|--|------------|------------|----------------------------|
| PROT_MPU0_MS_CTL_READ_MIR103 | 0x402341A0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR104 | 0x402341A4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR105 | 0x402341A8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR106 | 0x402341AC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR107 | 0x402341B0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR108 | 0x402341B4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR109 | 0x402341B8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR110 | 0x402341BC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR111 | 0x402341C0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR112 | 0x402341C4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR113 | 0x402341C8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR114 | 0x402341CC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR115 | 0x402341D0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR116 | 0x402341D4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR117 | 0x402341D8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR118 | 0x402341DC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR119 | 0x402341E0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR120 | 0x402341E4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR121 | 0x402341E8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR122 | 0x402341EC | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR123 | 0x402341F0 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR124 | 0x402341F4 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR125 | 0x402341F8 | FULL | Master control read mirror |
| PROT_MPU0_MS_CTL_READ_MIR126 | 0x402341FC | FULL | Master control read mirror |

22.3 MPU 14

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| PROT_MPU14_MS_CTL | 0x40237800 | FULL | Master control Note:PC_SAVED is not available for this register |
| PROT_MPU14_MS_CTL_READ_MIR0 | 0x40237804 | FULL | Master control read mirror Note:PC_SAVED is not available for this register |
| PROT_MPU14_MS_CTL_READ_MIR1 | 0x40237808 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR2 | 0x4023780C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR3 | 0x40237810 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR4 | 0x40237814 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR5 | 0x40237818 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR6 | 0x4023781C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR7 | 0x40237820 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR8 | 0x40237824 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR9 | 0x40237828 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR10 | 0x4023782C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR11 | 0x40237830 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR12 | 0x40237834 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR13 | 0x40237838 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR14 | 0x4023783C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR15 | 0x40237840 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR16 | 0x40237844 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR17 | 0x40237848 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR18 | 0x4023784C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR19 | 0x40237850 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR20 | 0x40237854 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR21 | 0x40237858 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR22 | 0x4023785C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR23 | 0x40237860 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR24 | 0x40237864 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR25 | 0x40237868 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR26 | 0x4023786C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR27 | 0x40237870 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR28 | 0x40237874 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR29 | 0x40237878 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR30 | 0x4023787C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR31 | 0x40237880 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR32 | 0x40237884 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|----------------------------|
| PROT_MPU14_MS_CTL_READ_MIR33 | 0x40237888 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR34 | 0x4023788C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR35 | 0x40237890 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR36 | 0x40237894 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR37 | 0x40237898 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR38 | 0x4023789C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR39 | 0x402378A0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR40 | 0x402378A4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR41 | 0x402378A8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR42 | 0x402378AC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR43 | 0x402378B0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR44 | 0x402378B4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR45 | 0x402378B8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR46 | 0x402378BC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR47 | 0x402378C0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR48 | 0x402378C4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR49 | 0x402378C8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR50 | 0x402378CC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR51 | 0x402378D0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR52 | 0x402378D4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR53 | 0x402378D8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR54 | 0x402378DC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR55 | 0x402378E0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR56 | 0x402378E4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR57 | 0x402378E8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR58 | 0x402378EC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR59 | 0x402378F0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR60 | 0x402378F4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR61 | 0x402378F8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR62 | 0x402378FC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR63 | 0x40237900 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR64 | 0x40237904 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR65 | 0x40237908 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR66 | 0x4023790C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR67 | 0x40237910 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR68 | 0x40237914 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR69 | 0x40237918 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR70 | 0x4023791C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR71 | 0x40237920 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR72 | 0x40237924 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR73 | 0x40237928 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR74 | 0x4023792C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR75 | 0x40237930 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR76 | 0x40237934 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR77 | 0x40237938 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR78 | 0x4023793C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR79 | 0x40237940 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR80 | 0x40237944 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR81 | 0x40237948 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR82 | 0x4023794C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR83 | 0x40237950 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR84 | 0x40237954 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR85 | 0x40237958 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR86 | 0x4023795C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR87 | 0x40237960 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR88 | 0x40237964 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR89 | 0x40237968 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR90 | 0x4023796C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR91 | 0x40237970 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR92 | 0x40237974 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR93 | 0x40237978 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR94 | 0x4023797C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR95 | 0x40237980 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|----------------------------|
| PROT_MPU14_MS_CTL_READ_MIR96 | 0x40237984 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR97 | 0x40237988 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR98 | 0x4023798C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR99 | 0x40237990 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR100 | 0x40237994 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR101 | 0x40237998 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR102 | 0x4023799C | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR103 | 0x402379A0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR104 | 0x402379A4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR105 | 0x402379A8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR106 | 0x402379AC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR107 | 0x402379B0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR108 | 0x402379B4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR109 | 0x402379B8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR110 | 0x402379BC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR111 | 0x402379C0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR112 | 0x402379C4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR113 | 0x402379C8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR114 | 0x402379CC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR115 | 0x402379D0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR116 | 0x402379D4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR117 | 0x402379D8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR118 | 0x402379DC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR119 | 0x402379E0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR120 | 0x402379E4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR121 | 0x402379E8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR122 | 0x402379EC | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR123 | 0x402379F0 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR124 | 0x402379F4 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR125 | 0x402379F8 | FULL | Master control read mirror |
| PROT_MPU14_MS_CTL_READ_MIR126 | 0x402379FC | FULL | Master control read mirror |

22.4 MPU 15

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|---|
| PROT_MPU15_MS_CTL | 0x40237C00 | FULL | Master control Note:PC_SAVED is not available for this register |
| PROT_MPU15_MS_CTL_READ_MIR0 | 0x40237C04 | FULL | Master control read mirror Note:PC_SAVED is not available for this register |
| PROT_MPU15_MS_CTL_READ_MIR1 | 0x40237C08 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR2 | 0x40237C0C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR3 | 0x40237C10 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR4 | 0x40237C14 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR5 | 0x40237C18 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR6 | 0x40237C1C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR7 | 0x40237C20 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR8 | 0x40237C24 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR9 | 0x40237C28 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR10 | 0x40237C2C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR11 | 0x40237C30 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR12 | 0x40237C34 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR13 | 0x40237C38 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR14 | 0x40237C3C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR15 | 0x40237C40 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR16 | 0x40237C44 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR17 | 0x40237C48 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR18 | 0x40237C4C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR19 | 0x40237C50 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR20 | 0x40237C54 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR21 | 0x40237C58 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR22 | 0x40237C5C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR23 | 0x40237C60 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR24 | 0x40237C64 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR25 | 0x40237C68 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|----------------------------|
| PROT_MPU15_MS_CTL_READ_MIR26 | 0x40237C6C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR27 | 0x40237C70 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR28 | 0x40237C74 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR29 | 0x40237C78 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR30 | 0x40237C7C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR31 | 0x40237C80 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR32 | 0x40237C84 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR33 | 0x40237C88 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR34 | 0x40237C8C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR35 | 0x40237C90 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR36 | 0x40237C94 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR37 | 0x40237C98 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR38 | 0x40237C9C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR39 | 0x40237CA0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR40 | 0x40237CA4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR41 | 0x40237CA8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR42 | 0x40237CAC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR43 | 0x40237CB0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR44 | 0x40237CB4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR45 | 0x40237CB8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR46 | 0x40237CBC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR47 | 0x40237CC0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR48 | 0x40237CC4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR49 | 0x40237CC8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR50 | 0x40237CCC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR51 | 0x40237CD0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR52 | 0x40237CD4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR53 | 0x40237CD8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR54 | 0x40237CDC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR55 | 0x40237CE0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR56 | 0x40237CE4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR57 | 0x40237CE8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR58 | 0x40237CEC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR59 | 0x40237CF0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR60 | 0x40237CF4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR61 | 0x40237CF8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR62 | 0x40237CFC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR63 | 0x40237D00 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR64 | 0x40237D04 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR65 | 0x40237D08 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR66 | 0x40237D0C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR67 | 0x40237D10 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR68 | 0x40237D14 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR69 | 0x40237D18 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR70 | 0x40237D1C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR71 | 0x40237D20 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR72 | 0x40237D24 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR73 | 0x40237D28 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR74 | 0x40237D2C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR75 | 0x40237D30 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR76 | 0x40237D34 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR77 | 0x40237D38 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR78 | 0x40237D3C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR79 | 0x40237D40 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR80 | 0x40237D44 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR81 | 0x40237D48 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR82 | 0x40237D4C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR83 | 0x40237D50 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR84 | 0x40237D54 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR85 | 0x40237D58 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR86 | 0x40237D5C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR87 | 0x40237D60 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR88 | 0x40237D64 | FULL | Master control read mirror |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|----------------------------|
| PROT_MPU15_MS_CTL_READ_MIR89 | 0x40237D68 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR90 | 0x40237D6C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR91 | 0x40237D70 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR92 | 0x40237D74 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR93 | 0x40237D78 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR94 | 0x40237D7C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR95 | 0x40237D80 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR96 | 0x40237D84 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR97 | 0x40237D88 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR98 | 0x40237D8C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR99 | 0x40237D90 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR100 | 0x40237D94 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR101 | 0x40237D98 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR102 | 0x40237D9C | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR103 | 0x40237DA0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR104 | 0x40237DA4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR105 | 0x40237DA8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR106 | 0x40237DAC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR107 | 0x40237DB0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR108 | 0x40237DB4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR109 | 0x40237DB8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR110 | 0x40237DBC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR111 | 0x40237DC0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR112 | 0x40237DC4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR113 | 0x40237DC8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR114 | 0x40237DCC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR115 | 0x40237DD0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR116 | 0x40237DD4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR117 | 0x40237DD8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR118 | 0x40237DDC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR119 | 0x40237DE0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR120 | 0x40237DE4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR121 | 0x40237DE8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR122 | 0x40237DEC | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR123 | 0x40237DF0 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR124 | 0x40237DF4 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR125 | 0x40237DF8 | FULL | Master control read mirror |
| PROT_MPU15_MS_CTL_READ_MIR126 | 0x40237DFC | FULL | Master control read mirror |

22.4.1 MPU_STRUCT 0

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT0_ADDR | 0x40237E00 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT0_ATT | 0x40237E04 | FULL | MPU region attributes |

22.4.2 MPU_STRUCT 1

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT1_ADDR | 0x40237E20 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT1_ATT | 0x40237E24 | FULL | MPU region attributes |

22.4.3 MPU_STRUCT 2

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT2_ADDR | 0x40237E40 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT2_ATT | 0x40237E44 | FULL | MPU region attributes |

22.4.4 MPU_STRUCT 3

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT3_ADDR | 0x40237E60 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT3_ATT | 0x40237E64 | FULL | MPU region attributes |

22.4.5 MPU_STRUCT 4

| Register Name | Address | Permission | Description |
|-----------------------------|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT4_ADDR | 0x40237E80 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT4_ATT | 0x40237E84 | FULL | MPU region attributes |

22.4.6 MPU_STRUCT 5

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT5_ADDR | 0x40237EA0 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT5_ATT | 0x40237EA4 | FULL | MPU region attributes |

22.4.7 MPU_STRUCT 6

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT6_ADDR | 0x40237EC0 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT6_ATT | 0x40237EC4 | FULL | MPU region attributes |

22.4.8 MPU_STRUCT 7

| Register Name | Address | Permission | Description |
|---|------------|------------|-----------------------|
| PROT_MPU15_MPU_STRUCT7_ADDR | 0x40237EE0 | FULL | MPU region address |
| PROT_MPU15_MPU_STRUCT7_ATT | 0x40237EE4 | FULL | MPU region attributes |

22.5 Register Details

22.5.1 SMPU

22.5.1.1 PROT_SMPU_MS0_CTL

Description: Master 0 protection context control

Address: 0x40230000

Offset: 0x0

Retention: Retained

IsDeepSleep: No

Comment: Each master has an associated SMPU MS_CTL register. This register provides master specific information. In a system with a secure entity, this register is typically only accessible by the secure entity, to prevent a master from changing its own privileged setting, security setting, arbitration priority or enabled protection contexts.
Master 0 (CM0+ processor) uses SMPU MS0_CTL.
Master 1 (cryptography IP) uses SMPU MS1_CTL.
Master 2 (DataWire 0) uses SMPU MS2_CTL.
Master 3 (DataWire 1) uses SMPU MS3_CTL.
....
Master 14 (CM4 processor) uses SMPU MS14_CTL.
Master 15 (test controller) uses SMPU MS15_CTL.

Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | P | RW | R | 1 | Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute. The default/reset field value provides privileged mode access capabilities. |
| 1 | NS | RW | R | 1 | Security setting ('0': secure mode; '1': non-secure mode). Notes: This field is ONLY used for masters that do NOT provide their own secure/non-secure access control attribute. Note that the default/reset field value provides non-secure mode access capabilities to all masters. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 8:9 | PRI0 | RW | R | 3 | <p>Device wide bus arbitration priority setting ('0': highest priority, '3': lowest priority).</p> <p>Notes:</p> <p>The AHB-Lite interconnect performs arbitration on the individual beats/transfers of a burst (this optimizes latency over locality/bandwidth).</p> <p>The AXI-Lite interconnects performs a single arbitration for the complete burst (this optimizes locality/bandwidth over latency).</p> <p>Masters with the same priority setting form a 'priority group'. Within a 'priority group', round robin arbitration is performed.</p> |
| 16 | PC_MASK_0 | R | R | 0 | <p>Protection context mask for protection context '0'. This field is a constant '0':</p> <ul style="list-style-type: none"> - PC_MASK_0 is '0': MPU MS_CTL.PC[3:0] can NOT be set to '0' and PC[3:0] is not changed. If the protection context of the write transfer is '0', protection is not applied and PC[3:0] can be changed. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | <p>Protection context mask for protection contexts '15' down to '1'. Bit PC_MASK_15_TO_1[i] indicates if the MPU MS_CTL.PC[3:0] protection context field can be set to the value 'i+1':</p> <ul style="list-style-type: none"> - PC_MASK_15_TO_1[i] is '0': MPU MS_CTL.PC[3:0] can NOT be set to 'i+1'; and PC[3:0] is not changed. If the protection context of the write transfer is '0', protection is not applied and PC[3:0] can be changed. - PC_MASK_15_TO_1[i] is '1': MPU MS_CTL.PC[3:0] can be set to 'i+1'. <p>Note: When CPUSS_CM0_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK_15_TO_1[i-1] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 1, 2 or 3 through (HW modifies MPU MS_CTL.PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts (SW modifies MPU MS_CTL.PC[3:0]).</p> |

22.5.1.2 PROT_SMPU_MS1_CTL

Description: Master 1 protection context control
Address: 0x40230004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|------------------------------|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

22.5.1.3 PROT_SMPU_MS2_CTL

Description: Master 2 protection context control
Address: 0x40230008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|------------------------------|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

22.5.1.4 PROT_SMPU_MS3_CTL

Description: Master 3 protection context control
Address: 0x4023000C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|------------------------------|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

22.5.1.5 PROT_SMPU_MS4_CTL

Description: Master 4 protection context control
Address: 0x40230010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|------------------------------|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

22.5.1.6 PROT_SMPU_MS14_CTL

Description: Master 14 protection context control
Address: 0x40230038
Offset: 0x38
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|------------------------------|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

22.5.1.7 PROT_SMPU_MS15_CTL

Description: Master 15 protection context control
Address: 0x4023003C
Offset: 0x3C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x303

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------|---------|
| Name | None [7:2] | | | | | | NS [1:1] | P [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|------------|---|
| Name | None [15:10] | | | | | | PRIO [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----|----|----|----|----|----|----|-------------------|
| Name | | | | | | | | PC_MASK_0 [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|------------------------------|
| 0 | P | RW | R | 1 | See MS0_CTL.P. |
| 1 | NS | RW | R | 1 | See MS0_CTL.NS. |
| 8:9 | PRIO | RW | R | 3 | See MS0_CTL.PRIO |
| 16 | PC_MASK_0 | R | R | 0 | See MS0_CTL.PC_MASK_0. |
| 17:31 | PC_MASK_15_TO_1 | RW | R | 0 | See MS0_CTL.PC_MASK_15_TO_1. |

22.5.1.8 SMPU_STRUCT

22.5.1.8.1 PROT_SMPU_SMPU_STRUCT_ADDR0

Description: SMPU region address 0 (slave structure)
Address: 0x40232000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register defines a SMPU address region.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------------|---|---|---|---|---|---|---|
| Name | SUBREGION_DISABLE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | ADDR24 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR24 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | ADDR24 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|---|
| 0:7 | SUBREGION_DISABLE | RW | R | Undefined | <p>This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable:</p> <p>Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable.</p> <p>E.g., a 64 KByte address region (ATT0.REGION_SIZE is '15') has eight 8 KByte subregions. The access control as defined by ATT0 applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B.</p> |
| 8:31 | ADDR24 | RW | R | Undefined | <p>This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT0.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is '15') is 64 KByte aligned, and ADDR24[7:0] are ignored.</p> |

22.5.1.8.2 PROT_SMPU_SMPU_STRUCT_ATT0

Description: SMPU region attributes 0 (slave structure)
Address: 0x40232004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register defines SMPU access control.
Default: 0x100

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----------|----------|----------|----------|----------|----------|----------|
| Name | None [7:7] | NS [6:6] | PX [5:5] | PW [4:4] | PR [3:3] | UX [2:2] | UW [1:1] | UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----|----|----|----|----|----|---|-----------------|
| Name | | | | | | | | PC_MASK_0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|------------------|--------------|---------------------|----|----|----|----|
| Name | ENABLED [31:31] | PC_MATCH [30:30] | None [29:29] | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0 | UR | RW | R | Undefined | User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). |
| 1 | UW | RW | R | Undefined | User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | UX | RW | R | Undefined | User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). |
| 3 | PR | RW | R | Undefined | Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). |
| 4 | PW | RW | R | Undefined | Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |
| 5 | PX | RW | R | Undefined | Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). |
| 6 | NS | RW | R | Undefined | Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC_MASK_0 | R | R | 1 | This field specifies protection context identifier based access control for protection context '0'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 9:23 | PC_MASK_15_TO_1 | RW | R | Undefined | This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. |
| 24:28 | REGION_SIZE | RW | R | Undefined | This field specifies the region size: '0'-'6': Undefined. '7': 256 B region '8': 512 B region '9': 1 KB region '10': 2 KB region '11': 4 KB region '12': 8 KB region '13': 16 KB region '14': 32 KB region '15': 64 KB region '16': 128 KB region '17': 256 KB region '18': 512 KB region '19': 1 MB region '20': 2 MB region '21': 4 MB region '22': 8 MB region '23': 16 MB region '24': 32 MB region '25': 64 MB region '26': 128 MB region '27': 256 MB region '28': 512 MB region '29': 1 GB region '30': 2 GB region '31': 4 GB region |
| 30 | PC_MATCH | RW | R | Undefined | This field specifies if the PC field participates in the 'matching' process or the 'access evaluation' process: '0': PC field participates in 'access evaluation'. '1': PC field participates in 'matching'. 'Matching' process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the 'matching' regions. 'Access evaluation' process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes. Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. |
| 31 | ENABLED | RW | R | 0 | Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. |

22.5.1.8.3 PROT_SMPU_SMPU_STRUCT_ADDR1

Description: SMPU region address 1 (master structure)
Address: 0x40232020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment: This register defines a SMPU address region. The address region is fixed, the region size is 64 B (two 32 B subregions within a 256 B region) and includes the ADDR0, ATT0, ADDR1 and ATT0 registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | SUBREGION_DISABLE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | ADDR24 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | ADDR24 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ADDR24 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|------------------------|---|
| 0:7 | SUBREGION_DISABLE | R | R | SUBREGION_DISABLE_DEF1 | <p>This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable:</p> <p>Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable.</p> <p>Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1.</p> <p>Note: this field is read-only.</p> |
| 8:31 | ADDR24 | R | R | ADDR_DEF1 | <p>This field specifies the most significant bits of the 32-bit address of an address region.</p> <p>'ADDR_DEF1': base address of structure.</p> <p>Note: this field is read-only.</p> |

22.5.1.8.4 PROT_SMPU_SMPU_STRUCT_ATT1

Description: SMPU region attributes 1 (master structure)
Address: 0x40232024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment: This register defines SMPU access control.
Default: 0x7000109

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----------|----------|----------|----------|----------|----------|----------|
| Name | None [7:7] | NS [6:6] | PX [5:5] | PW [4:4] | PR [3:3] | UX [2:2] | UW [1:1] | UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----|----|----|----|----|----|---|-----------------|
| Name | | | | | | | | PC_MASK_0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | PC_MASK_15_TO_1 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|------------------|--------------|---------------------|----|----|----|----|
| Name | ENABLED [31:31] | PC_MATCH [30:30] | None [29:29] | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | UR | R | R | 1 | User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. |
| 1 | UW | RW | R | Undefined | User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | UX | R | R | 0 | User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. |
| 3 | PR | R | R | 1 | Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. |
| 4 | PW | RW | R | Undefined | Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 5 | PX | R | R | 0 | Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. |
| 6 | NS | RW | R | Undefined | Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |
| 8 | PC_MASK_0 | R | R | 1 | This field specifies protection context identifier based access control for protection context '0'. |
| 9:23 | PC_MASK_15_TO_1 | RW | R | Undefined | This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. |
| 24:28 | REGION_SIZE | R | R | 7 | This field specifies the region size: '7': 256 B region (8 32 B subregions) Note: this field is read-only. |
| 30 | PC_MATCH | RW | R | Undefined | This field specifies if the PC field participates in the 'matching' process or the 'access evaluation' process: '0': PC field participates in 'access evaluation'. '1': PC field participates in 'matching'. 'Matching' process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the 'matching' regions. 'Access evaluation' process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes. Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. |
| 31 | ENABLED | RW | R | 0 | Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. |

22.5.2 MPU

22.5.2.1 PROT_MPU_MS_CTL

Description: Master control
Address: 0x40234000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------|---|---|---|
| Name | None [7:4] | | | | PC [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|------------------|----|----|----|
| Name | None [23:20] | | | | PC_SAVED [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:3 | PC | RW | RW | 0 | <p>Active protection context (PC). Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context '0' can change this field (protection context 0 has unrestricted access).</p> <p>The CM0+ MPU MS_CTL register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the MPU MS_CTL.PC field is modifiable by SW ONLY. For CM0+ PC field HW modifications, the following holds:</p> <p>* On entry of a CM0_PC0/1/2/3_HANDLER exception/interrupt handler: IF (the new PC is the same as MS_CTL.PC) PC is not affected; PC_SAVED is not affected. ELSE IF (CM0_PC_CTL.VALID[MS_CTL.PC]) An AHB-Lite bus error is generated for the exception handler fetch; PC is not affected; PC_SAVED is not affected. ELSE PC = 'new PC'; PC_SAVED = PC (push operation). * On entry of any other exception/interrupt handler: PC = PC_SAVED; PC_SAVED is not affected (pop operation).</p> <p>Note that the CM0_PC0/1/2/3_HANDLER and CM0_PC_CTL registers are part of repetitive CPUSS MMIO registers.</p> <p>Note: this field is NOT used by the DW controllers, DMA controller, AXI DMA controller, CRYPTO component and VIDEOSS.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|---|
| 16:19 | PC_SAVED | RW | RW | 0 | <p>Saved protection context. Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields.</p> <p>Note: this field is ONLY used by the CM0+.</p> |

22.5.2.2 PROT_MPU_MS_CTL_READ_MIR

Description: Master control read mirror
Address: 0x40234004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|----------|---|---|---|
| Name | None [7:4] | | | | PC [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|------------------|----|----|----|
| Name | None [23:20] | | | | PC_SAVED [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|-------------------------------------|
| 0:3 | PC | R | W | 0 | Read-only mirror of MS_CTL.PC |
| 16:19 | PC_SAVED | R | W | 0 | Read-only mirror of MS_CTL.PC_SAVED |

22.5.2.3 MPU_STRUCT

22.5.2.3.1 PROT_MPU_MPU_STRUCT_ADDR

Description: MPU region address
Address: 0x40234200
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: This register defines a MPU address region.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------------|----|----|----|----|----|----|----|
| Name | SUBREGION_DISABLE [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | ADDR24 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | ADDR24 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ADDR24 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|--|
| 0:7 | SUBREGION_DISABLE | RW | R | Undefined | <p>This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable:</p> <p>Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable.</p> <p>E.g., a 64 KByte address region (REGION_SIZE is '15') has eight 8 KByte subregions. The access control as defined by MPU_REGION_ATT applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B.</p> |
| 8:31 | ADDR24 | RW | R | Undefined | <p>This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is '15') is 64 KByte aligned, and ADDR24[7:0] are ignored.</p> |

22.5.2.3.2 PROT_MPU_MPU_STRUCT_ATT

Description: MPU region attributes
Address: 0x40234204
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: This register defines a MPU access control register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----------|----------|----------|----------|----------|----------|----------|
| Name | None [7:7] | NS [6:6] | PX [5:5] | PW [4:4] | PR [3:3] | UX [2:2] | UW [1:1] | UR [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|---------------------|----|----|----|----|
| Name | ENABLED [31:31] | None [30:29] | | REGION_SIZE [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | UR | RW | R | Undefined | User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). |
| 1 | UW | RW | R | Undefined | User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). |
| 2 | UX | RW | R | Undefined | User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). |
| 3 | PR | RW | R | Undefined | Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). |
| 4 | PW | RW | R | Undefined | Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). |
| 5 | PX | RW | R | Undefined | Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). |
| 6 | NS | RW | R | Undefined | Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|--|
| 24:28 | REGION_SIZE | RW | R | Undefined | <p>This field specifies the region size:</p> <p>'0'-'6': Undefined. '7': 256 B region '8': 512 B region '9': 1 KB region '10': 2 KB region '11': 4 KB region '12': 8 KB region '13': 16 KB region '14': 32 KB region '15': 64 KB region '16': 128 KB region '17': 256 KB region '18': 512 KB region '19': 1 MB region '20': 2 MB region '21': 4 MB region '22': 8 MB region '23': 16 MB region '24': 32 MB region '25': 64 MB region '26': 128 MB region '27': 256 MB region '28': 512 MB region '30': 2 GB region '31': 4 GB region</p> |
| 31 | ENABLED | RW | R | 0 | <p>Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled.</p> <p>Note: a disabled address region performs logic gating to reduce dynamic power consumption.</p> |

23 SCB

23.1 SCB 0

| | |
|---------------------|---|
| Description | Serial Communications Block (SPI/UART/I2C) |
| Base Address | 0x40600000 |
| Size | 0x10000 |
| Slave Num | MMIO6 - 0 |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|---------------------------|
| SCB0_CTRL | 0x40600000 | FULL | Generic control |
| SCB0_STATUS | 0x40600004 | FULL | Generic status |
| SCB0_CMD_RESP_CTRL | 0x40600008 | FULL | Command/response control |
| SCB0_CMD_RESP_STATUS | 0x4060000C | FULL | Command/response status |
| SCB0_SPI_CTRL | 0x40600020 | FULL | SPI control |
| SCB0_SPI_STATUS | 0x40600024 | FULL | SPI status |
| SCB0_SPI_TX_CTRL | 0x40600028 | FULL | SPI transmitter control |
| SCB0_SPI_RX_CTRL | 0x4060002C | FULL | SPI receiver control |
| SCB0_UART_CTRL | 0x40600040 | FULL | UART control |
| SCB0_UART_TX_CTRL | 0x40600044 | FULL | UART transmitter control |
| SCB0_UART_RX_CTRL | 0x40600048 | FULL | UART receiver control |
| SCB0_UART_RX_STATUS | 0x4060004C | FULL | UART receiver status |
| SCB0_UART_FLOW_CTRL | 0x40600050 | FULL | UART flow control |
| SCB0_I2C_CTRL | 0x40600060 | FULL | I2C control |
| SCB0_I2C_STATUS | 0x40600064 | FULL | I2C status |
| SCB0_I2C_M_CMD | 0x40600068 | FULL | I2C master command |
| SCB0_I2C_S_CMD | 0x4060006C | FULL | I2C slave command |
| SCB0_I2C_CFG | 0x40600070 | FULL | I2C configuration |
| SCB0_TX_CTRL | 0x40600200 | FULL | Transmitter control |
| SCB0_TX_FIFO_CTRL | 0x40600204 | FULL | Transmitter FIFO control |
| SCB0_TX_FIFO_STATUS | 0x40600208 | FULL | Transmitter FIFO status |
| SCB0_TX_FIFO_WR | 0x40600240 | FULL | Transmitter FIFO write |
| SCB0_RX_CTRL | 0x40600300 | FULL | Receiver control |
| SCB0_RX_FIFO_CTRL | 0x40600304 | FULL | Receiver FIFO control |
| SCB0_RX_FIFO_STATUS | 0x40600308 | FULL | Receiver FIFO status |
| SCB0_RX_MATCH | 0x40600310 | FULL | Slave address and mask |
| SCB0_RX_FIFO_RD | 0x40600340 | FULL | Receiver FIFO read |
| SCB0_RX_FIFO_RD_SILENT | 0x40600344 | FULL | Receiver FIFO read silent |
| SCB0_EZ_DATA0 | 0x40600400 | FULL | Memory buffer |
| SCB0_EZ_DATA1 | 0x40600404 | FULL | Memory buffer |
| SCB0_EZ_DATA2 | 0x40600408 | FULL | Memory buffer |
| SCB0_EZ_DATA3 | 0x4060040C | FULL | Memory buffer |
| SCB0_EZ_DATA4 | 0x40600410 | FULL | Memory buffer |
| SCB0_EZ_DATA5 | 0x40600414 | FULL | Memory buffer |
| SCB0_EZ_DATA6 | 0x40600418 | FULL | Memory buffer |
| SCB0_EZ_DATA7 | 0x4060041C | FULL | Memory buffer |
| SCB0_EZ_DATA8 | 0x40600420 | FULL | Memory buffer |
| SCB0_EZ_DATA9 | 0x40600424 | FULL | Memory buffer |
| SCB0_EZ_DATA10 | 0x40600428 | FULL | Memory buffer |
| SCB0_EZ_DATA11 | 0x4060042C | FULL | Memory buffer |
| SCB0_EZ_DATA12 | 0x40600430 | FULL | Memory buffer |
| SCB0_EZ_DATA13 | 0x40600434 | FULL | Memory buffer |
| SCB0_EZ_DATA14 | 0x40600438 | FULL | Memory buffer |
| SCB0_EZ_DATA15 | 0x4060043C | FULL | Memory buffer |
| SCB0_EZ_DATA16 | 0x40600440 | FULL | Memory buffer |
| SCB0_EZ_DATA17 | 0x40600444 | FULL | Memory buffer |
| SCB0_EZ_DATA18 | 0x40600448 | FULL | Memory buffer |
| SCB0_EZ_DATA19 | 0x4060044C | FULL | Memory buffer |
| SCB0_EZ_DATA20 | 0x40600450 | FULL | Memory buffer |
| SCB0_EZ_DATA21 | 0x40600454 | FULL | Memory buffer |
| SCB0_EZ_DATA22 | 0x40600458 | FULL | Memory buffer |
| SCB0_EZ_DATA23 | 0x4060045C | FULL | Memory buffer |
| SCB0_EZ_DATA24 | 0x40600460 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB0_EZ_DATA25 | 0x40600464 | FULL | Memory buffer |
| SCB0_EZ_DATA26 | 0x40600468 | FULL | Memory buffer |
| SCB0_EZ_DATA27 | 0x4060046C | FULL | Memory buffer |
| SCB0_EZ_DATA28 | 0x40600470 | FULL | Memory buffer |
| SCB0_EZ_DATA29 | 0x40600474 | FULL | Memory buffer |
| SCB0_EZ_DATA30 | 0x40600478 | FULL | Memory buffer |
| SCB0_EZ_DATA31 | 0x4060047C | FULL | Memory buffer |
| SCB0_EZ_DATA32 | 0x40600480 | FULL | Memory buffer |
| SCB0_EZ_DATA33 | 0x40600484 | FULL | Memory buffer |
| SCB0_EZ_DATA34 | 0x40600488 | FULL | Memory buffer |
| SCB0_EZ_DATA35 | 0x4060048C | FULL | Memory buffer |
| SCB0_EZ_DATA36 | 0x40600490 | FULL | Memory buffer |
| SCB0_EZ_DATA37 | 0x40600494 | FULL | Memory buffer |
| SCB0_EZ_DATA38 | 0x40600498 | FULL | Memory buffer |
| SCB0_EZ_DATA39 | 0x4060049C | FULL | Memory buffer |
| SCB0_EZ_DATA40 | 0x406004A0 | FULL | Memory buffer |
| SCB0_EZ_DATA41 | 0x406004A4 | FULL | Memory buffer |
| SCB0_EZ_DATA42 | 0x406004A8 | FULL | Memory buffer |
| SCB0_EZ_DATA43 | 0x406004AC | FULL | Memory buffer |
| SCB0_EZ_DATA44 | 0x406004B0 | FULL | Memory buffer |
| SCB0_EZ_DATA45 | 0x406004B4 | FULL | Memory buffer |
| SCB0_EZ_DATA46 | 0x406004B8 | FULL | Memory buffer |
| SCB0_EZ_DATA47 | 0x406004BC | FULL | Memory buffer |
| SCB0_EZ_DATA48 | 0x406004C0 | FULL | Memory buffer |
| SCB0_EZ_DATA49 | 0x406004C4 | FULL | Memory buffer |
| SCB0_EZ_DATA50 | 0x406004C8 | FULL | Memory buffer |
| SCB0_EZ_DATA51 | 0x406004CC | FULL | Memory buffer |
| SCB0_EZ_DATA52 | 0x406004D0 | FULL | Memory buffer |
| SCB0_EZ_DATA53 | 0x406004D4 | FULL | Memory buffer |
| SCB0_EZ_DATA54 | 0x406004D8 | FULL | Memory buffer |
| SCB0_EZ_DATA55 | 0x406004DC | FULL | Memory buffer |
| SCB0_EZ_DATA56 | 0x406004E0 | FULL | Memory buffer |
| SCB0_EZ_DATA57 | 0x406004E4 | FULL | Memory buffer |
| SCB0_EZ_DATA58 | 0x406004E8 | FULL | Memory buffer |
| SCB0_EZ_DATA59 | 0x406004EC | FULL | Memory buffer |
| SCB0_EZ_DATA60 | 0x406004F0 | FULL | Memory buffer |
| SCB0_EZ_DATA61 | 0x406004F4 | FULL | Memory buffer |
| SCB0_EZ_DATA62 | 0x406004F8 | FULL | Memory buffer |
| SCB0_EZ_DATA63 | 0x406004FC | FULL | Memory buffer |
| SCB0_EZ_DATA64 | 0x40600500 | FULL | Memory buffer |
| SCB0_EZ_DATA65 | 0x40600504 | FULL | Memory buffer |
| SCB0_EZ_DATA66 | 0x40600508 | FULL | Memory buffer |
| SCB0_EZ_DATA67 | 0x4060050C | FULL | Memory buffer |
| SCB0_EZ_DATA68 | 0x40600510 | FULL | Memory buffer |
| SCB0_EZ_DATA69 | 0x40600514 | FULL | Memory buffer |
| SCB0_EZ_DATA70 | 0x40600518 | FULL | Memory buffer |
| SCB0_EZ_DATA71 | 0x4060051C | FULL | Memory buffer |
| SCB0_EZ_DATA72 | 0x40600520 | FULL | Memory buffer |
| SCB0_EZ_DATA73 | 0x40600524 | FULL | Memory buffer |
| SCB0_EZ_DATA74 | 0x40600528 | FULL | Memory buffer |
| SCB0_EZ_DATA75 | 0x4060052C | FULL | Memory buffer |
| SCB0_EZ_DATA76 | 0x40600530 | FULL | Memory buffer |
| SCB0_EZ_DATA77 | 0x40600534 | FULL | Memory buffer |
| SCB0_EZ_DATA78 | 0x40600538 | FULL | Memory buffer |
| SCB0_EZ_DATA79 | 0x4060053C | FULL | Memory buffer |
| SCB0_EZ_DATA80 | 0x40600540 | FULL | Memory buffer |
| SCB0_EZ_DATA81 | 0x40600544 | FULL | Memory buffer |
| SCB0_EZ_DATA82 | 0x40600548 | FULL | Memory buffer |
| SCB0_EZ_DATA83 | 0x4060054C | FULL | Memory buffer |
| SCB0_EZ_DATA84 | 0x40600550 | FULL | Memory buffer |
| SCB0_EZ_DATA85 | 0x40600554 | FULL | Memory buffer |
| SCB0_EZ_DATA86 | 0x40600558 | FULL | Memory buffer |
| SCB0_EZ_DATA87 | 0x4060055C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB0_EZ_DATA88 | 0x40600560 | FULL | Memory buffer |
| SCB0_EZ_DATA89 | 0x40600564 | FULL | Memory buffer |
| SCB0_EZ_DATA90 | 0x40600568 | FULL | Memory buffer |
| SCB0_EZ_DATA91 | 0x4060056C | FULL | Memory buffer |
| SCB0_EZ_DATA92 | 0x40600570 | FULL | Memory buffer |
| SCB0_EZ_DATA93 | 0x40600574 | FULL | Memory buffer |
| SCB0_EZ_DATA94 | 0x40600578 | FULL | Memory buffer |
| SCB0_EZ_DATA95 | 0x4060057C | FULL | Memory buffer |
| SCB0_EZ_DATA96 | 0x40600580 | FULL | Memory buffer |
| SCB0_EZ_DATA97 | 0x40600584 | FULL | Memory buffer |
| SCB0_EZ_DATA98 | 0x40600588 | FULL | Memory buffer |
| SCB0_EZ_DATA99 | 0x4060058C | FULL | Memory buffer |
| SCB0_EZ_DATA100 | 0x40600590 | FULL | Memory buffer |
| SCB0_EZ_DATA101 | 0x40600594 | FULL | Memory buffer |
| SCB0_EZ_DATA102 | 0x40600598 | FULL | Memory buffer |
| SCB0_EZ_DATA103 | 0x4060059C | FULL | Memory buffer |
| SCB0_EZ_DATA104 | 0x406005A0 | FULL | Memory buffer |
| SCB0_EZ_DATA105 | 0x406005A4 | FULL | Memory buffer |
| SCB0_EZ_DATA106 | 0x406005A8 | FULL | Memory buffer |
| SCB0_EZ_DATA107 | 0x406005AC | FULL | Memory buffer |
| SCB0_EZ_DATA108 | 0x406005B0 | FULL | Memory buffer |
| SCB0_EZ_DATA109 | 0x406005B4 | FULL | Memory buffer |
| SCB0_EZ_DATA110 | 0x406005B8 | FULL | Memory buffer |
| SCB0_EZ_DATA111 | 0x406005BC | FULL | Memory buffer |
| SCB0_EZ_DATA112 | 0x406005C0 | FULL | Memory buffer |
| SCB0_EZ_DATA113 | 0x406005C4 | FULL | Memory buffer |
| SCB0_EZ_DATA114 | 0x406005C8 | FULL | Memory buffer |
| SCB0_EZ_DATA115 | 0x406005CC | FULL | Memory buffer |
| SCB0_EZ_DATA116 | 0x406005D0 | FULL | Memory buffer |
| SCB0_EZ_DATA117 | 0x406005D4 | FULL | Memory buffer |
| SCB0_EZ_DATA118 | 0x406005D8 | FULL | Memory buffer |
| SCB0_EZ_DATA119 | 0x406005DC | FULL | Memory buffer |
| SCB0_EZ_DATA120 | 0x406005E0 | FULL | Memory buffer |
| SCB0_EZ_DATA121 | 0x406005E4 | FULL | Memory buffer |
| SCB0_EZ_DATA122 | 0x406005E8 | FULL | Memory buffer |
| SCB0_EZ_DATA123 | 0x406005EC | FULL | Memory buffer |
| SCB0_EZ_DATA124 | 0x406005F0 | FULL | Memory buffer |
| SCB0_EZ_DATA125 | 0x406005F4 | FULL | Memory buffer |
| SCB0_EZ_DATA126 | 0x406005F8 | FULL | Memory buffer |
| SCB0_EZ_DATA127 | 0x406005FC | FULL | Memory buffer |
| SCB0_EZ_DATA128 | 0x40600600 | FULL | Memory buffer |
| SCB0_EZ_DATA129 | 0x40600604 | FULL | Memory buffer |
| SCB0_EZ_DATA130 | 0x40600608 | FULL | Memory buffer |
| SCB0_EZ_DATA131 | 0x4060060C | FULL | Memory buffer |
| SCB0_EZ_DATA132 | 0x40600610 | FULL | Memory buffer |
| SCB0_EZ_DATA133 | 0x40600614 | FULL | Memory buffer |
| SCB0_EZ_DATA134 | 0x40600618 | FULL | Memory buffer |
| SCB0_EZ_DATA135 | 0x4060061C | FULL | Memory buffer |
| SCB0_EZ_DATA136 | 0x40600620 | FULL | Memory buffer |
| SCB0_EZ_DATA137 | 0x40600624 | FULL | Memory buffer |
| SCB0_EZ_DATA138 | 0x40600628 | FULL | Memory buffer |
| SCB0_EZ_DATA139 | 0x4060062C | FULL | Memory buffer |
| SCB0_EZ_DATA140 | 0x40600630 | FULL | Memory buffer |
| SCB0_EZ_DATA141 | 0x40600634 | FULL | Memory buffer |
| SCB0_EZ_DATA142 | 0x40600638 | FULL | Memory buffer |
| SCB0_EZ_DATA143 | 0x4060063C | FULL | Memory buffer |
| SCB0_EZ_DATA144 | 0x40600640 | FULL | Memory buffer |
| SCB0_EZ_DATA145 | 0x40600644 | FULL | Memory buffer |
| SCB0_EZ_DATA146 | 0x40600648 | FULL | Memory buffer |
| SCB0_EZ_DATA147 | 0x4060064C | FULL | Memory buffer |
| SCB0_EZ_DATA148 | 0x40600650 | FULL | Memory buffer |
| SCB0_EZ_DATA149 | 0x40600654 | FULL | Memory buffer |
| SCB0_EZ_DATA150 | 0x40600658 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB0_EZ_DATA151 | 0x4060065C | FULL | Memory buffer |
| SCB0_EZ_DATA152 | 0x40600660 | FULL | Memory buffer |
| SCB0_EZ_DATA153 | 0x40600664 | FULL | Memory buffer |
| SCB0_EZ_DATA154 | 0x40600668 | FULL | Memory buffer |
| SCB0_EZ_DATA155 | 0x4060066C | FULL | Memory buffer |
| SCB0_EZ_DATA156 | 0x40600670 | FULL | Memory buffer |
| SCB0_EZ_DATA157 | 0x40600674 | FULL | Memory buffer |
| SCB0_EZ_DATA158 | 0x40600678 | FULL | Memory buffer |
| SCB0_EZ_DATA159 | 0x4060067C | FULL | Memory buffer |
| SCB0_EZ_DATA160 | 0x40600680 | FULL | Memory buffer |
| SCB0_EZ_DATA161 | 0x40600684 | FULL | Memory buffer |
| SCB0_EZ_DATA162 | 0x40600688 | FULL | Memory buffer |
| SCB0_EZ_DATA163 | 0x4060068C | FULL | Memory buffer |
| SCB0_EZ_DATA164 | 0x40600690 | FULL | Memory buffer |
| SCB0_EZ_DATA165 | 0x40600694 | FULL | Memory buffer |
| SCB0_EZ_DATA166 | 0x40600698 | FULL | Memory buffer |
| SCB0_EZ_DATA167 | 0x4060069C | FULL | Memory buffer |
| SCB0_EZ_DATA168 | 0x406006A0 | FULL | Memory buffer |
| SCB0_EZ_DATA169 | 0x406006A4 | FULL | Memory buffer |
| SCB0_EZ_DATA170 | 0x406006A8 | FULL | Memory buffer |
| SCB0_EZ_DATA171 | 0x406006AC | FULL | Memory buffer |
| SCB0_EZ_DATA172 | 0x406006B0 | FULL | Memory buffer |
| SCB0_EZ_DATA173 | 0x406006B4 | FULL | Memory buffer |
| SCB0_EZ_DATA174 | 0x406006B8 | FULL | Memory buffer |
| SCB0_EZ_DATA175 | 0x406006BC | FULL | Memory buffer |
| SCB0_EZ_DATA176 | 0x406006C0 | FULL | Memory buffer |
| SCB0_EZ_DATA177 | 0x406006C4 | FULL | Memory buffer |
| SCB0_EZ_DATA178 | 0x406006C8 | FULL | Memory buffer |
| SCB0_EZ_DATA179 | 0x406006CC | FULL | Memory buffer |
| SCB0_EZ_DATA180 | 0x406006D0 | FULL | Memory buffer |
| SCB0_EZ_DATA181 | 0x406006D4 | FULL | Memory buffer |
| SCB0_EZ_DATA182 | 0x406006D8 | FULL | Memory buffer |
| SCB0_EZ_DATA183 | 0x406006DC | FULL | Memory buffer |
| SCB0_EZ_DATA184 | 0x406006E0 | FULL | Memory buffer |
| SCB0_EZ_DATA185 | 0x406006E4 | FULL | Memory buffer |
| SCB0_EZ_DATA186 | 0x406006E8 | FULL | Memory buffer |
| SCB0_EZ_DATA187 | 0x406006EC | FULL | Memory buffer |
| SCB0_EZ_DATA188 | 0x406006F0 | FULL | Memory buffer |
| SCB0_EZ_DATA189 | 0x406006F4 | FULL | Memory buffer |
| SCB0_EZ_DATA190 | 0x406006F8 | FULL | Memory buffer |
| SCB0_EZ_DATA191 | 0x406006FC | FULL | Memory buffer |
| SCB0_EZ_DATA192 | 0x40600700 | FULL | Memory buffer |
| SCB0_EZ_DATA193 | 0x40600704 | FULL | Memory buffer |
| SCB0_EZ_DATA194 | 0x40600708 | FULL | Memory buffer |
| SCB0_EZ_DATA195 | 0x4060070C | FULL | Memory buffer |
| SCB0_EZ_DATA196 | 0x40600710 | FULL | Memory buffer |
| SCB0_EZ_DATA197 | 0x40600714 | FULL | Memory buffer |
| SCB0_EZ_DATA198 | 0x40600718 | FULL | Memory buffer |
| SCB0_EZ_DATA199 | 0x4060071C | FULL | Memory buffer |
| SCB0_EZ_DATA200 | 0x40600720 | FULL | Memory buffer |
| SCB0_EZ_DATA201 | 0x40600724 | FULL | Memory buffer |
| SCB0_EZ_DATA202 | 0x40600728 | FULL | Memory buffer |
| SCB0_EZ_DATA203 | 0x4060072C | FULL | Memory buffer |
| SCB0_EZ_DATA204 | 0x40600730 | FULL | Memory buffer |
| SCB0_EZ_DATA205 | 0x40600734 | FULL | Memory buffer |
| SCB0_EZ_DATA206 | 0x40600738 | FULL | Memory buffer |
| SCB0_EZ_DATA207 | 0x4060073C | FULL | Memory buffer |
| SCB0_EZ_DATA208 | 0x40600740 | FULL | Memory buffer |
| SCB0_EZ_DATA209 | 0x40600744 | FULL | Memory buffer |
| SCB0_EZ_DATA210 | 0x40600748 | FULL | Memory buffer |
| SCB0_EZ_DATA211 | 0x4060074C | FULL | Memory buffer |
| SCB0_EZ_DATA212 | 0x40600750 | FULL | Memory buffer |
| SCB0_EZ_DATA213 | 0x40600754 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|--|
| SCB0_EZ_DATA214 | 0x40600758 | FULL | Memory buffer |
| SCB0_EZ_DATA215 | 0x4060075C | FULL | Memory buffer |
| SCB0_EZ_DATA216 | 0x40600760 | FULL | Memory buffer |
| SCB0_EZ_DATA217 | 0x40600764 | FULL | Memory buffer |
| SCB0_EZ_DATA218 | 0x40600768 | FULL | Memory buffer |
| SCB0_EZ_DATA219 | 0x4060076C | FULL | Memory buffer |
| SCB0_EZ_DATA220 | 0x40600770 | FULL | Memory buffer |
| SCB0_EZ_DATA221 | 0x40600774 | FULL | Memory buffer |
| SCB0_EZ_DATA222 | 0x40600778 | FULL | Memory buffer |
| SCB0_EZ_DATA223 | 0x4060077C | FULL | Memory buffer |
| SCB0_EZ_DATA224 | 0x40600780 | FULL | Memory buffer |
| SCB0_EZ_DATA225 | 0x40600784 | FULL | Memory buffer |
| SCB0_EZ_DATA226 | 0x40600788 | FULL | Memory buffer |
| SCB0_EZ_DATA227 | 0x4060078C | FULL | Memory buffer |
| SCB0_EZ_DATA228 | 0x40600790 | FULL | Memory buffer |
| SCB0_EZ_DATA229 | 0x40600794 | FULL | Memory buffer |
| SCB0_EZ_DATA230 | 0x40600798 | FULL | Memory buffer |
| SCB0_EZ_DATA231 | 0x4060079C | FULL | Memory buffer |
| SCB0_EZ_DATA232 | 0x406007A0 | FULL | Memory buffer |
| SCB0_EZ_DATA233 | 0x406007A4 | FULL | Memory buffer |
| SCB0_EZ_DATA234 | 0x406007A8 | FULL | Memory buffer |
| SCB0_EZ_DATA235 | 0x406007AC | FULL | Memory buffer |
| SCB0_EZ_DATA236 | 0x406007B0 | FULL | Memory buffer |
| SCB0_EZ_DATA237 | 0x406007B4 | FULL | Memory buffer |
| SCB0_EZ_DATA238 | 0x406007B8 | FULL | Memory buffer |
| SCB0_EZ_DATA239 | 0x406007BC | FULL | Memory buffer |
| SCB0_EZ_DATA240 | 0x406007C0 | FULL | Memory buffer |
| SCB0_EZ_DATA241 | 0x406007C4 | FULL | Memory buffer |
| SCB0_EZ_DATA242 | 0x406007C8 | FULL | Memory buffer |
| SCB0_EZ_DATA243 | 0x406007CC | FULL | Memory buffer |
| SCB0_EZ_DATA244 | 0x406007D0 | FULL | Memory buffer |
| SCB0_EZ_DATA245 | 0x406007D4 | FULL | Memory buffer |
| SCB0_EZ_DATA246 | 0x406007D8 | FULL | Memory buffer |
| SCB0_EZ_DATA247 | 0x406007DC | FULL | Memory buffer |
| SCB0_EZ_DATA248 | 0x406007E0 | FULL | Memory buffer |
| SCB0_EZ_DATA249 | 0x406007E4 | FULL | Memory buffer |
| SCB0_EZ_DATA250 | 0x406007E8 | FULL | Memory buffer |
| SCB0_EZ_DATA251 | 0x406007EC | FULL | Memory buffer |
| SCB0_EZ_DATA252 | 0x406007F0 | FULL | Memory buffer |
| SCB0_EZ_DATA253 | 0x406007F4 | FULL | Memory buffer |
| SCB0_EZ_DATA254 | 0x406007F8 | FULL | Memory buffer |
| SCB0_EZ_DATA255 | 0x406007FC | FULL | Memory buffer |
| SCB0_INTR_CAUSE | 0x40600E00 | FULL | Active clocked interrupt signal |
| SCB0_INTR_I2C_EC | 0x40600E80 | FULL | Externally clocked I2C interrupt request |
| SCB0_INTR_I2C_EC_MASK | 0x40600E88 | FULL | Externally clocked I2C interrupt mask |
| SCB0_INTR_I2C_EC_MASKED | 0x40600E8C | FULL | Externally clocked I2C interrupt masked |
| SCB0_INTR_SPI_EC | 0x40600EC0 | FULL | Externally clocked SPI interrupt request |
| SCB0_INTR_SPI_EC_MASK | 0x40600EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB0_INTR_SPI_EC_MASKED | 0x40600ECC | FULL | Externally clocked SPI interrupt masked |
| SCB0_INTR_M | 0x40600F00 | FULL | Master interrupt request |
| SCB0_INTR_M_SET | 0x40600F04 | FULL | Master interrupt set request |
| SCB0_INTR_M_MASK | 0x40600F08 | FULL | Master interrupt mask |
| SCB0_INTR_M_MASKED | 0x40600F0C | FULL | Master interrupt masked request |
| SCB0_INTR_S | 0x40600F40 | FULL | Slave interrupt request |
| SCB0_INTR_S_SET | 0x40600F44 | FULL | Slave interrupt set request |
| SCB0_INTR_S_MASK | 0x40600F48 | FULL | Slave interrupt mask |
| SCB0_INTR_S_MASKED | 0x40600F4C | FULL | Slave interrupt masked request |
| SCB0_INTR_TX | 0x40600F80 | FULL | Transmitter interrupt request |
| SCB0_INTR_TX_SET | 0x40600F84 | FULL | Transmitter interrupt set request |
| SCB0_INTR_TX_MASK | 0x40600F88 | FULL | Transmitter interrupt mask |
| SCB0_INTR_TX_MASKED | 0x40600F8C | FULL | Transmitter interrupt masked request |
| SCB0_INTR_RX | 0x40600FC0 | FULL | Receiver interrupt request |
| SCB0_INTR_RX_SET | 0x40600FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|-----------------------------------|
| SCB0_INTR_RX_MASK | 0x40600FC8 | FULL | Receiver interrupt mask |
| SCB0_INTR_RX_MASKED | 0x40600FCC | FULL | Receiver interrupt masked request |

23.2 SCB 1

Description Serial Communications Block
(SPI/UART/I2C)
Base Address 0x40610000
Size 0x10000
Slave Num MMIO6 - 1

| Register Name | Address | Permission | Description |
|--|------------|------------|--|
| SCB1_CTRL | 0x40610000 | FULL | Generic control Note: CMD_RESP_MODE is not available for this register |
| SCB1_STATUS | 0x40610004 | FULL | Generic status |
| SCB1_SPI_CTRL | 0x40610020 | FULL | SPI control |
| SCB1_SPI_STATUS | 0x40610024 | FULL | SPI status |
| SCB1_SPI_TX_CTRL | 0x40610028 | FULL | SPI transmitter control |
| SCB1_SPI_RX_CTRL | 0x4061002C | FULL | SPI receiver control |
| SCB1_UART_CTRL | 0x40610040 | FULL | UART control |
| SCB1_UART_TX_CTRL | 0x40610044 | FULL | UART transmitter control |
| SCB1_UART_RX_CTRL | 0x40610048 | FULL | UART receiver control |
| SCB1_UART_RX_STATUS | 0x4061004C | FULL | UART receiver status |
| SCB1_UART_FLOW_CTRL | 0x40610050 | FULL | UART flow control |
| SCB1_I2C_CTRL | 0x40610060 | FULL | I2C control |
| SCB1_I2C_STATUS | 0x40610064 | FULL | I2C status Note: I2C_EC_BUSY is not available for this register |
| SCB1_I2C_M_CMD | 0x40610068 | FULL | I2C master command |
| SCB1_I2C_S_CMD | 0x4061006C | FULL | I2C slave command |
| SCB1_I2C_CFG | 0x40610070 | FULL | I2C configuration |
| SCB1_TX_CTRL | 0x40610200 | FULL | Transmitter control |
| SCB1_TX_FIFO_CTRL | 0x40610204 | FULL | Transmitter FIFO control |
| SCB1_TX_FIFO_STATUS | 0x40610208 | FULL | Transmitter FIFO status |
| SCB1_TX_FIFO_WR | 0x40610240 | FULL | Transmitter FIFO write |
| SCB1_RX_CTRL | 0x40610300 | FULL | Receiver control |
| SCB1_RX_FIFO_CTRL | 0x40610304 | FULL | Receiver FIFO control |
| SCB1_RX_FIFO_STATUS | 0x40610308 | FULL | Receiver FIFO status |
| SCB1_RX_MATCH | 0x40610310 | FULL | Slave address and mask |
| SCB1_RX_FIFO_RD | 0x40610340 | FULL | Receiver FIFO read |
| SCB1_RX_FIFO_RD_SILENT | 0x40610344 | FULL | Receiver FIFO read silent |
| SCB1_EZ_DATA0 | 0x40610400 | FULL | Memory buffer |
| SCB1_EZ_DATA1 | 0x40610404 | FULL | Memory buffer |
| SCB1_EZ_DATA2 | 0x40610408 | FULL | Memory buffer |
| SCB1_EZ_DATA3 | 0x4061040C | FULL | Memory buffer |
| SCB1_EZ_DATA4 | 0x40610410 | FULL | Memory buffer |
| SCB1_EZ_DATA5 | 0x40610414 | FULL | Memory buffer |
| SCB1_EZ_DATA6 | 0x40610418 | FULL | Memory buffer |
| SCB1_EZ_DATA7 | 0x4061041C | FULL | Memory buffer |
| SCB1_EZ_DATA8 | 0x40610420 | FULL | Memory buffer |
| SCB1_EZ_DATA9 | 0x40610424 | FULL | Memory buffer |
| SCB1_EZ_DATA10 | 0x40610428 | FULL | Memory buffer |
| SCB1_EZ_DATA11 | 0x4061042C | FULL | Memory buffer |
| SCB1_EZ_DATA12 | 0x40610430 | FULL | Memory buffer |
| SCB1_EZ_DATA13 | 0x40610434 | FULL | Memory buffer |
| SCB1_EZ_DATA14 | 0x40610438 | FULL | Memory buffer |
| SCB1_EZ_DATA15 | 0x4061043C | FULL | Memory buffer |
| SCB1_EZ_DATA16 | 0x40610440 | FULL | Memory buffer |
| SCB1_EZ_DATA17 | 0x40610444 | FULL | Memory buffer |
| SCB1_EZ_DATA18 | 0x40610448 | FULL | Memory buffer |
| SCB1_EZ_DATA19 | 0x4061044C | FULL | Memory buffer |
| SCB1_EZ_DATA20 | 0x40610450 | FULL | Memory buffer |
| SCB1_EZ_DATA21 | 0x40610454 | FULL | Memory buffer |
| SCB1_EZ_DATA22 | 0x40610458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB1_EZ_DATA23 | 0x4061045C | FULL | Memory buffer |
| SCB1_EZ_DATA24 | 0x40610460 | FULL | Memory buffer |
| SCB1_EZ_DATA25 | 0x40610464 | FULL | Memory buffer |
| SCB1_EZ_DATA26 | 0x40610468 | FULL | Memory buffer |
| SCB1_EZ_DATA27 | 0x4061046C | FULL | Memory buffer |
| SCB1_EZ_DATA28 | 0x40610470 | FULL | Memory buffer |
| SCB1_EZ_DATA29 | 0x40610474 | FULL | Memory buffer |
| SCB1_EZ_DATA30 | 0x40610478 | FULL | Memory buffer |
| SCB1_EZ_DATA31 | 0x4061047C | FULL | Memory buffer |
| SCB1_EZ_DATA32 | 0x40610480 | FULL | Memory buffer |
| SCB1_EZ_DATA33 | 0x40610484 | FULL | Memory buffer |
| SCB1_EZ_DATA34 | 0x40610488 | FULL | Memory buffer |
| SCB1_EZ_DATA35 | 0x4061048C | FULL | Memory buffer |
| SCB1_EZ_DATA36 | 0x40610490 | FULL | Memory buffer |
| SCB1_EZ_DATA37 | 0x40610494 | FULL | Memory buffer |
| SCB1_EZ_DATA38 | 0x40610498 | FULL | Memory buffer |
| SCB1_EZ_DATA39 | 0x4061049C | FULL | Memory buffer |
| SCB1_EZ_DATA40 | 0x406104A0 | FULL | Memory buffer |
| SCB1_EZ_DATA41 | 0x406104A4 | FULL | Memory buffer |
| SCB1_EZ_DATA42 | 0x406104A8 | FULL | Memory buffer |
| SCB1_EZ_DATA43 | 0x406104AC | FULL | Memory buffer |
| SCB1_EZ_DATA44 | 0x406104B0 | FULL | Memory buffer |
| SCB1_EZ_DATA45 | 0x406104B4 | FULL | Memory buffer |
| SCB1_EZ_DATA46 | 0x406104B8 | FULL | Memory buffer |
| SCB1_EZ_DATA47 | 0x406104BC | FULL | Memory buffer |
| SCB1_EZ_DATA48 | 0x406104C0 | FULL | Memory buffer |
| SCB1_EZ_DATA49 | 0x406104C4 | FULL | Memory buffer |
| SCB1_EZ_DATA50 | 0x406104C8 | FULL | Memory buffer |
| SCB1_EZ_DATA51 | 0x406104CC | FULL | Memory buffer |
| SCB1_EZ_DATA52 | 0x406104D0 | FULL | Memory buffer |
| SCB1_EZ_DATA53 | 0x406104D4 | FULL | Memory buffer |
| SCB1_EZ_DATA54 | 0x406104D8 | FULL | Memory buffer |
| SCB1_EZ_DATA55 | 0x406104DC | FULL | Memory buffer |
| SCB1_EZ_DATA56 | 0x406104E0 | FULL | Memory buffer |
| SCB1_EZ_DATA57 | 0x406104E4 | FULL | Memory buffer |
| SCB1_EZ_DATA58 | 0x406104E8 | FULL | Memory buffer |
| SCB1_EZ_DATA59 | 0x406104EC | FULL | Memory buffer |
| SCB1_EZ_DATA60 | 0x406104F0 | FULL | Memory buffer |
| SCB1_EZ_DATA61 | 0x406104F4 | FULL | Memory buffer |
| SCB1_EZ_DATA62 | 0x406104F8 | FULL | Memory buffer |
| SCB1_EZ_DATA63 | 0x406104FC | FULL | Memory buffer |
| SCB1_EZ_DATA64 | 0x40610500 | FULL | Memory buffer |
| SCB1_EZ_DATA65 | 0x40610504 | FULL | Memory buffer |
| SCB1_EZ_DATA66 | 0x40610508 | FULL | Memory buffer |
| SCB1_EZ_DATA67 | 0x4061050C | FULL | Memory buffer |
| SCB1_EZ_DATA68 | 0x40610510 | FULL | Memory buffer |
| SCB1_EZ_DATA69 | 0x40610514 | FULL | Memory buffer |
| SCB1_EZ_DATA70 | 0x40610518 | FULL | Memory buffer |
| SCB1_EZ_DATA71 | 0x4061051C | FULL | Memory buffer |
| SCB1_EZ_DATA72 | 0x40610520 | FULL | Memory buffer |
| SCB1_EZ_DATA73 | 0x40610524 | FULL | Memory buffer |
| SCB1_EZ_DATA74 | 0x40610528 | FULL | Memory buffer |
| SCB1_EZ_DATA75 | 0x4061052C | FULL | Memory buffer |
| SCB1_EZ_DATA76 | 0x40610530 | FULL | Memory buffer |
| SCB1_EZ_DATA77 | 0x40610534 | FULL | Memory buffer |
| SCB1_EZ_DATA78 | 0x40610538 | FULL | Memory buffer |
| SCB1_EZ_DATA79 | 0x4061053C | FULL | Memory buffer |
| SCB1_EZ_DATA80 | 0x40610540 | FULL | Memory buffer |
| SCB1_EZ_DATA81 | 0x40610544 | FULL | Memory buffer |
| SCB1_EZ_DATA82 | 0x40610548 | FULL | Memory buffer |
| SCB1_EZ_DATA83 | 0x4061054C | FULL | Memory buffer |
| SCB1_EZ_DATA84 | 0x40610550 | FULL | Memory buffer |
| SCB1_EZ_DATA85 | 0x40610554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB1_EZ_DATA86 | 0x40610558 | FULL | Memory buffer |
| SCB1_EZ_DATA87 | 0x4061055C | FULL | Memory buffer |
| SCB1_EZ_DATA88 | 0x40610560 | FULL | Memory buffer |
| SCB1_EZ_DATA89 | 0x40610564 | FULL | Memory buffer |
| SCB1_EZ_DATA90 | 0x40610568 | FULL | Memory buffer |
| SCB1_EZ_DATA91 | 0x4061056C | FULL | Memory buffer |
| SCB1_EZ_DATA92 | 0x40610570 | FULL | Memory buffer |
| SCB1_EZ_DATA93 | 0x40610574 | FULL | Memory buffer |
| SCB1_EZ_DATA94 | 0x40610578 | FULL | Memory buffer |
| SCB1_EZ_DATA95 | 0x4061057C | FULL | Memory buffer |
| SCB1_EZ_DATA96 | 0x40610580 | FULL | Memory buffer |
| SCB1_EZ_DATA97 | 0x40610584 | FULL | Memory buffer |
| SCB1_EZ_DATA98 | 0x40610588 | FULL | Memory buffer |
| SCB1_EZ_DATA99 | 0x4061058C | FULL | Memory buffer |
| SCB1_EZ_DATA100 | 0x40610590 | FULL | Memory buffer |
| SCB1_EZ_DATA101 | 0x40610594 | FULL | Memory buffer |
| SCB1_EZ_DATA102 | 0x40610598 | FULL | Memory buffer |
| SCB1_EZ_DATA103 | 0x4061059C | FULL | Memory buffer |
| SCB1_EZ_DATA104 | 0x406105A0 | FULL | Memory buffer |
| SCB1_EZ_DATA105 | 0x406105A4 | FULL | Memory buffer |
| SCB1_EZ_DATA106 | 0x406105A8 | FULL | Memory buffer |
| SCB1_EZ_DATA107 | 0x406105AC | FULL | Memory buffer |
| SCB1_EZ_DATA108 | 0x406105B0 | FULL | Memory buffer |
| SCB1_EZ_DATA109 | 0x406105B4 | FULL | Memory buffer |
| SCB1_EZ_DATA110 | 0x406105B8 | FULL | Memory buffer |
| SCB1_EZ_DATA111 | 0x406105BC | FULL | Memory buffer |
| SCB1_EZ_DATA112 | 0x406105C0 | FULL | Memory buffer |
| SCB1_EZ_DATA113 | 0x406105C4 | FULL | Memory buffer |
| SCB1_EZ_DATA114 | 0x406105C8 | FULL | Memory buffer |
| SCB1_EZ_DATA115 | 0x406105CC | FULL | Memory buffer |
| SCB1_EZ_DATA116 | 0x406105D0 | FULL | Memory buffer |
| SCB1_EZ_DATA117 | 0x406105D4 | FULL | Memory buffer |
| SCB1_EZ_DATA118 | 0x406105D8 | FULL | Memory buffer |
| SCB1_EZ_DATA119 | 0x406105DC | FULL | Memory buffer |
| SCB1_EZ_DATA120 | 0x406105E0 | FULL | Memory buffer |
| SCB1_EZ_DATA121 | 0x406105E4 | FULL | Memory buffer |
| SCB1_EZ_DATA122 | 0x406105E8 | FULL | Memory buffer |
| SCB1_EZ_DATA123 | 0x406105EC | FULL | Memory buffer |
| SCB1_EZ_DATA124 | 0x406105F0 | FULL | Memory buffer |
| SCB1_EZ_DATA125 | 0x406105F4 | FULL | Memory buffer |
| SCB1_EZ_DATA126 | 0x406105F8 | FULL | Memory buffer |
| SCB1_EZ_DATA127 | 0x406105FC | FULL | Memory buffer |
| SCB1_EZ_DATA128 | 0x40610600 | FULL | Memory buffer |
| SCB1_EZ_DATA129 | 0x40610604 | FULL | Memory buffer |
| SCB1_EZ_DATA130 | 0x40610608 | FULL | Memory buffer |
| SCB1_EZ_DATA131 | 0x4061060C | FULL | Memory buffer |
| SCB1_EZ_DATA132 | 0x40610610 | FULL | Memory buffer |
| SCB1_EZ_DATA133 | 0x40610614 | FULL | Memory buffer |
| SCB1_EZ_DATA134 | 0x40610618 | FULL | Memory buffer |
| SCB1_EZ_DATA135 | 0x4061061C | FULL | Memory buffer |
| SCB1_EZ_DATA136 | 0x40610620 | FULL | Memory buffer |
| SCB1_EZ_DATA137 | 0x40610624 | FULL | Memory buffer |
| SCB1_EZ_DATA138 | 0x40610628 | FULL | Memory buffer |
| SCB1_EZ_DATA139 | 0x4061062C | FULL | Memory buffer |
| SCB1_EZ_DATA140 | 0x40610630 | FULL | Memory buffer |
| SCB1_EZ_DATA141 | 0x40610634 | FULL | Memory buffer |
| SCB1_EZ_DATA142 | 0x40610638 | FULL | Memory buffer |
| SCB1_EZ_DATA143 | 0x4061063C | FULL | Memory buffer |
| SCB1_EZ_DATA144 | 0x40610640 | FULL | Memory buffer |
| SCB1_EZ_DATA145 | 0x40610644 | FULL | Memory buffer |
| SCB1_EZ_DATA146 | 0x40610648 | FULL | Memory buffer |
| SCB1_EZ_DATA147 | 0x4061064C | FULL | Memory buffer |
| SCB1_EZ_DATA148 | 0x40610650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB1_EZ_DATA149 | 0x40610654 | FULL | Memory buffer |
| SCB1_EZ_DATA150 | 0x40610658 | FULL | Memory buffer |
| SCB1_EZ_DATA151 | 0x4061065C | FULL | Memory buffer |
| SCB1_EZ_DATA152 | 0x40610660 | FULL | Memory buffer |
| SCB1_EZ_DATA153 | 0x40610664 | FULL | Memory buffer |
| SCB1_EZ_DATA154 | 0x40610668 | FULL | Memory buffer |
| SCB1_EZ_DATA155 | 0x4061066C | FULL | Memory buffer |
| SCB1_EZ_DATA156 | 0x40610670 | FULL | Memory buffer |
| SCB1_EZ_DATA157 | 0x40610674 | FULL | Memory buffer |
| SCB1_EZ_DATA158 | 0x40610678 | FULL | Memory buffer |
| SCB1_EZ_DATA159 | 0x4061067C | FULL | Memory buffer |
| SCB1_EZ_DATA160 | 0x40610680 | FULL | Memory buffer |
| SCB1_EZ_DATA161 | 0x40610684 | FULL | Memory buffer |
| SCB1_EZ_DATA162 | 0x40610688 | FULL | Memory buffer |
| SCB1_EZ_DATA163 | 0x4061068C | FULL | Memory buffer |
| SCB1_EZ_DATA164 | 0x40610690 | FULL | Memory buffer |
| SCB1_EZ_DATA165 | 0x40610694 | FULL | Memory buffer |
| SCB1_EZ_DATA166 | 0x40610698 | FULL | Memory buffer |
| SCB1_EZ_DATA167 | 0x4061069C | FULL | Memory buffer |
| SCB1_EZ_DATA168 | 0x406106A0 | FULL | Memory buffer |
| SCB1_EZ_DATA169 | 0x406106A4 | FULL | Memory buffer |
| SCB1_EZ_DATA170 | 0x406106A8 | FULL | Memory buffer |
| SCB1_EZ_DATA171 | 0x406106AC | FULL | Memory buffer |
| SCB1_EZ_DATA172 | 0x406106B0 | FULL | Memory buffer |
| SCB1_EZ_DATA173 | 0x406106B4 | FULL | Memory buffer |
| SCB1_EZ_DATA174 | 0x406106B8 | FULL | Memory buffer |
| SCB1_EZ_DATA175 | 0x406106BC | FULL | Memory buffer |
| SCB1_EZ_DATA176 | 0x406106C0 | FULL | Memory buffer |
| SCB1_EZ_DATA177 | 0x406106C4 | FULL | Memory buffer |
| SCB1_EZ_DATA178 | 0x406106C8 | FULL | Memory buffer |
| SCB1_EZ_DATA179 | 0x406106CC | FULL | Memory buffer |
| SCB1_EZ_DATA180 | 0x406106D0 | FULL | Memory buffer |
| SCB1_EZ_DATA181 | 0x406106D4 | FULL | Memory buffer |
| SCB1_EZ_DATA182 | 0x406106D8 | FULL | Memory buffer |
| SCB1_EZ_DATA183 | 0x406106DC | FULL | Memory buffer |
| SCB1_EZ_DATA184 | 0x406106E0 | FULL | Memory buffer |
| SCB1_EZ_DATA185 | 0x406106E4 | FULL | Memory buffer |
| SCB1_EZ_DATA186 | 0x406106E8 | FULL | Memory buffer |
| SCB1_EZ_DATA187 | 0x406106EC | FULL | Memory buffer |
| SCB1_EZ_DATA188 | 0x406106F0 | FULL | Memory buffer |
| SCB1_EZ_DATA189 | 0x406106F4 | FULL | Memory buffer |
| SCB1_EZ_DATA190 | 0x406106F8 | FULL | Memory buffer |
| SCB1_EZ_DATA191 | 0x406106FC | FULL | Memory buffer |
| SCB1_EZ_DATA192 | 0x40610700 | FULL | Memory buffer |
| SCB1_EZ_DATA193 | 0x40610704 | FULL | Memory buffer |
| SCB1_EZ_DATA194 | 0x40610708 | FULL | Memory buffer |
| SCB1_EZ_DATA195 | 0x4061070C | FULL | Memory buffer |
| SCB1_EZ_DATA196 | 0x40610710 | FULL | Memory buffer |
| SCB1_EZ_DATA197 | 0x40610714 | FULL | Memory buffer |
| SCB1_EZ_DATA198 | 0x40610718 | FULL | Memory buffer |
| SCB1_EZ_DATA199 | 0x4061071C | FULL | Memory buffer |
| SCB1_EZ_DATA200 | 0x40610720 | FULL | Memory buffer |
| SCB1_EZ_DATA201 | 0x40610724 | FULL | Memory buffer |
| SCB1_EZ_DATA202 | 0x40610728 | FULL | Memory buffer |
| SCB1_EZ_DATA203 | 0x4061072C | FULL | Memory buffer |
| SCB1_EZ_DATA204 | 0x40610730 | FULL | Memory buffer |
| SCB1_EZ_DATA205 | 0x40610734 | FULL | Memory buffer |
| SCB1_EZ_DATA206 | 0x40610738 | FULL | Memory buffer |
| SCB1_EZ_DATA207 | 0x4061073C | FULL | Memory buffer |
| SCB1_EZ_DATA208 | 0x40610740 | FULL | Memory buffer |
| SCB1_EZ_DATA209 | 0x40610744 | FULL | Memory buffer |
| SCB1_EZ_DATA210 | 0x40610748 | FULL | Memory buffer |
| SCB1_EZ_DATA211 | 0x4061074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB1_EZ_DATA212 | 0x40610750 | FULL | Memory buffer |
| SCB1_EZ_DATA213 | 0x40610754 | FULL | Memory buffer |
| SCB1_EZ_DATA214 | 0x40610758 | FULL | Memory buffer |
| SCB1_EZ_DATA215 | 0x4061075C | FULL | Memory buffer |
| SCB1_EZ_DATA216 | 0x40610760 | FULL | Memory buffer |
| SCB1_EZ_DATA217 | 0x40610764 | FULL | Memory buffer |
| SCB1_EZ_DATA218 | 0x40610768 | FULL | Memory buffer |
| SCB1_EZ_DATA219 | 0x4061076C | FULL | Memory buffer |
| SCB1_EZ_DATA220 | 0x40610770 | FULL | Memory buffer |
| SCB1_EZ_DATA221 | 0x40610774 | FULL | Memory buffer |
| SCB1_EZ_DATA222 | 0x40610778 | FULL | Memory buffer |
| SCB1_EZ_DATA223 | 0x4061077C | FULL | Memory buffer |
| SCB1_EZ_DATA224 | 0x40610780 | FULL | Memory buffer |
| SCB1_EZ_DATA225 | 0x40610784 | FULL | Memory buffer |
| SCB1_EZ_DATA226 | 0x40610788 | FULL | Memory buffer |
| SCB1_EZ_DATA227 | 0x4061078C | FULL | Memory buffer |
| SCB1_EZ_DATA228 | 0x40610790 | FULL | Memory buffer |
| SCB1_EZ_DATA229 | 0x40610794 | FULL | Memory buffer |
| SCB1_EZ_DATA230 | 0x40610798 | FULL | Memory buffer |
| SCB1_EZ_DATA231 | 0x4061079C | FULL | Memory buffer |
| SCB1_EZ_DATA232 | 0x406107A0 | FULL | Memory buffer |
| SCB1_EZ_DATA233 | 0x406107A4 | FULL | Memory buffer |
| SCB1_EZ_DATA234 | 0x406107A8 | FULL | Memory buffer |
| SCB1_EZ_DATA235 | 0x406107AC | FULL | Memory buffer |
| SCB1_EZ_DATA236 | 0x406107B0 | FULL | Memory buffer |
| SCB1_EZ_DATA237 | 0x406107B4 | FULL | Memory buffer |
| SCB1_EZ_DATA238 | 0x406107B8 | FULL | Memory buffer |
| SCB1_EZ_DATA239 | 0x406107BC | FULL | Memory buffer |
| SCB1_EZ_DATA240 | 0x406107C0 | FULL | Memory buffer |
| SCB1_EZ_DATA241 | 0x406107C4 | FULL | Memory buffer |
| SCB1_EZ_DATA242 | 0x406107C8 | FULL | Memory buffer |
| SCB1_EZ_DATA243 | 0x406107CC | FULL | Memory buffer |
| SCB1_EZ_DATA244 | 0x406107D0 | FULL | Memory buffer |
| SCB1_EZ_DATA245 | 0x406107D4 | FULL | Memory buffer |
| SCB1_EZ_DATA246 | 0x406107D8 | FULL | Memory buffer |
| SCB1_EZ_DATA247 | 0x406107DC | FULL | Memory buffer |
| SCB1_EZ_DATA248 | 0x406107E0 | FULL | Memory buffer |
| SCB1_EZ_DATA249 | 0x406107E4 | FULL | Memory buffer |
| SCB1_EZ_DATA250 | 0x406107E8 | FULL | Memory buffer |
| SCB1_EZ_DATA251 | 0x406107EC | FULL | Memory buffer |
| SCB1_EZ_DATA252 | 0x406107F0 | FULL | Memory buffer |
| SCB1_EZ_DATA253 | 0x406107F4 | FULL | Memory buffer |
| SCB1_EZ_DATA254 | 0x406107F8 | FULL | Memory buffer |
| SCB1_EZ_DATA255 | 0x406107FC | FULL | Memory buffer |
| SCB1_INTR_CAUSE | 0x40610E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB1_INTR_SPI_EC | 0x40610EC0 | FULL | Externally clocked SPI interrupt request |
| SCB1_INTR_SPI_EC_MASK | 0x40610EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB1_INTR_SPI_EC_MASKED | 0x40610ECC | FULL | Externally clocked SPI interrupt masked |
| SCB1_INTR_M | 0x40610F00 | FULL | Master interrupt request |
| SCB1_INTR_M_SET | 0x40610F04 | FULL | Master interrupt set request |
| SCB1_INTR_M_MASK | 0x40610F08 | FULL | Master interrupt mask |
| SCB1_INTR_M_MASKED | 0x40610F0C | FULL | Master interrupt masked request |
| SCB1_INTR_S | 0x40610F40 | FULL | Slave interrupt request |
| SCB1_INTR_S_SET | 0x40610F44 | FULL | Slave interrupt set request |
| SCB1_INTR_S_MASK | 0x40610F48 | FULL | Slave interrupt mask |
| SCB1_INTR_S_MASKED | 0x40610F4C | FULL | Slave interrupt masked request |
| SCB1_INTR_TX | 0x40610F80 | FULL | Transmitter interrupt request |
| SCB1_INTR_TX_SET | 0x40610F84 | FULL | Transmitter interrupt set request |
| SCB1_INTR_TX_MASK | 0x40610F88 | FULL | Transmitter interrupt mask |
| SCB1_INTR_TX_MASKED | 0x40610F8C | FULL | Transmitter interrupt masked request |
| SCB1_INTR_RX | 0x40610FC0 | FULL | Receiver interrupt request |
| SCB1_INTR_RX_SET | 0x40610FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|-----------------------------------|
| SCB1_INTR_RX_MASK | 0x40610FC8 | FULL | Receiver interrupt mask |
| SCB1_INTR_RX_MASKED | 0x40610FCC | FULL | Receiver interrupt masked request |

23.3 SCB 2

Description Serial Communications Block
(SPI/UART/I2C)
Base Address 0x40620000
Size 0x10000
Slave Num MMIO6 - 2

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| SCB2_CTRL | 0x40620000 | FULL | Generic control Note: CMD_RESP_MODE is not available for this register |
| SCB2_STATUS | 0x40620004 | FULL | Generic status |
| SCB2_SPI_CTRL | 0x40620020 | FULL | SPI control |
| SCB2_SPI_STATUS | 0x40620024 | FULL | SPI status |
| SCB2_SPI_TX_CTRL | 0x40620028 | FULL | SPI transmitter control |
| SCB2_SPI_RX_CTRL | 0x4062002C | FULL | SPI receiver control |
| SCB2_UART_CTRL | 0x40620040 | FULL | UART control |
| SCB2_UART_TX_CTRL | 0x40620044 | FULL | UART transmitter control |
| SCB2_UART_RX_CTRL | 0x40620048 | FULL | UART receiver control |
| SCB2_UART_RX_STATUS | 0x4062004C | FULL | UART receiver status |
| SCB2_UART_FLOW_CTRL | 0x40620050 | FULL | UART flow control |
| SCB2_I2C_CTRL | 0x40620060 | FULL | I2C control |
| SCB2_I2C_STATUS | 0x40620064 | FULL | I2C status Note: I2C_EC_BUSY is not available for this register |
| SCB2_I2C_M_CMD | 0x40620068 | FULL | I2C master command |
| SCB2_I2C_S_CMD | 0x4062006C | FULL | I2C slave command |
| SCB2_I2C_CFG | 0x40620070 | FULL | I2C configuration |
| SCB2_TX_CTRL | 0x40620200 | FULL | Transmitter control |
| SCB2_TX_FIFO_CTRL | 0x40620204 | FULL | Transmitter FIFO control |
| SCB2_TX_FIFO_STATUS | 0x40620208 | FULL | Transmitter FIFO status |
| SCB2_TX_FIFO_WR | 0x40620240 | FULL | Transmitter FIFO write |
| SCB2_RX_CTRL | 0x40620300 | FULL | Receiver control |
| SCB2_RX_FIFO_CTRL | 0x40620304 | FULL | Receiver FIFO control |
| SCB2_RX_FIFO_STATUS | 0x40620308 | FULL | Receiver FIFO status |
| SCB2_RX_MATCH | 0x40620310 | FULL | Slave address and mask |
| SCB2_RX_FIFO_RD | 0x40620340 | FULL | Receiver FIFO read |
| SCB2_RX_FIFO_RD_SILENT | 0x40620344 | FULL | Receiver FIFO read silent |
| SCB2_EZ_DATA0 | 0x40620400 | FULL | Memory buffer |
| SCB2_EZ_DATA1 | 0x40620404 | FULL | Memory buffer |
| SCB2_EZ_DATA2 | 0x40620408 | FULL | Memory buffer |
| SCB2_EZ_DATA3 | 0x4062040C | FULL | Memory buffer |
| SCB2_EZ_DATA4 | 0x40620410 | FULL | Memory buffer |
| SCB2_EZ_DATA5 | 0x40620414 | FULL | Memory buffer |
| SCB2_EZ_DATA6 | 0x40620418 | FULL | Memory buffer |
| SCB2_EZ_DATA7 | 0x4062041C | FULL | Memory buffer |
| SCB2_EZ_DATA8 | 0x40620420 | FULL | Memory buffer |
| SCB2_EZ_DATA9 | 0x40620424 | FULL | Memory buffer |
| SCB2_EZ_DATA10 | 0x40620428 | FULL | Memory buffer |
| SCB2_EZ_DATA11 | 0x4062042C | FULL | Memory buffer |
| SCB2_EZ_DATA12 | 0x40620430 | FULL | Memory buffer |
| SCB2_EZ_DATA13 | 0x40620434 | FULL | Memory buffer |
| SCB2_EZ_DATA14 | 0x40620438 | FULL | Memory buffer |
| SCB2_EZ_DATA15 | 0x4062043C | FULL | Memory buffer |
| SCB2_EZ_DATA16 | 0x40620440 | FULL | Memory buffer |
| SCB2_EZ_DATA17 | 0x40620444 | FULL | Memory buffer |
| SCB2_EZ_DATA18 | 0x40620448 | FULL | Memory buffer |
| SCB2_EZ_DATA19 | 0x4062044C | FULL | Memory buffer |
| SCB2_EZ_DATA20 | 0x40620450 | FULL | Memory buffer |
| SCB2_EZ_DATA21 | 0x40620454 | FULL | Memory buffer |
| SCB2_EZ_DATA22 | 0x40620458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB2_EZ_DATA23 | 0x4062045C | FULL | Memory buffer |
| SCB2_EZ_DATA24 | 0x40620460 | FULL | Memory buffer |
| SCB2_EZ_DATA25 | 0x40620464 | FULL | Memory buffer |
| SCB2_EZ_DATA26 | 0x40620468 | FULL | Memory buffer |
| SCB2_EZ_DATA27 | 0x4062046C | FULL | Memory buffer |
| SCB2_EZ_DATA28 | 0x40620470 | FULL | Memory buffer |
| SCB2_EZ_DATA29 | 0x40620474 | FULL | Memory buffer |
| SCB2_EZ_DATA30 | 0x40620478 | FULL | Memory buffer |
| SCB2_EZ_DATA31 | 0x4062047C | FULL | Memory buffer |
| SCB2_EZ_DATA32 | 0x40620480 | FULL | Memory buffer |
| SCB2_EZ_DATA33 | 0x40620484 | FULL | Memory buffer |
| SCB2_EZ_DATA34 | 0x40620488 | FULL | Memory buffer |
| SCB2_EZ_DATA35 | 0x4062048C | FULL | Memory buffer |
| SCB2_EZ_DATA36 | 0x40620490 | FULL | Memory buffer |
| SCB2_EZ_DATA37 | 0x40620494 | FULL | Memory buffer |
| SCB2_EZ_DATA38 | 0x40620498 | FULL | Memory buffer |
| SCB2_EZ_DATA39 | 0x4062049C | FULL | Memory buffer |
| SCB2_EZ_DATA40 | 0x406204A0 | FULL | Memory buffer |
| SCB2_EZ_DATA41 | 0x406204A4 | FULL | Memory buffer |
| SCB2_EZ_DATA42 | 0x406204A8 | FULL | Memory buffer |
| SCB2_EZ_DATA43 | 0x406204AC | FULL | Memory buffer |
| SCB2_EZ_DATA44 | 0x406204B0 | FULL | Memory buffer |
| SCB2_EZ_DATA45 | 0x406204B4 | FULL | Memory buffer |
| SCB2_EZ_DATA46 | 0x406204B8 | FULL | Memory buffer |
| SCB2_EZ_DATA47 | 0x406204BC | FULL | Memory buffer |
| SCB2_EZ_DATA48 | 0x406204C0 | FULL | Memory buffer |
| SCB2_EZ_DATA49 | 0x406204C4 | FULL | Memory buffer |
| SCB2_EZ_DATA50 | 0x406204C8 | FULL | Memory buffer |
| SCB2_EZ_DATA51 | 0x406204CC | FULL | Memory buffer |
| SCB2_EZ_DATA52 | 0x406204D0 | FULL | Memory buffer |
| SCB2_EZ_DATA53 | 0x406204D4 | FULL | Memory buffer |
| SCB2_EZ_DATA54 | 0x406204D8 | FULL | Memory buffer |
| SCB2_EZ_DATA55 | 0x406204DC | FULL | Memory buffer |
| SCB2_EZ_DATA56 | 0x406204E0 | FULL | Memory buffer |
| SCB2_EZ_DATA57 | 0x406204E4 | FULL | Memory buffer |
| SCB2_EZ_DATA58 | 0x406204E8 | FULL | Memory buffer |
| SCB2_EZ_DATA59 | 0x406204EC | FULL | Memory buffer |
| SCB2_EZ_DATA60 | 0x406204F0 | FULL | Memory buffer |
| SCB2_EZ_DATA61 | 0x406204F4 | FULL | Memory buffer |
| SCB2_EZ_DATA62 | 0x406204F8 | FULL | Memory buffer |
| SCB2_EZ_DATA63 | 0x406204FC | FULL | Memory buffer |
| SCB2_EZ_DATA64 | 0x40620500 | FULL | Memory buffer |
| SCB2_EZ_DATA65 | 0x40620504 | FULL | Memory buffer |
| SCB2_EZ_DATA66 | 0x40620508 | FULL | Memory buffer |
| SCB2_EZ_DATA67 | 0x4062050C | FULL | Memory buffer |
| SCB2_EZ_DATA68 | 0x40620510 | FULL | Memory buffer |
| SCB2_EZ_DATA69 | 0x40620514 | FULL | Memory buffer |
| SCB2_EZ_DATA70 | 0x40620518 | FULL | Memory buffer |
| SCB2_EZ_DATA71 | 0x4062051C | FULL | Memory buffer |
| SCB2_EZ_DATA72 | 0x40620520 | FULL | Memory buffer |
| SCB2_EZ_DATA73 | 0x40620524 | FULL | Memory buffer |
| SCB2_EZ_DATA74 | 0x40620528 | FULL | Memory buffer |
| SCB2_EZ_DATA75 | 0x4062052C | FULL | Memory buffer |
| SCB2_EZ_DATA76 | 0x40620530 | FULL | Memory buffer |
| SCB2_EZ_DATA77 | 0x40620534 | FULL | Memory buffer |
| SCB2_EZ_DATA78 | 0x40620538 | FULL | Memory buffer |
| SCB2_EZ_DATA79 | 0x4062053C | FULL | Memory buffer |
| SCB2_EZ_DATA80 | 0x40620540 | FULL | Memory buffer |
| SCB2_EZ_DATA81 | 0x40620544 | FULL | Memory buffer |
| SCB2_EZ_DATA82 | 0x40620548 | FULL | Memory buffer |
| SCB2_EZ_DATA83 | 0x4062054C | FULL | Memory buffer |
| SCB2_EZ_DATA84 | 0x40620550 | FULL | Memory buffer |
| SCB2_EZ_DATA85 | 0x40620554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB2_EZ_DATA86 | 0x40620558 | FULL | Memory buffer |
| SCB2_EZ_DATA87 | 0x4062055C | FULL | Memory buffer |
| SCB2_EZ_DATA88 | 0x40620560 | FULL | Memory buffer |
| SCB2_EZ_DATA89 | 0x40620564 | FULL | Memory buffer |
| SCB2_EZ_DATA90 | 0x40620568 | FULL | Memory buffer |
| SCB2_EZ_DATA91 | 0x4062056C | FULL | Memory buffer |
| SCB2_EZ_DATA92 | 0x40620570 | FULL | Memory buffer |
| SCB2_EZ_DATA93 | 0x40620574 | FULL | Memory buffer |
| SCB2_EZ_DATA94 | 0x40620578 | FULL | Memory buffer |
| SCB2_EZ_DATA95 | 0x4062057C | FULL | Memory buffer |
| SCB2_EZ_DATA96 | 0x40620580 | FULL | Memory buffer |
| SCB2_EZ_DATA97 | 0x40620584 | FULL | Memory buffer |
| SCB2_EZ_DATA98 | 0x40620588 | FULL | Memory buffer |
| SCB2_EZ_DATA99 | 0x4062058C | FULL | Memory buffer |
| SCB2_EZ_DATA100 | 0x40620590 | FULL | Memory buffer |
| SCB2_EZ_DATA101 | 0x40620594 | FULL | Memory buffer |
| SCB2_EZ_DATA102 | 0x40620598 | FULL | Memory buffer |
| SCB2_EZ_DATA103 | 0x4062059C | FULL | Memory buffer |
| SCB2_EZ_DATA104 | 0x406205A0 | FULL | Memory buffer |
| SCB2_EZ_DATA105 | 0x406205A4 | FULL | Memory buffer |
| SCB2_EZ_DATA106 | 0x406205A8 | FULL | Memory buffer |
| SCB2_EZ_DATA107 | 0x406205AC | FULL | Memory buffer |
| SCB2_EZ_DATA108 | 0x406205B0 | FULL | Memory buffer |
| SCB2_EZ_DATA109 | 0x406205B4 | FULL | Memory buffer |
| SCB2_EZ_DATA110 | 0x406205B8 | FULL | Memory buffer |
| SCB2_EZ_DATA111 | 0x406205BC | FULL | Memory buffer |
| SCB2_EZ_DATA112 | 0x406205C0 | FULL | Memory buffer |
| SCB2_EZ_DATA113 | 0x406205C4 | FULL | Memory buffer |
| SCB2_EZ_DATA114 | 0x406205C8 | FULL | Memory buffer |
| SCB2_EZ_DATA115 | 0x406205CC | FULL | Memory buffer |
| SCB2_EZ_DATA116 | 0x406205D0 | FULL | Memory buffer |
| SCB2_EZ_DATA117 | 0x406205D4 | FULL | Memory buffer |
| SCB2_EZ_DATA118 | 0x406205D8 | FULL | Memory buffer |
| SCB2_EZ_DATA119 | 0x406205DC | FULL | Memory buffer |
| SCB2_EZ_DATA120 | 0x406205E0 | FULL | Memory buffer |
| SCB2_EZ_DATA121 | 0x406205E4 | FULL | Memory buffer |
| SCB2_EZ_DATA122 | 0x406205E8 | FULL | Memory buffer |
| SCB2_EZ_DATA123 | 0x406205EC | FULL | Memory buffer |
| SCB2_EZ_DATA124 | 0x406205F0 | FULL | Memory buffer |
| SCB2_EZ_DATA125 | 0x406205F4 | FULL | Memory buffer |
| SCB2_EZ_DATA126 | 0x406205F8 | FULL | Memory buffer |
| SCB2_EZ_DATA127 | 0x406205FC | FULL | Memory buffer |
| SCB2_EZ_DATA128 | 0x40620600 | FULL | Memory buffer |
| SCB2_EZ_DATA129 | 0x40620604 | FULL | Memory buffer |
| SCB2_EZ_DATA130 | 0x40620608 | FULL | Memory buffer |
| SCB2_EZ_DATA131 | 0x4062060C | FULL | Memory buffer |
| SCB2_EZ_DATA132 | 0x40620610 | FULL | Memory buffer |
| SCB2_EZ_DATA133 | 0x40620614 | FULL | Memory buffer |
| SCB2_EZ_DATA134 | 0x40620618 | FULL | Memory buffer |
| SCB2_EZ_DATA135 | 0x4062061C | FULL | Memory buffer |
| SCB2_EZ_DATA136 | 0x40620620 | FULL | Memory buffer |
| SCB2_EZ_DATA137 | 0x40620624 | FULL | Memory buffer |
| SCB2_EZ_DATA138 | 0x40620628 | FULL | Memory buffer |
| SCB2_EZ_DATA139 | 0x4062062C | FULL | Memory buffer |
| SCB2_EZ_DATA140 | 0x40620630 | FULL | Memory buffer |
| SCB2_EZ_DATA141 | 0x40620634 | FULL | Memory buffer |
| SCB2_EZ_DATA142 | 0x40620638 | FULL | Memory buffer |
| SCB2_EZ_DATA143 | 0x4062063C | FULL | Memory buffer |
| SCB2_EZ_DATA144 | 0x40620640 | FULL | Memory buffer |
| SCB2_EZ_DATA145 | 0x40620644 | FULL | Memory buffer |
| SCB2_EZ_DATA146 | 0x40620648 | FULL | Memory buffer |
| SCB2_EZ_DATA147 | 0x4062064C | FULL | Memory buffer |
| SCB2_EZ_DATA148 | 0x40620650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB2_EZ_DATA149 | 0x40620654 | FULL | Memory buffer |
| SCB2_EZ_DATA150 | 0x40620658 | FULL | Memory buffer |
| SCB2_EZ_DATA151 | 0x4062065C | FULL | Memory buffer |
| SCB2_EZ_DATA152 | 0x40620660 | FULL | Memory buffer |
| SCB2_EZ_DATA153 | 0x40620664 | FULL | Memory buffer |
| SCB2_EZ_DATA154 | 0x40620668 | FULL | Memory buffer |
| SCB2_EZ_DATA155 | 0x4062066C | FULL | Memory buffer |
| SCB2_EZ_DATA156 | 0x40620670 | FULL | Memory buffer |
| SCB2_EZ_DATA157 | 0x40620674 | FULL | Memory buffer |
| SCB2_EZ_DATA158 | 0x40620678 | FULL | Memory buffer |
| SCB2_EZ_DATA159 | 0x4062067C | FULL | Memory buffer |
| SCB2_EZ_DATA160 | 0x40620680 | FULL | Memory buffer |
| SCB2_EZ_DATA161 | 0x40620684 | FULL | Memory buffer |
| SCB2_EZ_DATA162 | 0x40620688 | FULL | Memory buffer |
| SCB2_EZ_DATA163 | 0x4062068C | FULL | Memory buffer |
| SCB2_EZ_DATA164 | 0x40620690 | FULL | Memory buffer |
| SCB2_EZ_DATA165 | 0x40620694 | FULL | Memory buffer |
| SCB2_EZ_DATA166 | 0x40620698 | FULL | Memory buffer |
| SCB2_EZ_DATA167 | 0x4062069C | FULL | Memory buffer |
| SCB2_EZ_DATA168 | 0x406206A0 | FULL | Memory buffer |
| SCB2_EZ_DATA169 | 0x406206A4 | FULL | Memory buffer |
| SCB2_EZ_DATA170 | 0x406206A8 | FULL | Memory buffer |
| SCB2_EZ_DATA171 | 0x406206AC | FULL | Memory buffer |
| SCB2_EZ_DATA172 | 0x406206B0 | FULL | Memory buffer |
| SCB2_EZ_DATA173 | 0x406206B4 | FULL | Memory buffer |
| SCB2_EZ_DATA174 | 0x406206B8 | FULL | Memory buffer |
| SCB2_EZ_DATA175 | 0x406206BC | FULL | Memory buffer |
| SCB2_EZ_DATA176 | 0x406206C0 | FULL | Memory buffer |
| SCB2_EZ_DATA177 | 0x406206C4 | FULL | Memory buffer |
| SCB2_EZ_DATA178 | 0x406206C8 | FULL | Memory buffer |
| SCB2_EZ_DATA179 | 0x406206CC | FULL | Memory buffer |
| SCB2_EZ_DATA180 | 0x406206D0 | FULL | Memory buffer |
| SCB2_EZ_DATA181 | 0x406206D4 | FULL | Memory buffer |
| SCB2_EZ_DATA182 | 0x406206D8 | FULL | Memory buffer |
| SCB2_EZ_DATA183 | 0x406206DC | FULL | Memory buffer |
| SCB2_EZ_DATA184 | 0x406206E0 | FULL | Memory buffer |
| SCB2_EZ_DATA185 | 0x406206E4 | FULL | Memory buffer |
| SCB2_EZ_DATA186 | 0x406206E8 | FULL | Memory buffer |
| SCB2_EZ_DATA187 | 0x406206EC | FULL | Memory buffer |
| SCB2_EZ_DATA188 | 0x406206F0 | FULL | Memory buffer |
| SCB2_EZ_DATA189 | 0x406206F4 | FULL | Memory buffer |
| SCB2_EZ_DATA190 | 0x406206F8 | FULL | Memory buffer |
| SCB2_EZ_DATA191 | 0x406206FC | FULL | Memory buffer |
| SCB2_EZ_DATA192 | 0x40620700 | FULL | Memory buffer |
| SCB2_EZ_DATA193 | 0x40620704 | FULL | Memory buffer |
| SCB2_EZ_DATA194 | 0x40620708 | FULL | Memory buffer |
| SCB2_EZ_DATA195 | 0x4062070C | FULL | Memory buffer |
| SCB2_EZ_DATA196 | 0x40620710 | FULL | Memory buffer |
| SCB2_EZ_DATA197 | 0x40620714 | FULL | Memory buffer |
| SCB2_EZ_DATA198 | 0x40620718 | FULL | Memory buffer |
| SCB2_EZ_DATA199 | 0x4062071C | FULL | Memory buffer |
| SCB2_EZ_DATA200 | 0x40620720 | FULL | Memory buffer |
| SCB2_EZ_DATA201 | 0x40620724 | FULL | Memory buffer |
| SCB2_EZ_DATA202 | 0x40620728 | FULL | Memory buffer |
| SCB2_EZ_DATA203 | 0x4062072C | FULL | Memory buffer |
| SCB2_EZ_DATA204 | 0x40620730 | FULL | Memory buffer |
| SCB2_EZ_DATA205 | 0x40620734 | FULL | Memory buffer |
| SCB2_EZ_DATA206 | 0x40620738 | FULL | Memory buffer |
| SCB2_EZ_DATA207 | 0x4062073C | FULL | Memory buffer |
| SCB2_EZ_DATA208 | 0x40620740 | FULL | Memory buffer |
| SCB2_EZ_DATA209 | 0x40620744 | FULL | Memory buffer |
| SCB2_EZ_DATA210 | 0x40620748 | FULL | Memory buffer |
| SCB2_EZ_DATA211 | 0x4062074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB2_EZ_DATA212 | 0x40620750 | FULL | Memory buffer |
| SCB2_EZ_DATA213 | 0x40620754 | FULL | Memory buffer |
| SCB2_EZ_DATA214 | 0x40620758 | FULL | Memory buffer |
| SCB2_EZ_DATA215 | 0x4062075C | FULL | Memory buffer |
| SCB2_EZ_DATA216 | 0x40620760 | FULL | Memory buffer |
| SCB2_EZ_DATA217 | 0x40620764 | FULL | Memory buffer |
| SCB2_EZ_DATA218 | 0x40620768 | FULL | Memory buffer |
| SCB2_EZ_DATA219 | 0x4062076C | FULL | Memory buffer |
| SCB2_EZ_DATA220 | 0x40620770 | FULL | Memory buffer |
| SCB2_EZ_DATA221 | 0x40620774 | FULL | Memory buffer |
| SCB2_EZ_DATA222 | 0x40620778 | FULL | Memory buffer |
| SCB2_EZ_DATA223 | 0x4062077C | FULL | Memory buffer |
| SCB2_EZ_DATA224 | 0x40620780 | FULL | Memory buffer |
| SCB2_EZ_DATA225 | 0x40620784 | FULL | Memory buffer |
| SCB2_EZ_DATA226 | 0x40620788 | FULL | Memory buffer |
| SCB2_EZ_DATA227 | 0x4062078C | FULL | Memory buffer |
| SCB2_EZ_DATA228 | 0x40620790 | FULL | Memory buffer |
| SCB2_EZ_DATA229 | 0x40620794 | FULL | Memory buffer |
| SCB2_EZ_DATA230 | 0x40620798 | FULL | Memory buffer |
| SCB2_EZ_DATA231 | 0x4062079C | FULL | Memory buffer |
| SCB2_EZ_DATA232 | 0x406207A0 | FULL | Memory buffer |
| SCB2_EZ_DATA233 | 0x406207A4 | FULL | Memory buffer |
| SCB2_EZ_DATA234 | 0x406207A8 | FULL | Memory buffer |
| SCB2_EZ_DATA235 | 0x406207AC | FULL | Memory buffer |
| SCB2_EZ_DATA236 | 0x406207B0 | FULL | Memory buffer |
| SCB2_EZ_DATA237 | 0x406207B4 | FULL | Memory buffer |
| SCB2_EZ_DATA238 | 0x406207B8 | FULL | Memory buffer |
| SCB2_EZ_DATA239 | 0x406207BC | FULL | Memory buffer |
| SCB2_EZ_DATA240 | 0x406207C0 | FULL | Memory buffer |
| SCB2_EZ_DATA241 | 0x406207C4 | FULL | Memory buffer |
| SCB2_EZ_DATA242 | 0x406207C8 | FULL | Memory buffer |
| SCB2_EZ_DATA243 | 0x406207CC | FULL | Memory buffer |
| SCB2_EZ_DATA244 | 0x406207D0 | FULL | Memory buffer |
| SCB2_EZ_DATA245 | 0x406207D4 | FULL | Memory buffer |
| SCB2_EZ_DATA246 | 0x406207D8 | FULL | Memory buffer |
| SCB2_EZ_DATA247 | 0x406207DC | FULL | Memory buffer |
| SCB2_EZ_DATA248 | 0x406207E0 | FULL | Memory buffer |
| SCB2_EZ_DATA249 | 0x406207E4 | FULL | Memory buffer |
| SCB2_EZ_DATA250 | 0x406207E8 | FULL | Memory buffer |
| SCB2_EZ_DATA251 | 0x406207EC | FULL | Memory buffer |
| SCB2_EZ_DATA252 | 0x406207F0 | FULL | Memory buffer |
| SCB2_EZ_DATA253 | 0x406207F4 | FULL | Memory buffer |
| SCB2_EZ_DATA254 | 0x406207F8 | FULL | Memory buffer |
| SCB2_EZ_DATA255 | 0x406207FC | FULL | Memory buffer |
| SCB2_INTR_CAUSE | 0x40620E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB2_INTR_SPI_EC | 0x40620EC0 | FULL | Externally clocked SPI interrupt request |
| SCB2_INTR_SPI_EC_MASK | 0x40620EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB2_INTR_SPI_EC_MASKED | 0x40620ECC | FULL | Externally clocked SPI interrupt masked |
| SCB2_INTR_M | 0x40620F00 | FULL | Master interrupt request |
| SCB2_INTR_M_SET | 0x40620F04 | FULL | Master interrupt set request |
| SCB2_INTR_M_MASK | 0x40620F08 | FULL | Master interrupt mask |
| SCB2_INTR_M_MASKED | 0x40620F0C | FULL | Master interrupt masked request |
| SCB2_INTR_S | 0x40620F40 | FULL | Slave interrupt request |
| SCB2_INTR_S_SET | 0x40620F44 | FULL | Slave interrupt set request |
| SCB2_INTR_S_MASK | 0x40620F48 | FULL | Slave interrupt mask |
| SCB2_INTR_S_MASKED | 0x40620F4C | FULL | Slave interrupt masked request |
| SCB2_INTR_TX | 0x40620F80 | FULL | Transmitter interrupt request |
| SCB2_INTR_TX_SET | 0x40620F84 | FULL | Transmitter interrupt set request |
| SCB2_INTR_TX_MASK | 0x40620F88 | FULL | Transmitter interrupt mask |
| SCB2_INTR_TX_MASKED | 0x40620F8C | FULL | Transmitter interrupt masked request |
| SCB2_INTR_RX | 0x40620FC0 | FULL | Receiver interrupt request |
| SCB2_INTR_RX_SET | 0x40620FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|-----------------------------------|
| SCB2_INTR_RX_MASK | 0x40620FC8 | FULL | Receiver interrupt mask |
| SCB2_INTR_RX_MASKED | 0x40620FCC | FULL | Receiver interrupt masked request |

23.4 SCB 3

Description Serial Communications Block
(SPI/UART/I2C)
Base Address 0x40630000
Size 0x10000
Slave Num MMIO6 - 3

| Register Name | Address | Permission | Description |
|--|------------|------------|--|
| SCB3_CTRL | 0x40630000 | FULL | Generic control Note: CMD_RESP_MODE is not available for this register |
| SCB3_STATUS | 0x40630004 | FULL | Generic status |
| SCB3_SPI_CTRL | 0x40630020 | FULL | SPI control |
| SCB3_SPI_STATUS | 0x40630024 | FULL | SPI status |
| SCB3_SPI_TX_CTRL | 0x40630028 | FULL | SPI transmitter control |
| SCB3_SPI_RX_CTRL | 0x4063002C | FULL | SPI receiver control |
| SCB3_UART_CTRL | 0x40630040 | FULL | UART control |
| SCB3_UART_TX_CTRL | 0x40630044 | FULL | UART transmitter control |
| SCB3_UART_RX_CTRL | 0x40630048 | FULL | UART receiver control |
| SCB3_UART_RX_STATUS | 0x4063004C | FULL | UART receiver status |
| SCB3_UART_FLOW_CTRL | 0x40630050 | FULL | UART flow control |
| SCB3_I2C_CTRL | 0x40630060 | FULL | I2C control |
| SCB3_I2C_STATUS | 0x40630064 | FULL | I2C status Note: I2C_EC_BUSY is not available for this register |
| SCB3_I2C_M_CMD | 0x40630068 | FULL | I2C master command |
| SCB3_I2C_S_CMD | 0x4063006C | FULL | I2C slave command |
| SCB3_I2C_CFG | 0x40630070 | FULL | I2C configuration |
| SCB3_TX_CTRL | 0x40630200 | FULL | Transmitter control |
| SCB3_TX_FIFO_CTRL | 0x40630204 | FULL | Transmitter FIFO control |
| SCB3_TX_FIFO_STATUS | 0x40630208 | FULL | Transmitter FIFO status |
| SCB3_TX_FIFO_WR | 0x40630240 | FULL | Transmitter FIFO write |
| SCB3_RX_CTRL | 0x40630300 | FULL | Receiver control |
| SCB3_RX_FIFO_CTRL | 0x40630304 | FULL | Receiver FIFO control |
| SCB3_RX_FIFO_STATUS | 0x40630308 | FULL | Receiver FIFO status |
| SCB3_RX_MATCH | 0x40630310 | FULL | Slave address and mask |
| SCB3_RX_FIFO_RD | 0x40630340 | FULL | Receiver FIFO read |
| SCB3_RX_FIFO_RD_SILENT | 0x40630344 | FULL | Receiver FIFO read silent |
| SCB3_EZ_DATA0 | 0x40630400 | FULL | Memory buffer |
| SCB3_EZ_DATA1 | 0x40630404 | FULL | Memory buffer |
| SCB3_EZ_DATA2 | 0x40630408 | FULL | Memory buffer |
| SCB3_EZ_DATA3 | 0x4063040C | FULL | Memory buffer |
| SCB3_EZ_DATA4 | 0x40630410 | FULL | Memory buffer |
| SCB3_EZ_DATA5 | 0x40630414 | FULL | Memory buffer |
| SCB3_EZ_DATA6 | 0x40630418 | FULL | Memory buffer |
| SCB3_EZ_DATA7 | 0x4063041C | FULL | Memory buffer |
| SCB3_EZ_DATA8 | 0x40630420 | FULL | Memory buffer |
| SCB3_EZ_DATA9 | 0x40630424 | FULL | Memory buffer |
| SCB3_EZ_DATA10 | 0x40630428 | FULL | Memory buffer |
| SCB3_EZ_DATA11 | 0x4063042C | FULL | Memory buffer |
| SCB3_EZ_DATA12 | 0x40630430 | FULL | Memory buffer |
| SCB3_EZ_DATA13 | 0x40630434 | FULL | Memory buffer |
| SCB3_EZ_DATA14 | 0x40630438 | FULL | Memory buffer |
| SCB3_EZ_DATA15 | 0x4063043C | FULL | Memory buffer |
| SCB3_EZ_DATA16 | 0x40630440 | FULL | Memory buffer |
| SCB3_EZ_DATA17 | 0x40630444 | FULL | Memory buffer |
| SCB3_EZ_DATA18 | 0x40630448 | FULL | Memory buffer |
| SCB3_EZ_DATA19 | 0x4063044C | FULL | Memory buffer |
| SCB3_EZ_DATA20 | 0x40630450 | FULL | Memory buffer |
| SCB3_EZ_DATA21 | 0x40630454 | FULL | Memory buffer |
| SCB3_EZ_DATA22 | 0x40630458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB3_EZ_DATA23 | 0x4063045C | FULL | Memory buffer |
| SCB3_EZ_DATA24 | 0x40630460 | FULL | Memory buffer |
| SCB3_EZ_DATA25 | 0x40630464 | FULL | Memory buffer |
| SCB3_EZ_DATA26 | 0x40630468 | FULL | Memory buffer |
| SCB3_EZ_DATA27 | 0x4063046C | FULL | Memory buffer |
| SCB3_EZ_DATA28 | 0x40630470 | FULL | Memory buffer |
| SCB3_EZ_DATA29 | 0x40630474 | FULL | Memory buffer |
| SCB3_EZ_DATA30 | 0x40630478 | FULL | Memory buffer |
| SCB3_EZ_DATA31 | 0x4063047C | FULL | Memory buffer |
| SCB3_EZ_DATA32 | 0x40630480 | FULL | Memory buffer |
| SCB3_EZ_DATA33 | 0x40630484 | FULL | Memory buffer |
| SCB3_EZ_DATA34 | 0x40630488 | FULL | Memory buffer |
| SCB3_EZ_DATA35 | 0x4063048C | FULL | Memory buffer |
| SCB3_EZ_DATA36 | 0x40630490 | FULL | Memory buffer |
| SCB3_EZ_DATA37 | 0x40630494 | FULL | Memory buffer |
| SCB3_EZ_DATA38 | 0x40630498 | FULL | Memory buffer |
| SCB3_EZ_DATA39 | 0x4063049C | FULL | Memory buffer |
| SCB3_EZ_DATA40 | 0x406304A0 | FULL | Memory buffer |
| SCB3_EZ_DATA41 | 0x406304A4 | FULL | Memory buffer |
| SCB3_EZ_DATA42 | 0x406304A8 | FULL | Memory buffer |
| SCB3_EZ_DATA43 | 0x406304AC | FULL | Memory buffer |
| SCB3_EZ_DATA44 | 0x406304B0 | FULL | Memory buffer |
| SCB3_EZ_DATA45 | 0x406304B4 | FULL | Memory buffer |
| SCB3_EZ_DATA46 | 0x406304B8 | FULL | Memory buffer |
| SCB3_EZ_DATA47 | 0x406304BC | FULL | Memory buffer |
| SCB3_EZ_DATA48 | 0x406304C0 | FULL | Memory buffer |
| SCB3_EZ_DATA49 | 0x406304C4 | FULL | Memory buffer |
| SCB3_EZ_DATA50 | 0x406304C8 | FULL | Memory buffer |
| SCB3_EZ_DATA51 | 0x406304CC | FULL | Memory buffer |
| SCB3_EZ_DATA52 | 0x406304D0 | FULL | Memory buffer |
| SCB3_EZ_DATA53 | 0x406304D4 | FULL | Memory buffer |
| SCB3_EZ_DATA54 | 0x406304D8 | FULL | Memory buffer |
| SCB3_EZ_DATA55 | 0x406304DC | FULL | Memory buffer |
| SCB3_EZ_DATA56 | 0x406304E0 | FULL | Memory buffer |
| SCB3_EZ_DATA57 | 0x406304E4 | FULL | Memory buffer |
| SCB3_EZ_DATA58 | 0x406304E8 | FULL | Memory buffer |
| SCB3_EZ_DATA59 | 0x406304EC | FULL | Memory buffer |
| SCB3_EZ_DATA60 | 0x406304F0 | FULL | Memory buffer |
| SCB3_EZ_DATA61 | 0x406304F4 | FULL | Memory buffer |
| SCB3_EZ_DATA62 | 0x406304F8 | FULL | Memory buffer |
| SCB3_EZ_DATA63 | 0x406304FC | FULL | Memory buffer |
| SCB3_EZ_DATA64 | 0x40630500 | FULL | Memory buffer |
| SCB3_EZ_DATA65 | 0x40630504 | FULL | Memory buffer |
| SCB3_EZ_DATA66 | 0x40630508 | FULL | Memory buffer |
| SCB3_EZ_DATA67 | 0x4063050C | FULL | Memory buffer |
| SCB3_EZ_DATA68 | 0x40630510 | FULL | Memory buffer |
| SCB3_EZ_DATA69 | 0x40630514 | FULL | Memory buffer |
| SCB3_EZ_DATA70 | 0x40630518 | FULL | Memory buffer |
| SCB3_EZ_DATA71 | 0x4063051C | FULL | Memory buffer |
| SCB3_EZ_DATA72 | 0x40630520 | FULL | Memory buffer |
| SCB3_EZ_DATA73 | 0x40630524 | FULL | Memory buffer |
| SCB3_EZ_DATA74 | 0x40630528 | FULL | Memory buffer |
| SCB3_EZ_DATA75 | 0x4063052C | FULL | Memory buffer |
| SCB3_EZ_DATA76 | 0x40630530 | FULL | Memory buffer |
| SCB3_EZ_DATA77 | 0x40630534 | FULL | Memory buffer |
| SCB3_EZ_DATA78 | 0x40630538 | FULL | Memory buffer |
| SCB3_EZ_DATA79 | 0x4063053C | FULL | Memory buffer |
| SCB3_EZ_DATA80 | 0x40630540 | FULL | Memory buffer |
| SCB3_EZ_DATA81 | 0x40630544 | FULL | Memory buffer |
| SCB3_EZ_DATA82 | 0x40630548 | FULL | Memory buffer |
| SCB3_EZ_DATA83 | 0x4063054C | FULL | Memory buffer |
| SCB3_EZ_DATA84 | 0x40630550 | FULL | Memory buffer |
| SCB3_EZ_DATA85 | 0x40630554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB3_EZ_DATA86 | 0x40630558 | FULL | Memory buffer |
| SCB3_EZ_DATA87 | 0x4063055C | FULL | Memory buffer |
| SCB3_EZ_DATA88 | 0x40630560 | FULL | Memory buffer |
| SCB3_EZ_DATA89 | 0x40630564 | FULL | Memory buffer |
| SCB3_EZ_DATA90 | 0x40630568 | FULL | Memory buffer |
| SCB3_EZ_DATA91 | 0x4063056C | FULL | Memory buffer |
| SCB3_EZ_DATA92 | 0x40630570 | FULL | Memory buffer |
| SCB3_EZ_DATA93 | 0x40630574 | FULL | Memory buffer |
| SCB3_EZ_DATA94 | 0x40630578 | FULL | Memory buffer |
| SCB3_EZ_DATA95 | 0x4063057C | FULL | Memory buffer |
| SCB3_EZ_DATA96 | 0x40630580 | FULL | Memory buffer |
| SCB3_EZ_DATA97 | 0x40630584 | FULL | Memory buffer |
| SCB3_EZ_DATA98 | 0x40630588 | FULL | Memory buffer |
| SCB3_EZ_DATA99 | 0x4063058C | FULL | Memory buffer |
| SCB3_EZ_DATA100 | 0x40630590 | FULL | Memory buffer |
| SCB3_EZ_DATA101 | 0x40630594 | FULL | Memory buffer |
| SCB3_EZ_DATA102 | 0x40630598 | FULL | Memory buffer |
| SCB3_EZ_DATA103 | 0x4063059C | FULL | Memory buffer |
| SCB3_EZ_DATA104 | 0x406305A0 | FULL | Memory buffer |
| SCB3_EZ_DATA105 | 0x406305A4 | FULL | Memory buffer |
| SCB3_EZ_DATA106 | 0x406305A8 | FULL | Memory buffer |
| SCB3_EZ_DATA107 | 0x406305AC | FULL | Memory buffer |
| SCB3_EZ_DATA108 | 0x406305B0 | FULL | Memory buffer |
| SCB3_EZ_DATA109 | 0x406305B4 | FULL | Memory buffer |
| SCB3_EZ_DATA110 | 0x406305B8 | FULL | Memory buffer |
| SCB3_EZ_DATA111 | 0x406305BC | FULL | Memory buffer |
| SCB3_EZ_DATA112 | 0x406305C0 | FULL | Memory buffer |
| SCB3_EZ_DATA113 | 0x406305C4 | FULL | Memory buffer |
| SCB3_EZ_DATA114 | 0x406305C8 | FULL | Memory buffer |
| SCB3_EZ_DATA115 | 0x406305CC | FULL | Memory buffer |
| SCB3_EZ_DATA116 | 0x406305D0 | FULL | Memory buffer |
| SCB3_EZ_DATA117 | 0x406305D4 | FULL | Memory buffer |
| SCB3_EZ_DATA118 | 0x406305D8 | FULL | Memory buffer |
| SCB3_EZ_DATA119 | 0x406305DC | FULL | Memory buffer |
| SCB3_EZ_DATA120 | 0x406305E0 | FULL | Memory buffer |
| SCB3_EZ_DATA121 | 0x406305E4 | FULL | Memory buffer |
| SCB3_EZ_DATA122 | 0x406305E8 | FULL | Memory buffer |
| SCB3_EZ_DATA123 | 0x406305EC | FULL | Memory buffer |
| SCB3_EZ_DATA124 | 0x406305F0 | FULL | Memory buffer |
| SCB3_EZ_DATA125 | 0x406305F4 | FULL | Memory buffer |
| SCB3_EZ_DATA126 | 0x406305F8 | FULL | Memory buffer |
| SCB3_EZ_DATA127 | 0x406305FC | FULL | Memory buffer |
| SCB3_EZ_DATA128 | 0x40630600 | FULL | Memory buffer |
| SCB3_EZ_DATA129 | 0x40630604 | FULL | Memory buffer |
| SCB3_EZ_DATA130 | 0x40630608 | FULL | Memory buffer |
| SCB3_EZ_DATA131 | 0x4063060C | FULL | Memory buffer |
| SCB3_EZ_DATA132 | 0x40630610 | FULL | Memory buffer |
| SCB3_EZ_DATA133 | 0x40630614 | FULL | Memory buffer |
| SCB3_EZ_DATA134 | 0x40630618 | FULL | Memory buffer |
| SCB3_EZ_DATA135 | 0x4063061C | FULL | Memory buffer |
| SCB3_EZ_DATA136 | 0x40630620 | FULL | Memory buffer |
| SCB3_EZ_DATA137 | 0x40630624 | FULL | Memory buffer |
| SCB3_EZ_DATA138 | 0x40630628 | FULL | Memory buffer |
| SCB3_EZ_DATA139 | 0x4063062C | FULL | Memory buffer |
| SCB3_EZ_DATA140 | 0x40630630 | FULL | Memory buffer |
| SCB3_EZ_DATA141 | 0x40630634 | FULL | Memory buffer |
| SCB3_EZ_DATA142 | 0x40630638 | FULL | Memory buffer |
| SCB3_EZ_DATA143 | 0x4063063C | FULL | Memory buffer |
| SCB3_EZ_DATA144 | 0x40630640 | FULL | Memory buffer |
| SCB3_EZ_DATA145 | 0x40630644 | FULL | Memory buffer |
| SCB3_EZ_DATA146 | 0x40630648 | FULL | Memory buffer |
| SCB3_EZ_DATA147 | 0x4063064C | FULL | Memory buffer |
| SCB3_EZ_DATA148 | 0x40630650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB3_EZ_DATA149 | 0x40630654 | FULL | Memory buffer |
| SCB3_EZ_DATA150 | 0x40630658 | FULL | Memory buffer |
| SCB3_EZ_DATA151 | 0x4063065C | FULL | Memory buffer |
| SCB3_EZ_DATA152 | 0x40630660 | FULL | Memory buffer |
| SCB3_EZ_DATA153 | 0x40630664 | FULL | Memory buffer |
| SCB3_EZ_DATA154 | 0x40630668 | FULL | Memory buffer |
| SCB3_EZ_DATA155 | 0x4063066C | FULL | Memory buffer |
| SCB3_EZ_DATA156 | 0x40630670 | FULL | Memory buffer |
| SCB3_EZ_DATA157 | 0x40630674 | FULL | Memory buffer |
| SCB3_EZ_DATA158 | 0x40630678 | FULL | Memory buffer |
| SCB3_EZ_DATA159 | 0x4063067C | FULL | Memory buffer |
| SCB3_EZ_DATA160 | 0x40630680 | FULL | Memory buffer |
| SCB3_EZ_DATA161 | 0x40630684 | FULL | Memory buffer |
| SCB3_EZ_DATA162 | 0x40630688 | FULL | Memory buffer |
| SCB3_EZ_DATA163 | 0x4063068C | FULL | Memory buffer |
| SCB3_EZ_DATA164 | 0x40630690 | FULL | Memory buffer |
| SCB3_EZ_DATA165 | 0x40630694 | FULL | Memory buffer |
| SCB3_EZ_DATA166 | 0x40630698 | FULL | Memory buffer |
| SCB3_EZ_DATA167 | 0x4063069C | FULL | Memory buffer |
| SCB3_EZ_DATA168 | 0x406306A0 | FULL | Memory buffer |
| SCB3_EZ_DATA169 | 0x406306A4 | FULL | Memory buffer |
| SCB3_EZ_DATA170 | 0x406306A8 | FULL | Memory buffer |
| SCB3_EZ_DATA171 | 0x406306AC | FULL | Memory buffer |
| SCB3_EZ_DATA172 | 0x406306B0 | FULL | Memory buffer |
| SCB3_EZ_DATA173 | 0x406306B4 | FULL | Memory buffer |
| SCB3_EZ_DATA174 | 0x406306B8 | FULL | Memory buffer |
| SCB3_EZ_DATA175 | 0x406306BC | FULL | Memory buffer |
| SCB3_EZ_DATA176 | 0x406306C0 | FULL | Memory buffer |
| SCB3_EZ_DATA177 | 0x406306C4 | FULL | Memory buffer |
| SCB3_EZ_DATA178 | 0x406306C8 | FULL | Memory buffer |
| SCB3_EZ_DATA179 | 0x406306CC | FULL | Memory buffer |
| SCB3_EZ_DATA180 | 0x406306D0 | FULL | Memory buffer |
| SCB3_EZ_DATA181 | 0x406306D4 | FULL | Memory buffer |
| SCB3_EZ_DATA182 | 0x406306D8 | FULL | Memory buffer |
| SCB3_EZ_DATA183 | 0x406306DC | FULL | Memory buffer |
| SCB3_EZ_DATA184 | 0x406306E0 | FULL | Memory buffer |
| SCB3_EZ_DATA185 | 0x406306E4 | FULL | Memory buffer |
| SCB3_EZ_DATA186 | 0x406306E8 | FULL | Memory buffer |
| SCB3_EZ_DATA187 | 0x406306EC | FULL | Memory buffer |
| SCB3_EZ_DATA188 | 0x406306F0 | FULL | Memory buffer |
| SCB3_EZ_DATA189 | 0x406306F4 | FULL | Memory buffer |
| SCB3_EZ_DATA190 | 0x406306F8 | FULL | Memory buffer |
| SCB3_EZ_DATA191 | 0x406306FC | FULL | Memory buffer |
| SCB3_EZ_DATA192 | 0x40630700 | FULL | Memory buffer |
| SCB3_EZ_DATA193 | 0x40630704 | FULL | Memory buffer |
| SCB3_EZ_DATA194 | 0x40630708 | FULL | Memory buffer |
| SCB3_EZ_DATA195 | 0x4063070C | FULL | Memory buffer |
| SCB3_EZ_DATA196 | 0x40630710 | FULL | Memory buffer |
| SCB3_EZ_DATA197 | 0x40630714 | FULL | Memory buffer |
| SCB3_EZ_DATA198 | 0x40630718 | FULL | Memory buffer |
| SCB3_EZ_DATA199 | 0x4063071C | FULL | Memory buffer |
| SCB3_EZ_DATA200 | 0x40630720 | FULL | Memory buffer |
| SCB3_EZ_DATA201 | 0x40630724 | FULL | Memory buffer |
| SCB3_EZ_DATA202 | 0x40630728 | FULL | Memory buffer |
| SCB3_EZ_DATA203 | 0x4063072C | FULL | Memory buffer |
| SCB3_EZ_DATA204 | 0x40630730 | FULL | Memory buffer |
| SCB3_EZ_DATA205 | 0x40630734 | FULL | Memory buffer |
| SCB3_EZ_DATA206 | 0x40630738 | FULL | Memory buffer |
| SCB3_EZ_DATA207 | 0x4063073C | FULL | Memory buffer |
| SCB3_EZ_DATA208 | 0x40630740 | FULL | Memory buffer |
| SCB3_EZ_DATA209 | 0x40630744 | FULL | Memory buffer |
| SCB3_EZ_DATA210 | 0x40630748 | FULL | Memory buffer |
| SCB3_EZ_DATA211 | 0x4063074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB3_EZ_DATA212 | 0x40630750 | FULL | Memory buffer |
| SCB3_EZ_DATA213 | 0x40630754 | FULL | Memory buffer |
| SCB3_EZ_DATA214 | 0x40630758 | FULL | Memory buffer |
| SCB3_EZ_DATA215 | 0x4063075C | FULL | Memory buffer |
| SCB3_EZ_DATA216 | 0x40630760 | FULL | Memory buffer |
| SCB3_EZ_DATA217 | 0x40630764 | FULL | Memory buffer |
| SCB3_EZ_DATA218 | 0x40630768 | FULL | Memory buffer |
| SCB3_EZ_DATA219 | 0x4063076C | FULL | Memory buffer |
| SCB3_EZ_DATA220 | 0x40630770 | FULL | Memory buffer |
| SCB3_EZ_DATA221 | 0x40630774 | FULL | Memory buffer |
| SCB3_EZ_DATA222 | 0x40630778 | FULL | Memory buffer |
| SCB3_EZ_DATA223 | 0x4063077C | FULL | Memory buffer |
| SCB3_EZ_DATA224 | 0x40630780 | FULL | Memory buffer |
| SCB3_EZ_DATA225 | 0x40630784 | FULL | Memory buffer |
| SCB3_EZ_DATA226 | 0x40630788 | FULL | Memory buffer |
| SCB3_EZ_DATA227 | 0x4063078C | FULL | Memory buffer |
| SCB3_EZ_DATA228 | 0x40630790 | FULL | Memory buffer |
| SCB3_EZ_DATA229 | 0x40630794 | FULL | Memory buffer |
| SCB3_EZ_DATA230 | 0x40630798 | FULL | Memory buffer |
| SCB3_EZ_DATA231 | 0x4063079C | FULL | Memory buffer |
| SCB3_EZ_DATA232 | 0x406307A0 | FULL | Memory buffer |
| SCB3_EZ_DATA233 | 0x406307A4 | FULL | Memory buffer |
| SCB3_EZ_DATA234 | 0x406307A8 | FULL | Memory buffer |
| SCB3_EZ_DATA235 | 0x406307AC | FULL | Memory buffer |
| SCB3_EZ_DATA236 | 0x406307B0 | FULL | Memory buffer |
| SCB3_EZ_DATA237 | 0x406307B4 | FULL | Memory buffer |
| SCB3_EZ_DATA238 | 0x406307B8 | FULL | Memory buffer |
| SCB3_EZ_DATA239 | 0x406307BC | FULL | Memory buffer |
| SCB3_EZ_DATA240 | 0x406307C0 | FULL | Memory buffer |
| SCB3_EZ_DATA241 | 0x406307C4 | FULL | Memory buffer |
| SCB3_EZ_DATA242 | 0x406307C8 | FULL | Memory buffer |
| SCB3_EZ_DATA243 | 0x406307CC | FULL | Memory buffer |
| SCB3_EZ_DATA244 | 0x406307D0 | FULL | Memory buffer |
| SCB3_EZ_DATA245 | 0x406307D4 | FULL | Memory buffer |
| SCB3_EZ_DATA246 | 0x406307D8 | FULL | Memory buffer |
| SCB3_EZ_DATA247 | 0x406307DC | FULL | Memory buffer |
| SCB3_EZ_DATA248 | 0x406307E0 | FULL | Memory buffer |
| SCB3_EZ_DATA249 | 0x406307E4 | FULL | Memory buffer |
| SCB3_EZ_DATA250 | 0x406307E8 | FULL | Memory buffer |
| SCB3_EZ_DATA251 | 0x406307EC | FULL | Memory buffer |
| SCB3_EZ_DATA252 | 0x406307F0 | FULL | Memory buffer |
| SCB3_EZ_DATA253 | 0x406307F4 | FULL | Memory buffer |
| SCB3_EZ_DATA254 | 0x406307F8 | FULL | Memory buffer |
| SCB3_EZ_DATA255 | 0x406307FC | FULL | Memory buffer |
| SCB3_INTR_CAUSE | 0x40630E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB3_INTR_SPI_EC | 0x40630EC0 | FULL | Externally clocked SPI interrupt request |
| SCB3_INTR_SPI_EC_MASK | 0x40630EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB3_INTR_SPI_EC_MASKED | 0x40630ECC | FULL | Externally clocked SPI interrupt masked |
| SCB3_INTR_M | 0x40630F00 | FULL | Master interrupt request |
| SCB3_INTR_M_SET | 0x40630F04 | FULL | Master interrupt set request |
| SCB3_INTR_M_MASK | 0x40630F08 | FULL | Master interrupt mask |
| SCB3_INTR_M_MASKED | 0x40630F0C | FULL | Master interrupt masked request |
| SCB3_INTR_S | 0x40630F40 | FULL | Slave interrupt request |
| SCB3_INTR_S_SET | 0x40630F44 | FULL | Slave interrupt set request |
| SCB3_INTR_S_MASK | 0x40630F48 | FULL | Slave interrupt mask |
| SCB3_INTR_S_MASKED | 0x40630F4C | FULL | Slave interrupt masked request |
| SCB3_INTR_TX | 0x40630F80 | FULL | Transmitter interrupt request |
| SCB3_INTR_TX_SET | 0x40630F84 | FULL | Transmitter interrupt set request |
| SCB3_INTR_TX_MASK | 0x40630F88 | FULL | Transmitter interrupt mask |
| SCB3_INTR_TX_MASKED | 0x40630F8C | FULL | Transmitter interrupt masked request |
| SCB3_INTR_RX | 0x40630FC0 | FULL | Receiver interrupt request |
| SCB3_INTR_RX_SET | 0x40630FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|-----------------------------------|
| SCB3_INTR_RX_MASK | 0x40630FC8 | FULL | Receiver interrupt mask |
| SCB3_INTR_RX_MASKED | 0x40630FCC | FULL | Receiver interrupt masked request |

23.5 SCB 4

Description Serial Communications Block
(SPI/UART/I2C)
Base Address 0x40640000
Size 0x10000
Slave Num MMIO6 - 4

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--|
| SCB4_CTRL | 0x40640000 | FULL | Generic control Note: CMD_RESP_MODE is not available for this register |
| SCB4_STATUS | 0x40640004 | FULL | Generic status |
| SCB4_SPI_CTRL | 0x40640020 | FULL | SPI control |
| SCB4_SPI_STATUS | 0x40640024 | FULL | SPI status |
| SCB4_SPI_TX_CTRL | 0x40640028 | FULL | SPI transmitter control |
| SCB4_SPI_RX_CTRL | 0x4064002C | FULL | SPI receiver control |
| SCB4_UART_CTRL | 0x40640040 | FULL | UART control |
| SCB4_UART_TX_CTRL | 0x40640044 | FULL | UART transmitter control |
| SCB4_UART_RX_CTRL | 0x40640048 | FULL | UART receiver control |
| SCB4_UART_RX_STATUS | 0x4064004C | FULL | UART receiver status |
| SCB4_UART_FLOW_CTRL | 0x40640050 | FULL | UART flow control |
| SCB4_I2C_CTRL | 0x40640060 | FULL | I2C control |
| SCB4_I2C_STATUS | 0x40640064 | FULL | I2C status Note: I2C_EC_BUSY is not available for this register |
| SCB4_I2C_M_CMD | 0x40640068 | FULL | I2C master command |
| SCB4_I2C_S_CMD | 0x4064006C | FULL | I2C slave command |
| SCB4_I2C_CFG | 0x40640070 | FULL | I2C configuration |
| SCB4_TX_CTRL | 0x40640200 | FULL | Transmitter control |
| SCB4_TX_FIFO_CTRL | 0x40640204 | FULL | Transmitter FIFO control |
| SCB4_TX_FIFO_STATUS | 0x40640208 | FULL | Transmitter FIFO status |
| SCB4_TX_FIFO_WR | 0x40640240 | FULL | Transmitter FIFO write |
| SCB4_RX_CTRL | 0x40640300 | FULL | Receiver control |
| SCB4_RX_FIFO_CTRL | 0x40640304 | FULL | Receiver FIFO control |
| SCB4_RX_FIFO_STATUS | 0x40640308 | FULL | Receiver FIFO status |
| SCB4_RX_MATCH | 0x40640310 | FULL | Slave address and mask |
| SCB4_RX_FIFO_RD | 0x40640340 | FULL | Receiver FIFO read |
| SCB4_RX_FIFO_RD_SILENT | 0x40640344 | FULL | Receiver FIFO read silent |
| SCB4_EZ_DATA0 | 0x40640400 | FULL | Memory buffer |
| SCB4_EZ_DATA1 | 0x40640404 | FULL | Memory buffer |
| SCB4_EZ_DATA2 | 0x40640408 | FULL | Memory buffer |
| SCB4_EZ_DATA3 | 0x4064040C | FULL | Memory buffer |
| SCB4_EZ_DATA4 | 0x40640410 | FULL | Memory buffer |
| SCB4_EZ_DATA5 | 0x40640414 | FULL | Memory buffer |
| SCB4_EZ_DATA6 | 0x40640418 | FULL | Memory buffer |
| SCB4_EZ_DATA7 | 0x4064041C | FULL | Memory buffer |
| SCB4_EZ_DATA8 | 0x40640420 | FULL | Memory buffer |
| SCB4_EZ_DATA9 | 0x40640424 | FULL | Memory buffer |
| SCB4_EZ_DATA10 | 0x40640428 | FULL | Memory buffer |
| SCB4_EZ_DATA11 | 0x4064042C | FULL | Memory buffer |
| SCB4_EZ_DATA12 | 0x40640430 | FULL | Memory buffer |
| SCB4_EZ_DATA13 | 0x40640434 | FULL | Memory buffer |
| SCB4_EZ_DATA14 | 0x40640438 | FULL | Memory buffer |
| SCB4_EZ_DATA15 | 0x4064043C | FULL | Memory buffer |
| SCB4_EZ_DATA16 | 0x40640440 | FULL | Memory buffer |
| SCB4_EZ_DATA17 | 0x40640444 | FULL | Memory buffer |
| SCB4_EZ_DATA18 | 0x40640448 | FULL | Memory buffer |
| SCB4_EZ_DATA19 | 0x4064044C | FULL | Memory buffer |
| SCB4_EZ_DATA20 | 0x40640450 | FULL | Memory buffer |
| SCB4_EZ_DATA21 | 0x40640454 | FULL | Memory buffer |
| SCB4_EZ_DATA22 | 0x40640458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB4_EZ_DATA23 | 0x4064045C | FULL | Memory buffer |
| SCB4_EZ_DATA24 | 0x40640460 | FULL | Memory buffer |
| SCB4_EZ_DATA25 | 0x40640464 | FULL | Memory buffer |
| SCB4_EZ_DATA26 | 0x40640468 | FULL | Memory buffer |
| SCB4_EZ_DATA27 | 0x4064046C | FULL | Memory buffer |
| SCB4_EZ_DATA28 | 0x40640470 | FULL | Memory buffer |
| SCB4_EZ_DATA29 | 0x40640474 | FULL | Memory buffer |
| SCB4_EZ_DATA30 | 0x40640478 | FULL | Memory buffer |
| SCB4_EZ_DATA31 | 0x4064047C | FULL | Memory buffer |
| SCB4_EZ_DATA32 | 0x40640480 | FULL | Memory buffer |
| SCB4_EZ_DATA33 | 0x40640484 | FULL | Memory buffer |
| SCB4_EZ_DATA34 | 0x40640488 | FULL | Memory buffer |
| SCB4_EZ_DATA35 | 0x4064048C | FULL | Memory buffer |
| SCB4_EZ_DATA36 | 0x40640490 | FULL | Memory buffer |
| SCB4_EZ_DATA37 | 0x40640494 | FULL | Memory buffer |
| SCB4_EZ_DATA38 | 0x40640498 | FULL | Memory buffer |
| SCB4_EZ_DATA39 | 0x4064049C | FULL | Memory buffer |
| SCB4_EZ_DATA40 | 0x406404A0 | FULL | Memory buffer |
| SCB4_EZ_DATA41 | 0x406404A4 | FULL | Memory buffer |
| SCB4_EZ_DATA42 | 0x406404A8 | FULL | Memory buffer |
| SCB4_EZ_DATA43 | 0x406404AC | FULL | Memory buffer |
| SCB4_EZ_DATA44 | 0x406404B0 | FULL | Memory buffer |
| SCB4_EZ_DATA45 | 0x406404B4 | FULL | Memory buffer |
| SCB4_EZ_DATA46 | 0x406404B8 | FULL | Memory buffer |
| SCB4_EZ_DATA47 | 0x406404BC | FULL | Memory buffer |
| SCB4_EZ_DATA48 | 0x406404C0 | FULL | Memory buffer |
| SCB4_EZ_DATA49 | 0x406404C4 | FULL | Memory buffer |
| SCB4_EZ_DATA50 | 0x406404C8 | FULL | Memory buffer |
| SCB4_EZ_DATA51 | 0x406404CC | FULL | Memory buffer |
| SCB4_EZ_DATA52 | 0x406404D0 | FULL | Memory buffer |
| SCB4_EZ_DATA53 | 0x406404D4 | FULL | Memory buffer |
| SCB4_EZ_DATA54 | 0x406404D8 | FULL | Memory buffer |
| SCB4_EZ_DATA55 | 0x406404DC | FULL | Memory buffer |
| SCB4_EZ_DATA56 | 0x406404E0 | FULL | Memory buffer |
| SCB4_EZ_DATA57 | 0x406404E4 | FULL | Memory buffer |
| SCB4_EZ_DATA58 | 0x406404E8 | FULL | Memory buffer |
| SCB4_EZ_DATA59 | 0x406404EC | FULL | Memory buffer |
| SCB4_EZ_DATA60 | 0x406404F0 | FULL | Memory buffer |
| SCB4_EZ_DATA61 | 0x406404F4 | FULL | Memory buffer |
| SCB4_EZ_DATA62 | 0x406404F8 | FULL | Memory buffer |
| SCB4_EZ_DATA63 | 0x406404FC | FULL | Memory buffer |
| SCB4_EZ_DATA64 | 0x40640500 | FULL | Memory buffer |
| SCB4_EZ_DATA65 | 0x40640504 | FULL | Memory buffer |
| SCB4_EZ_DATA66 | 0x40640508 | FULL | Memory buffer |
| SCB4_EZ_DATA67 | 0x4064050C | FULL | Memory buffer |
| SCB4_EZ_DATA68 | 0x40640510 | FULL | Memory buffer |
| SCB4_EZ_DATA69 | 0x40640514 | FULL | Memory buffer |
| SCB4_EZ_DATA70 | 0x40640518 | FULL | Memory buffer |
| SCB4_EZ_DATA71 | 0x4064051C | FULL | Memory buffer |
| SCB4_EZ_DATA72 | 0x40640520 | FULL | Memory buffer |
| SCB4_EZ_DATA73 | 0x40640524 | FULL | Memory buffer |
| SCB4_EZ_DATA74 | 0x40640528 | FULL | Memory buffer |
| SCB4_EZ_DATA75 | 0x4064052C | FULL | Memory buffer |
| SCB4_EZ_DATA76 | 0x40640530 | FULL | Memory buffer |
| SCB4_EZ_DATA77 | 0x40640534 | FULL | Memory buffer |
| SCB4_EZ_DATA78 | 0x40640538 | FULL | Memory buffer |
| SCB4_EZ_DATA79 | 0x4064053C | FULL | Memory buffer |
| SCB4_EZ_DATA80 | 0x40640540 | FULL | Memory buffer |
| SCB4_EZ_DATA81 | 0x40640544 | FULL | Memory buffer |
| SCB4_EZ_DATA82 | 0x40640548 | FULL | Memory buffer |
| SCB4_EZ_DATA83 | 0x4064054C | FULL | Memory buffer |
| SCB4_EZ_DATA84 | 0x40640550 | FULL | Memory buffer |
| SCB4_EZ_DATA85 | 0x40640554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB4_EZ_DATA86 | 0x40640558 | FULL | Memory buffer |
| SCB4_EZ_DATA87 | 0x4064055C | FULL | Memory buffer |
| SCB4_EZ_DATA88 | 0x40640560 | FULL | Memory buffer |
| SCB4_EZ_DATA89 | 0x40640564 | FULL | Memory buffer |
| SCB4_EZ_DATA90 | 0x40640568 | FULL | Memory buffer |
| SCB4_EZ_DATA91 | 0x4064056C | FULL | Memory buffer |
| SCB4_EZ_DATA92 | 0x40640570 | FULL | Memory buffer |
| SCB4_EZ_DATA93 | 0x40640574 | FULL | Memory buffer |
| SCB4_EZ_DATA94 | 0x40640578 | FULL | Memory buffer |
| SCB4_EZ_DATA95 | 0x4064057C | FULL | Memory buffer |
| SCB4_EZ_DATA96 | 0x40640580 | FULL | Memory buffer |
| SCB4_EZ_DATA97 | 0x40640584 | FULL | Memory buffer |
| SCB4_EZ_DATA98 | 0x40640588 | FULL | Memory buffer |
| SCB4_EZ_DATA99 | 0x4064058C | FULL | Memory buffer |
| SCB4_EZ_DATA100 | 0x40640590 | FULL | Memory buffer |
| SCB4_EZ_DATA101 | 0x40640594 | FULL | Memory buffer |
| SCB4_EZ_DATA102 | 0x40640598 | FULL | Memory buffer |
| SCB4_EZ_DATA103 | 0x4064059C | FULL | Memory buffer |
| SCB4_EZ_DATA104 | 0x406405A0 | FULL | Memory buffer |
| SCB4_EZ_DATA105 | 0x406405A4 | FULL | Memory buffer |
| SCB4_EZ_DATA106 | 0x406405A8 | FULL | Memory buffer |
| SCB4_EZ_DATA107 | 0x406405AC | FULL | Memory buffer |
| SCB4_EZ_DATA108 | 0x406405B0 | FULL | Memory buffer |
| SCB4_EZ_DATA109 | 0x406405B4 | FULL | Memory buffer |
| SCB4_EZ_DATA110 | 0x406405B8 | FULL | Memory buffer |
| SCB4_EZ_DATA111 | 0x406405BC | FULL | Memory buffer |
| SCB4_EZ_DATA112 | 0x406405C0 | FULL | Memory buffer |
| SCB4_EZ_DATA113 | 0x406405C4 | FULL | Memory buffer |
| SCB4_EZ_DATA114 | 0x406405C8 | FULL | Memory buffer |
| SCB4_EZ_DATA115 | 0x406405CC | FULL | Memory buffer |
| SCB4_EZ_DATA116 | 0x406405D0 | FULL | Memory buffer |
| SCB4_EZ_DATA117 | 0x406405D4 | FULL | Memory buffer |
| SCB4_EZ_DATA118 | 0x406405D8 | FULL | Memory buffer |
| SCB4_EZ_DATA119 | 0x406405DC | FULL | Memory buffer |
| SCB4_EZ_DATA120 | 0x406405E0 | FULL | Memory buffer |
| SCB4_EZ_DATA121 | 0x406405E4 | FULL | Memory buffer |
| SCB4_EZ_DATA122 | 0x406405E8 | FULL | Memory buffer |
| SCB4_EZ_DATA123 | 0x406405EC | FULL | Memory buffer |
| SCB4_EZ_DATA124 | 0x406405F0 | FULL | Memory buffer |
| SCB4_EZ_DATA125 | 0x406405F4 | FULL | Memory buffer |
| SCB4_EZ_DATA126 | 0x406405F8 | FULL | Memory buffer |
| SCB4_EZ_DATA127 | 0x406405FC | FULL | Memory buffer |
| SCB4_EZ_DATA128 | 0x40640600 | FULL | Memory buffer |
| SCB4_EZ_DATA129 | 0x40640604 | FULL | Memory buffer |
| SCB4_EZ_DATA130 | 0x40640608 | FULL | Memory buffer |
| SCB4_EZ_DATA131 | 0x4064060C | FULL | Memory buffer |
| SCB4_EZ_DATA132 | 0x40640610 | FULL | Memory buffer |
| SCB4_EZ_DATA133 | 0x40640614 | FULL | Memory buffer |
| SCB4_EZ_DATA134 | 0x40640618 | FULL | Memory buffer |
| SCB4_EZ_DATA135 | 0x4064061C | FULL | Memory buffer |
| SCB4_EZ_DATA136 | 0x40640620 | FULL | Memory buffer |
| SCB4_EZ_DATA137 | 0x40640624 | FULL | Memory buffer |
| SCB4_EZ_DATA138 | 0x40640628 | FULL | Memory buffer |
| SCB4_EZ_DATA139 | 0x4064062C | FULL | Memory buffer |
| SCB4_EZ_DATA140 | 0x40640630 | FULL | Memory buffer |
| SCB4_EZ_DATA141 | 0x40640634 | FULL | Memory buffer |
| SCB4_EZ_DATA142 | 0x40640638 | FULL | Memory buffer |
| SCB4_EZ_DATA143 | 0x4064063C | FULL | Memory buffer |
| SCB4_EZ_DATA144 | 0x40640640 | FULL | Memory buffer |
| SCB4_EZ_DATA145 | 0x40640644 | FULL | Memory buffer |
| SCB4_EZ_DATA146 | 0x40640648 | FULL | Memory buffer |
| SCB4_EZ_DATA147 | 0x4064064C | FULL | Memory buffer |
| SCB4_EZ_DATA148 | 0x40640650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB4_EZ_DATA149 | 0x40640654 | FULL | Memory buffer |
| SCB4_EZ_DATA150 | 0x40640658 | FULL | Memory buffer |
| SCB4_EZ_DATA151 | 0x4064065C | FULL | Memory buffer |
| SCB4_EZ_DATA152 | 0x40640660 | FULL | Memory buffer |
| SCB4_EZ_DATA153 | 0x40640664 | FULL | Memory buffer |
| SCB4_EZ_DATA154 | 0x40640668 | FULL | Memory buffer |
| SCB4_EZ_DATA155 | 0x4064066C | FULL | Memory buffer |
| SCB4_EZ_DATA156 | 0x40640670 | FULL | Memory buffer |
| SCB4_EZ_DATA157 | 0x40640674 | FULL | Memory buffer |
| SCB4_EZ_DATA158 | 0x40640678 | FULL | Memory buffer |
| SCB4_EZ_DATA159 | 0x4064067C | FULL | Memory buffer |
| SCB4_EZ_DATA160 | 0x40640680 | FULL | Memory buffer |
| SCB4_EZ_DATA161 | 0x40640684 | FULL | Memory buffer |
| SCB4_EZ_DATA162 | 0x40640688 | FULL | Memory buffer |
| SCB4_EZ_DATA163 | 0x4064068C | FULL | Memory buffer |
| SCB4_EZ_DATA164 | 0x40640690 | FULL | Memory buffer |
| SCB4_EZ_DATA165 | 0x40640694 | FULL | Memory buffer |
| SCB4_EZ_DATA166 | 0x40640698 | FULL | Memory buffer |
| SCB4_EZ_DATA167 | 0x4064069C | FULL | Memory buffer |
| SCB4_EZ_DATA168 | 0x406406A0 | FULL | Memory buffer |
| SCB4_EZ_DATA169 | 0x406406A4 | FULL | Memory buffer |
| SCB4_EZ_DATA170 | 0x406406A8 | FULL | Memory buffer |
| SCB4_EZ_DATA171 | 0x406406AC | FULL | Memory buffer |
| SCB4_EZ_DATA172 | 0x406406B0 | FULL | Memory buffer |
| SCB4_EZ_DATA173 | 0x406406B4 | FULL | Memory buffer |
| SCB4_EZ_DATA174 | 0x406406B8 | FULL | Memory buffer |
| SCB4_EZ_DATA175 | 0x406406BC | FULL | Memory buffer |
| SCB4_EZ_DATA176 | 0x406406C0 | FULL | Memory buffer |
| SCB4_EZ_DATA177 | 0x406406C4 | FULL | Memory buffer |
| SCB4_EZ_DATA178 | 0x406406C8 | FULL | Memory buffer |
| SCB4_EZ_DATA179 | 0x406406CC | FULL | Memory buffer |
| SCB4_EZ_DATA180 | 0x406406D0 | FULL | Memory buffer |
| SCB4_EZ_DATA181 | 0x406406D4 | FULL | Memory buffer |
| SCB4_EZ_DATA182 | 0x406406D8 | FULL | Memory buffer |
| SCB4_EZ_DATA183 | 0x406406DC | FULL | Memory buffer |
| SCB4_EZ_DATA184 | 0x406406E0 | FULL | Memory buffer |
| SCB4_EZ_DATA185 | 0x406406E4 | FULL | Memory buffer |
| SCB4_EZ_DATA186 | 0x406406E8 | FULL | Memory buffer |
| SCB4_EZ_DATA187 | 0x406406EC | FULL | Memory buffer |
| SCB4_EZ_DATA188 | 0x406406F0 | FULL | Memory buffer |
| SCB4_EZ_DATA189 | 0x406406F4 | FULL | Memory buffer |
| SCB4_EZ_DATA190 | 0x406406F8 | FULL | Memory buffer |
| SCB4_EZ_DATA191 | 0x406406FC | FULL | Memory buffer |
| SCB4_EZ_DATA192 | 0x40640700 | FULL | Memory buffer |
| SCB4_EZ_DATA193 | 0x40640704 | FULL | Memory buffer |
| SCB4_EZ_DATA194 | 0x40640708 | FULL | Memory buffer |
| SCB4_EZ_DATA195 | 0x4064070C | FULL | Memory buffer |
| SCB4_EZ_DATA196 | 0x40640710 | FULL | Memory buffer |
| SCB4_EZ_DATA197 | 0x40640714 | FULL | Memory buffer |
| SCB4_EZ_DATA198 | 0x40640718 | FULL | Memory buffer |
| SCB4_EZ_DATA199 | 0x4064071C | FULL | Memory buffer |
| SCB4_EZ_DATA200 | 0x40640720 | FULL | Memory buffer |
| SCB4_EZ_DATA201 | 0x40640724 | FULL | Memory buffer |
| SCB4_EZ_DATA202 | 0x40640728 | FULL | Memory buffer |
| SCB4_EZ_DATA203 | 0x4064072C | FULL | Memory buffer |
| SCB4_EZ_DATA204 | 0x40640730 | FULL | Memory buffer |
| SCB4_EZ_DATA205 | 0x40640734 | FULL | Memory buffer |
| SCB4_EZ_DATA206 | 0x40640738 | FULL | Memory buffer |
| SCB4_EZ_DATA207 | 0x4064073C | FULL | Memory buffer |
| SCB4_EZ_DATA208 | 0x40640740 | FULL | Memory buffer |
| SCB4_EZ_DATA209 | 0x40640744 | FULL | Memory buffer |
| SCB4_EZ_DATA210 | 0x40640748 | FULL | Memory buffer |
| SCB4_EZ_DATA211 | 0x4064074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB4_EZ_DATA212 | 0x40640750 | FULL | Memory buffer |
| SCB4_EZ_DATA213 | 0x40640754 | FULL | Memory buffer |
| SCB4_EZ_DATA214 | 0x40640758 | FULL | Memory buffer |
| SCB4_EZ_DATA215 | 0x4064075C | FULL | Memory buffer |
| SCB4_EZ_DATA216 | 0x40640760 | FULL | Memory buffer |
| SCB4_EZ_DATA217 | 0x40640764 | FULL | Memory buffer |
| SCB4_EZ_DATA218 | 0x40640768 | FULL | Memory buffer |
| SCB4_EZ_DATA219 | 0x4064076C | FULL | Memory buffer |
| SCB4_EZ_DATA220 | 0x40640770 | FULL | Memory buffer |
| SCB4_EZ_DATA221 | 0x40640774 | FULL | Memory buffer |
| SCB4_EZ_DATA222 | 0x40640778 | FULL | Memory buffer |
| SCB4_EZ_DATA223 | 0x4064077C | FULL | Memory buffer |
| SCB4_EZ_DATA224 | 0x40640780 | FULL | Memory buffer |
| SCB4_EZ_DATA225 | 0x40640784 | FULL | Memory buffer |
| SCB4_EZ_DATA226 | 0x40640788 | FULL | Memory buffer |
| SCB4_EZ_DATA227 | 0x4064078C | FULL | Memory buffer |
| SCB4_EZ_DATA228 | 0x40640790 | FULL | Memory buffer |
| SCB4_EZ_DATA229 | 0x40640794 | FULL | Memory buffer |
| SCB4_EZ_DATA230 | 0x40640798 | FULL | Memory buffer |
| SCB4_EZ_DATA231 | 0x4064079C | FULL | Memory buffer |
| SCB4_EZ_DATA232 | 0x406407A0 | FULL | Memory buffer |
| SCB4_EZ_DATA233 | 0x406407A4 | FULL | Memory buffer |
| SCB4_EZ_DATA234 | 0x406407A8 | FULL | Memory buffer |
| SCB4_EZ_DATA235 | 0x406407AC | FULL | Memory buffer |
| SCB4_EZ_DATA236 | 0x406407B0 | FULL | Memory buffer |
| SCB4_EZ_DATA237 | 0x406407B4 | FULL | Memory buffer |
| SCB4_EZ_DATA238 | 0x406407B8 | FULL | Memory buffer |
| SCB4_EZ_DATA239 | 0x406407BC | FULL | Memory buffer |
| SCB4_EZ_DATA240 | 0x406407C0 | FULL | Memory buffer |
| SCB4_EZ_DATA241 | 0x406407C4 | FULL | Memory buffer |
| SCB4_EZ_DATA242 | 0x406407C8 | FULL | Memory buffer |
| SCB4_EZ_DATA243 | 0x406407CC | FULL | Memory buffer |
| SCB4_EZ_DATA244 | 0x406407D0 | FULL | Memory buffer |
| SCB4_EZ_DATA245 | 0x406407D4 | FULL | Memory buffer |
| SCB4_EZ_DATA246 | 0x406407D8 | FULL | Memory buffer |
| SCB4_EZ_DATA247 | 0x406407DC | FULL | Memory buffer |
| SCB4_EZ_DATA248 | 0x406407E0 | FULL | Memory buffer |
| SCB4_EZ_DATA249 | 0x406407E4 | FULL | Memory buffer |
| SCB4_EZ_DATA250 | 0x406407E8 | FULL | Memory buffer |
| SCB4_EZ_DATA251 | 0x406407EC | FULL | Memory buffer |
| SCB4_EZ_DATA252 | 0x406407F0 | FULL | Memory buffer |
| SCB4_EZ_DATA253 | 0x406407F4 | FULL | Memory buffer |
| SCB4_EZ_DATA254 | 0x406407F8 | FULL | Memory buffer |
| SCB4_EZ_DATA255 | 0x406407FC | FULL | Memory buffer |
| SCB4_INTR_CAUSE | 0x40640E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB4_INTR_SPI_EC | 0x40640EC0 | FULL | Externally clocked SPI interrupt request |
| SCB4_INTR_SPI_EC_MASK | 0x40640EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB4_INTR_SPI_EC_MASKED | 0x40640ECC | FULL | Externally clocked SPI interrupt masked |
| SCB4_INTR_M | 0x40640F00 | FULL | Master interrupt request |
| SCB4_INTR_M_SET | 0x40640F04 | FULL | Master interrupt set request |
| SCB4_INTR_M_MASK | 0x40640F08 | FULL | Master interrupt mask |
| SCB4_INTR_M_MASKED | 0x40640F0C | FULL | Master interrupt masked request |
| SCB4_INTR_S | 0x40640F40 | FULL | Slave interrupt request |
| SCB4_INTR_S_SET | 0x40640F44 | FULL | Slave interrupt set request |
| SCB4_INTR_S_MASK | 0x40640F48 | FULL | Slave interrupt mask |
| SCB4_INTR_S_MASKED | 0x40640F4C | FULL | Slave interrupt masked request |
| SCB4_INTR_TX | 0x40640F80 | FULL | Transmitter interrupt request |
| SCB4_INTR_TX_SET | 0x40640F84 | FULL | Transmitter interrupt set request |
| SCB4_INTR_TX_MASK | 0x40640F88 | FULL | Transmitter interrupt mask |
| SCB4_INTR_TX_MASKED | 0x40640F8C | FULL | Transmitter interrupt masked request |
| SCB4_INTR_RX | 0x40640FC0 | FULL | Receiver interrupt request |
| SCB4_INTR_RX_SET | 0x40640FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|-----------------------------------|
| SCB4_INTR_RX_MASK | 0x40640FC8 | FULL | Receiver interrupt mask |
| SCB4_INTR_RX_MASKED | 0x40640FCC | FULL | Receiver interrupt masked request |

23.6 SCB 5

Description Serial Communications Block
(SPI/UART/I2C)
Base Address 0x40650000
Size 0x10000
Slave Num MMIO6 - 5

| Register Name | Address | Permission | Description |
|--|------------|------------|--|
| SCB5_CTRL | 0x40650000 | FULL | Generic control Note: CMD_RESP_MODE is not available for this register |
| SCB5_STATUS | 0x40650004 | FULL | Generic status |
| SCB5_SPI_CTRL | 0x40650020 | FULL | SPI control |
| SCB5_SPI_STATUS | 0x40650024 | FULL | SPI status |
| SCB5_SPI_TX_CTRL | 0x40650028 | FULL | SPI transmitter control |
| SCB5_SPI_RX_CTRL | 0x4065002C | FULL | SPI receiver control |
| SCB5_UART_CTRL | 0x40650040 | FULL | UART control |
| SCB5_UART_TX_CTRL | 0x40650044 | FULL | UART transmitter control |
| SCB5_UART_RX_CTRL | 0x40650048 | FULL | UART receiver control |
| SCB5_UART_RX_STATUS | 0x4065004C | FULL | UART receiver status |
| SCB5_UART_FLOW_CTRL | 0x40650050 | FULL | UART flow control |
| SCB5_I2C_CTRL | 0x40650060 | FULL | I2C control |
| SCB5_I2C_STATUS | 0x40650064 | FULL | I2C status Note: I2C_EC_BUSY is not available for this register |
| SCB5_I2C_M_CMD | 0x40650068 | FULL | I2C master command |
| SCB5_I2C_S_CMD | 0x4065006C | FULL | I2C slave command |
| SCB5_I2C_CFG | 0x40650070 | FULL | I2C configuration |
| SCB5_TX_CTRL | 0x40650200 | FULL | Transmitter control |
| SCB5_TX_FIFO_CTRL | 0x40650204 | FULL | Transmitter FIFO control |
| SCB5_TX_FIFO_STATUS | 0x40650208 | FULL | Transmitter FIFO status |
| SCB5_TX_FIFO_WR | 0x40650240 | FULL | Transmitter FIFO write |
| SCB5_RX_CTRL | 0x40650300 | FULL | Receiver control |
| SCB5_RX_FIFO_CTRL | 0x40650304 | FULL | Receiver FIFO control |
| SCB5_RX_FIFO_STATUS | 0x40650308 | FULL | Receiver FIFO status |
| SCB5_RX_MATCH | 0x40650310 | FULL | Slave address and mask |
| SCB5_RX_FIFO_RD | 0x40650340 | FULL | Receiver FIFO read |
| SCB5_RX_FIFO_RD_SILENT | 0x40650344 | FULL | Receiver FIFO read silent |
| SCB5_EZ_DATA0 | 0x40650400 | FULL | Memory buffer |
| SCB5_EZ_DATA1 | 0x40650404 | FULL | Memory buffer |
| SCB5_EZ_DATA2 | 0x40650408 | FULL | Memory buffer |
| SCB5_EZ_DATA3 | 0x4065040C | FULL | Memory buffer |
| SCB5_EZ_DATA4 | 0x40650410 | FULL | Memory buffer |
| SCB5_EZ_DATA5 | 0x40650414 | FULL | Memory buffer |
| SCB5_EZ_DATA6 | 0x40650418 | FULL | Memory buffer |
| SCB5_EZ_DATA7 | 0x4065041C | FULL | Memory buffer |
| SCB5_EZ_DATA8 | 0x40650420 | FULL | Memory buffer |
| SCB5_EZ_DATA9 | 0x40650424 | FULL | Memory buffer |
| SCB5_EZ_DATA10 | 0x40650428 | FULL | Memory buffer |
| SCB5_EZ_DATA11 | 0x4065042C | FULL | Memory buffer |
| SCB5_EZ_DATA12 | 0x40650430 | FULL | Memory buffer |
| SCB5_EZ_DATA13 | 0x40650434 | FULL | Memory buffer |
| SCB5_EZ_DATA14 | 0x40650438 | FULL | Memory buffer |
| SCB5_EZ_DATA15 | 0x4065043C | FULL | Memory buffer |
| SCB5_EZ_DATA16 | 0x40650440 | FULL | Memory buffer |
| SCB5_EZ_DATA17 | 0x40650444 | FULL | Memory buffer |
| SCB5_EZ_DATA18 | 0x40650448 | FULL | Memory buffer |
| SCB5_EZ_DATA19 | 0x4065044C | FULL | Memory buffer |
| SCB5_EZ_DATA20 | 0x40650450 | FULL | Memory buffer |
| SCB5_EZ_DATA21 | 0x40650454 | FULL | Memory buffer |
| SCB5_EZ_DATA22 | 0x40650458 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB5_EZ_DATA23 | 0x4065045C | FULL | Memory buffer |
| SCB5_EZ_DATA24 | 0x40650460 | FULL | Memory buffer |
| SCB5_EZ_DATA25 | 0x40650464 | FULL | Memory buffer |
| SCB5_EZ_DATA26 | 0x40650468 | FULL | Memory buffer |
| SCB5_EZ_DATA27 | 0x4065046C | FULL | Memory buffer |
| SCB5_EZ_DATA28 | 0x40650470 | FULL | Memory buffer |
| SCB5_EZ_DATA29 | 0x40650474 | FULL | Memory buffer |
| SCB5_EZ_DATA30 | 0x40650478 | FULL | Memory buffer |
| SCB5_EZ_DATA31 | 0x4065047C | FULL | Memory buffer |
| SCB5_EZ_DATA32 | 0x40650480 | FULL | Memory buffer |
| SCB5_EZ_DATA33 | 0x40650484 | FULL | Memory buffer |
| SCB5_EZ_DATA34 | 0x40650488 | FULL | Memory buffer |
| SCB5_EZ_DATA35 | 0x4065048C | FULL | Memory buffer |
| SCB5_EZ_DATA36 | 0x40650490 | FULL | Memory buffer |
| SCB5_EZ_DATA37 | 0x40650494 | FULL | Memory buffer |
| SCB5_EZ_DATA38 | 0x40650498 | FULL | Memory buffer |
| SCB5_EZ_DATA39 | 0x4065049C | FULL | Memory buffer |
| SCB5_EZ_DATA40 | 0x406504A0 | FULL | Memory buffer |
| SCB5_EZ_DATA41 | 0x406504A4 | FULL | Memory buffer |
| SCB5_EZ_DATA42 | 0x406504A8 | FULL | Memory buffer |
| SCB5_EZ_DATA43 | 0x406504AC | FULL | Memory buffer |
| SCB5_EZ_DATA44 | 0x406504B0 | FULL | Memory buffer |
| SCB5_EZ_DATA45 | 0x406504B4 | FULL | Memory buffer |
| SCB5_EZ_DATA46 | 0x406504B8 | FULL | Memory buffer |
| SCB5_EZ_DATA47 | 0x406504BC | FULL | Memory buffer |
| SCB5_EZ_DATA48 | 0x406504C0 | FULL | Memory buffer |
| SCB5_EZ_DATA49 | 0x406504C4 | FULL | Memory buffer |
| SCB5_EZ_DATA50 | 0x406504C8 | FULL | Memory buffer |
| SCB5_EZ_DATA51 | 0x406504CC | FULL | Memory buffer |
| SCB5_EZ_DATA52 | 0x406504D0 | FULL | Memory buffer |
| SCB5_EZ_DATA53 | 0x406504D4 | FULL | Memory buffer |
| SCB5_EZ_DATA54 | 0x406504D8 | FULL | Memory buffer |
| SCB5_EZ_DATA55 | 0x406504DC | FULL | Memory buffer |
| SCB5_EZ_DATA56 | 0x406504E0 | FULL | Memory buffer |
| SCB5_EZ_DATA57 | 0x406504E4 | FULL | Memory buffer |
| SCB5_EZ_DATA58 | 0x406504E8 | FULL | Memory buffer |
| SCB5_EZ_DATA59 | 0x406504EC | FULL | Memory buffer |
| SCB5_EZ_DATA60 | 0x406504F0 | FULL | Memory buffer |
| SCB5_EZ_DATA61 | 0x406504F4 | FULL | Memory buffer |
| SCB5_EZ_DATA62 | 0x406504F8 | FULL | Memory buffer |
| SCB5_EZ_DATA63 | 0x406504FC | FULL | Memory buffer |
| SCB5_EZ_DATA64 | 0x40650500 | FULL | Memory buffer |
| SCB5_EZ_DATA65 | 0x40650504 | FULL | Memory buffer |
| SCB5_EZ_DATA66 | 0x40650508 | FULL | Memory buffer |
| SCB5_EZ_DATA67 | 0x4065050C | FULL | Memory buffer |
| SCB5_EZ_DATA68 | 0x40650510 | FULL | Memory buffer |
| SCB5_EZ_DATA69 | 0x40650514 | FULL | Memory buffer |
| SCB5_EZ_DATA70 | 0x40650518 | FULL | Memory buffer |
| SCB5_EZ_DATA71 | 0x4065051C | FULL | Memory buffer |
| SCB5_EZ_DATA72 | 0x40650520 | FULL | Memory buffer |
| SCB5_EZ_DATA73 | 0x40650524 | FULL | Memory buffer |
| SCB5_EZ_DATA74 | 0x40650528 | FULL | Memory buffer |
| SCB5_EZ_DATA75 | 0x4065052C | FULL | Memory buffer |
| SCB5_EZ_DATA76 | 0x40650530 | FULL | Memory buffer |
| SCB5_EZ_DATA77 | 0x40650534 | FULL | Memory buffer |
| SCB5_EZ_DATA78 | 0x40650538 | FULL | Memory buffer |
| SCB5_EZ_DATA79 | 0x4065053C | FULL | Memory buffer |
| SCB5_EZ_DATA80 | 0x40650540 | FULL | Memory buffer |
| SCB5_EZ_DATA81 | 0x40650544 | FULL | Memory buffer |
| SCB5_EZ_DATA82 | 0x40650548 | FULL | Memory buffer |
| SCB5_EZ_DATA83 | 0x4065054C | FULL | Memory buffer |
| SCB5_EZ_DATA84 | 0x40650550 | FULL | Memory buffer |
| SCB5_EZ_DATA85 | 0x40650554 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB5_EZ_DATA86 | 0x40650558 | FULL | Memory buffer |
| SCB5_EZ_DATA87 | 0x4065055C | FULL | Memory buffer |
| SCB5_EZ_DATA88 | 0x40650560 | FULL | Memory buffer |
| SCB5_EZ_DATA89 | 0x40650564 | FULL | Memory buffer |
| SCB5_EZ_DATA90 | 0x40650568 | FULL | Memory buffer |
| SCB5_EZ_DATA91 | 0x4065056C | FULL | Memory buffer |
| SCB5_EZ_DATA92 | 0x40650570 | FULL | Memory buffer |
| SCB5_EZ_DATA93 | 0x40650574 | FULL | Memory buffer |
| SCB5_EZ_DATA94 | 0x40650578 | FULL | Memory buffer |
| SCB5_EZ_DATA95 | 0x4065057C | FULL | Memory buffer |
| SCB5_EZ_DATA96 | 0x40650580 | FULL | Memory buffer |
| SCB5_EZ_DATA97 | 0x40650584 | FULL | Memory buffer |
| SCB5_EZ_DATA98 | 0x40650588 | FULL | Memory buffer |
| SCB5_EZ_DATA99 | 0x4065058C | FULL | Memory buffer |
| SCB5_EZ_DATA100 | 0x40650590 | FULL | Memory buffer |
| SCB5_EZ_DATA101 | 0x40650594 | FULL | Memory buffer |
| SCB5_EZ_DATA102 | 0x40650598 | FULL | Memory buffer |
| SCB5_EZ_DATA103 | 0x4065059C | FULL | Memory buffer |
| SCB5_EZ_DATA104 | 0x406505A0 | FULL | Memory buffer |
| SCB5_EZ_DATA105 | 0x406505A4 | FULL | Memory buffer |
| SCB5_EZ_DATA106 | 0x406505A8 | FULL | Memory buffer |
| SCB5_EZ_DATA107 | 0x406505AC | FULL | Memory buffer |
| SCB5_EZ_DATA108 | 0x406505B0 | FULL | Memory buffer |
| SCB5_EZ_DATA109 | 0x406505B4 | FULL | Memory buffer |
| SCB5_EZ_DATA110 | 0x406505B8 | FULL | Memory buffer |
| SCB5_EZ_DATA111 | 0x406505BC | FULL | Memory buffer |
| SCB5_EZ_DATA112 | 0x406505C0 | FULL | Memory buffer |
| SCB5_EZ_DATA113 | 0x406505C4 | FULL | Memory buffer |
| SCB5_EZ_DATA114 | 0x406505C8 | FULL | Memory buffer |
| SCB5_EZ_DATA115 | 0x406505CC | FULL | Memory buffer |
| SCB5_EZ_DATA116 | 0x406505D0 | FULL | Memory buffer |
| SCB5_EZ_DATA117 | 0x406505D4 | FULL | Memory buffer |
| SCB5_EZ_DATA118 | 0x406505D8 | FULL | Memory buffer |
| SCB5_EZ_DATA119 | 0x406505DC | FULL | Memory buffer |
| SCB5_EZ_DATA120 | 0x406505E0 | FULL | Memory buffer |
| SCB5_EZ_DATA121 | 0x406505E4 | FULL | Memory buffer |
| SCB5_EZ_DATA122 | 0x406505E8 | FULL | Memory buffer |
| SCB5_EZ_DATA123 | 0x406505EC | FULL | Memory buffer |
| SCB5_EZ_DATA124 | 0x406505F0 | FULL | Memory buffer |
| SCB5_EZ_DATA125 | 0x406505F4 | FULL | Memory buffer |
| SCB5_EZ_DATA126 | 0x406505F8 | FULL | Memory buffer |
| SCB5_EZ_DATA127 | 0x406505FC | FULL | Memory buffer |
| SCB5_EZ_DATA128 | 0x40650600 | FULL | Memory buffer |
| SCB5_EZ_DATA129 | 0x40650604 | FULL | Memory buffer |
| SCB5_EZ_DATA130 | 0x40650608 | FULL | Memory buffer |
| SCB5_EZ_DATA131 | 0x4065060C | FULL | Memory buffer |
| SCB5_EZ_DATA132 | 0x40650610 | FULL | Memory buffer |
| SCB5_EZ_DATA133 | 0x40650614 | FULL | Memory buffer |
| SCB5_EZ_DATA134 | 0x40650618 | FULL | Memory buffer |
| SCB5_EZ_DATA135 | 0x4065061C | FULL | Memory buffer |
| SCB5_EZ_DATA136 | 0x40650620 | FULL | Memory buffer |
| SCB5_EZ_DATA137 | 0x40650624 | FULL | Memory buffer |
| SCB5_EZ_DATA138 | 0x40650628 | FULL | Memory buffer |
| SCB5_EZ_DATA139 | 0x4065062C | FULL | Memory buffer |
| SCB5_EZ_DATA140 | 0x40650630 | FULL | Memory buffer |
| SCB5_EZ_DATA141 | 0x40650634 | FULL | Memory buffer |
| SCB5_EZ_DATA142 | 0x40650638 | FULL | Memory buffer |
| SCB5_EZ_DATA143 | 0x4065063C | FULL | Memory buffer |
| SCB5_EZ_DATA144 | 0x40650640 | FULL | Memory buffer |
| SCB5_EZ_DATA145 | 0x40650644 | FULL | Memory buffer |
| SCB5_EZ_DATA146 | 0x40650648 | FULL | Memory buffer |
| SCB5_EZ_DATA147 | 0x4065064C | FULL | Memory buffer |
| SCB5_EZ_DATA148 | 0x40650650 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB5_EZ_DATA149 | 0x40650654 | FULL | Memory buffer |
| SCB5_EZ_DATA150 | 0x40650658 | FULL | Memory buffer |
| SCB5_EZ_DATA151 | 0x4065065C | FULL | Memory buffer |
| SCB5_EZ_DATA152 | 0x40650660 | FULL | Memory buffer |
| SCB5_EZ_DATA153 | 0x40650664 | FULL | Memory buffer |
| SCB5_EZ_DATA154 | 0x40650668 | FULL | Memory buffer |
| SCB5_EZ_DATA155 | 0x4065066C | FULL | Memory buffer |
| SCB5_EZ_DATA156 | 0x40650670 | FULL | Memory buffer |
| SCB5_EZ_DATA157 | 0x40650674 | FULL | Memory buffer |
| SCB5_EZ_DATA158 | 0x40650678 | FULL | Memory buffer |
| SCB5_EZ_DATA159 | 0x4065067C | FULL | Memory buffer |
| SCB5_EZ_DATA160 | 0x40650680 | FULL | Memory buffer |
| SCB5_EZ_DATA161 | 0x40650684 | FULL | Memory buffer |
| SCB5_EZ_DATA162 | 0x40650688 | FULL | Memory buffer |
| SCB5_EZ_DATA163 | 0x4065068C | FULL | Memory buffer |
| SCB5_EZ_DATA164 | 0x40650690 | FULL | Memory buffer |
| SCB5_EZ_DATA165 | 0x40650694 | FULL | Memory buffer |
| SCB5_EZ_DATA166 | 0x40650698 | FULL | Memory buffer |
| SCB5_EZ_DATA167 | 0x4065069C | FULL | Memory buffer |
| SCB5_EZ_DATA168 | 0x406506A0 | FULL | Memory buffer |
| SCB5_EZ_DATA169 | 0x406506A4 | FULL | Memory buffer |
| SCB5_EZ_DATA170 | 0x406506A8 | FULL | Memory buffer |
| SCB5_EZ_DATA171 | 0x406506AC | FULL | Memory buffer |
| SCB5_EZ_DATA172 | 0x406506B0 | FULL | Memory buffer |
| SCB5_EZ_DATA173 | 0x406506B4 | FULL | Memory buffer |
| SCB5_EZ_DATA174 | 0x406506B8 | FULL | Memory buffer |
| SCB5_EZ_DATA175 | 0x406506BC | FULL | Memory buffer |
| SCB5_EZ_DATA176 | 0x406506C0 | FULL | Memory buffer |
| SCB5_EZ_DATA177 | 0x406506C4 | FULL | Memory buffer |
| SCB5_EZ_DATA178 | 0x406506C8 | FULL | Memory buffer |
| SCB5_EZ_DATA179 | 0x406506CC | FULL | Memory buffer |
| SCB5_EZ_DATA180 | 0x406506D0 | FULL | Memory buffer |
| SCB5_EZ_DATA181 | 0x406506D4 | FULL | Memory buffer |
| SCB5_EZ_DATA182 | 0x406506D8 | FULL | Memory buffer |
| SCB5_EZ_DATA183 | 0x406506DC | FULL | Memory buffer |
| SCB5_EZ_DATA184 | 0x406506E0 | FULL | Memory buffer |
| SCB5_EZ_DATA185 | 0x406506E4 | FULL | Memory buffer |
| SCB5_EZ_DATA186 | 0x406506E8 | FULL | Memory buffer |
| SCB5_EZ_DATA187 | 0x406506EC | FULL | Memory buffer |
| SCB5_EZ_DATA188 | 0x406506F0 | FULL | Memory buffer |
| SCB5_EZ_DATA189 | 0x406506F4 | FULL | Memory buffer |
| SCB5_EZ_DATA190 | 0x406506F8 | FULL | Memory buffer |
| SCB5_EZ_DATA191 | 0x406506FC | FULL | Memory buffer |
| SCB5_EZ_DATA192 | 0x40650700 | FULL | Memory buffer |
| SCB5_EZ_DATA193 | 0x40650704 | FULL | Memory buffer |
| SCB5_EZ_DATA194 | 0x40650708 | FULL | Memory buffer |
| SCB5_EZ_DATA195 | 0x4065070C | FULL | Memory buffer |
| SCB5_EZ_DATA196 | 0x40650710 | FULL | Memory buffer |
| SCB5_EZ_DATA197 | 0x40650714 | FULL | Memory buffer |
| SCB5_EZ_DATA198 | 0x40650718 | FULL | Memory buffer |
| SCB5_EZ_DATA199 | 0x4065071C | FULL | Memory buffer |
| SCB5_EZ_DATA200 | 0x40650720 | FULL | Memory buffer |
| SCB5_EZ_DATA201 | 0x40650724 | FULL | Memory buffer |
| SCB5_EZ_DATA202 | 0x40650728 | FULL | Memory buffer |
| SCB5_EZ_DATA203 | 0x4065072C | FULL | Memory buffer |
| SCB5_EZ_DATA204 | 0x40650730 | FULL | Memory buffer |
| SCB5_EZ_DATA205 | 0x40650734 | FULL | Memory buffer |
| SCB5_EZ_DATA206 | 0x40650738 | FULL | Memory buffer |
| SCB5_EZ_DATA207 | 0x4065073C | FULL | Memory buffer |
| SCB5_EZ_DATA208 | 0x40650740 | FULL | Memory buffer |
| SCB5_EZ_DATA209 | 0x40650744 | FULL | Memory buffer |
| SCB5_EZ_DATA210 | 0x40650748 | FULL | Memory buffer |
| SCB5_EZ_DATA211 | 0x4065074C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB5_EZ_DATA212 | 0x40650750 | FULL | Memory buffer |
| SCB5_EZ_DATA213 | 0x40650754 | FULL | Memory buffer |
| SCB5_EZ_DATA214 | 0x40650758 | FULL | Memory buffer |
| SCB5_EZ_DATA215 | 0x4065075C | FULL | Memory buffer |
| SCB5_EZ_DATA216 | 0x40650760 | FULL | Memory buffer |
| SCB5_EZ_DATA217 | 0x40650764 | FULL | Memory buffer |
| SCB5_EZ_DATA218 | 0x40650768 | FULL | Memory buffer |
| SCB5_EZ_DATA219 | 0x4065076C | FULL | Memory buffer |
| SCB5_EZ_DATA220 | 0x40650770 | FULL | Memory buffer |
| SCB5_EZ_DATA221 | 0x40650774 | FULL | Memory buffer |
| SCB5_EZ_DATA222 | 0x40650778 | FULL | Memory buffer |
| SCB5_EZ_DATA223 | 0x4065077C | FULL | Memory buffer |
| SCB5_EZ_DATA224 | 0x40650780 | FULL | Memory buffer |
| SCB5_EZ_DATA225 | 0x40650784 | FULL | Memory buffer |
| SCB5_EZ_DATA226 | 0x40650788 | FULL | Memory buffer |
| SCB5_EZ_DATA227 | 0x4065078C | FULL | Memory buffer |
| SCB5_EZ_DATA228 | 0x40650790 | FULL | Memory buffer |
| SCB5_EZ_DATA229 | 0x40650794 | FULL | Memory buffer |
| SCB5_EZ_DATA230 | 0x40650798 | FULL | Memory buffer |
| SCB5_EZ_DATA231 | 0x4065079C | FULL | Memory buffer |
| SCB5_EZ_DATA232 | 0x406507A0 | FULL | Memory buffer |
| SCB5_EZ_DATA233 | 0x406507A4 | FULL | Memory buffer |
| SCB5_EZ_DATA234 | 0x406507A8 | FULL | Memory buffer |
| SCB5_EZ_DATA235 | 0x406507AC | FULL | Memory buffer |
| SCB5_EZ_DATA236 | 0x406507B0 | FULL | Memory buffer |
| SCB5_EZ_DATA237 | 0x406507B4 | FULL | Memory buffer |
| SCB5_EZ_DATA238 | 0x406507B8 | FULL | Memory buffer |
| SCB5_EZ_DATA239 | 0x406507BC | FULL | Memory buffer |
| SCB5_EZ_DATA240 | 0x406507C0 | FULL | Memory buffer |
| SCB5_EZ_DATA241 | 0x406507C4 | FULL | Memory buffer |
| SCB5_EZ_DATA242 | 0x406507C8 | FULL | Memory buffer |
| SCB5_EZ_DATA243 | 0x406507CC | FULL | Memory buffer |
| SCB5_EZ_DATA244 | 0x406507D0 | FULL | Memory buffer |
| SCB5_EZ_DATA245 | 0x406507D4 | FULL | Memory buffer |
| SCB5_EZ_DATA246 | 0x406507D8 | FULL | Memory buffer |
| SCB5_EZ_DATA247 | 0x406507DC | FULL | Memory buffer |
| SCB5_EZ_DATA248 | 0x406507E0 | FULL | Memory buffer |
| SCB5_EZ_DATA249 | 0x406507E4 | FULL | Memory buffer |
| SCB5_EZ_DATA250 | 0x406507E8 | FULL | Memory buffer |
| SCB5_EZ_DATA251 | 0x406507EC | FULL | Memory buffer |
| SCB5_EZ_DATA252 | 0x406507F0 | FULL | Memory buffer |
| SCB5_EZ_DATA253 | 0x406507F4 | FULL | Memory buffer |
| SCB5_EZ_DATA254 | 0x406507F8 | FULL | Memory buffer |
| SCB5_EZ_DATA255 | 0x406507FC | FULL | Memory buffer |
| SCB5_INTR_CAUSE | 0x40650E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB5_INTR_SPI_EC | 0x40650EC0 | FULL | Externally clocked SPI interrupt request |
| SCB5_INTR_SPI_EC_MASK | 0x40650EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB5_INTR_SPI_EC_MASKED | 0x40650ECC | FULL | Externally clocked SPI interrupt masked |
| SCB5_INTR_M | 0x40650F00 | FULL | Master interrupt request |
| SCB5_INTR_M_SET | 0x40650F04 | FULL | Master interrupt set request |
| SCB5_INTR_M_MASK | 0x40650F08 | FULL | Master interrupt mask |
| SCB5_INTR_M_MASKED | 0x40650F0C | FULL | Master interrupt masked request |
| SCB5_INTR_S | 0x40650F40 | FULL | Slave interrupt request |
| SCB5_INTR_S_SET | 0x40650F44 | FULL | Slave interrupt set request |
| SCB5_INTR_S_MASK | 0x40650F48 | FULL | Slave interrupt mask |
| SCB5_INTR_S_MASKED | 0x40650F4C | FULL | Slave interrupt masked request |
| SCB5_INTR_TX | 0x40650F80 | FULL | Transmitter interrupt request |
| SCB5_INTR_TX_SET | 0x40650F84 | FULL | Transmitter interrupt set request |
| SCB5_INTR_TX_MASK | 0x40650F88 | FULL | Transmitter interrupt mask |
| SCB5_INTR_TX_MASKED | 0x40650F8C | FULL | Transmitter interrupt masked request |
| SCB5_INTR_RX | 0x40650FC0 | FULL | Receiver interrupt request |
| SCB5_INTR_RX_SET | 0x40650FC4 | FULL | Receiver interrupt set request |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|-----------------------------------|
| SCB5_INTR_RX_MASK | 0x40650FC8 | FULL | Receiver interrupt mask |
| SCB5_INTR_RX_MASKED | 0x40650FCC | FULL | Receiver interrupt masked request |

23.7 SCB 6

Description Serial Communications Block
(SPI/UART/I2C)
Base Address 0x40660000
Size 0x10000
Slave Num MMIO6 - 6

This instance is not available in the following part numbers:
CYT2BL3BAS, CYT2BL3BAE, CYT2BL3CAS, CYT2BL3CAE.

| Register Name | Address | Permission | Description |
|--|------------|------------|--|
| SCB6_CTRL | 0x40660000 | FULL | Generic control Note: CMD_RESP_MODE is not available for this register |
| SCB6_STATUS | 0x40660004 | FULL | Generic status |
| SCB6_SPI_CTRL | 0x40660020 | FULL | SPI control |
| SCB6_SPI_STATUS | 0x40660024 | FULL | SPI status |
| SCB6_SPI_TX_CTRL | 0x40660028 | FULL | SPI transmitter control |
| SCB6_SPI_RX_CTRL | 0x4066002C | FULL | SPI receiver control |
| SCB6_UART_CTRL | 0x40660040 | FULL | UART control |
| SCB6_UART_TX_CTRL | 0x40660044 | FULL | UART transmitter control |
| SCB6_UART_RX_CTRL | 0x40660048 | FULL | UART receiver control |
| SCB6_UART_RX_STATUS | 0x4066004C | FULL | UART receiver status |
| SCB6_UART_FLOW_CTRL | 0x40660050 | FULL | UART flow control |
| SCB6_I2C_CTRL | 0x40660060 | FULL | I2C control |
| SCB6_I2C_STATUS | 0x40660064 | FULL | I2C status Note: I2C_EC_BUSY is not available for this register |
| SCB6_I2C_M_CMD | 0x40660068 | FULL | I2C master command |
| SCB6_I2C_S_CMD | 0x4066006C | FULL | I2C slave command |
| SCB6_I2C_CFG | 0x40660070 | FULL | I2C configuration |
| SCB6_TX_CTRL | 0x40660200 | FULL | Transmitter control |
| SCB6_TX_FIFO_CTRL | 0x40660204 | FULL | Transmitter FIFO control |
| SCB6_TX_FIFO_STATUS | 0x40660208 | FULL | Transmitter FIFO status |
| SCB6_TX_FIFO_WR | 0x40660240 | FULL | Transmitter FIFO write |
| SCB6_RX_CTRL | 0x40660300 | FULL | Receiver control |
| SCB6_RX_FIFO_CTRL | 0x40660304 | FULL | Receiver FIFO control |
| SCB6_RX_FIFO_STATUS | 0x40660308 | FULL | Receiver FIFO status |
| SCB6_RX_MATCH | 0x40660310 | FULL | Slave address and mask |
| SCB6_RX_FIFO_RD | 0x40660340 | FULL | Receiver FIFO read |
| SCB6_RX_FIFO_RD_SILENT | 0x40660344 | FULL | Receiver FIFO read silent |
| SCB6_EZ_DATA0 | 0x40660400 | FULL | Memory buffer |
| SCB6_EZ_DATA1 | 0x40660404 | FULL | Memory buffer |
| SCB6_EZ_DATA2 | 0x40660408 | FULL | Memory buffer |
| SCB6_EZ_DATA3 | 0x4066040C | FULL | Memory buffer |
| SCB6_EZ_DATA4 | 0x40660410 | FULL | Memory buffer |
| SCB6_EZ_DATA5 | 0x40660414 | FULL | Memory buffer |
| SCB6_EZ_DATA6 | 0x40660418 | FULL | Memory buffer |
| SCB6_EZ_DATA7 | 0x4066041C | FULL | Memory buffer |
| SCB6_EZ_DATA8 | 0x40660420 | FULL | Memory buffer |
| SCB6_EZ_DATA9 | 0x40660424 | FULL | Memory buffer |
| SCB6_EZ_DATA10 | 0x40660428 | FULL | Memory buffer |
| SCB6_EZ_DATA11 | 0x4066042C | FULL | Memory buffer |
| SCB6_EZ_DATA12 | 0x40660430 | FULL | Memory buffer |
| SCB6_EZ_DATA13 | 0x40660434 | FULL | Memory buffer |
| SCB6_EZ_DATA14 | 0x40660438 | FULL | Memory buffer |
| SCB6_EZ_DATA15 | 0x4066043C | FULL | Memory buffer |
| SCB6_EZ_DATA16 | 0x40660440 | FULL | Memory buffer |
| SCB6_EZ_DATA17 | 0x40660444 | FULL | Memory buffer |
| SCB6_EZ_DATA18 | 0x40660448 | FULL | Memory buffer |
| SCB6_EZ_DATA19 | 0x4066044C | FULL | Memory buffer |
| SCB6_EZ_DATA20 | 0x40660450 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB6_EZ_DATA21 | 0x40660454 | FULL | Memory buffer |
| SCB6_EZ_DATA22 | 0x40660458 | FULL | Memory buffer |
| SCB6_EZ_DATA23 | 0x4066045C | FULL | Memory buffer |
| SCB6_EZ_DATA24 | 0x40660460 | FULL | Memory buffer |
| SCB6_EZ_DATA25 | 0x40660464 | FULL | Memory buffer |
| SCB6_EZ_DATA26 | 0x40660468 | FULL | Memory buffer |
| SCB6_EZ_DATA27 | 0x4066046C | FULL | Memory buffer |
| SCB6_EZ_DATA28 | 0x40660470 | FULL | Memory buffer |
| SCB6_EZ_DATA29 | 0x40660474 | FULL | Memory buffer |
| SCB6_EZ_DATA30 | 0x40660478 | FULL | Memory buffer |
| SCB6_EZ_DATA31 | 0x4066047C | FULL | Memory buffer |
| SCB6_EZ_DATA32 | 0x40660480 | FULL | Memory buffer |
| SCB6_EZ_DATA33 | 0x40660484 | FULL | Memory buffer |
| SCB6_EZ_DATA34 | 0x40660488 | FULL | Memory buffer |
| SCB6_EZ_DATA35 | 0x4066048C | FULL | Memory buffer |
| SCB6_EZ_DATA36 | 0x40660490 | FULL | Memory buffer |
| SCB6_EZ_DATA37 | 0x40660494 | FULL | Memory buffer |
| SCB6_EZ_DATA38 | 0x40660498 | FULL | Memory buffer |
| SCB6_EZ_DATA39 | 0x4066049C | FULL | Memory buffer |
| SCB6_EZ_DATA40 | 0x406604A0 | FULL | Memory buffer |
| SCB6_EZ_DATA41 | 0x406604A4 | FULL | Memory buffer |
| SCB6_EZ_DATA42 | 0x406604A8 | FULL | Memory buffer |
| SCB6_EZ_DATA43 | 0x406604AC | FULL | Memory buffer |
| SCB6_EZ_DATA44 | 0x406604B0 | FULL | Memory buffer |
| SCB6_EZ_DATA45 | 0x406604B4 | FULL | Memory buffer |
| SCB6_EZ_DATA46 | 0x406604B8 | FULL | Memory buffer |
| SCB6_EZ_DATA47 | 0x406604BC | FULL | Memory buffer |
| SCB6_EZ_DATA48 | 0x406604C0 | FULL | Memory buffer |
| SCB6_EZ_DATA49 | 0x406604C4 | FULL | Memory buffer |
| SCB6_EZ_DATA50 | 0x406604C8 | FULL | Memory buffer |
| SCB6_EZ_DATA51 | 0x406604CC | FULL | Memory buffer |
| SCB6_EZ_DATA52 | 0x406604D0 | FULL | Memory buffer |
| SCB6_EZ_DATA53 | 0x406604D4 | FULL | Memory buffer |
| SCB6_EZ_DATA54 | 0x406604D8 | FULL | Memory buffer |
| SCB6_EZ_DATA55 | 0x406604DC | FULL | Memory buffer |
| SCB6_EZ_DATA56 | 0x406604E0 | FULL | Memory buffer |
| SCB6_EZ_DATA57 | 0x406604E4 | FULL | Memory buffer |
| SCB6_EZ_DATA58 | 0x406604E8 | FULL | Memory buffer |
| SCB6_EZ_DATA59 | 0x406604EC | FULL | Memory buffer |
| SCB6_EZ_DATA60 | 0x406604F0 | FULL | Memory buffer |
| SCB6_EZ_DATA61 | 0x406604F4 | FULL | Memory buffer |
| SCB6_EZ_DATA62 | 0x406604F8 | FULL | Memory buffer |
| SCB6_EZ_DATA63 | 0x406604FC | FULL | Memory buffer |
| SCB6_EZ_DATA64 | 0x40660500 | FULL | Memory buffer |
| SCB6_EZ_DATA65 | 0x40660504 | FULL | Memory buffer |
| SCB6_EZ_DATA66 | 0x40660508 | FULL | Memory buffer |
| SCB6_EZ_DATA67 | 0x4066050C | FULL | Memory buffer |
| SCB6_EZ_DATA68 | 0x40660510 | FULL | Memory buffer |
| SCB6_EZ_DATA69 | 0x40660514 | FULL | Memory buffer |
| SCB6_EZ_DATA70 | 0x40660518 | FULL | Memory buffer |
| SCB6_EZ_DATA71 | 0x4066051C | FULL | Memory buffer |
| SCB6_EZ_DATA72 | 0x40660520 | FULL | Memory buffer |
| SCB6_EZ_DATA73 | 0x40660524 | FULL | Memory buffer |
| SCB6_EZ_DATA74 | 0x40660528 | FULL | Memory buffer |
| SCB6_EZ_DATA75 | 0x4066052C | FULL | Memory buffer |
| SCB6_EZ_DATA76 | 0x40660530 | FULL | Memory buffer |
| SCB6_EZ_DATA77 | 0x40660534 | FULL | Memory buffer |
| SCB6_EZ_DATA78 | 0x40660538 | FULL | Memory buffer |
| SCB6_EZ_DATA79 | 0x4066053C | FULL | Memory buffer |
| SCB6_EZ_DATA80 | 0x40660540 | FULL | Memory buffer |
| SCB6_EZ_DATA81 | 0x40660544 | FULL | Memory buffer |
| SCB6_EZ_DATA82 | 0x40660548 | FULL | Memory buffer |
| SCB6_EZ_DATA83 | 0x4066054C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB6_EZ_DATA84 | 0x40660550 | FULL | Memory buffer |
| SCB6_EZ_DATA85 | 0x40660554 | FULL | Memory buffer |
| SCB6_EZ_DATA86 | 0x40660558 | FULL | Memory buffer |
| SCB6_EZ_DATA87 | 0x4066055C | FULL | Memory buffer |
| SCB6_EZ_DATA88 | 0x40660560 | FULL | Memory buffer |
| SCB6_EZ_DATA89 | 0x40660564 | FULL | Memory buffer |
| SCB6_EZ_DATA90 | 0x40660568 | FULL | Memory buffer |
| SCB6_EZ_DATA91 | 0x4066056C | FULL | Memory buffer |
| SCB6_EZ_DATA92 | 0x40660570 | FULL | Memory buffer |
| SCB6_EZ_DATA93 | 0x40660574 | FULL | Memory buffer |
| SCB6_EZ_DATA94 | 0x40660578 | FULL | Memory buffer |
| SCB6_EZ_DATA95 | 0x4066057C | FULL | Memory buffer |
| SCB6_EZ_DATA96 | 0x40660580 | FULL | Memory buffer |
| SCB6_EZ_DATA97 | 0x40660584 | FULL | Memory buffer |
| SCB6_EZ_DATA98 | 0x40660588 | FULL | Memory buffer |
| SCB6_EZ_DATA99 | 0x4066058C | FULL | Memory buffer |
| SCB6_EZ_DATA100 | 0x40660590 | FULL | Memory buffer |
| SCB6_EZ_DATA101 | 0x40660594 | FULL | Memory buffer |
| SCB6_EZ_DATA102 | 0x40660598 | FULL | Memory buffer |
| SCB6_EZ_DATA103 | 0x4066059C | FULL | Memory buffer |
| SCB6_EZ_DATA104 | 0x406605A0 | FULL | Memory buffer |
| SCB6_EZ_DATA105 | 0x406605A4 | FULL | Memory buffer |
| SCB6_EZ_DATA106 | 0x406605A8 | FULL | Memory buffer |
| SCB6_EZ_DATA107 | 0x406605AC | FULL | Memory buffer |
| SCB6_EZ_DATA108 | 0x406605B0 | FULL | Memory buffer |
| SCB6_EZ_DATA109 | 0x406605B4 | FULL | Memory buffer |
| SCB6_EZ_DATA110 | 0x406605B8 | FULL | Memory buffer |
| SCB6_EZ_DATA111 | 0x406605BC | FULL | Memory buffer |
| SCB6_EZ_DATA112 | 0x406605C0 | FULL | Memory buffer |
| SCB6_EZ_DATA113 | 0x406605C4 | FULL | Memory buffer |
| SCB6_EZ_DATA114 | 0x406605C8 | FULL | Memory buffer |
| SCB6_EZ_DATA115 | 0x406605CC | FULL | Memory buffer |
| SCB6_EZ_DATA116 | 0x406605D0 | FULL | Memory buffer |
| SCB6_EZ_DATA117 | 0x406605D4 | FULL | Memory buffer |
| SCB6_EZ_DATA118 | 0x406605D8 | FULL | Memory buffer |
| SCB6_EZ_DATA119 | 0x406605DC | FULL | Memory buffer |
| SCB6_EZ_DATA120 | 0x406605E0 | FULL | Memory buffer |
| SCB6_EZ_DATA121 | 0x406605E4 | FULL | Memory buffer |
| SCB6_EZ_DATA122 | 0x406605E8 | FULL | Memory buffer |
| SCB6_EZ_DATA123 | 0x406605EC | FULL | Memory buffer |
| SCB6_EZ_DATA124 | 0x406605F0 | FULL | Memory buffer |
| SCB6_EZ_DATA125 | 0x406605F4 | FULL | Memory buffer |
| SCB6_EZ_DATA126 | 0x406605F8 | FULL | Memory buffer |
| SCB6_EZ_DATA127 | 0x406605FC | FULL | Memory buffer |
| SCB6_EZ_DATA128 | 0x40660600 | FULL | Memory buffer |
| SCB6_EZ_DATA129 | 0x40660604 | FULL | Memory buffer |
| SCB6_EZ_DATA130 | 0x40660608 | FULL | Memory buffer |
| SCB6_EZ_DATA131 | 0x4066060C | FULL | Memory buffer |
| SCB6_EZ_DATA132 | 0x40660610 | FULL | Memory buffer |
| SCB6_EZ_DATA133 | 0x40660614 | FULL | Memory buffer |
| SCB6_EZ_DATA134 | 0x40660618 | FULL | Memory buffer |
| SCB6_EZ_DATA135 | 0x4066061C | FULL | Memory buffer |
| SCB6_EZ_DATA136 | 0x40660620 | FULL | Memory buffer |
| SCB6_EZ_DATA137 | 0x40660624 | FULL | Memory buffer |
| SCB6_EZ_DATA138 | 0x40660628 | FULL | Memory buffer |
| SCB6_EZ_DATA139 | 0x4066062C | FULL | Memory buffer |
| SCB6_EZ_DATA140 | 0x40660630 | FULL | Memory buffer |
| SCB6_EZ_DATA141 | 0x40660634 | FULL | Memory buffer |
| SCB6_EZ_DATA142 | 0x40660638 | FULL | Memory buffer |
| SCB6_EZ_DATA143 | 0x4066063C | FULL | Memory buffer |
| SCB6_EZ_DATA144 | 0x40660640 | FULL | Memory buffer |
| SCB6_EZ_DATA145 | 0x40660644 | FULL | Memory buffer |
| SCB6_EZ_DATA146 | 0x40660648 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB6_EZ_DATA147 | 0x4066064C | FULL | Memory buffer |
| SCB6_EZ_DATA148 | 0x40660650 | FULL | Memory buffer |
| SCB6_EZ_DATA149 | 0x40660654 | FULL | Memory buffer |
| SCB6_EZ_DATA150 | 0x40660658 | FULL | Memory buffer |
| SCB6_EZ_DATA151 | 0x4066065C | FULL | Memory buffer |
| SCB6_EZ_DATA152 | 0x40660660 | FULL | Memory buffer |
| SCB6_EZ_DATA153 | 0x40660664 | FULL | Memory buffer |
| SCB6_EZ_DATA154 | 0x40660668 | FULL | Memory buffer |
| SCB6_EZ_DATA155 | 0x4066066C | FULL | Memory buffer |
| SCB6_EZ_DATA156 | 0x40660670 | FULL | Memory buffer |
| SCB6_EZ_DATA157 | 0x40660674 | FULL | Memory buffer |
| SCB6_EZ_DATA158 | 0x40660678 | FULL | Memory buffer |
| SCB6_EZ_DATA159 | 0x4066067C | FULL | Memory buffer |
| SCB6_EZ_DATA160 | 0x40660680 | FULL | Memory buffer |
| SCB6_EZ_DATA161 | 0x40660684 | FULL | Memory buffer |
| SCB6_EZ_DATA162 | 0x40660688 | FULL | Memory buffer |
| SCB6_EZ_DATA163 | 0x4066068C | FULL | Memory buffer |
| SCB6_EZ_DATA164 | 0x40660690 | FULL | Memory buffer |
| SCB6_EZ_DATA165 | 0x40660694 | FULL | Memory buffer |
| SCB6_EZ_DATA166 | 0x40660698 | FULL | Memory buffer |
| SCB6_EZ_DATA167 | 0x4066069C | FULL | Memory buffer |
| SCB6_EZ_DATA168 | 0x406606A0 | FULL | Memory buffer |
| SCB6_EZ_DATA169 | 0x406606A4 | FULL | Memory buffer |
| SCB6_EZ_DATA170 | 0x406606A8 | FULL | Memory buffer |
| SCB6_EZ_DATA171 | 0x406606AC | FULL | Memory buffer |
| SCB6_EZ_DATA172 | 0x406606B0 | FULL | Memory buffer |
| SCB6_EZ_DATA173 | 0x406606B4 | FULL | Memory buffer |
| SCB6_EZ_DATA174 | 0x406606B8 | FULL | Memory buffer |
| SCB6_EZ_DATA175 | 0x406606BC | FULL | Memory buffer |
| SCB6_EZ_DATA176 | 0x406606C0 | FULL | Memory buffer |
| SCB6_EZ_DATA177 | 0x406606C4 | FULL | Memory buffer |
| SCB6_EZ_DATA178 | 0x406606C8 | FULL | Memory buffer |
| SCB6_EZ_DATA179 | 0x406606CC | FULL | Memory buffer |
| SCB6_EZ_DATA180 | 0x406606D0 | FULL | Memory buffer |
| SCB6_EZ_DATA181 | 0x406606D4 | FULL | Memory buffer |
| SCB6_EZ_DATA182 | 0x406606D8 | FULL | Memory buffer |
| SCB6_EZ_DATA183 | 0x406606DC | FULL | Memory buffer |
| SCB6_EZ_DATA184 | 0x406606E0 | FULL | Memory buffer |
| SCB6_EZ_DATA185 | 0x406606E4 | FULL | Memory buffer |
| SCB6_EZ_DATA186 | 0x406606E8 | FULL | Memory buffer |
| SCB6_EZ_DATA187 | 0x406606EC | FULL | Memory buffer |
| SCB6_EZ_DATA188 | 0x406606F0 | FULL | Memory buffer |
| SCB6_EZ_DATA189 | 0x406606F4 | FULL | Memory buffer |
| SCB6_EZ_DATA190 | 0x406606F8 | FULL | Memory buffer |
| SCB6_EZ_DATA191 | 0x406606FC | FULL | Memory buffer |
| SCB6_EZ_DATA192 | 0x40660700 | FULL | Memory buffer |
| SCB6_EZ_DATA193 | 0x40660704 | FULL | Memory buffer |
| SCB6_EZ_DATA194 | 0x40660708 | FULL | Memory buffer |
| SCB6_EZ_DATA195 | 0x4066070C | FULL | Memory buffer |
| SCB6_EZ_DATA196 | 0x40660710 | FULL | Memory buffer |
| SCB6_EZ_DATA197 | 0x40660714 | FULL | Memory buffer |
| SCB6_EZ_DATA198 | 0x40660718 | FULL | Memory buffer |
| SCB6_EZ_DATA199 | 0x4066071C | FULL | Memory buffer |
| SCB6_EZ_DATA200 | 0x40660720 | FULL | Memory buffer |
| SCB6_EZ_DATA201 | 0x40660724 | FULL | Memory buffer |
| SCB6_EZ_DATA202 | 0x40660728 | FULL | Memory buffer |
| SCB6_EZ_DATA203 | 0x4066072C | FULL | Memory buffer |
| SCB6_EZ_DATA204 | 0x40660730 | FULL | Memory buffer |
| SCB6_EZ_DATA205 | 0x40660734 | FULL | Memory buffer |
| SCB6_EZ_DATA206 | 0x40660738 | FULL | Memory buffer |
| SCB6_EZ_DATA207 | 0x4066073C | FULL | Memory buffer |
| SCB6_EZ_DATA208 | 0x40660740 | FULL | Memory buffer |
| SCB6_EZ_DATA209 | 0x40660744 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB6_EZ_DATA210 | 0x40660748 | FULL | Memory buffer |
| SCB6_EZ_DATA211 | 0x4066074C | FULL | Memory buffer |
| SCB6_EZ_DATA212 | 0x40660750 | FULL | Memory buffer |
| SCB6_EZ_DATA213 | 0x40660754 | FULL | Memory buffer |
| SCB6_EZ_DATA214 | 0x40660758 | FULL | Memory buffer |
| SCB6_EZ_DATA215 | 0x4066075C | FULL | Memory buffer |
| SCB6_EZ_DATA216 | 0x40660760 | FULL | Memory buffer |
| SCB6_EZ_DATA217 | 0x40660764 | FULL | Memory buffer |
| SCB6_EZ_DATA218 | 0x40660768 | FULL | Memory buffer |
| SCB6_EZ_DATA219 | 0x4066076C | FULL | Memory buffer |
| SCB6_EZ_DATA220 | 0x40660770 | FULL | Memory buffer |
| SCB6_EZ_DATA221 | 0x40660774 | FULL | Memory buffer |
| SCB6_EZ_DATA222 | 0x40660778 | FULL | Memory buffer |
| SCB6_EZ_DATA223 | 0x4066077C | FULL | Memory buffer |
| SCB6_EZ_DATA224 | 0x40660780 | FULL | Memory buffer |
| SCB6_EZ_DATA225 | 0x40660784 | FULL | Memory buffer |
| SCB6_EZ_DATA226 | 0x40660788 | FULL | Memory buffer |
| SCB6_EZ_DATA227 | 0x4066078C | FULL | Memory buffer |
| SCB6_EZ_DATA228 | 0x40660790 | FULL | Memory buffer |
| SCB6_EZ_DATA229 | 0x40660794 | FULL | Memory buffer |
| SCB6_EZ_DATA230 | 0x40660798 | FULL | Memory buffer |
| SCB6_EZ_DATA231 | 0x4066079C | FULL | Memory buffer |
| SCB6_EZ_DATA232 | 0x406607A0 | FULL | Memory buffer |
| SCB6_EZ_DATA233 | 0x406607A4 | FULL | Memory buffer |
| SCB6_EZ_DATA234 | 0x406607A8 | FULL | Memory buffer |
| SCB6_EZ_DATA235 | 0x406607AC | FULL | Memory buffer |
| SCB6_EZ_DATA236 | 0x406607B0 | FULL | Memory buffer |
| SCB6_EZ_DATA237 | 0x406607B4 | FULL | Memory buffer |
| SCB6_EZ_DATA238 | 0x406607B8 | FULL | Memory buffer |
| SCB6_EZ_DATA239 | 0x406607BC | FULL | Memory buffer |
| SCB6_EZ_DATA240 | 0x406607C0 | FULL | Memory buffer |
| SCB6_EZ_DATA241 | 0x406607C4 | FULL | Memory buffer |
| SCB6_EZ_DATA242 | 0x406607C8 | FULL | Memory buffer |
| SCB6_EZ_DATA243 | 0x406607CC | FULL | Memory buffer |
| SCB6_EZ_DATA244 | 0x406607D0 | FULL | Memory buffer |
| SCB6_EZ_DATA245 | 0x406607D4 | FULL | Memory buffer |
| SCB6_EZ_DATA246 | 0x406607D8 | FULL | Memory buffer |
| SCB6_EZ_DATA247 | 0x406607DC | FULL | Memory buffer |
| SCB6_EZ_DATA248 | 0x406607E0 | FULL | Memory buffer |
| SCB6_EZ_DATA249 | 0x406607E4 | FULL | Memory buffer |
| SCB6_EZ_DATA250 | 0x406607E8 | FULL | Memory buffer |
| SCB6_EZ_DATA251 | 0x406607EC | FULL | Memory buffer |
| SCB6_EZ_DATA252 | 0x406607F0 | FULL | Memory buffer |
| SCB6_EZ_DATA253 | 0x406607F4 | FULL | Memory buffer |
| SCB6_EZ_DATA254 | 0x406607F8 | FULL | Memory buffer |
| SCB6_EZ_DATA255 | 0x406607FC | FULL | Memory buffer |
| SCB6_INTR_CAUSE | 0x40660E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB6_INTR_SPI_EC | 0x40660EC0 | FULL | Externally clocked SPI interrupt request |
| SCB6_INTR_SPI_EC_MASK | 0x40660EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB6_INTR_SPI_EC_MASKED | 0x40660ECC | FULL | Externally clocked SPI interrupt masked |
| SCB6_INTR_M | 0x40660F00 | FULL | Master interrupt request |
| SCB6_INTR_M_SET | 0x40660F04 | FULL | Master interrupt set request |
| SCB6_INTR_M_MASK | 0x40660F08 | FULL | Master interrupt mask |
| SCB6_INTR_M_MASKED | 0x40660F0C | FULL | Master interrupt masked request |
| SCB6_INTR_S | 0x40660F40 | FULL | Slave interrupt request |
| SCB6_INTR_S_SET | 0x40660F44 | FULL | Slave interrupt set request |
| SCB6_INTR_S_MASK | 0x40660F48 | FULL | Slave interrupt mask |
| SCB6_INTR_S_MASKED | 0x40660F4C | FULL | Slave interrupt masked request |
| SCB6_INTR_TX | 0x40660F80 | FULL | Transmitter interrupt request |
| SCB6_INTR_TX_SET | 0x40660F84 | FULL | Transmitter interrupt set request |
| SCB6_INTR_TX_MASK | 0x40660F88 | FULL | Transmitter interrupt mask |
| SCB6_INTR_TX_MASKED | 0x40660F8C | FULL | Transmitter interrupt masked request |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|-----------------------------------|
| SCB6_INTR_RX | 0x40660FC0 | FULL | Receiver interrupt request |
| SCB6_INTR_RX_SET | 0x40660FC4 | FULL | Receiver interrupt set request |
| SCB6_INTR_RX_MASK | 0x40660FC8 | FULL | Receiver interrupt mask |
| SCB6_INTR_RX_MASKED | 0x40660FCC | FULL | Receiver interrupt masked request |

23.8 SCB 7

Description Serial Communications Block
(SPI/UART/I2C)

Base Address 0x40670000

Size 0x10000

Slave Num MMIO6 - 7

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--|
| SCB7_CTRL | 0x40670000 | FULL | Generic control <i>Note: CMD_RESP_MODE is not available for this register</i> |
| SCB7_STATUS | 0x40670004 | FULL | Generic status |
| SCB7_SPI_CTRL | 0x40670020 | FULL | SPI control |
| SCB7_SPI_STATUS | 0x40670024 | FULL | SPI status |
| SCB7_SPI_TX_CTRL | 0x40670028 | FULL | SPI transmitter control |
| SCB7_SPI_RX_CTRL | 0x4067002C | FULL | SPI receiver control |
| SCB7_UART_CTRL | 0x40670040 | FULL | UART control |
| SCB7_UART_TX_CTRL | 0x40670044 | FULL | UART transmitter control |
| SCB7_UART_RX_CTRL | 0x40670048 | FULL | UART receiver control |
| SCB7_UART_RX_STATUS | 0x4067004C | FULL | UART receiver status |
| SCB7_UART_FLOW_CTRL | 0x40670050 | FULL | UART flow control |
| SCB7_I2C_CTRL | 0x40670060 | FULL | I2C control |
| SCB7_I2C_STATUS | 0x40670064 | FULL | I2C status <i>Note: I2C_EC_BUSY is not available for this register</i> |
| SCB7_I2C_M_CMD | 0x40670068 | FULL | I2C master command |
| SCB7_I2C_S_CMD | 0x4067006C | FULL | I2C slave command |
| SCB7_I2C_CFG | 0x40670070 | FULL | I2C configuration |
| SCB7_TX_CTRL | 0x40670200 | FULL | Transmitter control |
| SCB7_TX_FIFO_CTRL | 0x40670204 | FULL | Transmitter FIFO control |
| SCB7_TX_FIFO_STATUS | 0x40670208 | FULL | Transmitter FIFO status |
| SCB7_TX_FIFO_WR | 0x40670240 | FULL | Transmitter FIFO write |
| SCB7_RX_CTRL | 0x40670300 | FULL | Receiver control |
| SCB7_RX_FIFO_CTRL | 0x40670304 | FULL | Receiver FIFO control |
| SCB7_RX_FIFO_STATUS | 0x40670308 | FULL | Receiver FIFO status |
| SCB7_RX_MATCH | 0x40670310 | FULL | Slave address and mask |
| SCB7_RX_FIFO_RD | 0x40670340 | FULL | Receiver FIFO read |
| SCB7_RX_FIFO_RD_SILENT | 0x40670344 | FULL | Receiver FIFO read silent |
| SCB7_EZ_DATA0 | 0x40670400 | FULL | Memory buffer |
| SCB7_EZ_DATA1 | 0x40670404 | FULL | Memory buffer |
| SCB7_EZ_DATA2 | 0x40670408 | FULL | Memory buffer |
| SCB7_EZ_DATA3 | 0x4067040C | FULL | Memory buffer |
| SCB7_EZ_DATA4 | 0x40670410 | FULL | Memory buffer |
| SCB7_EZ_DATA5 | 0x40670414 | FULL | Memory buffer |
| SCB7_EZ_DATA6 | 0x40670418 | FULL | Memory buffer |
| SCB7_EZ_DATA7 | 0x4067041C | FULL | Memory buffer |
| SCB7_EZ_DATA8 | 0x40670420 | FULL | Memory buffer |
| SCB7_EZ_DATA9 | 0x40670424 | FULL | Memory buffer |
| SCB7_EZ_DATA10 | 0x40670428 | FULL | Memory buffer |
| SCB7_EZ_DATA11 | 0x4067042C | FULL | Memory buffer |
| SCB7_EZ_DATA12 | 0x40670430 | FULL | Memory buffer |
| SCB7_EZ_DATA13 | 0x40670434 | FULL | Memory buffer |
| SCB7_EZ_DATA14 | 0x40670438 | FULL | Memory buffer |
| SCB7_EZ_DATA15 | 0x4067043C | FULL | Memory buffer |
| SCB7_EZ_DATA16 | 0x40670440 | FULL | Memory buffer |
| SCB7_EZ_DATA17 | 0x40670444 | FULL | Memory buffer |
| SCB7_EZ_DATA18 | 0x40670448 | FULL | Memory buffer |
| SCB7_EZ_DATA19 | 0x4067044C | FULL | Memory buffer |
| SCB7_EZ_DATA20 | 0x40670450 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|----------------|------------|------------|---------------|
| SCB7_EZ_DATA21 | 0x40670454 | FULL | Memory buffer |
| SCB7_EZ_DATA22 | 0x40670458 | FULL | Memory buffer |
| SCB7_EZ_DATA23 | 0x4067045C | FULL | Memory buffer |
| SCB7_EZ_DATA24 | 0x40670460 | FULL | Memory buffer |
| SCB7_EZ_DATA25 | 0x40670464 | FULL | Memory buffer |
| SCB7_EZ_DATA26 | 0x40670468 | FULL | Memory buffer |
| SCB7_EZ_DATA27 | 0x4067046C | FULL | Memory buffer |
| SCB7_EZ_DATA28 | 0x40670470 | FULL | Memory buffer |
| SCB7_EZ_DATA29 | 0x40670474 | FULL | Memory buffer |
| SCB7_EZ_DATA30 | 0x40670478 | FULL | Memory buffer |
| SCB7_EZ_DATA31 | 0x4067047C | FULL | Memory buffer |
| SCB7_EZ_DATA32 | 0x40670480 | FULL | Memory buffer |
| SCB7_EZ_DATA33 | 0x40670484 | FULL | Memory buffer |
| SCB7_EZ_DATA34 | 0x40670488 | FULL | Memory buffer |
| SCB7_EZ_DATA35 | 0x4067048C | FULL | Memory buffer |
| SCB7_EZ_DATA36 | 0x40670490 | FULL | Memory buffer |
| SCB7_EZ_DATA37 | 0x40670494 | FULL | Memory buffer |
| SCB7_EZ_DATA38 | 0x40670498 | FULL | Memory buffer |
| SCB7_EZ_DATA39 | 0x4067049C | FULL | Memory buffer |
| SCB7_EZ_DATA40 | 0x406704A0 | FULL | Memory buffer |
| SCB7_EZ_DATA41 | 0x406704A4 | FULL | Memory buffer |
| SCB7_EZ_DATA42 | 0x406704A8 | FULL | Memory buffer |
| SCB7_EZ_DATA43 | 0x406704AC | FULL | Memory buffer |
| SCB7_EZ_DATA44 | 0x406704B0 | FULL | Memory buffer |
| SCB7_EZ_DATA45 | 0x406704B4 | FULL | Memory buffer |
| SCB7_EZ_DATA46 | 0x406704B8 | FULL | Memory buffer |
| SCB7_EZ_DATA47 | 0x406704BC | FULL | Memory buffer |
| SCB7_EZ_DATA48 | 0x406704C0 | FULL | Memory buffer |
| SCB7_EZ_DATA49 | 0x406704C4 | FULL | Memory buffer |
| SCB7_EZ_DATA50 | 0x406704C8 | FULL | Memory buffer |
| SCB7_EZ_DATA51 | 0x406704CC | FULL | Memory buffer |
| SCB7_EZ_DATA52 | 0x406704D0 | FULL | Memory buffer |
| SCB7_EZ_DATA53 | 0x406704D4 | FULL | Memory buffer |
| SCB7_EZ_DATA54 | 0x406704D8 | FULL | Memory buffer |
| SCB7_EZ_DATA55 | 0x406704DC | FULL | Memory buffer |
| SCB7_EZ_DATA56 | 0x406704E0 | FULL | Memory buffer |
| SCB7_EZ_DATA57 | 0x406704E4 | FULL | Memory buffer |
| SCB7_EZ_DATA58 | 0x406704E8 | FULL | Memory buffer |
| SCB7_EZ_DATA59 | 0x406704EC | FULL | Memory buffer |
| SCB7_EZ_DATA60 | 0x406704F0 | FULL | Memory buffer |
| SCB7_EZ_DATA61 | 0x406704F4 | FULL | Memory buffer |
| SCB7_EZ_DATA62 | 0x406704F8 | FULL | Memory buffer |
| SCB7_EZ_DATA63 | 0x406704FC | FULL | Memory buffer |
| SCB7_EZ_DATA64 | 0x40670500 | FULL | Memory buffer |
| SCB7_EZ_DATA65 | 0x40670504 | FULL | Memory buffer |
| SCB7_EZ_DATA66 | 0x40670508 | FULL | Memory buffer |
| SCB7_EZ_DATA67 | 0x4067050C | FULL | Memory buffer |
| SCB7_EZ_DATA68 | 0x40670510 | FULL | Memory buffer |
| SCB7_EZ_DATA69 | 0x40670514 | FULL | Memory buffer |
| SCB7_EZ_DATA70 | 0x40670518 | FULL | Memory buffer |
| SCB7_EZ_DATA71 | 0x4067051C | FULL | Memory buffer |
| SCB7_EZ_DATA72 | 0x40670520 | FULL | Memory buffer |
| SCB7_EZ_DATA73 | 0x40670524 | FULL | Memory buffer |
| SCB7_EZ_DATA74 | 0x40670528 | FULL | Memory buffer |
| SCB7_EZ_DATA75 | 0x4067052C | FULL | Memory buffer |
| SCB7_EZ_DATA76 | 0x40670530 | FULL | Memory buffer |
| SCB7_EZ_DATA77 | 0x40670534 | FULL | Memory buffer |
| SCB7_EZ_DATA78 | 0x40670538 | FULL | Memory buffer |
| SCB7_EZ_DATA79 | 0x4067053C | FULL | Memory buffer |
| SCB7_EZ_DATA80 | 0x40670540 | FULL | Memory buffer |
| SCB7_EZ_DATA81 | 0x40670544 | FULL | Memory buffer |
| SCB7_EZ_DATA82 | 0x40670548 | FULL | Memory buffer |
| SCB7_EZ_DATA83 | 0x4067054C | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB7_EZ_DATA84 | 0x40670550 | FULL | Memory buffer |
| SCB7_EZ_DATA85 | 0x40670554 | FULL | Memory buffer |
| SCB7_EZ_DATA86 | 0x40670558 | FULL | Memory buffer |
| SCB7_EZ_DATA87 | 0x4067055C | FULL | Memory buffer |
| SCB7_EZ_DATA88 | 0x40670560 | FULL | Memory buffer |
| SCB7_EZ_DATA89 | 0x40670564 | FULL | Memory buffer |
| SCB7_EZ_DATA90 | 0x40670568 | FULL | Memory buffer |
| SCB7_EZ_DATA91 | 0x4067056C | FULL | Memory buffer |
| SCB7_EZ_DATA92 | 0x40670570 | FULL | Memory buffer |
| SCB7_EZ_DATA93 | 0x40670574 | FULL | Memory buffer |
| SCB7_EZ_DATA94 | 0x40670578 | FULL | Memory buffer |
| SCB7_EZ_DATA95 | 0x4067057C | FULL | Memory buffer |
| SCB7_EZ_DATA96 | 0x40670580 | FULL | Memory buffer |
| SCB7_EZ_DATA97 | 0x40670584 | FULL | Memory buffer |
| SCB7_EZ_DATA98 | 0x40670588 | FULL | Memory buffer |
| SCB7_EZ_DATA99 | 0x4067058C | FULL | Memory buffer |
| SCB7_EZ_DATA100 | 0x40670590 | FULL | Memory buffer |
| SCB7_EZ_DATA101 | 0x40670594 | FULL | Memory buffer |
| SCB7_EZ_DATA102 | 0x40670598 | FULL | Memory buffer |
| SCB7_EZ_DATA103 | 0x4067059C | FULL | Memory buffer |
| SCB7_EZ_DATA104 | 0x406705A0 | FULL | Memory buffer |
| SCB7_EZ_DATA105 | 0x406705A4 | FULL | Memory buffer |
| SCB7_EZ_DATA106 | 0x406705A8 | FULL | Memory buffer |
| SCB7_EZ_DATA107 | 0x406705AC | FULL | Memory buffer |
| SCB7_EZ_DATA108 | 0x406705B0 | FULL | Memory buffer |
| SCB7_EZ_DATA109 | 0x406705B4 | FULL | Memory buffer |
| SCB7_EZ_DATA110 | 0x406705B8 | FULL | Memory buffer |
| SCB7_EZ_DATA111 | 0x406705BC | FULL | Memory buffer |
| SCB7_EZ_DATA112 | 0x406705C0 | FULL | Memory buffer |
| SCB7_EZ_DATA113 | 0x406705C4 | FULL | Memory buffer |
| SCB7_EZ_DATA114 | 0x406705C8 | FULL | Memory buffer |
| SCB7_EZ_DATA115 | 0x406705CC | FULL | Memory buffer |
| SCB7_EZ_DATA116 | 0x406705D0 | FULL | Memory buffer |
| SCB7_EZ_DATA117 | 0x406705D4 | FULL | Memory buffer |
| SCB7_EZ_DATA118 | 0x406705D8 | FULL | Memory buffer |
| SCB7_EZ_DATA119 | 0x406705DC | FULL | Memory buffer |
| SCB7_EZ_DATA120 | 0x406705E0 | FULL | Memory buffer |
| SCB7_EZ_DATA121 | 0x406705E4 | FULL | Memory buffer |
| SCB7_EZ_DATA122 | 0x406705E8 | FULL | Memory buffer |
| SCB7_EZ_DATA123 | 0x406705EC | FULL | Memory buffer |
| SCB7_EZ_DATA124 | 0x406705F0 | FULL | Memory buffer |
| SCB7_EZ_DATA125 | 0x406705F4 | FULL | Memory buffer |
| SCB7_EZ_DATA126 | 0x406705F8 | FULL | Memory buffer |
| SCB7_EZ_DATA127 | 0x406705FC | FULL | Memory buffer |
| SCB7_EZ_DATA128 | 0x40670600 | FULL | Memory buffer |
| SCB7_EZ_DATA129 | 0x40670604 | FULL | Memory buffer |
| SCB7_EZ_DATA130 | 0x40670608 | FULL | Memory buffer |
| SCB7_EZ_DATA131 | 0x4067060C | FULL | Memory buffer |
| SCB7_EZ_DATA132 | 0x40670610 | FULL | Memory buffer |
| SCB7_EZ_DATA133 | 0x40670614 | FULL | Memory buffer |
| SCB7_EZ_DATA134 | 0x40670618 | FULL | Memory buffer |
| SCB7_EZ_DATA135 | 0x4067061C | FULL | Memory buffer |
| SCB7_EZ_DATA136 | 0x40670620 | FULL | Memory buffer |
| SCB7_EZ_DATA137 | 0x40670624 | FULL | Memory buffer |
| SCB7_EZ_DATA138 | 0x40670628 | FULL | Memory buffer |
| SCB7_EZ_DATA139 | 0x4067062C | FULL | Memory buffer |
| SCB7_EZ_DATA140 | 0x40670630 | FULL | Memory buffer |
| SCB7_EZ_DATA141 | 0x40670634 | FULL | Memory buffer |
| SCB7_EZ_DATA142 | 0x40670638 | FULL | Memory buffer |
| SCB7_EZ_DATA143 | 0x4067063C | FULL | Memory buffer |
| SCB7_EZ_DATA144 | 0x40670640 | FULL | Memory buffer |
| SCB7_EZ_DATA145 | 0x40670644 | FULL | Memory buffer |
| SCB7_EZ_DATA146 | 0x40670648 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|---------------|
| SCB7_EZ_DATA147 | 0x4067064C | FULL | Memory buffer |
| SCB7_EZ_DATA148 | 0x40670650 | FULL | Memory buffer |
| SCB7_EZ_DATA149 | 0x40670654 | FULL | Memory buffer |
| SCB7_EZ_DATA150 | 0x40670658 | FULL | Memory buffer |
| SCB7_EZ_DATA151 | 0x4067065C | FULL | Memory buffer |
| SCB7_EZ_DATA152 | 0x40670660 | FULL | Memory buffer |
| SCB7_EZ_DATA153 | 0x40670664 | FULL | Memory buffer |
| SCB7_EZ_DATA154 | 0x40670668 | FULL | Memory buffer |
| SCB7_EZ_DATA155 | 0x4067066C | FULL | Memory buffer |
| SCB7_EZ_DATA156 | 0x40670670 | FULL | Memory buffer |
| SCB7_EZ_DATA157 | 0x40670674 | FULL | Memory buffer |
| SCB7_EZ_DATA158 | 0x40670678 | FULL | Memory buffer |
| SCB7_EZ_DATA159 | 0x4067067C | FULL | Memory buffer |
| SCB7_EZ_DATA160 | 0x40670680 | FULL | Memory buffer |
| SCB7_EZ_DATA161 | 0x40670684 | FULL | Memory buffer |
| SCB7_EZ_DATA162 | 0x40670688 | FULL | Memory buffer |
| SCB7_EZ_DATA163 | 0x4067068C | FULL | Memory buffer |
| SCB7_EZ_DATA164 | 0x40670690 | FULL | Memory buffer |
| SCB7_EZ_DATA165 | 0x40670694 | FULL | Memory buffer |
| SCB7_EZ_DATA166 | 0x40670698 | FULL | Memory buffer |
| SCB7_EZ_DATA167 | 0x4067069C | FULL | Memory buffer |
| SCB7_EZ_DATA168 | 0x406706A0 | FULL | Memory buffer |
| SCB7_EZ_DATA169 | 0x406706A4 | FULL | Memory buffer |
| SCB7_EZ_DATA170 | 0x406706A8 | FULL | Memory buffer |
| SCB7_EZ_DATA171 | 0x406706AC | FULL | Memory buffer |
| SCB7_EZ_DATA172 | 0x406706B0 | FULL | Memory buffer |
| SCB7_EZ_DATA173 | 0x406706B4 | FULL | Memory buffer |
| SCB7_EZ_DATA174 | 0x406706B8 | FULL | Memory buffer |
| SCB7_EZ_DATA175 | 0x406706BC | FULL | Memory buffer |
| SCB7_EZ_DATA176 | 0x406706C0 | FULL | Memory buffer |
| SCB7_EZ_DATA177 | 0x406706C4 | FULL | Memory buffer |
| SCB7_EZ_DATA178 | 0x406706C8 | FULL | Memory buffer |
| SCB7_EZ_DATA179 | 0x406706CC | FULL | Memory buffer |
| SCB7_EZ_DATA180 | 0x406706D0 | FULL | Memory buffer |
| SCB7_EZ_DATA181 | 0x406706D4 | FULL | Memory buffer |
| SCB7_EZ_DATA182 | 0x406706D8 | FULL | Memory buffer |
| SCB7_EZ_DATA183 | 0x406706DC | FULL | Memory buffer |
| SCB7_EZ_DATA184 | 0x406706E0 | FULL | Memory buffer |
| SCB7_EZ_DATA185 | 0x406706E4 | FULL | Memory buffer |
| SCB7_EZ_DATA186 | 0x406706E8 | FULL | Memory buffer |
| SCB7_EZ_DATA187 | 0x406706EC | FULL | Memory buffer |
| SCB7_EZ_DATA188 | 0x406706F0 | FULL | Memory buffer |
| SCB7_EZ_DATA189 | 0x406706F4 | FULL | Memory buffer |
| SCB7_EZ_DATA190 | 0x406706F8 | FULL | Memory buffer |
| SCB7_EZ_DATA191 | 0x406706FC | FULL | Memory buffer |
| SCB7_EZ_DATA192 | 0x40670700 | FULL | Memory buffer |
| SCB7_EZ_DATA193 | 0x40670704 | FULL | Memory buffer |
| SCB7_EZ_DATA194 | 0x40670708 | FULL | Memory buffer |
| SCB7_EZ_DATA195 | 0x4067070C | FULL | Memory buffer |
| SCB7_EZ_DATA196 | 0x40670710 | FULL | Memory buffer |
| SCB7_EZ_DATA197 | 0x40670714 | FULL | Memory buffer |
| SCB7_EZ_DATA198 | 0x40670718 | FULL | Memory buffer |
| SCB7_EZ_DATA199 | 0x4067071C | FULL | Memory buffer |
| SCB7_EZ_DATA200 | 0x40670720 | FULL | Memory buffer |
| SCB7_EZ_DATA201 | 0x40670724 | FULL | Memory buffer |
| SCB7_EZ_DATA202 | 0x40670728 | FULL | Memory buffer |
| SCB7_EZ_DATA203 | 0x4067072C | FULL | Memory buffer |
| SCB7_EZ_DATA204 | 0x40670730 | FULL | Memory buffer |
| SCB7_EZ_DATA205 | 0x40670734 | FULL | Memory buffer |
| SCB7_EZ_DATA206 | 0x40670738 | FULL | Memory buffer |
| SCB7_EZ_DATA207 | 0x4067073C | FULL | Memory buffer |
| SCB7_EZ_DATA208 | 0x40670740 | FULL | Memory buffer |
| SCB7_EZ_DATA209 | 0x40670744 | FULL | Memory buffer |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| SCB7_EZ_DATA210 | 0x40670748 | FULL | Memory buffer |
| SCB7_EZ_DATA211 | 0x4067074C | FULL | Memory buffer |
| SCB7_EZ_DATA212 | 0x40670750 | FULL | Memory buffer |
| SCB7_EZ_DATA213 | 0x40670754 | FULL | Memory buffer |
| SCB7_EZ_DATA214 | 0x40670758 | FULL | Memory buffer |
| SCB7_EZ_DATA215 | 0x4067075C | FULL | Memory buffer |
| SCB7_EZ_DATA216 | 0x40670760 | FULL | Memory buffer |
| SCB7_EZ_DATA217 | 0x40670764 | FULL | Memory buffer |
| SCB7_EZ_DATA218 | 0x40670768 | FULL | Memory buffer |
| SCB7_EZ_DATA219 | 0x4067076C | FULL | Memory buffer |
| SCB7_EZ_DATA220 | 0x40670770 | FULL | Memory buffer |
| SCB7_EZ_DATA221 | 0x40670774 | FULL | Memory buffer |
| SCB7_EZ_DATA222 | 0x40670778 | FULL | Memory buffer |
| SCB7_EZ_DATA223 | 0x4067077C | FULL | Memory buffer |
| SCB7_EZ_DATA224 | 0x40670780 | FULL | Memory buffer |
| SCB7_EZ_DATA225 | 0x40670784 | FULL | Memory buffer |
| SCB7_EZ_DATA226 | 0x40670788 | FULL | Memory buffer |
| SCB7_EZ_DATA227 | 0x4067078C | FULL | Memory buffer |
| SCB7_EZ_DATA228 | 0x40670790 | FULL | Memory buffer |
| SCB7_EZ_DATA229 | 0x40670794 | FULL | Memory buffer |
| SCB7_EZ_DATA230 | 0x40670798 | FULL | Memory buffer |
| SCB7_EZ_DATA231 | 0x4067079C | FULL | Memory buffer |
| SCB7_EZ_DATA232 | 0x406707A0 | FULL | Memory buffer |
| SCB7_EZ_DATA233 | 0x406707A4 | FULL | Memory buffer |
| SCB7_EZ_DATA234 | 0x406707A8 | FULL | Memory buffer |
| SCB7_EZ_DATA235 | 0x406707AC | FULL | Memory buffer |
| SCB7_EZ_DATA236 | 0x406707B0 | FULL | Memory buffer |
| SCB7_EZ_DATA237 | 0x406707B4 | FULL | Memory buffer |
| SCB7_EZ_DATA238 | 0x406707B8 | FULL | Memory buffer |
| SCB7_EZ_DATA239 | 0x406707BC | FULL | Memory buffer |
| SCB7_EZ_DATA240 | 0x406707C0 | FULL | Memory buffer |
| SCB7_EZ_DATA241 | 0x406707C4 | FULL | Memory buffer |
| SCB7_EZ_DATA242 | 0x406707C8 | FULL | Memory buffer |
| SCB7_EZ_DATA243 | 0x406707CC | FULL | Memory buffer |
| SCB7_EZ_DATA244 | 0x406707D0 | FULL | Memory buffer |
| SCB7_EZ_DATA245 | 0x406707D4 | FULL | Memory buffer |
| SCB7_EZ_DATA246 | 0x406707D8 | FULL | Memory buffer |
| SCB7_EZ_DATA247 | 0x406707DC | FULL | Memory buffer |
| SCB7_EZ_DATA248 | 0x406707E0 | FULL | Memory buffer |
| SCB7_EZ_DATA249 | 0x406707E4 | FULL | Memory buffer |
| SCB7_EZ_DATA250 | 0x406707E8 | FULL | Memory buffer |
| SCB7_EZ_DATA251 | 0x406707EC | FULL | Memory buffer |
| SCB7_EZ_DATA252 | 0x406707F0 | FULL | Memory buffer |
| SCB7_EZ_DATA253 | 0x406707F4 | FULL | Memory buffer |
| SCB7_EZ_DATA254 | 0x406707F8 | FULL | Memory buffer |
| SCB7_EZ_DATA255 | 0x406707FC | FULL | Memory buffer |
| SCB7_INTR_CAUSE | 0x40670E00 | FULL | Active clocked interrupt signal Note: I2C_EC is not available for this register |
| SCB7_INTR_SPI_EC | 0x40670EC0 | FULL | Externally clocked SPI interrupt request |
| SCB7_INTR_SPI_EC_MASK | 0x40670EC8 | FULL | Externally clocked SPI interrupt mask |
| SCB7_INTR_SPI_EC_MASKED | 0x40670ECC | FULL | Externally clocked SPI interrupt masked |
| SCB7_INTR_M | 0x40670F00 | FULL | Master interrupt request |
| SCB7_INTR_M_SET | 0x40670F04 | FULL | Master interrupt set request |
| SCB7_INTR_M_MASK | 0x40670F08 | FULL | Master interrupt mask |
| SCB7_INTR_M_MASKED | 0x40670F0C | FULL | Master interrupt masked request |
| SCB7_INTR_S | 0x40670F40 | FULL | Slave interrupt request |
| SCB7_INTR_S_SET | 0x40670F44 | FULL | Slave interrupt set request |
| SCB7_INTR_S_MASK | 0x40670F48 | FULL | Slave interrupt mask |
| SCB7_INTR_S_MASKED | 0x40670F4C | FULL | Slave interrupt masked request |
| SCB7_INTR_TX | 0x40670F80 | FULL | Transmitter interrupt request |
| SCB7_INTR_TX_SET | 0x40670F84 | FULL | Transmitter interrupt set request |
| SCB7_INTR_TX_MASK | 0x40670F88 | FULL | Transmitter interrupt mask |
| SCB7_INTR_TX_MASKED | 0x40670F8C | FULL | Transmitter interrupt masked request |

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|-----------------------------------|
| SCB7_INTR_RX | 0x40670FC0 | FULL | Receiver interrupt request |
| SCB7_INTR_RX_SET | 0x40670FC4 | FULL | Receiver interrupt set request |
| SCB7_INTR_RX_MASK | 0x40670FC8 | FULL | Receiver interrupt mask |
| SCB7_INTR_RX_MASKED | 0x40670FCC | FULL | Receiver interrupt masked request |

23.9 Register Details

23.9.1 SCB_CTRL

Description: Generic control
Address: 0x40600000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x300400F

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------|---|---|---|
| Name | None [7:4] | | | | OVS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------------|----|--------------|-----------------------|--------------|-----------------|------------------|------------------|
| Name | MEM_WIDTH [15:14] | | None [13:13] | CMD_RESP_MODE [12:12] | None [11:11] | EZ_MODE [10:10] | EC_OP_MODE [9:9] | EC_AM_MODE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|---------------|---------------------|
| Name | None [23:18] | | | | | | BLOCK [17:17] | ADDR_ACCEPT [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|--------------|----|-------------------|--------------|----|--------------|----|
| Name | ENABLED [31:31] | None [30:29] | | EC_ACCESS [28:28] | None [27:26] | | MODE [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:3 | OVS | RW | R | 15 | <p>Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. $OVS + 1$ SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period.</p> <p>In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate.</p> <p>In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support 'late MISO sample' functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE):</p> <ul style="list-style-type: none"> - MEDIAN is '0' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock ≥ 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock ≥ 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO 'late MISO sample functionality': SCB clock/IF clock ≥ 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has 'late MISO sample functionality': SCB clock/IF clock ≥ 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. <p>As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.</p> <p>In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| | | | | | <p>(Continuation)</p> <p>In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:</p> <ul style="list-style-type: none"> - 0: 16 times oversampling. <p>SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode.</p> <p>In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency):</p> <ul style="list-style-type: none"> - 0: 16 times oversampling. <p>SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode.</p> <p>Low power mode, OVS field values (with the required SCB clock frequency):</p> <ul style="list-style-type: none"> - 0: 16 times oversampling. - 1: 32 times oversampling. - 2: 48 times oversampling. - 3: 96 times oversampling. - 4: 192 times oversampling. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| | | | | | <p>(Continuation)</p> <p>SCB clock frequency of 192*9.6 KHz for 9.6 Kbps.</p> <ul style="list-style-type: none"> - 5: 768 times oversampling. <p>SCB clock frequency of 768*2.4 KHz for 2.4 Kbps.</p> <ul style="list-style-type: none"> - 6: 1536 times oversampling. <p>SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps.</p> <ul style="list-style-type: none"> - all other values are not used in low power mode. |
| 8 | EC_AM_MODE | RW | R | 0 | <p>This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI)</p> <p>'0': Internally clocked mode '1': Externally clocked mode</p> <p>In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface.</p> <p>The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE.</p> <p>Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported.</p> <p>In UART mode this field should be '0'.</p> |
| 9 | EC_OP_MODE | RW | R | 0 | <p>This field specifies the clocking for the SCB block</p> <p>'0': Internally clocked mode '1': externally clocked mode</p> <p>In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface.</p> <p>Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate).</p> <p>In UART mode this field should be '0'.</p> |
| 10 | EZ_MODE | RW | R | 0 | <p>Non EZ mode ('0') or EZ mode ('1').</p> <p>In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first.</p> <p>In UART mode this field should be '0'.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|---|
| 12 | CMD_RESP_MODE | RW | R | 0 | Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). |
| 14:15 | MEM_WIDTH | RW | R | 1 | Determines the number of bits per FIFO data element. |
| | BYTE | | | 0 | 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. |
| | HALFWORD | | | 1 | 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15]. |
| | WORD | | | 2 | 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31]. |
| | Reserved | | | 3 | N/A |
| 16 | ADDR_ACCEPT | RW | R | 0 | Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. |
| 17 | BLOCK | RW | R | 0 | Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. |
| 24:25 | MODE | RW | R | 3 | Mode of operation (3: Reserved) |
| | I2C | | | 0 | Inter-Integrated Circuits (I2C) mode. |
| | SPI | | | 1 | Serial Peripheral Interface (SPI) mode. |
| | UART | | | 2 | Universal Asynchronous Receiver/Transmitter (UART) mode. |
| 28 | EC_ACCESS | RW | R | 0 | EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this field should be set to 0. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 31 | ENABLED | RW | R | 0 | <p>SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows:</p> <ul style="list-style-type: none"> - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. <p>Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content).</p> <p>Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block,</p> <p>TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL,</p> |

23.9.2 SCB_STATUS

Description: Generic status
Address: 0x40600004
Offset: 0x4
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------|
| Name | None [7:1] | | | | | | | EC_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | EC_BUSY | R | W | Undefined | Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. |

23.9.3 SCB_CMD_RESP_CTRL

Description: Command/response control
Address: 0x40600008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | BASE_RD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|--------------------|
| Name | None [15:9] | | | | | | | BASE_RD_ADDR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | BASE_WR_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----------------------|
| Name | None [31:25] | | | | | | | BASE_WR_ADDR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| 0:8 | BASE_RD_ADDR | RW | R | 0 | I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers. |
| 16:24 | BASE_WR_ADDR | RW | R | 0 | I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. |

23.9.4 SCB_CMD_RESP_STATUS

Description: Command/response status

Address: 0x4060000C

Offset: 0xC

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields reflect register states without a default/reset value (CURR_RD_ADDR and CURR_WR_ADDR) or reflect an external bus state. Therefore, these registers are undefined after the IP is enabled.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | CURR_RD_ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|--------------------|
| Name | None [15:9] | | | | | | | CURR_RD_ADDR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | CURR_WR_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------------------|------------------------------|--------------|----|----|----|----|----------------------|
| Name | CMD_RESP_EC_BUSY [31:31] | CMD_RESP_EC_BUS_BUSY [30:30] | None [29:25] | | | | | CURR_WR_ADDR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0:8 | CURR_RD_ADDR | R | W | Undefined | <p>I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address).</p> <p>The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR).</p> <p>This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable.</p> |
| 16:24 | CURR_WR_ADDR | R | W | Undefined | <p>I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address).</p> <p>The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR).</p> <p>This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|---|
| 30 | CMD_RESP_EC_BUS_BUSY | R | W | Undefined | <p>Indicates whether there is an ongoing bus transfer to the IP. '0': no ongoing bus transfer. '1': ongoing bus transfer.</p> <p>For SPI, the field is '1' when slave mode is selected.</p> <p>For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match.</p> |
| 31 | CMD_RESP_EC_BUSY | R | W | Undefined | <p>Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note:</p> <ul style="list-style-type: none"> - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. <p>Note that this update lasts one I2C clock cycle, or two SPI clock cycles.</p> |

23.9.5 SCB_SPI_CTRL

Description: SPI control
Address: 0x40600020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3000010

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|-----------------------|------------------------|------------|------------|----------------------|-----------------------|
| Name | None [7:6] | | SCLK_CONTINUOUS [5:5] | LATE_MISO_SAMPLE [4:4] | CPOL [3:3] | CPHA [2:2] | SELECT_PRECEDE [1:1] | SSEL_CONTINUOUS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|-------------------------------|-----------------------|------------------------|------------------------|------------------------|----------------------|----------------------|
| Name | None [15:15] | SSEL_INTERR_FRAME_DEL [14:14] | SSEL_HOLD_DEL [13:13] | SSEL_SETUP_DEL [12:12] | SSEL_POLARITY3 [11:11] | SSEL_POLARITY2 [10:10] | SSEL_POLARITY1 [9:9] | SSEL_POLARITY0 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|------------------|
| Name | None [23:17] | | | | | | | LOOPBACK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|--------------|----|----|--------------|----|--------------|----|
| Name | MASTER_MODE [31:31] | None [30:28] | | | SSEL [27:26] | | MODE [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| 0 | SSEL_CONTINUOUS | RW | R | 0 | <p>Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field.</p> <p>When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are sent out without slave deselection.</p> <p>When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection.</p> |
| 1 | SELECT_PRECEDE | RW | R | 0 | <p>Only used in SPI Texas Instruments' submodule.</p> <p>When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit.</p> <p>When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 2 | CPHA | RW | R | 0 | <p>Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured:</p> <ul style="list-style-type: none"> - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. <p>In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid.</p> |
| 3 | CPOL | RW | R | 0 | <p>Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured:</p> <ul style="list-style-type: none"> - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. |
| 4 | LATE_MISO_SAMPLE | RW | R | 1 | <p>Changes the SCLK edge on which MISO is captured. Only used in master mode.</p> <p>When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK).</p> <p>When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.</p> |
| 5 | SCLK_CONTINUOUS | RW | R | 0 | <p>Only applicable in master mode.</p> <p>'0': SCLK is generated, when the SPI master is enabled and data is transmitted.</p> <p>'1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality.</p> |
| 8 | SSEL_POLARITY0 | RW | R | 0 | <p>Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes:</p> <p>'0': slave select is low/'0' active. '1': slave select is high/'1' active.</p> <p>For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse.</p> |
| 9 | SSEL_POLARITY1 | RW | R | 0 | Slave select polarity. |
| 10 | SSEL_POLARITY2 | RW | R | 0 | Slave select polarity. |
| 11 | SSEL_POLARITY3 | RW | R | 0 | Slave select polarity. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------------|----|----|-----------------|--|
| 12 | SSEL_SETUP_DEL | RW | R | 0 | <p>Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit).</p> <p>'0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles</p> <p>Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3.</p> <p>above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle.</p> |
| 13 | SSEL_HOLD_DEL | RW | R | 0 | <p>Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation).</p> <p>'0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles</p> <p>Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3.</p> <p>above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle.</p> |
| 14 | SSEL_INTER_FRAME_DEL | RW | R | 0 | <p>Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation).</p> <p>'0': 1.5 SPI clock cycles '1': 2.5 SPI clock cycles</p> <p>Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3.</p> <p>above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle.</p> |
| 16 | LOOPBACK | RW | R | 0 | <p>Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode.</p> <p>'0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI.</p> |
| 24:25 | MODE | RW | R | 3 | Submode of SPI operation (3: Reserved). |
| | SPI_MOTOROLA | | | 0 | <p>SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.</p> |
| | SPI_TI | | | 1 | <p>SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated.</p> |
| | SPI_NS | | | 2 | <p>SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 26:27 | SSEL | RW | R | 0 | Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. SCB block should be disabled when changes are made to this field. |
| 31 | MASTER_MODE | RW | R | 0 | Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. |

23.9.6 SCB_SPI_STATUS

Description: SPI status
Address: 0x40600024
Offset: 0x24
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-------------------|----------------|
| Name | None [7:2] | | | | | | SPI_EC_BUSY [1:1] | BUS_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | CURR_EZ_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | BASE_EZ_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0 | BUS_BUSY | R | W | Undefined | SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. |
| 1 | SPI_EC_BUSY | R | W | Undefined | Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. |
| 8:15 | CURR_EZ_ADDR | R | W | Undefined | SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. |
| 16:23 | BASE_EZ_ADDR | R | W | Undefined | SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. |

23.9.7 SCB_SPI_TX_CTRL

Description: SPI transmitter control
Address: 0x40600028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment: Only applies in SPI MOTOROLA submode, internally clocked SPI operation.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|----------------------|--------------|------------|---|---|---|
| Name | None [7:6] | | PARITY_ENABLED [5:5] | PARITY [4:4] | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity generation enabled ('1') or not ('0'). |

23.9.8 SCB_SPI_RX_CTRL

Description: SPI receiver control
Address: 0x4060002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment: Only applies in SPI MOTOROLA submode, internally clocked SPI operation.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|----------------------|--------------|------------|---|---|---|
| Name | None [7:6] | | PARITY_ENABLED [5:5] | PARITY [4:4] | None [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|----------------------------|
| Name | None [15:9] | | | | | | | DROP_ON_PARITY_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|--|
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity checking enabled ('1') or not ('0'). |
| 8 | DROP_ON_PARITY_ERROR | RW | R | 0 | Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. |

23.9.9 SCB_UART_CTRL

Description: UART control
Address: 0x40600040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x3000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|--------------|------------------|
| Name | None [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:17] | | | | | | | LOOPBACK [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:26] | | | | | | MODE [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------|----|----|-----------------|---|
| 16 | LOOPBACK | RW | R | 0 | Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. |
| 24:25 | MODE | RW | R | 3 | Submode of UART operation (3: Reserved) |
| | UART_STD | | | 0 | Standard UART submode. |
| | UART_SMARTCARD | | | 1 | SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. |
| | UART_IRDA | | | 2 | Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15. |

23.9.10 SCB_UART_TX_CTRL

Description: UART transmitter control
Address: 0x40600044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|----------------------|--------------|------------|-----------------|---|---|
| Name | None [7:6] | | PARITY_ENABLED [5:5] | PARITY [4:4] | None [3:3] | STOP_BITS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---------------------|
| Name | None [15:9] | | | | | | | RETRY_ON_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:2 | STOP_BITS | RW | R | 2 | Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. |
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware |
| 8 | RETRY_ON_NACK | RW | R | 0 | When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. |

23.9.11 SCB_UART_RX_CTRL

Description: UART receiver control
Address: 0x40600048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xA0002

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|----------------|----------------------|--------------|------------|-----------------|---|---|
| Name | None [7:7] | POLARITY [6:6] | PARITY_ENABLED [5:5] | PARITY [4:4] | None [3:3] | STOP_BITS [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|--------------------|------------------|--------------|-----------------|---------------------------|----------------------------|
| Name | None [15:14] | | SKIP_START [13:13] | LIN_MODE [12:12] | None [11:11] | MP_MODE [10:10] | DROP_ON_FRAME_ERROR [9:9] | DROP_ON_PARITY_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|---------------------|----|----|----|
| Name | None [23:20] | | | | BREAK_WIDTH [19:16] | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|---------------------|
| Name | None [31:25] | | | | | | | BREAK_LEVEL [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|---|
| 0:2 | STOP_BITS | RW | R | 2 | Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. |
| 4 | PARITY | RW | R | 0 | Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. |
| 5 | PARITY_ENABLED | RW | R | 0 | Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. |
| 6 | POLARITY | RW | R | 0 | Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. |
| 8 | DROP_ON_PARITY_ERROR | RW | R | 0 | Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------------|----|----|-----------------|--|
| 9 | DROP_ON_FRAME_ERROR | RW | R | 0 | Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. |
| 10 | MP_MODE | RW | R | 0 | Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. |
| 12 | LIN_MODE | RW | R | 0 | Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are used to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. |
| 13 | SKIP_START | RW | R | 0 | Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 16:19 | BREAK_WIDTH | RW | R | 10 | Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ('break field' detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. |
| 24 | BREAK_LEVEL | RW | R | 0 | 0: low level pulse detection, like Break field in LIN protocol 1: high level pulse detection, like IFS field in CXPI protocol, or idle line state in UART |

23.9.12 SCB_UART_RX_STATUS

Description: UART receiver status
Address: 0x4060004C
Offset: 0x4C
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|----|----|----|-------------------|----|----|----|
| Name | BR_COUNTER [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | BR_COUNTER [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:11 | BR_COUNTER | R | W | Undefined | Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. |

23.9.13 SCB_UART_FLOW_CTRL

Description: UART flow control

Address: 0x40600050

Offset: 0x50

Retention: Retained

IsDeepSleep: No

Comment: UART flow control is a design time configuration parameter, which make the presence of this MMIO register conditional to the configuration. The 'uart_rts_out' and 'uart_cts_in' are always present on the IP interface. If flow control is configured out, 'uart_rts_out' is NOT connected, and 'uart_cts_in' should be connected to '0'.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|---------------------|----------------------|
| Name | TRIGGER_LEVEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:17] | | | | | | | RTS_POLARITY [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:26] | | | | | | CTS_ENABLED [25:25] | CTS_POLARITY [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| 0:7 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to '0', flow control is effectively disabled (may be useful for debug purposes). |
| 16 | RTS_POLARITY | RW | R | 0 | Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. |
| 24 | CTS_POLARITY | RW | R | 0 | Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 25 | CTS_ENABLED | RW | R | 0 | <p>Enable use of CTS input signal by the UART transmitter:</p> <p>'0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register.</p> <p>'1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register.</p> <p>If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY).</p> |

23.9.14 SCB_I2C_CTRL

Description: I2C control
Address: 0x40600060
Offset: 0x60
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFB88

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|---|---|---|----------------------|---|---|---|
| Name | LOW_PHASE_OVS [7:4] | | | | HIGH_PHASE_OVS [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------------------------|-------------------------------|--------------------------|--------------------------|--------------------------|--------------|-----------------------------|------------------------|
| Name | S_NOT_READY_DATA_NACK [15:15] | S_NOT_READY_ADDR_NACK [14:14] | S_READY_DATA_ACK [13:13] | S_READY_ADDR_ACK [12:12] | S_GENERAL_IGNORE [11:11] | None [10:10] | M_NOT_READY_DATA_NACK [9:9] | M_READY_DATA_ACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|------------------|
| Name | None [23:17] | | | | | | | LOOPBACK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------------|--------------------|--------------|----|----|----|----|----|
| Name | MASTER_MODE [31:31] | SLAVE_MODE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:3 | HIGH_PHASE_OVS | RW | R | 8 | <p>Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering.</p> <p>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be ≥ 6 SCB clock cycles and ≤ 16 SCB clock cycles. Without input signal median filtering, the IF high time should be ≥ 5 SCB clock cycles and ≤ 16 SCB clock cycles.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------------|----|----|-----------------|---|
| 4:7 | LOW_PHASE_OVS | RW | R | 8 | <p>Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering.</p> <p>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be ≥ 8 SCB clock cycles and ≤ 16 IP clock cycles. Without input signal median filtering, the IF low time should be ≥ 7 SCB clock cycles and ≤ 16 SCB clock cycles.</p> <p>in slave mode, this field is used to define number of clk_scb cycles for tSU-DAT timing (from ACK/NACK/data ready, to SCL rising edge (released from I2C slave clock stretching))</p> |
| 8 | M_READY_DATA_ACK | RW | R | 1 | When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. |
| 9 | M_NOT_READY_DATA_NACK | RW | R | 1 | When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). |
| 11 | S_GENERAL_IGNORE | RW | R | 1 | When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. |
| 12 | S_READY_ADDR_ACK | RW | R | 1 | When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. |
| 13 | S_READY_DATA_ACK | RW | R | 1 | When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------------|----|----|-----------------|---|
| 14 | S_NOT_READY_ADDR_NACK | RW | R | 1 | <p>This field is used during an address match or general call address in internally clocked mode</p> <p>Only used when:</p> <ul style="list-style-type: none"> - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0' and non EZ mode. <p>Functionality is as follows:</p> <ul style="list-style-type: none"> - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). <p>For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode):</p> <ul style="list-style-type: none"> - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. <p>Functionality is as follows:</p> <ul style="list-style-type: none"> - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: <ol style="list-style-type: none"> 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. |
| 15 | S_NOT_READY_DATA_NACK | RW | R | 1 | <p>Only used when:</p> <ul style="list-style-type: none"> - non EZ mode <p>Functionality is as follows:</p> <ul style="list-style-type: none"> - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). |
| 16 | LOOPBACK | RW | R | 0 | <p>Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode.</p> <p>When '0', no loopback</p> <p>When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself.</p> |
| 30 | SLAVE_MODE | RW | R | 0 | Slave mode enabled ('1') or not ('0'). |
| 31 | MASTER_MODE | RW | R | 0 | Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. |

23.9.15 SCB_I2C_STATUS

Description: I2C status
Address: 0x40600064
Offset: 0x64
Retention: Not Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|--------------|--------------|------------|------------------------|-----------------------|----------------|
| Name | None [7:6] | | M_READ [5:5] | S_READ [4:4] | None [3:3] | I2CS_IC_B USY [2:2] | I2C_EC_BU SY [1:1] | BUS_BUSY [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | CURR_EZ_ADDR [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | BASE_EZ_ADDR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0 | BUS_BUSY | R | W | 0 | <p>I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period).</p> <p>For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions).</p> <p>For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions).</p> |
| 1 | I2C_EC_BUSY | R | W | Undefined | <p>Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable.</p> |
| 2 | I2CS_IC_BUSY | R | W | 0 | <p>Indicates whether the internally clocked slave logic is being accessed by external I2C master.</p> <p>--set at ADDR_MATCH</p> <p>--clear at START/RESET, STOP detection, or BUS_ERROR</p> <p>This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| 4 | S_READ | R | W | 0 | I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0'. |
| 5 | M_READ | R | W | 0 | I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0'. |
| 8:15 | CURR_EZ_ADDR | R | W | Undefined | I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. |
| 16:23 | BASE_EZ_ADDR | R | W | Undefined | I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. |

23.9.16 SCB_I2C_M_CMD

Description: I2C master command

Address: 0x40600068

Offset: 0x68

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------|-----------------|----------------|------------------------------|------------------|
| Name | None [7:5] | | | M_STOP [4:4] | M_NACK [3:3] | M_ACK [2:2] | M_START _ON_IDLE [1:1] | M_START [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|------|-----------------|--|
| 0 | M_START | RW | RW1C | 0 | When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. |
| 1 | M_START_ON_IDLE | RW | RW1C | 0 | When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0'). A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. |
| 2 | M_ACK | RW | RW1C | 0 | When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. |
| 3 | M_NACK | RW | RW1C | 0 | When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|------|-----------------|---|
| 4 | M_STOP | RW | RW1C | 0 | When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. |

23.9.17 SCB_I2C_S_CMD

Description: I2C slave command

Address: 0x4060006C

Offset: 0x6C

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------|-------------|
| Name | None [7:2] | | | | | | S_NACK [1:1] | S_ACK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|------|-----------------|---|
| 0 | S_ACK | RW | RW1C | 0 | When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). |
| 1 | S_NACK | RW | RW1C | 0 | When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. |

23.9.18 SCB_I2C_CFG

Description: I2C configuration

Address: 0x40600070

Offset: 0x70

Retention: Retained

IsDeepSleep: No

Comment: The filters are used to remove glitches and to guarantee I2C compliant SCL and SDA setup and hold times. The filters are trimmable.

Default: 0x2A1013

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-----------------------|------------|---|------------------------|---|
| Name | None [7:5] | | | SDA_IN_FILT_SEL [4:4] | None [3:2] | | SDA_IN_FILT_TRIM [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-------------------------|--------------|----|------------------------|---|
| Name | None [15:13] | | | SCL_IN_FILT_SEL [12:12] | None [11:10] | | SCL_IN_FILT_TRIM [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----------------------------|----|----------------------------|----|----------------------------|----|
| Name | None [23:22] | | SDA_OUT_FILT2_TRIM [21:20] | | SDA_OUT_FILT1_TRIM [19:18] | | SDA_OUT_FILT0_TRIM [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|--------------------------|----|--------------|----|----|----|
| Name | None [31:30] | | SDA_OUT_FILT_SEL [29:28] | | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------------|----|----|-----------------|--|
| 0:1 | SDA_IN_FILT_TRIM | RW | R | 3 | Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required |
| 4 | SDA_IN_FILT_SEL | RW | R | 1 | Enable for 50ns glitch filter on SDA input '0': 0 ns. '1': 50 ns (filter enabled). |
| 8:9 | SCL_IN_FILT_TRIM | RW | R | 0 | Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required |
| 12 | SCL_IN_FILT_SEL | RW | R | 1 | Enable for 50ns glitch filter on SCL input '0': 0 ns. '1': 50 ns (filter enabled). |
| 16:17 | SDA_OUT_FILT0_TRIM | RW | R | 2 | Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required |
| 18:19 | SDA_OUT_FILT1_TRIM | RW | R | 2 | Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required |
| 20:21 | SDA_OUT_FILT2_TRIM | RW | R | 2 | Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------------|----|----|-----------------|---|
| 28:29 | SDA_OUT_FILT_SEL | RW | R | 0 | Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter '0': 0 ns. '1': 50 ns (filter 0 enabled). '2': 100 ns (filters 0 and 1 enabled). '3': 150 ns (filters 0, 1 and 2 enabled). |

23.9.19 SCB_TX_CTRL

Description: Transmitter control
Address: 0x40600200
Offset: 0x200
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x107

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|---|---|---|---|
| Name | None [7:5] | | | DATA_WIDTH [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|-----------------|
| Name | None [15:9] | | | | | | | MSB_FIRST [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|--------------------|
| Name | None [23:17] | | | | | | | OPEN_DRAIN [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:4 | DATA_WIDTH | RW | R | 7 | Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. |
| 8 | MSB_FIRST | RW | R | 1 | Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 16 | OPEN_DRAIN | RW | R | 0 | <p>Each IO cell 'xxx' has two associated IP output signals 'xxx_out_en' and 'xxx_out'.</p> <p>'0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell 'xxx' that is used as an output, the 'xxx_out_en' output enable signal is typically constant '1' the 'xxx_out' output is the outputted value. In other words, in normal operation mode, the 'xxx_out' output is used to control the IO cell output value: 'xxx_out' is '0' to drive an IO cell output value of '0' and 'xxx_out' is '1' to drive an IO cell output value of '1'.</p> <p>'1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for an IO cell 'xxx' that is used as an output, the 'xxx_out_en' output controls the outputted value. Typically, open drain operation mode drives low/'0' and the 'xxx_out' output is constant '1'. In other words, in open drain operation mode, the 'xxx_out_en' output is used to control the IO cell output value: in drive low/'0' mode: 'xxx_out_en' is '1' (drive enabled) to drive an IO cell output value of '0' and 'xxx_out_en' is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1').</p> <p>The open drain mode is supported for:</p> <ul style="list-style-type: none"> - UART mode, 'uart_tx' IO cell. - SPI mode, 'spi_miso' IO cell. <p>not applicable to I2C mode, 'i2c_scl' and 'i2c_sda' IO cells. (I2C SCL/SDA always work in open-drain mode)</p> |

23.9.20 SCB_TX_FIFO_CTRL

Description: Transmitter FIFO control
Address: 0x40600204
Offset: 0x204
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----------------|---------------|
| Name | TRIGGER_LEVEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:7 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. |
| 16 | CLEAR | RW | R | 0 | When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. |
| 17 | FREEZE | RW | R | 0 | When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. |

23.9.21 SCB_TX_FIFO_STATUS

Description: Transmitter FIFO status
Address: 0x40600208
Offset: 0x208
Retention: Not Retained
IsDeepSleep: No
Comment: This register is not used in EZ and CMD_RESP modes.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | USED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|-------------|----|----|----|----|---|------------|
| Name | SR_VALID [15:15] | None [14:9] | | | | | | USED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | RD_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | WR_PTR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 0:8 | USED | R | W | 0 | Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). |
| 15 | SR_VALID | R | W | 0 | Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). |
| 16:23 | RD_PTR | R | W | 0 | FIFO read pointer: FIFO location from which a data frame is read by the hardware. |
| 24:31 | WR_PTR | R | W | 0 | FIFO write pointer: FIFO location at which a new data frame is written. |

23.9.22 SCB_TX_FIFO_WR

Description: Transmitter FIFO write
Address: 0x40600240
Offset: 0x240
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the TX FIFO is full, a write to this register is dropped. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'write only'; a read from this register returns '0'.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | DATA | W | R | 0 | <p>Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.MEM_WIDTH is '0', only DATA[7:0] are used and when CTRL.MEM_WIDTH is '1', only DATA[15:0] are used.</p> <p>A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'.</p> |

23.9.23 SCB_RX_CTRL

Description: Receiver control
Address: 0x40600300
Offset: 0x300
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x107

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------|---|---|---|---|
| Name | None [7:5] | | | DATA_WIDTH [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|--------------|-----------------|
| Name | None [15:10] | | | | | | MEDIAN [9:9] | MSB_FIRST [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:4 | DATA_WIDTH | RW | R | 7 | Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. |
| 8 | MSB_FIRST | RW | R | 1 | Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. |
| 9 | MEDIAN | RW | R | 0 | Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. |

23.9.24 SCB_RX_FIFO_CTRL

Description: Receiver FIFO control
Address: 0x40600304
Offset: 0x304
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----------------|---------------|
| Name | TRIGGER_LEVEL [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:18] | | | | | | FREEZE [17:17] | CLEAR [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:7 | TRIGGER_LEVEL | RW | R | 0 | Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. |
| 16 | CLEAR | RW | R | 0 | When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. |
| 17 | FREEZE | RW | R | 0 | When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. |

23.9.25 SCB_RX_FIFO_STATUS

Description: Receiver FIFO status
Address: 0x40600308
Offset: 0x308
Retention: Not Retained
IsDeepSleep: No
Comment: This register is not used in EZ and CMD_RESP modes.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | USED [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|-------------|----|----|----|----|---|------------|
| Name | SR_VALID [15:15] | None [14:9] | | | | | | USED [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | RD_PTR [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | WR_PTR [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|---|
| 0:8 | USED | R | W | 0 | Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). |
| 15 | SR_VALID | R | W | 0 | Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). |
| 16:23 | RD_PTR | R | W | 0 | FIFO read pointer: FIFO location from which a data frame is read. |
| 24:31 | WR_PTR | R | W | 0 | FIFO write pointer: FIFO location at which a new data frame is written by the hardware. |

23.9.26 SCB_RX_MATCH

Description: Slave address and mask
Address: 0x40600310
Offset: 0x310
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | ADDR [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | MASK [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------|----|----|-----------------|--|
| 0:7 | ADDR | RW | R | 0 | Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). |
| 16:23 | MASK | RW | R | 0 | Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ('slave address' & MASK)). |

23.9.27 SCB_RX_FIFO_RD

Description: Receiver FIFO read
Address: 0x40600340
Offset: 0x340
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff:ffff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes). This register is 'read only'; a write to this register is ignored.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | DATA | R | W | Undefined | <p>Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.MEM_WIDTH is '0', only DATA[7:0] are used and when CTRL.MEM_WIDTH is '1', only DATA[15:0] are used</p> <p>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'.</p> <p>When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT</p> |

23.9.28 SCB_RX_FIFO_RD_SILENT

Description: Receiver FIFO read silent
Address: 0x40600344
Offset: 0x344
Retention: Not Retained
IsDeepSleep: No
Comment: When the IP is disabled (CTRL.ENABLED is '0') or when the RX FIFO is empty, a read from this register returns 0xffff.fff. This register should only be used in FIFO mode (and not in EZ or CMD_RESP modes).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | DATA | R | W | Undefined | Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.MEM_WIDTH is '0', only DATA[7:0] are used and when CTRL.MEM_WIDTH is '1', only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. |

23.9.29 SCB_EZ_DATA

Description: Memory buffer

Address: 0x40600400

Offset: 0x400

Retention: Retained

IsDeepSleep: No

Comment: When the IP is disabled (CTRL.ENABLED is '0'), a read from these registers return 0xffff:ffff. It is under MMIO register control whether accesses to this register should introduce bus wait states or be discarded when the externally clocked logic is accessing the memory structure. These registers should only be used in EZ and CMD_RESP modes (and not in FIFO mode).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | EZ_DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | EZ_DATA | RW | RW | Undefined | Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. |

23.9.30 SCB_INTR_CAUSE

Description: Active clocked interrupt signal
Address: 0x40600E00
Offset: 0xE00
Retention: Retained
IsDeepSleep: No
Comment: Enables software to determine the source of the combined interrupt output signals 'interrupt_ic', 'interrupt_ec' and 'interrupt'.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|--------------|--------------|----------|----------|---------|---------|
| Name | None [7:6] | | SPI_EC [5:5] | I2C_EC [4:4] | RX [3:3] | TX [2:2] | S [1:1] | M [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0 | M | R | W | 0 | Master interrupt active ('interrupt_master'): INTR_M_MASKED != 0. |
| 1 | S | R | W | 0 | Slave interrupt active ('interrupt_slave'): INTR_S_MASKED != 0. |
| 2 | TX | R | W | 0 | Transmitter interrupt active ('interrupt_tx'): INTR_TX_MASKED != 0. |
| 3 | RX | R | W | 0 | Receiver interrupt active ('interrupt_rx'): INTR_RX_MASKED != 0. |
| 4 | I2C_EC | R | W | 0 | Externally clock I2C interrupt active ('interrupt_i2c_ec'): INTR_I2C_EC_MASKED != 0. |
| 5 | SPI_EC | R | W | 0 | Externally clocked SPI interrupt active ('interrupt_spi_ec'): INTR_SPI_EC_MASKED != 0. |

23.9.31 SCB_INTR_I2C_EC

Description: Externally clocked I2C interrupt request
Address: 0x40600E80
Offset: 0xE80
Retention: Retained
IsDeepSleep: No
Comment: The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------------|---------------------|---------------|---------------|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|----|-----------------|---|
| 0 | WAKE_UP | RW1C | A | 0 | Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. |
| 1 | EZ_STOP | RW1C | A | 0 | STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. |
| 2 | EZ_WRITE_STOP | RW1C | A | 0 | STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. |
| 3 | EZ_READ_STOP | RW1C | A | 0 | STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. |

23.9.32 SCB_INTR_I2C_EC_MASK

Description: Externally clocked I2C interrupt mask
Address: 0x40600E88
Offset: 0xE88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------------|---------------------|---------------|---------------|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | WAKE_UP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | EZ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | EZ_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | EZ_READ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

23.9.33 SCB_INTR_I2C_EC_MASKED

Description: Externally clocked I2C interrupt masked
Address: 0x40600E8C
Offset: 0xE8C
Retention: Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_I2C_EC_MASKED != 0.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------------|---------------------|---------------|---------------|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | WAKE_UP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | EZ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | EZ_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | EZ_READ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |

23.9.34 SCB_INTR_SPI_EC

Description: Externally clocked SPI interrupt request
Address: 0x40600EC0
Offset: 0xEC0
Retention: Retained
IsDeepSleep: No
Comment: The fields in this register are set by HW and are cleared by software by writing a '1'. These interrupt causes are generated by externally clocked logic. HW clears the interrupt causes to '0', when the IP is disabled.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------------|---------------------|---------------|---------------|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|----|-----------------|---|
| 0 | WAKE_UP | RW1C | A | 0 | Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. |
| 1 | EZ_STOP | RW1C | A | 0 | STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. |
| 2 | EZ_WRITE_STOP | RW1C | A | 0 | STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. |
| 3 | EZ_READ_STOP | RW1C | A | 0 | STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. |

23.9.35 SCB_INTR_SPI_EC_MASK

Description: Externally clocked SPI interrupt mask
Address: 0x40600EC8
Offset: 0xEC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|-----------------------|------------------------|------------------|------------------|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | WAKE_UP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | EZ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | EZ_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | EZ_READ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

23.9.36 SCB_INTR_SPI_EC_MASKED

Description: Externally clocked SPI interrupt masked
Address: 0x40600ECC
Offset: 0xECC
Retention: Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_SPI_EC_MASKED != 0.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|--------------------|---------------------|---------------|---------------|
| Name | None [7:4] | | | | EZ_READ_STOP [3:3] | EZ_WRITE_STOP [2:2] | EZ_STOP [1:1] | WAKE_UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | WAKE_UP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | EZ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | EZ_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | EZ_READ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |

23.9.37 SCB_INTR_M

Description: Master interrupt request

Address: 0x40600F00

Offset: 0xF00

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

Default: The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|------------|---------------|----------------|--------------------|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------|---------------------|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|------|-----------------|--|
| 0 | I2C_ARB_LOST | RW1C | RW1S | 0 | I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. |
| 1 | I2C_NACK | RW1C | RW1S | 0 | I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). |
| 2 | I2C_ACK | RW1C | RW1S | 0 | I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). |
| 4 | I2C_STOP | RW1C | RW1S | 0 | I2C master STOP. Set to '1', when the master has transmitted a STOP. |
| 8 | I2C_BUS_ERROR | RW1C | RW1S | 0 | I2C master bus error (unexpected detection of START or STOP condition). |
| 9 | SPI_DONE | RW1C | RW1S | 0 | SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is deselected. |

23.9.38 SCB_INTR_M_SET

Description: Master interrupt set request
Address: 0x40600F04
Offset: 0xF04
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|------------|---------------|----------------|--------------------|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------|---------------------|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|----|-----------------|--|
| 0 | I2C_ARB_LOST | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | SPI_DONE | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

23.9.39 SCB_INTR_M_MASK

Description: Master interrupt mask
Address: 0x40600F08
Offset: 0xF08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|----------------|------------|---------------|----------------|--------------------|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|----------------|---------------------|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | I2C_ARB_LOST | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | SPI_DONE | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

23.9.40 SCB_INTR_M_MASKED

Description: Master interrupt masked request

Address: 0x40600F0C

Offset: 0xF0C

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_M_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|-------------------|------------|------------------|-------------------|-----------------------|
| Name | None [7:5] | | | I2C_STOP [4:4] | None [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|-------------------|------------------------|
| Name | None [15:10] | | | | | | SPI_DONE [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | I2C_ARB_LOST | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | I2C_NACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | I2C_ACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | I2C_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | I2C_BUS_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | SPI_DONE | R | W | 0 | Logical and of corresponding request and mask bits. |

23.9.41 SCB_INTR_S

Description: Slave interrupt request

Address: 0x40600F40

Offset: 0xF40

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

Default: The interrupt causes should only be used for internally clocked operation; i.e. EC_OP is '0'.
0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----------------------|-----------------|----------------|-----------------------|---------------------|-------------------------|---------------------|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|------|------|-----------------|--|
| 0 | I2C_ARB_LOST | RW1C | RW1S | 0 | I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. |
| 1 | I2C_NACK | RW1C | RW1S | 0 | I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). |
| 2 | I2C_ACK | RW1C | RW1S | 0 | I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|------|------|-----------------|--|
| 3 | I2C_WRITE_STOP | RW1C | RW1S | 0 | <p>I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.</p> <p>In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd.</p> <p>In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected).</p> |
| 4 | I2C_STOP | RW1C | RW1S | 0 | <p>I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.</p> <p>The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd.</p> |
| 5 | I2C_START | RW1C | RW1S | 0 | <p>I2C slave START received. Set to '1', when START or REPEATED START event is detected.</p> <p>In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL.</p> |
| 6 | I2C_ADDR_MATCH | RW1C | RW1S | 0 | <p>I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected.</p> |
| 7 | I2C_GENERAL | RW1C | RW1S | 0 | <p>I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|------|-----------------|---|
| 8 | I2C_BUS_ERROR | RW1C | RW1S | 0 | I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. |
| 9 | SPI_EZ_WRITE_STOP | RW1C | RW1S | 0 | SPI slave deselected after a write EZ SPI transfer occurred. |
| 10 | SPI_EZ_STOP | RW1C | RW1S | 0 | SPI slave deselected after any EZ SPI transfer occurred. |
| 11 | SPI_BUS_ERROR | RW1C | RW1S | 0 | SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. |

23.9.42 SCB_INTR_S_SET

Description: Slave interrupt set request
Address: 0x40600F44
Offset: 0xF44
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----------------------|-----------------|----------------|----------------------|---------------|----------------|--------------------|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-----------------------|---------------------|-------------------------|---------------------|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|----|-----------------|--|
| 0 | I2C_ARB_LOST | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 3 | I2C_WRITE_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 5 | I2C_START | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 6 | I2C_ADDR_MATCH | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 7 | I2C_GENERAL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | SPI_EZ_WRITE_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 10 | SPI_EZ_STOP | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 11 | SPI_BUS_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

23.9.43 SCB_INTR_S_MASK

Description: Slave interrupt mask
Address: 0x40600F48
Offset: 0xF48
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----------------------|-----------------|----------------|----------------------|---------------|----------------|--------------------|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-----------------------|---------------------|-------------------------|---------------------|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|---|
| 0 | I2C_ARB_LOST | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | I2C_NACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | I2C_ACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | I2C_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | I2C_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | I2C_START | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | I2C_ADDR_MATCH | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 7 | I2C_GENERAL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | I2C_BUS_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | SPI_EZ_WRITE_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | SPI_EZ_STOP | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 11 | SPI_BUS_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

23.9.44 SCB_INTR_S_MASKED

Description: Slave interrupt masked request

Address: 0x40600F4C

Offset: 0xF4C

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_S_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----------------------|-----------------|----------------|----------------------|---------------|----------------|--------------------|
| Name | I2C_GENERAL [7:7] | I2C_ADDR_MATCH [6:6] | I2C_START [5:5] | I2C_STOP [4:4] | I2C_WRITE_STOP [3:3] | I2C_ACK [2:2] | I2C_NACK [1:1] | I2C_ARB_LOST [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-----------------------|---------------------|-------------------------|---------------------|
| Name | None [15:12] | | | | SPI_BUS_ERROR [11:11] | SPI_EZ_STOP [10:10] | SPI_EZ_WRITE_STOP [9:9] | I2C_BUS_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|---|
| 0 | I2C_ARB_LOST | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | I2C_NACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | I2C_ACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | I2C_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | I2C_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | I2C_START | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | I2C_ADDR_MATCH | R | W | 0 | Logical and of corresponding request and mask bits. |
| 7 | I2C_GENERAL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | I2C_BUS_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | SPI_EZ_WRITE_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | SPI_EZ_STOP | R | W | 0 | Logical and of corresponding request and mask bits. |
| 11 | SPI_BUS_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |

23.9.45 SCB_INTR_TX

Description: Transmitter interrupt request

Address: 0x40600F80

Offset: 0xF80

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------------|-------------------|----------------|------------|---|-------------------|------------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------------|--------------------|--------------------|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|------|------|-----------------|--|
| 0 | TRIGGER | RW1C | RW1S | 0 | Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. |
| 1 | NOT_FULL | RW1C | RW1S | 0 | TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is '0': # entries != FF_DATA_NR. MEM_WIDTH is '1': # entries != FF_DATA_NR/2. MEM_WIDTH is '2': # entries != FF_DATA_NR/4. Only used in FIFO mode. |
| 4 | EMPTY | RW1C | RW1S | 0 | TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. |
| 5 | OVERFLOW | RW1C | RW1S | 0 | Attempt to write to a full TX FIFO. Only used in FIFO mode. |
| 6 | UNDERFLOW | RW1C | RW1S | 0 | Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. |
| 7 | BLOCKED | RW1C | RW1S | 0 | SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. |
| 8 | UART_NACK | RW1C | RW1S | 0 | UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|------|-----------------|--|
| 9 | UART_DONE | RW1C | RW1S | 0 | UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Set to '1', when event is detected. Write with '1' to clear bit. |
| 10 | UART_ARB_LOST | RW1C | RW1S | 0 | UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. |

23.9.46 SCB_INTR_TX_SET

Description: Transmitter interrupt set request
Address: 0x40600F84
Offset: 0xF84
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------------|-------------------|----------------|------------|---|-------------------|------------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------------|--------------------|--------------------|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|----|-----------------|--|
| 0 | TRIGGER | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | NOT_FULL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 4 | EMPTY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 5 | OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 6 | UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 7 | BLOCKED | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 8 | UART_NACK | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 9 | UART_DONE | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 10 | UART_ARB_LOST | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

23.9.47 SCB_INTR_TX_MASK

Description: Transmitter interrupt mask
Address: 0x40600F88
Offset: 0xF88
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------------|-------------------|----------------|------------|---|-------------------|------------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------------|--------------------|--------------------|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | TRIGGER | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | NOT_FULL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 4 | EMPTY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 7 | BLOCKED | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | UART_NACK | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | UART_DONE | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | UART_ARB_LOST | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

23.9.48 SCB_INTR_TX_MASKED

Description: Transmitter interrupt masked request

Address: 0x40600F8C

Offset: 0xF8C

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_TX_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------------|-------------------|----------------|------------|---|-------------------|------------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | EMPTY [4:4] | None [3:2] | | NOT_FULL [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------------|--------------------|--------------------|
| Name | None [15:11] | | | | | UART_ARB_LOST [10:10] | UART_DONE [9:9] | UART_NACK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0 | TRIGGER | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | NOT_FULL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 4 | EMPTY | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 7 | BLOCKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | UART_NACK | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | UART_DONE | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | UART_ARB_LOST | R | W | 0 | Logical and of corresponding request and mask bits. |

23.9.49 SCB_INTR_RX

Description: Receiver interrupt request

Address: 0x40600FC0

Offset: 0xFC0

Retention: Not Retained

IsDeepSleep: No

Comment: The register fields are not retained In DeepSleep power mode: HW clears the interrupt causes to '0', when coming out of DeepSleep power mode. In addition, HW clears the interrupt causes to '0', when the IP is disabled. As a result, the interrupt causes are only available in Active/Sleep power modes; they are generated by internally clocked logic (this logic operates on a clock that is only available in Active/Sleep power modes).

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|-----------------|----------------|------------|------------|-----------------|------------|---------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT_EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----------------------|---------------------|--------------------|-------------------|
| Name | None [15:12] | | | | BREAK_DETECT [11:11] | BAUD_DETECT [10:10] | PARITY_ERROR [9:9] | FRAME_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|------|------|-----------------|--|
| 0 | TRIGGER | RW1C | RW1S | 0 | More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. |
| 2 | NOT_EMPTY | RW1C | RW1S | 0 | RX FIFO is not empty. Only used in FIFO mode. |
| 3 | FULL | RW1C | RW1S | 0 | RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is '0': # entries == FF_DATA_NR. MEM_WIDTH is '1': # entries == FF_DATA_NR/2. MEM_WIDTH is '2': # entries == FF_DATA_NR/4. Only used in FIFO mode. |
| 5 | OVERFLOW | RW1C | RW1S | 0 | Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. |
| 6 | UNDERFLOW | RW1C | RW1S | 0 | Attempt to read from an empty RX FIFO. Only used in FIFO mode. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|------|------|-----------------|---|
| 7 | BLOCKED | RW1C | RW1S | 0 | SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. |
| 8 | FRAME_ERROR | RW1C | RW1S | 0 | <p>Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error:</p> <p>Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received.</p> <p>Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received.</p> <p>A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames.</p> |
| 9 | PARITY_ERROR | RW1C | RW1S | 0 | <p>Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO.</p> |
| 10 | BAUD_DETECT | RW1C | RW1S | 0 | <p>LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit.</p> |
| 11 | BREAK_DETECT | RW1C | RW1S | 0 | <p>Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. 'break-in-data' is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit.</p> |

23.9.50 SCB_INTR_RX_SET

Description: Receiver interrupt set request
Address: 0x40600FC4
Offset: 0xFC4
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|--------------------|-------------------|------------|------------|--------------------|------------|------------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT_EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|-------------------------|------------------------|-----------------------|----------------------|
| Name | None [15:12] | | | | BREAK_DETECT [11:11] | BAUD_DETECT [10:10] | PARITY_ERROR [9:9] | FRAME_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|------|----|-----------------|--|
| 0 | TRIGGER | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | NOT_EMPTY | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 3 | FULL | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 5 | OVERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 6 | UNDERFLOW | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 7 | BLOCKED | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 8 | FRAME_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 9 | PARITY_ERROR | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 10 | BAUD_DETECT | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |
| 11 | BREAK_DETECT | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt status register. |

23.9.51 SCB_INTR_RX_MASK

Description: Receiver interrupt mask
Address: 0x40600FC8
Offset: 0xFC8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|-----------------|----------------|------------|------------|-----------------|------------|---------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT_EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----------------------|---------------------|--------------------|-------------------|
| Name | None [15:12] | | | | BREAK_DETECT [11:11] | BAUD_DETECT [10:10] | PARITY_ERROR [9:9] | FRAME_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0 | TRIGGER | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | NOT_EMPTY | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 3 | FULL | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 5 | OVERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 6 | UNDERFLOW | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 7 | BLOCKED | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 8 | FRAME_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 9 | PARITY_ERROR | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 10 | BAUD_DETECT | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 11 | BREAK_DETECT | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

23.9.52 SCB_INTR_RX_MASKED

Description: Receiver interrupt masked request

Address: 0x40600FCC

Offset: 0xFCC

Retention: Not Retained

IsDeepSleep: No

Comment: When read, this register reflects a bitwise and between the interrupt request and mask registers. This register allows SW to read the status of all mask enabled interrupt causes with a single load operation, rather than two load operations: one for the interrupt causes and one for the masks. This simplifies Firmware development. The associated interrupt is active ('1'), when INTR_RX_MASKED != 0.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|-----------------|----------------|------------|------------|-----------------|------------|---------------|
| Name | BLOCKED [7:7] | UNDERFLOW [6:6] | OVERFLOW [5:5] | None [4:4] | FULL [3:3] | NOT_EMPTY [2:2] | None [1:1] | TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----------------------|---------------------|--------------------|-------------------|
| Name | None [15:12] | | | | BREAK_DETECT [11:11] | BAUD_DETECT [10:10] | PARITY_ERROR [9:9] | FRAME_ERROR [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0 | TRIGGER | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | NOT_EMPTY | R | W | 0 | Logical and of corresponding request and mask bits. |
| 3 | FULL | R | W | 0 | Logical and of corresponding request and mask bits. |
| 5 | OVERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 6 | UNDERFLOW | R | W | 0 | Logical and of corresponding request and mask bits. |
| 7 | BLOCKED | R | W | 0 | Logical and of corresponding request and mask bits. |
| 8 | FRAME_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 9 | PARITY_ERROR | R | W | 0 | Logical and of corresponding request and mask bits. |
| 10 | BAUD_DETECT | R | W | 0 | Logical and of corresponding request and mask bits. |
| 11 | BREAK_DETECT | R | W | 0 | Logical and of corresponding request and mask bits. |

24 SFLASH

Description FLASH Supervisory Region
Base Address 0x17000000
Size 0x8000
Slave Num MEMORYMAP

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| SFLASH_SI_REVISION_ID | 0x17000001 | FULL | Indicates Silicon Revision ID of the device |
| SFLASH_SILICON_ID | 0x17000002 | FULL | Indicates Silicon ID of the device |
| SFLASH_SFLASH_SVN | 0x170000A8 | FULL | SFLASH Subversion |
| SFLASH_FB_FLAGS | 0x170001FC | FULL | Flash boot flags |
| SFLASH_EPASS_TEMP_TRIM_TEMP_ROOMSORT | 0x1700064E | FULL | On Chip temperature measured using external currents and external ADC at ROOM |
| SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT | 0x17000650 | FULL | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT | 0x17000652 | FULL | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_TEMP_COLDSORT | 0x17000654 | FULL | On Chip temperature measured using external currents and external ADC at COLD |
| SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT | 0x17000656 | FULL | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT | 0x17000658 | FULL | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_TEMP_HOTCLASS | 0x1700065A | FULL | On Chip temperature measured using external currents and external ADC at HOT |
| SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS | 0x1700065C | FULL | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT |
| SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS | 0x1700065E | FULL | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT |
| SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT_5V | 0x1700066A | FULL | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT_5V | 0x1700066C | FULL | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM |
| SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT_5V | 0x1700066E | FULL | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT_5V | 0x17000670 | FULL | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD |
| SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS_5V | 0x17000672 | FULL | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT |
| SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS_5V | 0x17000674 | FULL | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT |
| SFLASH_SRSS_PWR_OFFSET | 0x17000730 | FULL | SRSS_PWR_OFFSET |
| SFLASH_USER_FREE_ROW00 | 0x17000800 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW01 | 0x17000804 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW02 | 0x17000808 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW03 | 0x1700080C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW04 | 0x17000810 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW05 | 0x17000814 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW06 | 0x17000818 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW07 | 0x1700081C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW08 | 0x17000820 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW09 | 0x17000824 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW010 | 0x17000828 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW011 | 0x1700082C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW012 | 0x17000830 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW013 | 0x17000834 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW014 | 0x17000838 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW015 | 0x1700083C | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW016 | 0x17000840 | FULL | USER_FREE_ROW0 |
| SFLASH_USER_FREE_ROW017 | 0x17000844 | FULL | USER_FREE_ROW0 |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW018 | 0x17000848 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW019 | 0x1700084C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW020 | 0x17000850 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW021 | 0x17000854 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW022 | 0x17000858 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW023 | 0x1700085C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW024 | 0x17000860 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW025 | 0x17000864 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW026 | 0x17000868 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW027 | 0x1700086C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW028 | 0x17000870 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW029 | 0x17000874 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW030 | 0x17000878 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW031 | 0x1700087C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW032 | 0x17000880 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW033 | 0x17000884 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW034 | 0x17000888 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW035 | 0x1700088C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW036 | 0x17000890 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW037 | 0x17000894 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW038 | 0x17000898 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW039 | 0x1700089C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW040 | 0x170008A0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW041 | 0x170008A4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW042 | 0x170008A8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW043 | 0x170008AC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW044 | 0x170008B0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW045 | 0x170008B4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW046 | 0x170008B8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW047 | 0x170008BC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW048 | 0x170008C0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW049 | 0x170008C4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW050 | 0x170008C8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW051 | 0x170008CC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW052 | 0x170008D0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW053 | 0x170008D4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW054 | 0x170008D8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW055 | 0x170008DC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW056 | 0x170008E0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW057 | 0x170008E4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW058 | 0x170008E8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW059 | 0x170008EC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW060 | 0x170008F0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW061 | 0x170008F4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW062 | 0x170008F8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW063 | 0x170008FC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW064 | 0x17000900 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW065 | 0x17000904 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW066 | 0x17000908 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW067 | 0x1700090C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW068 | 0x17000910 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW069 | 0x17000914 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW070 | 0x17000918 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW071 | 0x1700091C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW072 | 0x17000920 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW073 | 0x17000924 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW074 | 0x17000928 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW075 | 0x1700092C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW076 | 0x17000930 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW077 | 0x17000934 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW078 | 0x17000938 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW079 | 0x1700093C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW080 | 0x17000940 | FULL | USER FREE ROW0 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW081 | 0x17000944 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW082 | 0x17000948 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW083 | 0x1700094C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW084 | 0x17000950 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW085 | 0x17000954 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW086 | 0x17000958 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW087 | 0x1700095C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW088 | 0x17000960 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW089 | 0x17000964 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW090 | 0x17000968 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW091 | 0x1700096C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW092 | 0x17000970 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW093 | 0x17000974 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW094 | 0x17000978 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW095 | 0x1700097C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW096 | 0x17000980 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW097 | 0x17000984 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW098 | 0x17000988 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW099 | 0x1700098C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0100 | 0x17000990 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0101 | 0x17000994 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0102 | 0x17000998 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0103 | 0x1700099C | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0104 | 0x170009A0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0105 | 0x170009A4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0106 | 0x170009A8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0107 | 0x170009AC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0108 | 0x170009B0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0109 | 0x170009B4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0110 | 0x170009B8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0111 | 0x170009BC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0112 | 0x170009C0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0113 | 0x170009C4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0114 | 0x170009C8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0115 | 0x170009CC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0116 | 0x170009D0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0117 | 0x170009D4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0118 | 0x170009D8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0119 | 0x170009DC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0120 | 0x170009E0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0121 | 0x170009E4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0122 | 0x170009E8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0123 | 0x170009EC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0124 | 0x170009F0 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0125 | 0x170009F4 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0126 | 0x170009F8 | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW0127 | 0x170009FC | FULL | USER FREE ROW0 |
| SFLASH_USER_FREE_ROW10 | 0x17000A00 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW11 | 0x17000A04 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW12 | 0x17000A08 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW13 | 0x17000A0C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW14 | 0x17000A10 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW15 | 0x17000A14 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW16 | 0x17000A18 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW17 | 0x17000A1C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW18 | 0x17000A20 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW19 | 0x17000A24 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW110 | 0x17000A28 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW111 | 0x17000A2C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW112 | 0x17000A30 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW113 | 0x17000A34 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW114 | 0x17000A38 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW115 | 0x17000A3C | FULL | USER FREE ROW1 |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW116 | 0x17000A40 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW117 | 0x17000A44 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW118 | 0x17000A48 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW119 | 0x17000A4C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW120 | 0x17000A50 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW121 | 0x17000A54 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW122 | 0x17000A58 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW123 | 0x17000A5C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW124 | 0x17000A60 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW125 | 0x17000A64 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW126 | 0x17000A68 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW127 | 0x17000A6C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW128 | 0x17000A70 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW129 | 0x17000A74 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW130 | 0x17000A78 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW131 | 0x17000A7C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW132 | 0x17000A80 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW133 | 0x17000A84 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW134 | 0x17000A88 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW135 | 0x17000A8C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW136 | 0x17000A90 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW137 | 0x17000A94 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW138 | 0x17000A98 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW139 | 0x17000A9C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW140 | 0x17000AA0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW141 | 0x17000AA4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW142 | 0x17000AA8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW143 | 0x17000AAC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW144 | 0x17000AB0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW145 | 0x17000AB4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW146 | 0x17000AB8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW147 | 0x17000ABC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW148 | 0x17000AC0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW149 | 0x17000AC4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW150 | 0x17000AC8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW151 | 0x17000ACC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW152 | 0x17000AD0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW153 | 0x17000AD4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW154 | 0x17000AD8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW155 | 0x17000ADC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW156 | 0x17000AE0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW157 | 0x17000AE4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW158 | 0x17000AE8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW159 | 0x17000AEC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW160 | 0x17000AF0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW161 | 0x17000AF4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW162 | 0x17000AF8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW163 | 0x17000AFC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW164 | 0x17000B00 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW165 | 0x17000B04 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW166 | 0x17000B08 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW167 | 0x17000B0C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW168 | 0x17000B10 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW169 | 0x17000B14 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW170 | 0x17000B18 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW171 | 0x17000B1C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW172 | 0x17000B20 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW173 | 0x17000B24 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW174 | 0x17000B28 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW175 | 0x17000B2C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW176 | 0x17000B30 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW177 | 0x17000B34 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW178 | 0x17000B38 | FULL | USER FREE ROW1 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW179 | 0x17000B3C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW180 | 0x17000B40 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW181 | 0x17000B44 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW182 | 0x17000B48 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW183 | 0x17000B4C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW184 | 0x17000B50 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW185 | 0x17000B54 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW186 | 0x17000B58 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW187 | 0x17000B5C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW188 | 0x17000B60 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW189 | 0x17000B64 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW190 | 0x17000B68 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW191 | 0x17000B6C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW192 | 0x17000B70 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW193 | 0x17000B74 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW194 | 0x17000B78 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW195 | 0x17000B7C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW196 | 0x17000B80 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW197 | 0x17000B84 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW198 | 0x17000B88 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW199 | 0x17000B8C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1100 | 0x17000B90 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1101 | 0x17000B94 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1102 | 0x17000B98 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1103 | 0x17000B9C | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1104 | 0x17000BA0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1105 | 0x17000BA4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1106 | 0x17000BA8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1107 | 0x17000BAC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1108 | 0x17000BB0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1109 | 0x17000BB4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1110 | 0x17000BB8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1111 | 0x17000BBC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1112 | 0x17000BC0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1113 | 0x17000BC4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1114 | 0x17000BC8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1115 | 0x17000BCC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1116 | 0x17000BD0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1117 | 0x17000BD4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1118 | 0x17000BD8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1119 | 0x17000BDC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1120 | 0x17000BE0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1121 | 0x17000BE4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1122 | 0x17000BE8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1123 | 0x17000BEC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1124 | 0x17000BF0 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1125 | 0x17000BF4 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1126 | 0x17000BF8 | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW1127 | 0x17000BFC | FULL | USER FREE ROW1 |
| SFLASH_USER_FREE_ROW20 | 0x17000C00 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW21 | 0x17000C04 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW22 | 0x17000C08 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW23 | 0x17000C0C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW24 | 0x17000C10 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW25 | 0x17000C14 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW26 | 0x17000C18 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW27 | 0x17000C1C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW28 | 0x17000C20 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW29 | 0x17000C24 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW210 | 0x17000C28 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW211 | 0x17000C2C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW212 | 0x17000C30 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW213 | 0x17000C34 | FULL | USER FREE ROW2 |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW214 | 0x17000C38 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW215 | 0x17000C3C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW216 | 0x17000C40 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW217 | 0x17000C44 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW218 | 0x17000C48 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW219 | 0x17000C4C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW220 | 0x17000C50 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW221 | 0x17000C54 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW222 | 0x17000C58 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW223 | 0x17000C5C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW224 | 0x17000C60 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW225 | 0x17000C64 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW226 | 0x17000C68 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW227 | 0x17000C6C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW228 | 0x17000C70 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW229 | 0x17000C74 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW230 | 0x17000C78 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW231 | 0x17000C7C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW232 | 0x17000C80 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW233 | 0x17000C84 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW234 | 0x17000C88 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW235 | 0x17000C8C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW236 | 0x17000C90 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW237 | 0x17000C94 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW238 | 0x17000C98 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW239 | 0x17000C9C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW240 | 0x17000CA0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW241 | 0x17000CA4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW242 | 0x17000CA8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW243 | 0x17000CAC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW244 | 0x17000CB0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW245 | 0x17000CB4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW246 | 0x17000CB8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW247 | 0x17000CBC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW248 | 0x17000CC0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW249 | 0x17000CC4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW250 | 0x17000CC8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW251 | 0x17000CCC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW252 | 0x17000CD0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW253 | 0x17000CD4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW254 | 0x17000CD8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW255 | 0x17000CDC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW256 | 0x17000CE0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW257 | 0x17000CE4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW258 | 0x17000CE8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW259 | 0x17000CEC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW260 | 0x17000CF0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW261 | 0x17000CF4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW262 | 0x17000CF8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW263 | 0x17000CFC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW264 | 0x17000D00 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW265 | 0x17000D04 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW266 | 0x17000D08 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW267 | 0x17000D0C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW268 | 0x17000D10 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW269 | 0x17000D14 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW270 | 0x17000D18 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW271 | 0x17000D1C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW272 | 0x17000D20 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW273 | 0x17000D24 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW274 | 0x17000D28 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW275 | 0x17000D2C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW276 | 0x17000D30 | FULL | USER FREE ROW2 |

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW277 | 0x17000D34 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW278 | 0x17000D38 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW279 | 0x17000D3C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW280 | 0x17000D40 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW281 | 0x17000D44 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW282 | 0x17000D48 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW283 | 0x17000D4C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW284 | 0x17000D50 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW285 | 0x17000D54 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW286 | 0x17000D58 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW287 | 0x17000D5C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW288 | 0x17000D60 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW289 | 0x17000D64 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW290 | 0x17000D68 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW291 | 0x17000D6C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW292 | 0x17000D70 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW293 | 0x17000D74 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW294 | 0x17000D78 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW295 | 0x17000D7C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW296 | 0x17000D80 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW297 | 0x17000D84 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW298 | 0x17000D88 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW299 | 0x17000D8C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2100 | 0x17000D90 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2101 | 0x17000D94 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2102 | 0x17000D98 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2103 | 0x17000D9C | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2104 | 0x17000DA0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2105 | 0x17000DA4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2106 | 0x17000DA8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2107 | 0x17000DAC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2108 | 0x17000DB0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2109 | 0x17000DB4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2110 | 0x17000DB8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2111 | 0x17000DBC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2112 | 0x17000DC0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2113 | 0x17000DC4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2114 | 0x17000DC8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2115 | 0x17000DCC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2116 | 0x17000DD0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2117 | 0x17000DD4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2118 | 0x17000DD8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2119 | 0x17000DDC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2120 | 0x17000DE0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2121 | 0x17000DE4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2122 | 0x17000DE8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2123 | 0x17000DEC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2124 | 0x17000DF0 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2125 | 0x17000DF4 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2126 | 0x17000DF8 | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW2127 | 0x17000DFC | FULL | USER FREE ROW2 |
| SFLASH_USER_FREE_ROW30 | 0x17000E00 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW31 | 0x17000E04 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW32 | 0x17000E08 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW33 | 0x17000E0C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW34 | 0x17000E10 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW35 | 0x17000E14 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW36 | 0x17000E18 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW37 | 0x17000E1C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW38 | 0x17000E20 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW39 | 0x17000E24 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW310 | 0x17000E28 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW311 | 0x17000E2C | FULL | USER FREE ROW3 |

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|----------------|
| SFLASH_USER_FREE_ROW312 | 0x17000E30 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW313 | 0x17000E34 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW314 | 0x17000E38 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW315 | 0x17000E3C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW316 | 0x17000E40 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW317 | 0x17000E44 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW318 | 0x17000E48 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW319 | 0x17000E4C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW320 | 0x17000E50 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW321 | 0x17000E54 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW322 | 0x17000E58 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW323 | 0x17000E5C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW324 | 0x17000E60 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW325 | 0x17000E64 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW326 | 0x17000E68 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW327 | 0x17000E6C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW328 | 0x17000E70 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW329 | 0x17000E74 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW330 | 0x17000E78 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW331 | 0x17000E7C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW332 | 0x17000E80 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW333 | 0x17000E84 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW334 | 0x17000E88 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW335 | 0x17000E8C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW336 | 0x17000E90 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW337 | 0x17000E94 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW338 | 0x17000E98 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW339 | 0x17000E9C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW340 | 0x17000EA0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW341 | 0x17000EA4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW342 | 0x17000EA8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW343 | 0x17000EAC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW344 | 0x17000EB0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW345 | 0x17000EB4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW346 | 0x17000EB8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW347 | 0x17000EBC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW348 | 0x17000EC0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW349 | 0x17000EC4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW350 | 0x17000EC8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW351 | 0x17000ECC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW352 | 0x17000ED0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW353 | 0x17000ED4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW354 | 0x17000ED8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW355 | 0x17000EDC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW356 | 0x17000EE0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW357 | 0x17000EE4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW358 | 0x17000EE8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW359 | 0x17000EEC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW360 | 0x17000EF0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW361 | 0x17000EF4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW362 | 0x17000EF8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW363 | 0x17000EFC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW364 | 0x17000F00 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW365 | 0x17000F04 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW366 | 0x17000F08 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW367 | 0x17000F0C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW368 | 0x17000F10 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW369 | 0x17000F14 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW370 | 0x17000F18 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW371 | 0x17000F1C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW372 | 0x17000F20 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW373 | 0x17000F24 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW374 | 0x17000F28 | FULL | USER FREE ROW3 |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|---|
| SFLASH_USER_FREE_ROW375 | 0x17000F2C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW376 | 0x17000F30 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW377 | 0x17000F34 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW378 | 0x17000F38 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW379 | 0x17000F3C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW380 | 0x17000F40 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW381 | 0x17000F44 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW382 | 0x17000F48 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW383 | 0x17000F4C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW384 | 0x17000F50 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW385 | 0x17000F54 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW386 | 0x17000F58 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW387 | 0x17000F5C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW388 | 0x17000F60 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW389 | 0x17000F64 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW390 | 0x17000F68 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW391 | 0x17000F6C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW392 | 0x17000F70 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW393 | 0x17000F74 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW394 | 0x17000F78 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW395 | 0x17000F7C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW396 | 0x17000F80 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW397 | 0x17000F84 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW398 | 0x17000F88 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW399 | 0x17000F8C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3100 | 0x17000F90 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3101 | 0x17000F94 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3102 | 0x17000F98 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3103 | 0x17000F9C | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3104 | 0x17000FA0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3105 | 0x17000FA4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3106 | 0x17000FA8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3107 | 0x17000FAC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3108 | 0x17000FB0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3109 | 0x17000FB4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3110 | 0x17000FB8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3111 | 0x17000FBC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3112 | 0x17000FC0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3113 | 0x17000FC4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3114 | 0x17000FC8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3115 | 0x17000FCC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3116 | 0x17000FD0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3117 | 0x17000FD4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3118 | 0x17000FD8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3119 | 0x17000FDC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3120 | 0x17000FE0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3121 | 0x17000FE4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3122 | 0x17000FE8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3123 | 0x17000FEC | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3124 | 0x17000FF0 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3125 | 0x17000FF4 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3126 | 0x17000FF8 | FULL | USER FREE ROW3 |
| SFLASH_USER_FREE_ROW3127 | 0x17000FFC | FULL | USER FREE ROW3 |
| SFLASH_SFLASH_UPDATE_MARKER0 | 0x17001800 | FULL | Markers for storing SFLASH programming states |
| SFLASH_SFLASH_UPDATE_MARKER1 | 0x17001804 | FULL | Markers for storing SFLASH programming states |
| SFLASH_FLASH_BOOT_OBJECT_SIZE | 0x17002000 | FULL | Flash Boot - Object Size |
| SFLASH_FLASH_BOOT_APP_ID | 0x17002004 | FULL | Flash Boot - Application ID/Version |
| SFLASH_FLASH_BOOT_VERSION_LOW | 0x17002018 | FULL | Flash Boot - Version Low |
| SFLASH_FLASH_BOOT_FAMILY_ID | 0x1700201C | FULL | Flash Boot - Family ID |
| SFLASH_PUBLIC_KEY0 | 0x17006400 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1 | 0x17006401 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2 | 0x17006402 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3 | 0x17006403 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY4 | 0x17006404 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY5 | 0x17006405 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY6 | 0x17006406 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY7 | 0x17006407 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY8 | 0x17006408 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY9 | 0x17006409 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY10 | 0x1700640A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY11 | 0x1700640B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY12 | 0x1700640C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY13 | 0x1700640D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY14 | 0x1700640E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY15 | 0x1700640F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY16 | 0x17006410 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY17 | 0x17006411 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY18 | 0x17006412 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY19 | 0x17006413 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY20 | 0x17006414 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY21 | 0x17006415 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY22 | 0x17006416 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY23 | 0x17006417 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY24 | 0x17006418 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY25 | 0x17006419 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY26 | 0x1700641A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY27 | 0x1700641B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY28 | 0x1700641C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY29 | 0x1700641D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY30 | 0x1700641E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY31 | 0x1700641F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY32 | 0x17006420 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY33 | 0x17006421 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY34 | 0x17006422 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY35 | 0x17006423 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY36 | 0x17006424 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY37 | 0x17006425 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY38 | 0x17006426 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY39 | 0x17006427 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY40 | 0x17006428 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY41 | 0x17006429 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY42 | 0x1700642A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY43 | 0x1700642B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY44 | 0x1700642C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY45 | 0x1700642D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY46 | 0x1700642E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY47 | 0x1700642F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY48 | 0x17006430 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY49 | 0x17006431 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY50 | 0x17006432 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY51 | 0x17006433 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY52 | 0x17006434 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY53 | 0x17006435 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY54 | 0x17006436 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY55 | 0x17006437 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY56 | 0x17006438 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY57 | 0x17006439 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY58 | 0x1700643A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY59 | 0x1700643B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY60 | 0x1700643C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY61 | 0x1700643D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY62 | 0x1700643E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY63 | 0x1700643F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY64 | 0x17006440 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY65 | 0x17006441 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY66 | 0x17006442 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY67 | 0x17006443 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY68 | 0x17006444 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY69 | 0x17006445 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY70 | 0x17006446 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY71 | 0x17006447 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY72 | 0x17006448 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY73 | 0x17006449 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY74 | 0x1700644A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY75 | 0x1700644B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY76 | 0x1700644C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY77 | 0x1700644D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY78 | 0x1700644E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY79 | 0x1700644F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY80 | 0x17006450 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY81 | 0x17006451 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY82 | 0x17006452 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY83 | 0x17006453 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY84 | 0x17006454 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY85 | 0x17006455 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY86 | 0x17006456 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY87 | 0x17006457 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY88 | 0x17006458 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY89 | 0x17006459 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY90 | 0x1700645A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY91 | 0x1700645B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY92 | 0x1700645C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY93 | 0x1700645D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY94 | 0x1700645E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY95 | 0x1700645F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY96 | 0x17006460 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY97 | 0x17006461 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY98 | 0x17006462 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY99 | 0x17006463 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY100 | 0x17006464 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY101 | 0x17006465 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY102 | 0x17006466 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY103 | 0x17006467 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY104 | 0x17006468 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY105 | 0x17006469 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY106 | 0x1700646A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY107 | 0x1700646B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY108 | 0x1700646C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY109 | 0x1700646D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY110 | 0x1700646E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY111 | 0x1700646F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY112 | 0x17006470 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY113 | 0x17006471 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY114 | 0x17006472 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY115 | 0x17006473 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY116 | 0x17006474 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY117 | 0x17006475 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY118 | 0x17006476 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY119 | 0x17006477 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY120 | 0x17006478 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY121 | 0x17006479 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY122 | 0x1700647A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY123 | 0x1700647B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY124 | 0x1700647C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY125 | 0x1700647D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY126 | 0x1700647E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY127 | 0x1700647F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY128 | 0x17006480 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY129 | 0x17006481 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY130 | 0x17006482 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY131 | 0x17006483 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY132 | 0x17006484 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY133 | 0x17006485 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY134 | 0x17006486 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY135 | 0x17006487 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY136 | 0x17006488 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY137 | 0x17006489 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY138 | 0x1700648A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY139 | 0x1700648B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY140 | 0x1700648C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY141 | 0x1700648D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY142 | 0x1700648E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY143 | 0x1700648F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY144 | 0x17006490 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY145 | 0x17006491 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY146 | 0x17006492 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY147 | 0x17006493 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY148 | 0x17006494 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY149 | 0x17006495 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY150 | 0x17006496 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY151 | 0x17006497 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY152 | 0x17006498 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY153 | 0x17006499 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY154 | 0x1700649A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY155 | 0x1700649B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY156 | 0x1700649C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY157 | 0x1700649D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY158 | 0x1700649E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY159 | 0x1700649F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY160 | 0x170064A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY161 | 0x170064A1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY162 | 0x170064A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY163 | 0x170064A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY164 | 0x170064A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY165 | 0x170064A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY166 | 0x170064A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY167 | 0x170064A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY168 | 0x170064A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY169 | 0x170064A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY170 | 0x170064AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY171 | 0x170064AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY172 | 0x170064AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY173 | 0x170064AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY174 | 0x170064AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY175 | 0x170064AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY176 | 0x170064B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY177 | 0x170064B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY178 | 0x170064B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY179 | 0x170064B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY180 | 0x170064B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY181 | 0x170064B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY182 | 0x170064B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY183 | 0x170064B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY184 | 0x170064B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY185 | 0x170064B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY186 | 0x170064BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY187 | 0x170064BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY188 | 0x170064BC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY189 | 0x170064BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY190 | 0x170064BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY191 | 0x170064BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY192 | 0x170064C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY193 | 0x170064C1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY194 | 0x170064C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY195 | 0x170064C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY196 | 0x170064C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY197 | 0x170064C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY198 | 0x170064C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY199 | 0x170064C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY200 | 0x170064C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY201 | 0x170064C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY202 | 0x170064CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY203 | 0x170064CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY204 | 0x170064CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY205 | 0x170064CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY206 | 0x170064CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY207 | 0x170064CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY208 | 0x170064D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY209 | 0x170064D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY210 | 0x170064D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY211 | 0x170064D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY212 | 0x170064D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY213 | 0x170064D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY214 | 0x170064D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY215 | 0x170064D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY216 | 0x170064D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY217 | 0x170064D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY218 | 0x170064DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY219 | 0x170064DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY220 | 0x170064DC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY221 | 0x170064DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY222 | 0x170064DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY223 | 0x170064DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY224 | 0x170064E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY225 | 0x170064E1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY226 | 0x170064E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY227 | 0x170064E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY228 | 0x170064E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY229 | 0x170064E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY230 | 0x170064E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY231 | 0x170064E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY232 | 0x170064E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY233 | 0x170064E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY234 | 0x170064EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY235 | 0x170064EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY236 | 0x170064EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY237 | 0x170064ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY238 | 0x170064EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY239 | 0x170064EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY240 | 0x170064F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY241 | 0x170064F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY242 | 0x170064F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY243 | 0x170064F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY244 | 0x170064F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY245 | 0x170064F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY246 | 0x170064F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY247 | 0x170064F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY248 | 0x170064F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY249 | 0x170064F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY250 | 0x170064FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY251 | 0x170064FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY252 | 0x170064FC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY253 | 0x170064FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY254 | 0x170064FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY255 | 0x170064FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY256 | 0x17006500 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY257 | 0x17006501 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY258 | 0x17006502 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY259 | 0x17006503 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY260 | 0x17006504 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY261 | 0x17006505 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY262 | 0x17006506 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY263 | 0x17006507 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY264 | 0x17006508 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY265 | 0x17006509 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY266 | 0x1700650A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY267 | 0x1700650B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY268 | 0x1700650C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY269 | 0x1700650D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY270 | 0x1700650E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY271 | 0x1700650F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY272 | 0x17006510 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY273 | 0x17006511 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY274 | 0x17006512 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY275 | 0x17006513 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY276 | 0x17006514 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY277 | 0x17006515 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY278 | 0x17006516 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY279 | 0x17006517 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY280 | 0x17006518 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY281 | 0x17006519 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY282 | 0x1700651A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY283 | 0x1700651B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY284 | 0x1700651C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY285 | 0x1700651D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY286 | 0x1700651E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY287 | 0x1700651F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY288 | 0x17006520 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY289 | 0x17006521 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY290 | 0x17006522 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY291 | 0x17006523 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY292 | 0x17006524 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY293 | 0x17006525 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY294 | 0x17006526 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY295 | 0x17006527 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY296 | 0x17006528 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY297 | 0x17006529 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY298 | 0x1700652A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY299 | 0x1700652B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY300 | 0x1700652C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY301 | 0x1700652D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY302 | 0x1700652E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY303 | 0x1700652F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY304 | 0x17006530 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY305 | 0x17006531 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY306 | 0x17006532 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY307 | 0x17006533 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY308 | 0x17006534 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY309 | 0x17006535 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY310 | 0x17006536 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY311 | 0x17006537 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY312 | 0x17006538 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY313 | 0x17006539 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY314 | 0x1700653A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY315 | 0x1700653B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY316 | 0x1700653C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY317 | 0x1700653D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY318 | 0x1700653E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY319 | 0x1700653F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY320 | 0x17006540 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY321 | 0x17006541 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY322 | 0x17006542 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY323 | 0x17006543 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY324 | 0x17006544 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY325 | 0x17006545 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY326 | 0x17006546 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY327 | 0x17006547 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY328 | 0x17006548 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY329 | 0x17006549 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY330 | 0x1700654A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY331 | 0x1700654B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY332 | 0x1700654C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY333 | 0x1700654D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY334 | 0x1700654E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY335 | 0x1700654F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY336 | 0x17006550 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY337 | 0x17006551 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY338 | 0x17006552 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY339 | 0x17006553 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY340 | 0x17006554 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY341 | 0x17006555 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY342 | 0x17006556 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY343 | 0x17006557 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY344 | 0x17006558 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY345 | 0x17006559 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY346 | 0x1700655A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY347 | 0x1700655B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY348 | 0x1700655C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY349 | 0x1700655D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY350 | 0x1700655E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY351 | 0x1700655F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY352 | 0x17006560 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY353 | 0x17006561 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY354 | 0x17006562 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY355 | 0x17006563 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY356 | 0x17006564 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY357 | 0x17006565 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY358 | 0x17006566 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY359 | 0x17006567 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY360 | 0x17006568 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY361 | 0x17006569 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY362 | 0x1700656A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY363 | 0x1700656B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY364 | 0x1700656C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY365 | 0x1700656D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY366 | 0x1700656E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY367 | 0x1700656F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY368 | 0x17006570 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY369 | 0x17006571 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY370 | 0x17006572 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY371 | 0x17006573 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY372 | 0x17006574 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY373 | 0x17006575 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY374 | 0x17006576 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY375 | 0x17006577 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY376 | 0x17006578 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY377 | 0x17006579 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY378 | 0x1700657A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY379 | 0x1700657B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY380 | 0x1700657C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY381 | 0x1700657D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY382 | 0x1700657E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY383 | 0x1700657F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY384 | 0x17006580 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY385 | 0x17006581 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY386 | 0x17006582 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY387 | 0x17006583 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY388 | 0x17006584 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY389 | 0x17006585 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY390 | 0x17006586 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY391 | 0x17006587 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY392 | 0x17006588 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY393 | 0x17006589 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY394 | 0x1700658A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY395 | 0x1700658B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY396 | 0x1700658C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY397 | 0x1700658D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY398 | 0x1700658E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY399 | 0x1700658F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY400 | 0x17006590 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY401 | 0x17006591 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY402 | 0x17006592 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY403 | 0x17006593 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY404 | 0x17006594 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY405 | 0x17006595 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY406 | 0x17006596 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY407 | 0x17006597 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY408 | 0x17006598 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY409 | 0x17006599 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY410 | 0x1700659A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY411 | 0x1700659B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY412 | 0x1700659C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY413 | 0x1700659D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY414 | 0x1700659E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY415 | 0x1700659F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY416 | 0x170065A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY417 | 0x170065A1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY418 | 0x170065A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY419 | 0x170065A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY420 | 0x170065A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY421 | 0x170065A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY422 | 0x170065A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY423 | 0x170065A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY424 | 0x170065A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY425 | 0x170065A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY426 | 0x170065AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY427 | 0x170065AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY428 | 0x170065AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY429 | 0x170065AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY430 | 0x170065AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY431 | 0x170065AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY432 | 0x170065B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY433 | 0x170065B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY434 | 0x170065B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY435 | 0x170065B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY436 | 0x170065B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY437 | 0x170065B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY438 | 0x170065B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY439 | 0x170065B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY440 | 0x170065B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY441 | 0x170065B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY442 | 0x170065BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY443 | 0x170065BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY444 | 0x170065BC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY445 | 0x170065BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY446 | 0x170065BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY447 | 0x170065BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY448 | 0x170065C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY449 | 0x170065C1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY450 | 0x170065C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY451 | 0x170065C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY452 | 0x170065C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY453 | 0x170065C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY454 | 0x170065C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY455 | 0x170065C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY456 | 0x170065C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY457 | 0x170065C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY458 | 0x170065CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY459 | 0x170065CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY460 | 0x170065CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY461 | 0x170065CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY462 | 0x170065CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY463 | 0x170065CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY464 | 0x170065D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY465 | 0x170065D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY466 | 0x170065D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY467 | 0x170065D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY468 | 0x170065D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY469 | 0x170065D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY470 | 0x170065D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY471 | 0x170065D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY472 | 0x170065D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY473 | 0x170065D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY474 | 0x170065DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY475 | 0x170065DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY476 | 0x170065DC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY477 | 0x170065DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY478 | 0x170065DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY479 | 0x170065DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY480 | 0x170065E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY481 | 0x170065E1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY482 | 0x170065E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY483 | 0x170065E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY484 | 0x170065E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY485 | 0x170065E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY486 | 0x170065E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY487 | 0x170065E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY488 | 0x170065E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY489 | 0x170065E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY490 | 0x170065EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY491 | 0x170065EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY492 | 0x170065EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY493 | 0x170065ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY494 | 0x170065EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY495 | 0x170065EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY496 | 0x170065F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY497 | 0x170065F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY498 | 0x170065F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY499 | 0x170065F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY500 | 0x170065F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY501 | 0x170065F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY502 | 0x170065F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY503 | 0x170065F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY504 | 0x170065F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY505 | 0x170065F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY506 | 0x170065FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY507 | 0x170065FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY508 | 0x170065FC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY509 | 0x170065FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY510 | 0x170065FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY511 | 0x170065FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY512 | 0x17006600 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY513 | 0x17006601 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY514 | 0x17006602 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY515 | 0x17006603 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY516 | 0x17006604 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY517 | 0x17006605 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY518 | 0x17006606 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY519 | 0x17006607 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY520 | 0x17006608 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY521 | 0x17006609 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY522 | 0x1700660A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY523 | 0x1700660B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY524 | 0x1700660C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY525 | 0x1700660D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY526 | 0x1700660E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY527 | 0x1700660F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY528 | 0x17006610 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY529 | 0x17006611 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY530 | 0x17006612 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY531 | 0x17006613 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY532 | 0x17006614 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY533 | 0x17006615 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY534 | 0x17006616 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY535 | 0x17006617 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY536 | 0x17006618 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY537 | 0x17006619 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY538 | 0x1700661A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY539 | 0x1700661B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY540 | 0x1700661C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY541 | 0x1700661D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY542 | 0x1700661E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY543 | 0x1700661F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY544 | 0x17006620 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY545 | 0x17006621 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY546 | 0x17006622 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY547 | 0x17006623 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY548 | 0x17006624 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY549 | 0x17006625 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY550 | 0x17006626 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY551 | 0x17006627 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY552 | 0x17006628 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY553 | 0x17006629 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY554 | 0x1700662A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY555 | 0x1700662B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY556 | 0x1700662C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY557 | 0x1700662D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY558 | 0x1700662E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY559 | 0x1700662F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY560 | 0x17006630 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY561 | 0x17006631 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY562 | 0x17006632 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY563 | 0x17006633 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY564 | 0x17006634 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY565 | 0x17006635 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY566 | 0x17006636 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY567 | 0x17006637 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY568 | 0x17006638 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY569 | 0x17006639 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY570 | 0x1700663A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY571 | 0x1700663B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY572 | 0x1700663C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY573 | 0x1700663D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY574 | 0x1700663E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY575 | 0x1700663F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY576 | 0x17006640 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY577 | 0x17006641 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY578 | 0x17006642 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY579 | 0x17006643 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY580 | 0x17006644 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY581 | 0x17006645 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY582 | 0x17006646 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY583 | 0x17006647 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY584 | 0x17006648 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY585 | 0x17006649 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY586 | 0x1700664A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY587 | 0x1700664B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY588 | 0x1700664C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY589 | 0x1700664D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY590 | 0x1700664E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY591 | 0x1700664F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY592 | 0x17006650 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY593 | 0x17006651 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY594 | 0x17006652 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY595 | 0x17006653 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY596 | 0x17006654 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY597 | 0x17006655 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY598 | 0x17006656 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY599 | 0x17006657 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY600 | 0x17006658 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY601 | 0x17006659 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY602 | 0x1700665A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY603 | 0x1700665B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY604 | 0x1700665C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY605 | 0x1700665D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY606 | 0x1700665E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY607 | 0x1700665F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY608 | 0x17006660 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY609 | 0x17006661 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY610 | 0x17006662 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY611 | 0x17006663 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY612 | 0x17006664 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY613 | 0x17006665 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY614 | 0x17006666 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY615 | 0x17006667 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY616 | 0x17006668 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY617 | 0x17006669 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY618 | 0x1700666A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY619 | 0x1700666B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY620 | 0x1700666C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY621 | 0x1700666D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY622 | 0x1700666E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY623 | 0x1700666F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY624 | 0x17006670 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY625 | 0x17006671 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY626 | 0x17006672 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY627 | 0x17006673 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY628 | 0x17006674 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY629 | 0x17006675 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY630 | 0x17006676 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY631 | 0x17006677 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY632 | 0x17006678 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY633 | 0x17006679 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY634 | 0x1700667A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY635 | 0x1700667B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY636 | 0x1700667C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY637 | 0x1700667D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY638 | 0x1700667E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY639 | 0x1700667F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY640 | 0x17006680 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY641 | 0x17006681 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY642 | 0x17006682 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY643 | 0x17006683 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY644 | 0x17006684 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY645 | 0x17006685 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY646 | 0x17006686 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY647 | 0x17006687 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY648 | 0x17006688 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY649 | 0x17006689 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY650 | 0x1700668A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY651 | 0x1700668B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY652 | 0x1700668C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY653 | 0x1700668D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY654 | 0x1700668E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY655 | 0x1700668F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY656 | 0x17006690 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY657 | 0x17006691 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY658 | 0x17006692 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY659 | 0x17006693 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY660 | 0x17006694 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY661 | 0x17006695 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY662 | 0x17006696 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY663 | 0x17006697 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY664 | 0x17006698 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY665 | 0x17006699 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY666 | 0x1700669A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY667 | 0x1700669B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY668 | 0x1700669C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY669 | 0x1700669D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY670 | 0x1700669E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY671 | 0x1700669F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY672 | 0x170066A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY673 | 0x170066A1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY674 | 0x170066A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY675 | 0x170066A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY676 | 0x170066A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY677 | 0x170066A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY678 | 0x170066A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY679 | 0x170066A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY680 | 0x170066A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY681 | 0x170066A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY682 | 0x170066AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY683 | 0x170066AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY684 | 0x170066AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY685 | 0x170066AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY686 | 0x170066AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY687 | 0x170066AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY688 | 0x170066B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY689 | 0x170066B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY690 | 0x170066B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY691 | 0x170066B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY692 | 0x170066B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY693 | 0x170066B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY694 | 0x170066B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY695 | 0x170066B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY696 | 0x170066B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY697 | 0x170066B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY698 | 0x170066BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY699 | 0x170066BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY700 | 0x170066BC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY701 | 0x170066BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY702 | 0x170066BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY703 | 0x170066BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY704 | 0x170066C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY705 | 0x170066C1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY706 | 0x170066C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY707 | 0x170066C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY708 | 0x170066C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY709 | 0x170066C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY710 | 0x170066C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY711 | 0x170066C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY712 | 0x170066C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY713 | 0x170066C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY714 | 0x170066CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY715 | 0x170066CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY716 | 0x170066CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY717 | 0x170066CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY718 | 0x170066CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY719 | 0x170066CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY720 | 0x170066D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY721 | 0x170066D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY722 | 0x170066D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY723 | 0x170066D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY724 | 0x170066D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY725 | 0x170066D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY726 | 0x170066D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY727 | 0x170066D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY728 | 0x170066D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY729 | 0x170066D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY730 | 0x170066DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY731 | 0x170066DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY732 | 0x170066DC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY733 | 0x170066DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY734 | 0x170066DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY735 | 0x170066DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY736 | 0x170066E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY737 | 0x170066E1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY738 | 0x170066E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY739 | 0x170066E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY740 | 0x170066E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY741 | 0x170066E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY742 | 0x170066E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY743 | 0x170066E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY744 | 0x170066E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY745 | 0x170066E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY746 | 0x170066EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY747 | 0x170066EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY748 | 0x170066EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY749 | 0x170066ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY750 | 0x170066EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY751 | 0x170066EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY752 | 0x170066F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY753 | 0x170066F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY754 | 0x170066F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY755 | 0x170066F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY756 | 0x170066F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY757 | 0x170066F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY758 | 0x170066F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY759 | 0x170066F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY760 | 0x170066F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY761 | 0x170066F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY762 | 0x170066FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY763 | 0x170066FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY764 | 0x170066FC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY765 | 0x170066FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY766 | 0x170066FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY767 | 0x170066FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY768 | 0x17006700 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY769 | 0x17006701 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY770 | 0x17006702 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY771 | 0x17006703 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY772 | 0x17006704 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY773 | 0x17006705 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY774 | 0x17006706 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY775 | 0x17006707 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY776 | 0x17006708 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY777 | 0x17006709 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY778 | 0x1700670A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY779 | 0x1700670B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY780 | 0x1700670C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY781 | 0x1700670D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY782 | 0x1700670E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY783 | 0x1700670F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY784 | 0x17006710 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY785 | 0x17006711 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY786 | 0x17006712 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY787 | 0x17006713 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY788 | 0x17006714 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY789 | 0x17006715 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY790 | 0x17006716 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY791 | 0x17006717 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY792 | 0x17006718 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY793 | 0x17006719 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY794 | 0x1700671A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY795 | 0x1700671B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY796 | 0x1700671C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY797 | 0x1700671D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY798 | 0x1700671E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY799 | 0x1700671F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY800 | 0x17006720 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY801 | 0x17006721 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY802 | 0x17006722 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY803 | 0x17006723 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY804 | 0x17006724 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY805 | 0x17006725 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY806 | 0x17006726 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY807 | 0x17006727 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY808 | 0x17006728 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY809 | 0x17006729 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY810 | 0x1700672A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY811 | 0x1700672B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY812 | 0x1700672C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY813 | 0x1700672D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY814 | 0x1700672E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY815 | 0x1700672F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY816 | 0x17006730 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY817 | 0x17006731 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY818 | 0x17006732 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY819 | 0x17006733 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY820 | 0x17006734 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY821 | 0x17006735 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY822 | 0x17006736 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY823 | 0x17006737 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY824 | 0x17006738 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY825 | 0x17006739 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY826 | 0x1700673A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY827 | 0x1700673B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY828 | 0x1700673C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY829 | 0x1700673D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY830 | 0x1700673E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY831 | 0x1700673F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY832 | 0x17006740 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY833 | 0x17006741 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY834 | 0x17006742 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY835 | 0x17006743 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY836 | 0x17006744 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY837 | 0x17006745 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY838 | 0x17006746 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY839 | 0x17006747 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY840 | 0x17006748 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY841 | 0x17006749 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY842 | 0x1700674A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY843 | 0x1700674B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY844 | 0x1700674C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY845 | 0x1700674D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY846 | 0x1700674E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY847 | 0x1700674F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY848 | 0x17006750 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY849 | 0x17006751 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY850 | 0x17006752 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY851 | 0x17006753 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY852 | 0x17006754 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY853 | 0x17006755 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY854 | 0x17006756 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY855 | 0x17006757 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY856 | 0x17006758 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY857 | 0x17006759 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY858 | 0x1700675A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY859 | 0x1700675B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY860 | 0x1700675C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY861 | 0x1700675D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY862 | 0x1700675E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY863 | 0x1700675F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY864 | 0x17006760 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY865 | 0x17006761 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY866 | 0x17006762 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY867 | 0x17006763 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY868 | 0x17006764 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY869 | 0x17006765 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY870 | 0x17006766 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY871 | 0x17006767 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY872 | 0x17006768 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY873 | 0x17006769 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY874 | 0x1700676A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY875 | 0x1700676B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY876 | 0x1700676C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY877 | 0x1700676D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY878 | 0x1700676E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY879 | 0x1700676F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY880 | 0x17006770 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY881 | 0x17006771 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY882 | 0x17006772 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY883 | 0x17006773 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY884 | 0x17006774 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY885 | 0x17006775 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY886 | 0x17006776 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY887 | 0x17006777 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY888 | 0x17006778 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY889 | 0x17006779 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY890 | 0x1700677A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY891 | 0x1700677B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY892 | 0x1700677C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY893 | 0x1700677D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY894 | 0x1700677E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY895 | 0x1700677F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY896 | 0x17006780 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY897 | 0x17006781 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY898 | 0x17006782 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY899 | 0x17006783 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY900 | 0x17006784 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY901 | 0x17006785 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY902 | 0x17006786 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY903 | 0x17006787 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY904 | 0x17006788 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY905 | 0x17006789 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY906 | 0x1700678A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY907 | 0x1700678B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY908 | 0x1700678C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY909 | 0x1700678D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY910 | 0x1700678E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY911 | 0x1700678F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY912 | 0x17006790 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY913 | 0x17006791 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY914 | 0x17006792 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY915 | 0x17006793 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY916 | 0x17006794 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY917 | 0x17006795 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY918 | 0x17006796 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY919 | 0x17006797 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY920 | 0x17006798 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY921 | 0x17006799 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY922 | 0x1700679A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY923 | 0x1700679B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY924 | 0x1700679C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY925 | 0x1700679D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY926 | 0x1700679E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY927 | 0x1700679F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY928 | 0x170067A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY929 | 0x170067A1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY930 | 0x170067A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY931 | 0x170067A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY932 | 0x170067A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY933 | 0x170067A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY934 | 0x170067A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY935 | 0x170067A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY936 | 0x170067A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY937 | 0x170067A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY938 | 0x170067AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY939 | 0x170067AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY940 | 0x170067AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY941 | 0x170067AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY942 | 0x170067AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY943 | 0x170067AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY944 | 0x170067B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY945 | 0x170067B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY946 | 0x170067B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY947 | 0x170067B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY948 | 0x170067B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY949 | 0x170067B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY950 | 0x170067B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY951 | 0x170067B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY952 | 0x170067B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY953 | 0x170067B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY954 | 0x170067BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY955 | 0x170067BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY956 | 0x170067BC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY957 | 0x170067BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY958 | 0x170067BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY959 | 0x170067BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY960 | 0x170067C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY961 | 0x170067C1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY962 | 0x170067C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY963 | 0x170067C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY964 | 0x170067C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY965 | 0x170067C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY966 | 0x170067C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY967 | 0x170067C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY968 | 0x170067C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY969 | 0x170067C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY970 | 0x170067CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY971 | 0x170067CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY972 | 0x170067CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY973 | 0x170067CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY974 | 0x170067CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY975 | 0x170067CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY976 | 0x170067D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY977 | 0x170067D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY978 | 0x170067D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY979 | 0x170067D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY980 | 0x170067D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY981 | 0x170067D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY982 | 0x170067D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY983 | 0x170067D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY984 | 0x170067D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY985 | 0x170067D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY986 | 0x170067DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY987 | 0x170067DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY988 | 0x170067DC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY989 | 0x170067DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY990 | 0x170067DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY991 | 0x170067DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY992 | 0x170067E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY993 | 0x170067E1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY994 | 0x170067E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY995 | 0x170067E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY996 | 0x170067E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY997 | 0x170067E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY998 | 0x170067E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY999 | 0x170067E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1000 | 0x170067E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1001 | 0x170067E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1002 | 0x170067EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1003 | 0x170067EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1004 | 0x170067EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1005 | 0x170067ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1006 | 0x170067EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1007 | 0x170067EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1008 | 0x170067F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1009 | 0x170067F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1010 | 0x170067F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1011 | 0x170067F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1012 | 0x170067F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1013 | 0x170067F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1014 | 0x170067F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1015 | 0x170067F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1016 | 0x170067F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1017 | 0x170067F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1018 | 0x170067FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1019 | 0x170067FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1020 | 0x170067FC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1021 | 0x170067FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1022 | 0x170067FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1023 | 0x170067FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1024 | 0x17006800 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1025 | 0x17006801 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1026 | 0x17006802 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1027 | 0x17006803 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1028 | 0x17006804 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1029 | 0x17006805 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1030 | 0x17006806 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1031 | 0x17006807 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1032 | 0x17006808 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1033 | 0x17006809 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1034 | 0x1700680A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1035 | 0x1700680B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1036 | 0x1700680C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1037 | 0x1700680D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1038 | 0x1700680E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1039 | 0x1700680F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1040 | 0x17006810 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1041 | 0x17006811 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1042 | 0x17006812 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1043 | 0x17006813 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1044 | 0x17006814 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1045 | 0x17006815 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1046 | 0x17006816 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1047 | 0x17006817 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1048 | 0x17006818 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1049 | 0x17006819 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1050 | 0x1700681A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1051 | 0x1700681B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1052 | 0x1700681C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1053 | 0x1700681D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1054 | 0x1700681E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1055 | 0x1700681F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1056 | 0x17006820 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1057 | 0x17006821 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1058 | 0x17006822 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1059 | 0x17006823 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1060 | 0x17006824 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1061 | 0x17006825 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1062 | 0x17006826 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1063 | 0x17006827 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1064 | 0x17006828 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1065 | 0x17006829 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1066 | 0x1700682A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1067 | 0x1700682B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1068 | 0x1700682C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1069 | 0x1700682D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1070 | 0x1700682E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1071 | 0x1700682F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1072 | 0x17006830 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1073 | 0x17006831 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1074 | 0x17006832 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1075 | 0x17006833 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1076 | 0x17006834 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1077 | 0x17006835 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1078 | 0x17006836 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1079 | 0x17006837 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1080 | 0x17006838 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1081 | 0x17006839 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1082 | 0x1700683A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1083 | 0x1700683B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1084 | 0x1700683C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1085 | 0x1700683D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1086 | 0x1700683E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1087 | 0x1700683F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1088 | 0x17006840 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1089 | 0x17006841 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1090 | 0x17006842 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1091 | 0x17006843 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1092 | 0x17006844 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1093 | 0x17006845 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1094 | 0x17006846 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1095 | 0x17006847 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1096 | 0x17006848 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1097 | 0x17006849 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1098 | 0x1700684A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1099 | 0x1700684B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1100 | 0x1700684C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1101 | 0x1700684D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1102 | 0x1700684E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1103 | 0x1700684F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1104 | 0x17006850 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1105 | 0x17006851 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1106 | 0x17006852 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1107 | 0x17006853 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1108 | 0x17006854 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1109 | 0x17006855 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1110 | 0x17006856 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1111 | 0x17006857 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1112 | 0x17006858 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1113 | 0x17006859 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1114 | 0x1700685A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1115 | 0x1700685B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1116 | 0x1700685C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1117 | 0x1700685D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1118 | 0x1700685E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1119 | 0x1700685F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1120 | 0x17006860 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1121 | 0x17006861 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1122 | 0x17006862 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1123 | 0x17006863 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1124 | 0x17006864 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1125 | 0x17006865 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1126 | 0x17006866 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1127 | 0x17006867 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1128 | 0x17006868 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1129 | 0x17006869 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1130 | 0x1700686A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1131 | 0x1700686B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1132 | 0x1700686C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1133 | 0x1700686D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1134 | 0x1700686E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1135 | 0x1700686F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1136 | 0x17006870 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1137 | 0x17006871 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1138 | 0x17006872 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1139 | 0x17006873 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1140 | 0x17006874 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1141 | 0x17006875 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1142 | 0x17006876 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1143 | 0x17006877 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1144 | 0x17006878 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1145 | 0x17006879 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1146 | 0x1700687A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1147 | 0x1700687B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1148 | 0x1700687C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1149 | 0x1700687D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1150 | 0x1700687E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1151 | 0x1700687F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1152 | 0x17006880 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1153 | 0x17006881 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1154 | 0x17006882 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1155 | 0x17006883 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1156 | 0x17006884 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1157 | 0x17006885 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1158 | 0x17006886 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1159 | 0x17006887 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1160 | 0x17006888 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1161 | 0x17006889 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1162 | 0x1700688A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1163 | 0x1700688B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1164 | 0x1700688C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1165 | 0x1700688D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1166 | 0x1700688E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1167 | 0x1700688F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1168 | 0x17006890 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1169 | 0x17006891 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1170 | 0x17006892 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1171 | 0x17006893 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1172 | 0x17006894 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1173 | 0x17006895 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1174 | 0x17006896 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1175 | 0x17006897 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1176 | 0x17006898 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1177 | 0x17006899 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1178 | 0x1700689A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1179 | 0x1700689B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1180 | 0x1700689C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1181 | 0x1700689D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1182 | 0x1700689E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1183 | 0x1700689F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1184 | 0x170068A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1185 | 0x170068A1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1186 | 0x170068A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1187 | 0x170068A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1188 | 0x170068A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1189 | 0x170068A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1190 | 0x170068A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1191 | 0x170068A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1192 | 0x170068A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1193 | 0x170068A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1194 | 0x170068AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1195 | 0x170068AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1196 | 0x170068AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1197 | 0x170068AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1198 | 0x170068AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1199 | 0x170068AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1200 | 0x170068B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1201 | 0x170068B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1202 | 0x170068B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1203 | 0x170068B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1204 | 0x170068B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1205 | 0x170068B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1206 | 0x170068B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1207 | 0x170068B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1208 | 0x170068B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1209 | 0x170068B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1210 | 0x170068BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1211 | 0x170068BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1212 | 0x170068BC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1213 | 0x170068BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1214 | 0x170068BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1215 | 0x170068BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1216 | 0x170068C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1217 | 0x170068C1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1218 | 0x170068C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1219 | 0x170068C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1220 | 0x170068C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1221 | 0x170068C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1222 | 0x170068C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1223 | 0x170068C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1224 | 0x170068C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1225 | 0x170068C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1226 | 0x170068CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1227 | 0x170068CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1228 | 0x170068CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1229 | 0x170068CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1230 | 0x170068CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1231 | 0x170068CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1232 | 0x170068D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1233 | 0x170068D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1234 | 0x170068D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1235 | 0x170068D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1236 | 0x170068D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1237 | 0x170068D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1238 | 0x170068D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1239 | 0x170068D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1240 | 0x170068D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1241 | 0x170068D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1242 | 0x170068DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1243 | 0x170068DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1244 | 0x170068DC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1245 | 0x170068DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1246 | 0x170068DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1247 | 0x170068DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1248 | 0x170068E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1249 | 0x170068E1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1250 | 0x170068E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1251 | 0x170068E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1252 | 0x170068E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1253 | 0x170068E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1254 | 0x170068E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1255 | 0x170068E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1256 | 0x170068E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1257 | 0x170068E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1258 | 0x170068EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1259 | 0x170068EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1260 | 0x170068EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1261 | 0x170068ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1262 | 0x170068EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1263 | 0x170068EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1264 | 0x170068F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1265 | 0x170068F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1266 | 0x170068F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1267 | 0x170068F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1268 | 0x170068F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1269 | 0x170068F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1270 | 0x170068F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1271 | 0x170068F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1272 | 0x170068F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1273 | 0x170068F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1274 | 0x170068FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1275 | 0x170068FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1276 | 0x170068FC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1277 | 0x170068FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1278 | 0x170068FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1279 | 0x170068FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1280 | 0x17006900 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1281 | 0x17006901 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1282 | 0x17006902 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1283 | 0x17006903 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1284 | 0x17006904 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1285 | 0x17006905 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1286 | 0x17006906 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1287 | 0x17006907 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1288 | 0x17006908 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1289 | 0x17006909 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1290 | 0x1700690A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1291 | 0x1700690B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1292 | 0x1700690C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1293 | 0x1700690D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1294 | 0x1700690E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1295 | 0x1700690F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1296 | 0x17006910 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1297 | 0x17006911 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1298 | 0x17006912 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1299 | 0x17006913 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1300 | 0x17006914 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1301 | 0x17006915 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1302 | 0x17006916 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1303 | 0x17006917 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1304 | 0x17006918 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1305 | 0x17006919 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1306 | 0x1700691A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1307 | 0x1700691B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1308 | 0x1700691C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1309 | 0x1700691D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1310 | 0x1700691E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1311 | 0x1700691F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1312 | 0x17006920 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1313 | 0x17006921 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1314 | 0x17006922 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1315 | 0x17006923 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1316 | 0x17006924 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1317 | 0x17006925 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1318 | 0x17006926 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1319 | 0x17006927 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1320 | 0x17006928 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1321 | 0x17006929 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1322 | 0x1700692A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1323 | 0x1700692B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1324 | 0x1700692C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1325 | 0x1700692D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1326 | 0x1700692E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1327 | 0x1700692F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1328 | 0x17006930 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1329 | 0x17006931 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1330 | 0x17006932 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1331 | 0x17006933 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1332 | 0x17006934 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1333 | 0x17006935 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1334 | 0x17006936 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1335 | 0x17006937 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1336 | 0x17006938 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1337 | 0x17006939 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1338 | 0x1700693A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1339 | 0x1700693B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1340 | 0x1700693C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1341 | 0x1700693D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1342 | 0x1700693E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1343 | 0x1700693F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1344 | 0x17006940 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1345 | 0x17006941 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1346 | 0x17006942 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1347 | 0x17006943 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1348 | 0x17006944 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1349 | 0x17006945 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1350 | 0x17006946 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1351 | 0x17006947 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1352 | 0x17006948 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1353 | 0x17006949 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1354 | 0x1700694A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1355 | 0x1700694B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1356 | 0x1700694C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1357 | 0x1700694D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1358 | 0x1700694E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1359 | 0x1700694F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1360 | 0x17006950 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1361 | 0x17006951 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1362 | 0x17006952 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1363 | 0x17006953 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1364 | 0x17006954 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1365 | 0x17006955 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1366 | 0x17006956 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1367 | 0x17006957 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1368 | 0x17006958 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1369 | 0x17006959 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1370 | 0x1700695A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1371 | 0x1700695B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1372 | 0x1700695C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1373 | 0x1700695D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1374 | 0x1700695E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1375 | 0x1700695F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1376 | 0x17006960 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1377 | 0x17006961 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1378 | 0x17006962 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1379 | 0x17006963 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1380 | 0x17006964 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1381 | 0x17006965 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1382 | 0x17006966 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1383 | 0x17006967 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1384 | 0x17006968 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1385 | 0x17006969 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1386 | 0x1700696A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1387 | 0x1700696B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1388 | 0x1700696C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1389 | 0x1700696D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1390 | 0x1700696E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1391 | 0x1700696F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1392 | 0x17006970 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1393 | 0x17006971 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1394 | 0x17006972 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1395 | 0x17006973 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1396 | 0x17006974 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1397 | 0x17006975 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1398 | 0x17006976 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1399 | 0x17006977 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1400 | 0x17006978 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1401 | 0x17006979 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1402 | 0x1700697A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1403 | 0x1700697B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1404 | 0x1700697C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1405 | 0x1700697D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1406 | 0x1700697E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1407 | 0x1700697F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1408 | 0x17006980 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1409 | 0x17006981 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1410 | 0x17006982 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1411 | 0x17006983 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1412 | 0x17006984 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1413 | 0x17006985 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1414 | 0x17006986 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1415 | 0x17006987 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1416 | 0x17006988 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1417 | 0x17006989 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1418 | 0x1700698A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1419 | 0x1700698B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1420 | 0x1700698C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1421 | 0x1700698D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1422 | 0x1700698E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1423 | 0x1700698F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1424 | 0x17006990 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1425 | 0x17006991 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1426 | 0x17006992 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1427 | 0x17006993 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1428 | 0x17006994 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1429 | 0x17006995 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1430 | 0x17006996 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1431 | 0x17006997 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1432 | 0x17006998 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1433 | 0x17006999 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1434 | 0x1700699A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1435 | 0x1700699B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1436 | 0x1700699C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1437 | 0x1700699D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1438 | 0x1700699E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1439 | 0x1700699F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1440 | 0x170069A0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1441 | 0x170069A1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1442 | 0x170069A2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1443 | 0x170069A3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1444 | 0x170069A4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1445 | 0x170069A5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1446 | 0x170069A6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1447 | 0x170069A7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1448 | 0x170069A8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1449 | 0x170069A9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1450 | 0x170069AA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1451 | 0x170069AB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1452 | 0x170069AC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1453 | 0x170069AD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1454 | 0x170069AE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1455 | 0x170069AF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1456 | 0x170069B0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1457 | 0x170069B1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1458 | 0x170069B2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1459 | 0x170069B3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1460 | 0x170069B4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1461 | 0x170069B5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1462 | 0x170069B6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1463 | 0x170069B7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1464 | 0x170069B8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1465 | 0x170069B9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1466 | 0x170069BA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1467 | 0x170069BB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1468 | 0x170069BC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1469 | 0x170069BD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1470 | 0x170069BE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1471 | 0x170069BF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1472 | 0x170069C0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1473 | 0x170069C1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1474 | 0x170069C2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1475 | 0x170069C3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1476 | 0x170069C4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1477 | 0x170069C5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1478 | 0x170069C6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1479 | 0x170069C7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1480 | 0x170069C8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1481 | 0x170069C9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1482 | 0x170069CA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1483 | 0x170069CB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1484 | 0x170069CC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1485 | 0x170069CD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1486 | 0x170069CE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1487 | 0x170069CF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1488 | 0x170069D0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1489 | 0x170069D1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1490 | 0x170069D2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1491 | 0x170069D3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1492 | 0x170069D4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1493 | 0x170069D5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1494 | 0x170069D6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1495 | 0x170069D7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1496 | 0x170069D8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1497 | 0x170069D9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1498 | 0x170069DA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1499 | 0x170069DB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1500 | 0x170069DC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1501 | 0x170069DD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1502 | 0x170069DE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1503 | 0x170069DF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1504 | 0x170069E0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1505 | 0x170069E1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1506 | 0x170069E2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1507 | 0x170069E3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1508 | 0x170069E4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1509 | 0x170069E5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1510 | 0x170069E6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1511 | 0x170069E7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1512 | 0x170069E8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1513 | 0x170069E9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1514 | 0x170069EA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1515 | 0x170069EB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1516 | 0x170069EC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1517 | 0x170069ED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1518 | 0x170069EE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1519 | 0x170069EF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1520 | 0x170069F0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1521 | 0x170069F1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1522 | 0x170069F2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1523 | 0x170069F3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1524 | 0x170069F4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1525 | 0x170069F5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1526 | 0x170069F6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1527 | 0x170069F7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1528 | 0x170069F8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1529 | 0x170069F9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1530 | 0x170069FA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1531 | 0x170069FB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1532 | 0x170069FC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1533 | 0x170069FD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1534 | 0x170069FE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1535 | 0x170069FF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1536 | 0x17006A00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1537 | 0x17006A01 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1538 | 0x17006A02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1539 | 0x17006A03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1540 | 0x17006A04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1541 | 0x17006A05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1542 | 0x17006A06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1543 | 0x17006A07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1544 | 0x17006A08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1545 | 0x17006A09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1546 | 0x17006A0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1547 | 0x17006A0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1548 | 0x17006A0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1549 | 0x17006A0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1550 | 0x17006A0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1551 | 0x17006A0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1552 | 0x17006A10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1553 | 0x17006A11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1554 | 0x17006A12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1555 | 0x17006A13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1556 | 0x17006A14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1557 | 0x17006A15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1558 | 0x17006A16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1559 | 0x17006A17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1560 | 0x17006A18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1561 | 0x17006A19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1562 | 0x17006A1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1563 | 0x17006A1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1564 | 0x17006A1C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1565 | 0x17006A1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1566 | 0x17006A1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1567 | 0x17006A1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1568 | 0x17006A20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1569 | 0x17006A21 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1570 | 0x17006A22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1571 | 0x17006A23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1572 | 0x17006A24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1573 | 0x17006A25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1574 | 0x17006A26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1575 | 0x17006A27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1576 | 0x17006A28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1577 | 0x17006A29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1578 | 0x17006A2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1579 | 0x17006A2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1580 | 0x17006A2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1581 | 0x17006A2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1582 | 0x17006A2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1583 | 0x17006A2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1584 | 0x17006A30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1585 | 0x17006A31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1586 | 0x17006A32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1587 | 0x17006A33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1588 | 0x17006A34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1589 | 0x17006A35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1590 | 0x17006A36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1591 | 0x17006A37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1592 | 0x17006A38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1593 | 0x17006A39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1594 | 0x17006A3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1595 | 0x17006A3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1596 | 0x17006A3C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1597 | 0x17006A3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1598 | 0x17006A3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1599 | 0x17006A3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1600 | 0x17006A40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1601 | 0x17006A41 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1602 | 0x17006A42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1603 | 0x17006A43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1604 | 0x17006A44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1605 | 0x17006A45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1606 | 0x17006A46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1607 | 0x17006A47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1608 | 0x17006A48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1609 | 0x17006A49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1610 | 0x17006A4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1611 | 0x17006A4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1612 | 0x17006A4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1613 | 0x17006A4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1614 | 0x17006A4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1615 | 0x17006A4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1616 | 0x17006A50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1617 | 0x17006A51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1618 | 0x17006A52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1619 | 0x17006A53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1620 | 0x17006A54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1621 | 0x17006A55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1622 | 0x17006A56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1623 | 0x17006A57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1624 | 0x17006A58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1625 | 0x17006A59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1626 | 0x17006A5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1627 | 0x17006A5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1628 | 0x17006A5C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1629 | 0x17006A5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1630 | 0x17006A5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1631 | 0x17006A5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1632 | 0x17006A60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1633 | 0x17006A61 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1634 | 0x17006A62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1635 | 0x17006A63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1636 | 0x17006A64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1637 | 0x17006A65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1638 | 0x17006A66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1639 | 0x17006A67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1640 | 0x17006A68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1641 | 0x17006A69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1642 | 0x17006A6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1643 | 0x17006A6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1644 | 0x17006A6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1645 | 0x17006A6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1646 | 0x17006A6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1647 | 0x17006A6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1648 | 0x17006A70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1649 | 0x17006A71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1650 | 0x17006A72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1651 | 0x17006A73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1652 | 0x17006A74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1653 | 0x17006A75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1654 | 0x17006A76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1655 | 0x17006A77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1656 | 0x17006A78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1657 | 0x17006A79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1658 | 0x17006A7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1659 | 0x17006A7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1660 | 0x17006A7C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1661 | 0x17006A7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1662 | 0x17006A7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1663 | 0x17006A7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1664 | 0x17006A80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1665 | 0x17006A81 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1666 | 0x17006A82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1667 | 0x17006A83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1668 | 0x17006A84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1669 | 0x17006A85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1670 | 0x17006A86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1671 | 0x17006A87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1672 | 0x17006A88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1673 | 0x17006A89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1674 | 0x17006A8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1675 | 0x17006A8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1676 | 0x17006A8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1677 | 0x17006A8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1678 | 0x17006A8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1679 | 0x17006A8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1680 | 0x17006A90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1681 | 0x17006A91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1682 | 0x17006A92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1683 | 0x17006A93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1684 | 0x17006A94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1685 | 0x17006A95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1686 | 0x17006A96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1687 | 0x17006A97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1688 | 0x17006A98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1689 | 0x17006A99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1690 | 0x17006A9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1691 | 0x17006A9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1692 | 0x17006A9C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1693 | 0x17006A9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1694 | 0x17006A9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1695 | 0x17006A9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1696 | 0x17006AA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1697 | 0x17006AA1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1698 | 0x17006AA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1699 | 0x17006AA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1700 | 0x17006AA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1701 | 0x17006AA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1702 | 0x17006AA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1703 | 0x17006AA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1704 | 0x17006AA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1705 | 0x17006AA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1706 | 0x17006AAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1707 | 0x17006AAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1708 | 0x17006AAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1709 | 0x17006AAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1710 | 0x17006AAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1711 | 0x17006AAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1712 | 0x17006AB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1713 | 0x17006AB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1714 | 0x17006AB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1715 | 0x17006AB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1716 | 0x17006AB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1717 | 0x17006AB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1718 | 0x17006AB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1719 | 0x17006AB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1720 | 0x17006AB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1721 | 0x17006AB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1722 | 0x17006ABA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1723 | 0x17006ABB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1724 | 0x17006ABC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1725 | 0x17006ABD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1726 | 0x17006ABE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1727 | 0x17006ABF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1728 | 0x17006AC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1729 | 0x17006AC1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1730 | 0x17006AC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1731 | 0x17006AC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1732 | 0x17006AC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1733 | 0x17006AC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1734 | 0x17006AC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1735 | 0x17006AC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1736 | 0x17006AC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1737 | 0x17006AC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1738 | 0x17006ACA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1739 | 0x17006ACB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1740 | 0x17006ACC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1741 | 0x17006ACD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1742 | 0x17006ACE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1743 | 0x17006ACF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1744 | 0x17006AD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1745 | 0x17006AD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1746 | 0x17006AD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1747 | 0x17006AD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1748 | 0x17006AD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1749 | 0x17006AD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1750 | 0x17006AD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1751 | 0x17006AD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1752 | 0x17006AD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1753 | 0x17006AD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1754 | 0x17006ADA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1755 | 0x17006ADB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1756 | 0x17006ADC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1757 | 0x17006ADD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1758 | 0x17006ADE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1759 | 0x17006ADF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1760 | 0x17006AE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1761 | 0x17006AE1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1762 | 0x17006AE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1763 | 0x17006AE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1764 | 0x17006AE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1765 | 0x17006AE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1766 | 0x17006AE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1767 | 0x17006AE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1768 | 0x17006AE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1769 | 0x17006AE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1770 | 0x17006AEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1771 | 0x17006AEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1772 | 0x17006AEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1773 | 0x17006AED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1774 | 0x17006AEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1775 | 0x17006AEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1776 | 0x17006AF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1777 | 0x17006AF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1778 | 0x17006AF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1779 | 0x17006AF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1780 | 0x17006AF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1781 | 0x17006AF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1782 | 0x17006AF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1783 | 0x17006AF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1784 | 0x17006AF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1785 | 0x17006AF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1786 | 0x17006AFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1787 | 0x17006AFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1788 | 0x17006AFC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1789 | 0x17006AFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1790 | 0x17006AFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1791 | 0x17006AFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1792 | 0x17006B00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1793 | 0x17006B01 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1794 | 0x17006B02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1795 | 0x17006B03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1796 | 0x17006B04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1797 | 0x17006B05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1798 | 0x17006B06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1799 | 0x17006B07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1800 | 0x17006B08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1801 | 0x17006B09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1802 | 0x17006B0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1803 | 0x17006B0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1804 | 0x17006B0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1805 | 0x17006B0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1806 | 0x17006B0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1807 | 0x17006B0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1808 | 0x17006B10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1809 | 0x17006B11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1810 | 0x17006B12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1811 | 0x17006B13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1812 | 0x17006B14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1813 | 0x17006B15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1814 | 0x17006B16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1815 | 0x17006B17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1816 | 0x17006B18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1817 | 0x17006B19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1818 | 0x17006B1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1819 | 0x17006B1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1820 | 0x17006B1C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1821 | 0x17006B1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1822 | 0x17006B1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1823 | 0x17006B1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1824 | 0x17006B20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1825 | 0x17006B21 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1826 | 0x17006B22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1827 | 0x17006B23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1828 | 0x17006B24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1829 | 0x17006B25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1830 | 0x17006B26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1831 | 0x17006B27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1832 | 0x17006B28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1833 | 0x17006B29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1834 | 0x17006B2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1835 | 0x17006B2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1836 | 0x17006B2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1837 | 0x17006B2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1838 | 0x17006B2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1839 | 0x17006B2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1840 | 0x17006B30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1841 | 0x17006B31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1842 | 0x17006B32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1843 | 0x17006B33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1844 | 0x17006B34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1845 | 0x17006B35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1846 | 0x17006B36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1847 | 0x17006B37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1848 | 0x17006B38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1849 | 0x17006B39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1850 | 0x17006B3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1851 | 0x17006B3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1852 | 0x17006B3C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1853 | 0x17006B3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1854 | 0x17006B3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1855 | 0x17006B3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1856 | 0x17006B40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1857 | 0x17006B41 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1858 | 0x17006B42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1859 | 0x17006B43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1860 | 0x17006B44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1861 | 0x17006B45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1862 | 0x17006B46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1863 | 0x17006B47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1864 | 0x17006B48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1865 | 0x17006B49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1866 | 0x17006B4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1867 | 0x17006B4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1868 | 0x17006B4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1869 | 0x17006B4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1870 | 0x17006B4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1871 | 0x17006B4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1872 | 0x17006B50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1873 | 0x17006B51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1874 | 0x17006B52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1875 | 0x17006B53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1876 | 0x17006B54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1877 | 0x17006B55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1878 | 0x17006B56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1879 | 0x17006B57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1880 | 0x17006B58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1881 | 0x17006B59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1882 | 0x17006B5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1883 | 0x17006B5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1884 | 0x17006B5C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1885 | 0x17006B5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1886 | 0x17006B5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1887 | 0x17006B5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1888 | 0x17006B60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1889 | 0x17006B61 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1890 | 0x17006B62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1891 | 0x17006B63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1892 | 0x17006B64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1893 | 0x17006B65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1894 | 0x17006B66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1895 | 0x17006B67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1896 | 0x17006B68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1897 | 0x17006B69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1898 | 0x17006B6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1899 | 0x17006B6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1900 | 0x17006B6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1901 | 0x17006B6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1902 | 0x17006B6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1903 | 0x17006B6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1904 | 0x17006B70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1905 | 0x17006B71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1906 | 0x17006B72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1907 | 0x17006B73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1908 | 0x17006B74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1909 | 0x17006B75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1910 | 0x17006B76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1911 | 0x17006B77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1912 | 0x17006B78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1913 | 0x17006B79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1914 | 0x17006B7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1915 | 0x17006B7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1916 | 0x17006B7C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1917 | 0x17006B7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1918 | 0x17006B7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1919 | 0x17006B7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1920 | 0x17006B80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1921 | 0x17006B81 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1922 | 0x17006B82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1923 | 0x17006B83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1924 | 0x17006B84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1925 | 0x17006B85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1926 | 0x17006B86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1927 | 0x17006B87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1928 | 0x17006B88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1929 | 0x17006B89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1930 | 0x17006B8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1931 | 0x17006B8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1932 | 0x17006B8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1933 | 0x17006B8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1934 | 0x17006B8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1935 | 0x17006B8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1936 | 0x17006B90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1937 | 0x17006B91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1938 | 0x17006B92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1939 | 0x17006B93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1940 | 0x17006B94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1941 | 0x17006B95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1942 | 0x17006B96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1943 | 0x17006B97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1944 | 0x17006B98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1945 | 0x17006B99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1946 | 0x17006B9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1947 | 0x17006B9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1948 | 0x17006B9C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1949 | 0x17006B9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1950 | 0x17006B9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1951 | 0x17006B9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1952 | 0x17006BA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1953 | 0x17006BA1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1954 | 0x17006BA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1955 | 0x17006BA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1956 | 0x17006BA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1957 | 0x17006BA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1958 | 0x17006BA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1959 | 0x17006BA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1960 | 0x17006BA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1961 | 0x17006BA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1962 | 0x17006BAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1963 | 0x17006BAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1964 | 0x17006BAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1965 | 0x17006BAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1966 | 0x17006BAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1967 | 0x17006BAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1968 | 0x17006BB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1969 | 0x17006BB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1970 | 0x17006BB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1971 | 0x17006BB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1972 | 0x17006BB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1973 | 0x17006BB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1974 | 0x17006BB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1975 | 0x17006BB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1976 | 0x17006BB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1977 | 0x17006BB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1978 | 0x17006BBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1979 | 0x17006BBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1980 | 0x17006BBC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1981 | 0x17006BBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1982 | 0x17006BBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1983 | 0x17006BBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1984 | 0x17006BC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1985 | 0x17006BC1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY1986 | 0x17006BC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1987 | 0x17006BC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1988 | 0x17006BC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1989 | 0x17006BC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1990 | 0x17006BC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1991 | 0x17006BC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1992 | 0x17006BC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1993 | 0x17006BC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1994 | 0x17006BCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1995 | 0x17006BCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1996 | 0x17006BCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1997 | 0x17006BCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1998 | 0x17006BCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY1999 | 0x17006BCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2000 | 0x17006BD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2001 | 0x17006BD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2002 | 0x17006BD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2003 | 0x17006BD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2004 | 0x17006BD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2005 | 0x17006BD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2006 | 0x17006BD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2007 | 0x17006BD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2008 | 0x17006BD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2009 | 0x17006BD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2010 | 0x17006BDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2011 | 0x17006BDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2012 | 0x17006BDC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2013 | 0x17006BDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2014 | 0x17006BDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2015 | 0x17006BDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2016 | 0x17006BE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2017 | 0x17006BE1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2018 | 0x17006BE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2019 | 0x17006BE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2020 | 0x17006BE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2021 | 0x17006BE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2022 | 0x17006BE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2023 | 0x17006BE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2024 | 0x17006BE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2025 | 0x17006BE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2026 | 0x17006BEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2027 | 0x17006BEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2028 | 0x17006BEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2029 | 0x17006BED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2030 | 0x17006BEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2031 | 0x17006BEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2032 | 0x17006BF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2033 | 0x17006BF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2034 | 0x17006BF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2035 | 0x17006BF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2036 | 0x17006BF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2037 | 0x17006BF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2038 | 0x17006BF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2039 | 0x17006BF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2040 | 0x17006BF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2041 | 0x17006BF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2042 | 0x17006BFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2043 | 0x17006BFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2044 | 0x17006BFC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2045 | 0x17006BFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2046 | 0x17006BFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2047 | 0x17006BFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2048 | 0x17006C00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2049 | 0x17006C01 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2050 | 0x17006C02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2051 | 0x17006C03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2052 | 0x17006C04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2053 | 0x17006C05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2054 | 0x17006C06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2055 | 0x17006C07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2056 | 0x17006C08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2057 | 0x17006C09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2058 | 0x17006C0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2059 | 0x17006C0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2060 | 0x17006C0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2061 | 0x17006C0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2062 | 0x17006C0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2063 | 0x17006C0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2064 | 0x17006C10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2065 | 0x17006C11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2066 | 0x17006C12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2067 | 0x17006C13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2068 | 0x17006C14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2069 | 0x17006C15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2070 | 0x17006C16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2071 | 0x17006C17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2072 | 0x17006C18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2073 | 0x17006C19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2074 | 0x17006C1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2075 | 0x17006C1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2076 | 0x17006C1C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2077 | 0x17006C1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2078 | 0x17006C1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2079 | 0x17006C1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2080 | 0x17006C20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2081 | 0x17006C21 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2082 | 0x17006C22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2083 | 0x17006C23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2084 | 0x17006C24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2085 | 0x17006C25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2086 | 0x17006C26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2087 | 0x17006C27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2088 | 0x17006C28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2089 | 0x17006C29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2090 | 0x17006C2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2091 | 0x17006C2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2092 | 0x17006C2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2093 | 0x17006C2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2094 | 0x17006C2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2095 | 0x17006C2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2096 | 0x17006C30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2097 | 0x17006C31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2098 | 0x17006C32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2099 | 0x17006C33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2100 | 0x17006C34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2101 | 0x17006C35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2102 | 0x17006C36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2103 | 0x17006C37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2104 | 0x17006C38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2105 | 0x17006C39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2106 | 0x17006C3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2107 | 0x17006C3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2108 | 0x17006C3C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2109 | 0x17006C3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2110 | 0x17006C3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2111 | 0x17006C3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2112 | 0x17006C40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2113 | 0x17006C41 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2114 | 0x17006C42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2115 | 0x17006C43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2116 | 0x17006C44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2117 | 0x17006C45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2118 | 0x17006C46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2119 | 0x17006C47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2120 | 0x17006C48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2121 | 0x17006C49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2122 | 0x17006C4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2123 | 0x17006C4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2124 | 0x17006C4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2125 | 0x17006C4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2126 | 0x17006C4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2127 | 0x17006C4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2128 | 0x17006C50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2129 | 0x17006C51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2130 | 0x17006C52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2131 | 0x17006C53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2132 | 0x17006C54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2133 | 0x17006C55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2134 | 0x17006C56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2135 | 0x17006C57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2136 | 0x17006C58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2137 | 0x17006C59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2138 | 0x17006C5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2139 | 0x17006C5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2140 | 0x17006C5C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2141 | 0x17006C5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2142 | 0x17006C5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2143 | 0x17006C5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2144 | 0x17006C60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2145 | 0x17006C61 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2146 | 0x17006C62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2147 | 0x17006C63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2148 | 0x17006C64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2149 | 0x17006C65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2150 | 0x17006C66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2151 | 0x17006C67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2152 | 0x17006C68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2153 | 0x17006C69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2154 | 0x17006C6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2155 | 0x17006C6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2156 | 0x17006C6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2157 | 0x17006C6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2158 | 0x17006C6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2159 | 0x17006C6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2160 | 0x17006C70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2161 | 0x17006C71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2162 | 0x17006C72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2163 | 0x17006C73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2164 | 0x17006C74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2165 | 0x17006C75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2166 | 0x17006C76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2167 | 0x17006C77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2168 | 0x17006C78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2169 | 0x17006C79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2170 | 0x17006C7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2171 | 0x17006C7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2172 | 0x17006C7C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2173 | 0x17006C7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2174 | 0x17006C7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2175 | 0x17006C7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2176 | 0x17006C80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2177 | 0x17006C81 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2178 | 0x17006C82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2179 | 0x17006C83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2180 | 0x17006C84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2181 | 0x17006C85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2182 | 0x17006C86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2183 | 0x17006C87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2184 | 0x17006C88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2185 | 0x17006C89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2186 | 0x17006C8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2187 | 0x17006C8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2188 | 0x17006C8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2189 | 0x17006C8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2190 | 0x17006C8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2191 | 0x17006C8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2192 | 0x17006C90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2193 | 0x17006C91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2194 | 0x17006C92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2195 | 0x17006C93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2196 | 0x17006C94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2197 | 0x17006C95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2198 | 0x17006C96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2199 | 0x17006C97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2200 | 0x17006C98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2201 | 0x17006C99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2202 | 0x17006C9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2203 | 0x17006C9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2204 | 0x17006C9C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2205 | 0x17006C9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2206 | 0x17006C9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2207 | 0x17006C9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2208 | 0x17006CA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2209 | 0x17006CA1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2210 | 0x17006CA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2211 | 0x17006CA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2212 | 0x17006CA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2213 | 0x17006CA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2214 | 0x17006CA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2215 | 0x17006CA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2216 | 0x17006CA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2217 | 0x17006CA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2218 | 0x17006CAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2219 | 0x17006CAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2220 | 0x17006CAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2221 | 0x17006CAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2222 | 0x17006CAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2223 | 0x17006CAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2224 | 0x17006CB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2225 | 0x17006CB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2226 | 0x17006CB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2227 | 0x17006CB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2228 | 0x17006CB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2229 | 0x17006CB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2230 | 0x17006CB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2231 | 0x17006CB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2232 | 0x17006CB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2233 | 0x17006CB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2234 | 0x17006CBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2235 | 0x17006CBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2236 | 0x17006CBC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2237 | 0x17006CBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2238 | 0x17006CBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2239 | 0x17006CBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2240 | 0x17006CC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2241 | 0x17006CC1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2242 | 0x17006CC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2243 | 0x17006CC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2244 | 0x17006CC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2245 | 0x17006CC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2246 | 0x17006CC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2247 | 0x17006CC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2248 | 0x17006CC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2249 | 0x17006CC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2250 | 0x17006CCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2251 | 0x17006CCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2252 | 0x17006CCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2253 | 0x17006CCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2254 | 0x17006CCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2255 | 0x17006CCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2256 | 0x17006CD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2257 | 0x17006CD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2258 | 0x17006CD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2259 | 0x17006CD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2260 | 0x17006CD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2261 | 0x17006CD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2262 | 0x17006CD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2263 | 0x17006CD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2264 | 0x17006CD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2265 | 0x17006CD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2266 | 0x17006CDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2267 | 0x17006CDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2268 | 0x17006CDC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2269 | 0x17006CDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2270 | 0x17006CDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2271 | 0x17006CDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2272 | 0x17006CE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2273 | 0x17006CE1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2274 | 0x17006CE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2275 | 0x17006CE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2276 | 0x17006CE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2277 | 0x17006CE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2278 | 0x17006CE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2279 | 0x17006CE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2280 | 0x17006CE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2281 | 0x17006CE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2282 | 0x17006CEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2283 | 0x17006CEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2284 | 0x17006CEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2285 | 0x17006CED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2286 | 0x17006CEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2287 | 0x17006CEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2288 | 0x17006CF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2289 | 0x17006CF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2290 | 0x17006CF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2291 | 0x17006CF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2292 | 0x17006CF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2293 | 0x17006CF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2294 | 0x17006CF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2295 | 0x17006CF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2296 | 0x17006CF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2297 | 0x17006CF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2298 | 0x17006CFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2299 | 0x17006CFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2300 | 0x17006CFC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2301 | 0x17006CFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2302 | 0x17006CFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2303 | 0x17006CFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2304 | 0x17006D00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2305 | 0x17006D01 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2306 | 0x17006D02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2307 | 0x17006D03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2308 | 0x17006D04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2309 | 0x17006D05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2310 | 0x17006D06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2311 | 0x17006D07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2312 | 0x17006D08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2313 | 0x17006D09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2314 | 0x17006D0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2315 | 0x17006D0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2316 | 0x17006D0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2317 | 0x17006D0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2318 | 0x17006D0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2319 | 0x17006D0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2320 | 0x17006D10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2321 | 0x17006D11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2322 | 0x17006D12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2323 | 0x17006D13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2324 | 0x17006D14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2325 | 0x17006D15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2326 | 0x17006D16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2327 | 0x17006D17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2328 | 0x17006D18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2329 | 0x17006D19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2330 | 0x17006D1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2331 | 0x17006D1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2332 | 0x17006D1C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2333 | 0x17006D1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2334 | 0x17006D1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2335 | 0x17006D1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2336 | 0x17006D20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2337 | 0x17006D21 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2338 | 0x17006D22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2339 | 0x17006D23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2340 | 0x17006D24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2341 | 0x17006D25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2342 | 0x17006D26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2343 | 0x17006D27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2344 | 0x17006D28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2345 | 0x17006D29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2346 | 0x17006D2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2347 | 0x17006D2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2348 | 0x17006D2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2349 | 0x17006D2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2350 | 0x17006D2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2351 | 0x17006D2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2352 | 0x17006D30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2353 | 0x17006D31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2354 | 0x17006D32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2355 | 0x17006D33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2356 | 0x17006D34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2357 | 0x17006D35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2358 | 0x17006D36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2359 | 0x17006D37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2360 | 0x17006D38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2361 | 0x17006D39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2362 | 0x17006D3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2363 | 0x17006D3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2364 | 0x17006D3C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2365 | 0x17006D3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2366 | 0x17006D3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2367 | 0x17006D3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2368 | 0x17006D40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2369 | 0x17006D41 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2370 | 0x17006D42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2371 | 0x17006D43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2372 | 0x17006D44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2373 | 0x17006D45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2374 | 0x17006D46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2375 | 0x17006D47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2376 | 0x17006D48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2377 | 0x17006D49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2378 | 0x17006D4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2379 | 0x17006D4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2380 | 0x17006D4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2381 | 0x17006D4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2382 | 0x17006D4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2383 | 0x17006D4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2384 | 0x17006D50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2385 | 0x17006D51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2386 | 0x17006D52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2387 | 0x17006D53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2388 | 0x17006D54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2389 | 0x17006D55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2390 | 0x17006D56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2391 | 0x17006D57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2392 | 0x17006D58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2393 | 0x17006D59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2394 | 0x17006D5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2395 | 0x17006D5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2396 | 0x17006D5C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2397 | 0x17006D5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2398 | 0x17006D5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2399 | 0x17006D5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2400 | 0x17006D60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2401 | 0x17006D61 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2402 | 0x17006D62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2403 | 0x17006D63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2404 | 0x17006D64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2405 | 0x17006D65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2406 | 0x17006D66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2407 | 0x17006D67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2408 | 0x17006D68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2409 | 0x17006D69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2410 | 0x17006D6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2411 | 0x17006D6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2412 | 0x17006D6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2413 | 0x17006D6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2414 | 0x17006D6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2415 | 0x17006D6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2416 | 0x17006D70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2417 | 0x17006D71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2418 | 0x17006D72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2419 | 0x17006D73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2420 | 0x17006D74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2421 | 0x17006D75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2422 | 0x17006D76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2423 | 0x17006D77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2424 | 0x17006D78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2425 | 0x17006D79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2426 | 0x17006D7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2427 | 0x17006D7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2428 | 0x17006D7C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2429 | 0x17006D7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2430 | 0x17006D7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2431 | 0x17006D7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2432 | 0x17006D80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2433 | 0x17006D81 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2434 | 0x17006D82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2435 | 0x17006D83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2436 | 0x17006D84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2437 | 0x17006D85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2438 | 0x17006D86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2439 | 0x17006D87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2440 | 0x17006D88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2441 | 0x17006D89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2442 | 0x17006D8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2443 | 0x17006D8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2444 | 0x17006D8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2445 | 0x17006D8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2446 | 0x17006D8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2447 | 0x17006D8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2448 | 0x17006D90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2449 | 0x17006D91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2450 | 0x17006D92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2451 | 0x17006D93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2452 | 0x17006D94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2453 | 0x17006D95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2454 | 0x17006D96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2455 | 0x17006D97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2456 | 0x17006D98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2457 | 0x17006D99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2458 | 0x17006D9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2459 | 0x17006D9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2460 | 0x17006D9C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2461 | 0x17006D9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2462 | 0x17006D9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2463 | 0x17006D9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2464 | 0x17006DA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2465 | 0x17006DA1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2466 | 0x17006DA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2467 | 0x17006DA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2468 | 0x17006DA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2469 | 0x17006DA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2470 | 0x17006DA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2471 | 0x17006DA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2472 | 0x17006DA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2473 | 0x17006DA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2474 | 0x17006DAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2475 | 0x17006DAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2476 | 0x17006DAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2477 | 0x17006DAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2478 | 0x17006DAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2479 | 0x17006DAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2480 | 0x17006DB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2481 | 0x17006DB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2482 | 0x17006DB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2483 | 0x17006DB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2484 | 0x17006DB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2485 | 0x17006DB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2486 | 0x17006DB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2487 | 0x17006DB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2488 | 0x17006DB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2489 | 0x17006DB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2490 | 0x17006DBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2491 | 0x17006DBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2492 | 0x17006DBC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2493 | 0x17006DBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2494 | 0x17006DBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2495 | 0x17006DBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2496 | 0x17006DC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2497 | 0x17006DC1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2498 | 0x17006DC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2499 | 0x17006DC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2500 | 0x17006DC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2501 | 0x17006DC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2502 | 0x17006DC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2503 | 0x17006DC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2504 | 0x17006DC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2505 | 0x17006DC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2506 | 0x17006DCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2507 | 0x17006DCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2508 | 0x17006DCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2509 | 0x17006DCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2510 | 0x17006DCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2511 | 0x17006DCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2512 | 0x17006DD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2513 | 0x17006DD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2514 | 0x17006DD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2515 | 0x17006DD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2516 | 0x17006DD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2517 | 0x17006DD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2518 | 0x17006DD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2519 | 0x17006DD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2520 | 0x17006DD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2521 | 0x17006DD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2522 | 0x17006DDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2523 | 0x17006ddb | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2524 | 0x17006DDC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2525 | 0x17006DDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2526 | 0x17006DDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2527 | 0x17006DDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2528 | 0x17006DE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2529 | 0x17006DE1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2530 | 0x17006DE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2531 | 0x17006DE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2532 | 0x17006DE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2533 | 0x17006DE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2534 | 0x17006DE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2535 | 0x17006DE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2536 | 0x17006DE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2537 | 0x17006DE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2538 | 0x17006DEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2539 | 0x17006DEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2540 | 0x17006DEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2541 | 0x17006DED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2542 | 0x17006DEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2543 | 0x17006DEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2544 | 0x17006DF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2545 | 0x17006DF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2546 | 0x17006DF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2547 | 0x17006DF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2548 | 0x17006DF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2549 | 0x17006DF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2550 | 0x17006DF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2551 | 0x17006DF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2552 | 0x17006DF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2553 | 0x17006DF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2554 | 0x17006DFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2555 | 0x17006DFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2556 | 0x17006DFC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2557 | 0x17006DFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2558 | 0x17006DFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2559 | 0x17006DFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2560 | 0x17006E00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2561 | 0x17006E01 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2562 | 0x17006E02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2563 | 0x17006E03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2564 | 0x17006E04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2565 | 0x17006E05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2566 | 0x17006E06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2567 | 0x17006E07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2568 | 0x17006E08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2569 | 0x17006E09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2570 | 0x17006E0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2571 | 0x17006E0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2572 | 0x17006E0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2573 | 0x17006E0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2574 | 0x17006E0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2575 | 0x17006E0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2576 | 0x17006E10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2577 | 0x17006E11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2578 | 0x17006E12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2579 | 0x17006E13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2580 | 0x17006E14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2581 | 0x17006E15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2582 | 0x17006E16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2583 | 0x17006E17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2584 | 0x17006E18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2585 | 0x17006E19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2586 | 0x17006E1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2587 | 0x17006E1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2588 | 0x17006E1C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2589 | 0x17006E1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2590 | 0x17006E1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2591 | 0x17006E1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2592 | 0x17006E20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2593 | 0x17006E21 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2594 | 0x17006E22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2595 | 0x17006E23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2596 | 0x17006E24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2597 | 0x17006E25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2598 | 0x17006E26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2599 | 0x17006E27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2600 | 0x17006E28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2601 | 0x17006E29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2602 | 0x17006E2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2603 | 0x17006E2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2604 | 0x17006E2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2605 | 0x17006E2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2606 | 0x17006E2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2607 | 0x17006E2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2608 | 0x17006E30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2609 | 0x17006E31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2610 | 0x17006E32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2611 | 0x17006E33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2612 | 0x17006E34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2613 | 0x17006E35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2614 | 0x17006E36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2615 | 0x17006E37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2616 | 0x17006E38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2617 | 0x17006E39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2618 | 0x17006E3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2619 | 0x17006E3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2620 | 0x17006E3C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2621 | 0x17006E3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2622 | 0x17006E3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2623 | 0x17006E3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2624 | 0x17006E40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2625 | 0x17006E41 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2626 | 0x17006E42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2627 | 0x17006E43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2628 | 0x17006E44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2629 | 0x17006E45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2630 | 0x17006E46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2631 | 0x17006E47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2632 | 0x17006E48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2633 | 0x17006E49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2634 | 0x17006E4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2635 | 0x17006E4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2636 | 0x17006E4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2637 | 0x17006E4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2638 | 0x17006E4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2639 | 0x17006E4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2640 | 0x17006E50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2641 | 0x17006E51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2642 | 0x17006E52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2643 | 0x17006E53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2644 | 0x17006E54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2645 | 0x17006E55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2646 | 0x17006E56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2647 | 0x17006E57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2648 | 0x17006E58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2649 | 0x17006E59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2650 | 0x17006E5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2651 | 0x17006E5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2652 | 0x17006E5C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2653 | 0x17006E5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2654 | 0x17006E5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2655 | 0x17006E5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2656 | 0x17006E60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2657 | 0x17006E61 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2658 | 0x17006E62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2659 | 0x17006E63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2660 | 0x17006E64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2661 | 0x17006E65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2662 | 0x17006E66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2663 | 0x17006E67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2664 | 0x17006E68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2665 | 0x17006E69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2666 | 0x17006E6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2667 | 0x17006E6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2668 | 0x17006E6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2669 | 0x17006E6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2670 | 0x17006E6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2671 | 0x17006E6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2672 | 0x17006E70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2673 | 0x17006E71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2674 | 0x17006E72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2675 | 0x17006E73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2676 | 0x17006E74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2677 | 0x17006E75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2678 | 0x17006E76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2679 | 0x17006E77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2680 | 0x17006E78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2681 | 0x17006E79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2682 | 0x17006E7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2683 | 0x17006E7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2684 | 0x17006E7C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2685 | 0x17006E7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2686 | 0x17006E7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2687 | 0x17006E7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2688 | 0x17006E80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2689 | 0x17006E81 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2690 | 0x17006E82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2691 | 0x17006E83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2692 | 0x17006E84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2693 | 0x17006E85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2694 | 0x17006E86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2695 | 0x17006E87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2696 | 0x17006E88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2697 | 0x17006E89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2698 | 0x17006E8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2699 | 0x17006E8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2700 | 0x17006E8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2701 | 0x17006E8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2702 | 0x17006E8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2703 | 0x17006E8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2704 | 0x17006E90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2705 | 0x17006E91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2706 | 0x17006E92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2707 | 0x17006E93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2708 | 0x17006E94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2709 | 0x17006E95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2710 | 0x17006E96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2711 | 0x17006E97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2712 | 0x17006E98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2713 | 0x17006E99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2714 | 0x17006E9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2715 | 0x17006E9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2716 | 0x17006E9C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2717 | 0x17006E9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2718 | 0x17006E9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2719 | 0x17006E9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2720 | 0x17006EA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2721 | 0x17006EA1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2722 | 0x17006EA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2723 | 0x17006EA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2724 | 0x17006EA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2725 | 0x17006EA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2726 | 0x17006EA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2727 | 0x17006EA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2728 | 0x17006EA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2729 | 0x17006EA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2730 | 0x17006EAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2731 | 0x17006EAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2732 | 0x17006EAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2733 | 0x17006EAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2734 | 0x17006EAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2735 | 0x17006EAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2736 | 0x17006EB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2737 | 0x17006EB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2738 | 0x17006EB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2739 | 0x17006EB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2740 | 0x17006EB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2741 | 0x17006EB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2742 | 0x17006EB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2743 | 0x17006EB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2744 | 0x17006EB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2745 | 0x17006EB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2746 | 0x17006EBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2747 | 0x17006EBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2748 | 0x17006EBC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2749 | 0x17006EBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2750 | 0x17006EBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2751 | 0x17006EBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2752 | 0x17006EC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2753 | 0x17006EC1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2754 | 0x17006EC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2755 | 0x17006EC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2756 | 0x17006EC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2757 | 0x17006EC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2758 | 0x17006EC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2759 | 0x17006EC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2760 | 0x17006EC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2761 | 0x17006EC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2762 | 0x17006ECA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2763 | 0x17006ECB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2764 | 0x17006ECC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2765 | 0x17006ECD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2766 | 0x17006ECE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2767 | 0x17006ECF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2768 | 0x17006ED0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2769 | 0x17006ED1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2770 | 0x17006ED2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2771 | 0x17006ED3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2772 | 0x17006ED4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2773 | 0x17006ED5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2774 | 0x17006ED6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2775 | 0x17006ED7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2776 | 0x17006ED8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2777 | 0x17006ED9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2778 | 0x17006EDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2779 | 0x17006EDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2780 | 0x17006EDC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2781 | 0x17006EDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2782 | 0x17006EDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2783 | 0x17006EDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2784 | 0x17006EE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2785 | 0x17006EE1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2786 | 0x17006EE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2787 | 0x17006EE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2788 | 0x17006EE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2789 | 0x17006EE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2790 | 0x17006EE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2791 | 0x17006EE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2792 | 0x17006EE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2793 | 0x17006EE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2794 | 0x17006EEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2795 | 0x17006EEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2796 | 0x17006EEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2797 | 0x17006EED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2798 | 0x17006EEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2799 | 0x17006EEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2800 | 0x17006EF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2801 | 0x17006EF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2802 | 0x17006EF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2803 | 0x17006EF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2804 | 0x17006EF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2805 | 0x17006EF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2806 | 0x17006EF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2807 | 0x17006EF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2808 | 0x17006EF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2809 | 0x17006EF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2810 | 0x17006EFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2811 | 0x17006EFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2812 | 0x17006EFC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2813 | 0x17006EFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2814 | 0x17006EFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2815 | 0x17006EFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2816 | 0x17006F00 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2817 | 0x17006F01 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2818 | 0x17006F02 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2819 | 0x17006F03 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2820 | 0x17006F04 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2821 | 0x17006F05 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2822 | 0x17006F06 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2823 | 0x17006F07 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2824 | 0x17006F08 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2825 | 0x17006F09 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2826 | 0x17006F0A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2827 | 0x17006F0B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2828 | 0x17006F0C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2829 | 0x17006F0D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2830 | 0x17006F0E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2831 | 0x17006F0F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2832 | 0x17006F10 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2833 | 0x17006F11 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2834 | 0x17006F12 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2835 | 0x17006F13 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2836 | 0x17006F14 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2837 | 0x17006F15 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2838 | 0x17006F16 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2839 | 0x17006F17 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2840 | 0x17006F18 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2841 | 0x17006F19 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2842 | 0x17006F1A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2843 | 0x17006F1B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2844 | 0x17006F1C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2845 | 0x17006F1D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2846 | 0x17006F1E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2847 | 0x17006F1F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2848 | 0x17006F20 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2849 | 0x17006F21 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2850 | 0x17006F22 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2851 | 0x17006F23 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2852 | 0x17006F24 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2853 | 0x17006F25 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2854 | 0x17006F26 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2855 | 0x17006F27 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2856 | 0x17006F28 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2857 | 0x17006F29 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2858 | 0x17006F2A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2859 | 0x17006F2B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2860 | 0x17006F2C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2861 | 0x17006F2D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2862 | 0x17006F2E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2863 | 0x17006F2F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2864 | 0x17006F30 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2865 | 0x17006F31 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2866 | 0x17006F32 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2867 | 0x17006F33 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2868 | 0x17006F34 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2869 | 0x17006F35 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2870 | 0x17006F36 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2871 | 0x17006F37 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2872 | 0x17006F38 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2873 | 0x17006F39 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2874 | 0x17006F3A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2875 | 0x17006F3B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2876 | 0x17006F3C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2877 | 0x17006F3D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2878 | 0x17006F3E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2879 | 0x17006F3F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2880 | 0x17006F40 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2881 | 0x17006F41 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2882 | 0x17006F42 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2883 | 0x17006F43 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2884 | 0x17006F44 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2885 | 0x17006F45 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2886 | 0x17006F46 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2887 | 0x17006F47 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2888 | 0x17006F48 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2889 | 0x17006F49 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2890 | 0x17006F4A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2891 | 0x17006F4B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2892 | 0x17006F4C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2893 | 0x17006F4D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2894 | 0x17006F4E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2895 | 0x17006F4F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2896 | 0x17006F50 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2897 | 0x17006F51 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2898 | 0x17006F52 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2899 | 0x17006F53 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2900 | 0x17006F54 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2901 | 0x17006F55 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2902 | 0x17006F56 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2903 | 0x17006F57 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2904 | 0x17006F58 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2905 | 0x17006F59 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2906 | 0x17006F5A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2907 | 0x17006F5B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2908 | 0x17006F5C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2909 | 0x17006F5D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2910 | 0x17006F5E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2911 | 0x17006F5F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2912 | 0x17006F60 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2913 | 0x17006F61 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2914 | 0x17006F62 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2915 | 0x17006F63 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2916 | 0x17006F64 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2917 | 0x17006F65 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2918 | 0x17006F66 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2919 | 0x17006F67 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2920 | 0x17006F68 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2921 | 0x17006F69 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2922 | 0x17006F6A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2923 | 0x17006F6B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2924 | 0x17006F6C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2925 | 0x17006F6D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2926 | 0x17006F6E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2927 | 0x17006F6F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2928 | 0x17006F70 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2929 | 0x17006F71 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2930 | 0x17006F72 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2931 | 0x17006F73 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2932 | 0x17006F74 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2933 | 0x17006F75 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2934 | 0x17006F76 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2935 | 0x17006F77 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2936 | 0x17006F78 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2937 | 0x17006F79 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2938 | 0x17006F7A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2939 | 0x17006F7B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2940 | 0x17006F7C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2941 | 0x17006F7D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2942 | 0x17006F7E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2943 | 0x17006F7F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2944 | 0x17006F80 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2945 | 0x17006F81 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2946 | 0x17006F82 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2947 | 0x17006F83 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2948 | 0x17006F84 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2949 | 0x17006F85 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2950 | 0x17006F86 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2951 | 0x17006F87 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2952 | 0x17006F88 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2953 | 0x17006F89 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2954 | 0x17006F8A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2955 | 0x17006F8B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2956 | 0x17006F8C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2957 | 0x17006F8D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2958 | 0x17006F8E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2959 | 0x17006F8F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2960 | 0x17006F90 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2961 | 0x17006F91 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2962 | 0x17006F92 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2963 | 0x17006F93 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2964 | 0x17006F94 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2965 | 0x17006F95 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2966 | 0x17006F96 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2967 | 0x17006F97 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2968 | 0x17006F98 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2969 | 0x17006F99 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2970 | 0x17006F9A | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2971 | 0x17006F9B | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2972 | 0x17006F9C | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2973 | 0x17006F9D | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2974 | 0x17006F9E | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2975 | 0x17006F9F | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2976 | 0x17006FA0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2977 | 0x17006FA1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY2978 | 0x17006FA2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2979 | 0x17006FA3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2980 | 0x17006FA4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2981 | 0x17006FA5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2982 | 0x17006FA6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2983 | 0x17006FA7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2984 | 0x17006FA8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2985 | 0x17006FA9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2986 | 0x17006FAA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2987 | 0x17006FAB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2988 | 0x17006FAC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2989 | 0x17006FAD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2990 | 0x17006FAE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2991 | 0x17006FAF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2992 | 0x17006FB0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2993 | 0x17006FB1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2994 | 0x17006FB2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2995 | 0x17006FB3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2996 | 0x17006FB4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2997 | 0x17006FB5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2998 | 0x17006FB6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY2999 | 0x17006FB7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3000 | 0x17006FB8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3001 | 0x17006FB9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3002 | 0x17006FBA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3003 | 0x17006FBB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3004 | 0x17006FBC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3005 | 0x17006FBD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3006 | 0x17006FBE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3007 | 0x17006FBF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3008 | 0x17006FC0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3009 | 0x17006FC1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY3010 | 0x17006FC2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3011 | 0x17006FC3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3012 | 0x17006FC4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3013 | 0x17006FC5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3014 | 0x17006FC6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3015 | 0x17006FC7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3016 | 0x17006FC8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3017 | 0x17006FC9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3018 | 0x17006FCA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3019 | 0x17006FCB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3020 | 0x17006FCC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3021 | 0x17006FCD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3022 | 0x17006FCE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3023 | 0x17006FCF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3024 | 0x17006FD0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3025 | 0x17006FD1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3026 | 0x17006FD2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3027 | 0x17006FD3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3028 | 0x17006FD4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3029 | 0x17006FD5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3030 | 0x17006FD6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3031 | 0x17006FD7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3032 | 0x17006FD8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3033 | 0x17006FD9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3034 | 0x17006FDA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3035 | 0x17006FDB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3036 | 0x17006FDC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3037 | 0x17006FDD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3038 | 0x17006FDE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3039 | 0x17006FDF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3040 | 0x17006FE0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3041 | 0x17006FE1 | FULL | Public key for signature verification (max RSA key size 4096) |

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| SFLASH_PUBLIC_KEY3042 | 0x17006FE2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3043 | 0x17006FE3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3044 | 0x17006FE4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3045 | 0x17006FE5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3046 | 0x17006FE6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3047 | 0x17006FE7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3048 | 0x17006FE8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3049 | 0x17006FE9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3050 | 0x17006FEA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3051 | 0x17006FEB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3052 | 0x17006FEC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3053 | 0x17006FED | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3054 | 0x17006FEE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3055 | 0x17006FEF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3056 | 0x17006FF0 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3057 | 0x17006FF1 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3058 | 0x17006FF2 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3059 | 0x17006FF3 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3060 | 0x17006FF4 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3061 | 0x17006FF5 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3062 | 0x17006FF6 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3063 | 0x17006FF7 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3064 | 0x17006FF8 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3065 | 0x17006FF9 | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3066 | 0x17006FFA | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3067 | 0x17006FFB | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3068 | 0x17006FFC | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3069 | 0x17006FFD | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3070 | 0x17006FFE | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_PUBLIC_KEY3071 | 0x17006FFF | FULL | Public key for signature verification (max RSA key size 4096) |
| SFLASH_APP_PROT_SETTINGS0 | 0x17007600 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS1 | 0x17007604 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS2 | 0x17007608 | FULL | Application protection settings (4*128=512 bytes) |
| SFLASH_APP_PROT_SETTINGS3 | 0x1700760C | FULL | Application protection settings (4*128=512 bytes) |

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[illegible]

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| SFLASH_TOC2_MAGIC_NUMBER | 0x17007C04 | FULL | Magic number(0x01211220) |
| SFLASH_TOC2_SMIF_CFG_STRUCT_ADDR | 0x17007C08 | FULL | Null terminated table of pointers representing the SMIF configuration structure |
| SFLASH_TOC2_FIRST_USER_APP_ADDR | 0x17007C0C | FULL | Address of First User Application Object |
| SFLASH_TOC2_FIRST_USER_APP_FORMAT | 0x17007C10 | FULL | Format of First User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified |
| SFLASH_TOC2_SECOND_USER_APP_ADDR | 0x17007C14 | FULL | Address of Second User Application Object |
| SFLASH_TOC2_SECOND_USER_APP_FORMAT | 0x17007C18 | FULL | Format of Second User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified |
| SFLASH_TOC2_FIRST_CMX_1_USER_APP_ADDR | 0x17007C1C | FULL | Address of First CM4 or CM7 core1 User Application Object |
| SFLASH_TOC2_SECOND_CMX_1_USER_APP_ADDR | 0x17007C20 | FULL | Address of Second CM4 or CM7 core1 User Application Object |
| SFLASH_TOC2_FIRST_CMX_2_USER_APP_ADDR | 0x17007C24 | FULL | Address of First CM4 or CM7 core2 User Application Object |
| SFLASH_TOC2_SECOND_CMX_2_USER_APP_ADDR | 0x17007C28 | FULL | Address of Second CM4 or CM7 core2 User Application Object |
| SFLASH_TOC2_SECURITY_UPDATES_MARKER | 0x17007CFC | FULL | Marker for Security Updates |
| SFLASH_TOC2_SHASH_OBJECTS | 0x17007D00 | FULL | Number of additional objects to be verified for SECURE_HASH |
| SFLASH_TOC2_SIGNATURE_VERIF_KEY | 0x17007D04 | FULL | Address of signature verification key (0 if none).The object is signature specific key. It is the public key in case of RSA |
| SFLASH_TOC2_APP_PROTECTION_ADDR | 0x17007D08 | FULL | Address of Application Protection |
| SFLASH_TOC2_REVISION | 0x17007DF4 | FULL | Indicates TOC2 Revision. It is not used now. |
| SFLASH_TOC2_FLAGS | 0x17007DF8 | FULL | Controls default configuration |

24.1 Register Details

24.1.1 SFLASH_SI_REVISION_ID

Description: Indicates Silicon Revision ID of the device
Address: 0x17000001
Offset: 0x1
Retention: Retained
IsDeepSleep: No
Comment: Used to store Silicon Revision ID
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | SI_REVISION_ID [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---------------------|
| 0:7 | SI_REVISION_ID | RW | | X | Silicon Revision ID |

24.1.2 SFLASH_SILICON_ID

Description: Indicates Silicon ID of the device
Address: 0x17000002
Offset: 0x2
Retention: Retained
IsDeepSleep: No
Comment: Used to store silicon ID
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | ID [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | ID [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|-------------|
| 0:15 | ID | RW | | X | Silicon ID |

24.1.3 SFLASH_SFLASH_SVN

Description: SFLASH Subversion
Address: 0x170000A8
Offset: 0xA8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------------|
| 0:31 | DATA32 | RW | | 0 | SFLASH Subversion |

24.1.4 SFLASH_FB_FLAGS

Description: Flash boot flags
Address: 0x170001FC
Offset: 0x1FC
Retention: Retained
IsDeepSleep: No
Comment: Flash boot flags are used by the flash boot. The default value is 0x0000_0015
Default: 0x15

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|--------------------|---|--------------------|---|------------------|---|
| Name | None [7:6] | | FB_RSA4K_CTL [5:4] | | FB_RSA3K_CTL [3:2] | | FB_PIN_CTL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:1 | FB_PIN_CTL | RW | | 1 | Determines toggling a GPIO pin at the start and end of Flash boot 2 = Enable toggling a GPIO pin at the start and end of Flash boot Others = Disable toggling a GPIO pin at the start and end of Flash boot Default value = 1. |
| 2:3 | FB_RSA3K_CTL | RW | | 1 | Determines if RSA-3K is supported. 2 = RSA-3K is supported. RSA public key modulo length should be in range 512 to 3072 bit. The field FB_RSA4K_CTL must be set to 0. Others = RSA-3K is not supported. RSA public key modulo length should be in range 512 to 2048 bit. Default value = 1. |
| 4:5 | FB_RSA4K_CTL | RW | | 1 | Determines if RSA-4K is supported. 2 = RSA-4K is supported. RSA public key modulo length should be in range 512 to 4096 bit. RSA4K already includes RSA3K option. The field FB_RSA3K_CTL must be set to 0. Others = RSA-4K is not supported. Default value = 1. |

24.1.5 SFLASH_EPASS_TEMP_TRIM_TEMP_ROOMSORT

Description: On Chip temperature measured using external currents and external ADC at ROOM
Address: 0x1700064E
Offset: 0x64E
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | On Chip temperature measured using external currents and external ADC at ROOM |

24.1.6 SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT

Description: Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM
Address: 0x17000650
Offset: 0x650
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA16 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA16 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM |

24.1.7 SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT

Description: Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM
Address: 0x17000652
Offset: 0x652
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM |

24.1.8 SFLASH_EPASS_TEMP_TRIM_TEMP_COLDSORT

Description: On Chip temperature measured using external currents and external ADC at COLD
Address: 0x17000654
Offset: 0x654
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | On Chip temperature measured using external currents and external ADC at COLD |

24.1.9 SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT

Description: Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD
Address: 0x17000656
Offset: 0x656
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA16 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA16 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD |

24.1.10 SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT

Description: Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD
Address: 0x17000658
Offset: 0x658
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD |

24.1.11 SFLASH_EPASS_TEMP_TRIM_TEMP_HOTCLASS

Description: On Chip temperature measured using external currents and external ADC at HOT
Address: 0x1700065A
Offset: 0x65A
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | On Chip temperature measured using external currents and external ADC at HOT |

24.1.12 SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS

Description: Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT
Address: 0x1700065C
Offset: 0x65C
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA16 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA16 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT |

24.1.13 SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS

Description: Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT
Address: 0x1700065E
Offset: 0x65E
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT |

24.1.14 SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT_5V

Description: Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM
Address: 0x1700066A
Offset: 0x66A
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA16 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA16 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM |

24.1.15 SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT_5V

Description: Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM
Address: 0x1700066C
Offset: 0x66C
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM |

24.1.16 SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT_5V

Description: Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD
Address: 0x1700066E
Offset: 0x66E
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | DATA16 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA16 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD |

24.1.17 SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT_5V

Description: Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD
Address: 0x17000670
Offset: 0x670
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD |

24.1.18 SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS_5V

Description: Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT
Address: 0x17000672
Offset: 0x672
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT |

24.1.19 SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS_5V

Description: Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT
Address: 0x17000674
Offset: 0x674
Retention: Retained
IsDeepSleep: No
Comment: Temperature calibration data for EPASS Temperature sensor
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA16 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA16 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | DATA16 | RW | | X | Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT |

24.1.20 SFLASH_SRSS_PWR_OFFSET

Description: SRSS_PWR_OFFSET
Address: 0x17000730
Offset: 0x730
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|------------------------|---|---|---|---|
| Name | None [7:5] | | | PMIC_VADJ_OFFSET [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|--------------------------------|----|----|---|---|
| Name | None [15:13] | | | REGHC_TRANS_VADJ_OFFSET [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------------|----|----|-----------------|---|
| 0:4 | PMIC_VADJ_OFFSET | RW | | X | Die-specific offset for VADJ when using it for feedback to an external PMIC |
| 8:12 | REGHC_TRANS_VADJ_OFFSET | RW | | X | Die-specific offset for VADJ when using REGHC with external transistor |

24.1.21 SFLASH_USER_FREE_ROW0

Description: USER_FREE_ROW0
Address: 0x17000800
Offset: 0x800
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.22 SFLASH_USER_FREE_ROW1

Description: USER_FREE_ROW1
Address: 0x17000A00
Offset: 0xA00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.23 SFLASH_USER_FREE_ROW2

Description: USER_FREE_ROW2
Address: 0x17000C00
Offset: 0xC00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.24 SFLASH_USER_FREE_ROW3

Description: USER_FREE_ROW3
Address: 0x17000E00
Offset: 0xE00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.25 SFLASH_SFLASH_UPDATE_MARKER

Description: Markers for storing SFLASH programming states
Address: 0x17001800
Offset: 0x1800
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | DATA32 | RW | | X | Marker which indicates SFLASH programming state |

24.1.26 SFLASH_FLASH_BOOT_OBJECT_SIZE

Description: Flash Boot - Object Size
Address: 0x17002000
Offset: 0x2000
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.27 SFLASH_FLASH_BOOT_APP_ID

Description: Flash Boot - Application ID/Version
Address: 0x17002004
Offset: 0x2004
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|----|----|----|-----------------------|----|----|----|
| Name | APP_ID [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | APP_ID [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | MINOR_VERSION [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:28] | | | | MAJOR_VERSION [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|-------------|
| 0:15 | APP_ID | RW | | X | N/A |
| 16:23 | MINOR_VERSION | RW | | X | N/A |
| 24:27 | MAJOR_VERSION | RW | | X | N/A |

24.1.28 SFLASH_FLASH_BOOT_VERSION_LOW

Description: Flash Boot - Version Low
Address: 0x17002018
Offset: 0x2018
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.29 SFLASH_FLASH_BOOT_FAMILY_ID

Description: Flash Boot - Family ID
Address: 0x1700201C
Offset: 0x201C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.30 SFLASH_PUBLIC_KEY

Description: Public key for signature verification (max RSA key size 4096)
Address: 0x17006400
Offset: 0x6400
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|-------------|
| 0:7 | DATA | RW | | X | N/A |

24.1.31 SFLASH_APP_PROT_SETTINGS

Description: Application protection settings (4*128=512 bytes)
Address: 0x17007600
Offset: 0x7600
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.32 SFLASH_TOC2_OBJECT_SIZE

Description: Object size in bytes for CRC calculation starting from offset 0x00
Address: 0x17007C00
Offset: 0x7C00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.33 SFLASH_TOC2_MAGIC_NUMBER

Description: Magic number(0x01211220)
Address: 0x17007C04
Offset: 0x7C04
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.34 SFLASH_TOC2_SMIF_CFG_STRUCT_ADDR

Description: Null terminated table of pointers representing the SMIF configuration structure
Address: 0x17007C08
Offset: 0x7C08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.35 SFLASH_TOC2_FIRST_USER_APP_ADDR

Description: Address of First User Application Object
Address: 0x17007C0C
Offset: 0x7C0C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.36 SFLASH_TOC2_FIRST_USER_APP_FORMAT

Description: Format of First User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
Address: 0x17007C10
Offset: 0x7C10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.37 SFLASH_TOC2_SECOND_USER_APP_ADDR

Description: Address of Second User Application Object
Address: 0x17007C14
Offset: 0x7C14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.38 SFLASH_TOC2_SECOND_USER_APP_FORMAT

Description: Format of Second User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
Address: 0x17007C18
Offset: 0x7C18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.39 SFLASH_TOC2_FIRST_CMX_1_USER_APP_ADDR

Description: Address of First CM4 or CM7 core1 User Application Object
Address: 0x17007C1C
Offset: 0x7C1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | DATA32 | RW | | X | Address of First CM4 or CM7 core1 User Application Object |

24.1.40 SFLASH_TOC2_SECOND_CMX_1_USER_APP_ADDR

Description: Address of Second CM4 or CM7 core1 User Application Object
Address: 0x17007C20
Offset: 0x7C20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.41 SFLASH_TOC2_FIRST_CMX_2_USER_APP_ADDR

Description: Address of First CM4 or CM7 core2 User Application Object
Address: 0x17007C24
Offset: 0x7C24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.42 SFLASH_TOC2_SECOND_CMX_2_USER_APP_ADDR

Description: Address of Second CM4 or CM7 core2 User Application Object
Address: 0x17007C28
Offset: 0x7C28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.43 SFLASH_TOC2_SECURITY_UPDATES_MARKER

Description: Marker for Security Updates
Address: 0x17007CFC
Offset: 0x7CFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | DATA32 | RW | | X | <p>This field is valid in flash boot version 3.1.0.556 and later.</p> <p>When marker is set to 0xFEDEEDDF the following PPU's will be configured during boot:</p> <ul style="list-style-type: none"> - PERI_MS_PPU_FX_PERI_GR2_GROUP (Fixed PPU) - read only for all PCs; - Programmable PPU#11 configured to allow full access for the following region 0x40201000 - 0x4020100C. The HSM may overwrite the default configuration and reconfigure the PPU. - Programmable PPU#12 configured to allow full access for the CPUSS_ECC_CTL register (0x402013C8). The HSM may overwrite the default configuration and reconfigure the PPU. - Programmable PPU#13 configured to allow full access for the following region 0x40201300 - 0x402013C8. The HSM may overwrite the default configuration and reconfigure the PPU. |

24.1.44 SFLASH_TOC2_SHASH_OBJECTS

Description: Number of additional objects to be verified for SECURE_HASH
Address: 0x17007D00
Offset: 0x7D00
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.45 SFLASH_TOC2_SIGNATURE_VERIF_KEY

Description: Address of signature verification key (0 if none).The object is signature specific key. It is the public key in case of RSA

Address: 0x17007D04

Offset: 0x7D04

Retention: Retained

IsDeepSleep: No

Comment:

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DATA32 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DATA32 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.46 SFLASH_TOC2_APP_PROTECTION_ADDR

Description: Address of Application Protection
Address: 0x17007D08
Offset: 0x7D08
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|-------------|
| 0:31 | DATA32 | RW | | X | N/A |

24.1.47 SFLASH_TOC2_REVISION

Description: Indicates TOC2 Revision. It is not used now.
Address: 0x17007DF4
Offset: 0x7DF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | DATA32 [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | DATA32 [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|----|----|----|----|----|----|----|
| Name | DATA32 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | DATA32 | RW | | X | Indicate TOC2 Revision Value: 0x0000_0000 and 0xFFFF_FFFF - default. |

24.1.48 SFLASH_TOC2_FLAGS

Description: Controls default configuration
Address: 0x17007DF8
Offset: 0x7DF8
Retention: Retained
IsDeepSleep: No
Comment: If TOC2 is erased (default), Flash boot assumes TOC2_FLAGS = 0x0000_0243
Default: 0x243

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|--------------------|---|---------------------|---|---|--------------------|---|
| Name | | SWJ_PINS_CTL [6:5] | | LISTEN_WINDOW [4:2] | | | CLOCK_CONFIG [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------------|---|--------------------|
| Name | None [15:11] | | | | | FB_BOOTLOADER_CTL [10:9] | | APP_AUTH_CTL [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| 0:1 | CLOCK_CONFIG | RW | | 3 | Indicates clock frequency configuration. The clock should stay the same after Flash Boot execution. 0 = 8 MHz, IMO, no FLL 1 = 25 MHz, IMO + FLL 2 = 50 MHz, IMO + FLL 3 = Use ROM boot clocks configuration (default) |
| 2:4 | LISTEN_WINDOW | RW | | 0 | Determines the Listen window to allow sufficient time to acquire debug port. When CLOCK_CONFIG is set to 3, these window times are calculated assuming ROM boot clock is at 100MHz. 0 = 20 ms (Default) 1 = 10 ms 2 = 1 ms 3 = 0 ms (No Listen window) 4 = 100 ms |
| 5:6 | SWJ_PINS_CTL | RW | | 2 | Determines if SWJ pins are configured in SWJ mode by Flash boot. Note: SWJ pins may be enabled later in the user code. 0 = Do not enable SWJ pins in Flash boot. Listen window is skipped. 1 = Do not enable SWJ pins in Flash boot. Listen window is skipped. 2 = Enable SWJ pins in Flash boot (default). 3 = Do not enable SWJ pins in Flash boot. Listen window is skipped. |
| 7:8 | APP_AUTH_CTL | RW | | 0 | Determines if the application image digital signature verification (authentication) is performed: 0 = Authentication is enabled (default). 1 = Authentication is disabled. 2 = Authentication is enabled (recommended). 3 = Authentication is enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|--|
| 9:10 | FB_BOOTLOADER_CTL | RW | | 1 | Determine if the internal bootloader in Flash boot is disabled: 0 = Internal bootloader is disabled. 1 = Internal bootloader is launched if the other bootloader conditions are met (default). 2 = Internal bootloader is disabled. 3 = Internal bootloader is disabled. |

25 SMARTIO

| | |
|---------------------|-------------------------------|
| Description | Programmable IO configuration |
| Base Address | 0x40320000 |
| Size | 0x10000 |
| Slave Num | MMIO3 - 2 |

25.1 PRT 12

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------------------|
| SMARTIO_PRT12_CTL | 0x40320C00 | FULL | Control register |
| SMARTIO_PRT12_SYNC_CTL | 0x40320C10 | FULL | Synchronization control register |
| SMARTIO_PRT12_LUT_SEL0 | 0x40320C20 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL1 | 0x40320C24 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL2 | 0x40320C28 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL3 | 0x40320C2C | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL4 | 0x40320C30 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL5 | 0x40320C34 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL6 | 0x40320C38 | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_SEL7 | 0x40320C3C | FULL | LUT component input selection |
| SMARTIO_PRT12_LUT_CTL0 | 0x40320C40 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL1 | 0x40320C44 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL2 | 0x40320C48 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL3 | 0x40320C4C | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL4 | 0x40320C50 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL5 | 0x40320C54 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL6 | 0x40320C58 | FULL | LUT component control register |
| SMARTIO_PRT12_LUT_CTL7 | 0x40320C5C | FULL | LUT component control register |
| SMARTIO_PRT12_DU_SEL | 0x40320CC0 | FULL | Data unit component input selection |
| SMARTIO_PRT12_DU_CTL | 0x40320CC4 | FULL | Data unit component control register |
| SMARTIO_PRT12_DATA | 0x40320CF0 | FULL | Data register |

25.2 PRT 13

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------------------|
| SMARTIO_PRT13_CTL | 0x40320D00 | FULL | Control register |
| SMARTIO_PRT13_SYNC_CTL | 0x40320D10 | FULL | Synchronization control register |
| SMARTIO_PRT13_LUT_SEL0 | 0x40320D20 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL1 | 0x40320D24 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL2 | 0x40320D28 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL3 | 0x40320D2C | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL4 | 0x40320D30 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL5 | 0x40320D34 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL6 | 0x40320D38 | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_SEL7 | 0x40320D3C | FULL | LUT component input selection |
| SMARTIO_PRT13_LUT_CTL0 | 0x40320D40 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL1 | 0x40320D44 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL2 | 0x40320D48 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL3 | 0x40320D4C | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL4 | 0x40320D50 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL5 | 0x40320D54 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL6 | 0x40320D58 | FULL | LUT component control register |
| SMARTIO_PRT13_LUT_CTL7 | 0x40320D5C | FULL | LUT component control register |
| SMARTIO_PRT13_DU_SEL | 0x40320DC0 | FULL | Data unit component input selection |
| SMARTIO_PRT13_DU_CTL | 0x40320DC4 | FULL | Data unit component control register |
| SMARTIO_PRT13_DATA | 0x40320DF0 | FULL | Data register |

25.3 PRT 14

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|----------------------------------|
| SMARTIO_PRT14_CTL | 0x40320E00 | FULL | Control register |
| SMARTIO_PRT14_SYNC_CTL | 0x40320E10 | FULL | Synchronization control register |
| SMARTIO_PRT14_LUT_SEL0 | 0x40320E20 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL1 | 0x40320E24 | FULL | LUT component input selection |

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------------------|
| SMARTIO_PRT14_LUT_SEL2 | 0x40320E28 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL3 | 0x40320E2C | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL4 | 0x40320E30 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL5 | 0x40320E34 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL6 | 0x40320E38 | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_SEL7 | 0x40320E3C | FULL | LUT component input selection |
| SMARTIO_PRT14_LUT_CTL0 | 0x40320E40 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL1 | 0x40320E44 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL2 | 0x40320E48 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL3 | 0x40320E4C | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL4 | 0x40320E50 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL5 | 0x40320E54 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL6 | 0x40320E58 | FULL | LUT component control register |
| SMARTIO_PRT14_LUT_CTL7 | 0x40320E5C | FULL | LUT component control register |
| SMARTIO_PRT14_DU_SEL | 0x40320EC0 | FULL | Data unit component input selection |
| SMARTIO_PRT14_DU_CTL | 0x40320EC4 | FULL | Data unit component control register |
| SMARTIO_PRT14_DATA | 0x40320EF0 | FULL | Data register |

25.4 PRT 15

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--------------------------------------|
| SMARTIO_PRT15_CTL | 0x40320F00 | FULL | Control register |
| SMARTIO_PRT15_SYNC_CTL | 0x40320F10 | FULL | Synchronization control register |
| SMARTIO_PRT15_LUT_SEL0 | 0x40320F20 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL1 | 0x40320F24 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL2 | 0x40320F28 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL3 | 0x40320F2C | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL4 | 0x40320F30 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL5 | 0x40320F34 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL6 | 0x40320F38 | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_SEL7 | 0x40320F3C | FULL | LUT component input selection |
| SMARTIO_PRT15_LUT_CTL0 | 0x40320F40 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL1 | 0x40320F44 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL2 | 0x40320F48 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL3 | 0x40320F4C | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL4 | 0x40320F50 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL5 | 0x40320F54 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL6 | 0x40320F58 | FULL | LUT component control register |
| SMARTIO_PRT15_LUT_CTL7 | 0x40320F5C | FULL | LUT component control register |
| SMARTIO_PRT15_DU_SEL | 0x40320FC0 | FULL | Data unit component input selection |
| SMARTIO_PRT15_DU_CTL | 0x40320FC4 | FULL | Data unit component control register |
| SMARTIO_PRT15_DATA | 0x40320FF0 | FULL | Data register |

25.5 PRT 17

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|----------------------------------|
| SMARTIO_PRT17_CTL | 0x40321100 | FULL | Control register |
| SMARTIO_PRT17_SYNC_CTL | 0x40321110 | FULL | Synchronization control register |
| SMARTIO_PRT17_LUT_SEL0 | 0x40321120 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL1 | 0x40321124 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL2 | 0x40321128 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL3 | 0x4032112C | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL4 | 0x40321130 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL5 | 0x40321134 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL6 | 0x40321138 | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_SEL7 | 0x4032113C | FULL | LUT component input selection |
| SMARTIO_PRT17_LUT_CTL0 | 0x40321140 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL1 | 0x40321144 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL2 | 0x40321148 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL3 | 0x4032114C | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL4 | 0x40321150 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL5 | 0x40321154 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL6 | 0x40321158 | FULL | LUT component control register |
| SMARTIO_PRT17_LUT_CTL7 | 0x4032115C | FULL | LUT component control register |

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|--------------------------------------|
| SMARTIO_PRT17_DU_SEL | 0x403211C0 | FULL | Data unit component input selection |
| SMARTIO_PRT17_DU_CTL | 0x403211C4 | FULL | Data unit component control register |
| SMARTIO_PRT17_DATA | 0x403211F0 | FULL | Data register |

25.6 Register Details

25.6.1 PRT

25.6.1.1 SMARTIO_PRT_CTL

Description: Control register
Address: 0x40320000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x2001400

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|--------------|----|------------------|----|----|---------------------|-----------------|
| Name | BYPASS [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | CLOCK_SRC [12:8] | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | None [30:26] | | | | | PIPELINE_EN [25:25] | HLD_OVR [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:7 | BYPASS | RW | R | Undefined | Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed. '0': No bypass (programmable SMARTIO fabric is exposed). '1': Bypass (programmable SMARTIO fabric is hidden). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 8:12 | CLOCK_SRC | RW | R | 20 | <p>Clock ('clk_fabric') and reset ('rst_fabric_n') source selection:</p> <p>'0': io_data_in[0]/'1'.</p> <p>...</p> <p>'7': io_data_in[7]/'1'.</p> <p>'8': chip_data[0]/'1'.</p> <p>...</p> <p>'15': chip_data[7]/'1'.</p> <p>'16': clk_smartio/rst_sys_act_n. Used for both Active functionality synchronous logic on 'clk_smartio'. This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_smartio_pos_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'.</p> <p>'17': clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on 'clk_smartio' (note that 'clk_smartio' is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ('clock_smartio_pos_en'). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to 'clk_sys'.</p> <p>'18': Same as '17'. Note that the M0S8 SMARTIO version used the Hibernate reset for this value, but the MXS40 SMARTIO version does not support Hibernate functionality.</p> <p>'19': clk_if/rst_if_dpslp_n (note that 'clk_if' is available in DeepSleep power mode). This selection is intended for synchronous operation on 'clk_if'. Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other 'clk_if' clocked elements.</p> <p>'20'-'30': Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption.</p> <p>'31': asynchronous mode/'1'. Select this when clockless operation is configured.</p> <p>NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block, but is not available for clocking.</p> |
| 24 | HLD_OVR | RW | R | Undefined | <p>IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO:</p> <p>'0': The HSIOM controls the IO cell hold override functionality ('hsiom_hld_ovr').</p> <p>'1': The SMARTIO controls the IO cel hold override functionality:</p> <ul style="list-style-type: none"> - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to 'pwr_hld_ovr_hib' to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 25 | PIPELINE_EN | RW | R | 1 | Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. |
| 31 | ENABLED | RW | R | 0 | <p>Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated.</p> <p>If the IP is disabled:</p> <ul style="list-style-type: none"> - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to '20'-'30' (clock is constant '0'), to ensure low power consumption. <p>'1': Enabled. Once enabled, it takes 3 'clk_fabric' clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional.</p> |

25.6.1.2 SMARTIO_PRT_SYNC_CTL

Description: Synchronization control register
Address: 0x40320010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|---|---|---|---|---|---|
| Name | IO_SYNC_EN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | CHIP_SYNC_EN [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:7 | IO_SYNC_EN | RW | R | Undefined | Synchronization of the IO pin input signals to 'clk_fabric', one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. |
| 8:15 | CHIP_SYNC_EN | RW | R | Undefined | Synchronization of the chip input signals to 'clk_fabric', one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. |

25.6.1.3 SMARTIO_PRT_LUT_SEL

Description: LUT component input selection
Address: 0x40320020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|---------------------|----|----|----|
| Name | None [7:4] | | | | LUT_TR0_SEL [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | LUT_TR1_SEL [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | LUT_TR2_SEL [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:3 | LUT_TR0_SEL | RW | R | Undefined | LUT input signal 'tr0_in' source selection: '0': Data unit output. '1': LUT 1 output. '2': LUT 2 output. '3': LUT 3 output. '4': LUT 4 output. '5': LUT 5 output. '6': LUT 6 output. '7': LUT 7 output. '8': chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). '9': chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). '10': chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). '11': chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). '12': io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). '13': io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). '14': io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). '15': io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 8:11 | LUT_TR1_SEL | RW | R | Undefined | LUT input signal 'tr1_in' source selection: '0': LUT 0 output. '1': LUT 1 output. '2': LUT 2 output. '3': LUT 3 output. '4': LUT 4 output. '5': LUT 5 output. '6': LUT 6 output. '7': LUT 7 output. '8': chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). '9': chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). '10': chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). '11': chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). '12': io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). '13': io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). '14': io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). '15': io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). |
| 16:19 | LUT_TR2_SEL | RW | R | Undefined | LUT input signal 'tr2_in' source selection. Encoding is the same as for LUT_TR1_SEL. |

25.6.1.4 SMARTIO_PRT_LUT_CTL

Description: LUT component control register
Address: 0x40320040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|---------------|----|
| Name | LUT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:10] | | | | | | LUT_OPC [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | LUT | RW | R | Undefined | LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). |
| 8:9 | LUT_OPC | RW | R | Undefined | <p>LUT opcode specifies the LUT operation:</p> <p>'0': Combinatorial output, no feedback. $tr_out = LUT[\{tr2_in, tr1_in, tr0_in\}]$.</p> <p>'1': Combinatorial output, feedback. $tr_out = LUT[\{lut_reg, tr1_in, tr0_in\}]$.</p> <p>On clock: $lut_reg \leq tr_in2$.</p> <p>'2': Sequential output, no feedback. $temp = LUT[\{tr2_in, tr1_in, tr0_in\}]$. $tr_out = lut_reg$.</p> <p>On clock: $lut_reg \leq temp$.</p> <p>'3': Register with asynchronous set and reset. $tr_out = lut_reg$. $enable = (tr2_in \wedge LUT[4]) \vee LUT[5]$. $set = enable \wedge (tr1_in \wedge LUT[2]) \wedge LUT[3]$. $clr = enable \wedge (tr0_in \wedge LUT[0]) \wedge LUT[1]$. Asynchronously (no clock required): $lut_reg \leq \text{if } (clr) '0' \text{ else if } (set) '1'$</p> |

25.6.1.5 SMARTIO_PRT_DU_SEL

Description: Data unit component input selection
Address: 0x403200C0
Offset: 0xC0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----------------------|----|--------------------|----|----------------------|----|
| Name | None [7:4] | | | | DU_TR0_SEL [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | DU_TR1_SEL [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | DU_TR2_SEL [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:30] | | DU_DATA1_SEL [29:28] | | None [27:26] | | DU_DATA0_SEL [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|--|
| 0:3 | DU_TR0_SEL | RW | R | Undefined | Data unit input signal 'tr0_in' source selection: '0': Constant '0'. '1': Constant '1'. '2': Data unit output. '10-3': LUT 7 - 0 outputs. Otherwise: Undefined. |
| 8:11 | DU_TR1_SEL | RW | R | Undefined | Data unit input signal 'tr1_in' source selection. Encoding is the same as for DU_TR0_SEL. |
| 16:19 | DU_TR2_SEL | RW | R | Undefined | Data unit input signal 'tr2_in' source selection. Encoding is the same as for DU_TR0_SEL. |
| 24:25 | DU_DATA0_SEL | RW | R | Undefined | Data unit input data 'data0_in' source selection: '0': Constant '0'. '1': chip_data[7:0]. '2': io_data_in[7:0]. '3': DATA.DATA MMIO register field. |
| 28:29 | DU_DATA1_SEL | RW | R | Undefined | Data unit input data 'data1_in' source selection. Encoding is the same as for DU_DATA0_SEL. |

25.6.1.6 SMARTIO_PRT_DU_CTL

Description: Data unit component control register
Address: 0x403200C4
Offset: 0xC4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---------------|---|---|
| Name | None [7:3] | | | | | DU_SIZE [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|---------------|---|---|
| Name | None [15:12] | | | | | DU_OPC [11:8] | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:2 | DU_SIZE | RW | R | Undefined | Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. |
| 8:11 | DU_OPC | RW | R | Undefined | Data unit opcode specifies the data unit operation: '1': INCR '2': DECR '3': INCR_WRAP '4': DECR_WRAP '5': INCR_DECR '6': INCR_DECR_WRAP '7': ROR '8': SHR '9': AND_OR '10': SHR_MAJ3 '11': SHR_EQL. Otherwise: Undefined. |

25.6.1.7 SMARTIO_PRT_DATA

Description: Data register
Address: 0x403200F0
Offset: 0xF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | DATA [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|------------------------------|
| 0:7 | DATA | RW | R | Undefined | Data unit input data source. |

26 SRSS

Description SRSS Core Registers (ver3)
Base Address 0x40260000
Size 0x10000
Slave Num MMIO2 - 5

| Register Name | Address | Permission | Description |
|------------------|------------|------------|---|
| PWR_LVD_STATUS | 0x40260040 | FULL | High Voltage / Low Voltage Detector (HVLVD) Status Register |
| PWR_LVD_STATUS2 | 0x40260044 | FULL | High Voltage / Low Voltage Detector (HVLVD) Status Register #2 |
| CLK_DSI_SELECT0 | 0x40260100 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT1 | 0x40260104 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT2 | 0x40260108 | FULL | Clock DSI Select Register |
| CLK_DSI_SELECT3 | 0x4026010C | FULL | Clock DSI Select Register |
| CLK_OUTPUT_FAST | 0x40260140 | FULL | Fast Clock Output Select Register |
| CLK_OUTPUT_SLOW | 0x40260144 | FULL | Slow Clock Output Select Register |
| CLK_CAL_CNT1 | 0x40260148 | FULL | Clock Calibration Counter 1 |
| CLK_CAL_CNT2 | 0x4026014C | FULL | Clock Calibration Counter 2 |
| SRSS_INTR | 0x40260200 | FULL | SRSS Interrupt Register |
| SRSS_INTR_SET | 0x40260204 | FULL | SRSS Interrupt Set Register |
| SRSS_INTR_MASK | 0x40260208 | FULL | SRSS Interrupt Mask Register |
| SRSS_INTR_MASKED | 0x4026020C | FULL | SRSS Interrupt Masked Register |
| PWR_CTL | 0x40261000 | FULL | Power Mode Control |
| PWR_CTL2 | 0x40261004 | FULL | Power Mode Control 2 Note: LINREG_LPMODE_RET_REG_DIS NWEELL_REG_DIS REFV_OK REFVBUF_LPMODE REFI_LPMODE PORBOD_LPMODE are not available for this register |
| PWR_HIBERNATE | 0x40261008 | FULL | HIBERNATE Mode Register |
| PWR_SSV_CTL | 0x40261018 | FULL | Supply Supervision Control Register |
| PWR_SSV_STATUS | 0x4026101C | FULL | Supply Supervision Status Register |
| PWR_LVD_CTL | 0x40261020 | FULL | High Voltage / Low Voltage Detector (HVLVD) Configuration Register Note: HVLVD1_TRIPSEL HVLVD1_SRCSEL HVLVD1_EN are not available for this register |
| PWR_LVD_CTL2 | 0x40261024 | FULL | High Voltage / Low Voltage Detector (HVLVD) Configuration Register #2 |
| PWR_HIB_DATA0 | 0x40261040 | FULL | HIBERNATE Data Register |
| CLK_PATH_SELECT0 | 0x40261200 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT1 | 0x40261204 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT2 | 0x40261208 | FULL | Clock Path Select Register |
| CLK_PATH_SELECT3 | 0x4026120C | FULL | Clock Path Select Register |
| CLK_ROOT_SELECT0 | 0x40261240 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT1 | 0x40261244 | FULL | Clock Root Select Register |
| CLK_ROOT_SELECT2 | 0x40261248 | FULL | Clock Root Select Register |
| CLK_SELECT | 0x40261500 | FULL | Clock selection register |
| CLK_TIMER_CTL | 0x40261504 | FULL | Timer Clock Control Register |
| CLK_ILO0_CONFIG | 0x40261508 | FULL | ILO0 Configuration |
| CLK_ILO1_CONFIG | 0x4026150C | FULL | ILO1 Configuration |
| CLK_IMO_CONFIG | 0x40261518 | FULL | IMO Configuration |
| CLK_ECO_CONFIG | 0x4026151C | FULL | ECO Configuration Register |
| CLK_ECO_PRESCALE | 0x40261520 | FULL | ECO Prescaler Configuration Register |
| CLK_ECO_STATUS | 0x40261524 | FULL | ECO Status Register |
| CLK_FLL_CONFIG | 0x40261530 | FULL | FLL Configuration Register |
| CLK_FLL_CONFIG2 | 0x40261534 | FULL | FLL Configuration Register 2 |
| CLK_FLL_CONFIG3 | 0x40261538 | FULL | FLL Configuration Register 3 |
| CLK_FLL_CONFIG4 | 0x4026153C | FULL | FLL Configuration Register 4 |
| CLK_FLL_STATUS | 0x40261540 | FULL | FLL Status Register |
| CLK_ECO_CONFIG2 | 0x40261544 | FULL | ECO Configuration Register 2 |
| CLK_PLL_CONFIG0 | 0x40261600 | FULL | PLL Configuration Register |
| CLK_PLL_STATUS0 | 0x40261640 | FULL | PLL Status Register |
| CSV_REF_SEL | 0x40261700 | FULL | Select CSV Reference clock for Active domain |

| Register Name | Address | Permission | Description |
|-----------------------------------|------------|------------|--|
| RES_CAUSE | 0x40261800 | FULL | Reset Cause Observation Register |
| RES_CAUSE2 | 0x40261804 | FULL | Reset Cause Observation Register 2 |
| TST_XRES_SECURE | 0x40262054 | READ | SECURE TEST and FIRMWARE TEST Key control register |
| RES_PXRES_CTL | 0x4026207C | READ | Programmable XRES Control Register |
| PWR_TRIM_WAKE_CTL | 0x40263008 | READ | Wakeup Trim Register |
| CLK_TRIM_ILO0_CTL | 0x40263014 | READ | ILO0 Trim Register |
| CLK_TRIM_ILO1_CTL | 0x40263220 | READ | ILO1 Trim Register |

26.1 CSV_HF

26.1.1 CSV 0

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|-------------------------------------|
| CSV_HF_CSV0_REF_CTL | 0x40261400 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV0_REF_LIMIT | 0x40261404 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV0_MON_CTL | 0x40261408 | FULL | Clock Supervision Monitor Control |

26.1.2 CSV 1

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|-------------------------------------|
| CSV_HF_CSV1_REF_CTL | 0x40261410 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV1_REF_LIMIT | 0x40261414 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV1_MON_CTL | 0x40261418 | FULL | Clock Supervision Monitor Control |

26.1.3 CSV 2

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|-------------------------------------|
| CSV_HF_CSV2_REF_CTL | 0x40261420 | FULL | Clock Supervision Reference Control |
| CSV_HF_CSV2_REF_LIMIT | 0x40261424 | FULL | Clock Supervision Reference Limits |
| CSV_HF_CSV2_MON_CTL | 0x40261428 | FULL | Clock Supervision Monitor Control |

26.2 CSV_REF

26.2.1 CSV

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|-------------------------------------|
| CSV_REF_CSV_REF_CTL | 0x40261710 | FULL | Clock Supervision Reference Control |
| CSV_REF_CSV_REF_LIMIT | 0x40261714 | FULL | Clock Supervision Reference Limits |
| CSV_REF_CSV_MON_CTL | 0x40261718 | FULL | Clock Supervision Monitor Control |

26.3 CSV_LF

26.3.1 CSV

| Register Name | Address | Permission | Description |
|--------------------------------------|------------|------------|-------------------------------------|
| CSV_LF_CSV_REF_CTL | 0x40261720 | FULL | Clock Supervision Reference Control |
| CSV_LF_CSV_REF_LIMIT | 0x40261724 | FULL | Clock Supervision Reference Limits |
| CSV_LF_CSV_MON_CTL | 0x40261728 | FULL | Clock Supervision Monitor Control |

26.4 CSV_ILO

26.4.1 CSV

| Register Name | Address | Permission | Description |
|---------------------------------------|------------|------------|-------------------------------------|
| CSV_ILO_CSV_REF_CTL | 0x40261730 | FULL | Clock Supervision Reference Control |
| CSV_ILO_CSV_REF_LIMIT | 0x40261734 | FULL | Clock Supervision Reference Limits |
| CSV_ILO_CSV_MON_CTL | 0x40261738 | FULL | Clock Supervision Monitor Control |

26.5 MCWDT 0

| Register Name | Address | Permission | Description |
|------------------------------------|------------|------------|---|
| MCWDT0_CPU_SELECT | 0x40268040 | FULL | MCWDT CPU selection register |
| MCWDT0_CTR2_CTL | 0x40268080 | FULL | MCWDT Subcounter 2 Control register |
| MCWDT0_CTR2_CONFIG | 0x40268084 | FULL | MCWDT Subcounter 2 Configuration register |
| MCWDT0_CTR2_CNT | 0x40268088 | FULL | MCWDT Subcounter 2 Count Register |
| MCWDT0_LOCK | 0x40268090 | FULL | MCWDT Lock Register |
| MCWDT0_SERVICE | 0x40268094 | FULL | MCWDT Service Register |
| MCWDT0_INTR | 0x402680A0 | FULL | MCWDT Interrupt Register |
| MCWDT0_INTR_SET | 0x402680A4 | FULL | MCWDT Interrupt Set Register |

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|---------------------------------|
| MCWDT0_INTR_MASK | 0x402680A8 | FULL | MCWDT Interrupt Mask Register |
| MCWDT0_INTR_MASKED | 0x402680AC | FULL | MCWDT Interrupt Masked Register |

26.5.1 CTR 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| MCWDT0_CTR0_CTL | 0x40268000 | FULL | MCWDT Subcounter Control Register |
| MCWDT0_CTR0_LOWER_LIMIT | 0x40268004 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT0_CTR0_UPPER_LIMIT | 0x40268008 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT0_CTR0_WARN_LIMIT | 0x4026800C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT0_CTR0_CONFIG | 0x40268010 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT0_CTR0_CNT | 0x40268014 | FULL | MCWDT Subcounter Count Register |

26.5.2 CTR 1

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| MCWDT0_CTR1_CTL | 0x40268020 | FULL | MCWDT Subcounter Control Register |
| MCWDT0_CTR1_LOWER_LIMIT | 0x40268024 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT0_CTR1_UPPER_LIMIT | 0x40268028 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT0_CTR1_WARN_LIMIT | 0x4026802C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT0_CTR1_CONFIG | 0x40268030 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT0_CTR1_CNT | 0x40268034 | FULL | MCWDT Subcounter Count Register |

26.6 MCWDT 1

| Register Name | Address | Permission | Description |
|--------------------|------------|------------|---|
| MCWDT1_CPU_SELECT | 0x40268140 | FULL | MCWDT CPU selection register |
| MCWDT1_CTR2_CTL | 0x40268180 | FULL | MCWDT Subcounter 2 Control register |
| MCWDT1_CTR2_CONFIG | 0x40268184 | FULL | MCWDT Subcounter 2 Configuration register |
| MCWDT1_CTR2_CNT | 0x40268188 | FULL | MCWDT Subcounter 2 Count Register |
| MCWDT1_LOCK | 0x40268190 | FULL | MCWDT Lock Register |
| MCWDT1_SERVICE | 0x40268194 | FULL | MCWDT Service Register |
| MCWDT1_INTR | 0x402681A0 | FULL | MCWDT Interrupt Register |
| MCWDT1_INTR_SET | 0x402681A4 | FULL | MCWDT Interrupt Set Register |
| MCWDT1_INTR_MASK | 0x402681A8 | FULL | MCWDT Interrupt Mask Register |
| MCWDT1_INTR_MASKED | 0x402681AC | FULL | MCWDT Interrupt Masked Register |

26.6.1 CTR 0

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| MCWDT1_CTR0_CTL | 0x40268100 | FULL | MCWDT Subcounter Control Register |
| MCWDT1_CTR0_LOWER_LIMIT | 0x40268104 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT1_CTR0_UPPER_LIMIT | 0x40268108 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT1_CTR0_WARN_LIMIT | 0x4026810C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT1_CTR0_CONFIG | 0x40268110 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT1_CTR0_CNT | 0x40268114 | FULL | MCWDT Subcounter Count Register |

26.6.2 CTR 1

| Register Name | Address | Permission | Description |
|-------------------------|------------|------------|---|
| MCWDT1_CTR1_CTL | 0x40268120 | FULL | MCWDT Subcounter Control Register |
| MCWDT1_CTR1_LOWER_LIMIT | 0x40268124 | FULL | MCWDT Subcounter Lower Limit Register |
| MCWDT1_CTR1_UPPER_LIMIT | 0x40268128 | FULL | MCWDT Subcounter Upper Limit Register |
| MCWDT1_CTR1_WARN_LIMIT | 0x4026812C | FULL | MCWDT Subcounter Warn Limit Register |
| MCWDT1_CTR1_CONFIG | 0x40268130 | FULL | MCWDT Subcounter Configuration Register |
| MCWDT1_CTR1_CNT | 0x40268134 | FULL | MCWDT Subcounter Count Register |

26.7 WDT

| Register Name | Address | Permission | Description |
|-----------------|------------|------------|----------------------------|
| WDT_CTL | 0x4026C000 | FULL | WDT Control Register |
| WDT_LOWER_LIMIT | 0x4026C004 | FULL | WDT Lower Limit Register |
| WDT_UPPER_LIMIT | 0x4026C008 | FULL | WDT Upper Limit Register |
| WDT_WARN_LIMIT | 0x4026C00C | FULL | WDT Warn Limit Register |
| WDT_CONFIG | 0x4026C010 | FULL | WDT Configuration Register |
| WDT_CNT | 0x4026C014 | FULL | WDT Count Register |
| WDT_LOCK | 0x4026C040 | FULL | WDT Lock register |
| WDT_SERVICE | 0x4026C044 | FULL | WDT Service register |

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|-------------------------------|
| WDT_INTR | 0x4026C050 | FULL | WDT Interrupt Register |
| WDT_INTR_SET | 0x4026C054 | FULL | WDT Interrupt Set Register |
| WDT_INTR_MASK | 0x4026C058 | FULL | WDT Interrupt Mask Register |
| WDT_INTR_MASKED | 0x4026C05C | FULL | WDT Interrupt Masked Register |

26.8 Register Details

26.8.1 PWR_LVD_STATUS

Description: High Voltage / Low Voltage Detector (HVLVD) Status Register
Address: 0x40260040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Real-time status for Voltage Monitoring System
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------------|
| Name | None [7:1] | | | | | | | HVLVD1_OUT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | HVLVD1_OUT | R | RW | 0 | HVLVD1 output. 0: below voltage threshold 1: above voltage threshold |

26.8.2 PWR_LVD_STATUS2

Description: High Voltage / Low Voltage Detector (HVLVD) Status Register #2
Address: 0x40260044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Real-time status for Voltage Monitoring System
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|------------------|
| Name | None [7:1] | | | | | | | HVLVD2_OUT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0 | HVLVD2_OUT | R | RW | 0 | HVLVD2 output. 0: below voltage threshold 1: above voltage threshold |

26.8.3 CLK_DSI_SELECT

Description: Clock DSI Select Register
Address: 0x40260100
Offset: 0x100
Retention: Retained
IsDeepSleep: Yes
Comment: Configures DSI mux in clock generation path. Each path has its own copy of this register. See PAS for DSI signal connectivity list.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---------------|---|---|---|---|
| Name | None [7:5] | | | DSI_MUX [4:0] | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 0:4 | DSI_MUX | RW | R | 0 | Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH<i></i> using CLK_PATH_SELECT register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or as reference inputs for the FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. |
| | DSI_OUT0 | | | 0 | DSI0 - dsi_out[0] |
| | DSI_OUT1 | | | 1 | DSI1 - dsi_out[1] |
| | DSI_OUT2 | | | 2 | DSI2 - dsi_out[2] |
| | DSI_OUT3 | | | 3 | DSI3 - dsi_out[3] |
| | DSI_OUT4 | | | 4 | DSI4 - dsi_out[4] |
| | DSI_OUT5 | | | 5 | DSI5 - dsi_out[5] |
| | DSI_OUT6 | | | 6 | DSI6 - dsi_out[6] |
| | DSI_OUT7 | | | 7 | DSI7 - dsi_out[7] |
| | DSI_OUT8 | | | 8 | DSI8 - dsi_out[8] |
| | DSI_OUT9 | | | 9 | DSI9 - dsi_out[9] |
| | DSI_OUT10 | | | 10 | DSI10 - dsi_out[10] |
| | DSI_OUT11 | | | 11 | DSI11 - dsi_out[11] |
| | DSI_OUT12 | | | 12 | DSI12 - dsi_out[12] |
| | DSI_OUT13 | | | 13 | DSI13 - dsi_out[13] |
| | DSI_OUT14 | | | 14 | DSI14 - dsi_out[14] |
| | DSI_OUT15 | | | 15 | DSI15 - dsi_out[15] |
| | ILO0 | | | 16 | ILO0 - Internal Low-speed Oscillator #0 |
| | WCO | | | 17 | WCO - Watch-Crystal Oscillator |
| | ALTIF | | | 18 | ALTIF - Alternate Low-Frequency Clock |
| | PILO | | | 19 | PILO - Precision Internal Low-speed Oscillator |
| | ILO1 | | | 20 | ILO1 - Internal Low-speed Oscillator #1, if present. |

26.8.4 CLK_OUTPUT_FAST

Description: Fast Clock Output Select Register
Address: 0x40260140
Offset: 0x140
Retention: Retained
IsDeepSleep: Yes
Comment: Selects clocks for calibration
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|----|--------------------|----|----|----|
| Name | PATH_SEL0 [7:4] | | | | FAST_SEL0 [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | HFCLK_SEL0 [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PATH_SEL1 [23:20] | | | | FAST_SEL1 [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:28] | | | | HFCLK_SEL1 [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|---|
| 0:3 | FAST_SEL0 | RW | R | 0 | Select signal for fast clock output #0 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0. |
| | ECO | | | 1 | External Crystal Oscillator (ECO) |
| | EXTCLK | | | 2 | External clock input (EXTCLK) |
| | ALTHF | | | 3 | Alternate High-Frequency (ALTHF) clock input to SRSS |
| | TIMERCLK | | | 4 | Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. |
| | PATH_SEL0 | | | 5 | Selects the clock path chosen by PATH_SEL0 field |
| | HFCLK_SEL0 | | | 6 | Selects the output of the HFCLK_SEL0 mux |
| 4:7 | SLOW_SEL0 | | | 7 | Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0 |
| | PATH_SEL0 | RW | R | 0 | Selects a clock path to use in fast clock output #0 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) |
| | HFCLK_SEL0 | RW | R | 0 | Selects a HFCLK tree for use in fast clock output #0 |
| | FAST_SEL1 | RW | R | 0 | Select signal for fast clock output #1 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1. |
| | ECO | | | 1 | External Crystal Oscillator (ECO) |
| | EXTCLK | | | 2 | External clock input (EXTCLK) |
| | ALTHF | | | 3 | Alternate High-Frequency (ALTHF) clock input to SRSS |
| 16:19 | TIMERCLK | | | 4 | Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. |
| | PATH_SEL1 | | | 5 | Selects the clock path chosen by PATH_SEL1 field |
| | HFCLK_SEL1 | | | 6 | Selects the output of the HFCLK_SEL1 mux |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------|----|----|-----------------|--|
| | SLOW_SEL1 | | | 7 | Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1 |
| 20:23 | PATH_SEL1 | RW | R | 0 | Selects a clock path to use in fast clock output #1 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) |
| 24:27 | HFCLK_SEL1 | RW | R | 0 | Selects a HFCLK tree for use in fast clock output #1 logic |

26.8.5 CLK_OUTPUT_SLOW

Description: Slow Clock Output Select Register
Address: 0x40260144
Offset: 0x144
Retention: Retained
IsDeepSleep: Yes
Comment: Selects a slow clock for calibration. The outputs of these muxes go into CLK_OUTPUT_FAST.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|-----------------|----|----|----|
| Name | SLOW_SEL1 [7:4] | | | | SLOW_SEL0 [3:0] | | | |
| | | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| | | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| | | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|---|
| 0:3 | SLOW_SEL0 | RW | R | 0 | Select signal for slow clock output #0 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. |
| | ILO0 | | | 1 | Internal Low Speed Oscillator (ILO0) |
| | WCO | | | 2 | Watch-Crystal Oscillator (WCO) |
| | BAK | | | 3 | Root of the Backup domain clock tree (BAK) |
| | ALTLF | | | 4 | Alternate low-frequency clock input to SRSS (ALTLF) |
| | LFCLK | | | 5 | Root of the low-speed clock tree (LFCLK) |
| | IMO | | | 6 | Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |
| | SLPCTRL | | | 7 | Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |
| | PILO | | | 8 | Precision Internal Low Speed Oscillator (PILO) |
| | ILO1 | | | 9 | Internal Low Speed Oscillator (ILO1), if present on the product. |
| | ECO_PRESCALER | | | 10 | ECO Prescaler (ECO_PRESCALER) |
| | LPECO | | | 11 | LPECO |
| | LPECO_PRESCALER | | | 12 | LPECO Prescaler (LPECO_PRESCALER) |
| 4:7 | SLOW_SEL1 | RW | R | 0 | Select signal for slow clock output #1 |
| | NC | | | 0 | Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. |
| | ILO0 | | | 1 | Internal Low Speed Oscillator (ILO) |
| | WCO | | | 2 | Watch-Crystal Oscillator (WCO) |
| | BAK | | | 3 | Root of the Backup domain clock tree (BAK) |
| | ALTLF | | | 4 | Alternate low-frequency clock input to SRSS (ALTLF) |
| | LFCLK | | | 5 | Root of the low-speed clock tree (LFCLK) |
| | IMO | | | 6 | Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|---|
| | SLPCTRL | | | 7 | Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. |
| | PILO | | | 8 | Precision Internal Low Speed Oscillator (PILO) |
| | ILO1 | | | 9 | Internal Low Speed Oscillator (ILO1), if present on the product. |
| | ECO_PRESCALER | | | 10 | ECO Prescaler (ECO_PRESCALER) |
| | LPECO | | | 11 | LPECO |
| | LPECO_PRESCALER | | | 12 | LPECO Prescaler (LPECO_PRESCALER) |

26.8.6 CLK_CAL_CNT1

Description: Clock Calibration Counter 1
Address: 0x40260148
Offset: 0x148
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x80000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------------|--------------|----|----|----|----|----|----|
| Name | CAL_COUNTER1 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CAL_COUNTER1 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CAL_COUNTER1 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CAL_COUNTER_DONE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:23 | CAL_COUNTER1 | RW | A | 0 | Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and discarding the first result. |
| 31 | CAL_COUNTER_DONE | R | W | 1 | Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up |

26.8.7 CLK_CAL_CNT2

Description: Clock Calibration Counter 2
Address: 0x4026014C
Offset: 0x14C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|----|----|----|----|----|----|----|
| Name | CAL_COUNTER2 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CAL_COUNTER2 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CAL_COUNTER2 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:23 | CAL_COUNTER2 | R | RW | 0 | Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: $\text{CLK_CAL_CNT2.COUNTER} = (\text{F_cnt2} / \text{F_cnt1}) * (\text{CLK_CAL_CNT1.COUNTER})$ |

26.8.8 SRSS_INTR

Description: SRSS Interrupt Register
Address: 0x40260200
Offset: 0x200
Retention: Retained
IsDeepSleep: Yes
Comment: Interrupt signal from SRSS includes this register and also BACKUP_INTR, if present.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------------|------------|---|-----------------|-----------------|------------|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|----|-----------------|---|
| 1 | HVLVD1 | RW1C | A | 0 | Interrupt for low voltage detector HVLVD1 |
| 2 | HVLVD2 | RW1C | A | 0 | Interrupt for low voltage detector HVLVD2 |
| 5 | CLK_CAL | RW1C | A | 0 | Clock calibration counter is done. This field is reset during DEEPSLEEP mode. |

26.8.9 SRSS_INTR_SET

Description: SRSS Interrupt Set Register
Address: 0x40260204
Offset: 0x204
Retention: Retained
IsDeepSleep: Yes
Comment: Can be used to set interrupts for firmware testing.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|------------------|------------|---|-----------------|-----------------|------------|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|----|-----------------|--|
| 1 | HVLVD1 | RW1S | A | 0 | Set interrupt for low voltage detector HVLVD1 |
| 2 | HVLVD2 | RW1S | A | 0 | Set interrupt for low voltage detector HVLVD2 |
| 5 | CLK_CAL | RW1S | A | 0 | Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. |

26.8.10 SRSS_INTR_MASK

Description: SRSS Interrupt Mask Register
Address: 0x40260208
Offset: 0x208
Retention: Retained
IsDeepSleep: Yes
Comment: Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---------------|------------|---|--------------|--------------|------------|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--------------------------------------|
| 1 | HVLVD1 | RW | R | 0 | Mask for low voltage detector HVLVD1 |
| 2 | HVLVD2 | RW | R | 0 | Mask for low voltage detector HVLVD2 |
| 5 | CLK_CAL | RW | R | 0 | Mask for clock calibration done |

26.8.11 SRSS_INTR_MASKED

Description: SRSS Interrupt Masked Register
Address: 0x4026020C
Offset: 0x20C
Retention: Retained
IsDeepSleep: Yes
Comment: Bitwise and between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---------------|------------|---|--------------|--------------|------------|
| Name | None [7:6] | | CLK_CAL [5:5] | None [4:3] | | HVLVD2 [2:2] | HVLVD1 [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 1 | HVLVD1 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 2 | HVLVD2 | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 5 | CLK_CAL | R | RW | 0 | Logical and of corresponding request and mask bits. |

26.8.12 PWR_CTL

Description: Power Mode Control
Address: 0x40261000
Offset: 0x1000
Retention: Retained
IsDeepSleep: Yes
Comment: Controls the device power mode options and allows observation of current state.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|-----------------|---------------------|------------|---|------------------|---|
| Name | None [7:6] | | LPM_READY [5:5] | DEBUG_SESSION [4:4] | None [3:2] | | POWER_MODE [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0:1 | POWER_MODE | R | RW | 0 | Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. |
| | RESET | | | 0 | System is resetting. |
| | ACTIVE | | | 1 | At least one CPU is running. |
| | SLEEP | | | 2 | No CPUs are running. Peripherals may be running. |
| | DEEPSLEEP | | | 3 | Main high-frequency clock is off; low speed clocks are available. Communication interface clocks may be present. |
| 4 | DEBUG_SESSION | R | RW | 0 | Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) |
| | NO_SESSION | | | 0 | No debug session active |
| | SESSION_ACTIVE | | | 1 | Debug session is active. Power modes behave differently to keep the debug session active. |
| 5 | LPM_READY | R | RW | 0 | Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES, HIBERNATE wakeup, or supply supervision reset wakeup than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit. 0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. |

26.8.13 PWR_CTL2

Description: Power Mode Control 2
Address: 0x40261004
Offset: 0x1004
Retention: Retained
IsDeepSleep: Yes
Comment: Controls the device power mode options and allows observation of current state.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---------------------|------------|---------------------|-----------------|------------------|
| Name | None [7:5] | | | DPSLP_REG_DIS [4:4] | None [3:3] | LINREG_LPMODE [2:2] | LINREG_OK [1:1] | LINREG_DIS [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|-----------------------|-------------|----|---|-------------------|
| Name | None [15:13] | | | NWELL_REG_DIS [12:12] | None [11:9] | | | RET_REG_DIS [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|------------------------|--------------------|---------------------|--------------|----|-----------------|------------------|
| Name | None [23:23] | REFVBUF_LPMODE [22:22] | REFVBUF_OK [21:21] | REFVBUF_DIS [20:20] | None [19:18] | | REFV_OK [17:17] | REFV_DIS [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------------|--------------|----|----------------------|-----------------------|---------------------|-----------------|------------------|
| Name | PLL_LS_BY_PASS [31:31] | None [30:29] | | BGREF_LPMODE [28:28] | PORBOD_LPMODE [27:27] | REFI_LPMODE [26:26] | REFI_OK [25:25] | REFI_DIS [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| 0 | LINREG_DIS | RW | A | 0 | Explicitly disable the linear Core Regulator. Write zero for Traveo II devices. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Linear Core Regulator is not explicitly disabled. Hardware disables it automatically for internal sequences, including for DEEPSLEEP, HIBERNATE, and XRES low power modes. 1: Linear Core Regulator is explicitly disabled. Only use this for special cases when another source supplies vccd during ACTIVE and SLEEP modes. This setting is only legal when another source supplies vccd, but there is no special hardware protection for this case. |
| 1 | LINREG_OK | R | RW | 0 | Status of the linear Core Regulator. |
| 2 | LINREG_LPMODE | RW | A | 0 | Control the power mode of the Linear Regulator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Linear Regulator operates in normal mode. Internal current consumption is 50uA and load current capability is 50mA to 300mA, depending on the number of regulator modules present in the product. 1: Linear Regulator operates in low power mode. Internal current consumption is 5uA and load current capability is 25mA. Firmware must ensure the current is kept within the limit. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 4 | DPSLP_REG_DIS | RW | A | 0 | <p>Explicitly disable the DeepSleep regulator, including circuits shared with the Active Regulator. This register must not be set except as part of a Cypress-provided sequence or API, such as the PMIC case described below. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. If the DeepSleep regulator is disabled, it is not supported to enable it again later by clearing this bit.</p> <p>0: DeepSleep Regulator is not explicitly disabled. This is the normal setting, and hardware automatically controls the DeepSleep regulator for most sequences, including for HIBERNATE and XRES low power modes. This setting must be used if the Active Linear Regulator is used, because some circuitry is shared.</p> <p>1: DeepSleep Regulator is explicitly disabled. Only use this for special cases when another source supplies vccdpslp during DEEPSLEEP mode and there is no future intention to use the Active Regulator for ACTIVE/SLEEP modes. For example, this setting is used as part of a Cypress-provided handover sequence to a PMIC that operates in ACTIVE, SLEEP, and DEEPSLEEP and disables both the Active Linear Regulator and DeepSleep Regulator.</p> |
| 8 | RET_REG_DIS | RW | A | 0 | <p>Explicitly disable the Retention regulator. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset.</p> <p>0: Retention Regulator is not explicitly disabled. Hardware disables it automatically for internal sequences, including for HIBERNATE and XRES low power modes. Hardware keeps the Retention Regulator enabled during ACTIVE/SLEEP modes, so it is ready to enter DEEPSLEEP at any time.</p> <p>1: Retention Regulator is explicitly disabled. Only use this for special cases when another source supplies vccret during DEEPSLEEP mode. This setting is only legal when another source supplies vccret, but there is no special hardware protection for this case.</p> |
| 12 | NWELL_REG_DIS | RW | A | 0 | <p>Explicitly disable the Nwell regulator. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset.</p> <p>0: Nwell Regulator is on. Hardware disables it automatically for internal sequences, including for HIBERNATE and XRES low power modes. Hardware keeps the Nwell Regulator enabled during ACTIVE/SLEEP modes, so it is ready to enter DEEPSLEEP at any time.</p> <p>1: Nwell Regulator is explicitly disabled. Only use this for special cases when another source supplies vnwell during DEEPSLEEP mode. This setting is only legal when another source supplies vnwell, but there is no special hardware protection for this case.</p> |
| 16 | REFV_DIS | RW | A | 0 | <p>Disables the voltage reference.</p> <p>PSoC products: This disables the Active voltage reference. Firmware must ensure that LPM_READY==1 and BGREF_LPMODE==1 for at least 1us before disabling the Active Reference. When enabling the Active Reference, use REFV_OK indicator to know when it is ready. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset.</p> <p>Traveo II products: Reserved. Write zero.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 17 | REFV_OK | R | RW | 0 | Indicates that the normal mode of the voltage reference is ready. |
| 20 | REFVBUF_DIS | RW | A | 0 | Disable the voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the PLL and ECO. A particular product may have circuits outside the SRSS that use the buffer. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. |
| 21 | REFVBUF_OK | R | RW | 0 | Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFVBUF_DIS=1. |
| 22 | REFVBUF_LPMODE | RW | A | 0 | Control the power mode of the 800mV voltage reference buffer. The value in this register is ignored and normal mode is used until LPM_READY==1. 0: Voltage Reference Buffer operates in normal mode. They work for vddd ramp rates of 100mV/us or less. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 1: Voltage Reference Buffer operates in low power mode. Power supply rejection is reduced to save current, and they work for vddd ramp rates of 10mV/us or less. |
| 24 | REFI_DIS | RW | A | 0 | Reserved. Write zero. |
| 25 | REFI_OK | R | RW | 0 | Indicates that the current reference is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFI_DIS=1. |
| 26 | REFI_LPMODE | RW | A | 0 | Control the power mode of the reference current generator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Current reference generator operates in normal mode. It works for vddd ramp rates of 100mV/us or less. 1: Current reference generator operates in low power mode. Response time is reduced to save current, and it works for vddd ramp rates of 10mV/us or less. |
| 27 | PORBOD_LPMODE | RW | A | 0 | Control the power mode of the POR/BOD circuits. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: POR/BOD circuits operate in normal mode. They work for vddd ramp rates of 100mV/us or less. 1: POR/BOD circuits operate in low power mode. Response time is reduced to save current, and they work for vddd ramp rates of 10mV/us or less. |
| 28 | BGREF_LPMODE | RW | A | 0 | Control the circuit-level power mode of the Bandgap Reference circuits. 0: Bandgap Reference circuits operate in higher current mode. 1: Bandgap Reference circuits operate in low power. Refer to documentation for restrictions. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 31 | PLL_LS_BYPASS | RW | R | 0 | <p>Bypass level shifter inside the PLL. Unused, if no PLL is present in the product.</p> <p>0: Do not bypass the level shifter. This setting is ok for all operational modes and vccd target voltage.</p> <p>1: Bypass the level shifter. This may reduce jitter on the PLL output clock, but can only be used when vccd is targeted to 1.1V nominal. Otherwise, it can result in clock degradation and static current.</p> |

26.8.14 PWR_HIBERNATE

Description: HIBERNATE Mode Register

Address: 0x40261008

Offset: 0x1008

Retention: Retained

IsDeepSleep: No

Comment: This register controls entry/exit from HIBERNATE power mode. This register is implemented in the unregulated voltage domain. This register and PWR_HIB_DATA registers are the only ones that continue to retain information during HIBERNATE mode. Three identical writes are required to enter HIBERNATE mode. Ensure changes settle after the third write by reading this register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | TOKEN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------|----|----|----|----|----|---|---|
| Name | UNLOCK [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------------|----|----|----|---------------------|-----------------------|----------------|--------------|
| Name | POLARITY_HIBPIN [23:20] | | | | MASK_HIBWDT [19:19] | MASK_HIBALARM [18:18] | FREEZE [17:17] | None [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|---------------------------|--------------|----|---------------------|----|----|----|
| Name | HIBERNATE [31:31] | HIBERNATE_DISABLE [30:30] | None [29:28] | | MASK_HIBPIN [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| 0:7 | TOKEN | RW | A | 0 | Contains a 8-bit token that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES will reset this register. |
| 8:15 | UNLOCK | RW | A | 0 | This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/HIBERNATE to have no effect, except as noted in the FREEZE description. |
| 17 | FREEZE | RW | A | 0 | Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Supply supervision is disabled during HIBERNATE mode. HIBERNATE peripherals ignore resets (excluding XRES) while FREEZE==1. |
| 18 | MASK_HIBALARM | RW | A | 0 | When set, HIBERNATE will wakeup for a RTC interrupt |
| 19 | MASK_HIBWDT | RW | A | 0 | When set, HIBERNATE will wakeup for WDT interrupt |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|------|----|-----------------|--|
| 20:23 | POLARITY_HIBPIN | RW | A | 0 | Each bit sets the active polarity of the corresponding wakeup pin. 0: Pin input of 0 will wakeup the part from HIBERNATE 1: Pin input of 1 will wakeup the part from HIBERNATE |
| 24:27 | MASK_HIBPIN | RW | A | 0 | When set, HIBERNATE will wakeup if the corresponding pin input matches the POLARITY_HIBPIN setting. Each bit corresponds to one of the wakeup pins. |
| 30 | HIBERNATE_DISABLE | RW1S | R | 0 | Hibernate disable bit. 0: Normal operation, HIBERNATE works as described 1: Further writes to this register are ignored Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. |
| 31 | HIBERNATE | RW | A | 0 | Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. |

26.8.15 PWR_SSV_CTL

Description: Supply Supervision Control Register
Address: 0x40261018
Offset: 0x1018
Retention: Retained
IsDeepSleep: Yes
Comment: Controls for brownout and over-voltage detectors. Fields *_VSEL and *_ACTION are only reset by XRES/POR/BOD/OVD/OCD/HIBERNATE. Fields *_ENABLE are reset by all resets.
Default: 0x8080808

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|------------|------------|--------------------|----------------------|------------|------------|--------------------|
| Name | BODVDDA_ACTION [7:6] | None [5:5] | None [5:5] | BODVDDA_VSEL [4:4] | BODVDDD_ENABLE [3:3] | None [2:1] | None [2:1] | BODVDDD_VSEL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|--------------|--------------|--------------|------------------------|-------------|-------------|----------------------|
| Name | None [15:12] | None [15:12] | None [15:12] | None [15:12] | BODVCCD_ENABLE [11:11] | None [10:9] | None [10:9] | BODVDDA_ENABLE [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------------|------------------------|--------------|----------------------|------------------------|--------------|--------------|----------------------|
| Name | OVDVDDA_ACTION [23:22] | OVDVDDA_ACTION [23:22] | None [21:21] | OVDVDDA_VSEL [20:20] | OVDVDDD_ENABLE [19:19] | None [18:17] | None [18:17] | OVDVDDD_VSEL [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|--------------|--------------|--------------|------------------------|--------------|--------------|------------------------|
| Name | None [31:28] | None [31:28] | None [31:28] | None [31:28] | OVDVCCD_ENABLE [27:27] | None [26:25] | None [26:25] | OVDVDDA_ENABLE [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0 | BODVDDD_VSEL | RW | A | 0 | Selects the voltage threshold for BOD on vddd. The BOD does not reliably monitor the supply during the transition. 0: vddd<2.7V 1: vddd<3.0V |
| 3 | BODVDDD_ENABLE | RW | A | 1 | Enable for BOD on vddd. This cannot be disabled during normal operation. |
| 4 | BODVDDA_VSEL | RW | A | 0 | Selects the voltage threshold for BOD on vdda. Ensure BODVDDA_ENABLE==0 before changing this setting to prevent false triggers. 0: vdda<2.7V 1: vdda<3.0V |
| 6:7 | BODVDDA_ACTION | RW | A | 0 | Action taken when the BOD on vdda triggers. |
| | NOTHING | | | 0 | No action |
| | FAULT | | | 1 | Generate a fault |
| | RESET | | | 2 | Reset the chip |
| 8 | BODVDDA_ENABLE | RW | A | 0 | Enable for BOD on vdda. BODVDDA_ACTION will be triggered when the BOD is disabled. If no action is desired when disabling, firmware must first write BODVDDA_ACTION=NOTHING in a separate write cycle. |
| 11 | BODVCCD_ENABLE | RW | A | 1 | Enable for BOD on vccd. This cannot be disabled during normal operation. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------|----|----|-----------------|--|
| 16 | OVDVDDD_VSEL | RW | A | 0 | Selects the voltage threshold for OVD on vddd. The OVD does not reliably monitor the supply during the transition. 0: vddd>5.5V 1: vddd>5.0V |
| 19 | OVDVDDD_ENABLE | RW | A | 1 | Enable for OVD on vddd. This cannot be disabled during normal operation. |
| 20 | OVDVDDA_VSEL | RW | A | 0 | Selects the voltage threshold for OVD on vdda. Ensure OVDVDDA_ENABLE==0 before changing this setting to prevent false triggers 0: vddd>5.5V 1: vddd>5.0V |
| 22:23 | OVDVDDA_ACTION | RW | A | 0 | Action taken when the OVD on vdda triggers. |
| | NOTHING | | | 0 | No action |
| | FAULT | | | 1 | Generate a fault |
| | RESET | | | 2 | Reset the chip |
| 24 | OVDVDDA_ENABLE | RW | A | 0 | Enable for OVD on vdda. |
| 27 | OVDVCCD_ENABLE | RW | A | 1 | Enable for OVD on vccd. This cannot be disabled during normal operation. |

26.8.16 PWR_SSV_STATUS

Description: Supply Supervision Status Register
Address: 0x4026101C
Offset: 0x101C
Retention: Retained
IsDeepSleep: Yes
Comment: Status for brownout and over-voltage detectors.
Default: 0x30505

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|------------------|------------------|------------------|
| Name | None [7:3] | | | | | BODVCCD_OK [2:2] | BODVDDA_OK [1:1] | BODVDDD_OK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|--------------------|------------------|------------------|
| Name | None [15:11] | | | | | OVDVCCD_OK [10:10] | OVDVDDA_OK [9:9] | OVDVDDD_OK [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|--------------------------|---------------------------|
| Name | None [23:18] | | | | | | OCD_DPSLP_REG_OK [17:17] | OCD_ACT_LINREG_OK [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|--|
| 0 | BODVDDD_OK | R | RW | 1 | BOD indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip. |
| 1 | BODVDDA_OK | R | RW | 0 | BOD indicates vdda is ok. |
| 2 | BODVCCD_OK | R | RW | 1 | BOD indicates vccd is ok. This will always read 1, because a detected brownout will reset the chip. |
| 8 | OVDVDDD_OK | R | RW | 1 | OVD indicates vddd is ok. This will always read 1, because a detected over-voltage condition will reset the chip. |
| 9 | OVDVDDA_OK | R | RW | 0 | OVD indicates vdda is ok. |
| 10 | OVDVCCD_OK | R | RW | 1 | OVD indicates vccd is ok. This will always read 1, because a detected over-over-voltage condition will reset the chip. |
| 16 | OCD_ACT_LINREG_OK | R | RW | 1 | OCD indicates the current drawn from the linear Active Regulator is ok. This will always read 1, because a detected over-current condition will reset the chip. |
| 17 | OCD_DPSLP_REG_OK | R | RW | 1 | OCD indicates the current drawn from the linear DeepSleep Regulator is ok. This will always read 1, because a detected over-current condition will reset the chip. |

26.8.17 PWR_LVD_CTL

Description: High Voltage / Low Voltage Detector (HVLVD) Configuration Register
Address: 0x40261020
Offset: 0x1020
Retention: Retained
IsDeepSleep: Yes
Comment: Trim and configuration bits for Voltage Monitoring System.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---------------------|---|---|----------------------|---|---|---|
| Name | HVLVD1_EN [7:7] | HVLVD1_SRCSEL [6:4] | | | HVLVD1_TRIPSEL [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------------|----------------------------|--------------|--------------------------|----|----|---|---|
| Name | HVLVD1_EN_HT [15:15] | HVLVD1_DPSLP_EN_HT [14:14] | None [13:13] | HVLVD1_TRIPSEL_HT [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|-----------------------|-------------------------|----|
| Name | None [23:19] | | | | | HVLVD1_ACTION [18:18] | HVLVD1_EDGE_SEL [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:3 | HVLVD1_TRIPSEL | RW | R | 0 | Threshold selection for HVLVD1. Disable the detector (HVLVD1_EN=0) before changing the threshold. 0: rise=1.225V (nom), fall=1.2V (nom) 1: rise=1.425V (nom), fall=1.4V (nom) 2: rise=1.625V (nom), fall=1.6V (nom) 3: rise=1.825V (nom), fall=1.8V (nom) 4: rise=2.025V (nom), fall=2V (nom) 5: rise=2.125V (nom), fall=2.1V (nom) 6: rise=2.225V (nom), fall=2.2V (nom) 7: rise=2.325V (nom), fall=2.3V (nom) 8: rise=2.425V (nom), fall=2.4V (nom) 9: rise=2.525V (nom), fall=2.5V (nom) 10: rise=2.625V (nom), fall=2.6V (nom) 11: rise=2.725V (nom), fall=2.7V (nom) 12: rise=2.825V (nom), fall=2.8V (nom) 13: rise=2.925V (nom), fall=2.9V (nom) 14: rise=3.025V (nom), fall=3.0V (nom) 15: rise=3.125V (nom), fall=3.1V (nom) |
| 4:6 | HVLVD1_SRCSEL | RW | R | 0 | Source selection for HVLVD1 |
| | VDDD | | | 0 | Select VDDD |
| | AMUXBUSA | | | 1 | Select AMUXBUSA (VDDD branch) |
| | RESERVED | | | 2 | N/A |
| | VDDIO | | | 3 | N/A |
| | AMUXBUSB | | | 4 | Select AMUXBUSB (VDDD branch) |
| 7 | HVLVD1_EN | RW | R | 0 | Enable HVLVD1 voltage monitor. HVLVD1 does not function during DEEPSLEEP, but it automatically returns to its configured setting after DEEPSLEEP wakeup. Do not change other HVLVD1 settings when enabled. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------------|----|----|-----------------|---|
| 8:12 | HVLVD1_TRIPSEL_HT | RW | R | 0 | Threshold selection for HVLVD1 for HT products. Detector accuracy is +/-4 percent of the nominal values listed below. Disable the detector (HVLVD1_EN=0) before changing the threshold. 0: rise 2.825V (nom), fall=2.8V (nom) 1: rise 2.925V (nom), fall=2.9V (nom) 2: rise 3.025V (nom), fall=3.0V (nom) 3: rise 3.125V (nom), fall=3.1V (nom) 4: rise 3.225V (nom), fall=3.2V (nom) 5: rise 3.325V (nom), fall=3.3V (nom) 6: rise 3.425V (nom), fall=3.4V (nom) 7: rise 3.525V (nom), fall=3.5V (nom) 8: rise 3.625V (nom), fall=3.6V (nom) 9: rise 3.725V (nom), fall=3.7V (nom) 10: rise 3.825V (nom), fall=3.8V (nom) 11: rise 3.925V (nom), fall=3.9V (nom) 12: rise 4.025V (nom), fall=4.0V (nom) 13: rise 4.125V (nom), fall=4.1V (nom) 14: rise 4.225V (nom), fall=4.2V (nom) 15: rise 4.325V (nom), fall=4.3V (nom) 16: rise 4.425V (nom), fall=4.4V (nom) 17: rise 4.525V (nom), fall=4.5V (nom) 18: rise 4.625V (nom), fall=4.6V (nom) 19: rise 4.725V (nom), fall=4.7V (nom) 20: rise 4.825V (nom), fall=4.8V (nom) 21: rise 4.925V (nom), fall=4.9V (nom) 22: rise 5.025V (nom), fall=5.0V (nom) 23: rise 5.125V (nom), fall=5.1V (nom) 24: rise 5.225V (nom), fall=5.2V (nom) 25: rise 5.325V (nom), fall=5.3V (nom) others: reserved |
| 14 | HVLVD1_DPSLP_EN_HT | RW | R | 0 | Keep HVLVD1 voltage monitor enabled during DEEPSLEEP mode. This field is only used when HVLVD1_EN_HT==1. |
| 15 | HVLVD1_EN_HT | RW | R | 0 | Enable HVLVD1 voltage monitor. This detector monitors vddd only. Do not change other HVLVD1 settings when enabled. |
| 16:17 | HVLVD1_EDGE_SEL | RW | R | 0 | Sets which edge(s) will trigger an action when the threshold is crossed. |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 18 | HVLVD1_ACTION | RW | R | 0 | Action taken when the threshold is crossed in the programmed direction(s) |
| | INTERRUPT | | | 0 | Generate an interrupt |
| | FAULT | | | 1 | Generate a fault |

26.8.18 PWR_LVD_CTL2

Description: High Voltage / Low Voltage Detector (HVLVD) Configuration Register #2
Address: 0x40261024
Offset: 0x1024
Retention: Retained
IsDeepSleep: Yes
Comment: Trim and configuration bits for Voltage Monitoring System.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------------|----------------------------|--------------|--------------------------|----|----|---|---|
| Name | HVLVD2_EN_HT [15:15] | HVLVD2_DPSLP_EN_HT [14:14] | None [13:13] | HVLVD2_TRIPSEL_HT [12:8] | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|-----------------------|-------------------------|----|
| Name | None [23:19] | | | | | HVLVD2_ACTION [18:18] | HVLVD2_EDGE_SEL [17:16] | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|----|----|-----------------|--|
| 8:12 | HVLVD2_TRIPSEL_HT | RW | R | 0 | <p>Threshold selection for HVLVD2 for HT products. Detector accuracy is +/-4 percent of the nominal values listed below. Disable the detector (HVLVD1_EN=0) before changing the threshold.</p> <p>0: rise 2.825V (nom), fall=2.8V (nom) 1: rise 2.925V (nom), fall=2.9V (nom) 2: rise 3.025V (nom), fall=3.0V (nom) 3: rise 3.125V (nom), fall=3.1V (nom) 4: rise 3.225V (nom), fall=3.2V (nom) 5: rise 3.325V (nom), fall=3.3V (nom) 6: rise 3.425V (nom), fall=3.4V (nom) 7: rise 3.525V (nom), fall=3.5V (nom) 8: rise 3.625V (nom), fall=3.6V (nom) 9: rise 3.725V (nom), fall=3.7V (nom) 10: rise 3.825V (nom), fall=3.8V (nom) 11: rise 3.925V (nom), fall=3.9V (nom) 12: rise 4.025V (nom), fall=4.0V (nom) 13: rise 4.125V (nom), fall=4.1V (nom) 14: rise 4.225V (nom), fall=4.2V (nom) 15: rise 4.325V (nom), fall=4.3V (nom) 16: rise 4.425V (nom), fall=4.4V (nom) 17: rise 4.525V (nom), fall=4.5V (nom) 18: rise 4.625V (nom), fall=4.6V (nom) 19: rise 4.725V (nom), fall=4.7V (nom) 20: rise 4.825V (nom), fall=4.8V (nom) 21: rise 4.925V (nom), fall=4.9V (nom) 22: rise 5.025V (nom), fall=5.0V (nom) 23: rise 5.125V (nom), fall=5.1V (nom) 24: rise 5.225V (nom), fall=5.2V (nom) 25: rise 5.325V (nom), fall=5.3V (nom) others: reserved</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------------|----|----|-----------------|--|
| 14 | HVLVD2_DPSLP_EN_HT | RW | R | 0 | Keep HVLVD2 voltage monitor enabled during DEEPSLEEP mode. This field is only used when HVLVD1_EN_HT==1. |
| 15 | HVLVD2_EN_HT | RW | R | 0 | Enable HVLVD2 voltage monitor. This detector monitors vddd only. Do not change other HVLVD2 settings when enabled. |
| 16:17 | HVLVD2_EDGE_SEL | RW | R | 0 | Sets which edge(s) will trigger an action when the threshold is crossed. |
| | DISABLE | | | 0 | Disabled |
| | RISING | | | 1 | Rising edge |
| | FALLING | | | 2 | Falling edge |
| | BOTH | | | 3 | Both rising and falling edges |
| 18 | HVLVD2_ACTION | RW | R | 0 | Action taken when the threshold is crossed in the programmed directions(s) |
| | INTERRUPT | | | 0 | Generate an interrupt |
| | FAULT | | | 1 | Generate a fault |

26.8.19 PWR_HIB_DATA

Description: HIBERNATE Data Register
Address: 0x40261040
Offset: 0x1040
Retention: Retained
IsDeepSleep: No
Comment: This register can retain information during HIBERNATE mode.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|----|----|----|----|----|----|----|
| Name | HIB_DATA [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | HIB_DATA [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | HIB_DATA [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | HIB_DATA [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:31 | HIB_DATA | RW | A | 0 | Additional data that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware for any application-specific purpose. Note that waking up from HIBERNATE using XRES will reset this register. |

26.8.20 CLK_PATH_SELECT

Description: Clock Path Select Register

Address: 0x40261200

Offset: 0x1200

Retention: Retained

IsDeepSleep: Yes

Comment: Selects a source for clock path. The output of this mux can be used as the root of a clock tree. If there is a PLL on the path, this mux output is the PLL reference clock. The related PLL register contains a mux to select whether the clock path uses the PLL output or is bypassed to the PLL reference clock.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------|---|---|
| Name | None [7:3] | | | | | PATH_MUX [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:2 | PATH_MUX | RW | R | 0 | Selects a source for clock PATH<i>. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | IMO | | | 0 | IMO - Internal R/C Oscillator |
| | EXTCLK | | | 1 | EXTCLK - External Clock Pin |
| | ECO | | | 2 | ECO - External-Crystal Oscillator |
| | ALTHF | | | 3 | ALTHF - Alternate High-Frequency clock input (product-specific clock) |
| | DSI_MUX | | | 4 | DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior. |
| | LPECO | | | 5 | LPECO - Low-Power External-Crystal Oscillator |

26.8.21 CLK_ROOT_SELECT

Description: Clock Root Select Register
Address: 0x40261240
Offset: 0x1240
Retention: Retained
IsDeepSleep: Yes
Comment: Selects a root for a HF clock tree and DSI input. There is a copy of this register for each clock root.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------|----------------|----|----------------|----|----|------------------|
| Name | None [7:6] | | ROOT_DIV [5:4] | | ROOT_MUX [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:9] | | | | | | | DIRECT_MUX [8:8] |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:3 | ROOT_MUX | RW | R | 0 | Selects a clock path as the root of HFCLK<k> and for SRSS DSI input <k>. Use CLK_PATH_SELECT[i] to configure the desired path. Some paths may have FLL or PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure the FLL using CLK_FLL_CONFIG register. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | PATH0 | | | 0 | Select PATH0 (can be configured for FLL) |
| | PATH1 | | | 1 | Select PATH1 (can be configured for PLL0, if available in the product) |
| | PATH2 | | | 2 | Select PATH2 (can be configured for PLL1, if available in the product) |
| | PATH3 | | | 3 | Select PATH3 (can be configured for PLL2, if available in the product) |
| | PATH4 | | | 4 | Select PATH4 (can be configured for PLL3, if available in the product) |
| | PATH5 | | | 5 | Select PATH5 (can be configured for PLL4, if available in the product) |
| | PATH6 | | | 6 | Select PATH6 (can be configured for PLL5, if available in the product) |
| | PATH7 | | | 7 | Select PATH7 (can be configured for PLL6, if available in the product) |
| | PATH8 | | | 8 | Select PATH8 (can be configured for PLL7, if available in the product) |
| | PATH9 | | | 9 | Select PATH9 (can be configured for PLL8, if available in the product) |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|--|--|
| | PATH10 | | | 10 | Select PATH10 (can be configured for PLL9, if available in the product) |
| | PATH11 | | | 11 | Select PATH11 (can be configured for PLL10, if available in the product) |
| | PATH12 | | | 12 | Select PATH12 (can be configured for PLL11, if available in the product) |
| | PATH13 | | | 13 | Select PATH13 (can be configured for PLL12, if available in the product) |
| | PATH14 | | | 14 | Select PATH14 (can be configured for PLL13, if available in the product) |
| | PATH15 | | | 15 | Select PATH15 (can be configured for PLL14, if available in the product) |
| 4:5 | ROOT_DIV | RW | R | 0 | Selects predivider value for this clock root and DSI input. This divider is after DIRECT_MUX. For products with DSI, the output of this mux is routed to DSI for use as a signal. For products with clock supervision, the output of this mux is the monitored clock for CSV_HF<k>. |
| | NO_DIV | | | 0 | Transparent mode, feed through selected clock source w/o dividing. |
| | DIV_BY_2 | | | 1 | Divide selected clock source by 2 |
| | DIV_BY_4 | | | 2 | Divide selected clock source by 4 |
| | DIV_BY_8 | | | 3 | Divide selected clock source by 8 |
| 8 | DIRECT_MUX | RW | A | (1 << internals.reg_index & MASK_DIRECT_MUX_DEF) >> internal.s.reg_index | Direct selection mux that allows IMO to bypass most of the clock mux structure. For products with multiple regulators, this mux can be used to reduce current without requiring significant reconfiguration of the clocking network. The default value of HFCLK<0>==ROOT_MUX, and the default value for other clock trees is product-specific. |
| | IMO | | | 0 | Select IMO |
| | ROOT_MUX | | | 1 | Select ROOT_MUX selection |
| 31 | ENABLE | RW | A | 0 | Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. |

26.8.22 CLK_SELECT

Description: Clock selection register
Address: 0x40261500
Offset: 0x1500
Retention: Retained
IsDeepSleep: Yes
Comment: Clock source selection register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|---|---|
| Name | None [7:3] | | | | | LFCLK_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|------------------|----|----|-----------------|----|---|---|
| Name | PUMP_ENABLE [15:15] | PUMP_DIV [14:12] | | | PUMP_SEL [11:8] | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 0:2 | LFCLK_SEL | RW | A | 0 | Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | ILO0 | | | 0 | ILO0 - Internal Low-speed Oscillator #0. |
| | WCO | | | 1 | WCO - Watch-Crystal Oscillator. Requires Backup domain to be present and properly configured (including external watch crystal, if used). |
| | ALTLF | | | 2 | ALTLF - Alternate Low-Frequency Clock. Capability is product-specific |
| | PILO | | | 3 | PILO - Precision ILO. If present, it works in DEEPSLEEP and higher modes. Does not work in HIBERNATE mode. |
| | ILO1 | | | 4 | ILO1 - Internal Low-speed Oscillator #1, if present. |
| | ECO_PRESCALER | | | 5 | ECO_PRESCALER - External-Crystal Oscillator after prescaling, if present. Does not work in DEEPSLEEP or HIBERNATE modes. Intended for applications that operate in ACTIVE/SLEEP modes only. This option is only valid when ECO is present in the product. |
| | LPECO_PRESCALER | | | 6 | LPECO_PRESCALER - Low-Power External-Crystal Oscillator after prescaling, if present. This choice works in ACTIVE/SLEEP/DEEPSLEEP modes. This option is only valid when LPECO is present in the product. |
| 8:11 | PUMP_SEL | RW | R | 0 | Reserved. Not used the product. |
| 12:14 | PUMP_DIV | RW | R | 0 | Reserved. Not used in the product. |
| | NO_DIV | | | 0 | N/A |
| | DIV_BY_2 | | | 1 | N/A |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|------------------------------------|
| | DIV_BY_4 | | | 2 | N/A |
| | DIV_BY_8 | | | 3 | N/A |
| | DIV_BY_16 | | | 4 | N/A |
| 15 | PUMP_ENABLE | RW | R | 0 | Reserved. Not used in the product. |

26.8.23 CLK_TIMER_CTL

Description: Timer Clock Control Register
Address: 0x40261504
Offset: 0x1504
Retention: Retained
IsDeepSleep: Yes
Comment: Timer clock source selection register.
Default: 0x80070000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-----------------|
| Name | None [7:1] | | | | | | | TIMER_SEL [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---------------------|---|
| Name | None [15:10] | | | | | | TIMER_HF0_DIV [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | TIMER_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|---|
| 0 | TIMER_SEL | RW | R | 0 | Obsolete. Do not use in new designs. Keep default value in new designs. |
| | IMO | | | 0 | Obsolete. Do not use in new designs. Keep default value in new designs. |
| | HF0_DIV | | | 1 | Obsolete. Do not use in new designs. |
| 8:9 | TIMER_HF0_DIV | RW | R | 0 | Obsolete. Do not use in new designs. Keep default value in new designs. |
| | NO_DIV | | | 0 | Obsolete. Do not use in new designs. Keep default value in new designs. |
| | DIV_BY_2 | | | 1 | Obsolete. Do not use in new designs. |
| | DIV_BY_4 | | | 2 | Obsolete. Do not use in new designs. |
| | DIV_BY_8 | | | 3 | Obsolete. Do not use in new designs. |
| 16:23 | TIMER_DIV | RW | R | 7 | Obsolete. Do not use in new designs. Keep default value in new designs. |
| 31 | ENABLE | RW | R | 1 | Obsolete. Do not use in new designs. Keep default value in new designs. |

26.8.24 CLK_ILO0_CONFIG

Description: ILO0 Configuration

Address: 0x40261508

Offset: 0x1508

Retention: Retained

IsDeepSleep: No

Comment: Configuration register for ILO0. ILO0 configuration and trims are reset by XRES, HIBERNATE, and power-related resets, unless otherwise noted.

Default: 0x80000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|--------------------|
| Name | None [7:1] | | | | | | | ILO0_BACK UP [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|-------------------------|--------------|----|----|----|----|----|
| Name | ENABLE [31:31] | ILO0_MON_ENABLE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|---|
| 0 | ILO0_BACKUP | RW | A | 0 | This register indicates that ILO0 should stay enabled during XRES and HIBERNATE modes. If backup voltage domain is implemented on the product, this bit also indicates if ILO0 should stay enabled through power-related resets on other supplies, e.g.. BOD on VDDD/VCCD. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. This register is reset when the backup logic resets. 0: ILO0 turns off during XRES, HIBERNATE, and power-related resets. ILO0 configuration and trims are reset by these events. 1: ILO0 stays enabled, as described above. ILO0 configuration and trims are not reset by these events. |
| 30 | ILO0_MON_ENABLE | RW | A | 0 | Reserved. Always write a zero. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. |
| 31 | ENABLE | RW | A | 1 | Master enable for ILO. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. HT-variant: This register will not clear unless PWR_CTL2.BGREF_LPMODE==0. After enabling, the first ILO0 cycle occurs within 12us and is +/-10 percent accuracy. Thereafter, ILO0 is +/-5 percent accurate. |

26.8.25 CLK_ILO1_CONFIG

Description: ILO1 Configuration
Address: 0x4026150C
Offset: 0x150C
Retention: Retained
IsDeepSleep: Yes
Comment: Configuration register for ILO1.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|--------------------------------|--------------|----|----|----|----|----|
| Name | ENABLE [31:31] | ILO1_MON _ENABLE [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| 30 | ILO1_MON_ENABLE | RW | R | 0 | Reserved. Always write a zero. |
| 31 | ENABLE | RW | R | 0 | Master enable for ILO1. HT-variant: After enabling, the first ILO1 cycle occurs within 12us and is +/-10 percent accuracy. Thereafter, ILO1 is +/-5 percent accurate. |

26.8.26 CLK_IMO_CONFIG

Description: IMO Configuration

Address: 0x40261518

Offset: 0x1518

Retention: Retained

IsDeepSleep: Yes

Comment: Internal high speed R/C oscillator configuration register. Note that this oscillator comes up active on power up. The oscillator provides the primary system clock (HFCLK) on power up until firmware configures differently. This oscillator is also used before system start to count out power up delays. This is done in fast IMO (FIMO) mode that does not require any external references and runs at a fixed 12MHz.

Default: 0x80000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---|
| Name | None [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 31 | ENABLE | RW | R | 1 | Master enable for IMO oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the IMO during DEEPSLEEP, HIBERNATE, and XRES. |

26.8.27 CLK_ECO_CONFIG

Description: ECO Configuration Register
Address: 0x4026151C
Offset: 0x151C
Retention: Retained
IsDeepSleep: Yes
Comment: Internal high speed oscillator configuration register for External-Crystal.
Default: 0x2

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------|------------|
| Name | None [7:2] | | | | | | AGC_EN [1:1] | None [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|------------------------|-------------------------|--------------|----|
| Name | ECO_EN [31:31] | None [30:29] | | | ECO_DIV_ENABLE [28:28] | ECO_DIV_DISABLE [27:27] | None [26:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|------|-----------------|---|
| 1 | AGC_EN | RW | R | 1 | Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by CLK_ECO_CONFIG2.ATRIM. When low, the amplitude is not explicitly controlled and can be as high as the vddd supply. WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. |
| 27 | ECO_DIV_DISABLE | RW | RW1C | 0 | ECO prescaler disable command (mutually exclusive with ECO_DIV_ENABLE). SW sets this field to '1' and HW sets this field to '0'. HW sets ECO_DIV_DISABLE field to '0' immediately and HW sets CLK_ECO_PRESCALE.ECO_DIV_EN field to '0' immediately. |
| 28 | ECO_DIV_ENABLE | RW | RW1C | 0 | ECO prescaler enable command (mutually exclusive with ECO_DIV_DISABLE). ECO Prescaler only works in ACTIVE and SLEEP modes. SW sets this field to '1' to enable the divider and HW sets this field to '0' to indicate that divider enabling has completed. When the divider is enabled, its integer and fractional counters are initialized to '0'. If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the ECO_DIV_DISABLE field. 1: Configure CLK_ECO_PRESCALE registers. 2: Enable the divider using the ECO_DIV_ENABLE field. HW sets the ECO_DIV_ENABLE field to '0' when the enabling is performed and HW set CLK_ECO_PRESCALER.ENABLED to '1' when the enabling is performed. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 31 | ECO_EN | RW | R | 0 | Master enable for ECO oscillator. Configure the settings in CLK_ECO_CONFIG2 to work with the selected crystal, before enabling ECO. |

26.8.28 CLK_ECO_PRESCALE

Description: ECO Prescaler Configuration Register
Address: 0x40261520
Offset: 0x1520
Retention: Retained
IsDeepSleep: Yes
Comment: Fractional prescaler value to bring down the ECO frequency to 32768 Hz if used as LFCLK.
Do not change divider settings while ECO prescaler is enabled or enabling.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-----------------------|
| Name | None [7:1] | | | | | | | ECO_DIV_ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | ECO_FRAC_DIV [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | ECO_INT_DIV [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|---------------------|----|
| Name | None [31:26] | | | | | | ECO_INT_DIV [25:24] | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-----------------|----|----|-----------------|---|
| 0 | ECO_DIV_ENABLED | R | RW | 0 | ECO prescaler enabled. HW sets this field to '1' as a result of an CLK_ECO_CONFIG.ECO_DIV_ENABLE command. HW sets this field to '0' as a result on a CLK_ECO_CONFIG.ECO_DIV_DISABLE command. |
| 8:15 | ECO_FRAC_DIV | RW | R | 0 | 8-bit fractional value, sufficient to get prescaler output within the +/-65ppm calibration range. Do not change this setting when ECO Prescaler is enabled. |
| 16:25 | ECO_INT_DIV | RW | R | 0 | 10-bit integer value allows for ECO frequencies up to 33.55MHz. Subtract one from the desired divide value when writing this field. For example, to divide by 1, write ECO_INT_DIV=0. Do not change this setting when ECO Prescaler is enabled. |

26.8.29 CLK_ECO_STATUS

Description: ECO Status Register
Address: 0x40261524
Offset: 0x1524
Retention: Retained
IsDeepSleep: Yes
Comment: Status indications for external crystal oscillator (ECO).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|-----------------|--------------|
| Name | None [7:2] | | | | | | ECO_READY [1:1] | ECO_OK [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0 | ECO_OK | R | W | 0 | Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. |
| 1 | ECO_READY | R | W | 0 | Indicates the ECO internal oscillator circuit has had enough time to fully stabilize. This is the output of a counter since ECO was enabled, and it does not check the ECO output. It is recommended to also confirm ECO_OK==1. |

26.8.30 CLK_FLL_CONFIG

Description: FLL Configuration Register

Address: 0x40261530

Offset: 0x1530

Retention: Retained

IsDeepSleep: Yes

Comment: This register contains frequency lock loop (FLL) configuration. FLL circuit settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic. Deselect the FLL using .BYPASS_SEL=FLL_REF

Default: 0x1000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|--------------|----|----|----|----|------------------|------------------------|
| Name | FLL_MULT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | FLL_MULT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:18] | | | | | | FLL_MULT [17:16] | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | FLL_ENABLE [31:31] | None [30:25] | | | | | | FLL_OUTPUT_DIV [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0:17 | FLL_MULT | RW | R | 0 | Multiplier to determine CCO frequency in multiples of the frequency of the selected reference clock (Fref). $F_{ll} = (FLL_MULT) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV + 1)$ |
| 24 | FLL_OUTPUT_DIV | RW | R | 1 | Control bits for Output divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: no division 1: divide by 2 |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 31 | FLL_ENABLE | RW | R | 0 | <p>Master enable for FLL. The FLL requires firmware sequencing when enabling and disabling. Hardware handles sequencing automatically when entering/exiting DEEPSLEEP.</p> <p>To enable the FLL, use the following sequence:</p> <ol style="list-style-type: none"> 1) Configure FLL and CCO settings. Do not modify CLK_FLL_CONFIG3.BYPASS_SEL (must be AUTO) or CLK_FLL_CONFIG.FLL_ENABLE (must be 0). 2) Enable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=1 3) Wait until CLK_FLL_STATUS.CCO_READY==1. 4) Ensure the reference clock has stabilized. 5) Write FLL_ENABLE=1. 6) Optionally wait until CLK_FLL_STATUS.LOCKED==1. The hardware automatically changes to the FLL output when LOCKED==1. <p>To disable the FLL, use the following sequence:</p> <ol style="list-style-type: none"> 1) Write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF. 2) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional). 3) Wait at least ten cycles of either FLL reference clock or FLL output clock, whichever is slower. It is recommended to use a HW counter (e.g. clock calibration counter, event generator) running on the slower clock. 4) Disable FLL with FLL_ENABLE=0. 5) Disable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=0. 6) Write CLK_FLL_CONFIG3.BYPASS_SEL=AUTO. 7) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional). 8) Wait three cycles of FLL reference clock. It is recommended to use a HW counter (e.g. clock calibration counter, event generator) running on the reference clock. <p>0: Block is powered off 1: Block is powered on</p> |

26.8.31 CLK_FLL_CONFIG2

Description: FLL Configuration Register 2

Address: 0x40261534

Offset: 0x1534

Retention: Retained

IsDeepSleep: Yes

Comment: This register contains frequency lock loop (FLL) configuration. FLL circuit settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic. Deselect the FLL using .BYPASS_SEL=FLL_REF

Default: 0x20001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|--------------------|----|----|----|----|
| Name | FLL_REF_DIV [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | FLL_REF_DIV [12:8] | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | LOCK_TOL [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | UPDATE_TOL [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------|----|----|-----------------|---|
| 0:12 | FLL_REF_DIV | RW | R | 1 | Control bits for reference divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 8191: divide by 8191 |
| 16:23 | LOCK_TOL | RW | R | 2 | Lock tolerance sets the error threshold for when the FLL output is considered locked to the reference input. A high tolerance can be used to lock more quickly or allow less accuracy. The tolerance is the allowed difference between the count value for the ideal formula and the measured value. 0: tolerate error of 1 count value 1: tolerate error of 2 count values ... 255: tolerate error of 256 count values |
| 24:31 | UPDATE_TOL | RW | R | 0 | Update tolerance sets the error threshold for when the FLL will update the CCO frequency settings. The update tolerance is the allowed difference between the count value for the ideal formula and the measured value. UPDATE_TOL should be less than LOCK_TOL. |

26.8.32 CLK_FLL_CONFIG3

Description: FLL Configuration Register 3

Address: 0x40261538

Offset: 0x1538

Retention: Retained

IsDeepSleep: Yes

Comment: This register contains frequency lock loop (FLL) configuration. Do not change settings while the FLL is running, except BYPASS_SEL.

Default: 0x2800

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------------|----|--------------------|----|------------------------|----|----|----|
| Name | FLL_LF_PGAIN [7:4] | | | | FLL_LF_IGAIN [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | SETTLING_COUNT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:21] | | | | SETTLING_COUNT [20:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:30] | | BYPASS_SEL [29:28] | | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:3 | FLL_LF_IGAIN | RW | R | 0 | FLL Loop Filter Gain Setting #1. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal |
| 4:7 | FLL_LF_PGAIN | RW | R | 0 | FLL Loop Filter Gain Setting #2. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|---|
| 8:20 | SETTLING_COUNT | RW | R | 40 | Number of undivided reference clock cycles to wait after changing the CCO trim until the loop measurement restarts. A delay allows the CCO output to settle and gives a more accurate measurement. The default is tuned to an 8MHz reference clock since the IMO is expected to be the most common use case. 0: no settling time 1: wait one reference clock cycle ... 8191: wait 8191 reference clock cycles |
| 28:29 | BYPASS_SEL | RW | R | 0 | Bypass mux located just after FLL output. This register can be written while the FLL is enabled. When changing BYPASS_SEL, do not turn off the reference clock or CCO clock for five cycles (whichever is slower). In case of disabling FLL(FLL_ENABLE=0), additional five cycles are required. Refer to FLL disable sequence for more details in CLK_FLL_CONFIG->FLL_ENABLE. Whenever BYPASS_SEL is changed, it is required to read CLK_FLL_CONFIG3 to ensure the change takes effect. |
| | AUTO | | | 0 | Automatic using lock indicator. When unlocked, automatically selects FLL reference input (bypass mode). When locked, automatically selects FLL output. This can allow some processing to occur while the FLL is locking, such as after DEEPSLEEP wakeup. It is incompatible with clock supervision, because the frequency changes based on the lock signal. |
| | LOCKED_OR_NOTHING | | | 1 | Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. |
| | FLL_REF | | | 2 | Select FLL reference input (bypass mode). Ignores lock indicator |
| | FLL_OUT | | | 3 | Select FLL output. Ignores lock indicator. |

26.8.33 CLK_FLL_CONFIG4

Description: FLL Configuration Register 4

Address: 0x4026153C

Offset: 0x153C

Retention: Retained

IsDeepSleep: Yes

Comment: This register contains frequency lock loop (FLL) configuration. Do not change settings while the FLL is running.

Default: 0xFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---------------------------|--------------|----|----|------------------|----|------------------|
| Name | CCO_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:11] | | | | | CCO_RANGE [10:8] | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CCO_FREQ [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CCO_ENABLE [31:31] | CCO_HW_UPDATE_DIS [30:30] | None [29:25] | | | | | CCO_FREQ [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|--|
| 0:7 | CCO_LIMIT | RW | R | 255 | Maximum CCO offset allowed (used to prevent FLL dynamics from selecting an CCO frequency that the logic cannot support) |
| 8:10 | CCO_RANGE | RW | R | 0 | Frequency range of CCO |
| | RANGE0 | | | 0 | Target frequency is in range [48, 64) MHz |
| | RANGE1 | | | 1 | Target frequency is in range [64, 85) MHz |
| | RANGE2 | | | 2 | Target frequency is in range [85, 113) MHz |
| | RANGE3 | | | 3 | Target frequency is in range [113, 150) MHz |
| | RANGE4 | | | 4 | Target frequency is in range [150, 200] MHz |
| 16:24 | CCO_FREQ | RW | RW | 0 | CCO frequency code. This is updated by HW when the FLL is enabled. It can be manually updated to use the CCO in an open loop configuration. The meaning of each frequency code depends on the range. |
| 30 | CCO_HW_UPDATE_DIS | RW | R | 0 | Disable CCO frequency update by FLL hardware 0: Hardware update of CCO settings is allowed. Use this setting for normal FLL operation. 1: Hardware update of CCO settings is disabled. Use this setting for open-loop FLL operation. |
| 31 | CCO_ENABLE | RW | R | 0 | Enable the CCO. It is required to enable the CCO before using the FLL. 0: Block is powered off 1: Block is powered on |

26.8.34 CLK_FLL_STATUS

Description: FLL Status Register
Address: 0x40261540
Offset: 0x1540
Retention: Retained
IsDeepSleep: No
Comment: This register indicates status for the FLL. This register is synchronized during an AHB read transaction. This causes a number wait-states to be inserted in the transaction depending on the frequency ratio between system and FLL frequency.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|------------------------|--------------|
| Name | None [7:3] | | | | | CCO_READY [2:2] | UNLOCK_OC CURRED [1:1] | LOCKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|------|----|-----------------|---|
| 0 | LOCKED | R | W | 0 | FLL Lock Indicator |
| 1 | UNLOCK_OCCURRED | RW1C | A | 0 | This bit sets whenever the FLL is enabled and goes out of lock. This bit stays set until cleared by firmware. |
| 2 | CCO_READY | R | RW | 0 | This indicates that the CCO is internally settled and ready to use. |

26.8.35 CLK_ECO_CONFIG2

Description: ECO Configuration Register 2
Address: 0x40261544
Offset: 0x1544
Retention: Retained
IsDeepSleep: Yes
Comment: Internal high speed oscillator configuration register for External-Crystal.
Default: 0x3

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|------------|--------------|---|---|
| Name | ATRIM [7:4] | | | | None [3:3] | WDTRIM [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|---------------|----|----|---------------|----|-------------|---|
| Name | None [15:15] | GTRIM [14:12] | | | RTRIM [11:10] | | FTRIM [9:8] | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:2 | WDTRIM | RW | R | 3 | Watch Dog Trim. Sets the minimum oscillation amplitude (Vp) for the crystal drive level. The minimum amplitude detector output is readable in CLK_ECO_STATUS.ECO_OK. 0x0: Vp > 0.05V 0x1: Vp > 0.10V 0x2: Vp > 0.15V 0x3: Vp > 0.20V 0x4: Vp > 0.25V 0x5: Vp > 0.30V 0x6: Vp > 0.35V 0x7: Vp > 0.40V |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--|
| 4:7 | ATRIM | RW | R | 0 | Amplitude trim. Sets maximum oscillation amplitude (Vp) to set the crystal drive level when ECO_CONFIG.AGC_EN=1. When AGC_EN=0, most values of this register are unused, except as noted. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0: Vp < 0.35V 0x1: Vp < 0.40V 0x2: Vp < 0.45V 0x3: Vp < 0.50V 0x4: Vp < 0.55V 0x5: Vp < 0.60V 0x6: Vp < 0.65V 0x7: Vp < 0.70V 0x8: Vp < 0.75V 0x9: Vp < 0.80V 0xA: Vp < 0.85V 0xB: Vp < 0.90V 0xC: Vp < 0.95V 0xD: Vp < 1.00V 0xE: Vp < 1.05V 0xF: Vp < 1.10V when AGC_EN=1. When AGC_EN=0, this setting enables maximum swing between vddd and vssd. |
| 8:9 | FTRIM | RW | R | 0 | Filter Trim - 3rd harmonic oscillation |
| 10:11 | RTRIM | RW | R | 0 | Feedback resistor Trim |
| 12:14 | GTRIM | RW | R | 0 | Gain Trim - Startup time. |

26.8.36 CLK_PLL_CONFIG

Description: PLL Configuration Register

Address: 0x40261600

Offset: 0x1600

Retention: Retained

IsDeepSleep: Yes

Comment: This register contains PLL configuration. There is a copy of this register for each PLL. PLL circuit settings should not be changed while it is a selected clock (connected to logic). This prevents clock glitches that can crash the logic.

Default: 0x20116

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------------|--------------------|----------------------|---------------------|--------------------|----|--------------|
| Name | None [7:7] | FEEDBACK_DIV [6:0] | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:13] | | | REFERENCE_DIV [12:8] | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:21] | | | OUTPUT_DIV [20:16] | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLE [31:31] | None [30:30] | BYPASS_SEL [29:28] | | PLL_LF_MODE [27:27] | LOCK_DELAY [26:25] | | None [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|---|
| 0:6 | FEEDBACK_DIV | RW | R | 22 | Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0-21: illegal (undefined behavior) 22: divide by 22 ... 112: divide by 112 >112: illegal (undefined behavior) |
| 8:12 | REFERENCE_DIV | RW | R | 1 | Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 20: divide by 20 others: illegal (undefined behavior) |
| 16:20 | OUTPUT_DIV | RW | R | 2 | Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: illegal (undefined behavior) 2: divide by 2. Suitable for direct usage as HFCLK source. ... 16: divide by 16. Suitable for direct usage as HFCLK source. >16: illegal (undefined behavior) |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|--|
| 25:26 | LOCK_DELAY | RW | R | 0 | Configures the sensitivity of the lock detection logic. 0: normal operation 1: reduced sensitivity to allow tracking a modulating reference clock. When this option is selected, configure fVCO=320MHz. The PLL can track the a reference clock frequency that modulates within +/-4 percent at a rate of fREF/1000 MHz. 2,3: reserved (do not use) |
| 27 | PLL_LF_MODE | RW | R | 0 | VCO frequency range selection. Configure this bit according to the targeted VCO frequency. Do not change this setting while the PLL is enabled. 0: VCO frequency is [200MHz, 400MHz] 1: VCO frequency is [170MHz, 200MHz] |
| 28:29 | BYPASS_SEL | RW | R | 0 | Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). |
| | AUTO | | | 0 | Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input. |
| | LOCKED_OR_NOTHING | | | 1 | Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output. |
| | PLL_REF | | | 2 | Select PLL reference input (bypass mode). Ignores lock indicator |
| | PLL_OUT | | | 3 | Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output. |
| 31 | ENABLE | RW | R | 0 | Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1. $F_{pll} = (FEEDBACK_DIV) * (F_{ref} / REFERENCE_DIV) / (OUTPUT_DIV)$ 0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit. 1: Block is enabled |

26.8.37 CLK_PLL_STATUS

Description: PLL Status Register

Address: 0x40261640

Offset: 0x1640

Retention: Retained

IsDeepSleep: No

Comment: This register indicates status for the PLL. There is a copy of this register for each PLL. This register is synchronized during an AHB read transaction. This causes a number wait-states to be inserted in the transaction depending on the frequency ration between system and PLL frequency.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|------------------------------|-----------------|
| Name | None [7:2] | | | | | | UNLOCK_OC CURRED [1:1] | LOCKED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|------|----|-----------------|--|
| 0 | LOCKED | R | W | 0 | PLL Lock Indicator |
| 1 | UNLOCK_OCCURRED | RW1C | A | 0 | This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. |

26.8.38 CSV_REF_SEL

Description: Select CSV Reference clock for Active domain
Address: 0x40261700
Offset: 0x1700
Retention: Retained
IsDeepSleep: Yes
Comment: Selects a source to be used as the Reference clock for CSV in the Active domain. (matching CLK_PATH_SELECT.PATH_MUX)
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|---------------|----|----|
| Name | None [7:3] | | | | | REF_MUX [2:0] | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:2 | REF_MUX | RW | R | 0 | Selects a source for clock clk_ref_hf. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. |
| | IMO | | | 0 | IMO - Internal R/C Oscillator |
| | EXTCLK | | | 1 | EXTCLK - External Clock Pin |
| | ECO | | | 2 | ECO - External-Crystal Oscillator |
| | ALTHF | | | 3 | ALTHF - Alternate High-Frequency clock input (product-specific clock) |

26.8.39 RES_CAUSE

Description: Reset Cause Observation Register

Address: 0x40261800

Offset: 0x1800

Retention: Retained

IsDeepSleep: Yes

Comment: Indicates the cause for reset(s) that occurred in the system. All bits in this register assert when the corresponding reset cause occurs and must be cleared by firmware. Low-voltage cause bits are reset whenever the low-voltage supply is initialized, including XRES, POR, brown-out, and during Hibernate wakeup. HT products also clear low-voltage cause bits for over-voltage, over-current, and WDT resets. Refer to the reset source documentation to understand what reset source behavior for different configuration or modes.

Default: 0x40000000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|--------------------|--------------------|------------------|-------------------------|-------------------------|-----------------------|-----------------|
| Name | RESET_MCWDT2 [7:7] | RESET_MCWDT1 [6:6] | RESET_MCWDT0 [5:5] | RESET_SOFT [4:4] | RESET_TC_DBGRESET [3:3] | RESET_DPSLP_FAULT [2:2] | RESET_ACT_FAULT [1:1] | RESET_WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|--------------------|
| Name | None [15:9] | | | | | | | RESET_MCWDT3 [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|--------------------|
| Name | RESET_OCD_ACT_LINREG [23:23] | RESET_OVD_VCCD [22:22] | RESET_OVD_VDDA [21:21] | RESET_OVD_VDDD [20:20] | RESET_BOD_VCCD [19:19] | RESET_BOD_VDDA [18:18] | RESET_BOD_VDDD [17:17] | RESET_XRES [16:16] |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|------------------------|---------------------------|---------------------|--------------|--------------------|-------------------------|--------------------------------|
| Name | None [31:31] | RESET_POR_VDDD [30:30] | RESET_STRUCT_XRES [29:29] | RESET_PXRES [28:28] | None [27:27] | RESET_PMIC [26:26] | RESET_OCD_REGHC [25:25] | RESET_OCD_DPSLP_LINREG [24:24] |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|----|-----------------|---|
| 0 | RESET_WDT | RW1C | A | 0 | A basic WatchDog Timer (WDT) reset has occurred since last power cycle. ULP products: This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). For products that support high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 1 | RESET_ACT_FAULT | RW1C | A | 0 | Fault logging system requested a reset from its Active logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 2 | RESET_DPSLP_FAULT | RW1C | A | 0 | Fault logging system requested a reset from its DeepSleep logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------------|------|----|-----------------|--|
| 3 | RESET_TC_DBGRESET | RW1C | A | 0 | Test controller or debugger asserted reset. Only resets debug domain. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 4 | RESET_SOFT | RW1C | A | 0 | A CPU requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 5 | RESET_MCWDT0 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #0. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 6 | RESET_MCWDT1 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #1. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 7 | RESET_MCWDT2 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #2. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 8 | RESET_MCWDT3 | RW1C | A | 0 | Multi-Counter Watchdog timer reset #3. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). |
| 16 | RESET_XRES | RW1C | A | 0 | External XRES pin was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 17 | RESET_BODVDDD | RW1C | A | 0 | External VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 18 | RESET_BODVDDA | RW1C | A | 0 | External VDDA supply crossed the brown-out limit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 19 | RESET_BODVCCD | RW1C | A | 0 | Internal VCCD core supply crossed the brown-out limit. Note that this detector will detect gross issues with the internal core supply, but may not catch all brown-out conditions. Functional and timing supervision (CSV, WDT) is provided to create fully failsafe internal crash detection. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 20 | RESET_OVDVDDD | RW1C | A | 0 | Overvoltage detection on the external VDDD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 21 | RESET_OVDVDDA | RW1C | A | 0 | Overvoltage detection on the external VDDA supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------------|------|----|-----------------|---|
| 22 | RESET_OVDVCCD | RW1C | A | 0 | Overvoltage detection on the internal core VCCD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 23 | RESET_OCD_ACT_LINREG | RW1C | A | 0 | Overcurrent detection on the internal VCCD supply when supplied by the ACTIVE power mode linear regulator. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 24 | RESET_OCD_DPSLP_LINREG | RW1C | A | 0 | Overcurrent detection on the internal VCCD supply when supplied by the DEEPSLEEP power mode linear regulator. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 25 | RESET_OCD_REGHC | RW1C | A | 0 | Overcurrent detection from REGHC (if present). If REGHC is not present, hardware will never set this bit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 26 | RESET_PMIC | RW1C | A | 0 | PMIC status triggered a reset. If PMIC control is not present, hardware will never set this bit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. |
| 28 | RESET_PXRES | RW1C | A | 0 | PXRES triggered. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 29 | RESET_STRUCT_XRES | RW1C | A | 0 | Structural reset was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. |
| 30 | RESET_PORVDDD | RW1C | A | 1 | Indicator that a POR occurred. This is a high-voltage cause bit, and hardware clears the other bits when this one is set. It does not block further recording of other high-voltage causes. |

26.8.40 RES_CAUSE2

Description: Reset Cause Observation Register 2
Address: 0x40261804
Offset: 0x1804
Retention: Retained
IsDeepSleep: Yes
Comment: Indicates the cause for the latest reset(s) that occurred in the system. Note that resets due to power up and brown-outs below state retention voltages in regulated and unregulated domains cannot be distinguished from each other. All bits in this register assert when the corresponding reset cause occurs and must be cleared by firmware. These bits are cleared by hardware only during XRES, POR or after a detected brown-out.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----|-----------------------|
| Name | RESET_CSV_HF [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | RESET_CSV_HF [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:17] | | | | | | | RESET_CSV_REF [16:16] |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|------|----|-----------------|---|
| 0:15 | RESET_CSV_HF | RW1C | A | 0 | Clock supervision logic requested a reset due to loss or frequency violation of a high-frequency clock. Each bit index K corresponds to a HFCLK<K>. Unimplemented clock bits return zero. |
| 16 | RESET_CSV_REF | RW1C | A | 0 | Clock supervision logic requested a reset due to loss or frequency violation of the reference clock source that is used to monitor the other HF clock sources. |

26.8.41 TST_XRES_SECURE

Description: SECURE TEST and FIRMWARE TEST Key control register
Address: 0x40262054
Offset: 0x2054
Retention: Retained
IsDeepSleep: Yes
Comment: When initialized with the correct 'magic' value, this register enables test modes that are otherwise blocked in devices in NORMAL, SECURE life cycle stages and variants thereof. Enabling the SECURE TEST key will automatically block access to secure portions of EFUSE and/or FLASH.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------------|-----------------------|-------------------|--------------|-------------------|----|----|----|
| Name | DATA8 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | FW_WR [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:20] | | | | SECURE_WR [19:16] | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | SECURE_DISABLE [31:31] | SECURE_KEY_OK [30:30] | FW_KEY_OK [29:29] | None [28:24] | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------------|------|----|-----------------|---|
| 0:7 | DATA8 | RW | R | 0 | Data byte to be set into either SECURE TEST or FIRMWARE TEST key. Must not be changed in the same write that is toggling any of the *_WR bits below, |
| 8:11 | FW_WR | RW | R | 0 | Latch enables for each of the 4 bytes in the 32-bit FIRMWARE TEST key. Must be toggled high and then low while keeping DATA8 to the correct value. |
| 16:19 | SECURE_WR | RW | R | 0 | Latch enables for each of the 4 bytes in the 32-bit SECURE TEST key. Must be toggled high and then low while keeping DATA8 to the correct value. |
| 29 | FW_KEY_OK | R | RW | 0 | Indicates that the 32-bit FIRMWARE TEST key is observing the correct key. Firmware key is reset by (A)XRES and STRUCT_XRES. |
| 30 | SECURE_KEY_OK | R | RW | 0 | Indicates that the 32-bit SECURE TEST key is observing the correct key. Secure key is not reset, but it will establish low after a deep power cycle that causes it to lose its written state. |
| 31 | SECURE_DISABLE | RW1S | R | 0 | Disables the SECURE TEST key entry capability until next reset. Must not be set in the same write when any of the above *_WR bits are set or toggling. |

26.8.42 RES_PXRES_CTL

Description: Programmable XRES Control Register
Address: 0x4026207C
Offset: 0x207C
Retention: Retained
IsDeepSleep: No
Comment: Control register for programmable external reset (PXRES). PXRES gives a way for software to trigger a full-scope reset that is equivalent to XRES, except for RES_CAUSE registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------------|
| Name | None [7:1] | | | | | | | PXRES_TRIGGER [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|-----|----|-----------------|--|
| 0 | PXRES_TRIGGER | W1S | R | 0 | Triggers PXRES. This causes a full-scope reset and reboot. |

26.8.43 PWR_TRIM_WAKE_CTL

Description: Wakeup Trim Register
Address: 0x40263008
Offset: 0x3008
Retention: Retained
IsDeepSleep: Yes
Comment: Trim bits for DEEPSLEEP wakeup.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|----|----|----|----|----|----|----|
| Name | WAKE_DELAY [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:7 | WAKE_DELAY | RW | R | 0 | Wakeup holdoff specifies the number of IMO cycles for power system settling before continuing the wakeup sequence. Fastest wakeup is achieved by using the smallest number allowed for the product. |

26.8.44 CLK_TRIM_ILO0_CTL

Description: ILO0 Trim Register
Address: 0x40263014
Offset: 0x3014
Retention: Retained
IsDeepSleep: No
Comment: Trims ILO frequency. Determined during manufacturing sort/class, but may be updated in the field to calibrate voltage and temperature conditions. This register is protected by WDT_CTL.WDT_LOCK. ILO0 configuration and trims are reset by XRES and power-related resets, unless configured otherwise.
Default: 0x52C

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|------------------|----|---------------------|----|----|----|
| Name | None [7:6] | | ILO0_FTRIM [5:0] | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | ILO0_MONTRIM [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:5 | ILO0_FTRIM | RW | A | 44 | ILO0 frequency trims. LSB step size is 1.5 percent (typical) of the frequency. |
| 8:11 | ILO0_MONTRIM | RW | A | 5 | ILO0 internal monitor trim. |

26.8.45 CLK_TRIM_ILO1_CTL

Description: ILO1 Trim Register
Address: 0x40263220
Offset: 0x3220
Retention: Retained
IsDeepSleep: Yes
Comment: Trims ILO frequency. Determined during manufacturing sort/class, but may be updated in the field to calibrate voltage and temperature conditions.
Default: 0x52C

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|------------------|----|---------------------|----|----|----|
| Name | None [7:6] | | ILO1_FTRIM [5:0] | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | ILO1_MONTRIM [11:8] | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|--|
| 0:5 | ILO1_FTRIM | RW | R | 44 | ILO1 frequency trims. LSB step size is 1.5 percent (typical) of the frequency. |
| 8:11 | ILO1_MONTRIM | RW | R | 5 | ILO1 internal monitor trim. |

26.8.46 CSV_HF

26.8.46.1 CSV

26.8.46.1.1 CSV_HF_CSV_REF_CTL

Description: Clock Supervision Reference Control
Address: 0x40261400
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Controls clock supervision for a clock tree.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------------|--------------|----|----|----|----|----|
| Name | STARTUP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | STARTUP [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CSV_EN [31:31] | CSV_ACTION [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:15 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 30 | CSV_ACTION | RW | R | 0 | Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). |
| | FAULT | | | 0 | Do a Fault report. |
| | RESET | | | 1 | Cause a power reset. This should only be used for clk_hf0. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. |

26.8.46.1.2 CSV_HF_CSV_REF_LIMIT

Description: Clock Supervision Reference Limits
Address: 0x40261404
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | LOWER [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | LOWER [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | UPPER [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | UPPER [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--|
| 0:15 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:31 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

26.8.46.1.3 CSV_HF_CSV_MON_CTL

Description: Clock Supervision Monitor Control
Address: 0x40261408
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | PERIOD [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PERIOD [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:15 | PERIOD | RW | R | 0 | <p>Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens.</p> <p>$PERIOD \leq (UPPER+1) / FREQ_RATIO -1$, with $FREQ_RATIO = (Reference\ frequency / Monitored\ frequency)$</p> <p>In case the clocks are asynchronous: $PERIOD \leq UPPER / FREQ_RATIO -1$</p> <p>Additionally margin must be added for accuracy of both clocks.</p> |

26.8.47 CSV_REF

26.8.47.1 CSV

26.8.47.1.1 CSV_REF_CSV_REF_CTL

Description: Clock Supervision Reference Control
Address: 0x40261710
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Controls clock supervision for a clock tree.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------------|--------------|----|----|----|----|----|
| Name | STARTUP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | STARTUP [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CSV_EN [31:31] | CSV_ACTION [30:30] | None [29:24] | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:15 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 30 | CSV_ACTION | RW | R | 0 | Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). |
| | FAULT | | | 0 | Do a Fault report. |
| | RESET | | | 1 | Cause a power reset. This should only be used for clk_hf0. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. |

26.8.47.1.2 CSV_REF_CSV_REF_LIMIT

Description: Clock Supervision Reference Limits
Address: 0x40261714
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | LOWER [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | LOWER [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | UPPER [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | UPPER [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--|
| 0:15 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:31 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

26.8.47.1.3 CSV_REF_CSV_MON_CTL

Description: Clock Supervision Monitor Control
Address: 0x40261718
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | PERIOD [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PERIOD [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:15 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. $PERIOD \leq (UPPER+1) / FREQ_RATIO -1$, with $FREQ_RATIO = (Reference\ frequency / Monitored\ frequency)$ In case the clocks are asynchronous: $PERIOD \leq UPPER / FREQ_RATIO -1$ Additionally margin must be added for accuracy of both clocks. |

26.8.48 CSV_LF

26.8.48.1 CSV

26.8.48.1.1 CSV_LF_CSV_REF_CTL

Description: Clock Supervision Reference Control
Address: 0x40261720
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Controls clock supervision for a clock tree.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | STARTUP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CSV_EN [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot. A CSV error detection is reported to the Fault structure. |

26.8.48.1.2 CSV_LF_CSV_REF_LIMIT

Description: Clock Supervision Reference Limits
Address: 0x40261724
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | LOWER [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | UPPER [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--|
| 0:7 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:23 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

26.8.48.1.3 CSV_LF_CSV_MON_CTL

Description: Clock Supervision Monitor Control
Address: 0x40261728
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | PERIOD [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. $PERIOD \leq (UPPER+1) / FREQ_RATIO - 1$, with $FREQ_RATIO = (\text{Reference frequency} / \text{Monitored frequency})$ In case the clocks are asynchronous: $PERIOD \leq UPPER / FREQ_RATIO - 1$ Additionally margin must be added for accuracy of both clocks. |

26.8.49 CSV_ILO

26.8.49.1 CSV

26.8.49.1.1 CSV_ILO_CSV_REF_CTL

Description: Clock Supervision Reference Control
Address: 0x40261730
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment: Controls clock supervision for a clock tree.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | STARTUP [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CSV_EN [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:7 | STARTUP | RW | R | 0 | Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. |
| 31 | CSV_EN | RW | R | 0 | Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot. A CSV error detection is reported to the Fault structure. |

26.8.49.1.2 CSV_ILO_CSV_REF_LIMIT

Description: Clock Supervision Reference Limits
Address: 0x40261734
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | LOWER [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | UPPER [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------|----|----|-----------------|--|
| 0:7 | LOWER | RW | R | 0 | Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. |
| 16:23 | UPPER | RW | R | 0 | Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. |

26.8.49.1.3 CSV_ILO_CSV_MON_CTL

Description: Clock Supervision Monitor Control
Address: 0x40261738
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | PERIOD [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:7 | PERIOD | RW | R | 0 | Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. $PERIOD \leq (UPPER+1) / FREQ_RATIO -1$, with $FREQ_RATIO = (Reference\ frequency / Monitored\ frequency)$ In case the clocks are asynchronous: $PERIOD \leq UPPER / FREQ_RATIO -1$ Additionally margin must be added for accuracy of both clocks. |

26.8.50 MCWDT

26.8.50.1 MCWDT_CPU_SELECT

Description: MCWDT CPU selection register
Address: 0x40268040
Offset: 0x40
Retention: Retained
IsDeepSleep: Yes
Comment: Assigns this MCWDT to a CPU.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---------------|---|
| Name | None [7:2] | | | | | | CPU_SEL [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0:1 | CPU_SEL | RW | R | 0 | Assigns this MCWDT to a CPU. This selects which CPU SLEEPDEEP signal is used for SLEEPDEEP_PAUSE. |

26.8.50.2 MCWDT_CTR2_CTL

Description: MCWDT Subcounter 2 Control register
Address: 0x40268080
Offset: 0x80
Retention: Retained
IsDeepSleep: Yes
Comment: Control register for MCWDT subcounter 2. Writes are ignored when locked (i.e. corresponding LOCK.MCWDT_LOCK<=>0). This register may be written while the counter is running, but new values may take up to 2 clk_Lf cycles to take effect.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------|
| Name | None [7:1] | | | | | | | ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | ENABLED | R | RW | 0 | Indicates actual state of this subcounter. May lag ENABLE by up to two clk_Lf cycles. |
| 31 | ENABLE | RW | R | 0 | Enable subcounter. May take up to 2 clk_Lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) |

26.8.50.3 MCWDT_CTR2_CONFIG

Description: MCWDT Subcounter 2 Configuration register
Address: 0x40268084
Offset: 0x84
Retention: Retained
IsDeepSleep: Yes
Comment: Configuration for MCWDT subcounter 2. Writes are ignored when locked (i.e. corresponding LOCK.MCWDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_If cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter and wait until it reads back low. This prevents possible unintended actions caused by synchronization delays.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|--------------|
| Name | None [7:1] | | | | | | | ACTION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|--------------|----|----|----|----|
| Name | None [23:21] | | | BITS [20:16] | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|-------------------------|--------------|--------------------------|--------------|----|----|----|
| Name | DEBUG_RUN [31:31] | SLEEPDEEP_PAUSE [30:30] | None [29:29] | DEBUG_TRIGGER_EN [28:28] | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|------------------|----|----|-----------------|--|
| 0 | ACTION | RW | R | 0 | Action taken when the specified BIT toggles. Action will be triggered on the same edge where BITS to observe toggle. |
| | NOTHING | | | 0 | Do nothing |
| | INT | | | 1 | Trigger an interrupt |
| 16:20 | BITS | RW | R | 0 | Bit to observe for a toggle: 0: Do ACTION after CNT[0] toggles (i.e. every tick) . 31: Do ACTION after CNT[31] toggles (i.e. every 2^31 ticks) |
| 28 | DEBUG_TRIGGER_EN | RW | R | 0 | Enables the trigger input for this MCWDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this MCWDT, and then set this bit. It takes up to two clk_If cycles for the trigger signal to be processed. Triggers that are less than two clk_If cycles may be missed. Synchronization errors can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| 30 | SLEEPDEEP_PAUSE | RW | R | 0 | <p>Pauses/runs this counter when the corresponding processor is in SLEEPDEEP. Note it may take up to two clk_If cycles for the counter to pause and up to two clk_If cycles for it to unpause, due to internal synchronization.</p> <p>0: Counter runs normally regardless of processor mode.</p> <p>1: Counter pauses when corresponding processor is in SLEEPDEEP.</p> |
| 31 | DEBUG_RUN | RW | R | 0 | <p>Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_If cycles for the counter to pause and another two cycles to unpause, due to internal synchronization.</p> <p>0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN.</p> <p>1: When debugger connected, counter increments normally, but reset generation is blocked.</p> |

26.8.50.4 MCWDT_CTR2_CNT

Description: MCWDT Subcounter 2 Count Register
Address: 0x40268088
Offset: 0x88
Retention: Retained
IsDeepSleep: Yes
Comment: Count value for this MCWDT subcounter 2. Writes are ignored when this subcounter is enabled or when it is locked (i.e. corresponding LOCK.MCWDT_LOCK<>0).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | CNT2 [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CNT2 [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CNT2 [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CNT2 [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CNT2 | RW | A | 0 | Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_if cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. |

26.8.50.5 MCWDT_LOCK

Description: MCWDT Lock Register
Address: 0x40268090
Offset: 0x90
Retention: Retained
IsDeepSleep: No
Comment: Lock or unlock the respective configuration registers of subcounters 0/1/2 of this MCWDT.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|------------------|---|
| Name | None [7:2] | | | | | | MCWDT_LOCK [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:1 | MCWDT_LOCK | RW | A | 0 | Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. |
| | NO_CHG | | | 0 | No effect |
| | CLR0 | | | 1 | Clears bit 0 |
| | CLR1 | | | 2 | Clears bit 1 |
| | SET01 | | | 3 | Sets both bits 0 and 1 |

26.8.50.6 MCWDT_SERVICE

Description: MCWDT Service Register
Address: 0x40268094
Offset: 0x94
Retention: Retained
IsDeepSleep: Yes
Comment: Control the behavior of the Watchdog counters. Writes to this register are ignored when LOCK.MCWDT_LOCK<>0. All fields in this register can be used while counter is in operation.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|--------------------|--------------------|
| Name | None [7:2] | | | | | | CTR1_SERVICE [1:1] | CTR0_SERVICE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|------|------|-----------------|---|
| 0 | CTR0_SERVICE | RW1S | RW1C | 0 | Services subcounter 0. This resets the count value for subcounter 0 to zero. This may take up to three clk_if cycles to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending CTR0_SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write CTR0_SERVICE=1. If subcounter 0 is disabled, CTR0_SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. |
| 1 | CTR1_SERVICE | RW1S | RW1C | 0 | Services subcounter 1. This resets the count value for subcounter 1 to zero. This may take up to three clk_if cycles to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending CTR1_SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write CTR1_SERVICE=1. If subcounter 1 is disabled, CTR1_SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. |

26.8.50.7 MCWDT_INTR

Description: MCWDT Interrupt Register
Address: 0x402680A0
Offset: 0xA0
Retention: Retained
IsDeepSleep: No
Comment: Interrupt status register for MCWDT subcounters.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------|----------------|----------------|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|----|-----------------|---|
| 0 | CTR0_INT | RW1C | A | 0 | MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. |
| 1 | CTR1_INT | RW1C | A | 0 | MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. |
| 2 | CTR2_INT | RW1C | A | 0 | MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. |

26.8.50.8 MCWDT_INTR_SET

Description: MCWDT Interrupt Set Register
Address: 0x402680A4
Offset: 0xA4
Retention: Retained
IsDeepSleep: No
Comment: This register can be used to trigger an interrupt for firmware testing.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------|----------------|----------------|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|----|-----------------|------------------------------|
| 0 | CTR0_INT | RW1S | A | 0 | Set interrupt for MCWDT_INT0 |
| 1 | CTR1_INT | RW1S | A | 0 | Set interrupt for MCWDT_INT1 |
| 2 | CTR2_INT | RW1S | A | 0 | Set interrupt for MCWDT_INT2 |

26.8.50.9 MCWDT_INTR_MASK

Description: MCWDT Interrupt Mask Register
Address: 0x402680A8
Offset: 0xA8
Retention: Retained
IsDeepSleep: No
Comment: This register controls whether a subcounter interrupt is forwarded to the corresponding processor. All masks block the interrupt when 0 and forward the interrupt when 1.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------|----------------|----------------|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|--|
| 0 | CTR0_INT | RW | R | 0 | Interrupt Mask for sub-counter 0 for warning interrupt. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. |
| 1 | CTR1_INT | RW | R | 0 | Interrupt Mask for sub-counter 1 for warning interrupt. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. |
| 2 | CTR2_INT | RW | R | 0 | Interrupt Mask for sub-counter 2. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. |

26.8.50.10 MCWDT_INTR_MASKED

Description: MCWDT Interrupt Masked Register

Address: 0x402680AC

Offset: 0xAC

Retention: Retained

IsDeepSleep: No

Comment: Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation. Each available MCWDT has a copy of this register.

Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|----------------|----------------|----------------|
| Name | None [7:3] | | | | | CTR2_INT [2:2] | CTR1_INT [1:1] | CTR0_INT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0 | CTR0_INT | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 1 | CTR1_INT | R | RW | 0 | Logical and of corresponding request and mask bits. |
| 2 | CTR2_INT | R | RW | 0 | Logical and of corresponding request and mask bits. |

26.8.50.11 CTR

26.8.50.11.1 MCWDT_CTR_CTL

Description: MCWDT Subcounter Control Register
Address: 0x40268000
Offset: 0x0
Retention: Retained
IsDeepSleep: Yes
Comment: Control register for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_Lf cycles to take effect.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------|
| Name | None [7:1] | | | | | | | ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | ENABLED | R | RW | 0 | Indicates actual state of this subcounter. May lag ENABLE by up to two clk_Lf cycles. |
| 31 | ENABLE | RW | R | 0 | Enable subcounter. May take up to 2 clk_Lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) |

26.8.50.11.2 MCWDT_CTR_LOWER_LIMIT

Description: MCWDT Subcounter Lower Limit Register
Address: 0x40268004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: Lower limit for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_{lf} cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter within the configured limits. This prevents possible unintended actions caused by the updated limits.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | LOWER_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | LOWER_LIMIT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:15 | LOWER_LIMIT | RW | R | 0 | Lower limit for this MCWDT subcounter. See LOWER_ACTION. |

26.8.50.11.3 MCWDT_CTR_UPPER_LIMIT

Description: MCWDT Subcounter Upper Limit Register
Address: 0x40268008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Upper limit for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_{lf} cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter within the configured limits. This prevents possible unintended actions caused by the updated limits.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | UPPER_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | UPPER_LIMIT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|--|
| 0:15 | UPPER_LIMIT | RW | R | 0 | Upper limit for this MCWDT subcounter. See UPPER_ACTION. |

26.8.50.11.4 MCWDT_CTR_WARN_LIMIT

Description: MCWDT Subcounter Warn Limit Register
Address: 0x4026800C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Warn limit for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_{If} cycles to take effect. Before changing the limit, it is recommended to set the service bit for this subcounter within the configured limits. This prevents possible unintended actions caused by the updated limits.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | WARN_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | WARN_LIMIT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|--|
| 0:15 | WARN_LIMIT | RW | R | 0 | Warn limit for this MCWDT subcounter. See WARN_ACTION. |

26.8.50.11.5 MCWDT_CTR_CONFIG

| | |
|---------------------|--|
| Description: | MCWDT Subcounter Configuration Register |
| Address: | 0x40268010 |
| Offset: | 0x10 |
| Retention: | Retained |
| IsDeepSleep: | No |
| Comment: | Configuration for this MCWDT subcounter. Writes are ignored when locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0). This register may be written while the counter is running, but new values may take up to 2 clk_If cycles to take effect. MCWDT always reports the first fault that occurs across subcounter #0 and subcounter #1 for this MCWDT, but may not report additional faults that occur while the first is being processed. |
| Default: | 0x0 |

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|--------------------|---|------------|---|--------------------|---|
| Name | None [7:6] | | UPPER_ACTION [5:4] | | None [3:2] | | LOWER_ACTION [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----------------------|-------------|----|---|-------------------|
| Name | None [15:13] | | | AUTO_SERVICE [12:12] | None [11:9] | | | WARN_ACTION [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|-------------------------|--------------|--------------------------|--------------|----|----|----|
| Name | DEBUG_RUN [31:31] | SLEEPDEEP_PAUSE [30:30] | None [29:29] | DEBUG_TRIGGER_EN [28:28] | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|---|
| 0:1 | LOWER_ACTION | RW | R | 0 | Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the corresponding processor is in SLEEPDEEP. |
| | NOTHING | | | 0 | Do nothing |
| | FAULT | | | 1 | Trigger a fault. It can take up to 3 clk_If cycles for the fault to be transferred to the fault manager. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered. |
| | FAULT_THEN_RESET | | | 2 | Trigger a fault. Further, trigger a system-wide reset if the fault is not serviced and the watchdog is not cleared within 6 clk_If cycles. It can take up to 3 clk_If cycles for the fault to be transferred to the fault manager, which gives at least 3 clk_If cycles for software to respond. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered. |
| 4:5 | UPPER_ACTION | RW | R | 0 | Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. |
| | NOTHING | | | 0 | Do nothing |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| | FAULT | | | 1 | Trigger a fault. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_Lf cycle to trigger. |
| | FAULT_THEN_RESET | | | 2 | Trigger a fault. Further, trigger a system-wide reset if the fault is not serviced and the watchdog is not cleared within 6 clk_Lf cycles. It can take up to 3 clk_Lf cycles for the fault to be transferred to the fault manager, which gives at least 3 clk_Lf cycles for software to respond. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_Lf cycle to trigger. |
| 8 | WARN_ACTION | RW | R | 0 | Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically. For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For WARN_LIMIT == [0,1] : The action may take up to one extra clk_Lf cycle to trigger. |
| | NOTHING | | | 0 | Do nothing |
| | INT | | | 1 | Trigger an interrupt. |
| 12 | AUTO_SERVICE | RW | R | 0 | Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING. |
| 28 | DEBUG_TRIGGER_EN | RW | R | 0 | Enables the trigger input for this MCWDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this MCWDT, and then set this bit. It takes up to two clk_Lf cycles for the trigger signal to be processed. Triggers that are less than two clk_Lf cycles may be missed. Synchronization errors can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high. |
| 30 | SLEEPDEEP_PAUSE | RW | R | 0 | Pauses/runs this counter when the corresponding processor is in SLEEPDEEP. Note it may take up to two clk_Lf cycles for the counter to pause and up to two clk_Lf cycles for it to unpause, due to internal synchronization. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter runs normally regardless of processor mode. 1: Counter pauses when corresponding processor is in SLEEPDEEP. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 31 | DEBUG_RUN | RW | R | 0 | <p>Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_If cycles for the counter to pause, due to internal synchronization.</p> <p>When (DEBUG_RUN==1 or DEBUG_TRIGGER_EN==0) and the debugger is connected for at least two clk_If cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. After the debugger is disconnected, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_If cycles, the LOWER_ACTION may or may not be ignored.</p> <p>0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN.</p> <p>1: When debugger connected, counter increments normally, but reset generation is blocked. To block LOWER_ACTION fault generation, write DEBUG_TRIGGER_EN==0.</p> |

26.8.50.11.6 MCWDT_CTR_CNT

Description: MCWDT Subcounter Count Register
Address: 0x40268014
Offset: 0x14
Retention: Retained
IsDeepSleep: Yes
Comment: Count value for this MCWDT subcounter. Writes are ignored when this subcounter is enabled or when it is locked (i.e. corresponding MCWDT[i]_LOCK.WDT_LOCK<>0).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | CNT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CNT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:15 | CNT | RW | A | 0 | Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk. If cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. |

26.8.51 WDT

26.8.51.1 WDT_CTL

Description: WDT Control Register
Address: 0x4026C000
Offset: 0x0
Retention: Retained
IsDeepSleep: Yes
Comment: Control register for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0).
Default: 0x80000001

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------|
| Name | None [7:1] | | | | | | | ENABLED [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|----------------|--------------|----|----|----|----|----|----|
| Name | ENABLE [31:31] | None [30:24] | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|---|
| 0 | ENABLED | R | RW | 1 | Indicates actual state of watchdog. May lag ENABLE by up to three clk_ilo0 cycles. |
| 31 | ENABLE | RW | A | 1 | Enable watchdog. May take up to three clk_ilo0 cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. Do not enter DEEPSLEEP or HIBERNATE mode if ENABLE<>ENABLED. This can be done by waiting until ENABLE==ENABLED whenever ENABLE is changed. 0: Counter is disabled (not clocked). 1: Counter is enabled (counting up) |

26.8.51.2 WDT_LOWER_LIMIT

Description: WDT Lower Limit Register
Address: 0x4026C004
Offset: 0x4
Retention: Retained
IsDeepSleep: No
Comment: Lower limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | LOWER_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | LOWER_LIMIT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | LOWER_LIMIT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | LOWER_LIMIT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:31 | LOWER_LIMIT | RW | A | 0 | Lower limit for watchdog. See LOWER_ACTION. |

26.8.51.3 WDT_UPPER_LIMIT

Description: WDT Upper Limit Register
Address: 0x4026C008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment: Upper limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x8000

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------|----|----|----|----|----|----|----|
| Name | UPPER_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | UPPER_LIMIT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | UPPER_LIMIT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | UPPER_LIMIT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------------|----|----|-----------------|---|
| 0:31 | UPPER_LIMIT | RW | A | 32768 | Upper limit for watchdog. See UPPER_ACTION. |

26.8.51.4 WDT_WARN_LIMIT

Description: WDT Warn Limit Register
Address: 0x4026C00C
Offset: 0xC
Retention: Retained
IsDeepSleep: No
Comment: Warn limit for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | WARN_LIMIT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | WARN_LIMIT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | WARN_LIMIT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | WARN_LIMIT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------|----|----|-----------------|---|
| 0:31 | WARN_LIMIT | RW | A | 0 | Warn limit for watchdog. See WARN_ACTION. |

26.8.51.5 WDT_CONFIG

Description: WDT Configuration Register
Address: 0x4026C010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment: Configuration for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|--------------------|------------|---|---|--------------------|
| Name | None [7:5] | | | UPPER_ACTION [4:4] | None [3:1] | | | LOWER_ACTION [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----------------------|-------------|----|---|-------------------|
| Name | None [15:13] | | | AUTO_SERVICE [12:12] | None [11:9] | | | WARN_ACTION [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-------------------|-------------------|---------------------|--------------------------|--------------|----|----|----|
| Name | DEBUG_RUN [31:31] | HIB_PAUSE [30:30] | DPSLP_PAUSE [29:29] | DEBUG_TRIGGER_EN [28:28] | None [27:24] | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0 | LOWER_ACTION | RW | A | 0 | Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the chip is in DEEPSLEEP/HIBERNATE modes. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered. |
| | NOTHING | | | 0 | Do nothing |
| | RESET | | | 1 | Trigger a reset. |
| 4 | UPPER_ACTION | RW | A | 1 | Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_ilo0 cycle to trigger. |
| | NOTHING | | | 0 | Do nothing |
| | RESET | | | 1 | Trigger a reset. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 8 | WARN_ACTION | RW | A | 0 | Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically. For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For WARN_LIMIT < 2 : The action may take up to one extra clk_ilo0 cycle to trigger. |
| | NOTHING | | | 0 | Do nothing |
| | INT | | | 1 | Trigger an interrupt. |
| 12 | AUTO_SERVICE | RW | A | 0 | Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING. |
| 28 | DEBUG_TRIGGER_EN | RW | A | 0 | Enables the trigger input for WDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this WDT, and then set this bit. It takes up to two clk_ilo0 cycles for the trigger signal to be processed. Triggers that are less than two clk_ilo0 cycles may be missed. Synchronization error can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high. |
| 29 | DPSLP_PAUSE | RW | A | 0 | Pauses/runs this counter when the system is in DEEPSLEEP. Note it may take up to two clk_ilo0 cycles for the counter to pause, due to internal synchronization. During DEEPSLEEP wakeup, the pause request is removed when clk_hf0 starts clocking, and then it may take up to two clk_ilo0 cycles for the counter to start. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter behaves normally during DEEPSLEEP. 1: Counter pauses during DEEPSLEEP. |
| 30 | HIB_PAUSE | RW | A | 0 | Pauses/runs this counter when the system is in HIBERNATE. Note it may take up to two clk_ilo0 cycles for the counter to pause, due to internal synchronization. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter behaves normally during HIBERNATE. 1: Counter pauses during HIBERNATE. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| 31 | DEBUG_RUN | RW | A | 0 | <p>Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_ilo0 cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_ilo0 cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_ilo0 cycles, the LOWER_ACTION may or may not be ignored.</p> <p>0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN. 1: When debugger connected, counter increments normally, but reset generation is blocked.</p> |

26.8.51.6 WDT_CNT

Description: WDT Count Register
Address: 0x4026C014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment: Count value for watchdog. Writes are ignored when locked (i.e. Corresponding LOCK.WDT_LOCK<>0) or when enabled (i.e. ENABLE==1 and ENABLED==1).
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | CNT [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | CNT [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | CNT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | CNT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CNT | RW | A | 0 | Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_ilo0 cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. |

26.8.51.7 WDT_LOCK

Description: WDT Lock register
Address: 0x4026C040
Offset: 0x40
Retention: Retained
IsDeepSleep: No
Comment: Lock or unlock the registers in this WDT
Default: 0x3

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|----------------|---|
| Name | None [7:2] | | | | | | WDT_LOCK [1:0] | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|----|----|-----------------|---|
| 0:1 | WDT_LOCK | RW | A | 3 | Prohibits writing control and configuration registers related to this WDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. This register also locks the clk_ilo0 settings. |
| | NO_CHG | | | 0 | No effect |
| | CLR0 | | | 1 | Clears bit 0 |
| | CLR1 | | | 2 | Clears bit 1 |
| | SET01 | | | 3 | Sets both bits 0 and 1 |

26.8.51.8 WDT_SERVICE

Description: WDT Service register
Address: 0x4026C044
Offset: 0x44
Retention: Retained
IsDeepSleep: Yes
Comment: Control the behavior of the Watchdog counters. Writes to this register are ignored when LOCK.WDT_LOCK<>0. All fields in this register can be used while counter is in operation.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|---------------|
| Name | None [7:1] | | | | | | | SERVICE [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|------|------|-----------------|---|
| 0 | SERVICE | RW1S | RW1C | 0 | Services the watchdog. This resets the count value to zero. This may take up to three clk_ilo0 cycle to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write SERVICE=1. If WDT is disabled, SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. |

26.8.51.9 WDT_INTR

Description: WDT Interrupt Register
Address: 0x4026C050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Interrupt signal from WDT
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-----------|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0 | WDT | RW1C | A | 0 | WDT Interrupt Request. This bit is set as configured by WDT action and limits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1C or reading this register and during this time AHB bus is stalled. |

26.8.51.10 WDT_INTR_SET

Description: WDT Interrupt Set Register
Address: 0x4026C054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment: Can be used to set interrupts for firmware testing.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-----------|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|------|----|-----------------|--|
| 0 | WDT | RW1S | A | 0 | Set interrupt. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1S or reading from this register and during this time AHB bus is stalled. |

26.8.51.11 WDT_INTR_MASK

Description: WDT Interrupt Mask Register
Address: 0x4026C058
Offset: 0x58
Retention: Retained
IsDeepSleep: No
Comment: Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|---|---|-----------|
| Name | None [7:1] | | | | | | | WDT [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0 | WDT | RW | R | 0 | Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. |

26.8.51.12 WDT_INTR_MASKED

Description: WDT Interrupt Masked Register
Address: 0x4026C05C
Offset: 0x5C
Retention: Retained
IsDeepSleep: No
Comment: Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|----|----|----|----|----|----|-----------|
| Name | None [7:1] | | | | | | | WDT [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0 | WDT | R | RW | 0 | Logical and of corresponding request and mask bits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to read from this register. During this time AHB bus is stalled. |

27 SYSAP

| | |
|---------------------|--|
| Description | System debug Access Port (SYSAP) registers |
| Base Address | 0xE0000000 |
| Size | 0x20000000 |
| Slave Num | SYSTEM |

27.1 ROMTABLE

| Register Name | Address | Permission | Description |
|-------------------------------------|------------|------------|---------------------------------------|
| SYSAP_ROMTABLE_DID | 0xF1000FCC | FULL | Device Type Identifier register. |
| SYSAP_ROMTABLE_PID4 | 0xF1000FD0 | FULL | Peripheral Identification Register 4. |
| SYSAP_ROMTABLE_PID5 | 0xF1000FD4 | FULL | Peripheral Identification Register 5. |
| SYSAP_ROMTABLE_PID6 | 0xF1000FD8 | FULL | Peripheral Identification Register 6. |
| SYSAP_ROMTABLE_PID7 | 0xF1000FDC | FULL | Peripheral Identification Register 7. |
| SYSAP_ROMTABLE_PID0 | 0xF1000FE0 | FULL | Peripheral Identification Register 0. |
| SYSAP_ROMTABLE_PID1 | 0xF1000FE4 | FULL | Peripheral Identification Register 1. |
| SYSAP_ROMTABLE_PID2 | 0xF1000FE8 | FULL | Peripheral Identification Register 2. |
| SYSAP_ROMTABLE_PID3 | 0xF1000FEC | FULL | Peripheral Identification Register 3. |
| SYSAP_ROMTABLE_CID0 | 0xF1000FF0 | FULL | Component Identification Register 0. |
| SYSAP_ROMTABLE_CID1 | 0xF1000FF4 | FULL | Component Identification Register 1. |
| SYSAP_ROMTABLE_CID2 | 0xF1000FF8 | FULL | Component Identification Register 2. |
| SYSAP_ROMTABLE_CID3 | 0xF1000FFC | FULL | Component Identification Register 3. |

27.2 Register Details

27.2.1 ROMTABLE

27.2.1.1 SYSAP_ROMTABLE_DID

Description: Device Type Identifier register.
Address: 0xF1000FCC
Offset: 0xFCC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 1 | . |

27.2.1.2 SYSAP_ROMTABLE_PID4

Description: Peripheral Identification Register 4.
Address: 0xF1000FD0
Offset: 0xFD0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|------------------------|---|---|---|
| Name | COUNT [7:4] | | | | JEP_CONTINUATION [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------------------|----|----|-----------------|--|
| 0:3 | JEP_CONTINUATION | R | R | Undefined | JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. |
| 4:7 | COUNT | R | R | 0 | Size of ROM Table is $2^{\text{COUNT}} * 4$ KByte. |

27.2.1.3 SYSAP_ROMTABLE_PID5

Description: Peripheral Identification Register 5.
Address: 0xF1000FD4
Offset: 0xFD4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | . |

27.2.1.4 SYSAP_ROMTABLE_PID6

Description: Peripheral Identification Register 6.
Address: 0xF1000FD8
Offset: 0xFD8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | . |

27.2.1.5 SYSAP_ROMTABLE_PID7

Description: Peripheral Identification Register 7.
Address: 0xF1000FDC
Offset: 0xFDC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|-------------|
| 0:31 | VALUE | R | R | 0 | . |

27.2.1.6 SYSAP_ROMTABLE_PID0

Description: Peripheral Identification Register 0.
Address: 0xF1000FE0
Offset: 0xFE0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | PN_MIN [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:7 | PN_MIN | R | R | Undefined | JEP106 part number. 4 lsb of CPUSS.PARTNUMBER parameter. |

27.2.1.7 SYSAP_ROMTABLE_PID1

Description: Peripheral Identification Register 1.
Address: 0xF1000FE4
Offset: 0xFE4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|----|----|--------------|----|----|----|
| Name | JEPID_MIN [7:4] | | | | PN_MAJ [3:0] | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:3 | PN_MAJ | R | R | Undefined | JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. |
| 4:7 | JEPID_MIN | R | R | Undefined | JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. |

27.2.1.8 SYSAP_ROMTABLE_PID2

Description: Peripheral Identification Register 2.
Address: 0xF1000FE8
Offset: 0xFE8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|------------|-----------------|---|---|
| Name | REV [7:4] | | | | None [3:3] | JEPID_MAJ [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:2 | JEPID_MAJ | R | R | Undefined | JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. |
| 4:7 | REV | R | R | Undefined | Major REVersion number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. |

27.2.1.9 SYSAP_ROMTABLE_PID3

Description: Peripheral Identification Register 3.
Address: 0xF1000FEC
Offset: 0xFEC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|----------|---|---|---|
| Name | REV_AND [7:4] | | | | CM [3:0] | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:3 | CM | R | R | 0 | N/A |
| 4:7 | REV_AND | R | R | Undefined | Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs. |

27.2.1.10 SYSAP_ROMTABLE_CID0

Description: Component Identification Register 0.
Address: 0xF1000FF0
Offset: 0xFF0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xD

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 13 | Component identification byte 0 of 4-byte component identification 0xB105:100D. |

27.2.1.11 SYSAP_ROMTABLE_CID1

Description: Component Identification Register 1.
Address: 0xF1000FF4
Offset: 0xFF4
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x10

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 16 | Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: 'ROM Table'. |

27.2.1.12 SYSAP_ROMTABLE_CID2

Description: Component Identification Register 2.
Address: 0xF1000FF8
Offset: 0xFF8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x5

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 5 | Component identification byte 2 of 4-byte component identification 0xB105:100D. |

27.2.1.13 SYSAP_ROMTABLE_CID3

Description: Component Identification Register 3.
Address: 0xF1000FFC
Offset: 0xFFC
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xB1

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------|---|---|---|---|---|---|---|
| Name | VALUE [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|--------------|----|----|----|----|----|---|---|
| Name | VALUE [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|---------------|----|----|----|----|----|----|----|
| Name | VALUE [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-------|----|----|-----------------|---|
| 0:31 | VALUE | R | R | 177 | Component identification byte 3 of 4-byte component identification 0xB105:100D. |

28 TCPWM

| | |
|--------------|-------------------|
| Description | Timer/Counter/PWM |
| Base Address | 0x40380000 |
| Size | 0x20000 |
| Slave Num | MMIO3 - 3 |

28.1 GRP 0

28.1.1 CNT 0

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT0_CTRL | 0x40380000 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT0_STATUS | 0x40380004 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT0_COUNTER | 0x40380008 | FULL | Counter count register |
| TCPWM0_GRP0_CNT0_CC0 | 0x40380010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT0_CC0_BUFF | 0x40380014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT0_CC1 | 0x40380018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT0_CC1_BUFF | 0x4038001C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT0_PERIOD | 0x40380020 | FULL | Counter period register |
| TCPWM0_GRP0_CNT0_PERIOD_BUFF | 0x40380024 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT0_DT | 0x40380030 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT0_TR_CMD | 0x40380040 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT0_TR_IN_SEL0 | 0x40380044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT0_TR_IN_SEL1 | 0x40380048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL | 0x4038004C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT0_TR_PWM_CTRL | 0x40380050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT0_TR_OUT_SEL | 0x40380054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT0_INTR | 0x40380070 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT0_INTR_SET | 0x40380074 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT0_INTR_MASK | 0x40380078 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT0_INTR_MASKED | 0x4038007C | FULL | Interrupt masked request register |

28.1.2 CNT 1

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT1_CTRL | 0x40380080 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT1_STATUS | 0x40380084 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT1_COUNTER | 0x40380088 | FULL | Counter count register |
| TCPWM0_GRP0_CNT1_CC0 | 0x40380090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT1_CC0_BUFF | 0x40380094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT1_CC1 | 0x40380098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT1_CC1_BUFF | 0x4038009C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT1_PERIOD | 0x403800A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT1_PERIOD_BUFF | 0x403800A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT1_DT | 0x403800B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT1_TR_CMD | 0x403800C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT1_TR_IN_SEL0 | 0x403800C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT1_TR_IN_SEL1 | 0x403800C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT1_TR_IN_EDGE_SEL | 0x403800CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT1_TR_PWM_CTRL | 0x403800D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT1_TR_OUT_SEL | 0x403800D4 | FULL | Counter output trigger selection register |

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP0_CNT1_INTR | 0x403800F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT1_INTR_SET | 0x403800F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT1_INTR_MASK | 0x403800F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT1_INTR_MASKED | 0x403800FC | FULL | Interrupt masked request register |

28.1.3 CNT 2

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT2_CTRL | 0x40380100 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT2_STATUS | 0x40380104 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT2_COUNTER | 0x40380108 | FULL | Counter count register |
| TCPWM0_GRP0_CNT2_CC0 | 0x40380110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT2_CC0_BUFF | 0x40380114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT2_CC1 | 0x40380118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT2_CC1_BUFF | 0x4038011C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT2_PERIOD | 0x40380120 | FULL | Counter period register |
| TCPWM0_GRP0_CNT2_PERIOD_BUFF | 0x40380124 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT2_DT | 0x40380130 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT2_TR_CMD | 0x40380140 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT2_TR_IN_SEL0 | 0x40380144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT2_TR_IN_SEL1 | 0x40380148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT2_TR_IN_EDGE_SEL | 0x4038014C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT2_TR_PWM_CTRL | 0x40380150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT2_TR_OUT_SEL | 0x40380154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT2_INTR | 0x40380170 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT2_INTR_SET | 0x40380174 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT2_INTR_MASK | 0x40380178 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT2_INTR_MASKED | 0x4038017C | FULL | Interrupt masked request register |

28.1.4 CNT 3

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT3_CTRL | 0x40380180 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT3_STATUS | 0x40380184 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT3_COUNTER | 0x40380188 | FULL | Counter count register |
| TCPWM0_GRP0_CNT3_CC0 | 0x40380190 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT3_CC0_BUFF | 0x40380194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT3_CC1 | 0x40380198 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT3_CC1_BUFF | 0x4038019C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT3_PERIOD | 0x403801A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT3_PERIOD_BUFF | 0x403801A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT3_DT | 0x403801B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT3_TR_CMD | 0x403801C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT3_TR_IN_SEL0 | 0x403801C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT3_TR_IN_SEL1 | 0x403801C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT3_TR_IN_EDGE_SEL | 0x403801CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT3_TR_PWM_CTRL | 0x403801D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT3_TR_OUT_SEL | 0x403801D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT3_INTR | 0x403801F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT3_INTR_SET | 0x403801F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT3_INTR_MASK | 0x403801F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT3_INTR_MASKED | 0x403801FC | FULL | Interrupt masked request register |

28.1.5 CNT 4

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT4_CTRL | 0x40380200 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT4_STATUS | 0x40380204 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT4_COUNTER | 0x40380208 | FULL | Counter count register |
| TCPWM0_GRP0_CNT4_CC0 | 0x40380210 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT4_CC0_BUFF | 0x40380214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT4_CC1 | 0x40380218 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT4_CC1_BUFF | 0x4038021C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT4_PERIOD | 0x40380220 | FULL | Counter period register |
| TCPWM0_GRP0_CNT4_PERIOD_BUFF | 0x40380224 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT4_DT | 0x40380230 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT4_TR_CMD | 0x40380240 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT4_TR_IN_SEL0 | 0x40380244 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT4_TR_IN_SEL1 | 0x40380248 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT4_TR_IN_EDGE_SEL | 0x4038024C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT4_TR_PWM_CTRL | 0x40380250 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT4_TR_OUT_SEL | 0x40380254 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT4_INTR | 0x40380270 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT4_INTR_SET | 0x40380274 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT4_INTR_MASK | 0x40380278 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT4_INTR_MASKED | 0x4038027C | FULL | Interrupt masked request register |

28.1.6 CNT 5

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT5_CTRL | 0x40380280 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT5_STATUS | 0x40380284 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT5_COUNTER | 0x40380288 | FULL | Counter count register |
| TCPWM0_GRP0_CNT5_CC0 | 0x40380290 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT5_CC0_BUFF | 0x40380294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT5_CC1 | 0x40380298 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT5_CC1_BUFF | 0x4038029C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT5_PERIOD | 0x403802A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT5_PERIOD_BUFF | 0x403802A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT5_DT | 0x403802B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT5_TR_CMD | 0x403802C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT5_TR_IN_SEL0 | 0x403802C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT5_TR_IN_SEL1 | 0x403802C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT5_TR_IN_EDGE_SEL | 0x403802CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT5_TR_PWM_CTRL | 0x403802D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT5_TR_OUT_SEL | 0x403802D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT5_INTR | 0x403802F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT5_INTR_SET | 0x403802F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT5_INTR_MASK | 0x403802F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT5_INTR_MASKED | 0x403802FC | FULL | Interrupt masked request register |

28.1.7 CNT 6

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT6_CTRL | 0x40380300 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT6_STATUS | 0x40380304 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT6_COUNTER | 0x40380308 | FULL | Counter count register |
| TCPWM0_GRP0_CNT6_CC0 | 0x40380310 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT6_CC0_BUFF | 0x40380314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT6_CC1 | 0x40380318 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT6_CC1_BUFF | 0x4038031C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT6_PERIOD | 0x40380320 | FULL | Counter period register |
| TCPWM0_GRP0_CNT6_PERIOD_BUFF | 0x40380324 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT6_DT | 0x40380330 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT6_TR_CMD | 0x40380340 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT6_TR_IN_SEL0 | 0x40380344 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT6_TR_IN_SEL1 | 0x40380348 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT6_TR_IN_EDGE_SEL | 0x4038034C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT6_TR_PWM_CTRL | 0x40380350 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT6_TR_OUT_SEL | 0x40380354 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT6_INTR | 0x40380370 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT6_INTR_SET | 0x40380374 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT6_INTR_MASK | 0x40380378 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT6_INTR_MASKED | 0x4038037C | FULL | Interrupt masked request register |

28.1.8 CNT 7

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT7_CTRL | 0x40380380 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT7_STATUS | 0x40380384 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT7_COUNTER | 0x40380388 | FULL | Counter count register |
| TCPWM0_GRP0_CNT7_CC0 | 0x40380390 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT7_CC0_BUFF | 0x40380394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT7_CC1 | 0x40380398 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT7_CC1_BUFF | 0x4038039C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT7_PERIOD | 0x403803A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT7_PERIOD_BUFF | 0x403803A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT7_DT | 0x403803B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT7_TR_CMD | 0x403803C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT7_TR_IN_SEL0 | 0x403803C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT7_TR_IN_SEL1 | 0x403803C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT7_TR_IN_EDGE_SEL | 0x403803CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT7_TR_PWM_CTRL | 0x403803D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT7_TR_OUT_SEL | 0x403803D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT7_INTR | 0x403803F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT7_INTR_SET | 0x403803F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT7_INTR_MASK | 0x403803F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT7_INTR_MASKED | 0x403803FC | FULL | Interrupt masked request register |

28.1.9 CNT 8

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|--|
| TCPWM0_GRP0_CNT8_CTRL | 0x40380400 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT8_STATUS | 0x40380404 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT8_COUNTER | 0x40380408 | FULL | Counter count register |
| TCPWM0_GRP0_CNT8_CC0 | 0x40380410 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT8_CC0_BUFF | 0x40380414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT8_CC1 | 0x40380418 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT8_CC1_BUFF | 0x4038041C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT8_PERIOD | 0x40380420 | FULL | Counter period register |
| TCPWM0_GRP0_CNT8_PERIOD_BUFF | 0x40380424 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT8_DT | 0x40380430 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT8_TR_CMD | 0x40380440 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT8_TR_IN_SEL0 | 0x40380444 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT8_TR_IN_SEL1 | 0x40380448 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT8_TR_IN_EDGE_SEL | 0x4038044C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT8_TR_PWM_CTRL | 0x40380450 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT8_TR_OUT_SEL | 0x40380454 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT8_INTR | 0x40380470 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT8_INTR_SET | 0x40380474 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT8_INTR_MASK | 0x40380478 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT8_INTR_MASKED | 0x4038047C | FULL | Interrupt masked request register |

28.1.10 CNT 9

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT9_CTRL | 0x40380480 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT9_STATUS | 0x40380484 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT9_COUNTER | 0x40380488 | FULL | Counter count register |
| TCPWM0_GRP0_CNT9_CC0 | 0x40380490 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT9_CC0_BUFF | 0x40380494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT9_CC1 | 0x40380498 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT9_CC1_BUFF | 0x4038049C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT9_PERIOD | 0x403804A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT9_PERIOD_BUFF | 0x403804A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT9_DT | 0x403804B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT9_TR_CMD | 0x403804C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT9_TR_IN_SEL0 | 0x403804C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT9_TR_IN_SEL1 | 0x403804C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT9_TR_IN_EDGE_SEL | 0x403804CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT9_TR_PWM_CTRL | 0x403804D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT9_TR_OUT_SEL | 0x403804D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT9_INTR | 0x403804F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT9_INTR_SET | 0x403804F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT9_INTR_MASK | 0x403804F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT9_INTR_MASKED | 0x403804FC | FULL | Interrupt masked request register |

28.1.11 CNT 10

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT10_CTRL | 0x40380500 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT10_STATUS | 0x40380504 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT10_COUNTER | 0x40380508 | FULL | Counter count register |
| TCPWM0_GRP0_CNT10_CC0 | 0x40380510 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT10_CC0_BUFF | 0x40380514 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT10_CC1 | 0x40380518 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT10_CC1_BUFF | 0x4038051C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT10_PERIOD | 0x40380520 | FULL | Counter period register |
| TCPWM0_GRP0_CNT10_PERIOD_BUFF | 0x40380524 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT10_DT | 0x40380530 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT10_TR_CMD | 0x40380540 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT10_TR_IN_SEL0 | 0x40380544 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT10_TR_IN_SEL1 | 0x40380548 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT10_TR_IN_EDGE_SEL | 0x4038054C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT10_TR_PWM_CTRL | 0x40380550 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT10_TR_OUT_SEL | 0x40380554 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT10_INTR | 0x40380570 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT10_INTR_SET | 0x40380574 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT10_INTR_MASK | 0x40380578 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT10_INTR_MASKED | 0x4038057C | FULL | Interrupt masked request register |

28.1.12 CNT 11

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT11_CTRL | 0x40380580 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT11_STATUS | 0x40380584 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT11_COUNTER | 0x40380588 | FULL | Counter count register |
| TCPWM0_GRP0_CNT11_CC0 | 0x40380590 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT11_CC0_BUFF | 0x40380594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT11_CC1 | 0x40380598 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT11_CC1_BUFF | 0x4038059C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT11_PERIOD | 0x403805A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT11_PERIOD_BUFF | 0x403805A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT11_DT | 0x403805B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT11_TR_CMD | 0x403805C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT11_TR_IN_SEL0 | 0x403805C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT11_TR_IN_SEL1 | 0x403805C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT11_TR_IN_EDGE_SEL | 0x403805CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT11_TR_PWM_CTRL | 0x403805D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT11_TR_OUT_SEL | 0x403805D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT11_INTR | 0x403805F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT11_INTR_SET | 0x403805F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT11_INTR_MASK | 0x403805F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT11_INTR_MASKED | 0x403805FC | FULL | Interrupt masked request register |

28.1.13 CNT 12

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT12_CTRL | 0x40380600 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT12_STATUS | 0x40380604 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT12_COUNTER | 0x40380608 | FULL | Counter count register |
| TCPWM0_GRP0_CNT12_CC0 | 0x40380610 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT12_CC0_BUFF | 0x40380614 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT12_CC1 | 0x40380618 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT12_CC1_BUFF | 0x4038061C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT12_PERIOD | 0x40380620 | FULL | Counter period register |
| TCPWM0_GRP0_CNT12_PERIOD_BUFF | 0x40380624 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT12_DT | 0x40380630 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT12_TR_CMD | 0x40380640 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT12_TR_IN_SEL0 | 0x40380644 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT12_TR_IN_SEL1 | 0x40380648 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT12_TR_IN_EDGE_SEL | 0x4038064C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT12_TR_PWM_CTRL | 0x40380650 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT12_TR_OUT_SEL | 0x40380654 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT12_INTR | 0x40380670 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT12_INTR_SET | 0x40380674 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT12_INTR_MASK | 0x40380678 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT12_INTR_MASKED | 0x4038067C | FULL | Interrupt masked request register |

28.1.14 CNT 13

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT13_CTRL | 0x40380680 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT13_STATUS | 0x40380684 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT13_COUNTER | 0x40380688 | FULL | Counter count register |
| TCPWM0_GRP0_CNT13_CC0 | 0x40380690 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT13_CC0_BUFF | 0x40380694 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT13_CC1 | 0x40380698 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT13_CC1_BUFF | 0x4038069C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT13_PERIOD | 0x403806A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT13_PERIOD_BUFF | 0x403806A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT13_DT | 0x403806B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT13_TR_CMD | 0x403806C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT13_TR_IN_SEL0 | 0x403806C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT13_TR_IN_SEL1 | 0x403806C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT13_TR_IN_EDGE_SEL | 0x403806CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT13_TR_PWM_CTRL | 0x403806D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT13_TR_OUT_SEL | 0x403806D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT13_INTR | 0x403806F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT13_INTR_SET | 0x403806F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT13_INTR_MASK | 0x403806F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT13_INTR_MASKED | 0x403806FC | FULL | Interrupt masked request register |

28.1.15 CNT 14

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT14_CTRL | 0x40380700 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT14_STATUS | 0x40380704 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT14_COUNTER | 0x40380708 | FULL | Counter count register |
| TCPWM0_GRP0_CNT14_CC0 | 0x40380710 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT14_CC0_BUFF | 0x40380714 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT14_CC1 | 0x40380718 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT14_CC1_BUFF | 0x4038071C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT14_PERIOD | 0x40380720 | FULL | Counter period register |
| TCPWM0_GRP0_CNT14_PERIOD_BUFF | 0x40380724 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT14_DT | 0x40380730 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT14_TR_CMD | 0x40380740 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT14_TR_IN_SEL0 | 0x40380744 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT14_TR_IN_SEL1 | 0x40380748 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT14_TR_IN_EDGE_SEL | 0x4038074C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT14_TR_PWM_CTRL | 0x40380750 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT14_TR_OUT_SEL | 0x40380754 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT14_INTR | 0x40380770 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT14_INTR_SET | 0x40380774 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT14_INTR_MASK | 0x40380778 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT14_INTR_MASKED | 0x4038077C | FULL | Interrupt masked request register |

28.1.16 CNT 15

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT15_CTRL | 0x40380780 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT15_STATUS | 0x40380784 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT15_COUNTER | 0x40380788 | FULL | Counter count register |
| TCPWM0_GRP0_CNT15_CC0 | 0x40380790 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT15_CC0_BUFF | 0x40380794 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT15_CC1 | 0x40380798 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT15_CC1_BUFF | 0x4038079C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT15_PERIOD | 0x403807A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT15_PERIOD_BUFF | 0x403807A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT15_DT | 0x403807B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT15_TR_CMD | 0x403807C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT15_TR_IN_SEL0 | 0x403807C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT15_TR_IN_SEL1 | 0x403807C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT15_TR_IN_EDGE_SEL | 0x403807CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT15_TR_PWM_CTRL | 0x403807D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT15_TR_OUT_SEL | 0x403807D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT15_INTR | 0x403807F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT15_INTR_SET | 0x403807F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT15_INTR_MASK | 0x403807F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT15_INTR_MASKED | 0x403807FC | FULL | Interrupt masked request register |

28.1.17 CNT 16

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT16_CTRL | 0x40380800 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT16_STATUS | 0x40380804 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT16_COUNTER | 0x40380808 | FULL | Counter count register |
| TCPWM0_GRP0_CNT16_CC0 | 0x40380810 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT16_CC0_BUFF | 0x40380814 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT16_CC1 | 0x40380818 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT16_CC1_BUFF | 0x4038081C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT16_PERIOD | 0x40380820 | FULL | Counter period register |
| TCPWM0_GRP0_CNT16_PERIOD_BUFF | 0x40380824 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT16_DT | 0x40380830 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT16_TR_CMD | 0x40380840 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT16_TR_IN_SEL0 | 0x40380844 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT16_TR_IN_SEL1 | 0x40380848 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT16_TR_IN_EDGE_SEL | 0x4038084C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT16_TR_PWM_CTRL | 0x40380850 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT16_TR_OUT_SEL | 0x40380854 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT16_INTR | 0x40380870 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP0_CNT16_INTR_SET | 0x40380874 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT16_INTR_MASK | 0x40380878 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT16_INTR_MASKED | 0x4038087C | FULL | Interrupt masked request register |

28.1.18 CNT 17

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT17_CTRL | 0x40380880 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT17_STATUS | 0x40380884 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT17_COUNTER | 0x40380888 | FULL | Counter count register |
| TCPWM0_GRP0_CNT17_CC0 | 0x40380890 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT17_CC0_BUFF | 0x40380894 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT17_CC1 | 0x40380898 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT17_CC1_BUFF | 0x4038089C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT17_PERIOD | 0x403808A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT17_PERIOD_BUFF | 0x403808A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT17_DT | 0x403808B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT17_TR_CMD | 0x403808C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT17_TR_IN_SEL0 | 0x403808C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT17_TR_IN_SEL1 | 0x403808C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT17_TR_IN_EDGE_SEL | 0x403808CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT17_TR_PWM_CTRL | 0x403808D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT17_TR_OUT_SEL | 0x403808D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT17_INTR | 0x403808F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT17_INTR_SET | 0x403808F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT17_INTR_MASK | 0x403808F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT17_INTR_MASKED | 0x403808FC | FULL | Interrupt masked request register |

28.1.19 CNT 18

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT18_CTRL | 0x40380900 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT18_STATUS | 0x40380904 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT18_COUNTER | 0x40380908 | FULL | Counter count register |
| TCPWM0_GRP0_CNT18_CC0 | 0x40380910 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT18_CC0_BUFF | 0x40380914 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT18_CC1 | 0x40380918 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT18_CC1_BUFF | 0x4038091C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT18_PERIOD | 0x40380920 | FULL | Counter period register |
| TCPWM0_GRP0_CNT18_PERIOD_BUFF | 0x40380924 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT18_DT | 0x40380930 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT18_TR_CMD | 0x40380940 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT18_TR_IN_SEL0 | 0x40380944 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT18_TR_IN_SEL1 | 0x40380948 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT18_TR_IN_EDGE_SEL | 0x4038094C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT18_TR_PWM_CTRL | 0x40380950 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT18_TR_OUT_SEL | 0x40380954 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT18_INTR | 0x40380970 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT18_INTR_SET | 0x40380974 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT18_INTR_MASK | 0x40380978 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT18_INTR_MASKED | 0x4038097C | FULL | Interrupt masked request register |

28.1.20 CNT 19

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT19_CTRL | 0x40380980 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT19_STATUS | 0x40380984 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT19_COUNTER | 0x40380988 | FULL | Counter count register |
| TCPWM0_GRP0_CNT19_CC0 | 0x40380990 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT19_CC0_BUFF | 0x40380994 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT19_CC1 | 0x40380998 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT19_CC1_BUFF | 0x4038099C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT19_PERIOD | 0x403809A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT19_PERIOD_BUFF | 0x403809A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT19_DT | 0x403809B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT19_TR_CMD | 0x403809C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT19_TR_IN_SEL0 | 0x403809C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT19_TR_IN_SEL1 | 0x403809C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT19_TR_IN_EDGE_SEL | 0x403809CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT19_TR_PWM_CTRL | 0x403809D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT19_TR_OUT_SEL | 0x403809D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT19_INTR | 0x403809F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT19_INTR_SET | 0x403809F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT19_INTR_MASK | 0x403809F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT19_INTR_MASKED | 0x403809FC | FULL | Interrupt masked request register |

28.1.21 CNT 20

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT20_CTRL | 0x40380A00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT20_STATUS | 0x40380A04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT20_COUNTER | 0x40380A08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT20_CC0 | 0x40380A10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT20_CC0_BUFF | 0x40380A14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT20_CC1 | 0x40380A18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT20_CC1_BUFF | 0x40380A1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT20_PERIOD | 0x40380A20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT20_PERIOD_BUFF | 0x40380A24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT20_DT | 0x40380A30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT20_TR_CMD | 0x40380A40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT20_TR_IN_SEL0 | 0x40380A44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT20_TR_IN_SEL1 | 0x40380A48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT20_TR_IN_EDGE_SEL | 0x40380A4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT20_TR_PWM_CTRL | 0x40380A50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT20_TR_OUT_SEL | 0x40380A54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT20_INTR | 0x40380A70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT20_INTR_SET | 0x40380A74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT20_INTR_MASK | 0x40380A78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT20_INTR_MASKED | 0x40380A7C | FULL | Interrupt masked request register |

28.1.22 CNT 21

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT21_CTRL | 0x40380A80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT21_STATUS | 0x40380A84 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT21_COUNTER | 0x40380A88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT21_CC0 | 0x40380A90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT21_CC0_BUFF | 0x40380A94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT21_CC1 | 0x40380A98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT21_CC1_BUFF | 0x40380A9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT21_PERIOD | 0x40380AA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT21_PERIOD_BUFF | 0x40380AA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT21_DT | 0x40380AB0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT21_TR_CMD | 0x40380AC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT21_TR_IN_SEL0 | 0x40380AC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT21_TR_IN_SEL1 | 0x40380AC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT21_TR_IN_EDGE_SEL | 0x40380ACC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT21_TR_PWM_CTRL | 0x40380AD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT21_TR_OUT_SEL | 0x40380AD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT21_INTR | 0x40380AF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT21_INTR_SET | 0x40380AF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT21_INTR_MASK | 0x40380AF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT21_INTR_MASKED | 0x40380AFC | FULL | Interrupt masked request register |

28.1.23 CNT 22

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT22_CTRL | 0x40380B00 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT22_STATUS | 0x40380B04 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT22_COUNTER | 0x40380B08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT22_CC0 | 0x40380B10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT22_CC0_BUFF | 0x40380B14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT22_CC1 | 0x40380B18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT22_CC1_BUFF | 0x40380B1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT22_PERIOD | 0x40380B20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT22_PERIOD_BUFF | 0x40380B24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT22_DT | 0x40380B30 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT22_TR_CMD | 0x40380B40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT22_TR_IN_SEL0 | 0x40380B44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT22_TR_IN_SEL1 | 0x40380B48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT22_TR_IN_EDGE_SEL | 0x40380B4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT22_TR_PWM_CTRL | 0x40380B50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT22_TR_OUT_SEL | 0x40380B54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT22_INTR | 0x40380B70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT22_INTR_SET | 0x40380B74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT22_INTR_MASK | 0x40380B78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT22_INTR_MASKED | 0x40380B7C | FULL | Interrupt masked request register |

28.1.24 CNT 23

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT23_CTRL | 0x40380B80 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT23_STATUS | 0x40380B84 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT23_COUNTER | 0x40380B88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT23_CC0 | 0x40380B90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT23_CC0_BUFF | 0x40380B94 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT23_CC1 | 0x40380B98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT23_CC1_BUFF | 0x40380B9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT23_PERIOD | 0x40380BA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT23_PERIOD_BUFF | 0x40380BA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT23_DT | 0x40380BB0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT23_TR_CMD | 0x40380BC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT23_TR_IN_SEL0 | 0x40380BC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT23_TR_IN_SEL1 | 0x40380BC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT23_TR_IN_EDGE_SEL | 0x40380BCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT23_TR_PWM_CTRL | 0x40380BD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT23_TR_OUT_SEL | 0x40380BD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT23_INTR | 0x40380BF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT23_INTR_SET | 0x40380BF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT23_INTR_MASK | 0x40380BF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT23_INTR_MASKED | 0x40380BFC | FULL | Interrupt masked request register |

28.1.25 CNT 24

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT24_CTRL | 0x40380C00 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT24_STATUS | 0x40380C04 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT24_COUNTER | 0x40380C08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT24_CC0 | 0x40380C10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT24_CC0_BUFF | 0x40380C14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT24_CC1 | 0x40380C18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT24_CC1_BUFF | 0x40380C1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT24_PERIOD | 0x40380C20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT24_PERIOD_BUFF | 0x40380C24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT24_DT | 0x40380C30 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT24_TR_CMD | 0x40380C40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT24_TR_IN_SEL0 | 0x40380C44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT24_TR_IN_SEL1 | 0x40380C48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT24_TR_IN_EDGE_SEL | 0x40380C4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT24_TR_PWM_CTRL | 0x40380C50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT24_TR_OUT_SEL | 0x40380C54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT24_INTR | 0x40380C70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT24_INTR_SET | 0x40380C74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT24_INTR_MASK | 0x40380C78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT24_INTR_MASKED | 0x40380C7C | FULL | Interrupt masked request register |

28.1.26 CNT 25

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT25_CTRL | 0x40380C80 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT25_STATUS | 0x40380C84 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT25_COUNTER | 0x40380C88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT25_CC0 | 0x40380C90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT25_CC0_BUFF | 0x40380C94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT25_CC1 | 0x40380C98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT25_CC1_BUFF | 0x40380C9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT25_PERIOD | 0x40380CA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT25_PERIOD_BUFF | 0x40380CA4 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT25_DT | 0x40380CB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT25_TR_CMD | 0x40380CC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT25_TR_IN_SEL0 | 0x40380CC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT25_TR_IN_SEL1 | 0x40380CC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT25_TR_IN_EDGE_SEL | 0x40380CCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT25_TR_PWM_CTRL | 0x40380CD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT25_TR_OUT_SEL | 0x40380CD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT25_INTR | 0x40380CF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT25_INTR_SET | 0x40380CF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT25_INTR_MASK | 0x40380CF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT25_INTR_MASKED | 0x40380CFC | FULL | Interrupt masked request register |

28.1.27 CNT 26

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT26_CTRL | 0x40380D00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT26_STATUS | 0x40380D04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT26_COUNTER | 0x40380D08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT26_CC0 | 0x40380D10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT26_CC0_BUFF | 0x40380D14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT26_CC1 | 0x40380D18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT26_CC1_BUFF | 0x40380D1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT26_PERIOD | 0x40380D20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT26_PERIOD_BUFF | 0x40380D24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT26_DT | 0x40380D30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT26_TR_CMD | 0x40380D40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT26_TR_IN_SEL0 | 0x40380D44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT26_TR_IN_SEL1 | 0x40380D48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT26_TR_IN_EDGE_SEL | 0x40380D4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT26_TR_PWM_CTRL | 0x40380D50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT26_TR_OUT_SEL | 0x40380D54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT26_INTR | 0x40380D70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT26_INTR_SET | 0x40380D74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT26_INTR_MASK | 0x40380D78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT26_INTR_MASKED | 0x40380D7C | FULL | Interrupt masked request register |

28.1.28 CNT 27

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT27_CTRL | 0x40380D80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT27_STATUS | 0x40380D84 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT27_COUNTER | 0x40380D88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT27_CC0 | 0x40380D90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT27_CC0_BUFF | 0x40380D94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT27_CC1 | 0x40380D98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT27_CC1_BUFF | 0x40380D9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT27_PERIOD | 0x40380DA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT27_PERIOD_BUFF | 0x40380DA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT27_DT | 0x40380DB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT27_TR_CMD | 0x40380DC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT27_TR_IN_SEL0 | 0x40380DC4 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT27_TR_IN_SEL1 | 0x40380DC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT27_TR_IN_EDGE_SEL | 0x40380DCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT27_TR_PWM_CTRL | 0x40380DD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT27_TR_OUT_SEL | 0x40380DD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT27_INTR | 0x40380DF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT27_INTR_SET | 0x40380DF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT27_INTR_MASK | 0x40380DF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT27_INTR_MASKED | 0x40380DFC | FULL | Interrupt masked request register |

28.1.29 CNT 28

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT28_CTRL | 0x40380E00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT28_STATUS | 0x40380E04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT28_COUNTER | 0x40380E08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT28_CC0 | 0x40380E10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT28_CC0_BUFF | 0x40380E14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT28_CC1 | 0x40380E18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT28_CC1_BUFF | 0x40380E1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT28_PERIOD | 0x40380E20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT28_PERIOD_BUFF | 0x40380E24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT28_DT | 0x40380E30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT28_TR_CMD | 0x40380E40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT28_TR_IN_SEL0 | 0x40380E44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT28_TR_IN_SEL1 | 0x40380E48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT28_TR_IN_EDGE_SEL | 0x40380E4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT28_TR_PWM_CTRL | 0x40380E50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT28_TR_OUT_SEL | 0x40380E54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT28_INTR | 0x40380E70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT28_INTR_SET | 0x40380E74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT28_INTR_MASK | 0x40380E78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT28_INTR_MASKED | 0x40380E7C | FULL | Interrupt masked request register |

28.1.30 CNT 29

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT29_CTRL | 0x40380E80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT29_STATUS | 0x40380E84 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT29_COUNTER | 0x40380E88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT29_CC0 | 0x40380E90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT29_CC0_BUFF | 0x40380E94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT29_CC1 | 0x40380E98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT29_CC1_BUFF | 0x40380E9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT29_PERIOD | 0x40380EA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT29_PERIOD_BUFF | 0x40380EA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT29_DT | 0x40380EB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT29_TR_CMD | 0x40380EC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT29_TR_IN_SEL0 | 0x40380EC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT29_TR_IN_SEL1 | 0x40380EC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT29_TR_IN_EDGE_SEL | 0x40380ECC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT29_TR_PWM_CTRL | 0x40380ED0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT29_TR_OUT_SEL | 0x40380ED4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT29_INTR | 0x40380EF0 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP0_CNT29_INTR_SET | 0x40380EF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT29_INTR_MASK | 0x40380EF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT29_INTR_MASKED | 0x40380EFC | FULL | Interrupt masked request register |

28.1.31 CNT 30

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT30_CTRL | 0x40380F00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT30_STATUS | 0x40380F04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT30_COUNTER | 0x40380F08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT30_CC0 | 0x40380F10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT30_CC0_BUFF | 0x40380F14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT30_CC1 | 0x40380F18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT30_CC1_BUFF | 0x40380F1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT30_PERIOD | 0x40380F20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT30_PERIOD_BUFF | 0x40380F24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT30_DT | 0x40380F30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT30_TR_CMD | 0x40380F40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT30_TR_IN_SEL0 | 0x40380F44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT30_TR_IN_SEL1 | 0x40380F48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT30_TR_IN_EDGE_SEL | 0x40380F4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT30_TR_PWM_CTRL | 0x40380F50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT30_TR_OUT_SEL | 0x40380F54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT30_INTR | 0x40380F70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT30_INTR_SET | 0x40380F74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT30_INTR_MASK | 0x40380F78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT30_INTR_MASKED | 0x40380F7C | FULL | Interrupt masked request register |

28.1.32 CNT 31

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT31_CTRL | 0x40380F80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT31_STATUS | 0x40380F84 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT31_COUNTER | 0x40380F88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT31_CC0 | 0x40380F90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT31_CC0_BUFF | 0x40380F94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT31_CC1 | 0x40380F98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT31_CC1_BUFF | 0x40380F9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT31_PERIOD | 0x40380FA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT31_PERIOD_BUFF | 0x40380FA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT31_DT | 0x40380FB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT31_TR_CMD | 0x40380FC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT31_TR_IN_SEL0 | 0x40380FC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT31_TR_IN_SEL1 | 0x40380FC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT31_TR_IN_EDGE_SEL | 0x40380FCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT31_TR_PWM_CTRL | 0x40380FD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT31_TR_OUT_SEL | 0x40380FD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT31_INTR | 0x40380FF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT31_INTR_SET | 0x40380FF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT31_INTR_MASK | 0x40380FF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT31_INTR_MASKED | 0x40380FFC | FULL | Interrupt masked request register |

28.1.33 CNT 32

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT32_CTRL | 0x40381000 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT32_STATUS | 0x40381004 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT32_COUNTER | 0x40381008 | FULL | Counter count register |
| TCPWM0_GRP0_CNT32_CC0 | 0x40381010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT32_CC0_BUFF | 0x40381014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT32_CC1 | 0x40381018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT32_CC1_BUFF | 0x4038101C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT32_PERIOD | 0x40381020 | FULL | Counter period register |
| TCPWM0_GRP0_CNT32_PERIOD_BUFF | 0x40381024 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT32_DT | 0x40381030 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT32_TR_CMD | 0x40381040 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT32_TR_IN_SEL0 | 0x40381044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT32_TR_IN_SEL1 | 0x40381048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT32_TR_IN_EDGE_SEL | 0x4038104C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT32_TR_PWM_CTRL | 0x40381050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT32_TR_OUT_SEL | 0x40381054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT32_INTR | 0x40381070 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT32_INTR_SET | 0x40381074 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT32_INTR_MASK | 0x40381078 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT32_INTR_MASKED | 0x4038107C | FULL | Interrupt masked request register |

28.1.34 CNT 33

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT33_CTRL | 0x40381080 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT33_STATUS | 0x40381084 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT33_COUNTER | 0x40381088 | FULL | Counter count register |
| TCPWM0_GRP0_CNT33_CC0 | 0x40381090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT33_CC0_BUFF | 0x40381094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT33_CC1 | 0x40381098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT33_CC1_BUFF | 0x4038109C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT33_PERIOD | 0x403810A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT33_PERIOD_BUFF | 0x403810A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT33_DT | 0x403810B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT33_TR_CMD | 0x403810C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT33_TR_IN_SEL0 | 0x403810C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT33_TR_IN_SEL1 | 0x403810C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT33_TR_IN_EDGE_SEL | 0x403810CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT33_TR_PWM_CTRL | 0x403810D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT33_TR_OUT_SEL | 0x403810D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT33_INTR | 0x403810F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT33_INTR_SET | 0x403810F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT33_INTR_MASK | 0x403810F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT33_INTR_MASKED | 0x403810FC | FULL | Interrupt masked request register |

28.1.35 CNT 34

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT34_CTRL | 0x40381100 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT34_STATUS | 0x40381104 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT34_COUNTER | 0x40381108 | FULL | Counter count register |
| TCPWM0_GRP0_CNT34_CC0 | 0x40381110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT34_CC0_BUFF | 0x40381114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT34_CC1 | 0x40381118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT34_CC1_BUFF | 0x4038111C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT34_PERIOD | 0x40381120 | FULL | Counter period register |
| TCPWM0_GRP0_CNT34_PERIOD_BUFF | 0x40381124 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT34_DT | 0x40381130 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT34_TR_CMD | 0x40381140 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT34_TR_IN_SEL0 | 0x40381144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT34_TR_IN_SEL1 | 0x40381148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT34_TR_IN_EDGE_SEL | 0x4038114C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT34_TR_PWM_CTRL | 0x40381150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT34_TR_OUT_SEL | 0x40381154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT34_INTR | 0x40381170 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT34_INTR_SET | 0x40381174 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT34_INTR_MASK | 0x40381178 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT34_INTR_MASKED | 0x4038117C | FULL | Interrupt masked request register |

28.1.36 CNT 35

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT35_CTRL | 0x40381180 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT35_STATUS | 0x40381184 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT35_COUNTER | 0x40381188 | FULL | Counter count register |
| TCPWM0_GRP0_CNT35_CC0 | 0x40381190 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT35_CC0_BUFF | 0x40381194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT35_CC1 | 0x40381198 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT35_CC1_BUFF | 0x4038119C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT35_PERIOD | 0x403811A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT35_PERIOD_BUFF | 0x403811A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT35_DT | 0x403811B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT35_TR_CMD | 0x403811C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT35_TR_IN_SEL0 | 0x403811C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT35_TR_IN_SEL1 | 0x403811C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT35_TR_IN_EDGE_SEL | 0x403811CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT35_TR_PWM_CTRL | 0x403811D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT35_TR_OUT_SEL | 0x403811D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT35_INTR | 0x403811F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT35_INTR_SET | 0x403811F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT35_INTR_MASK | 0x403811F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT35_INTR_MASKED | 0x403811FC | FULL | Interrupt masked request register |

28.1.37 CNT 36

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT36_CTRL | 0x40381200 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT36_STATUS | 0x40381204 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT36_COUNTER | 0x40381208 | FULL | Counter count register |
| TCPWM0_GRP0_CNT36_CC0 | 0x40381210 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT36_CC0_BUFF | 0x40381214 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT36_CC1 | 0x40381218 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT36_CC1_BUFF | 0x4038121C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT36_PERIOD | 0x40381220 | FULL | Counter period register |
| TCPWM0_GRP0_CNT36_PERIOD_BUFF | 0x40381224 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT36_DT | 0x40381230 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT36_TR_CMD | 0x40381240 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT36_TR_IN_SEL0 | 0x40381244 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT36_TR_IN_SEL1 | 0x40381248 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT36_TR_IN_EDGE_SEL | 0x4038124C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT36_TR_PWM_CTRL | 0x40381250 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT36_TR_OUT_SEL | 0x40381254 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT36_INTR | 0x40381270 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT36_INTR_SET | 0x40381274 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT36_INTR_MASK | 0x40381278 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT36_INTR_MASKED | 0x4038127C | FULL | Interrupt masked request register |

28.1.38 CNT 37

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT37_CTRL | 0x40381280 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT37_STATUS | 0x40381284 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT37_COUNTER | 0x40381288 | FULL | Counter count register |
| TCPWM0_GRP0_CNT37_CC0 | 0x40381290 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT37_CC0_BUFF | 0x40381294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT37_CC1 | 0x40381298 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT37_CC1_BUFF | 0x4038129C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT37_PERIOD | 0x403812A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT37_PERIOD_BUFF | 0x403812A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT37_DT | 0x403812B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT37_TR_CMD | 0x403812C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT37_TR_IN_SEL0 | 0x403812C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT37_TR_IN_SEL1 | 0x403812C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT37_TR_IN_EDGE_SEL | 0x403812CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT37_TR_PWM_CTRL | 0x403812D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT37_TR_OUT_SEL | 0x403812D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT37_INTR | 0x403812F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT37_INTR_SET | 0x403812F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT37_INTR_MASK | 0x403812F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT37_INTR_MASKED | 0x403812FC | FULL | Interrupt masked request register |

28.1.39 CNT 38

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT38_CTRL | 0x40381300 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT38_STATUS | 0x40381304 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT38_COUNTER | 0x40381308 | FULL | Counter count register |
| TCPWM0_GRP0_CNT38_CC0 | 0x40381310 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT38_CC0_BUFF | 0x40381314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT38_CC1 | 0x40381318 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT38_CC1_BUFF | 0x4038131C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT38_PERIOD | 0x40381320 | FULL | Counter period register |
| TCPWM0_GRP0_CNT38_PERIOD_BUFF | 0x40381324 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT38_DT | 0x40381330 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT38_TR_CMD | 0x40381340 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT38_TR_IN_SEL0 | 0x40381344 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT38_TR_IN_SEL1 | 0x40381348 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT38_TR_IN_EDGE_SEL | 0x4038134C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT38_TR_PWM_CTRL | 0x40381350 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT38_TR_OUT_SEL | 0x40381354 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT38_INTR | 0x40381370 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT38_INTR_SET | 0x40381374 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT38_INTR_MASK | 0x40381378 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT38_INTR_MASKED | 0x4038137C | FULL | Interrupt masked request register |

28.1.40 CNT 39

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT39_CTRL | 0x40381380 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT39_STATUS | 0x40381384 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT39_COUNTER | 0x40381388 | FULL | Counter count register |
| TCPWM0_GRP0_CNT39_CC0 | 0x40381390 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT39_CC0_BUFF | 0x40381394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT39_CC1 | 0x40381398 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT39_CC1_BUFF | 0x4038139C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT39_PERIOD | 0x403813A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT39_PERIOD_BUFF | 0x403813A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT39_DT | 0x403813B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT39_TR_CMD | 0x403813C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT39_TR_IN_SEL0 | 0x403813C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT39_TR_IN_SEL1 | 0x403813C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT39_TR_IN_EDGE_SEL | 0x403813CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT39_TR_PWM_CTRL | 0x403813D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT39_TR_OUT_SEL | 0x403813D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT39_INTR | 0x403813F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT39_INTR_SET | 0x403813F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT39_INTR_MASK | 0x403813F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT39_INTR_MASKED | 0x403813FC | FULL | Interrupt masked request register |

28.1.41 CNT 40

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT40_CTRL | 0x40381400 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT40_STATUS | 0x40381404 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT40_COUNTER | 0x40381408 | FULL | Counter count register |
| TCPWM0_GRP0_CNT40_CC0 | 0x40381410 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT40_CC0_BUFF | 0x40381414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT40_CC1 | 0x40381418 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT40_CC1_BUFF | 0x4038141C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT40_PERIOD | 0x40381420 | FULL | Counter period register |
| TCPWM0_GRP0_CNT40_PERIOD_BUFF | 0x40381424 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT40_DT | 0x40381430 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT40_TR_CMD | 0x40381440 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT40_TR_IN_SEL0 | 0x40381444 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT40_TR_IN_SEL1 | 0x40381448 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT40_TR_IN_EDGE_SEL | 0x4038144C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT40_TR_PWM_CTRL | 0x40381450 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT40_TR_OUT_SEL | 0x40381454 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT40_INTR | 0x40381470 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT40_INTR_SET | 0x40381474 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT40_INTR_MASK | 0x40381478 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT40_INTR_MASKED | 0x4038147C | FULL | Interrupt masked request register |

28.1.42 CNT 41

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT41_CTRL | 0x40381480 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT41_STATUS | 0x40381484 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT41_COUNTER | 0x40381488 | FULL | Counter count register |
| TCPWM0_GRP0_CNT41_CC0 | 0x40381490 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT41_CC0_BUFF | 0x40381494 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT41_CC1 | 0x40381498 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT41_CC1_BUFF | 0x4038149C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT41_PERIOD | 0x403814A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT41_PERIOD_BUFF | 0x403814A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT41_DT | 0x403814B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT41_TR_CMD | 0x403814C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT41_TR_IN_SEL0 | 0x403814C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT41_TR_IN_SEL1 | 0x403814C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT41_TR_IN_EDGE_SEL | 0x403814CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT41_TR_PWM_CTRL | 0x403814D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT41_TR_OUT_SEL | 0x403814D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT41_INTR | 0x403814F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT41_INTR_SET | 0x403814F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT41_INTR_MASK | 0x403814F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT41_INTR_MASKED | 0x403814FC | FULL | Interrupt masked request register |

28.1.43 CNT 42

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT42_CTRL | 0x40381500 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT42_STATUS | 0x40381504 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT42_COUNTER | 0x40381508 | FULL | Counter count register |
| TCPWM0_GRP0_CNT42_CC0 | 0x40381510 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT42_CC0_BUFF | 0x40381514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT42_CC1 | 0x40381518 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT42_CC1_BUFF | 0x4038151C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT42_PERIOD | 0x40381520 | FULL | Counter period register |
| TCPWM0_GRP0_CNT42_PERIOD_BUFF | 0x40381524 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT42_DT | 0x40381530 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT42_TR_CMD | 0x40381540 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT42_TR_IN_SEL0 | 0x40381544 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT42_TR_IN_SEL1 | 0x40381548 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT42_TR_IN_EDGE_SEL | 0x4038154C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT42_TR_PWM_CTRL | 0x40381550 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT42_TR_OUT_SEL | 0x40381554 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT42_INTR | 0x40381570 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP0_CNT42_INTR_SET | 0x40381574 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT42_INTR_MASK | 0x40381578 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT42_INTR_MASKED | 0x4038157C | FULL | Interrupt masked request register |

28.1.44 CNT 43

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT43_CTRL | 0x40381580 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT43_STATUS | 0x40381584 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT43_COUNTER | 0x40381588 | FULL | Counter count register |
| TCPWM0_GRP0_CNT43_CC0 | 0x40381590 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT43_CC0_BUFF | 0x40381594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT43_CC1 | 0x40381598 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT43_CC1_BUFF | 0x4038159C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT43_PERIOD | 0x403815A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT43_PERIOD_BUFF | 0x403815A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT43_DT | 0x403815B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT43_TR_CMD | 0x403815C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT43_TR_IN_SEL0 | 0x403815C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT43_TR_IN_SEL1 | 0x403815C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT43_TR_IN_EDGE_SEL | 0x403815CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT43_TR_PWM_CTRL | 0x403815D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT43_TR_OUT_SEL | 0x403815D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT43_INTR | 0x403815F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT43_INTR_SET | 0x403815F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT43_INTR_MASK | 0x403815F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT43_INTR_MASKED | 0x403815FC | FULL | Interrupt masked request register |

28.1.45 CNT 44

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT44_CTRL | 0x40381600 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT44_STATUS | 0x40381604 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT44_COUNTER | 0x40381608 | FULL | Counter count register |
| TCPWM0_GRP0_CNT44_CC0 | 0x40381610 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT44_CC0_BUFF | 0x40381614 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT44_CC1 | 0x40381618 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT44_CC1_BUFF | 0x4038161C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT44_PERIOD | 0x40381620 | FULL | Counter period register |
| TCPWM0_GRP0_CNT44_PERIOD_BUFF | 0x40381624 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT44_DT | 0x40381630 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT44_TR_CMD | 0x40381640 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT44_TR_IN_SEL0 | 0x40381644 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT44_TR_IN_SEL1 | 0x40381648 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT44_TR_IN_EDGE_SEL | 0x4038164C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT44_TR_PWM_CTRL | 0x40381650 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT44_TR_OUT_SEL | 0x40381654 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT44_INTR | 0x40381670 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT44_INTR_SET | 0x40381674 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT44_INTR_MASK | 0x40381678 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT44_INTR_MASKED | 0x4038167C | FULL | Interrupt masked request register |

28.1.46 CNT 45

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| TCPWM0_GRP0_CNT45_CTRL | 0x40381680 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT45_STATUS | 0x40381684 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT45_COUNTER | 0x40381688 | FULL | Counter count register |
| TCPWM0_GRP0_CNT45_CC0 | 0x40381690 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT45_CC0_BUFF | 0x40381694 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT45_CC1 | 0x40381698 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT45_CC1_BUFF | 0x4038169C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT45_PERIOD | 0x403816A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT45_PERIOD_BUFF | 0x403816A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT45_DT | 0x403816B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT45_TR_CMD | 0x403816C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT45_TR_IN_SEL0 | 0x403816C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT45_TR_IN_SEL1 | 0x403816C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT45_TR_IN_EDGE_SEL | 0x403816CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT45_TR_PWM_CTRL | 0x403816D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT45_TR_OUT_SEL | 0x403816D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT45_INTR | 0x403816F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT45_INTR_SET | 0x403816F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT45_INTR_MASK | 0x403816F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT45_INTR_MASKED | 0x403816FC | FULL | Interrupt masked request register |

28.1.47 CNT 46

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| TCPWM0_GRP0_CNT46_CTRL | 0x40381700 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT46_STATUS | 0x40381704 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT46_COUNTER | 0x40381708 | FULL | Counter count register |
| TCPWM0_GRP0_CNT46_CC0 | 0x40381710 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT46_CC0_BUFF | 0x40381714 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT46_CC1 | 0x40381718 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT46_CC1_BUFF | 0x4038171C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT46_PERIOD | 0x40381720 | FULL | Counter period register |
| TCPWM0_GRP0_CNT46_PERIOD_BUFF | 0x40381724 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT46_DT | 0x40381730 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT46_TR_CMD | 0x40381740 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT46_TR_IN_SEL0 | 0x40381744 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT46_TR_IN_SEL1 | 0x40381748 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT46_TR_IN_EDGE_SEL | 0x4038174C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT46_TR_PWM_CTRL | 0x40381750 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT46_TR_OUT_SEL | 0x40381754 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT46_INTR | 0x40381770 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT46_INTR_SET | 0x40381774 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT46_INTR_MASK | 0x40381778 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT46_INTR_MASKED | 0x4038177C | FULL | Interrupt masked request register |

28.1.48 CNT 47

| Register Name | Address | Permission | Description |
|--|------------|------------|---|
| TCPWM0_GRP0_CNT47_CTRL | 0x40381780 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT47_STATUS | 0x40381784 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT47_COUNTER | 0x40381788 | FULL | Counter count register |
| TCPWM0_GRP0_CNT47_CC0 | 0x40381790 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT47_CC0_BUFF | 0x40381794 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT47_CC1 | 0x40381798 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT47_CC1_BUFF | 0x4038179C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT47_PERIOD | 0x403817A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT47_PERIOD_BUFF | 0x403817A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT47_DT | 0x403817B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT47_TR_CMD | 0x403817C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT47_TR_IN_SEL0 | 0x403817C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT47_TR_IN_SEL1 | 0x403817C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT47_TR_IN_EDGE_SEL | 0x403817CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT47_TR_PWM_CTRL | 0x403817D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT47_TR_OUT_SEL | 0x403817D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT47_INTR | 0x403817F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT47_INTR_SET | 0x403817F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT47_INTR_MASK | 0x403817F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT47_INTR_MASKED | 0x403817FC | FULL | Interrupt masked request register |

28.1.49 CNT 48

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT48_CTRL | 0x40381800 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT48_STATUS | 0x40381804 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT48_COUNTER | 0x40381808 | FULL | Counter count register |
| TCPWM0_GRP0_CNT48_CC0 | 0x40381810 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT48_CC0_BUFF | 0x40381814 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT48_CC1 | 0x40381818 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT48_CC1_BUFF | 0x4038181C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT48_PERIOD | 0x40381820 | FULL | Counter period register |
| TCPWM0_GRP0_CNT48_PERIOD_BUFF | 0x40381824 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT48_DT | 0x40381830 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT48_TR_CMD | 0x40381840 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT48_TR_IN_SEL0 | 0x40381844 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT48_TR_IN_SEL1 | 0x40381848 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT48_TR_IN_EDGE_SEL | 0x4038184C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT48_TR_PWM_CTRL | 0x40381850 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT48_TR_OUT_SEL | 0x40381854 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT48_INTR | 0x40381870 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT48_INTR_SET | 0x40381874 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT48_INTR_MASK | 0x40381878 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT48_INTR_MASKED | 0x4038187C | FULL | Interrupt masked request register |

28.1.50 CNT 49

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT49_CTRL | 0x40381880 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT49_STATUS | 0x40381884 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT49_COUNTER | 0x40381888 | FULL | Counter count register |
| TCPWM0_GRP0_CNT49_CC0 | 0x40381890 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT49_CC0_BUFF | 0x40381894 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT49_CC1 | 0x40381898 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT49_CC1_BUFF | 0x4038189C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT49_PERIOD | 0x403818A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT49_PERIOD_BUFF | 0x403818A4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT49_DT | 0x403818B0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT49_TR_CMD | 0x403818C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT49_TR_IN_SEL0 | 0x403818C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT49_TR_IN_SEL1 | 0x403818C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT49_TR_IN_EDGE_SEL | 0x403818CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT49_TR_PWM_CTRL | 0x403818D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT49_TR_OUT_SEL | 0x403818D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT49_INTR | 0x403818F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT49_INTR_SET | 0x403818F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT49_INTR_MASK | 0x403818F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT49_INTR_MASKED | 0x403818FC | FULL | Interrupt masked request register |

28.1.51 CNT 50

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT50_CTRL | 0x40381900 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT50_STATUS | 0x40381904 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT50_COUNTER | 0x40381908 | FULL | Counter count register |
| TCPWM0_GRP0_CNT50_CC0 | 0x40381910 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT50_CC0_BUFF | 0x40381914 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT50_CC1 | 0x40381918 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT50_CC1_BUFF | 0x4038191C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT50_PERIOD | 0x40381920 | FULL | Counter period register |
| TCPWM0_GRP0_CNT50_PERIOD_BUFF | 0x40381924 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT50_DT | 0x40381930 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT50_TR_CMD | 0x40381940 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT50_TR_IN_SEL0 | 0x40381944 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT50_TR_IN_SEL1 | 0x40381948 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT50_TR_IN_EDGE_SEL | 0x4038194C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT50_TR_PWM_CTRL | 0x40381950 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT50_TR_OUT_SEL | 0x40381954 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT50_INTR | 0x40381970 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT50_INTR_SET | 0x40381974 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT50_INTR_MASK | 0x40381978 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT50_INTR_MASKED | 0x4038197C | FULL | Interrupt masked request register |

28.1.52 CNT 51

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT51_CTRL | 0x40381980 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT51_STATUS | 0x40381984 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT51_COUNTER | 0x40381988 | FULL | Counter count register |
| TCPWM0_GRP0_CNT51_CC0 | 0x40381990 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT51_CC0_BUFF | 0x40381994 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT51_CC1 | 0x40381998 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT51_CC1_BUFF | 0x4038199C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT51_PERIOD | 0x403819A0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT51_PERIOD_BUFF | 0x403819A4 | FULL | Counter buffered period register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT51_DT | 0x403819B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT51_TR_CMD | 0x403819C0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT51_TR_IN_SEL0 | 0x403819C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT51_TR_IN_SEL1 | 0x403819C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT51_TR_IN_EDGE_SEL | 0x403819CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT51_TR_PWM_CTRL | 0x403819D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT51_TR_OUT_SEL | 0x403819D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT51_INTR | 0x403819F0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT51_INTR_SET | 0x403819F4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT51_INTR_MASK | 0x403819F8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT51_INTR_MASKED | 0x403819FC | FULL | Interrupt masked request register |

28.1.53 CNT 52

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT52_CTRL | 0x40381A00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT52_STATUS | 0x40381A04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT52_COUNTER | 0x40381A08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT52_CC0 | 0x40381A10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT52_CC0_BUFF | 0x40381A14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT52_CC1 | 0x40381A18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT52_CC1_BUFF | 0x40381A1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT52_PERIOD | 0x40381A20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT52_PERIOD_BUFF | 0x40381A24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT52_DT | 0x40381A30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT52_TR_CMD | 0x40381A40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT52_TR_IN_SEL0 | 0x40381A44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT52_TR_IN_SEL1 | 0x40381A48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT52_TR_IN_EDGE_SEL | 0x40381A4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT52_TR_PWM_CTRL | 0x40381A50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT52_TR_OUT_SEL | 0x40381A54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT52_INTR | 0x40381A70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT52_INTR_SET | 0x40381A74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT52_INTR_MASK | 0x40381A78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT52_INTR_MASKED | 0x40381A7C | FULL | Interrupt masked request register |

28.1.54 CNT 53

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT53_CTRL | 0x40381A80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT53_STATUS | 0x40381A84 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT53_COUNTER | 0x40381A88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT53_CC0 | 0x40381A90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT53_CC0_BUFF | 0x40381A94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT53_CC1 | 0x40381A98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT53_CC1_BUFF | 0x40381A9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT53_PERIOD | 0x40381AA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT53_PERIOD_BUFF | 0x40381AA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT53_DT | 0x40381AB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT53_TR_CMD | 0x40381AC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT53_TR_IN_SEL0 | 0x40381AC4 | FULL | Counter input trigger selection register 0 |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT53_TR_IN_SEL1 | 0x40381AC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT53_TR_IN_EDGE_SEL | 0x40381ACC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT53_TR_PWM_CTRL | 0x40381AD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT53_TR_OUT_SEL | 0x40381AD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT53_INTR | 0x40381AF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT53_INTR_SET | 0x40381AF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT53_INTR_MASK | 0x40381AF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT53_INTR_MASKED | 0x40381AFC | FULL | Interrupt masked request register |

28.1.55 CNT 54

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT54_CTRL | 0x40381B00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT54_STATUS | 0x40381B04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT54_COUNTER | 0x40381B08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT54_CC0 | 0x40381B10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT54_CC0_BUFF | 0x40381B14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT54_CC1 | 0x40381B18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT54_CC1_BUFF | 0x40381B1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT54_PERIOD | 0x40381B20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT54_PERIOD_BUFF | 0x40381B24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT54_DT | 0x40381B30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT54_TR_CMD | 0x40381B40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT54_TR_IN_SEL0 | 0x40381B44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT54_TR_IN_SEL1 | 0x40381B48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT54_TR_IN_EDGE_SEL | 0x40381B4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT54_TR_PWM_CTRL | 0x40381B50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT54_TR_OUT_SEL | 0x40381B54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT54_INTR | 0x40381B70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT54_INTR_SET | 0x40381B74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT54_INTR_MASK | 0x40381B78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT54_INTR_MASKED | 0x40381B7C | FULL | Interrupt masked request register |

28.1.56 CNT 55

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT55_CTRL | 0x40381B80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT55_STATUS | 0x40381B84 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT55_COUNTER | 0x40381B88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT55_CC0 | 0x40381B90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT55_CC0_BUFF | 0x40381B94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT55_CC1 | 0x40381B98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT55_CC1_BUFF | 0x40381B9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT55_PERIOD | 0x40381BA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT55_PERIOD_BUFF | 0x40381BA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT55_DT | 0x40381BB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT55_TR_CMD | 0x40381BC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT55_TR_IN_SEL0 | 0x40381BC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT55_TR_IN_SEL1 | 0x40381BC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT55_TR_IN_EDGE_SEL | 0x40381BCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT55_TR_PWM_CTRL | 0x40381BD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT55_TR_OUT_SEL | 0x40381BD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT55_INTR | 0x40381BF0 | FULL | Interrupt request register |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP0_CNT55_INTR_SET | 0x40381BF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT55_INTR_MASK | 0x40381BF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT55_INTR_MASKED | 0x40381BFC | FULL | Interrupt masked request register |

28.1.57 CNT 56

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT56_CTRL | 0x40381C00 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT56_STATUS | 0x40381C04 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT56_COUNTER | 0x40381C08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT56_CC0 | 0x40381C10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT56_CC0_BUFF | 0x40381C14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT56_CC1 | 0x40381C18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT56_CC1_BUFF | 0x40381C1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT56_PERIOD | 0x40381C20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT56_PERIOD_BUFF | 0x40381C24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT56_DT | 0x40381C30 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT56_TR_CMD | 0x40381C40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT56_TR_IN_SEL0 | 0x40381C44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT56_TR_IN_SEL1 | 0x40381C48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT56_TR_IN_EDGE_SEL | 0x40381C4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT56_TR_PWM_CTRL | 0x40381C50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT56_TR_OUT_SEL | 0x40381C54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT56_INTR | 0x40381C70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT56_INTR_SET | 0x40381C74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT56_INTR_MASK | 0x40381C78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT56_INTR_MASKED | 0x40381C7C | FULL | Interrupt masked request register |

28.1.58 CNT 57

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT57_CTRL | 0x40381C80 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT57_STATUS | 0x40381C84 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT57_COUNTER | 0x40381C88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT57_CC0 | 0x40381C90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT57_CC0_BUFF | 0x40381C94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT57_CC1 | 0x40381C98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT57_CC1_BUFF | 0x40381C9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT57_PERIOD | 0x40381CA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT57_PERIOD_BUFF | 0x40381CA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT57_DT | 0x40381CB0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT57_TR_CMD | 0x40381CC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT57_TR_IN_SEL0 | 0x40381CC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT57_TR_IN_SEL1 | 0x40381CC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT57_TR_IN_EDGE_SEL | 0x40381CCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT57_TR_PWM_CTRL | 0x40381CD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT57_TR_OUT_SEL | 0x40381CD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT57_INTR | 0x40381CF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT57_INTR_SET | 0x40381CF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT57_INTR_MASK | 0x40381CF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT57_INTR_MASKED | 0x40381CFC | FULL | Interrupt masked request register |

28.1.59 CNT 58

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT58_CTRL | 0x40381D00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT58_STATUS | 0x40381D04 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT58_COUNTER | 0x40381D08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT58_CC0 | 0x40381D10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT58_CC0_BUFF | 0x40381D14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT58_CC1 | 0x40381D18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT58_CC1_BUFF | 0x40381D1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT58_PERIOD | 0x40381D20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT58_PERIOD_BUFF | 0x40381D24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT58_DT | 0x40381D30 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT58_TR_CMD | 0x40381D40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT58_TR_IN_SEL0 | 0x40381D44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT58_TR_IN_SEL1 | 0x40381D48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT58_TR_IN_EDGE_SEL | 0x40381D4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT58_TR_PWM_CTRL | 0x40381D50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT58_TR_OUT_SEL | 0x40381D54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT58_INTR | 0x40381D70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT58_INTR_SET | 0x40381D74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT58_INTR_MASK | 0x40381D78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT58_INTR_MASKED | 0x40381D7C | FULL | Interrupt masked request register |

28.1.60 CNT 59

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT59_CTRL | 0x40381D80 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT59_STATUS | 0x40381D84 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT59_COUNTER | 0x40381D88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT59_CC0 | 0x40381D90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT59_CC0_BUFF | 0x40381D94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT59_CC1 | 0x40381D98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT59_CC1_BUFF | 0x40381D9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT59_PERIOD | 0x40381DA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT59_PERIOD_BUFF | 0x40381DA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT59_DT | 0x40381DB0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT59_TR_CMD | 0x40381DC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT59_TR_IN_SEL0 | 0x40381DC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT59_TR_IN_SEL1 | 0x40381DC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT59_TR_IN_EDGE_SEL | 0x40381DCC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT59_TR_PWM_CTRL | 0x40381DD0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT59_TR_OUT_SEL | 0x40381DD4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT59_INTR | 0x40381DF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT59_INTR_SET | 0x40381DF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT59_INTR_MASK | 0x40381DF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT59_INTR_MASKED | 0x40381DFC | FULL | Interrupt masked request register |

28.1.61 CNT 60

| Register Name | Address | Permission | Description |
|------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT60_CTRL | 0x40381E00 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT60_STATUS | 0x40381E04 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT60_COUNTER | 0x40381E08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT60_CC0 | 0x40381E10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT60_CC0_BUFF | 0x40381E14 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT60_CC1 | 0x40381E18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT60_CC1_BUFF | 0x40381E1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT60_PERIOD | 0x40381E20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT60_PERIOD_BUFF | 0x40381E24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT60_DT | 0x40381E30 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT60_TR_CMD | 0x40381E40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT60_TR_IN_SEL0 | 0x40381E44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT60_TR_IN_SEL1 | 0x40381E48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT60_TR_IN_EDGE_SEL | 0x40381E4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT60_TR_PWM_CTRL | 0x40381E50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT60_TR_OUT_SEL | 0x40381E54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT60_INTR | 0x40381E70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT60_INTR_SET | 0x40381E74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT60_INTR_MASK | 0x40381E78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT60_INTR_MASKED | 0x40381E7C | FULL | Interrupt masked request register |

28.1.62 CNT 61

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT61_CTRL | 0x40381E80 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT61_STATUS | 0x40381E84 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT61_COUNTER | 0x40381E88 | FULL | Counter count register |
| TCPWM0_GRP0_CNT61_CC0 | 0x40381E90 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT61_CC0_BUFF | 0x40381E94 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP0_CNT61_CC1 | 0x40381E98 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT61_CC1_BUFF | 0x40381E9C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT61_PERIOD | 0x40381EA0 | FULL | Counter period register |
| TCPWM0_GRP0_CNT61_PERIOD_BUFF | 0x40381EA4 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT61_DT | 0x40381EB0 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT61_TR_CMD | 0x40381EC0 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT61_TR_IN_SEL0 | 0x40381EC4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT61_TR_IN_SEL1 | 0x40381EC8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT61_TR_IN_EDGE_SEL | 0x40381ECC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT61_TR_PWM_CTRL | 0x40381ED0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT61_TR_OUT_SEL | 0x40381ED4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT61_INTR | 0x40381EF0 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT61_INTR_SET | 0x40381EF4 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT61_INTR_MASK | 0x40381EF8 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT61_INTR_MASKED | 0x40381EFC | FULL | Interrupt masked request register |

28.1.63 CNT 62

| Register Name | Address | Permission | Description |
|----------------------------|------------|------------|--|
| TCPWM0_GRP0_CNT62_CTRL | 0x40381F00 | FULL | Counter control register Note:AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP0_CNT62_STATUS | 0x40381F04 | FULL | Counter status register Note:DT_CNT_H is not available for this register |
| TCPWM0_GRP0_CNT62_COUNTER | 0x40381F08 | FULL | Counter count register |
| TCPWM0_GRP0_CNT62_CC0 | 0x40381F10 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP0_CNT62_CC0_BUFF | 0x40381F14 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP0_CNT62_CC1 | 0x40381F18 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP0_CNT62_CC1_BUFF | 0x40381F1C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP0_CNT62_PERIOD | 0x40381F20 | FULL | Counter period register |
| TCPWM0_GRP0_CNT62_PERIOD_BUFF | 0x40381F24 | FULL | Counter buffered period register |
| TCPWM0_GRP0_CNT62_DT | 0x40381F30 | FULL | Counter PWM dead time register Note:DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP0_CNT62_TR_CMD | 0x40381F40 | FULL | Counter trigger command register |
| TCPWM0_GRP0_CNT62_TR_IN_SEL0 | 0x40381F44 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP0_CNT62_TR_IN_SEL1 | 0x40381F48 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP0_CNT62_TR_IN_EDGE_SEL | 0x40381F4C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP0_CNT62_TR_PWM_CTRL | 0x40381F50 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP0_CNT62_TR_OUT_SEL | 0x40381F54 | FULL | Counter output trigger selection register |
| TCPWM0_GRP0_CNT62_INTR | 0x40381F70 | FULL | Interrupt request register |
| TCPWM0_GRP0_CNT62_INTR_SET | 0x40381F74 | FULL | Interrupt set request register |
| TCPWM0_GRP0_CNT62_INTR_MASK | 0x40381F78 | FULL | Interrupt mask register |
| TCPWM0_GRP0_CNT62_INTR_MASKED | 0x40381F7C | FULL | Interrupt masked request register |

28.2 GRP 1

28.2.1 CNT 0

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT0_CTRL | 0x40388000 | FULL | Counter control register |
| TCPWM0_GRP1_CNT0_STATUS | 0x40388004 | FULL | Counter status register |
| TCPWM0_GRP1_CNT0_COUNTER | 0x40388008 | FULL | Counter count register |
| TCPWM0_GRP1_CNT0_CC0 | 0x40388010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT0_CC0_BUFF | 0x40388014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT0_CC1 | 0x40388018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT0_CC1_BUFF | 0x4038801C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT0_PERIOD | 0x40388020 | FULL | Counter period register |
| TCPWM0_GRP1_CNT0_PERIOD_BUFF | 0x40388024 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT0_LINE_SEL | 0x40388028 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT0_LINE_SEL_BUFF | 0x4038802C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT0_DT | 0x40388030 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT0_TR_CMD | 0x40388040 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT0_TR_IN_SEL0 | 0x40388044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT0_TR_IN_SEL1 | 0x40388048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL | 0x4038804C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT0_TR_PWM_CTRL | 0x40388050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT0_TR_OUT_SEL | 0x40388054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT0_INTR | 0x40388070 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT0_INTR_SET | 0x40388074 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT0_INTR_MASK | 0x40388078 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT0_INTR_MASKED | 0x4038807C | FULL | Interrupt masked request register |

28.2.2 CNT 1

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT1_CTRL | 0x40388080 | FULL | Counter control register |
| TCPWM0_GRP1_CNT1_STATUS | 0x40388084 | FULL | Counter status register |
| TCPWM0_GRP1_CNT1_COUNTER | 0x40388088 | FULL | Counter count register |
| TCPWM0_GRP1_CNT1_CC0 | 0x40388090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT1_CC0_BUFF | 0x40388094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT1_CC1 | 0x40388098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT1_CC1_BUFF | 0x4038809C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT1_PERIOD | 0x403880A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT1_PERIOD_BUFF | 0x403880A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT1_LINE_SEL | 0x403880A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT1_LINE_SEL_BUFF | 0x403880AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT1_DT | 0x403880B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT1_TR_CMD | 0x403880C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT1_TR_IN_SEL0 | 0x403880C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT1_TR_IN_SEL1 | 0x403880C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT1_TR_IN_EDGE_SEL | 0x403880CC | FULL | Counter input trigger edge selection register |

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT1_TR_PWM_CTRL | 0x403880D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT1_TR_OUT_SEL | 0x403880D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT1_INTR | 0x403880F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT1_INTR_SET | 0x403880F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT1_INTR_MASK | 0x403880F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT1_INTR_MASKED | 0x403880FC | FULL | Interrupt masked request register |

28.2.3 CNT 2

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT2_CTRL | 0x40388100 | FULL | Counter control register |
| TCPWM0_GRP1_CNT2_STATUS | 0x40388104 | FULL | Counter status register |
| TCPWM0_GRP1_CNT2_COUNTER | 0x40388108 | FULL | Counter count register |
| TCPWM0_GRP1_CNT2_CC0 | 0x40388110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT2_CC0_BUFF | 0x40388114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT2_CC1 | 0x40388118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT2_CC1_BUFF | 0x4038811C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT2_PERIOD | 0x40388120 | FULL | Counter period register |
| TCPWM0_GRP1_CNT2_PERIOD_BUFF | 0x40388124 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT2_LINE_SEL | 0x40388128 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT2_LINE_SEL_BUFF | 0x4038812C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT2_DT | 0x40388130 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT2_TR_CMD | 0x40388140 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT2_TR_IN_SEL0 | 0x40388144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT2_TR_IN_SEL1 | 0x40388148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT2_TR_IN_EDGE_SEL | 0x4038814C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT2_TR_PWM_CTRL | 0x40388150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT2_TR_OUT_SEL | 0x40388154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT2_INTR | 0x40388170 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT2_INTR_SET | 0x40388174 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT2_INTR_MASK | 0x40388178 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT2_INTR_MASKED | 0x4038817C | FULL | Interrupt masked request register |

28.2.4 CNT 3

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT3_CTRL | 0x40388180 | FULL | Counter control register |
| TCPWM0_GRP1_CNT3_STATUS | 0x40388184 | FULL | Counter status register |
| TCPWM0_GRP1_CNT3_COUNTER | 0x40388188 | FULL | Counter count register |
| TCPWM0_GRP1_CNT3_CC0 | 0x40388190 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT3_CC0_BUFF | 0x40388194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT3_CC1 | 0x40388198 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT3_CC1_BUFF | 0x4038819C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT3_PERIOD | 0x403881A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT3_PERIOD_BUFF | 0x403881A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT3_LINE_SEL | 0x403881A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT3_LINE_SEL_BUFF | 0x403881AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT3_DT | 0x403881B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT3_TR_CMD | 0x403881C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT3_TR_IN_SEL0 | 0x403881C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT3_TR_IN_SEL1 | 0x403881C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT3_TR_IN_EDGE_SEL | 0x403881CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT3_TR_PWM_CTRL | 0x403881D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT3_TR_OUT_SEL | 0x403881D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT3_INTR | 0x403881F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT3_INTR_SET | 0x403881F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT3_INTR_MASK | 0x403881F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT3_INTR_MASKED | 0x403881FC | FULL | Interrupt masked request register |

28.2.5 CNT 4

| Register Name | Address | Permission | Description |
|--------------------------|------------|------------|------------------------------------|
| TCPWM0_GRP1_CNT4_CTRL | 0x40388200 | FULL | Counter control register |
| TCPWM0_GRP1_CNT4_STATUS | 0x40388204 | FULL | Counter status register |
| TCPWM0_GRP1_CNT4_COUNTER | 0x40388208 | FULL | Counter count register |
| TCPWM0_GRP1_CNT4_CC0 | 0x40388210 | FULL | Counter compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT4_CC0_BUFF | 0x40388214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT4_CC1 | 0x40388218 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT4_CC1_BUFF | 0x4038821C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT4_PERIOD | 0x40388220 | FULL | Counter period register |
| TCPWM0_GRP1_CNT4_PERIOD_BUFF | 0x40388224 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT4_LINE_SEL | 0x40388228 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT4_LINE_SEL_BUFF | 0x4038822C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT4_DT | 0x40388230 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT4_TR_CMD | 0x40388240 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT4_TR_IN_SEL0 | 0x40388244 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT4_TR_IN_SEL1 | 0x40388248 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT4_TR_IN_EDGE_SEL | 0x4038824C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT4_TR_PWM_CTRL | 0x40388250 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT4_TR_OUT_SEL | 0x40388254 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT4_INTR | 0x40388270 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT4_INTR_SET | 0x40388274 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT4_INTR_MASK | 0x40388278 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT4_INTR_MASKED | 0x4038827C | FULL | Interrupt masked request register |

28.2.6 CNT 5

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT5_CTRL | 0x40388280 | FULL | Counter control register |
| TCPWM0_GRP1_CNT5_STATUS | 0x40388284 | FULL | Counter status register |
| TCPWM0_GRP1_CNT5_COUNTER | 0x40388288 | FULL | Counter count register |
| TCPWM0_GRP1_CNT5_CC0 | 0x40388290 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT5_CC0_BUFF | 0x40388294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT5_CC1 | 0x40388298 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT5_CC1_BUFF | 0x4038829C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT5_PERIOD | 0x403882A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT5_PERIOD_BUFF | 0x403882A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT5_LINE_SEL | 0x403882A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT5_LINE_SEL_BUFF | 0x403882AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT5_DT | 0x403882B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT5_TR_CMD | 0x403882C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT5_TR_IN_SEL0 | 0x403882C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT5_TR_IN_SEL1 | 0x403882C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT5_TR_IN_EDGE_SEL | 0x403882CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT5_TR_PWM_CTRL | 0x403882D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT5_TR_OUT_SEL | 0x403882D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT5_INTR | 0x403882F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT5_INTR_SET | 0x403882F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT5_INTR_MASK | 0x403882F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT5_INTR_MASKED | 0x403882FC | FULL | Interrupt masked request register |

28.2.7 CNT 6

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT6_CTRL | 0x40388300 | FULL | Counter control register |
| TCPWM0_GRP1_CNT6_STATUS | 0x40388304 | FULL | Counter status register |
| TCPWM0_GRP1_CNT6_COUNTER | 0x40388308 | FULL | Counter count register |
| TCPWM0_GRP1_CNT6_CC0 | 0x40388310 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT6_CC0_BUFF | 0x40388314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT6_CC1 | 0x40388318 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT6_CC1_BUFF | 0x4038831C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT6_PERIOD | 0x40388320 | FULL | Counter period register |
| TCPWM0_GRP1_CNT6_PERIOD_BUFF | 0x40388324 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT6_LINE_SEL | 0x40388328 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT6_LINE_SEL_BUFF | 0x4038832C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT6_DT | 0x40388330 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT6_TR_CMD | 0x40388340 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT6_TR_IN_SEL0 | 0x40388344 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT6_TR_IN_SEL1 | 0x40388348 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT6_TR_IN_EDGE_SEL | 0x4038834C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT6_TR_PWM_CTRL | 0x40388350 | FULL | Counter trigger PWM control register |

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT6_TR_OUT_SEL | 0x40388354 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT6_INTR | 0x40388370 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT6_INTR_SET | 0x40388374 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT6_INTR_MASK | 0x40388378 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT6_INTR_MASKED | 0x4038837C | FULL | Interrupt masked request register |

28.2.8 CNT 7

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT7_CTRL | 0x40388380 | FULL | Counter control register |
| TCPWM0_GRP1_CNT7_STATUS | 0x40388384 | FULL | Counter status register |
| TCPWM0_GRP1_CNT7_COUNTER | 0x40388388 | FULL | Counter count register |
| TCPWM0_GRP1_CNT7_CC0 | 0x40388390 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT7_CC0_BUFF | 0x40388394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT7_CC1 | 0x40388398 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT7_CC1_BUFF | 0x4038839C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT7_PERIOD | 0x403883A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT7_PERIOD_BUFF | 0x403883A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT7_LINE_SEL | 0x403883A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT7_LINE_SEL_BUFF | 0x403883AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT7_DT | 0x403883B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT7_TR_CMD | 0x403883C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT7_TR_IN_SEL0 | 0x403883C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT7_TR_IN_SEL1 | 0x403883C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT7_TR_IN_EDGE_SEL | 0x403883CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT7_TR_PWM_CTRL | 0x403883D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT7_TR_OUT_SEL | 0x403883D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT7_INTR | 0x403883F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT7_INTR_SET | 0x403883F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT7_INTR_MASK | 0x403883F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT7_INTR_MASKED | 0x403883FC | FULL | Interrupt masked request register |

28.2.9 CNT 8

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT8_CTRL | 0x40388400 | FULL | Counter control register |
| TCPWM0_GRP1_CNT8_STATUS | 0x40388404 | FULL | Counter status register |
| TCPWM0_GRP1_CNT8_COUNTER | 0x40388408 | FULL | Counter count register |
| TCPWM0_GRP1_CNT8_CC0 | 0x40388410 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT8_CC0_BUFF | 0x40388414 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT8_CC1 | 0x40388418 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT8_CC1_BUFF | 0x4038841C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT8_PERIOD | 0x40388420 | FULL | Counter period register |
| TCPWM0_GRP1_CNT8_PERIOD_BUFF | 0x40388424 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT8_LINE_SEL | 0x40388428 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT8_LINE_SEL_BUFF | 0x4038842C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT8_DT | 0x40388430 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT8_TR_CMD | 0x40388440 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT8_TR_IN_SEL0 | 0x40388444 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT8_TR_IN_SEL1 | 0x40388448 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT8_TR_IN_EDGE_SEL | 0x4038844C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT8_TR_PWM_CTRL | 0x40388450 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT8_TR_OUT_SEL | 0x40388454 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT8_INTR | 0x40388470 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT8_INTR_SET | 0x40388474 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT8_INTR_MASK | 0x40388478 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT8_INTR_MASKED | 0x4038847C | FULL | Interrupt masked request register |

28.2.10 CNT 9

| Register Name | Address | Permission | Description |
|---------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT9_CTRL | 0x40388480 | FULL | Counter control register |
| TCPWM0_GRP1_CNT9_STATUS | 0x40388484 | FULL | Counter status register |
| TCPWM0_GRP1_CNT9_COUNTER | 0x40388488 | FULL | Counter count register |
| TCPWM0_GRP1_CNT9_CC0 | 0x40388490 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT9_CC0_BUFF | 0x40388494 | FULL | Counter buffered compare/capture 0 register |

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT9_CC1 | 0x40388498 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT9_CC1_BUFF | 0x4038849C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT9_PERIOD | 0x403884A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT9_PERIOD_BUFF | 0x403884A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT9_LINE_SEL | 0x403884A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT9_LINE_SEL_BUFF | 0x403884AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT9_DT | 0x403884B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT9_TR_CMD | 0x403884C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT9_TR_IN_SEL0 | 0x403884C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT9_TR_IN_SEL1 | 0x403884C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT9_TR_IN_EDGE_SEL | 0x403884CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT9_TR_PWM_CTRL | 0x403884D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT9_TR_OUT_SEL | 0x403884D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT9_INTR | 0x403884F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT9_INTR_SET | 0x403884F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT9_INTR_MASK | 0x403884F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT9_INTR_MASKED | 0x403884FC | FULL | Interrupt masked request register |

28.2.11 CNT 10

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT10_CTRL | 0x40388500 | FULL | Counter control register |
| TCPWM0_GRP1_CNT10_STATUS | 0x40388504 | FULL | Counter status register |
| TCPWM0_GRP1_CNT10_COUNTER | 0x40388508 | FULL | Counter count register |
| TCPWM0_GRP1_CNT10_CC0 | 0x40388510 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT10_CC0_BUFF | 0x40388514 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT10_CC1 | 0x40388518 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT10_CC1_BUFF | 0x4038851C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT10_PERIOD | 0x40388520 | FULL | Counter period register |
| TCPWM0_GRP1_CNT10_PERIOD_BUFF | 0x40388524 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT10_LINE_SEL | 0x40388528 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT10_LINE_SEL_BUFF | 0x4038852C | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT10_DT | 0x40388530 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT10_TR_CMD | 0x40388540 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT10_TR_IN_SEL0 | 0x40388544 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT10_TR_IN_SEL1 | 0x40388548 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT10_TR_IN_EDGE_SEL | 0x4038854C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT10_TR_PWM_CTRL | 0x40388550 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT10_TR_OUT_SEL | 0x40388554 | FULL | Counter output trigger selection register |
| TCPWM0_GRP1_CNT10_INTR | 0x40388570 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT10_INTR_SET | 0x40388574 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT10_INTR_MASK | 0x40388578 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT10_INTR_MASKED | 0x4038857C | FULL | Interrupt masked request register |

28.2.12 CNT 11

| Register Name | Address | Permission | Description |
|----------------------------------|------------|------------|---|
| TCPWM0_GRP1_CNT11_CTRL | 0x40388580 | FULL | Counter control register |
| TCPWM0_GRP1_CNT11_STATUS | 0x40388584 | FULL | Counter status register |
| TCPWM0_GRP1_CNT11_COUNTER | 0x40388588 | FULL | Counter count register |
| TCPWM0_GRP1_CNT11_CC0 | 0x40388590 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP1_CNT11_CC0_BUFF | 0x40388594 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP1_CNT11_CC1 | 0x40388598 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP1_CNT11_CC1_BUFF | 0x4038859C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP1_CNT11_PERIOD | 0x403885A0 | FULL | Counter period register |
| TCPWM0_GRP1_CNT11_PERIOD_BUFF | 0x403885A4 | FULL | Counter buffered period register |
| TCPWM0_GRP1_CNT11_LINE_SEL | 0x403885A8 | FULL | Counter line selection register |
| TCPWM0_GRP1_CNT11_LINE_SEL_BUFF | 0x403885AC | FULL | Counter buffered line selection register |
| TCPWM0_GRP1_CNT11_DT | 0x403885B0 | FULL | Counter PWM dead time register |
| TCPWM0_GRP1_CNT11_TR_CMD | 0x403885C0 | FULL | Counter trigger command register |
| TCPWM0_GRP1_CNT11_TR_IN_SEL0 | 0x403885C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP1_CNT11_TR_IN_SEL1 | 0x403885C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP1_CNT11_TR_IN_EDGE_SEL | 0x403885CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP1_CNT11_TR_PWM_CTRL | 0x403885D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP1_CNT11_TR_OUT_SEL | 0x403885D4 | FULL | Counter output trigger selection register |

| Register Name | Address | Permission | Description |
|-------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP1_CNT11_INTR | 0x403885F0 | FULL | Interrupt request register |
| TCPWM0_GRP1_CNT11_INTR_SET | 0x403885F4 | FULL | Interrupt set request register |
| TCPWM0_GRP1_CNT11_INTR_MASK | 0x403885F8 | FULL | Interrupt mask register |
| TCPWM0_GRP1_CNT11_INTR_MASKED | 0x403885FC | FULL | Interrupt masked request register |

28.3 GRP 2

28.3.1 CNT 0

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT0_CTRL | 0x40390000 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT0_STATUS | 0x40390004 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT0_COUNTER | 0x40390008 | FULL | Counter count register |
| TCPWM0_GRP2_CNT0_CC0 | 0x40390010 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT0_CC0_BUFF | 0x40390014 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT0_CC1 | 0x40390018 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT0_CC1_BUFF | 0x4039001C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT0_PERIOD | 0x40390020 | FULL | Counter period register |
| TCPWM0_GRP2_CNT0_PERIOD_BUFF | 0x40390024 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT0_DT | 0x40390030 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT0_TR_CMD | 0x40390040 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT0_TR_IN_SEL0 | 0x40390044 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT0_TR_IN_SEL1 | 0x40390048 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT0_TR_IN_EDGE_SEL | 0x4039004C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT0_TR_PWM_CTRL | 0x40390050 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT0_TR_OUT_SEL | 0x40390054 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT0_INTR | 0x40390070 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT0_INTR_SET | 0x40390074 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT0_INTR_MASK | 0x40390078 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT0_INTR_MASKED | 0x4039007C | FULL | Interrupt masked request register |

28.3.2 CNT 1

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT1_CTRL | 0x40390080 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT1_STATUS | 0x40390084 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT1_COUNTER | 0x40390088 | FULL | Counter count register |
| TCPWM0_GRP2_CNT1_CC0 | 0x40390090 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT1_CC0_BUFF | 0x40390094 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT1_CC1 | 0x40390098 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT1_CC1_BUFF | 0x4039009C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT1_PERIOD | 0x403900A0 | FULL | Counter period register |
| TCPWM0_GRP2_CNT1_PERIOD_BUFF | 0x403900A4 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT1_DT | 0x403900B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT1_TR_CMD | 0x403900C0 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT1_TR_IN_SEL0 | 0x403900C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT1_TR_IN_SEL1 | 0x403900C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT1_TR_IN_EDGE_SEL | 0x403900CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT1_TR_PWM_CTRL | 0x403900D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT1_TR_OUT_SEL | 0x403900D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT1_INTR | 0x403900F0 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT1_INTR_SET | 0x403900F4 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT1_INTR_MASK | 0x403900F8 | FULL | Interrupt mask register |

| Register Name | Address | Permission | Description |
|------------------------------|------------|------------|-----------------------------------|
| TCPWM0_GRP2_CNT1_INTR_MASKED | 0x403900FC | FULL | Interrupt masked request register |

28.3.3 CNT 2

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT2_CTRL | 0x40390100 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT2_STATUS | 0x40390104 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT2_COUNTER | 0x40390108 | FULL | Counter count register |
| TCPWM0_GRP2_CNT2_CC0 | 0x40390110 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT2_CC0_BUFF | 0x40390114 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT2_CC1 | 0x40390118 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT2_CC1_BUFF | 0x4039011C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT2_PERIOD | 0x40390120 | FULL | Counter period register |
| TCPWM0_GRP2_CNT2_PERIOD_BUFF | 0x40390124 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT2_DT | 0x40390130 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT2_TR_CMD | 0x40390140 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT2_TR_IN_SEL0 | 0x40390144 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT2_TR_IN_SEL1 | 0x40390148 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT2_TR_IN_EDGE_SEL | 0x4039014C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT2_TR_PWM_CTRL | 0x40390150 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT2_TR_OUT_SEL | 0x40390154 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT2_INTR | 0x40390170 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT2_INTR_SET | 0x40390174 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT2_INTR_MASK | 0x40390178 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT2_INTR_MASKED | 0x4039017C | FULL | Interrupt masked request register |

28.3.4 CNT 3

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT3_CTRL | 0x40390180 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT3_STATUS | 0x40390184 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT3_COUNTER | 0x40390188 | FULL | Counter count register |
| TCPWM0_GRP2_CNT3_CC0 | 0x40390190 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT3_CC0_BUFF | 0x40390194 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT3_CC1 | 0x40390198 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT3_CC1_BUFF | 0x4039019C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT3_PERIOD | 0x403901A0 | FULL | Counter period register |
| TCPWM0_GRP2_CNT3_PERIOD_BUFF | 0x403901A4 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT3_DT | 0x403901B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT3_TR_CMD | 0x403901C0 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT3_TR_IN_SEL0 | 0x403901C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT3_TR_IN_SEL1 | 0x403901C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT3_TR_IN_EDGE_SEL | 0x403901CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT3_TR_PWM_CTRL | 0x403901D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT3_TR_OUT_SEL | 0x403901D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT3_INTR | 0x403901F0 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT3_INTR_SET | 0x403901F4 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT3_INTR_MASK | 0x403901F8 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT3_INTR_MASKED | 0x403901FC | FULL | Interrupt masked request register |

28.3.5 CNT 4

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT4_CTRL | 0x40390200 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT4_STATUS | 0x40390204 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT4_COUNTER | 0x40390208 | FULL | Counter count register |
| TCPWM0_GRP2_CNT4_CC0 | 0x40390210 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT4_CC0_BUFF | 0x40390214 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT4_CC1 | 0x40390218 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT4_CC1_BUFF | 0x4039021C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT4_PERIOD | 0x40390220 | FULL | Counter period register |
| TCPWM0_GRP2_CNT4_PERIOD_BUFF | 0x40390224 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT4_DT | 0x40390230 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT4_TR_CMD | 0x40390240 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT4_TR_IN_SEL0 | 0x40390244 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT4_TR_IN_SEL1 | 0x40390248 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT4_TR_IN_EDGE_SEL | 0x4039024C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT4_TR_PWM_CTRL | 0x40390250 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT4_TR_OUT_SEL | 0x40390254 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT4_INTR | 0x40390270 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT4_INTR_SET | 0x40390274 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT4_INTR_MASK | 0x40390278 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT4_INTR_MASKED | 0x4039027C | FULL | Interrupt masked request register |

28.3.6 CNT 5

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT5_CTRL | 0x40390280 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT5_STATUS | 0x40390284 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT5_COUNTER | 0x40390288 | FULL | Counter count register |
| TCPWM0_GRP2_CNT5_CC0 | 0x40390290 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT5_CC0_BUFF | 0x40390294 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT5_CC1 | 0x40390298 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT5_CC1_BUFF | 0x4039029C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT5_PERIOD | 0x403902A0 | FULL | Counter period register |
| TCPWM0_GRP2_CNT5_PERIOD_BUFF | 0x403902A4 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT5_DT | 0x403902B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT5_TR_CMD | 0x403902C0 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT5_TR_IN_SEL0 | 0x403902C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT5_TR_IN_SEL1 | 0x403902C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT5_TR_IN_EDGE_SEL | 0x403902CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT5_TR_PWM_CTRL | 0x403902D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT5_TR_OUT_SEL | 0x403902D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT5_INTR | 0x403902F0 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT5_INTR_SET | 0x403902F4 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT5_INTR_MASK | 0x403902F8 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT5_INTR_MASKED | 0x403902FC | FULL | Interrupt masked request register |

28.3.7 CNT 6

| Register Name | Address | Permission | Description |
|-----------------------|------------|------------|---|
| TCPWM0_GRP2_CNT6_CTRL | 0x40390300 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|--|
| TCPWM0_GRP2_CNT6_STATUS | 0x40390304 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT6_COUNTER | 0x40390308 | FULL | Counter count register |
| TCPWM0_GRP2_CNT6_CC0 | 0x40390310 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT6_CC0_BUFF | 0x40390314 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT6_CC1 | 0x40390318 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT6_CC1_BUFF | 0x4039031C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT6_PERIOD | 0x40390320 | FULL | Counter period register |
| TCPWM0_GRP2_CNT6_PERIOD_BUFF | 0x40390324 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT6_DT | 0x40390330 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT6_TR_CMD | 0x40390340 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT6_TR_IN_SEL0 | 0x40390344 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT6_TR_IN_SEL1 | 0x40390348 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT6_TR_IN_EDGE_SEL | 0x4039034C | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT6_TR_PWM_CTRL | 0x40390350 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT6_TR_OUT_SEL | 0x40390354 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT6_INTR | 0x40390370 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT6_INTR_SET | 0x40390374 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT6_INTR_MASK | 0x40390378 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT6_INTR_MASKED | 0x4039037C | FULL | Interrupt masked request register |

28.3.8 CNT 7

| Register Name | Address | Permission | Description |
|---------------------------------|------------|------------|---|
| TCPWM0_GRP2_CNT7_CTRL | 0x40390380 | FULL | Counter control register Note: AUTO_RELOAD_LINE_SEL CC0_MATCH_UP_EN CC0_MATCH_DOWN_EN CC1_MATCH_UP_EN CC1_MATCH_DOWN_EN are not available for this register |
| TCPWM0_GRP2_CNT7_STATUS | 0x40390384 | FULL | Counter status register Note: DT_CNT_H is not available for this register |
| TCPWM0_GRP2_CNT7_COUNTER | 0x40390388 | FULL | Counter count register |
| TCPWM0_GRP2_CNT7_CC0 | 0x40390390 | FULL | Counter compare/capture 0 register |
| TCPWM0_GRP2_CNT7_CC0_BUFF | 0x40390394 | FULL | Counter buffered compare/capture 0 register |
| TCPWM0_GRP2_CNT7_CC1 | 0x40390398 | FULL | Counter compare/capture 1 register |
| TCPWM0_GRP2_CNT7_CC1_BUFF | 0x4039039C | FULL | Counter buffered compare/capture 1 register |
| TCPWM0_GRP2_CNT7_PERIOD | 0x403903A0 | FULL | Counter period register |
| TCPWM0_GRP2_CNT7_PERIOD_BUFF | 0x403903A4 | FULL | Counter buffered period register |
| TCPWM0_GRP2_CNT7_DT | 0x403903B0 | FULL | Counter PWM dead time register Note: DT_LINE_OUT_H DT_LINE_COMPL_OUT are not available for this register |
| TCPWM0_GRP2_CNT7_TR_CMD | 0x403903C0 | FULL | Counter trigger command register |
| TCPWM0_GRP2_CNT7_TR_IN_SEL0 | 0x403903C4 | FULL | Counter input trigger selection register 0 |
| TCPWM0_GRP2_CNT7_TR_IN_SEL1 | 0x403903C8 | FULL | Counter input trigger selection register 1 |
| TCPWM0_GRP2_CNT7_TR_IN_EDGE_SEL | 0x403903CC | FULL | Counter input trigger edge selection register |
| TCPWM0_GRP2_CNT7_TR_PWM_CTRL | 0x403903D0 | FULL | Counter trigger PWM control register |
| TCPWM0_GRP2_CNT7_TR_OUT_SEL | 0x403903D4 | FULL | Counter output trigger selection register |
| TCPWM0_GRP2_CNT7_INTR | 0x403903F0 | FULL | Interrupt request register |
| TCPWM0_GRP2_CNT7_INTR_SET | 0x403903F4 | FULL | Interrupt set request register |
| TCPWM0_GRP2_CNT7_INTR_MASK | 0x403903F8 | FULL | Interrupt mask register |
| TCPWM0_GRP2_CNT7_INTR_MASKED | 0x403903FC | FULL | Interrupt masked request register |

28.4 Register Details

28.4.1 GRP

28.4.1.1 CNT

28.4.1.1.1 TCPWM_GRP_CNT_CTRL

Description: Counter control register
Address: 0x40380000
Offset: 0x0
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xF0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------------------------|----------------------------------|-------------------------------------|----------------------------------|---------------------------------------|-------------------------------------|--------------------------------|-------------------------------|
| Name | CC1 _MATCH _DOWN _EN [7:7] | CC1 _MATCH _UP_EN [6:6] | CC0 _MATCH _DOWN _EN [5:5] | CC0 _MATCH _UP_EN [4:4] | AUTO _RELOAD _LINE_SEL [3:3] | AUTO _RELOAD _PERIOD [2:2] | AUTO _RELOAD _CC1 [1:1] | AUTO _RELOAD _CC0 [0:0] |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:14] | | PWM_DISABLE_MODE [13:12] | | None [11:11] | PWM _SYNC_ KILL [10:10] | PWM _STOP_ON _KILL [9:9] | PWM_IMM _KILL [8:8] |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:22] | | QUAD_ENCODING _MODE [21:20] | | None [19:19] | ONE _SHOT [18:18] | UP_DOWN_MODE [17:16] | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | ENABLED [31:31] | DBG _FREEZE _EN [30:30] | None [29:27] | | | MODE [26:24] | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|---|
| 0 | AUTO_RELOAD_CC0 | RW | R | 0 | Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0': never switch. '1': switch on a terminal count event with an actively pending switch event. |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------------|----|----|-----------------|--|
| 1 | AUTO_RELOAD_CC1 | RW | R | 0 | Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 1 event. PWM, PWM_DT, PWM_PR modes: '0': never switch. '1': switch on a terminal count event with an actively pending switch event. |
| 2 | AUTO_RELOAD_PERIOD | RW | R | 0 | Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. |
| 3 | AUTO_RELOAD_LINE_SEL | RW | R | 0 | Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with an actively pending switch event. |
| 4 | CC0_MATCH_UP_EN | RW | R | 1 | Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting up '1': compare match 0 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. |
| 5 | CC0_MATCH_DOWN_EN | RW | R | 1 | Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting down '1': compare match 0 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|---|
| 6 | CC1_MATCH_UP_EN | RW | R | 1 | <p>Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode.</p> <p>'0': compare match 1 event generation disabled when counting up '1': compare match 1 event generation enabled when counting up</p> <p>This field has a function in PWM and PWM_DT modes only.</p> |
| 7 | CC1_MATCH_DOWN_EN | RW | R | 1 | <p>Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode.</p> <p>'0': compare match 1 event generation disabled when counting down '1': compare match 1 event generation enabled when counting down</p> <p>This field has a function in PWM and PWM_DT modes only.</p> |
| 8 | PWM_IMM_KILL | RW | R | 0 | <p>Specifies whether the kill event immediately deactivates the 'dt_line_out' and 'dt_line_compl_out' signals or with the next module clock ('active count' pre-scaled 'clk_counter').</p> <p>'0': synchronous kill activation. Deactivates the 'dt_line_out' and 'dt_line_compl_out' signals with the next module clock ('active count' pre-scaled 'clk_counter'). '1': immediate kill activation. Immediately deactivates the 'dt_line_out' and 'dt_line_compl_out' signals.</p> <p>This field has a function in PWM, PWM_DT and PWM_PR modes only.</p> |
| 9 | PWM_STOP_ON_KILL | RW | R | 0 | <p>Specifies whether the counter stops on a kill events:</p> <p>'0': kill event does NOT stop counter. '1': kill event stops counter.</p> <p>This field has a function in PWM, PWM_DT and PWM_PR modes only.</p> |
| 10 | PWM_SYNC_KILL | RW | R | 0 | <p>Specifies asynchronous/synchronous kill behavior:</p> <p>'1': synchronous kill mode: the kill event disables the 'dt_line_out' and 'dt_line_compl_out' signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the 'dt_line_out' and 'dt_line_compl_out' signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET.</p> <p>This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'.</p> |
| 12:13 | PWM_DISABLE_MODE | RW | R | 0 | <p>Specifies the behavior of the PWM outputs 'line_out' and 'line_compl_out' while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped.</p> <p>Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE).</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| | Z | | | 0 | <p>The behavior is the same as in previous mxcpwm (version 1).</p> <p>When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. 'Z' (high impedance). Note: This is realized by driving the TCPWM output 'line_out_en' to 0.</p> <p>When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE).</p> |
| | RETAIN | | | 1 | <p>When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are driven by the TCPWM.</p> <p>When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1).</p> |
| | L | | | 2 | <p>When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are driven by the TCPWM.</p> <p>When the counter is disabled or stopped upon a stop event the PWM output 'line_out' is driven as a fixed '0' and the PWM output 'line_compl_out' is driven as a fixed '1'.</p> |
| | H | | | 3 | <p>When the counter is disabled the PWM outputs 'line_out' and 'line_compl_out' are driven by the TCPWM.</p> <p>When the counter is disabled or stopped upon a stop event the PWM output 'line_out' is driven as a fixed '1' and the PWM output 'line_compl_out' is driven as a fixed '0'.</p> |
| 16:17 | UP_DOWN_MODE | RW | R | 0 | <p>Determines counter direction.</p> <p>In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior.</p> |
| | COUNT_UP | | | 0 | <p>Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD.</p> |
| | COUNT_DOWN | | | 1 | <p>Count down (to '0'). An underflow event is generated when the counter changes from a state in which COUNTER equals '0'. A terminal count event is generated when the counter changes from a state in which COUNTER equals '0'.</p> |
| | COUNT_UPDN1 | | | 2 | <p>Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals '0'. A terminal count event is generated when the counter changes from a state in which COUNTER equals '0'.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------------|----|----|-----------------|--|
| | COUNT_UPDN2 | | | 3 | Count up (to PERIOD), then count down (to '0'). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals '0'. A terminal count event is generated when the counter changes from a state in which COUNTER equals '0' AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates). |
| | QUAD_RANGE0 | | | 0 | <p>In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior:</p> <ul style="list-style-type: none"> - COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32) - on reload / index event: - CC0 is copied to CC0_BUFF - COUNTER is copied to CC0 - COUNTER is set to midpoint (0x8000 / 0x80000000) - tc and cc0_match events are generated - when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF: - CC0 is copied to CC0_BUFF - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0 - COUNTER is set to midpoint (0x8000 / 0x80000000) - cc0_match event is generated <p>This mode is 100 percent backward compatible with previous TCPWM quadrature behavior.</p> |
| | QUAD_RANGE0_CMP | | | 1 | <p>In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior:</p> <ul style="list-style-type: none"> - COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32) - the capture0 event acts as 2nd reload / index event - on reload / index event: - COUNTER is set to midpoint (0x8000 / 0x80000000) - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0): - tc event is generated - PERIOD is copied to PERIOD_BUFF - COUNTER is copied to PERIOD - when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF: - COUNTER is set to midpoint (0x8000 / 0x80000000) - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1): - tc event is generated - PERIOD is copied to PERIOD_BUFF - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD - 1 or 2 compare functions (depending on CC1_PRESENT) available <p>This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.</p> |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------------|----|----|-----------------|---|
| | QUAD_RANGE1_CAPT | | | 2 | <p>In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior:</p> <ul style="list-style-type: none"> - COUNTER range is between 0x0000 and PERIOD - on reload / index event: <ul style="list-style-type: none"> - COUNTER is set to 0x0000 - tc event is generated - when COUNTER is 0x0000 and decrementing: <ul style="list-style-type: none"> - COUNTER is set to PERIOD - tc event is generated - when COUNTER equals PERIOD and is incrementing: <ul style="list-style-type: none"> - COUNTER is set to 0x0000 - tc event is generated - 1 or 2 capture functions (depending on CC1_PRESENT) available - on capture0 / capture1 event: <ul style="list-style-type: none"> - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF - COUNTER value is copied to CC0 <p>This mode is NOT backward compatible with previous TCPWM quadrature behavior. It is to a certain extend compatible with previous Traveo 1 QPRC behavior. It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.</p> |
| | QUAD_RANGE1_CMP | | | 3 | <p>In QUAD mode this setting selects the QUAD_RANGE1_CMP mode.</p> <p>The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.</p> |
| 18 | ONE_SHOT | RW | R | 0 | <p>When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated.</p> |
| 20:21 | QUAD_ENCODING_MODE | RW | R | 0 | <p>In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode.</p> <p>In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert 'dt_line_out' and 'dt_line_compl_out'. Inversion is the last step in generation of 'dt_line_out' and 'dt_line_compl_out'; i.e. a disabled output line 'dt_line_out' has the value QUAD_ENCODING_MODE[0] and a disabled output line 'dt_line_compl_out' has the value QUAD_ENCODING_MODE[1].</p> |
| | X1 | | | 0 | <p>X1 encoding (QUAD mode)</p> <p>This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input).</p> |
| | X2 | | | 1 | X2 encoding (QUAD mode) |
| | X4 | | | 2 | X4 encoding (QUAD mode) |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|--|
| | UP_DOWN | | | 3 | Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply. |
| | INV_OUT | | | 1 | When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts 'dt_line_out' (PWM/PWM_DT modes) |
| | INV_COMPL_OUT | | | 2 | When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts 'dt_line_compl_out' (PWM/PWM_DT modes) |
| 24:26 | MODE | RW | R | 0 | Counter mode. |
| | TIMER | | | 0 | Timer mode |
| | Reserved1 | | | 1 | N/A |
| | CAPTURE | | | 2 | Capture mode |
| | QUAD | | | 3 | Quadrature mode Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality. Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_MODE (overloaded field UP_DOWN_MODE). |
| | PWM | | | 4 | Pulse width modulation (PWM) mode |
| | PWM_DT | | | 5 | PWM with deadtime insertion mode |
| | PWM_PR | | | 6 | Pseudo random pulse width modulation |
| | SR | | | 7 | Shift register mode. |
| 30 | DBG_FREEZE_EN | RW | R | 0 | Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. |
| 31 | ENABLED | RW | R | 0 | Counter Enable '0': counter disabled. '1': counter enabled. Counter static configuration register fields should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ('tr_out0' and tr_out1'). - the counter's line outputs ('line_out' and 'line_compl_out'). The following are Counter static configuration registers: CTRL (with the exception of DEBUG_FREEZE_EN bit), DT, TR_IN_SEL0, TR_IN_SEL1, TR_IN_EDGE_SEL, TR_PWM_CTRL_TR_OUT_SEL, INTR, INTR_MASK, INTR_MASKED Modifying these registers while the counter is running could produce unexcepted waveform results, but will not cause a fatal issue such as an illegal stop, lost control, or waveform stability issues. |

28.4.1.1.2 TCPWM_GRP_CNT_STATUS

Description: Counter status register

Address: 0x40380004

Offset: 0x4

Retention: Not Retained

IsDeepSleep: No

Comment: When the counter is disabled (CTRL.ENABLED = 0), then the STATUS.TR_* bit fields are typically reset to their default values. However, there are exceptions possible in the following cases, based on the selected input trigger via TR_IN_SEL*._SEL:

- If a constant '0' is selected, then a '0' is read.
- If a constant '1' is selected, then a '1' is read.
- If a general purpose trigger input 'tr_all_cnt_in' is selected which is also selected by another counter and that counter is enabled, then the actual level of the selected trigger is read.

Default: 0x20

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|-----------------|----------------|-------------------|------------|---|---|------------|
| Name | TR_STOP [7:7] | TR_RELOAD [6:6] | TR_COUNT [5:5] | TR_CAPTURE0 [4:4] | None [3:1] | | | DOWN [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------------|--------------|----|----|------------------------|------------------|-------------------|----------------|
| Name | RUNNING [15:15] | None [14:12] | | | LINE_COMPL_OUT [11:11] | LINE_OUT [10:10] | TR_CAPTURE1 [9:9] | TR_START [8:8] |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------------|----|----|----|----|----|----|----|
| Name | DT_CNT_L [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | DT_CNT_H [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|---|
| 0 | DOWN | R | RW | 0 | When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. |
| 4 | TR_CAPTURE0 | R | RW | 0 | Indicates the actual level of the selected capture 0 trigger. |
| 5 | TR_COUNT | R | RW | 1 | Indicates the actual level of the selected count trigger. |
| 6 | TR_RELOAD | R | RW | 0 | Indicates the actual level of the selected reload trigger. |
| 7 | TR_STOP | R | RW | 0 | Indicates the actual level of the selected stop trigger. |
| 8 | TR_START | R | RW | 0 | Indicates the actual level of the selected start trigger. |
| 9 | TR_CAPTURE1 | R | RW | 0 | Indicates the actual level of the selected capture 1 trigger. |
| 10 | LINE_OUT | R | RW | 0 | Indicates the actual level of the PWM line output signal. |
| 11 | LINE_COMPL_OUT | R | RW | 0 | Indicates the actual level of the complementary PWM line output signal. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 15 | RUNNING | R | RW | 0 | <p>When '0', the counter is NOT running. When '1', the counter is running.</p> <p>This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event.</p> <p>When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'.</p> |
| 16:23 | DT_CNT_L | R | RW | 0 | <p>Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality.</p> |
| 24:31 | DT_CNT_H | R | RW | 0 | <p>High byte of 16-bit dead time counter. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this field has no effect.</p> <p>Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8bit wide and the only the field DT_CNT_L is used as dead time counter.</p> |

28.4.1.1.3 TCPWM_GRP_CNT_COUNTER

Description: Counter count register
Address: 0x40380008
Offset: 0x8
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | COUNTER [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|----------------|----|----|----|----|----|---|---|
| Name | COUNTER [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | COUNTER [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | COUNTER [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------|----|----|-----------------|--|
| 0:31 | COUNTER | RW | RW | 0 | 16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. |

28.4.1.1.4 TCPWM_GRP_CNT_CC0

Description: Counter compare/capture 0 register
Address: 0x40380010
Offset: 0x10
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CC | RW | RW | 4294967295 | In CAPTURE mode, captures the counter value. In other modes, compared to counter value. |

28.4.1.1.5 TCPWM_GRP_CNT_CC0_BUFF

Description: Counter buffered compare/capture 0 register
Address: 0x40380014
Offset: 0x14
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|--|
| 0:31 | CC | RW | RW | 4294967295 | Additional buffer for counter CC register. |

28.4.1.1.6 TCPWM_GRP_CNT_CC1

Description: Counter compare/capture 1 register
Address: 0x40380018
Offset: 0x18
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CC | RW | RW | 4294967295 | In CAPTURE mode, captures the counter value. In other modes, compared to counter value. |

28.4.1.1.7 TCPWM_GRP_CNT_CC1_BUFF

Description: Counter buffered compare/capture 1 register
Address: 0x4038001C
Offset: 0x1C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | CC [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----------|----|----|----|----|----|---|---|
| Name | CC [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------|----|----|----|----|----|----|----|
| Name | CC [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|------|----|----|-----------------|---|
| 0:31 | CC | RW | RW | 4294967295 | Additional buffer for counter CC1 register. |

28.4.1.1.8 TCPWM_GRP_CNT_PERIOD

Description: Counter period register
Address: 0x40380020
Offset: 0x20
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | PERIOD [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PERIOD [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PERIOD [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PERIOD [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|--|
| 0:31 | PERIOD | RW | RW | 4294967295 | Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. |

28.4.1.1.9 TCPWM_GRP_CNT_PERIOD_BUFF

Description: Counter buffered period register
Address: 0x40380024
Offset: 0x24
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0xFFFFFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|----|----|----|----|----|----|----|
| Name | PERIOD [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | PERIOD [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PERIOD [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PERIOD [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------|----|----|-----------------|---|
| 0:31 | PERIOD | RW | RW | 4294967295 | <p>Additional buffer for counter PERIOD register.</p> <p>In PWM_PR mode PERIOD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree.</p> <p>Examples for GRP_CNT_WIDTH = 16:</p> <ul style="list-style-type: none"> - Maximum length 16bit LFSR - polynomial $x^{16} + x^{14} + x^{13} + x^{11} + 1$ - taps 0,2,3,5 -> PERIOD = 0x002d - period is $2^{16}-1 = 65535$ cycles - Maximum length 8bit LFSR: - polynomial $x^8 + x^6 + x^5 + x^4 + 1$ - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is $2^8-1 = 255$ cycles <p>In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined.</p> |

28.4.1.1.10 TCPWM_GRP_CNT_LINE_SEL

Description: Counter line selection register
Address: 0x40380028
Offset: 0x28
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x32

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---------------------|---|---|------------|---------------|---|---|
| Name | None [7:7] | COMPL_OUT_SEL [6:4] | | | None [3:3] | OUT_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:2 | OUT_SEL | RW | RW | 2 | <p>Selects the source for the output signal 'line_out'. Default setting is the PWM signal 'line'. Other settings are useful for Stepper Motor Control. This field has a function in PWM and PWM_PR modes only.</p> <p>Note: The output signal of this selection can be further modified by the stop / kill logic and line_out polarity setting (CTRL.QUAD_ENCODING_MODE[0]).</p> |
| | L | | | 0 | fixed '0' |
| | H | | | 1 | fixed '1' |
| | PWM | | | 2 | PWM signal 'line' |
| | PWM_INV | | | 3 | inverted PWM signal 'line' |
| | Z | | | 4 | <p>The output 'line_out' is not driven by the TCPWM. Instead the port default level configuration applies, e.g. 'Z' (high impedance).</p> <p>Note: This is realized by driving the output 'line_out_en' to 0.</p> |
| | Reserved5 | | | 5 | N/A |
| | Reserved6 | | | 6 | N/A |
| | Reserved7 | | | 7 | N/A |
| 4:6 | COMPL_OUT_SEL | RW | RW | 3 | <p>Selects the source for the output signal 'line_compl_out'. Default setting is the inverted PWM signal 'line'. Other settings are useful for Stepper Motor Control. This field has a function in PWM and PWM_PR modes only.</p> <p>Note: The output signal of this selection can be further modified by the stop / kill logic and line_compl_out polarity setting (CTRL.QUAD_ENCODING_MODE[1]).</p> |
| | L | | | 0 | fixed '0' |
| | H | | | 1 | fixed '1' |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|--|
| | PWM | | | 2 | PWM signal 'line' |
| | PWM_INV | | | 3 | inverted PWM signal 'line' |
| | Z | | | 4 | The output 'line_compl_out' is not driven by the TCPWM. Instead the port default level configuration applies, e.g. 'Z' (high impedance). Note: This is realized by driving the output 'line_compl_out_en' to 0. |
| | Reserved5 | | | 5 | N/A |
| | Reserved6 | | | 6 | N/A |
| | Reserved7 | | | 7 | N/A |
| | | | | | |

28.4.1.1.11 TCPWM_GRP_CNT_LINE_SEL_BUFF

Description: Counter buffered line selection register
Address: 0x4038002C
Offset: 0x2C
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x32

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---------------------|---|---|------------|---------------|---|---|
| Name | None [7:7] | COMPL_OUT_SEL [6:4] | | | None [3:3] | OUT_SEL [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|---|
| 0:2 | OUT_SEL | RW | RW | 2 | <p>Buffer for LINE_SEL.OUT_SEL. Can be exchanged with LINE_SEL.LINE_OUT_SEL on a terminal count event with an actively pending switch event.</p> <p>This field has a function in PWM and PWM_PR modes only.</p> |
| 4:6 | COMPL_OUT_SEL | RW | RW | 3 | <p>Buffer for LINE_SEL.COMPL.OUT_SEL. Can be exchanged with LINE_SEL.LINE_COMPL_OUT_SEL on a terminal count event with an actively pending switch event.</p> <p>This field has a function in PWM and PWM_PR modes only.</p> |

28.4.1.1.12 TCPWM_GRP_CNT_DT

Description: Counter PWM dead time register
Address: 0x40380030
Offset: 0x30
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------------------|----|----|----|----|----|----|----|
| Name | DT_LINE_OUT_L [7:0] | | | | | | | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | DT_LINE_OUT_H [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | DT_LINE_COMPL_OUT [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | DT_LINE_COMPL_OUT [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| 0:7 | DT_LINE_OUT_L | RW | R | 0 | In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal 'line_out': amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating 'line_out' when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating 'line_out' and 'line_compl_out'. |
| | DIVBY1 | | | 0 | Divide by 1 (other-than-PWM_DT mode) |
| | DIVBY2 | | | 1 | Divide by 2 (other-than-PWM_DT mode) |
| | DIVBY4 | | | 2 | Divide by 4 (other-than-PWM_DT mode) |
| | DIVBY8 | | | 3 | Divide by 8 (other-than-PWM_DT mode) |
| | DIVBY16 | | | 4 | Divide by 16 (other-than-PWM_DT mode) |
| | DIVBY32 | | | 5 | Divide by 32 (other-than-PWM_DT mode) |
| | DIVBY64 | | | 6 | Divide by 64 (other-than-PWM_DT mode) |
| | DIVBY128 | | | 7 | Divide by 128 (other-than-PWM_DT mode) |
| 8:15 | DT_LINE_OUT_H | RW | R | 0 | In PWM_DT mode, this field is used to determine the high byte of the dead time before activating the PWM line output signal 'line_out': amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating 'line_out' and 'line_compl_out'. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|-------------------|----|----|-----------------|--|
| 16:31 | DT_LINE_COMPL_OUT | RW | R | 0 | <p>In PWM_DT mode, this field is used to determine the dead time before activating the complementary PWM line output signal 'line_compl_out': amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect.</p> <p>Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating 'line_out' and 'line_compl_out'.</p> |

28.4.1.1.13 TCPWM_GRP_CNT_TR_CMD

Description: Counter trigger command register
Address: 0x40380040
Offset: 0x40
Retention: Not Retained
IsDeepSleep: No
Comment: Enables software controlled operation for this counter.
Note: Synchronized operation on multiple counters can be done using trigger multipliers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|----------------|-------------|------------|--------------|------------|----------------|
| Name | None [7:6] | | CAPTURE1 [5:5] | START [4:4] | STOP [3:3] | RELOAD [2:2] | None [1:1] | CAPTURE0 [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------|------|------|-----------------|--|
| 0 | CAPTURE0 | RW1S | RW1C | 0 | SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. |
| 2 | RELOAD | RW1S | RW1C | 0 | SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. |
| 3 | STOP | RW1S | RW1C | 0 | SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. |
| 4 | START | RW1S | RW1C | 0 | SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. |
| 5 | CAPTURE1 | RW1S | RW1C | 0 | SW capture 1 trigger. For HW behavior, see COUNTER_CAPTURE0 field. |

28.4.1.1.14 TCPWM_GRP_CNT_TR_IN_SEL0

Description: Counter input trigger selection register 0
Address: 0x40380044
Offset: 0x44
Retention: Retained
IsDeepSleep: No
Comment: Used to select triggers for specific counter events.
Default: 0x100

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------------|---|---|---|---|---|---|---|
| Name | CAPTURE0_SEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|------------------|----|----|----|----|----|---|---|
| Name | COUNT_SEL [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------------|----|----|----|----|----|----|----|
| Name | RELOAD_SEL [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------------------|----|----|----|----|----|----|----|
| Name | STOP_SEL [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|--------------|----|----|-----------------|---|
| 0:7 | CAPTURE0_SEL | RW | R | 0 | Selects one of the up to 256 input triggers as a capture0 trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. If existing, the one-to-one trigger inputs 'tr_one_cnt_in' (different to each counter) are selected by setting 2 and above. The settings above are used for the general purpose trigger inputs 'tr_all_cnt_in' connected to all counters selected. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. |
| 8:15 | COUNT_SEL | RW | R | 1 | Selects one of the 256 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Note: In the modes: TIMER, CAPTURE, PWM, PWM_DT, and SR, If the counter is externally triggered (COUNT_SEL > 1), an external trigger will be required for each TR_CMD to execute. For example, a write to TR_CMD.START will not start the counter until the trigger selected by COUNT_SEL asserts. The next trigger will increment the counter since the counter is now running. This goes for all TR_CMD fields. |
| 16:23 | RELOAD_SEL | RW | R | 0 | Selects one of the 256 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In these modes, it will update the counter with 0x8000 (counter midpoint) or 0x0000 depending on the QUAD_RANGE_MODE. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|----------|----|----|-----------------|--|
| 24:31 | STOP_SEL | RW | R | 0 | Selects one of the 256 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. |

28.4.1.1.15 TCPWM_GRP_CNT_TR_IN_SEL1

Description: Counter input trigger selection register 1
Address: 0x40380048
Offset: 0x48
Retention: Retained
IsDeepSleep: No
Comment: Used to select triggers for specific counter events.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | START_SEL [7:0] | | | | | | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|---------------------|----|----|----|----|----|---|---|
| Name | CAPTURE1_SEL [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|--------------|----|----|-----------------|---|
| 0:7 | START_SEL | RW | R | 0 | Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). |
| 8:15 | CAPTURE1_SEL | RW | R | 0 | Selects one of the 256 input triggers as a capture 1 trigger. |

28.4.1.1.16 TCPWM_GRP_CNT_TR_IN_EDGE_SEL

Description: Counter input trigger edge selection register
Address: 0x4038004C
Offset: 0x4C
Retention: Retained
IsDeepSleep: No
Comment: Used to determine edge detection for specific counter triggers. Events will only take effect on enabled counters.
Default: 0xFFFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|----|-------------------|----|-----------------------|----|---------------------|----|
| Name | STOP_EDGE [7:6] | | RELOAD_EDGE [5:4] | | COUNT_EDGE [3:2] | | CAPTURE0_EDGE [1:0] | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:12] | | | | CAPTURE1_EDGE [11:10] | | START_EDGE [9:8] | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|---------------|----|----|-----------------|--|
| 0:1 | CAPTURE0_EDGE | RW | R | 3 | A capture 0 event will copy the counter value into the CC0 register. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 2:3 | COUNT_EDGE | RW | R | 3 | A counter event will increase or decrease the counter by '1'. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 4:5 | RELOAD_EDGE | RW | R | 3 | A reload event will initialize the counter. When counting up, the counter is initialized to '0'. When counting down, the counter is initialized with PERIOD. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 6:7 | STOP_EDGE | RW | R | 3 | A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |

| Bits | Name | SW | HW | Default or Enum | Description |
|-------|---------------|----|----|-----------------|--|
| 8:9 | START_EDGE | RW | R | 3 | A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |
| 10:11 | CAPTURE1_EDGE | RW | R | 3 | A capture 1 event will copy the counter value into the CC1 register. |
| | RISING_EDGE | | | 0 | Rising edge. Any rising edge generates an event. |
| | FALLING_EDGE | | | 1 | Falling edge. Any falling edge generates an event. |
| | ANY_EDGE | | | 2 | Rising AND falling edge. Any odd amount of edges generates an event. |
| | NO_EDGE_DET | | | 3 | No edge detection, use trigger as is. |

28.4.1.1.17 TCPWM_GRP_CNT_TR_PWM_CTRL

Description: Counter trigger PWM control register
Address: 0x40380050
Offset: 0x50
Retention: Retained
IsDeepSleep: No
Comment: Used to control counter 'line_out', 'dt_line_out' and 'dt_line_compl_out' output signals.
Default: 0xFF

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|----|----------------------|----|---------------------|----|----------------------|----|
| Name | CC1_MATCH_MODE [7:6] | | UNDERFLOW_MODE [5:4] | | OVERFLOW_MODE [3:2] | | CC0_MATCH_MODE [1:0] | |
| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Name | None [15:8] | | | | | | | |
| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | None [23:16] | | | | | | | |
| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|----------------|----|----|-----------------|--|
| 0:1 | CC0_MATCH_MODE | RW | R | 3 | Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the 'line_out' output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0 percent, the counter CC0 register should be set to '0'. For a 100 percent duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |
| | NO_CHANGE | | | 3 | No Change |
| 2:3 | OVERFLOW_MODE | RW | R | 3 | Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the 'line_out' output signals. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |
| | NO_CHANGE | | | 3 | No Change |
| 4:5 | UNDERFLOW_MODE | RW | R | 3 | Determines the effect of a counter underflow event (COUNTER reaches '0') on the 'line_out' output signals. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |
| | NO_CHANGE | | | 3 | No Change |
| 6:7 | CC1_MATCH_MODE | RW | R | 3 | Determines the effect of a compare match 1 event (COUNTER equals CC1 register) on the 'line_out' output signals. |
| | SET | | | 0 | Set to '1' |
| | CLEAR | | | 1 | Set to '0' |
| | INVERT | | | 2 | Invert |

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|-------------|
| | NO_CHANGE | | | 3 | No Change |

28.4.1.1.18 TCPWM_GRP_CNT_TR_OUT_SEL

Description: Counter output trigger selection register
Address: 0x40380054
Offset: 0x54
Retention: Retained
IsDeepSleep: No
Comment: Used to select internal events for output trigger generation.
Default: 0x32

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|------------|---|---|------------|------------|---|---|
| Name | None [7:7] | OUT1 [6:4] | | | None [3:3] | OUT0 [2:0] | | |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0:2 | OUT0 | RW | R | 2 | Selects one of the internal events to generate the output trigger 0. Default setting selects the terminal count event. |
| | OVERFLOW | | | 0 | Overflow event |
| | UNDERFLOW | | | 1 | Underflow event |
| | TC | | | 2 | Terminal count event (default selection) |
| | CC0_MATCH | | | 3 | Compare match 0 event |
| | CC1_MATCH | | | 4 | Compare match 1 event |
| | LINE_OUT | | | 5 | PWM output signal 'line_out' |
| | Reserved6 | | | 6 | N/A |
| 4:6 | OUT1 | RW | R | 3 | Selects one of the internal events to generate the output trigger 1. Default setting selects the compare match 0 event. |
| | OVERFLOW | | | 0 | Overflow event |
| | UNDERFLOW | | | 1 | Underflow event |
| | TC | | | 2 | Terminal count event |
| | CC0_MATCH | | | 3 | Compare match 0 event (default selection) |
| | CC1_MATCH | | | 4 | Compare match 1 event |
| | LINE_OUT | | | 5 | PWM output signal 'line_out' |
| | Reserved6 | | | 6 | N/A |
| | Disabled | | | 7 | Output trigger disabled. |

28.4.1.1.19 TCPWM_GRP_CNT_INTR

Description: Interrupt request register
Address: 0x40380070
Offset: 0x70
Retention: Not Retained
IsDeepSleep: No
Comment: The register fields are not retained. This is to ensure that they come up as '0' after coming out of DeepSleep system power mode. HW clears the interrupt causes to '0', when the counter is disabled.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|-----------------|----------|
| Name | None [7:3] | | | | | CC1_MATCH [2:2] | CC0_MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|------|------|-----------------|--|
| 0 | TC | RW1C | RW1S | 0 | Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. |
| 1 | CC0_MATCH | RW1C | RW1S | 0 | Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. |
| 2 | CC1_MATCH | RW1C | RW1S | 0 | Counter matches CC1 register event. Set to '1', when event is detected. Write with '1' to clear bit. |

28.4.1.1.20 TCPWM_GRP_CNT_INTR_SET

Description: Interrupt set request register
Address: 0x40380074
Offset: 0x74
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects the interrupt request register.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|-----------------|----------|
| Name | None [7:3] | | | | | CC1_MATCH [2:2] | CC0_MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|------|----|-----------------|--|
| 0 | TC | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 1 | CC0_MATCH | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |
| 2 | CC1_MATCH | RW1S | A | 0 | Write with '1' to set corresponding bit in interrupt request register. |

28.4.1.1.21 TCPWM_GRP_CNT_INTR_MASK

Description: Interrupt mask register
Address: 0x40380078
Offset: 0x78
Retention: Retained
IsDeepSleep: No
Comment:
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|-----------------|----------|
| Name | None [7:3] | | | | | CC1_MATCH [2:2] | CC0_MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0 | TC | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 1 | CC0_MATCH | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |
| 2 | CC1_MATCH | RW | R | 0 | Mask bit for corresponding bit in interrupt request register. |

28.4.1.1.22 TCPWM_GRP_CNT_INTR_MASKED

Description: Interrupt masked request register
Address: 0x4038007C
Offset: 0x7C
Retention: Not Retained
IsDeepSleep: No
Comment: When read, this register reflects a bitwise AND between the interrupt request and mask registers.
Default: 0x0

Bit-field Table

| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------|---|---|---|---|-----------------|-----------------|----------|
| Name | None [7:3] | | | | | CC1_MATCH [2:2] | CC0_MATCH [1:1] | TC [0:0] |

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-------------|----|----|----|----|----|---|---|
| Name | None [15:8] | | | | | | | |

| Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [23:16] | | | | | | | |

| Bits | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|--------------|----|----|----|----|----|----|----|
| Name | None [31:24] | | | | | | | |

Bit-fields

| Bits | Name | SW | HW | Default or Enum | Description |
|------|-----------|----|----|-----------------|---|
| 0 | TC | R | W | 0 | Logical and of corresponding request and mask bits. |
| 1 | CC0_MATCH | R | W | 0 | Logical and of corresponding request and mask bits. |
| 2 | CC1_MATCH | R | W | 0 | Logical and of corresponding request and mask bits. |

References

- [1] 002-19314: TRAVEO™ T2G Automotive MCU body controller entry architecture technical reference manual.

Revision history

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|---|
| ** | 2020-03-05 | <p>Features:</p> <ol style="list-style-type: none"> 1. Extensive search options using address or register or bit fields. Search option is supported for "Registers", register "Addresses" and register "Bit Fields" using prefixes "reg:" or "add:" or "bit:" respectively. 2. Buttons "Home", and "Up" included. 3. Register Structure with links, all homepage notes are moved down. 4. Some fixes which were present in the previous revision in spec system. Missing contents due to parser errors (CDT#343334). 5. Print options for the selected registers. 6. HTML is supported only on Chrome, Mozilla Firefox, Opera, UC Browser and Microsoft Edge browsers. (No support for any other OS/Mobiles etc.) 7. Issue of content overlap while re-sizing after "restore down" option is fixed. <p>Known Issues:</p> <ol style="list-style-type: none"> 1. Whole HTML print option not available. |
| *A | 2020-08-07 | <ol style="list-style-type: none"> 1. Based on Rev_A of Silicon tape out. 2. SW Access note enhanced. 3. Added HW access note for registers behavior. |
| *B | 2020-04-18 | PR4 release |

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